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A Multilevel Energy Buffer and Voltage Modulator for Grid-Interfaced Micro-Inverters

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***Abstract*—Micro-inverters operating into the single-phase grid from solar photovoltaic (PV) panels or other low-voltage sources must buffer the twice-line-frequency variations between the energy sourced by the PV panel and that required for the grid. Moreover, in addition to operating over wide average power ranges, they inherently operate over a wide range of voltage conversion ratios as the line voltage traverses a cycle. These factors make the design of micro-inverters challenging. This paper presents a multilevel energy buffer and voltage modulator (MEB) that significantly reduces the range of voltage conversion ratios that the dc-ac converter portion of the micro-inverter must operate over by stepping its effective input voltage in pace with the line voltage. The MEB also functions as an active energy buffer to reduce the twice-line-frequency voltage ripple at the output of the solar panel. The small additional loss of the MEB can be compensated by the improved efficiency of the dc-ac converter stage, leading to a higher overall system efficiency. A prototype micro-inverter incorporating a MEB, designed for 27 V to 38 V dc input voltage, 230 V rms ac output voltage, and rated for line cycle average power of 70 W, has been built and tested in grid-connected mode. It is shown that the MEB can successfully enhance the performance of a single-phase grid-interfaced micro-inverter by increasing its efficiency and reducing the total size of the twice-line-frequency energy buffering capacitance.**

I. Introduction

In large-scale solar photovoltaic (PV) installations, multiple PV modules (panels) are connected to the electric grid through a single high-power inverter. However, for smaller residential and commercial applications, PV micro-inverters are attractive and are a focus of extensive research in both academia and industry. Each micro-inverter directly connects one PV module to the grid, hence enabling higher overall maximum power point tracking (MPPT) efficiency and improved system reliability by eliminating the potential single point of failure [1]–[8]. Two important considerations in the design of micro-inverters are converter efficiency and size. The size of the micro-inverter can be reduced by increasing its switching frequency. However, to maintain or enhance efficiency at the higher switching frequencies, advanced topologies and control strategies are necessary.

One attractive architecture for micro-inverters is shown in Fig. 1 [4], [5]. It comprises a high frequency resonant inverter, a transformer, and a cycloconverter. The resonant inverter is controlled in such a manner that it produces a high-frequency-sinusoidal current with its amplitude modulated at the line-frequency (60 Hz in the US). The high frequency transformer steps up the voltage, and the cycloconverter converts the high frequency current into a sinusoidal line-frequency current, which is injected into the grid. Output power can be controlled by a combination of frequency control and phase-shift control. Twice-line-frequency energy buffering in the circuit of Fig. 1 - and in many other micro-inverter architectures - is provided by the input capacitor, C_{IN}, though other methods are possible (e.g., [3], [6]–[8]). Related micro-inverter architectures likewise incorporate a high-frequency inverter and step-up transformation, with subsequent transformation of energy to the line voltage. However, all such architectures must buffer twice-line-frequency energy and must vary the amplitude of the high frequency output current across a very wide range (e.g., in proportion to the line voltage and the average power delivered by the inverter), posing design and control challenges. For example, if frequency control alone is used to control the amplitude of the output current, the required frequency range can be very wide, reducing efficiency. Hence, there is an evident need for micro-inverter circuit designs and associated controls that can provide improved performance for operating over wide output voltages and power ranges while providing buffering for twice-line-frequency power variations.

The challenges faced by micro-inverters - wide operating voltage and power ranges and the need to buffer line-frequency energy - also exist in other single-phase grid-interfaced dc-ac converters. Many approaches have been employed to handle twice-line-frequency energy concerns, including energy buffers interfaced within the high-frequency portion of the inverter system [6]–[8], "dc" interface energy buffers that have wider operating range than simple capacitors placed across the panel or elsewhere [9]–[13], and active power filters placed on the ac side of the system [14], among other approaches. To reduce the required operating ranges of the high-frequency parts of the system, cascaded power stages (such as variable switched-capacitor stages) have sometimes been employed (e.g., [15], [16]).

In this paper we introduce a new technique to address the above-mentioned challenges. The new technique shares some of the benefits of both variable-topology cascade converter structures [16] and switched-capacitor energy buffers [12], [13], while enabling very high efficiency to be maintained. The new power converter architecture incorporates a Multilevel Energy Buffer and Voltage Modulator (MEB) to achieve

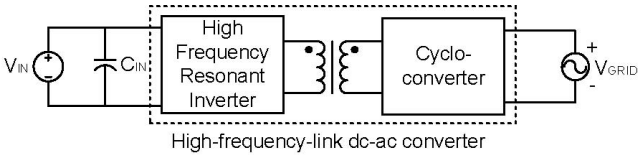


Fig. 1. Architecture of a micro-inverter incorporating a twice-line-frequency energy buffer capacitance, C_{IN}, a high-frequency resonant inverter, a transformer and cycloconverter.

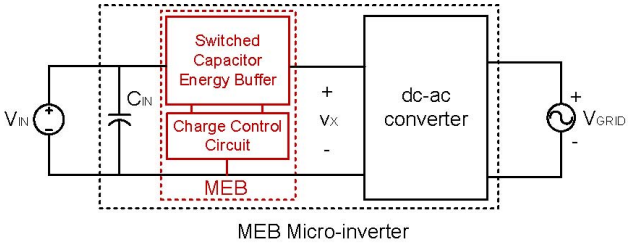


Fig. 2. Architecture of the proposed micro-inverter. It incorporates a Multilevel Energy Buffer and Voltage Modulator (MEB).

compression of the high-frequency inverter operating range, thereby improving the efficiency of the high-frequency-link dc-ac converter stage. The MEB also provides twice-line-frequency energy buffering between dc and ac. The remainder of this paper is organized as follows: Section II describes the overall architecture of the proposed MEB micro-inverter. A specific implementation of the MEB micro-inverter and its design methodology is described in section III. Section III also discusses the expected efficiency benefits of this implementation. The design details of a prototype MEB micro-inverter are given in section IV. Section V presents the experimental results of the MEB micro-inverter tested while connected to the grid. Finally, conclusions are presented in section VI.

II. Architecture of the Proposed MEB Micro-inverter

The architecture of the proposed MEB micro-inverter is shown in Fig. 2. The MEB is connected in cascade between the input capacitor and a dc-ac converter block. The MEB comprises a Switched-Capacitor Energy Buffer (SCEB) and an optional Charge Control Circuit (CCC). The SCEB is used to modulate the dc-ac converter block's input voltage, v_X, as the line voltage traverses a cycle to reduce the required amount and variations in voltage conversion ratio of the high-frequency dc-ac converter block over the line cycle. Consequently, the operating range of the high-frequency, high-step-up portion of the micro-inverter is reduced. The SCEB also functions as an active energy buffer and helps to reduce the total energy storage requirement for twice-line-frequency energy buffering by separating the energy buffer voltage from the input (panel) voltage. Since the capacitor(s) in the SCEB can be charged over a wider range than is permissible for a buffer capacitor across the panel output, the required total energy storage (and capacitor size) can be reduced. This represents a form of third-port energy buffering [2], [3], [6]–[8], providing active control of the energy storage stage, independent of the input and output voltages. The switches in the SCEB switch at low multiples of the line frequency, allowing the SCEB to be highly efficient. The SCEB also steps up the voltage on the primary side of the transformer. Hence, it reduces the transformer primary-side current and the primary-side conduction losses.

The optional charge control circuit (CCC) provides an additional means to balance the total charge entering and leaving the SCEB over a line cycle, thereby providing greater flexibility in the operation of the SCEB. The power rating of the CCC is a fraction of the power rating of the MEB micro-inverter, and it only operates over part of the line cycle. Hence, it can be small and its losses do not substantially impact the overall efficiency of the micro-inverter. The small additional loss of the MEB can be compensated by the improved efficiency of the dc-ac converter block, leading to a higher overall system efficiency.

Although in this paper we present the use of the MEB in the context of a micro-inverter, this MEB based architecture can be applied more broadly to converters interfacing between low-voltage dc and the single-phase ac grid.

III. Design of An Example MEB Micro-inverter

There are many possible implementations of the proposed MEB micro-inverter and the MEB itself, allowing trade-offs to be made between complexity and performance. In this section we describe an example MEB micro-inverter implementation and its design methodology. The full system is shown in Fig. 3. It consists of two parts: a MEB and a dc-ac converter stage. The dc-ac converter stage considered in this paper is a high-frequency-link converter, incorporating a series resonant inverter operated under a combination of frequency and phase-shift control. The full system also includes a line angle detector circuit and a micro-controller (MCU). We first discuss the design methodology of the MEB, and then the high-frequency dc-ac converter stage.

A. Design of the MEB

One implementation of the MEB is shown in Fig. 4a. The MEB has two subsystems: a Switched-Capacitor Energy Buffer (SCEB) and an associated charge-control circuit (CCC). The SCEB comprises four switches, connected as a full bridge, and one buffer capacitor C_{BUF}. The switches of the SCEB change state at line angles α, β, $(180^\circ - \beta)$ and $(180^\circ - \alpha)$ to generate the dc-ac converter input voltage v_X shown in Fig. 4b. When the magnitude of the line voltage, $|v_{GRID}|$, is low (corresponding to $\theta \in [0^\circ, \alpha] \cup [180^\circ - \alpha, 180^\circ]$, i.e., line angles in the range 0° to α and $180^\circ - \alpha$ to 180°), the SCEB operates in the Step-down Mode with S_a and S_d on (S_b and S_c off) and $v_X = V_{IN} - v_{BUF}$; when $|v_{GRID}|$ is in the mid-range ($\theta \in [\alpha, \beta] \cup [180^\circ - \beta, 180^\circ - \alpha]$), the SCEB operates in the Bypass Mode (S_a, S_b on) and $v_X = V_{IN}$; and when $|v_{GRID}|$ is high ($\theta \in [\beta, 180^\circ - \beta]$), the SCEB operates in the Step-up Mode (S_b, S_c on) and $v_X = V_{IN} + v_{BUF}$. In Fig. 4b and the

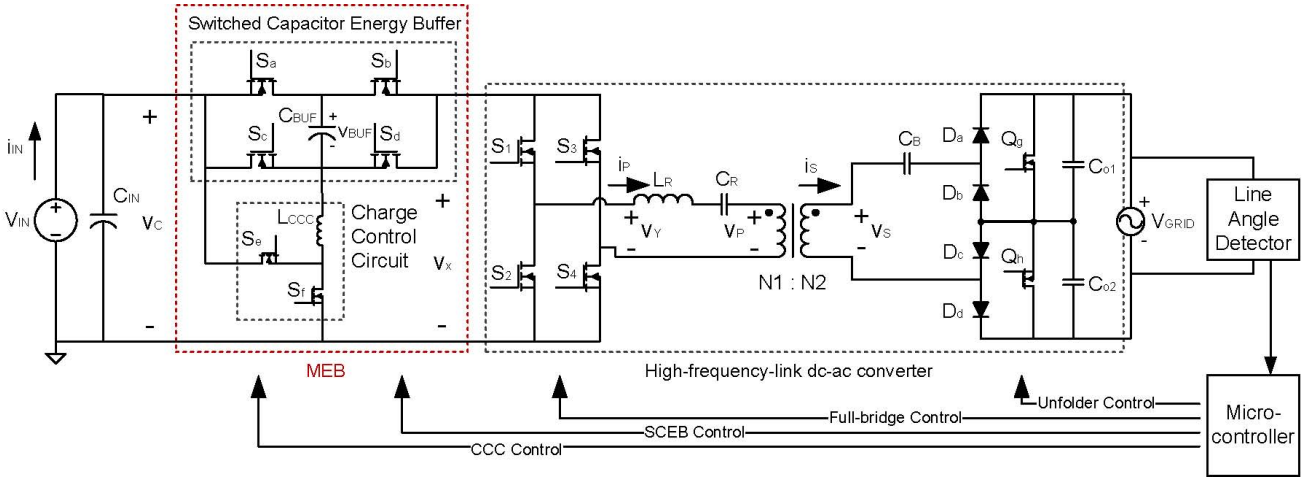
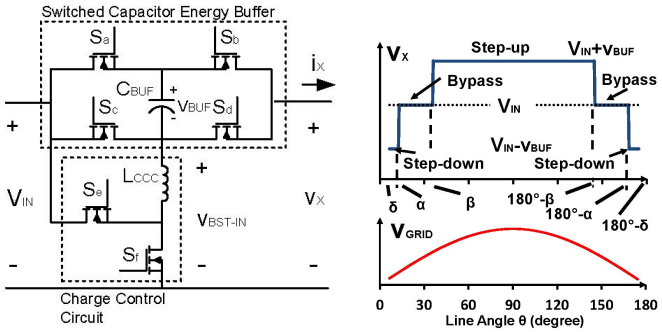
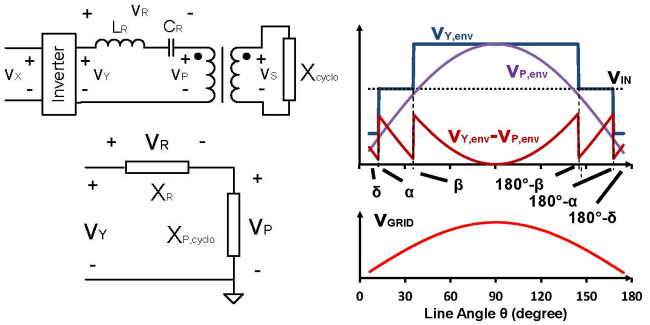


Fig. 3. One implementation of the MEB micro-inverter.



(a) (b)

Fig. 4. One embodiment of the proposed MEB: (a) MEB circuit implementation, and (b) waveform of v_{X} relative to v_{GRID} during a half line-cycle.



(a) (b)

Fig. 5. (a) Model of the dc-ac converter stage. Here $\mathrm{X_R}$ is the impedance of the resonant tank, $\mathrm{X_{cyclo}}$ is the impedance of the cycloconverter (rectifier/unfolder), and $\mathrm{X_{P,cyclo}}$ is the impedance of the cycloconverter reflected to the primary side of the transformer. (b) Waveforms of the envelope of v_{Y}, v_{P} ,$v_{\mathrm{Y}} - v_{\mathrm{P}}$ and v_{GRID} relative to the line voltage during a half line-cycle.

following analysis, $\mathrm{C_{BUF}}$ is assumed to be large enough that v_{BUF} does not vary significantly over a line cycle. With the SCEB operated in this manner, v_{X} is modulated in pace with the line voltage, yielding a significantly compressed range of voltage conversion ratios for the high-frequency inverter. The three SCEB modes repeat periodically every half-line cycle. Each switch changes state twice in each half-line cycle, leading to low switching loss of the SCEB.

Note that in Fig. 4b, v_{X} is not specified for line angles close to the zero crossings of the line. At the zero crossings of the line voltage (i.e., when $\theta = 0°$ and $\theta = 180°$), the output current needs to be zero to achieve a perfect power factor. This is practically unachievable under continuous modulation of the converter. To limit the operating frequency range of the dc-ac converter block, a dead-angle, δ, of several degrees is introduced before and after the zero-crossings of the line voltage, during which time the micro-inverter is shut-off and no current is injected into the grid. In this paper, a δ of 6° is selected.

The design of the MEB involves selecting optimal values for the three design parameters: v_{BUF}, α and β, so as to achieve the maximum reduction in dc-ac converter block's operating range. To minimize this operating range we must minimize the maximum voltage drop across the resonant tank, v_{R}, over the line cycle. This is equivalent to minimizing the difference between the envelope of the high frequency output voltage of the full bridge, $v_{\mathrm{Y,env}}$, and the envelope of the voltage across the primary side of the transformer, $v_{\mathrm{P,env}}$ (see Fig. 5). Note $v_{\mathrm{P,env}}$ is sinusoidal and in phase with v_{GRID}. Since we are using a series resonant converter, the amplitude $v_{\mathrm{P,env}}$, is limited to $V_{\mathrm{IN}} + v_{\mathrm{BUF}}$. Therefore, if $v_{\mathrm{P,env}}$ is modulated to be $v_{\mathrm{P,env}}(\theta) = (V_{\mathrm{IN}} + v_{\mathrm{BUF}}) \sin(\theta)$, the difference between $v_{\mathrm{Y,env}}(\theta)$ and $v_{\mathrm{P,env}}(\theta)$ will be minimized, as shown in Fig. 5b. Furthermore, we can minimize this difference by making $v_{\mathrm{Y,env}}(\theta)$ and $v_{\mathrm{P,env}}(\theta)$ equal at $\theta = \alpha$ and at $\theta = \beta$. Hence, v_{BUF}, α and β satisfy the following two constraints:

$$(V_{\mathrm{IN}} + v_{\mathrm{BUF}}) \sin(\alpha) = V_{\mathrm{IN}} - v_{\mathrm{BUF}} \tag{1}$$

$$(V_{\mathrm{IN}} + v_{\mathrm{BUF}}) \sin(\beta) = V_{\mathrm{IN}} \tag{2}$$

The normalized difference between $v_{\mathrm{Y,env}}(\theta)$ and

$v_{\mathrm{P,env}}(\theta)$, which must be minimized, can be quantified as $\frac{v_{\mathrm{Y,env}}(\theta)-v_{\mathrm{P,env}}(\theta)}{v_{\mathrm{P,env}}(\theta)}$. From Fig. 5b it is easy to see that the maximum of this normalized difference can only occur at one of the following line angles: δ, α or β. Hence, the cost function, C, that needs to be minimized is given by:

$$C = \max\Big(\frac{V_{\mathrm{IN}} - v_{\mathrm{BUF}} - (V_{\mathrm{IN}} + v_{\mathrm{BUF}})\sin(\delta)}{(V_{\mathrm{IN}} + v_{\mathrm{BUF}})\sin(\delta)}, \frac{v_{\mathrm{BUF}}}{(V_{\mathrm{IN}} + v_{\mathrm{BUF}})\sin(\alpha)}, \frac{v_{\mathrm{BUF}}}{(V_{\mathrm{IN}} + v_{\mathrm{BUF}})\sin(\beta)}\Big). \quad (3)$$

Since $\alpha < \beta < \pi/2$, the second argument of (3) is greater than its third argument, i.e., $\frac{v_{\mathrm{BUF}}}{(v_{\mathrm{IN}}+v_{\mathrm{BUF}})\sin(\alpha)} > \frac{v_{\mathrm{BUF}}}{(v_{\mathrm{IN}}+v_{\mathrm{BUF}})\sin(\beta)}$. Hence, the normalized difference will be minimized when the first argument of (3) is equal to its second argument, i.e., when $\frac{V_{\mathrm{IN}}-v_{\mathrm{BUF}}-(V_{\mathrm{IN}}+v_{\mathrm{BUF}})\sin(\delta)}{(V_{\mathrm{IN}}+v_{\mathrm{BUF}})\sin(\delta)} = \frac{v_{\mathrm{BUF}}}{(V_{\mathrm{IN}}+v_{\mathrm{BUF}})\sin(\alpha)}$. Using (1) to eliminate α from this equation yields:

$$(1-\sin(\delta))V_{\mathrm{IN}}^2 - (2+\sin(\delta))V_{\mathrm{IN}}v_{\mathrm{BUF}} + v_{\mathrm{BUF}}^2 = 0, \quad (4)$$

which can be solved for the optimal value of v_{BUF}:

$$v_{\mathrm{BUF}} = \frac{V_{\mathrm{IN}}(2+\sin(\delta)) + V_{\mathrm{IN}}\sqrt{(2+\sin(\delta))^2 - 4(1-\sin(\delta))}}{2}. \quad (5)$$

The optimal values of α and β can now be determined using (1) and (2), rewritten explicitly below:

$$\alpha = \sin^{-1}\Big(\frac{V_{\mathrm{IN}} - v_{\mathrm{BUF}}}{V_{\mathrm{IN}} + v_{\mathrm{BUF}}}\Big), \quad (6)$$

$$\beta = \sin^{-1}\Big(\frac{V_{\mathrm{IN}}}{V_{\mathrm{IN}} + v_{\mathrm{BUF}}}\Big). \quad (7)$$

With δ chosen as 6°, the optimal value of v_{BUF} is $0.6V_{\mathrm{IN}}$, α is 12.8°, and β is 40.9°.

The optional charge control circuit (CCC) provides flexibility in setting the SCEB switching angles (α and β) while maintaining charge balance of $\mathrm{C_{BUF}}$ (hence maintaining v_{BUF}). An example implementation of the CCC is shown in Fig. 4a, where a modified boost converter connects the negative terminal of $\mathrm{C_{BUF}}$ to the MEB input. Instead of the output voltage, the input voltage of this boost converter is regulated. The CCC switches at a higher frequency than the operating frequency of the SCEB, acting as a controlled current source. In the Step-down mode, the CCC and the dc-ac converter block charge $\mathrm{C_{BUF}}$ adiabatically; in the Bypass mode, the CCC continuous to charge $\mathrm{C_{BUF}}$ adiabatically; and in the Step-up mode, the CCC is turned off, and $\mathrm{C_{BUF}}$ is charged adiabatically by the dc-ac converter block. Figure 6 shows the current flow directions in the MEB during the three operating modes. In this design, the CCC operates in continuous conduction mode (CCM) with the duty-ratio of switch $\mathrm{S_e}$ fixed at 0.4. This keeps the voltage at the negative terminal of $\mathrm{C_{BUF}}$ at $0.4V_{\mathrm{IN}}$, maintaining v_{BUF} at $0.6V_{\mathrm{IN}}$ as required. With this control, v_{X} equals $1.6V_{\mathrm{IN}}$ during the Step-up mode, V_{IN} during the Bypass mode, and $0.4V_{\mathrm{IN}}$ during the Step-down mode.

In the steady state, the buffer capacitor $\mathrm{C_{BUF}}$, is charged when the line voltage is low, and is discharged when the line voltage is high. However, before the system enters periodic steady state operation, v_{BUF} needs to be precharged to $0.6V_{\mathrm{IN}}$. The CCC implementation described above has a built-in feedback mechanism which automatically precharges $\mathrm{C_{BUF}}$ to this level without the need for additional control. For example, when v_{BUF} is less than $0.6V_{\mathrm{IN}}$, then during the Step-down mode, since v_{X} will be larger than $0.4V_{\mathrm{IN}}$, the fixed duty ratio control of the CCC will charge up $\mathrm{C_{BUF}}$. Furthermore, during the step-up mode, since v_{X} will be smaller than the desired value of $1.6V_{\mathrm{IN}}$, the dc-ac converter block will have a lower input voltage and thus draw less charge from $\mathrm{C_{BUF}}$. This process is repeated over a few line cycles until $\mathrm{C_{BUF}}$ precharges and v_{BUF} reaches its steady state value of $0.6V_{\mathrm{IN}}$. Note that since the input voltage of the CCC boost converter is regulated, its dynamics are similar to that of a buck converter and it remains stable in the face of disturbances.

One advantage of the MEB architecture presented here is that the average power processed by the CCC circuit is a fraction of the average output power of the micro-inverter. The average power over a line cycle processed by the CCC (P_{CCC}) can be calculated from the extra energy that must be delivered to $\mathrm{C_{BUF}}$ to maintain its charge balance:

$$P_{\mathrm{CCC}} = \frac{\int_\beta^{\pi-\beta} V_{\mathrm{BUF}} I_{\mathrm{IN}} \sin(\theta) d\theta - 2\int_\delta^\alpha V_{\mathrm{BUF}} I_{\mathrm{IN}} \sin(\theta) d\theta}{\pi} = \frac{2V_{\mathrm{BUF}} I_{\mathrm{IN}}(\cos(\alpha) + \cos(\beta) - \cos(\delta))}{\pi}. \quad (8)$$

Here I_{IN} is the amplitude of the envelope of the input current of the dc-ac converter block. The fraction of line cycle average output power ($P_{\mathrm{OUT(avg)}} = \frac{2V_{\mathrm{IN}} I_{\mathrm{IN}} \cos(\delta)}{\pi}$) processed by the CCC is given by:

$$\gamma_{\mathrm{CCC}} = \frac{P_{\mathrm{CCC}}}{P_{\mathrm{OUT(avg)}}} = \frac{V_{\mathrm{BUF}}(\cos(\alpha) + \cos(\beta) - \cos(\delta))}{V_{\mathrm{IN}}\cos(\delta)}. \quad (9)$$

With $v_{\mathrm{BUF}} = 0.6V_{\mathrm{IN}}$, $\delta = 6^\circ$, $\alpha = 12.8^\circ$, and $\beta = 40.9^\circ$, γ_{CCC} equals 44.43%. Hence, only 44.43% of the average output power is processed by the CCC. Since the SCEB is switching at a low frequency (240 Hz), its switching loss is negligible compared to that of the CCC. Therefore, assuming the efficiency of the CCC circuit is η_{CCC}, and neglecting the losses in the SCEB, the efficiency of the MEB architecture can be estimated as:

$$\eta_{\mathrm{MEB}} = \frac{P_{\mathrm{OUT(avg)}} - P_{\mathrm{Loss,CCC}}}{P_{\mathrm{OUT(avg)}}} = 1 - \gamma_{\mathrm{CCC}}(1 - \eta_{\mathrm{CCC}}). \quad (10)$$

This shows that the loss caused by the CCC circuit only penalizes the energy passing through the CCC in the MEB architecture. This, together with the high efficiency of the SCEB,

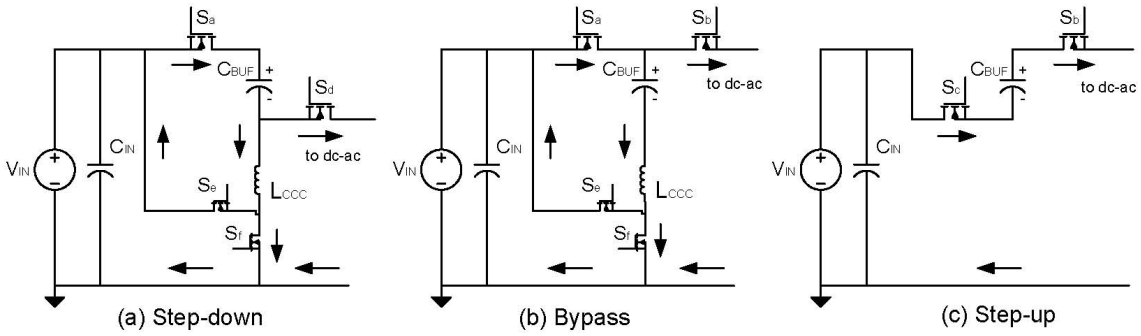


Fig. 6. Current flow directions in the MEB during the three operating modes: (a) Step-down mode, (b) Bypass mode and (c) Step-up mode.

allows the MEB based micro-inverter architecture to have a higher efficiency than conventional two stage architectures.

With the SCEB controlled as described above, the peak power rating of the CCC, $P_{\mathrm{CCC,peak}}$, is 97.7% of the line cycle average output power of the micro-inverter, $P_{\mathrm{OUT(avg)}}$. Hence, the peak power rating of the CCC is only 48.8% of the peak power rating of the micro-inverter ($2P_{\mathrm{OUT(avg)}}$). Furthermore, the CCC can be made extremely small and highly efficient since it has a fixed and reasonably small voltage conversion ratio ($V_{\mathrm{IN}} : V_{\mathrm{OUT}} = 0.4 : 1$) and it can be switched at a relatively high switching frequency.

Many micro-inverter topologies require all the twice-line-frequency energy buffering to be done by a capacitor placed across the PV panel (e.g., $\mathrm{C_{IN}}$ in Fig. 1) [4], [5]. This makes the size of the energy buffering capacitor large, since there is a limit (of typically 10% peak-to-peak) on the maximum voltage ripple allowed across the PV panel (to ensure it is operating near it maximum power point) resulting in a low utilization of the energy in $\mathrm{C_{IN}}$. In the MEB micro-inverter, the buffer capacitor, $\mathrm{C_{BUF}}$, absorbs energy when the SCEB is in the Step-down or Bypass mode (i.e., when the power delivered to the grid is low), and delivers energy to the grid when the SCEB is in the Step-up mode (i.e., when the power delivered to the grid is high). In this way, $\mathrm{C_{BUF}}$ functions as the storage element of an active energy buffer. Since $\mathrm{C_{BUF}}$ is not across the PV panel, a larger voltage ripple is allowed across it. This increases the utilization of energy in $\mathrm{C_{BUF}}$, and opens new opportunities for reducing the total capacitor size in the micro-inverter. It also creates the opportunity to exploit non-electrolytic capacitors that have a lower energy density but a longer life. The size of $\mathrm{C_{BUF}}$ can potentially be further reduced by using a Stacked Switched Capacitor (SSC) energy buffer instead of a single capacitor [12], [13].

B. Design of the dc-ac converter stage

A series-resonant high-frequency-link dc-ac converter is chosen as the dc-ac converter stage, although the benefits of the MEB apply directly to many other dc-ac converter topologies [1]–[5], [7], [8]. The MEB provides two benefits to the dc-ac converter stage: a reduced transformer turns ratio, and a compressed operation range.

The transformer turns ratio of the dc-ac converter stage needs to satisfy $\frac{N2}{N1} > \frac{v_{\mathrm{S},1}(\theta)}{v_{\mathrm{P},1}(\theta)}$, where $v_{\mathrm{P},1}$ and $v_{\mathrm{S},1}$ are the fundamental components of v_{P} and v_{S} (Fig. 3). Without the MEB, assuming square-wave switching of a full-bridge, $v_{\mathrm{P},1} = \frac{4}{\pi} V_{\mathrm{IN}} \sin(\theta)$, and $v_{S,1} = \frac{2\sqrt{2}}{\pi} V_{\mathrm{GRID,rms}} \sin(\theta)$; thus:

$$\frac{v_{\mathrm{S},1}(\theta)}{v_{\mathrm{P},1}(\theta)} = \frac{\frac{2\sqrt{2}}{\pi} V_{\mathrm{GRID,rms}} \sin(\theta)}{\frac{4}{\pi} V_{\mathrm{IN}} \sin(\theta)} = \frac{\sqrt{2} V_{\mathrm{GRID,rms}}}{2V_{\mathrm{IN}}}. \quad (11)$$

This is a lower bound on the required transformer turns ratio if there is no MEB. With the MEB, as described in Section III-A, $v_{\mathrm{P},1} = \frac{4}{\pi}(V_{\mathrm{IN}} + V_{\mathrm{BUF}}) \sin(\theta)$, and $v_{\mathrm{S},1} = \frac{2\sqrt{2}}{\pi} V_{\mathrm{GRID,rms}} \sin(\theta)$; thus:

$$\frac{v_{\mathrm{S},1}(\theta)}{v_{\mathrm{P},1}(\theta)} = \frac{\frac{2\sqrt{2}}{\pi} V_{\mathrm{GRID,rms}} \sin(\theta)}{\frac{4}{\pi}(V_{\mathrm{IN}} + V_{\mathrm{BUF}}) \sin(\theta)} = \frac{\sqrt{2} V_{\mathrm{GRID,rms}}}{2(V_{\mathrm{IN}} + V_{\mathrm{BUF}})}. \quad (12)$$

If $v_{\mathrm{BUF}} = 0.6 V_{\mathrm{IN}}$, then $\frac{v_{\mathrm{S},1}(\theta)}{v_{\mathrm{P},1}(\theta)} = \frac{\sqrt{2} V_{\mathrm{GRID,rms}}}{3.2 V_{\mathrm{IN}}}$. Hence, in this case the MEB reduces the transformer turns ratio of the dc-ac converter stage by a factor of 1.6.

The MEB also provides unique opportunities in the control of the dc-ac converter stage. To keep the explanation of this benefit simple, we assume in the following analysis that the dc-ac converter stage is under pure frequency control. In practice, both frequency control and phase-shift control are used. When the micro-inverter has no MEB, and if the resonant inverter is designed to operate at its resonant frequency when the line voltage is at its peak, then its required switching frequency, f_{noMEB}, as function of line angle θ ($0° < \theta < 180°$), is given by:

$$f_{\mathrm{noMEB}}(\theta) = \frac{\frac{X_{\mathrm{cyclo}} C_{\mathrm{R}}}{N^2} |\cot(\theta)| + \sqrt{(\frac{X_{\mathrm{cyclo}} C_{\mathrm{R}}}{N^2} \cot(\theta))^2 + 4 L_{\mathrm{R}} C_{\mathrm{R}}}}{4\pi L_{\mathrm{R}} C_{\mathrm{R}}}. \quad (13)$$

Here, L_{R} and C_{R} are the inductance and the capacitance of the resonant tank, respectively, N ($= \frac{N2}{N1}$) is the transformer turns ratio, and X_{cyclo} is the impedance of the cycloconverter (or rectifier/unfolder). Under fundamental frequency approximation, for a unity power factor microinverter, X_{cyclo} is resistive and given by $\frac{4V_{\mathrm{IN}}^2}{\pi^2 P_{\mathrm{OUT(avg)}}}$. When the micro-inverter is designed with the MEB, the required switching frequency, f_{MEB}, as a

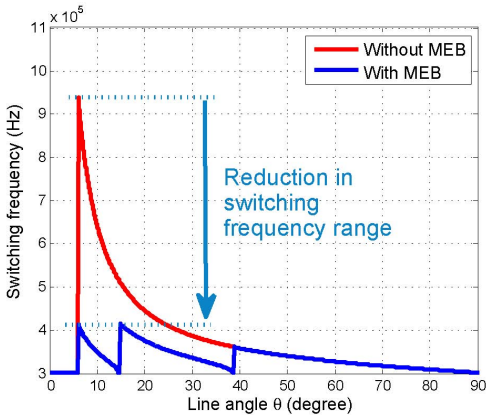


Fig. 7. Calculated switching frequencies of the microinverter over a quarter line cycle with and without the MEB with only frequency control, plotted for $P_{\mathrm{OUT(avg)}}$ equals 70 W, $C_{\mathrm{R}} = 62$ nF, $L_{\mathrm{R}} = 4.5$ μH, $V_{\mathrm{IN}} = 27$ V, $V_{\mathrm{BUF}} = 16.2$ V, $V_{\mathrm{GRID}} = 230$ $\mathrm{V_{rms}}$. The transformer turns ratio for the micro-inverter with the MEB is 4:28, and the transformer turns rato for the micro-inverter without the MEB is 5:28. The value of $X_{\mathrm{P,cyclo}}$ is 10.7 Ω for the micro-inverter with the MEB, and is 4.22 Ω without the MEB.

function of line angle is given by:

$$f_{\mathrm{MEB}}(\theta) = \frac{C_{\mathrm{R}}|X_{\mathrm{R}}(\theta)| + \sqrt{C_{\mathrm{R}}^2 X_{\mathrm{R}}(\theta)^2 - 4L_{\mathrm{R}}C_{\mathrm{R}}}}{4\pi L_{\mathrm{R}}C_{\mathrm{R}}}. \quad (14)$$

Here, $|X_{\mathrm{R}}(\theta)|$ is the magnitude of the impedance of the resonant tank and is given by:

$$|X_{\mathrm{R}}(\theta)| = \sqrt{(\frac{X_{\mathrm{cyclo}}v_{\mathrm{X}}(\theta)}{N^2(V_{\mathrm{IN}}+V_{\mathrm{BUF}})\sin(\theta)})^2 - (\frac{X_{\mathrm{cyclo}}}{N^2})^2}, \quad (15)$$

where $v_{\mathrm{X}}(\theta)$ is the inverter input voltage as shown in Fig. 4b, and X_{cyclo} equals $\frac{4(V_{\mathrm{IN}}+V_{\mathrm{BUF}})^2}{\pi^2 P_{\mathrm{OUT(avg)}}}$. Figure 7 illustrates the difference in switching frequency operating range across a half-line cycle for the micro-inverter without and with the MEB (computed using (13), (14), respectively). When the resonant frequency of the inverter is chosen to be 300 kHz, the MEB compresses the switching frequency range from 300-950 kHz to 300-410 kHz.

IV. Prototype Micro-Inverter

To validate the proposed architecture, a prototype MEB micro-inverter, designed for 27 V to 38 V dc input voltage, 230 V rms ac output voltage, and rated for 70 W (line cycle average power), has been built, tied to the grid and tested. The peak power rating of the dc-ac converter stage is 140 W, and the peak power rating of the CCC is 65 W. A photograph of the prototype is shown in Fig. 8. Also shown is a pencil and a US quarter to indicate relative size. For comparison purposes, a micro-inverter without the MEB (and with a different transformer turns ratio) has also been built and tested. The components used in these two prototypes are listed in Table I. The board area used by the various functional blocks in the case of the micro-inverter with the MEB is shown in Table II. Figure 9 shows the rear side of the board where some major passive components - $\mathrm{C_{IN}}$, $\mathrm{C_{BUF}}$, $\mathrm{L_{CCC}}$, and $\mathrm{L_R}$ - are placed. The transformer is on the front side of the board and is shown in Fig. 8.

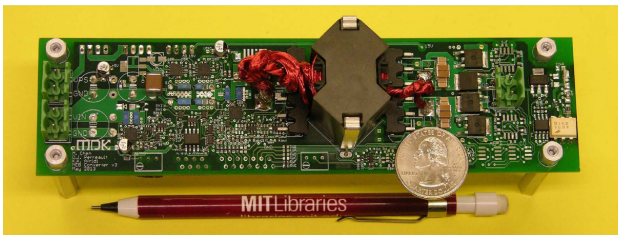


Fig. 8. Photograph of the prototype MEB micro-inverter. Also shown are a pencil and a US quarter to indicate relative size.

TABLE I
Micro-inverter Component Lists

Name	With MEB	Without MEB
$\mathrm{C_{IN}}$	3 × 1 mF, 50 V, Panasonic ECA-1HM102 (3.4cm^3 each)	5 × 1 mF, 50 V, ECA-1HM102 (3.4cm^3 each)
$\mathrm{C_{BUF}}$	5.6 mF, 25 V, Panasonic EEU-HD1E562 (5.4 cm^3)	Not needed
Total Cap Size	15.6 cm^3	17 cm^3
$\mathrm{S_{b,d}}$	EPC2016 100 V 11 A GaN FETs	
$\mathrm{S_{a,c,e,f,1,2,3,4}}$	EPC2001 100 V 25 A GaN FETs	
$\mathrm{Q_{g,h}}$	Infineon IPD65R380C6 CoolMOS MOSFETs	
$\mathrm{D_{a,b,c,d}}$	CREE CSD01060 SiC Schottky diodes	
$\mathrm{L_R}$	4.3 uH, $\mathrm{R_{dc}}$ smaller than 4mΩ, size: 15.75 cm^3; Core area: 3 cm^2	
$\mathrm{L_{CCC}}$	10 uH, $\mathrm{R_{dc}}$ smaller than 10 mΩ, size: 1 cm^3	Not needed
$\mathrm{C_R}$	60 nF (10nF × 6) 100 V 1206 C0G Ceramic	
Transformer	RM12-3F3, Primary: 5 turns, Secondary: 28 turns	RM12-3F3, Primary: 4 turns, Secondary: 28 turns
CCC control	Fixed duty ratio control with LTC6992 VCO	Not Needed
Full bridge timing	LTC6990 VCO with LTC6994 time delay block	
Gate drive ICs for Ss	TI LM5113; Five half-bridge pairs: ($\mathrm{S_a}$-$\mathrm{S_c}$), ($\mathrm{S_b}$-$\mathrm{S_d}$), ($\mathrm{S_e}$-$\mathrm{S_f}$), ($\mathrm{S_1}$-$\mathrm{S_2}$), ($\mathrm{S_3}$-$\mathrm{S_4}$)	
Gate Drive ICs for Qs	Silicon labs Si8420 digital isolator	
Optocoupler	Fairchild 4N35 optocoupler	

The switch and gate drive implementations of the MEB are shown in Fig. 10. The GaN switches are intentionally oversized. This improves the transient and fault capability, with negligible increase in overall area. $\mathrm{S_a}$ and $\mathrm{S_c}$ have higher current ratings compared to $\mathrm{S_b}$ and $\mathrm{S_d}$ because they need to handle the sum of the current of the CCC and the dc-ac converter block. Three half-bridge gate drives (LM5113) drive these six switches. The gate drive IC for $\mathrm{S_e}$ and $\mathrm{S_f}$ is referenced to ground. The gate drive ICs for $\mathrm{S_a}$, $\mathrm{S_b}$, $\mathrm{S_c}$, and

TABLE II
BOARD AREA USED BY THE VARIOUS FUNCTIONAL BLOCKS OF THE MEB MICRO-INVERTER

Function Block	Area	Percentage
CCC	3 cm^2	3.75%
SCEB	6 cm^2	7.5%
Dc-ac converter block	40 cm^2	50%
Line angle detector	5 cm^2	6.25%
Others	26 cm^2	32.5%
Total	80 cm^2	100%

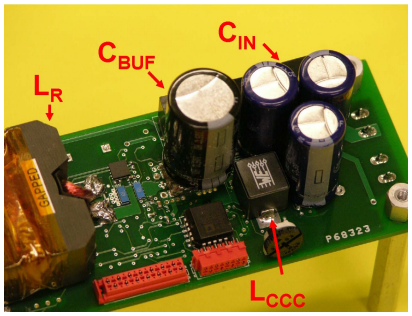


Fig. 9. Photograph of the rear side of the board showing: C_{IN}, C_{BUF}, L_{CCC}, and L_R.

S_d are referenced to the negative terminal of C_{BUF}, and can be powered by v_{BUF} through a 5V linear regulator. The body diode of S_a is used to precharge C_{BUF} when v_{BUF} is smaller than 5 V. As a result, no isolated power supply for the gate drive is needed. The high-frequency-current ripple created by the full bridge passes through the SCEB and is buffered by C_{IN}. The size of the MEB stage is compared to a US quarter in Fig. 11. Figure 11 also shows the length of the high frequency current path through the SCEB switches. The extremely small size of the GaN switches and careful PCB layout enables low parasitic inductances and mitigates possible parasitic effects. The CCC is designed to switch at 500 kHz. The CCC and the SCEB (not including C_{BUF}, which is counted separately in the capacitor size comparison) collectively uses 11.25% of the total board area.

All switches in the full-bridge inverter are EPC2001 GaN switches. Their low output capacitance enables high-frequency switching, and helps to reduce any loss caused by the stepped waveform of v_X. A 4.5 μH inductor and a 60 nF $(6 \times 10\text{nF})$ C0G ceramic capacitor form the series resonant tank of the inverter, with a resonant frequency of 300 kHz. The dc-ac converter stage is operated above the resonant frequency to achieve ZVS soft-switching. The MEB increases the input voltage of the dc-ac converter stage during a portion of the line cycle. As a result, the peak voltage stress of the switches in the full-bridge is higher than in the micro-inverter without a MEB. However, the current stress of the full-bridge switches is reduced with the MEB present.

The MEB reduces the transformer turns ratio. However, since the transformer volt-seconds and the number of turns on the secondary are the same with or without the MEB, the MEB converter has more primary side turns. The transformer

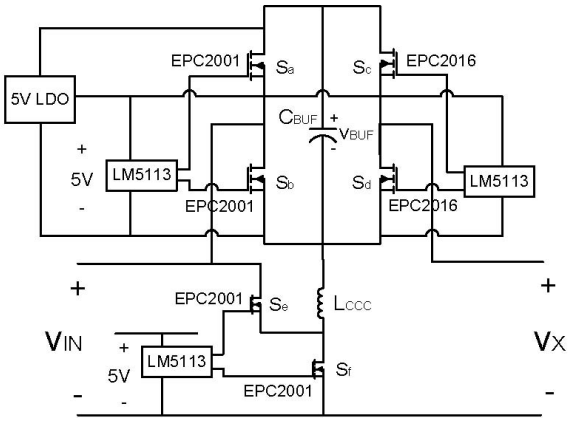


Fig. 10. Switch and gate drive implementation of the MEB.

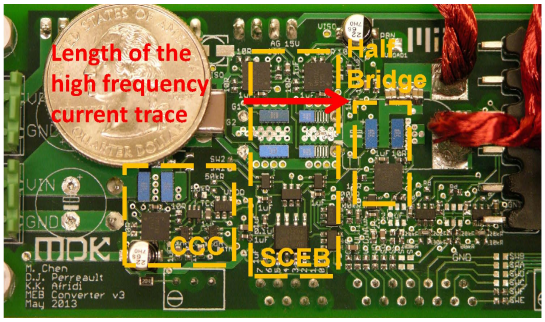


Fig. 11. PCB layout of the MEB comparing the size of the MEB and a US quarter. The area of the high-frequency current loop is minimized.

turns ratio is 4:28 in the converter without the MEB, and 5:28 in the MEB converter.

Four Cree CSD01060 SiC diodes and two Infineon IPD65R380C6 power transistors are used for the combined rectifier and unfolder stage. While using diodes increases the losses in the rectifier/unfolder stage, it avoids the control complexity of synchronous conversion. To further improve efficiency, synchronous cycloconverter designs similar to those in [5], [7] can be used. If a synchronous cycloconverter is implemented, power can be controlled by phase shifting the full-bridge inverter relative to the cycloconverter in addition to frequency control, full-bridge phase-shift control, and burst-mode control of the inverter (e.g., [5], [7], [17]–[20]).

An opto-isolated line angle detector is implemented to synchronize the microinverter with the grid. It senses the zero crossing and the polarity of the line voltage, and computes the line angle. A state machine triggered by the line angle detector is implemented in a micro-controller (MCU). The state machine uses the line angle and a look-up table to control the switches in the SCEB, the CCC, the high-frequency-link dc-ac converter and the cycloconverter. It modulates the output current to be sinusoidal in phase with the line voltage. The look-up table for the state machine over a quarter line cycle at full power operation is shown in Table III. This pattern is repeated in the remaining portions of the line cycle. Considering an inverter phase-shift range of up to 20 degrees

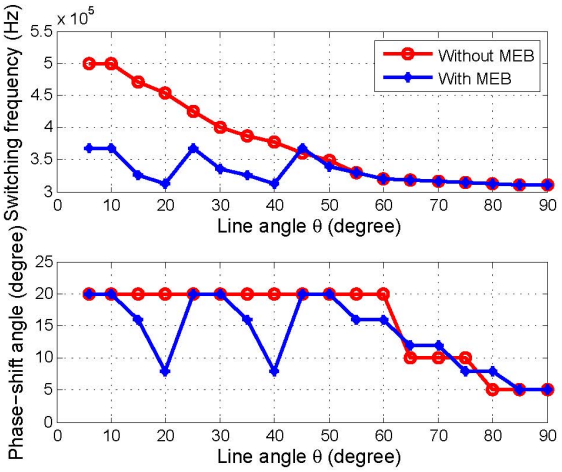


Fig. 12. Frequency and phase modulation range of the micro-inverter without and with the MEB. Range plotted for $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}} = 70$ W.

(each half-bridge goes positive or negative 10 degrees from center), it is experimentally verified that the MEB helps to compress frequency control range of the dc-ac converter block from 310-500 kHz to 310-368 kHz when $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}} = 70$ W (see Fig. 12).

V. Experimental Results

The prototype MEB micro-inverter described in the previous section has been tested in both islanded and grid-connected mode. Figure 13 shows the waveforms of the MEB micro-inverter when it is delivering full power (line cycle average output power, $P_{\mathrm{OUT(avg)}}$, of 70 W) from a 27 V input into a 230 $\mathrm{V_{rms}}$ (60 Hz) mains. The output current, i_{GRID}, has a sinusoidal shape and is in phase with the line voltage; although it contains switching noise since the prototype micro-inverter does not have an EMI filter. The input voltage of the dc-ac converter stage, v_{X}, is also shown in Fig. 13. As expected it follows a staircase pattern, synchronized with the line voltage, similar to the idealized waveform of Fig. 4b. However, unlike in the idealized waveform there is a droop of about 4 V in v_{X} during the Step-up mode when the finite sized buffer capacitor, $\mathrm{C_{BUF}}$, is being discharged. To maintain high efficiency, all the switches in the full-bridge inverter of the dc-ac converter stage are soft-switched by operating the inverter at switching frequencies above resonance. Figure 14 illustrates the soft-switching of switch $\mathrm{S_1}$, when the MEB micro-inverter has an input voltage of 27 V and an average output power of 48 W while switching at 312 kHz. In Fig. 14 the inverter output current, i_{P}, is negative when $\mathrm{S_1}$ turns on, ensuring that the current is flowing through its anti-parallel diode and holding its voltage near zero volts during switch turn-on.

The expected advantages of the MEB micro-inverter compared to the one without the MEB are in terms of efficiency and the total size of the twice-line-buffering capacitors. To confirm these advantages, the performance of the prototype MEB micro-inverter is compared with the performance of

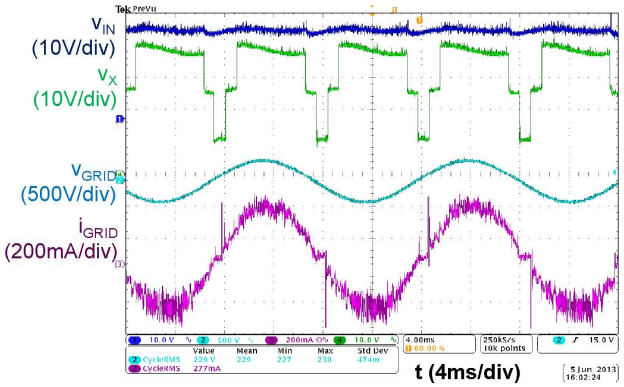


Fig. 13. Waveforms of the MEB micro-inverter, when $V_{\mathrm{IN}} = 27$ V, $V_{\mathrm{GRID}} = 230\mathrm{V_{rms}}$ and $P_{\mathrm{OUT(avg)}} = 70$ W.

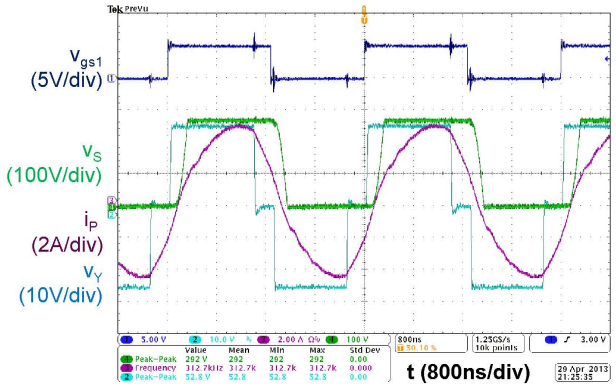


Fig. 14. Waveforms of the MEB micro-inverter showing soft-switching of $\mathrm{S_1}$ when the switching frequency is 312 kHz, $V_{\mathrm{IN}} = 27$ V, $V_{\mathrm{GRID}} = 230$ $\mathrm{V_{rms}}$ and $P_{\mathrm{OUT(avg)}} = 48$ W.

TABLE IV
Prototype Specifications

Input voltage range	27 V to 38 V dc
Output voltage	230 V rms ac
Line cycle average power	70 W (peak power: 140 W)

the prototype micro-inverter without the MEB. Both micro-inverters have been designed for the same specifications as shown in Table IV. The maximum line cycle average power delivery capability of the two prototypes has been confirmed by running them into the mains, and their instantaneous peak power capability has been confirmed by operating them in islanded mode into a resistive load. Figure 15 shows the measured waveforms for the two prototype micro-inverters while delivering power into the 230 $\mathrm{V_{rms}}$ (60 Hz) mains. Note the difference in the waveform of the input voltage of the dc-ac converter stage, v_{X}, for the two prototypes. This voltage is modulated in the case of the MEB micro-inverter (Fig. 15a), but is not in the micro-inverter without the MEB (Fig. 15b).

A. Efficiency Comparison

The line cycle average efficiency of the two prototypes is measured across a range of line cycle average power levels

TABLE III
LOOK-UP TABLE FOR THE MICRO-CONTROLLER OF THE MICRO-INVERTER WITHOUT AND WITH THE MEB WHEN $V_{\mathrm{IN}} = 27$ V AND $P_{\mathrm{OUT(avg)}} = 70$ W.

	Without MEB		**With MEB**				
Line angle θ	f_{FM}(kHz)	$\delta_{PM}(^\circ)$	**SCEB Mode**	**CCC**	f_{FM}(kHz)	$\delta_{PM}(^\circ)$	**Cycloconverter**
$0^\circ \rightarrow 6^\circ$	dead-angle (Micro-inverter off)						
$6^\circ \rightarrow 15^\circ$	500	20	Step-down	On	368	20	Q_h on, Q_g off
$15^\circ \rightarrow 20^\circ$	470	20	Bypass	On	325	16	Q_h on, Q_g off
$20^\circ \rightarrow 25^\circ$	454	20	Bypass	On	312	8	Q_h on, Q_g off
$25^\circ \rightarrow 30^\circ$	425	20	Bypass	On	368	20	Q_h on, Q_g off
$30^\circ \rightarrow 35^\circ$	400	20	Bypass	On	335	20	Q_h on, Q_g off
$35^\circ \rightarrow 40^\circ$	386	20	Bypass	On	325	16	Q_h on, Q_g off
$40^\circ \rightarrow 45^\circ$	378	20	Step-up	Off	312	8	Q_h on, Q_g off
$45^\circ \rightarrow 50^\circ$	360	20	Step-up	Off	368	20	Q_h on, Q_g off
$50^\circ \rightarrow 55^\circ$	348	20	Step-up	Off	340	20	Q_h on, Q_g off
$55^\circ \rightarrow 60^\circ$	330	20	Step-up	Off	330	16	Q_h on, Q_g off
$60^\circ \rightarrow 65^\circ$	320	20	Step-up	Off	320	16	Q_h on, Q_g off
$65^\circ \rightarrow 70^\circ$	318	10	Step-up	Off	318	12	Q_h on, Q_g off
$70^\circ \rightarrow 75^\circ$	316	10	Step-up	Off	316	12	Q_h on, Q_g off
$75^\circ \rightarrow 80^\circ$	314	10	Step-up	Off	314	8	Q_h on, Q_g off
$80^\circ \rightarrow 85^\circ$	312	5	Step-up	Off	312	8	Q_h on, Q_g off
$85^\circ \rightarrow 90^\circ$	311	5	Step-up	Off	311	5	Q_h on, Q_g off
$90^\circ \rightarrow 180^\circ$	Same as $90^\circ \rightarrow 0^\circ$						Q_h on, Q_g off
$180^\circ \rightarrow 270^\circ$	Same as $0^\circ \rightarrow 90^\circ$						Q_h off, Q_g on
$270^\circ \rightarrow 360^\circ$	Same as $90^\circ \rightarrow 0^\circ$						Q_h off, Q_g on

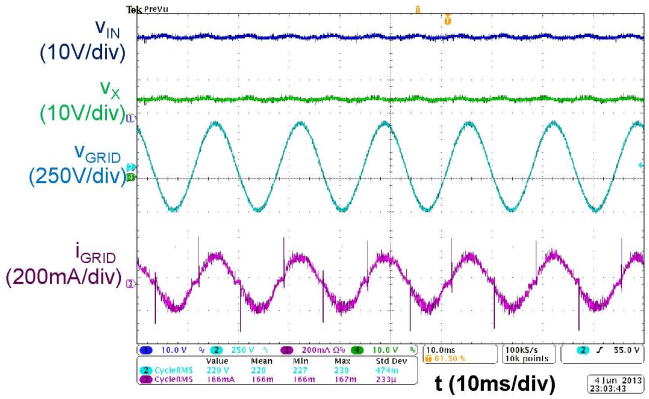
while the micro-inverters were operating in grid-connected mode. The measured efficiency for the micro-inverter with and without the MEB is plotted in Fig. 16 for two different input voltages levels: 30 V and 33 V. At both input voltages, the micro-inverter with the MEB has a higher efficiency across the measured power range of 15 W to 70 W. Although the MEB introduces small additional losses, it significantly reduces the losses in the dc-ac converter stage by compressing its operating range. Hence, resulting in an overall higher system efficiency. The MEB is more effective at improving converter efficiency in the low power range, when the switching frequency without its presence is very high. It is less effective in improving efficiency at the high power range since both micro-inverters are already operating close to the resonant frequency. For both micro-inverters, a higher input voltage results in lower efficiency. This is because a higher input voltage requires a larger voltage to be dropped across the resonant tank of the inverter, meaning that the inverter must be operated at a higher switching frequency and leading to higher losses. The measured CEC efficiency [21] of the MEB micro-inverter is 92.4%, compared to 91.1% for the micro-inverter without the MEB. Both micro-inverters have similar power factor and total harmonic distortion (THD). Table V summarizes the measured performance of the two prototype micro-inverters. The overall efficiency of the two micro-inverters could be enhanced further by using a synchronous cycloconverter instead of the diode-based rectifier/unfolder.

To gain an understanding of the loss breakdown in the two prototype micro-inverters, the efficiencies of the MEB and the dc-ac converter stage are separately measured. To measure the efficiency of the MEB, switch S_a is kept on, while switches S_b, S_c and S_d are kept off. The efficiency of the CCC of the MEB is measured at different power levels using a variable resistive load placed across the buffer capacitor, C_{BUF}, to vary the power drawn by the CCC from close to 0 W to 60 W. The efficiency of the dc-ac converter block is measured under conditions mimicking its operation without and with the MEB. First its efficiency is measured with a fixed input voltage, V_{IN}, of 30 V and with frequency control similar to that used in the micro-inverter without the MEB, as given by (13). Next its efficiency is measured with a multilevel input voltage (mimicking the output of the MEB) created by manually adjusting the voltage of a dc voltage source. In this case output power is controlled using frequency control similar to that used in the micro-inverter with the MEB, as given by (14). In both cases the efficiency of the dc-ac converter block is measured across its full instantaneous power range (0 V to 140 W). The results of these efficiency measurements are shown in Fig. 17.

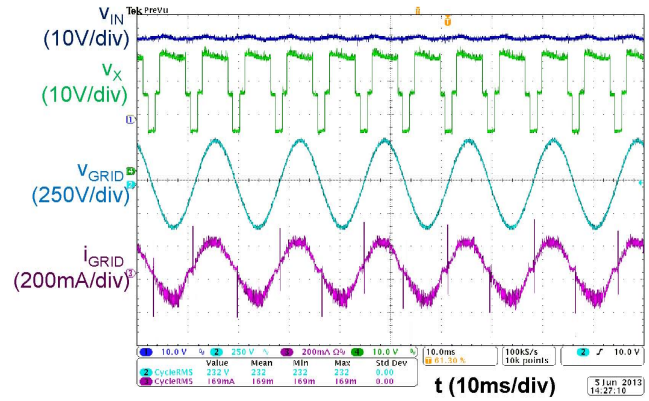
TABLE V
PROTOTYPE PERFORMANCES

	Without MEB	**With MEB**
CEC efficiency [21]	91.1%	92.4%
Power factor (measured without EMI filter)	above 98%	above 98%
THD (measured without EMI filter)	below 0.25	below 0.25

This measured efficiency data along with theoretical modeling can be used to estimate the power losses in some of the micro-inverter components. The results of this loss breakdown analysis for the micro-inverter with and without the MEB are shown in Fig. 18. This loss breakdown is computed for an input voltage of 30 V and an average output power of 70 W.



(a)



(b)

Fig. 15. Waveforms of the micro-inverter (a) without the MEB (power factor of 99.1% and THD of 0.19), and (b) with the MEB (power factor of 98.4% and THD of 0.23). Both figures are measured under the same set-up: $V_{\mathrm{IN}} = 27$ V, $V_{\mathrm{GRID}} = 230$ $\mathrm{V_{rms}}$, $P_{\mathrm{OUT(avg)}} = 38.4$ W.

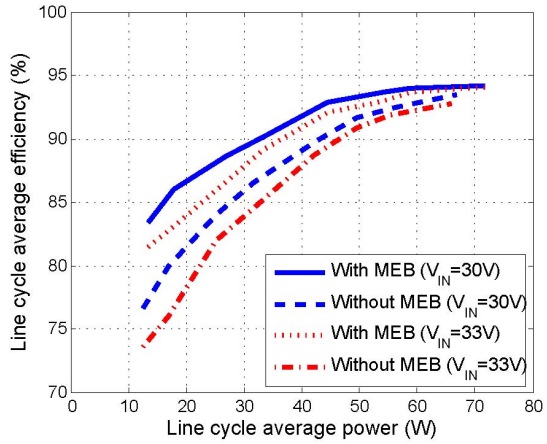


Fig. 16. Line cycle average efficiency of the microinverter with and without the MEB, with $V_{\mathrm{GRID}} = 230$ $\mathrm{V_{rms}}$, and $V_{\mathrm{IN}} = 30$ V or 33 V.

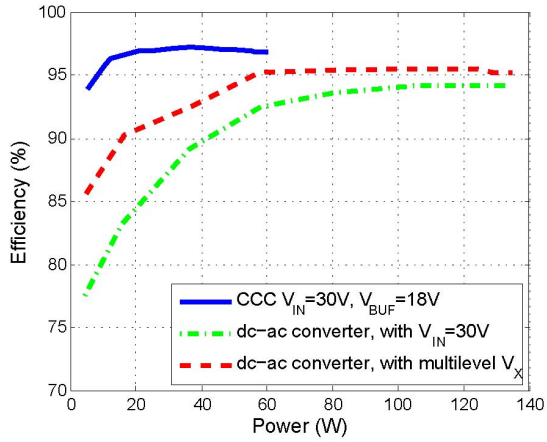


Fig. 17. Measured efficiency of the CCC, the dc-ac converter block with a fixed input voltage, and the dc-ac converter block with a multilevel input voltage when $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}} = 70$ W. The peak power rating of the dc-ac converter block is 140 W, and the peak power rating of the CCC is 65 W.

Based on this analysis the losses in the MEB are only about 0.7 W. While the presence of the MEB reduces the net losses in the dc-ac converter block. For example, the winding losses in the resonant inductor and in the primary winding of the transformer are slightly reduced since the primary side current goes down. The main loss reduction due to the MEB comes from the magnetic core loss. Since, the MEB reduces the switching frequency range of the dc-ac converter block, the inductor core losses are reduced by a factor of three and the transformer core losses are halved. The MEB has negligible impact on the losses in the components on the secondary side of the transformer. The losses in the cycloconverter are significant in both micro-inverters due to the use of diode-rectifiers. The MEB micro-inverter has slightly higher control and gating related losses due to the additional floating gate drives and control components.

B. Capacitor Size Comparison

In the MEB micro-inverter the twice-line-frequency energy buffering is provided by both $\mathrm{C_{IN}}$ and $\mathrm{C_{BUF}}$. Moving some of the buffering capability away from the output of the solar panel allows more flexibility in setting the total size of the capacitors. Selecting the relative sizes of $\mathrm{C_{IN}}$ and $\mathrm{C_{BUF}}$ requires a trade-off. Buffering more energy in $\mathrm{C_{BUF}}$ reduces the total capacitor size, but introduces more ripple in the dc-ac converter block's input voltage, v_{X}. A larger variation in v_{X} complicates the control of the dc-ac converter block and increases the peak voltage stress on the full-bridge switches. The potential for capacitor size reduction also depends on the allowed voltage ripple across the PV panel. As the voltage ripple allowance at the output of the solar panel becomes smaller, the amount of total capacitor size reduction possible with the MEB becomes larger.

In the prototype MEB micro-inverter, three 1 mF, 50 V capacitors (Panasonic ECA-1HM102) serve as $\mathrm{C_{IN}}$, while one 5.6 mF, 25 V capacitor (Panasonic EEU-HD1E562) serves as the $\mathrm{C_{BUF}}$. The total volume of these capacitors is 15.6 $\mathrm{cm^3}$. It is experimentally verified that with an input voltage of 27 V and an average output power of 70 W, the MEB micro-inverter has a 7% peak-to-peak voltage ripple across $\mathrm{C_{IN}}$ (and a 4 V

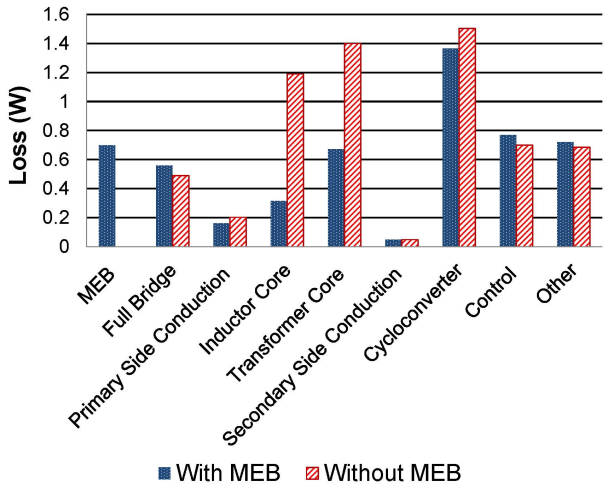


Fig. 18. Loss break-down comparison between the micro-inverter with and without the MEB, when $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}} = 70$ W.

peak-to-peak voltage ripple across $\mathrm{C_{BUF}}$). To achieve the same voltage ripple across $\mathrm{C_{IN}}$ without the MEB, five 1 mF, 50 V capacitors (Panasonic ECA-1HM102) must serve as $\mathrm{C_{IN}}$. The total volume of these capacitors is 17 cm^3, which is 9% larger than the total capacitor volume in the MEB micro-inverter. The volume reduction with the MEB can be larger if a smaller ripple is allowed at the micro-inverter input and/or a larger ripple on $\mathrm{C_{BUF}}$ can be managed.

VI. Conclusions

This paper introduces a Multilevel Energy Buffer and Voltage Modulator (MEB) for grid-interfaced micro-inverters. The MEB significantly reduces the range of voltage conversion ratios that the high-frequency dc-ac converter portion of the micro-inverter must operate over by stepping its input voltage in pace with the line voltage. This enables the dc-ac converter stage to operate over a narrower operating range and achieve higher efficiency. The MEB also functions as an active energy buffer, which helps to reduce the twice-line-frequency voltage ripple at the output of the panel. A prototype 70 W MEB micro-inverter, designed for 27 V to 38 V dc input and 230 V rms ac output, has been built, and used to validate the operational principles and performance advantages of the MEB converter.

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