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Switched-Capacitor Step-Down Rectifier for Low-Voltage Power Conversion

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***Abstract*—This paper presents a switched-capacitor rectifier that provides step down voltage conversion from an ac input voltage to a dc output. Coupled with current-drive source, low-loss and high step-down rectification is realized. Implementation in CMOS with appropriate controls results in a design suitable for low-voltage very-high-frequency conversion. Applications include switched-capacitor rectification to convert high-frequency ac to a dc output and, combined with inversion and transformation, to dc-dc converters for low-voltage outputs. A two-step CMOS integrated full-bridge switched-capacitor rectifier is implemented in TSMC 0.25 μm CMOS technology for demonstration purposes. For an operation frequency of 50 MHz and an output voltage of 2.5 V, the peak efficiency of the rectifier is 81% at a power level of 4 W.**

I. INTRODUCTION

Power conversion for the myriad low-voltage electronic circuits in use today, including portable electronic devices, digital electronics, sensors and communication circuits, is becoming increasingly challenging due to the desire for lower voltages, higher conversion ratios and higher bandwidth. The size and cost of the power conversion electronics (dc-dc converters) for these applications are also important.

Fig. 1 shows the three major blocks of a dc-dc converter: inverter stage, transformation stage and rectification stage. The conversion ratio of conventional rectifiers for high-frequency rectification do not provide a desirable step down from the ac voltage amplitude to the dc voltage output. This places a greater burden on the transformation stage to achieve a large step-down. This can be detrimental, as the percentage loss of a matching network (or other transformer) is often directly related to the voltage conversion ratio [1].

For example, consider the traditional half-bridge rectifier of Fig. 2 (which may be implemented with diodes or more typically with CMOS transistors acting as synchronous rectifiers). When driven from a current source, this rectifier provides a $\pi/2$ voltage conversion ratio between the fundamental component of the ac voltage to the output dc voltage ($V_{dc}/V_{ac,pk}$) (Fig. 2). This step up in voltage in the rectification stage has the effect of increasing the required conversion ratio of the other system portions in a step-down system. If the rectification stage can instead provide step-down characteristics, then the voltage transformation ratio in the transformation stage can be reduced while maintaining the same conversion ratio in the system as whole, and hence improve the system performance. A full-bridge rectifier doubles the input voltage swing and gives a step-down voltage ratio of $\pi/4$. However, double-ended operation (such as enabled by transformer isolation) is required for the full-bridge rectifier. Therefore, a rectifier with higher step-down voltage conversion ratio for single-ended operation is desired.

This paper presents a voltage step-down rectifier with switched-capacitor architecture suitable for integration on-die in CMOS. This rectifier has application to both dc-dc conversion and to ac power delivery [2] for low-voltage electronics. When coupled with an inverter and transformation stage as in Fig. 1, the rectifier provides a dc-dc converter having improved voltage transformation characteristics as compared to conventional converters. The inverter may be realized with high-voltage low-current devices (either on the same die as the rectifier or a different die) and the transformation stage may be realized with magnetics (transformers or matching network, etc.) realized on or off the rectifier die.

It should be noted that some kinds of switched-capacitor rectifiers have been previously explored in the context of low-frequency applications (e.g., [3]–[6]), and multi-level converter structures such as those in [7] can be controlled to provide rectification. However, the approach presented here goes beyond existing techniques in that it is structured and

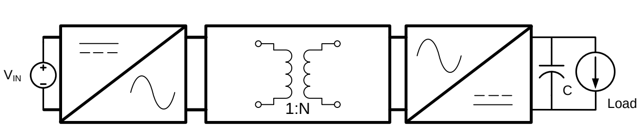


Fig. 1. A architecture for a dc-dc converter.

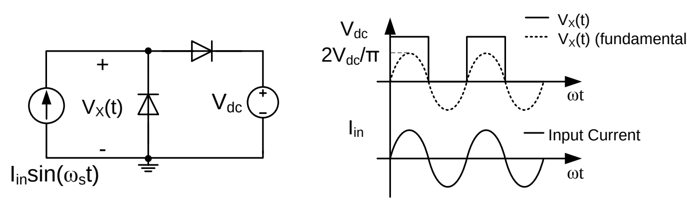


Fig. 2. The half-bridge rectifier and its characteristics. When provided with a dc blocking capacitor at its input, this design can also be recognized as a "voltage doubler" rectifier.

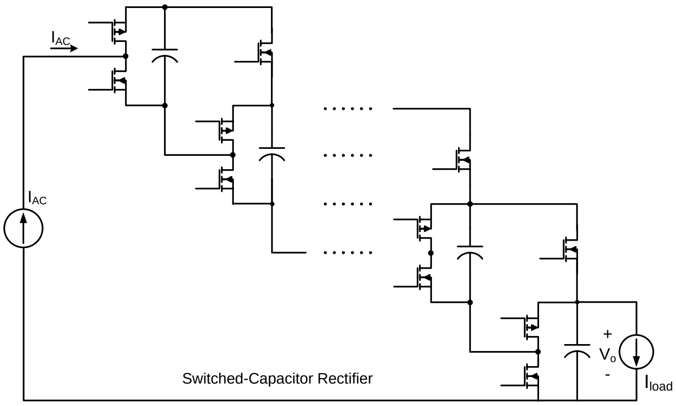


Fig. 3. General schematic of a multi-step switched-capacitor rectifier.

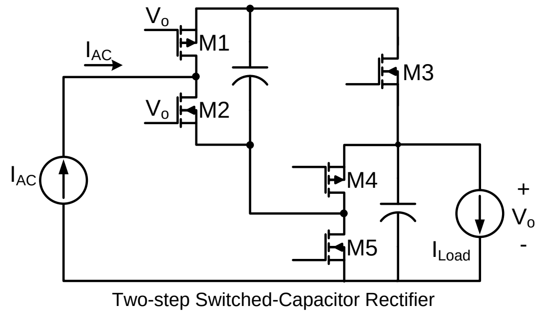


Fig. 4. Sample schematic of a two-step CMOS switched-capacitor step-down rectifier. The drive and control structure is shown in Fig. 5. Note that in some cases a dc blocking capacitor (not shown) may be desired at the rectifier input; this does not change the rectification characteristics.

controlled to provide large step-down rectification at very high frequencies (VHF) from current-driven (e.g., inductive) ac sources. To accomplish this, the proposed approach leverages the characteristics of on-die CMOS devices, utilizes self-drive of "flying" switches, and integrates key control and drive logic together with the power stage.

Section II of the paper provides detailed analysis of the proposed switched-capacitor rectifier circuit. Section III shows the design of the IC prototype of the proposed rectifier. Section IV presents the experimental result of the prototype system and section V concludes the paper.

II. Analysis

Fig. 3 shows the general structure of the switched-capacitor (SC) rectifier. This rectifier is ideally driven from an inductive ac source, or an ac source that looks similar to a current source. Excepting the switches referenced to the top of the half bridges, the switches can be replaced by diodes. In steady-state, the voltages across all the capacitors are equal to the output voltage. In "diode operation", whether the capacitors are stacked in series or parallel by the operation of the switches depends on the ac-drive current direction. (With active devices, it is also possible to phase shift the rectifier switching with respect to the ac-drive current). In either case, the input voltage swing of the switched-capacitor rectifier is N times the output voltage for N "steps" (with N = 1 representing only a half-bridge). The switched-capacitor rectifier can provide a $\pi/(2N)$ step-down voltage conversion ratio between the fundamental component of the ac input voltage to the output dc voltage ($V_{dc}/V_{ac,pk}$). This increases the step down transformation in the rectification stage of a dc-dc or ac-dc power converter, and also minimizes the step down conversion ratio of a transformation stage in ac power delivery system to provide better performance.

To illustrate the operation of the system, a two-step switched-capacitor rectifier is presented here. Fig. 4 shows a schematic of one version of our proposed switched-capacitor rectifier. Fig. 6 shows the switching pattern of the SC rectifier and Fig. 7 describes the theoretical switching and voltage waveforms for "diode rectification". When the input ac current is positive, switches labeled S_1 are closed and switches labeled S_2 are open. The capacitors C_1 and C_2 are connected such that positive current charges C_1. This current recharges C_2 during at least a portion of this state, and this current and the current in C_2 support the load current. Since the capacitor C_1 and C_2 both hold the same average voltage V_o in steady-state operation, the input voltage of the SC rectifier is approximately $2V_o$ in this state. When the input current is negative, switches S_1 are opened and switches S_2 are closed. In this case, C_1 and C_2 are connected in parallel to support the load, and the input of the SC rectifier is shorted to the ground. As a result, the input voltage of the SC rectifier is 0 V. In this case, it has a $2V_o$ voltage swing at the input of a rectifier, thus providing a $V_{dc}/V_{in,fundamental} = 1/\frac{4}{\pi} = \frac{\pi}{4}$ fundamental peak ac-to-dc conversion, which results in step-down in the rectification stage. This design thus provides an additional factor of two in voltage step down as compared to a conventional half-bridge rectifier. Higher-stage versions of this switched-capacitor rectifier can provide higher step-down ratios, but require a higher device count and greater control complexity.

As can be seen from the switched-capacitor rectifier operation, each of the devices only need to block the low output voltage level. As a result, low-voltage CMOS devices rated for the converter output voltage can be used to provide fast switching speed. As device M3 has its control port referenced to the dc output voltage, level-shifting its control signal is straightforward, and it can be driven easily. The detailed control circuit for the SC rectifier is shown in Fig. 5. Flying capacitor C_1 can be used as a bootstrap capacitor to provide energy for the gate driver of M3. This eliminates the extra circuit that would otherwise be required to supply power for the gate driver of M3 and also minimizes the driver energy storage capacitance C_3. In addition, since M1, M2, M3 and M4 share the same control pattern, only a constant voltage is required to drive the gates of M1 and M2, while the V_X node can be controlled by switching M4 and M5 using ground-referenced logic and drivers. As a result, the first-stage devices M1 and M2 can be self-driven by the output voltage, as is also shown in Fig. 5.

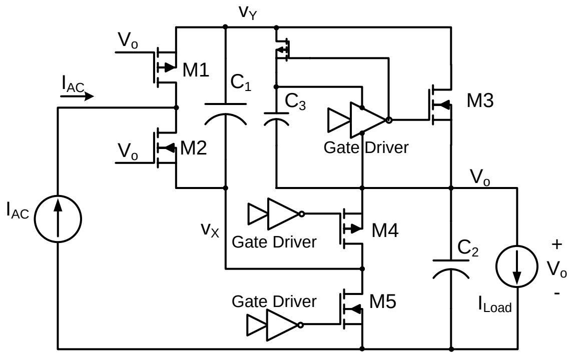


Fig. 5. Control details of the switched-capacitor rectifier.

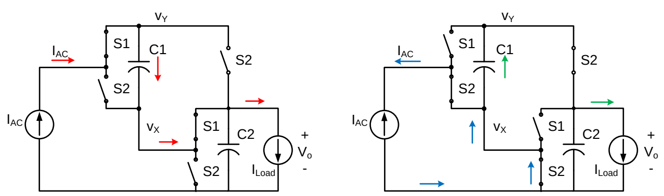


Fig. 6. Switching patterns of the switched-capacitor rectifier.

In general, devices in the bridge of previous "step" can be driven by the positive voltage of the capacitor in the next "step". Furthermore, the devices referencing to the positive node of the flying capacitors can be driven by a dc voltage $N \times V_o$ (N is the level where the device is at) since their reference nodes are switching with the flying capacitors. This reduces the complexity of the driving scheme greatly. Only the devices in the last stage are required to be controlled and all other devices in the multi-level SC rectifier can be either self-driven or driven by dc voltages. The driving scheme of the multi-level SC rectifier is shown in Fig. 8.

It will also be recognized that this rectifier can be driven in reverse to provide an inverter with a large step-up voltage conversion ratio. Implemented in this manner, one gets a large amplitude square wave output. This is more crude than achievable with multi-level topologies such as a Marx inverter [8] or other multi-level inverter [7], but takes advantage of the self-driven nature of many of the switches in a CMOS implementation to provide a distinct performance advantage.

Similar to the full bridge rectifier, the SC rectifier can also be connected in a double-ended fashion to double its ac

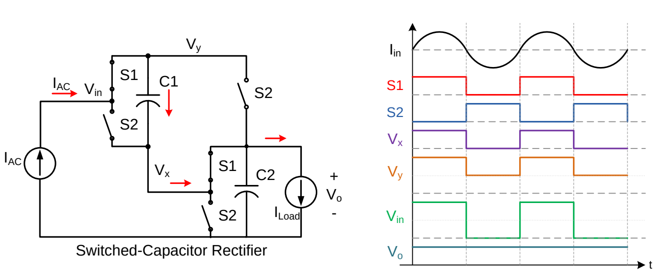


Fig. 7. Switched-capacitor rectifier operating waveforms.

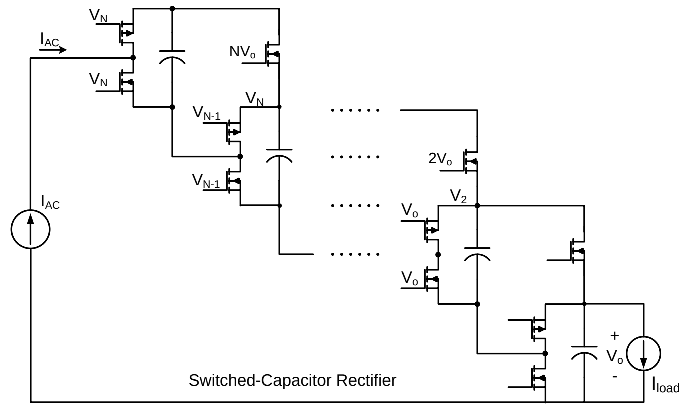


Fig. 8. Self-driven scheme for the multi-level switched-capacitor rectifier circuit.

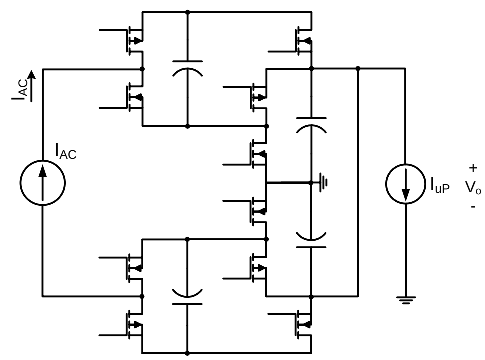


Fig. 9. Schematic of a double-ended two-step switched-capacitor rectifier.

voltage and eliminate the dc offset at the input. Fig. 9 shows the schematic of a double-ended SC rectifier structure. The double-ended SC rectifier has the same operation pattern as a single-ended SC rectifier. It just has two single-ended SC rectifiers operating 180^o out of phase. In the double-ended SC rectifier, the input voltage swing is $\pm NV_o$, so the step-down voltage conversion ratio is $\pi/(4N)$.

III. Integrated Circuit Design

To demonstrate the functionality of the switched-capacitor rectifier and validate the concept, an integrated version of the two-step switched-capacitor rectifier has been designed and fabricated in a TSMC 0.25 μm process. A 2.5 V output voltage is chosen based on the native operating voltage of the TSMC 0.25 μm process. An operation frequency of 50 MHz is chosen to minimize the size of passive components while providing acceptable efficiency. (Finer-width processes enable a combination of lower voltages, higher frequencies, and higher efficiencies based on CMOS scaling characteristics.) There are two single-ended switched-capacitor rectifiers on the chip, which can be configured into a double-ended rectifier. Each single-ended switched-capacitor rectifier has an output power of 2 W (4 W total for the full circuit). (This power level can represent that of a small zone in a microprocessor, or that of an entire low-power digital IC). The device sizes for the rectifiers are optimized to balance the conduction loss and

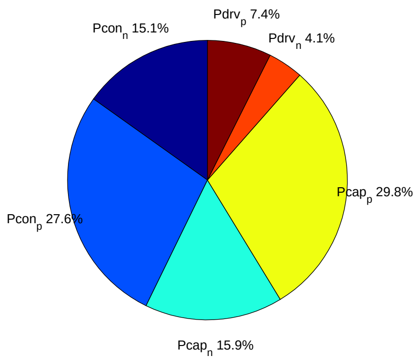


Fig. 10. Figure shows the loss break down in the rectifier. $Pcon_n$ and $Pcon_p$ mean the conduction loss in NMOS device and PMOS device respectively, $Pcap_n$ and $Pcap_p$ are the capacitively loss for the NMOS device and PMOS device. $Pdrv_n$ and $Pdrv_p$ are the gate driver loss for the devices.

capacitive loss [9]–[11]. The loss distribution of the rectifier is shown in Fig. 10. A taper factor of 8 is chosen for the gate driver to balance the tapered gate driver loss and switching loss of the power devices. In the rectifiers, the optimized width of each NMOS device is 23100 μm and the optimized width of the PMOS device is 48000 μm.

In order to explore the proposed approach and compare it to other rectification architectures, conventional CMOS bridge rectifiers are also built on the IC. There are a total of 6 half-bridge rectifiers integrated on the chip for testing flexibility, which can be reconfigured into 3 sets of individual full bridge rectifiers. Each full-bridge rectifier is optimized to handle 2 W of output power. Since the rectifier is driven by an inductive sinusoidal current source, soft-switched class D or DE operation can be achieved in the rectifiers if the control timing is adjusted carefully [12]. Fig. 11 shows the simulated switching waveforms of the soft-switched rectifier. When the sinusoidal input current changes from negative to positive, the low-side NMOS can be turned off under a near-zero-current-switching condition. With the high-side PMOS remaining off, the positive input current can charge the drain-source capacitance of the NMOS and discharge the drain-source capacitance of the PMOS. If this dead-time period is controlled accurately, zero-voltage-switching can be achieved at the turn-on transition of the high-side PMOS. Similarly, the high-side PMOS can be turned off close to zero-current-switching condition when the input current is making the positive to negative transition. By controlling the dead-time, zero-voltage-switching can be achieved at the turn-on transition of the low-side NMOS. In this way, the energy stored in the output capacitance of the switches can be recycled and hence improve the performance of the rectifier. In this particular design, 1 nS fixed dead-time is used based on the sizes of the devices and input current level; this dead-time is also used in the switched-capacitor rectifier for the same purpose.

A simplified full-chip schematic is shown in Fig. 12. Only a single full-bridge rectifier and a single-ended switched-capacitor rectifier are shown in the schematic for simplicity. Synchronous rectification is controlled by two-stage voltage-controlled delay lines. The first stage comprises coarse voltage-controlled delay lines, which gives a 2 nS to 11 nS adjustable delay range. Three of these coarse voltage-controlled delays are connected in series and a 2-bit ADC is used to select between the center tap delays. The second stage comprises a fine voltage-controlled delay lines, which only give a 1 nS adjustable delay range. With this stage, the timings of rectifiers can be fine tuned to achieved optimal performance. The schematic of the voltage-controlled delay line is shown in Fig. 13. The delay is controlled by the RC time constant between the inverters. The NMOS connected in series with the capacitor is used as voltage-controlled resistor. When the RC time constant is comparable to the switching frequency, the delay is highly nonlinearly dependent on the control voltage due to the nonlinearity in the inverter. As a result, a multi-stage system is required for long delays.

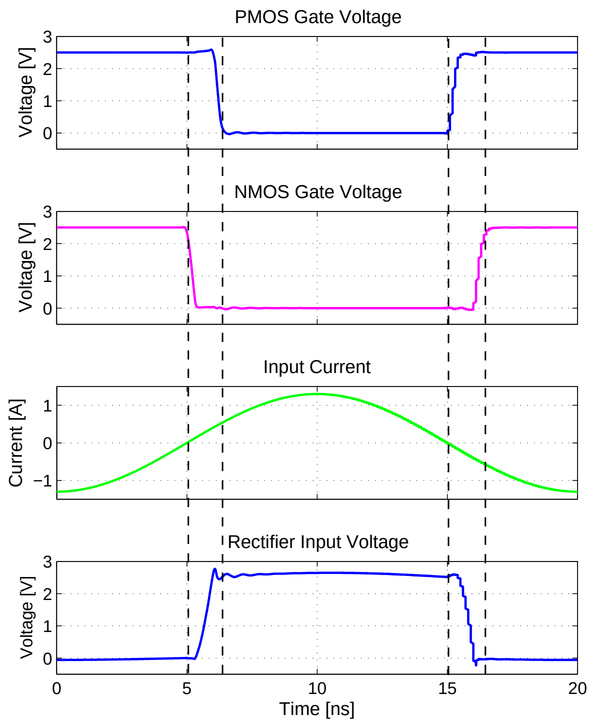


Fig. 11. Simulated soft-switched class D rectifier switching waveforms. It shows that both devices can achieve zero-voltage turn-on and close to zero-current turn off.

In addition, a level shifting circuit is required to control the NMOS referenced to the output voltage in the switched-capacitor rectifier. The level shifter needs to convert the ground-referenced signal to an output-voltage-referenced signal. A capacitor-coupled level shifting circuit is used here and the schematic is shown in Fig. 14. Compared to resistive-loaded level shifting circuits, this capacitor coupled level shifter consumes no static power and has faster transition time (smaller RC time constant in the switching node). Furthermore, the level shifting is based on the output voltage instead

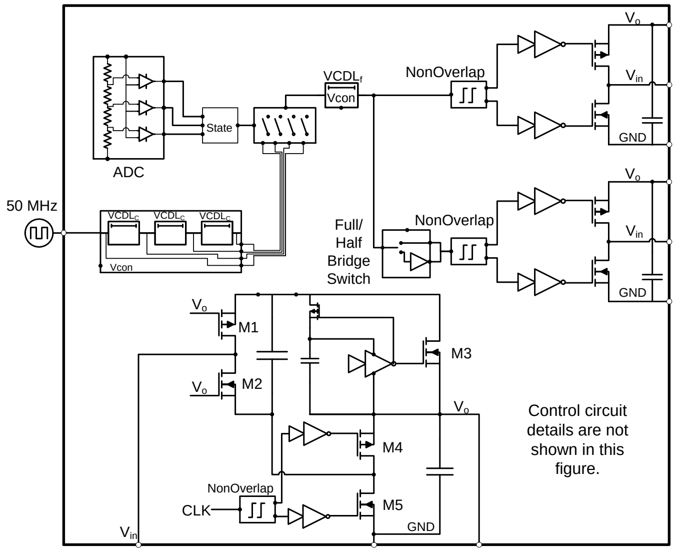


Fig. 12. A simplified schematic of the chip. Control circuit details are not shown in the figure. In addition, only a single full-bridge rectifier and single-ended switched-capacitor rectifier are shown. $VCDL_c$ is the coarse control of the voltage-controlled delay line and $VCDL_f$ is the fine-tune control of the voltage-controlled delay line.

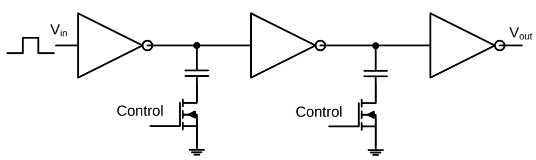


Fig. 13. The schematic of the voltage-controlled delay line.

of the 2.5 V logic supply voltage. In this case, the logic driven by the level shifter will never experience a voltage higher than the output voltage during the startup transient. As a result, only native 2.5 V MOSFETs are used in the circuit and no high-voltage devices are required. However, deep-n-well NMOS is required when the body substrate is not referenced to ground.

A 390 pF dc decoupling NMOS bypass capacitor is integrated for the output of switched-capacitor rectifier, and a 170 pF deep-n-well NMOS capacitor is integrated for the flying capacitor in the switched-capacitor rectifier. For each of the half-bridge rectifiers, a 280 pF dc decoupling NMOS capacitor is also integrated on die. These capacitors are used to prevent

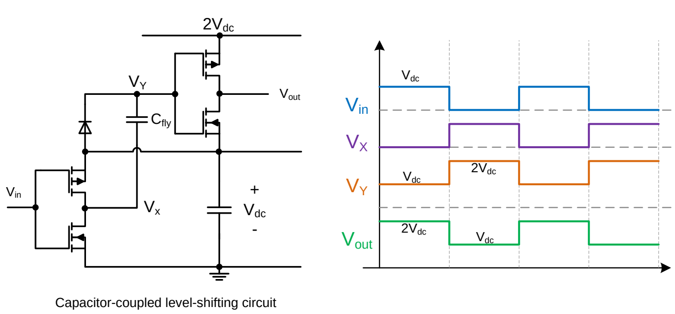


Fig. 14. The schematic of the level shifting circuit.

TABLE I
IC DESIGN SUMMARY

	Devices	Size	Area (mm^2)
SC Rectifier	M1	480000 μm	0.085
	M2	231000 μm	0.046
	M3	231000 μm	0.046
	M4	480000 μm	0.085
	M5	450000 μm	0.080
	Flying capacitor	170 pF	0.33
	Decoupling capacitor	390 pF	0.78
	Efficiency	81%	
Bridge Rectifier	NMOS device	231000 μm	0.046
	PMOS device	480000 μm	0.085
	Decoupling capacitor	280 pF	0.51
	Efficiency	87%	

This table shows the detailed sizing for each power MOSFET in both the SC rectifier and bridge rectifier and the area breakdown in both designs. For the bridge rectifier, the design detail is for a single half-bridge rectifier only. There are total six of this half-bridge rectifier on the chip.

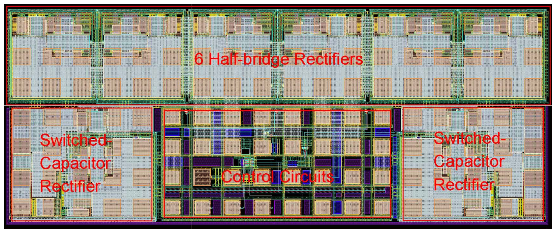
the devices from being damaged by excessive ringing due the package parasitics. These capacitors are over-sized to optimize the layout structure. For sufficient filtering, external 100 nF 0204 ceramic capacitors are also used.

Table I shows the sizing details and area breakdown of the power MOSFETs and decoupling capacitors in both the switched-capacitor rectifier and conventional bridge rectifier. From the simulation, the switched-capacitor rectifier has 81% peak efficiency at 4 W of output power with switching frequency of 50 MHz and 2.5 V of dc output voltage. This efficiency includes all the logic and gate driver losses, the estimated interconnect loss on the layout and ESR loss on the external decoupling capacitors (60 mΩ ESR on the external 100nF 0204 ceramic capacitors contribute an estimated 10% of the total loss in the SC rectifier system). For the full-bridge rectifier system, the simulated peak efficiency is 87%. Even the double-ended SC rectifier alone has a lower efficiency as compared to the full-bridge rectifier, but its step-down ratio is two times higher. This reduces the burden on the transformation stage while maintaining the same system conversion ratio and gives a better overall system performance. The experimental result in the next section further verifies this conclusion.

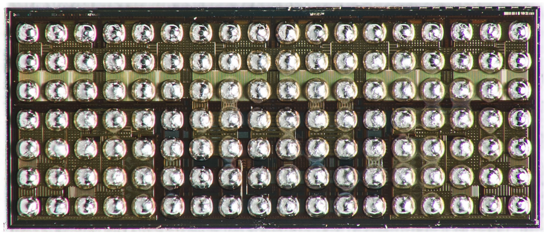
To optimize the performance and minimize the parasitic effects, flip chip packaging is used. The layout and the picture of the die after solder ball bumping are shown in Fig. 15. The pad size is 200 μm square with a 350 μm pitch. The total chip size is 6600 μm x 2800 μm (A quarter of the chip is used for test pins).

IV. Experimental Results

In order to compare both the performance and operation of the proposed switched-capacitor rectifier and conventional bridge rectifier, two prototype boards were built for the rectifier circuit validation, one with the proposed rectifier and a second implementing a conventional full-bridge CMOS rectifier. For

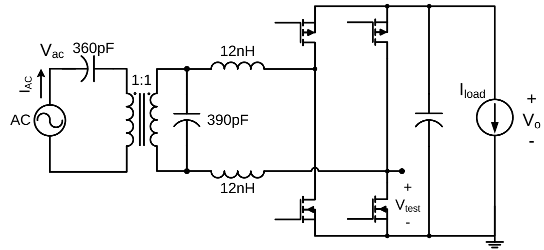


(a) Layout of the rectifier chip

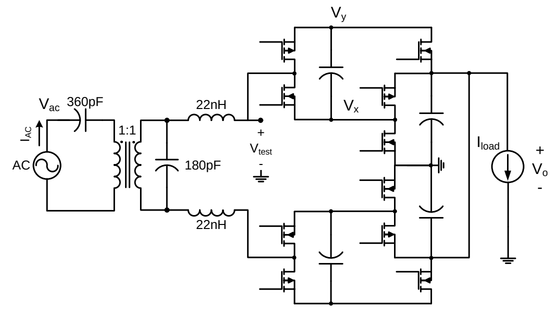


(b) Flipchip bumping on the die

Fig. 15. The layout of the rectifier chip as seen from the board side of the IC. The pads of the flip-chip IC are 200 μm square with a 350 μm pitch. The solder balls are 200 μm.



(a) Full-bridge rectifier schematic



(b) Double-ended SC rectifier schematic

Fig. 16. Schematics of the rectifier prototypes. 50 MHz, 20 V ac input voltage, 2.5 V output voltage and 4 W of output power. Drive to the rectifiers in the experimental system is provided by an RF power amplifier. V_{test} is the rectifier input voltage swing measurement point.

testing purposes, the very-high-frequency (VHF) ac power is supplied by an RF power amplifier. Both systems have the same operation frequency of 50 MHz and 4 W of output power. The ac input voltages are 20 V (line-to-neutral) and output dc voltages are 2.5 V. As a result, the voltage conversion ratio in the system is 8:1. Fig. 16(a) shows the schematic of the conventional full-bridge rectifier system. 390 pF ATC capacitors and two 12.5 nH Coilcraft Mini Spring air core inductors (A04T_L) were used to form a matching network with a 2π:1 voltage conversion ratio to match the input impedance of the SC rectifier to the 50 Ω output impedance of the power amplifier. Isolation and single-to-double-ended operation is provided by a 1:1 hand-wound transformer with a BLN1728-8A/94 core. There are 7 turns of each winding on the transformer providing a magnetizing inductance L_m of 1.2 uH and leakage inductance L_l of 30 nH. A 360 pF capacitor is connected in series of the primary side of the transformer for leakage inductance cancellation. The whole system provides an 8:1 voltage conversion ratio from the ac input voltage to the dc output voltage. Fig. 16(b) shows the schematic of the double-ended switched-capacitor rectifier system. 180 pF ATC capacitors and two 22 nH Coilcraft Midi Spring air core inductors (1812SMS-22N) were used to form a matching network with a π:1 voltage conversion ratio to match the input impedance of the rectifier to the output impedance of the power amplifier. Since the two-step SC rectifier has twice the step-down voltage conversion ratio as the conventional bridge rectifier, the voltage transformation ratio of the matching network is reduced by half that of the conventional bridge rectifier to achieve the same voltage conversion ratio in the overall system. Again, transformer is used for isolation and single to double-ended operation. And a 360 pF capacitor is connected in series of the primary side of the transformer for leakage inductance cancellation.

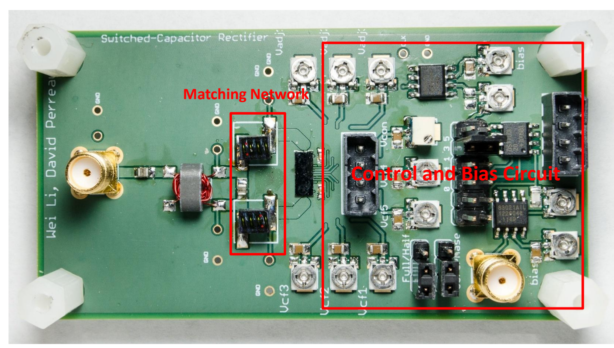


Fig. 17. A picture of the switched-capacitor rectifier prototype board. The black rectangle in the middle of the board is the rectifier IC.

Fig. 17 shows the picture of the SC rectifier system prototype; the conventional bridge rectifier system has the same PCB footprint. Fig. 18 shows the switched-capacitor rectifier operating waveforms. In the first step, the node V_x switches between ground and output voltage V_o. In the second step, the node V_y switches between V_o and 2 V_o. As a result, the input of the single-ended switched-capacitor rectifier switches between ground and twice the output voltage V_o, as shown in the center plot of the Fig. 18. A 20 V_{peak} ac input voltage waveform and $\pm$5 V ($2V_o$) voltage swing in the input of the double-ended switched-capacitor rectifier are shown in the bottom plot of Fig. 18.

Fig. 19 shows the experimental waveforms comparison of both rectifier prototypes. Both systems shown the same 50

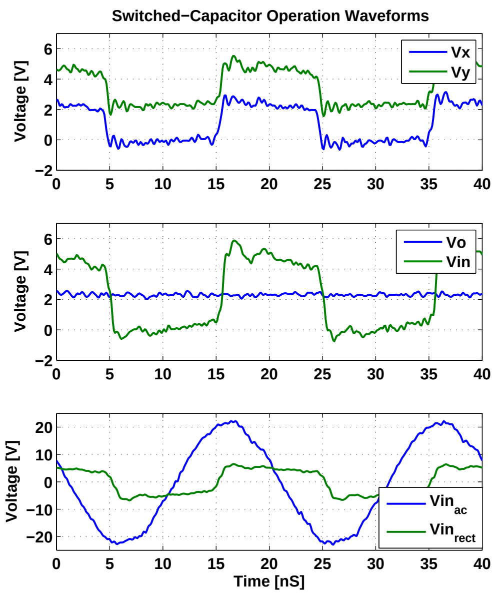


Fig. 18. Experimental waveforms show the operation of the double-ended switched-capacitor rectifier.

MHz 20 V line-to-neutral ac input voltages and 2.5 V output voltages with 4 W of output power. The ground-referenced input of the SC rectifier shows ground to $2V_o$ swing as the input of the conventional rectifier only shows ground to V_o swing (The differential input swings are $\pm 2V_o$ and $\pm V_o$ respectively). The measured overall system efficiency is about 66% for the SC rectifier system, which matches with the calculated performance (estimated transformer efficiency is 90%, matching network efficiency is 93% with an inductor Q of 80 and the SC rectifier efficiency is approximately 81%). However, the overall system efficiency of the conventional full-bridge rectifier is about 63% due to the lower performance in the transformation stage (estimated transformer efficiency is 90%, matching network efficiency is 83% with an inductor Q of 56 and the rectifier efficiency is approximately 87%). (The inductor sizes are kept similar in this comparison; as a result, the inductor Q is different for different inductances). This measurement results confirm that the switched-capacitor rectifier reduces the burden of the matching network to provide high voltage step-down while improving overall system performance. In addition, the ESR in the flying capacitors contribute a considerable amount of loss (approximately 10% of the total loss) in the switched-capacitor system due to the high RMS input current. Better capacitor technology (e.g., integrated trench capacitors) with smaller ESR can further improve the SC rectifier efficiency.

V. Conclusion

This paper presents a switched-capacitor rectifier architecture for low-voltage electronics. By providing large step-down voltage conversion in the rectification stage, the burden in the transformation stage in a dc-dc converter or ac power

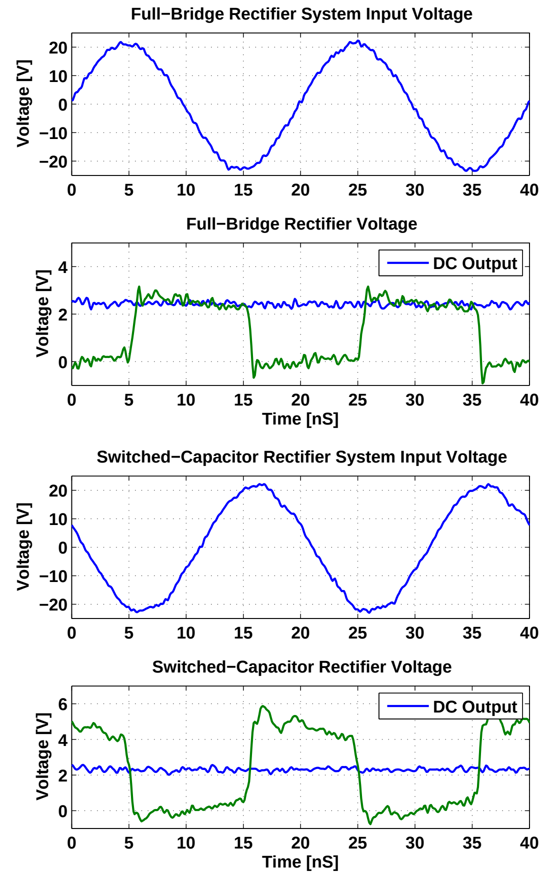


Fig. 19. Experimental waveforms of the rectifier prototypes. Only one phase of the full-bridge rectifier input voltage is shown here, which is ground referenced. The other phase of the rectifier input voltage is simply shifted by a half cycle from the waveform shown here.

delivery system is reduced, providing a better performance in the overall system. An integrated prototype operating at a 50 MHz switching frequency and 2.5 V output voltage has been designed and fabricated in a TSMC 0.25 μm CMOS process to demonstrate and verify the concept. The prototype shows the advantages of the SC rectifier and validates the self-driven scheme in the SC rectifier. The proposed switched-capacitor rectifier provides improved voltage transformation capabilities as compared to a conventional bridge rectifier, making it suitable for applications where high power density and high voltage conversion ratio are desired.

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