Optimization of Integrated Transistors for Very High Frequency dc-dc Converters

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***Abstract*—This document presents a method to optimize integrated LDMOS (Lateral Double-Diffused MOSFET) transistors for use in very high frequency (VHF, 30-300 MHz) dc-dc converters. A transistor model valid at VHF switching frequencies is developed. Device parameters are related to layout geometry and the resulting layout vs. loss tradeoffs are illustrated. A method of finding an optimal layout for a given converter application is developed and experimentally verified in a 50 MHz converter, resulting in a 54% reduction in power loss over a hand-optimized device. It is further demonstrated that hot-carrier limits on device safe operating area may be relaxed under soft switching, yielding significant further loss reduction. A device fabricated with 3 um gate length in 20-V design rules is validated at 35-V, offering reduced parasitic resistance and capacitance as compared to the 5.5 um device. Compared to the original design, loss is up to 75% lower in the example application.**

I. INTRODUCTION

SMALLER and higher performance power converters see increasing demand as portable devices drive more compact form factors and higher power consumption. While there are a number of ways to sate this requirement, reducing power converter size is tantamount to reducing passive component volume. One approach is the direct reduction of passive component volume at constant energy storage. L-C-T structures embody this approach [1], [2] and have met with success in a number of areas.

Another means to achieve smaller passives is through a dramatic increase in switching frequency, which leads to a direct reduction in required energy storage enabling smaller power converters. The caveat to such an approach is that magnetic materials and semiconductor devices contribute frequency-dependent losses that yield poor converter efficiency as frequency is increased. This challenge is addressed through the use of soft-switching techniques and advanced converter architectures suited for VHF operation. Only a subset of semiconductor devices are suitable for VHF application and this paper focuses on their improvement.

The device losses that dominate in soft-switched VHF converters differ significantly from those of hard-switched operation. As a result only a small subset of commercially available power MOSFETs are suitable for this application. These tend to be discrete RF LDMOSFETs (Lateral Double-Diffused MOSFETs) that are too expensive and over-packaged for most power converter applications [3]–[12]. On the other hand, while desirable for their high degree of integration, most semiconductor processes for power conversion are intended for operation below a few megahertz. Optimization of these devices for hard-switched operation has driven process, design-rule, and layout tradeoffs [13]–[15] that produce devices with excellent hard-switching performance, but marginal VHF performance.

In this paper we show that reconsidering device optimization with a different set of loss metrics leads to greatly improved VHF performance. This opens the possibility of realizing highly integrated VHF converter designs that use inexpensive silicon processes. Since device loss drives the optimization, we begin by identifying the mechanisms particular to resonant converters in the VHF regime in Section II. These losses are cast in terms of a set of intrinsic device parameters that are easily measured. In turn, a set of layout parameters is chosen to uniquely define a layout geometry in Section III. The number of parameters is held to the minimum necessary to realize performance gains so that the optimization can be accomplished within a reasonable amount of time.

By way of metrics, we compare computer-optimized device layouts against one that was provided as a hand-optimized sample in the same LDMOS power process. We additionally baseline the process performance against a discrete power device optimized for RF operation. The power process utilized

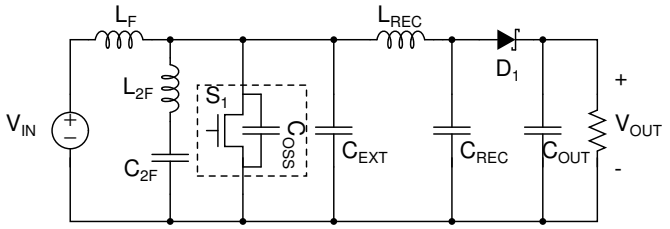


Fig. 1: Φ_2 resonant boost converter with C_{OSS} and the external capacitance C_{EXT} explicitly drawn.

is a 50V BCD (Bipolar, CMOS, LDMOS) process with a 700 um minimum feature size, LDMOS power devices with scalable gate-plus-drift-region lengths from 3 um to 5.5 um allow breakdown voltages up to 50V. Losses are reduced by 54% when the proposed layout optimization is employed.

Further benefit arises through relaxation of the safe operating area (SOA) constraints normally specified for devices under hard-switched operation (Section IV). In particular, we demonstrate that devices can be operated under soft-switching at higher peak voltages than those normally specified for hard-switching. This allows devices with shorter gate lengths to be used for a given application. In this case, 3 um devices are substituted for 5.5 um devices. Thus, in the intended converter application smaller parasitic resistance and capacitance obtains, reducing device loss and improving overall converter efficiency.

In a case study we show that the combination of layout optimization and relaxation of the SOA leads to better than 74% reduction in device loss for LDMOSFETs fabricated in the integrated power process used for this work. The VHF performance of the optimized devices is verified through the construction and testing of two converters. Results are presented in Section V.

II. VHF Device Loss Model

A. Overview

Semiconductor device losses place critical limits on the design and performance of power converters. As a result, significant effort has been devoted to the optimization of power devices. Most converters operate under hard-switching conditions, or at frequencies below a few megahertz, and optimization has focused on reducing loss under these conditions. This has led to devices that are very good for these applications, but do not realize the potential of power silicon in the VHF regime. In this work, optimization is accomplished for the set of device losses that result when soft switching is employed to attain very high switching frequencies. This requires a model that captures the loss mechanisms and their scaling behaviors as identified in Section II-B.

B. VHF Device Losses

To construct a model for VHF operation it is first necessary to consider the loss mechanisms of interest and their scaling behaviors. In general, to achieve extreme high frequency operation requires a means of rescaling or otherwise mitigating

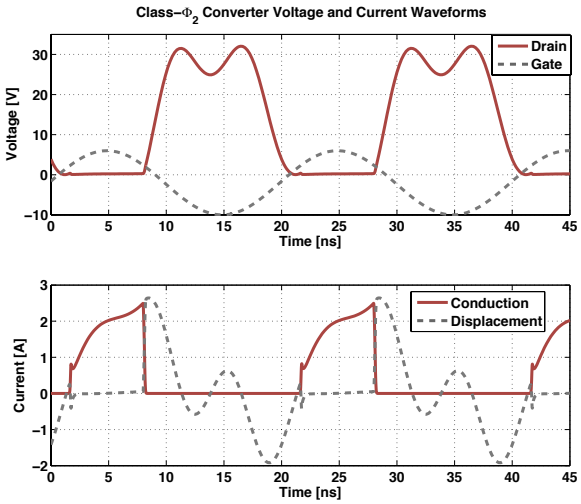


Fig. 2: Simulated Φ_2 resonant boost converter switch voltage and current waveforms.

frequency-dependent loss. This gives rise to the differences that merit a new device optimization. One example of a circuit topology that rescales and mitigates frequency-dependent loss is the Class-Φ_2 converter illustrated in Figure 1 [9]. It employs fully-resonant soft-switching and soft-gating to achieve efficient operation in the VHF regime. It is used here to illustrate the important VHF loss mechanisms and to provide experimental validation of improvements derived from device optimization.

The Φ_2 voltage and current waveforms (Figure 2) elucidate the device loss and scaling behaviors that form the basis for the proposed optimization. These waveforms derived from a SPICE simulation of a Φ_2 converter at 50 MHz with the input voltage set to 14.4 V, the output voltage set to 33 V, and P_{OUT} set to 12 W. The simulation models inductor and capacitor Qs as well as the power device losses using the model described in this paper.

Further details of the modeling and simulation of Φ_2 converters can be found in [3], [9]. The drain- and gate-voltage waveforms, V_{DS} and V_{GS} respectively, are plotted together with the drain current. The latter is subdivided into conduction current, i_{cond}, that flows through the active channel when the device is turned on and displacement current, i_{disp}, that flows through the device output capacitance, C_{OSS}, when the device is turned off. Owing to a soft-switching trajectory enforced by the Φ_2 network [3], V_{DS} and i_{cond} have almost no overlap and therefore no overlap loss over a switching cycle. Similarly, before the device is commutated V_{DS} approaches zero and capacitive discharge loss is also eliminated. This mitigation of switching loss is accomplished through the resonant action of the converter network. A similar fully-resonant scheme is employed to reduce gating loss [5], [16]–[18]. These techniques allow an increase in frequency, but they also change the relative importance of the various losses.

Of the device losses that dominate VHF operation, conduction loss remains the most similar to the hard-switching case. It behaves as an i^2R loss. The RMS conduction current,

$i_{cond,RMS}$, is independent of frequency as is the on-state resistance, R_{DS-on}. Therefore, even as frequency is scaled into the VHF regime, conduction loss remains significant and sets the minimum device area necessary to process a given amount of power.

In contrast to conduction loss, the frequency-dependent losses behave differently from the hard-switching case. With overlap and capacitive discharge mitigated, what remains in terms of switching loss is the circulating current i_{disp}. This current circulates through the output capacitance. A resistance, R_{OSS}, which includes the drain access resistance, the bulk resistance, and drain-source metal resistance, appears in series with C_{OSS} giving rise to loss. As a result the displacement loss, as it is referred to here, takes the form of an i^2R loss. Gating loss under the assumption of resonant gating takes the same i^2R dependence, since a current i_{gate} circulates through the gate capacitance and its equivalent series resistance, R_{GATE}. R_{GATE} is composed of the source access resistance, poly resistance, and gate metal resistance.

An important consequence of the i^2R scaling of the frequency-dependent losses under soft-switching is their behavior as a function of frequency. This can be determined by establishing how i_{disp} and i_{gate} scale. In each case, the currents flow in a circuit branch that comprises a device capacitance in series with an equivalent resistance where the impedance is dominated by the capacitance. As frequency scales, the capacitor impedance falls linearly resulting in a linear increase in the branch current. This implies that both displacement and gating losses scale with the square of frequency, since loss is dependent on i^2_{RMS} in each case. In contrast, both gating and switching losses under hard gating scale proportionally to frequency. With respect to device parameters, an increase in capacitance corresponds to a proportional increase in current and a square-law increase in loss. Scaling with respect to resistance is linear. Table I outlines the device loss mechanisms and their scaling behaviors for both hard- and soft-switching cases.

The loss mechanisms discussed above are captured in Figure 3. It is a simplified model that allows rapid calculation of loss within the framework of an optimization, yet provides a good estimate of loss as demonstrated in Appendix 1. The resistances R_{DS-on}, R_{OSS}, and R_{GATE} correspond to the three important VHF device loss mechanisms: conduction loss, displacement loss, and gating loss. C_{ISS} and C_{OSS} are the lumped input and output capacitances. In each case, these represent equivalent linear capacitances. The capacitance value is chosen by first determining the R.M.S. current in each capacitor, which comes from the waveform and the particular C-V curve of the non-linear capacitor. Once an R.M.S value is determined, a linear capacitor can be chosen that gives the same R.M.S. current. This technique works well in the VHF design space because the waveform shapes are held fixed over a wide range of the design space. The coupling from the drain to the gate via C_{GD} is ignored in favor of lumping it with the input and output capacitances. This simplification is possible because a prerequisite of VHF operation is a small C_{GD} relative C_{GS}. In addition to the small C_{GD}, the soft-switching, zero dv/dt operation of these converters also aids in this simplification.

TABLE I: VHF vs. Hard-Switched Loss Mechanisms

Loss Mechanism	Hard-Switched	Soft-Switched VHF
Conduction	$\propto I^2_{cond,RMS}R_{DS}$	$\propto I^2_{cond,RMS}R_{DS}$
Gating	$\propto C_{ISS}f_{SW}$	$\propto C^2_{ISS}R_{GATE}f^2_{SW}$
Off-State Conduction	N/A	$\propto C^2_{OSS}R_{OSS}f^2_{SW}$
Overlap	$\propto f_{SW}$	N/A
Cap. Discharge	$\propto C_{OSS}f_{SW}$	N/A

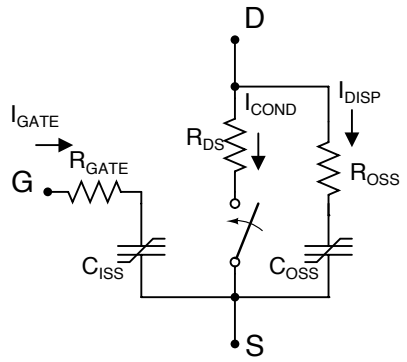


Fig. 3: MOSFET model with loss elements relevant under soft-switched VHF operation

Equation 1 makes explicit the relationships among device, circuit, and loss. It parameterizes loss in two separate sets of variables, the intrinsic resistances and capacitances of the semiconductor device and circuit constants (K_1, K_2, K_3) derived from the circuit in which the device is employed. This facilitates optimization of the device because once a circuit design is established device performance is only a function of the intrinsic characteristics of the device, which are in turn related to the semiconductor process and layout geometry. Regarding the circuit constants, K_3 is shown for sinusoidal resonant gating. Other schemes such as trapezoidal resonant gating [16] result in different relationships. The currents, $i_{cond,RMS}$ and $i_{disp,RMS}$ are circuit dependent and may be found by SPICE simulation, or directly calculated depending on the circuit topology.

The addition of an external capacitance in parallel with C_{OSS}, C_{EXT}, is a technique often used for VHF converters. It establishes a particular drain-source impedance for proper circuit operation [3], [19]. For a given converter design, the total drain-source capacitance is held constant. In the case of device optimization, where minimizing loss dictates a certain C_{OSS}, C_{EXT} is adjusted to compensate the total drain-source capacitance. This allows the optimization of the device without requiring that the circuit parameters be recalculated. It also permits trading the conduction loss against the displacement and gating losses because total device area is scalable independent of the circuit design. For instance, in the case of displacement loss the total circulating current during the off-state is shared between C_{OSS}, a relatively lossy capacitance, and C_{EXT}, a capacitor with much higher Q. Therefore, reducing die area corresponds to a decrease in displacement loss as C_{EXT} carries a larger fraction of the off-state circulating currents. These relationships typically lead to

TABLE II: Measured Device Parameters

Parameter	MRF6S9060	Integrated LDMOS (F)
R_{DS-ON}, V_{GS} = 8 V, 25°C	175 mΩ	200 mΩ
C_{OSS}, V_{DS} = 14.4 V	50 pF	132 pF
R_{OSS}	170 mΩ	500 mΩ
C_{ISS}	110 pF	275 pF
R_{GATE}	135 mΩ	1300 mΩ
P_{TOT}	288 mW	915 mW

an optimal device size as discussed in Section II-C.

$$\begin{aligned} P_{TOT} &= P_{cond} + P_{cond-off} + P_{gate} \\ P_{cond} &= K_1 \cdot R_{DS-ON} \\ P_{cond-off} &= K_2 \cdot R_{OSS,eq} \cdot C_{OSS,eq}^2 \\ P_{gate} &= K_3 \cdot R_{GATE,eq} \cdot C_{ISS,eq}^2 \end{aligned} \quad (1)$$

$$\begin{aligned} K_1 &= I_{cond,RMS}^2 \\ K_2 &= \left(\frac{I_{disp,RMS}}{C_{TOT}}\right)^2 \\ K_3 &= 2(\pi \cdot V_{gate,AC-pk} \cdot f_{SW})^2 \end{aligned}$$

$$C_{TOT} = C_{OSS,eq} + C_{EXT}$$

The model outlined above can be used to make comparisons between devices given a target power converter design. Here a Class-Φ_2 resonant boost converter switching at 50 MHz is enlisted as a case study. This design has V_{IN} = 12 V, V_{OUT} = 33 V, P_{OUT} = 12 W, C_{TOT} = 143 pF, $i_{disp,RMS}$ = 954 mA, $i_{cond,RMS}$ = 1040 mA, and $v_{gate,AC-pk}$ = 8 V. To establish a performance baseline a discrete RF-optimized LDMOSFET, the Freescale MRF6S9060, is compared to a custom LDMOSFET fabricated on an integrated BCD power process. Table II shows that in the case study the discrete RF transistor dissipates only 288 mW, while the integrated device dissipates 915 mW. This difference highlights a need for optimization.

C. Device Scaling Considerations

By applying scaling relationships to intrinsic device parameters, operating frequency, and circuit components it is possible to identify an optimal ratio between device area and converter power as well as an optimal operating frequency. The applied scalings assume first-order relationships, for example doubling device area doubles each capacitance and halves each resistance. While the true scaling is more complex, a first-order analysis is useful because it provides the basis for an overall optimization scheme.

The parameters of interest are the device losses: conduction, displacement, and gating losses, and their behavior as device area, A, switching frequency, f_{SW}, and converter output power, P_{OUT} are scaled. By asserting that: i) capacitance scales in direct proportion to area, ii) resistance scales inversely with area, iii) i_{disp} is proportional to P_{OUT} and f_{SW}, iv) i_{cond} is proportional to P_{OUT}, v) C_{TOT} is proportional to output power, and vi) i_{gate} is proportional to f_{SW}, the following relationships are established:

$$\begin{aligned} P_{cond} &= k_1 \cdot \frac{P_{OUT}^2}{A} \\ P_{disp} &= k_2 \cdot f_{SW}^2 A \\ P_{gate} &= k_3 \cdot f_{SW}^2 A \end{aligned} \quad (2)$$

Normalizing by output power yields:

$$P_{TOT} = k1 \cdot \frac{P_{OUT}}{A} + k2 \cdot \frac{f_{SW}^2 A}{P_{OUT}} + k3 \cdot \frac{f_{SW}^2 A}{P_{OUT}} \quad (3)$$

where k_1, k_2, and k_3 are constants to relate the scaling parameters to the actual loss. Equation 3 implies that an optimum ratio between device area and output power exists given the choice of circuit and semiconductor process because the conduction loss term has a power-area dependence opposite that of the frequency-dependent terms. This is illustrated in the top plot in Figure 4. It is generated in MATLAB by plotting the sum $P_{disp} + P_{gate}$ from Equation 2 (the straight lines) and P_{cond} the curved lines while fixing f_{SW}, selecting 3 values of P_{OUT} and scaling A. At each output power level the conduction and frequency dependent losses cross and an optimum area exists. However, as power is scaled the optimum area scales in direct proportion exposing the optimum ratio between device area and power. The latter is intuitive upon imagining the paralleling of two identical converters operating at the same power and efficiency. The device area doubles along with the output power and branch currents maintaining a constant loss density and equivalently, efficiency.

The middle plot in Figure 4 compares the conduction and frequency-dependent losses versus normalized device area with frequency as a parameter. This plot is generated in MATLAB by plotting the sum $P_{disp} + P_{gate}$ from Equation 2 (the straight lines), P_{cond} alone (which shows as a single, red, curved line because conduction loss is independent of frequency), and the sum $P_{cond} + P_{disp} + P_{gate}$ (representing the total device loss and showing as the three gray curved lines) while fixing P_{OUT}, selecting 3 values of f_{SW} and scaling A. As frequency is increased, the switching and gating losses increase quadratically as expected. This results in a continually decreasing optimal area. Comparing the total loss at the optimal area for each frequency point reveals a linear dependence despite a quadratic increase in the frequency-dependent losses. This obtains because area scaling of the device with converter design frequency allows the exchange of frequency-dependent loss for conduction loss.

Bottommost in Figure 4 is a plot of the total device loss (Equation 3), air-core inductor loss (expressed as $P_{inductor} = k_4/\sqrt{f_{SW}}$), and total converter loss ($P_{TOT}+P_{inductor}$) versus normalized frequency. The device loss is plotted at the optimal device area for each frequency point. This is accomplished in a MATLAB script by scaling the area to minimize total device loss for each frequency point on the plot. The quadratic tail is an artifact. It arises at very low frequencies because the maximum normalized area was limited to 10. Air core inductor loss is approximated as inversely proportional to the square root of frequency. This is because a linear increase

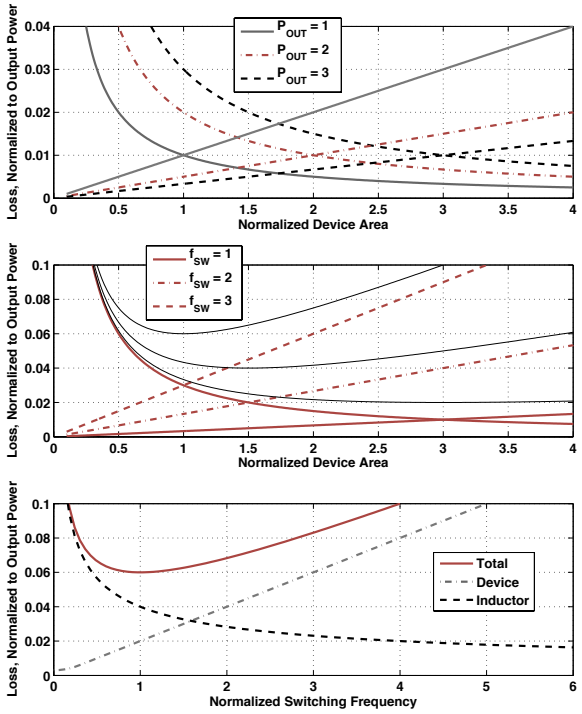


Fig. 4: Top: Plotting conduction loss (curved lines) and frequency-dependent losses (displacement and gating loss, straight lines) vs. normalized device area reveals an optimum ratio of normalized area to output power. Middle: Frequency dependent losses scale quadratically with frequency, but the total device loss is linear when area is simultaneously adjusted for minimum loss. Bottom: When inductor loss is considered, an optimum operating frequency given semiconductor process, circuit, and operating point.

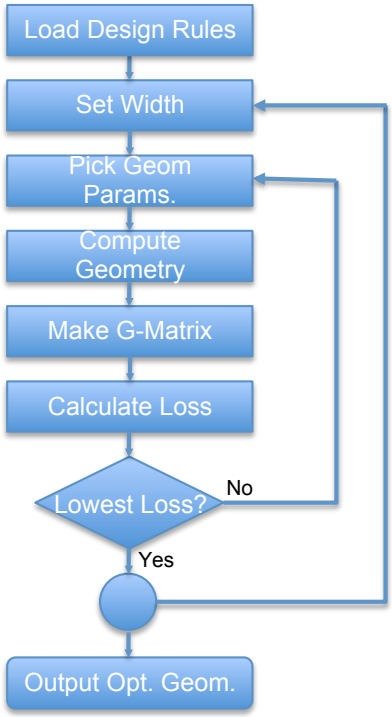


Fig. 5: Optimization flowchart

in reactance (and therefore inductor Q) is partially offset by a square-root rise in AC resistance owing to skin effect. As a result, the device loss and inductor loss have opposite behaviors and an optimum frequency exists given the circuit topology, process, and intended operating conditions. For the power semiconductor process and circuits considered here, this ranges between about 50 MHz and 100 MHz.

III. Layout Optimization

A. Overview

Power device optimization can be addressed on several levels. These include making changes to the process recipe, design rules, and layout. Among these options, layout changes typically represent the least investment in time or capital, but still offer substantial gains. Layout optimization is the focus of this effort. In order to realize the full benefit of layout modification, edge and interconnect effects must be considered in addition to scaling as discussed in Section II-C. For instance, as a device grows in size, metal resistance becomes a significant concern. Similarly for a small device, or devices comprising a very large number of small cells, capacitances along the diffusion edges, which do not scale with cell conductance, become significant. The relative importance of these parameters to the device parasitics identified in Equation 1 also depends on frequency, aspect ratio, and back-end process parameters such as the size and spacing requirements of inter-metal vias. These must be evaluated simultaneously to find an optimum layout for a given circuit design.

The optimization algorithm used here looks at all layout changes in concert. It is depicted in Figure 5. The outer loop finds the optimal device effective gate width (roughly corresponding to the device area discussed in Section II-C), and the inner loop finds the best geometry given the chosen width. As a result, at each width the best geometry is determined and the width that provides the lowest total loss is the best overall geometry.

B. Layout Description

A layout framework was first decided upon by excluding layouts that would clearly not result in an optimum as well as those which could not meet the process design rule criteria. As a result, the optimized power transistor consists of a 2-dimensional array of transistor cells with their drains, gates, and sources interconnected in parallel. This layout can be defined in terms a set of parameters and the process layout rules. Once the two are combined a unique layout is defined. The subsequent optimization is performed on the chosen parametrized layout. As a result, it does not include all possible layouts. However, the strategy does not preclude dealing with other layouts. Rather, it favors a layout framework that starts with what industry standard practice has converged on given the constraints of modern silicon processing and performance.

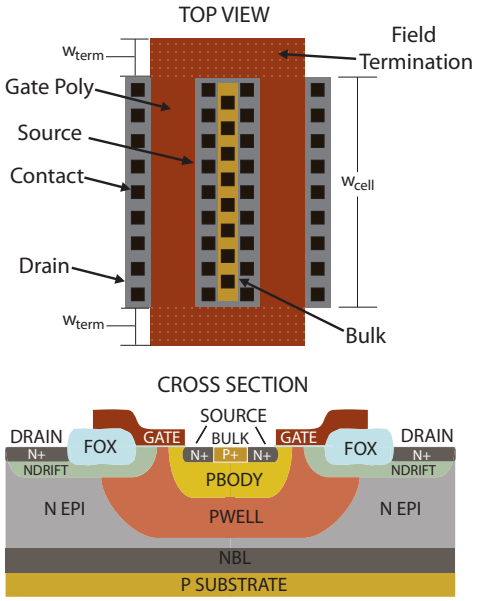


Fig. 6: The top view and cross-section of a single LDMOS cell. All the dimensions are fixed excepting w_{cell} which is scalable.

A single cell is depicted in Figure 6 and represents a gate finger that is a rectangular ring of polysilicon defining two channels with shared source and bulk diffusions and a drain diffusion along each vertical length of polysilicon. The width of the cell is a free variable that determines the balance of the cell geometry. The array of these cells that forms the complete transistor is packed such that adjacent columns of cells share their drain diffusions and adjacent rows of cells abut at their gates. This results in both the minimum parasitic capacitance and metal resistance for all considered geometries and is therefore a basic layout constraint.

Three layers of metal interconnect are available in this process. It was determined that the most effective use of these layers is to connect all the gate fingers using metal-1. The width of the metal-1 gate interconnects, which run parallel to each row at the gate finger edges, was parameterized for optimization. The drains and sources of each row are interconnected using horizontal strips of metal-2. Adjacent rows of cells share a strip of metal-2 that connects their drains, while there is only one strip of metal-2 centered over the sources in each row. Viewed from the metal-2 layer one would see a repeating pattern of horizontal strips arranged: D-S-D-S....S-D where the drain strips at the top and bottom are only connected to a single row. The ratio of drain metal width to source metal width was also an optimization parameter.

Metal-3 is used to vertically connect across these metal-2 strips and bring the drains to the top of the device where the drain pads are located, and the sources to the bottom of the device and the source pads. The strips are interdigitated so that looking at the metal-3 layer one would see a vertical pattern of D-S-D-S...D. The number of metal-3 strips is a parameter to be optimized. The vertical metal-3 strips are tapered to keep current density more constant and therefore minimize loss. The taper angle is also a parameter.

Figure 7 is a detailed diagram of the interconnect showing the relationship between the cells and metal geometry. The bottom of the figure is at the metal-1 level and shows the individual transistor cells arranged in a grid. The horizontal metal-1 strips connect the gate fingers of each cell together and are shorted at each end creating a single gate connection for the entire power device. The alternating vertical strips of metal-1 connect to the the drain and source contacts of the cells and provide a means to connect to the next layer of metal. Drain contacts of adjacent cells share a single metal-1 strip (excepting cells on the edge) while the source contacts have one metal-1 strip per cell.

Moving up the diagram to the middle drawing, the metal-2 layer is represented. The dark horizontal stripes are metal-2 that form drain and source busses. The pink squares connect to the metal-1 drain and source straps on the layer below, which can be seen in the gaps between each metal-2 strip. The metal-2 strips labeled, "DRAIN," connect the drains of all the cells in two adjacent rows. The strips labeled, "SOURCE," only connect the sources of all the cells in a single row.

The topmost drawing in Figure 7 shows the device from the metal-3 level. The medium-blue metal-3 fingers are tapered to reduce loss. They aggregate all the metal-2 straps of drain and source interconnect by the yellow vias which can be seen to connect the metal-3 fingers to the metal-2 strips below. This puts all the drain and source connections in parallel creating a large power device from many small cells.

Each complete power transistor is divided into many-cell segments sharing ajacent gate pads. As a result gate pad arrays are placed at the outermost edges of the device running vertically, as well as between the segments running vertically. The number of segments is a parameter for optimization with a minimum of one segment. The maximum was constrained by the ability to bond the gates to the the available package type (a TSSOP in this case).

Two additional parameters are considered for optimization. The first is the aspect ratio of the device. This is the total length vs. the total height of the device. A high aspect ratio corresponds to few rows and many columns, and vice versa a low aspect ratio. The final parameter, device width, was discussed above and is the total gate width expressed as the sum of the equivalent gate width of each cell. All individual cells have the same effective width in a given layout geometry.

Since the process design rules place additional constraints on the layout of the device owing to minimum metal widths, metal-metal spacings, diffusion size and spacing, and so on, a complete device layout can be specified by picking the values of the seven geometric parameters mentioned above. These are repeated in Table III for convenience.

C. Layout to Device Parasitic Parameters

Once a layout is defined by choice of geometric parameters, the device parasitic parameters of Equation 1 can be calculated. This is accomplished by tabulating the contributions of each device element, whether cell or metal interconnect and computing aggregate values for the resistances and capacitances of interest.

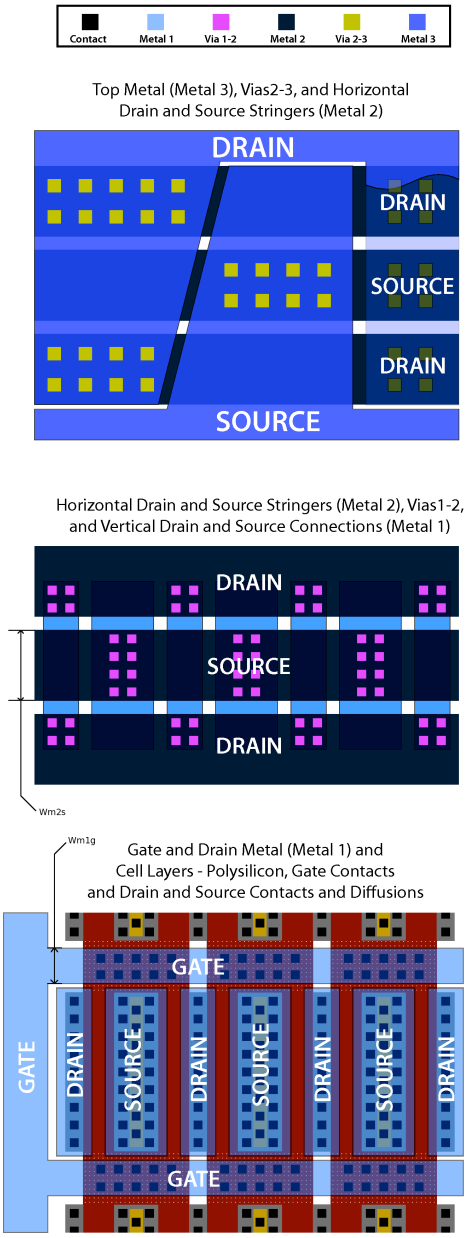


Fig. 7: A portion of a complete LDMOS layout showing the array pattern and interconnect. The bottom portion of the figure starts at the cell level and shows the gate interconnect, drain and source straps and adjacent cells. The middle diagram is at the metal-2 level showing how horizontal runs of metal-2 aggregate individual cells in parallel. The top layer details the metal-3 interconnect.

For the capacitances, this amounts to summing the various components of each transistor cell while accounting for junction edges, components that scale with cell width, those independent of cell width, and areal components. This data is derived from basic process characterization information and the formulae are widely available (see, for instance [20]). The same approach is used for the resistance components intrinsic to each cell, such as the gate polysilicon resistance and the access and drift resistances that define the channel and R_{OSS} components.

TABLE III: Optimization Parameters

Parameter	Importance to Device
Device Width	Sets intrinsic R_{DS-ON}, overall device size
Cell Width	Affects $R_{GATE}C_{ISS}$ and $R_{DS-ON}C_{OSS}$
Aspect Ratio	Trades drain/source and gate metal losses
w_{m1g}	Trades R_{GATE} and C_{OSS} and C_{ISS}
# metal-3 cuts	Drain-source metal resistance
angle metal-3 cuts	Drain-source metal resistance
w_{m2s}	Drain-source metal resistance
# gate bondpad arrays	Trades R_{GATE} and total device area

The resistance contributions of the metal are established from the resistivity parameters provided with the process documentation and the metal geometry itself. The latter requires dividing the metal layers, vias, and contacts into small pieces that are treated as individual resistances. These resistance components are placed into a conductance matrix that includes the cell conductances. The effective resistances required by Equation 1 are then determined by solving the matrix equation that results. This process is similar to that outlined in [14].

D. Optimization

The complete optimization process is managed using MATLAB scripts. The full details of the algorithms, scripts, associated mathematical descriptions and rule sets used to perform the optimization can be found in [21]. The circuit constants are determined by a target circuit design and provided as input variables. The flow follows the chart in Figure 5. An initial device width is chosen, then one layout geometry is generated for each permutation of the optimization parameters. This layout is used to compute the device parasitic parameters as outlined above. The resulting parameters are used in conjunction with the circuit parameters to compute the loss for each layout. The layout with the lowest loss is stored, and the next effective width is chosen. Once all the widths have been processed, the geometry with the lowest total width represents the optimum device.

The results of the layout optimization are detailed in Section V. They are baselined against a transistor in the same process that was optimized assuming scaling laws similar to those in Section II-C. The latter device was hand optimized to provide the capability of operating in the VHF regime, in contrast to the standard sample devices available for the process. By performing the optimization outlined above, which includes the effects of the interconnect and the resistance and capacitance effects caused by cell scaling and device aspect ratio changes, a 54% reduction in device loss was achieved for the case-study converter design from Section II.

IV. Safe Operating Area Considerations

Soft-switched converters are able to achieve high efficiency at VHF by avoiding voltage and current overlap in the switching device. The resulting switching trajectory closely follows the voltage and current axes for both turn-on and turn-off transitions. Figure 8 shows the simulated switching trajectories for a Class-Φ_2 boost converter and an ideal hard-switched boost converter. In the Class-Φ_2 converter the switch

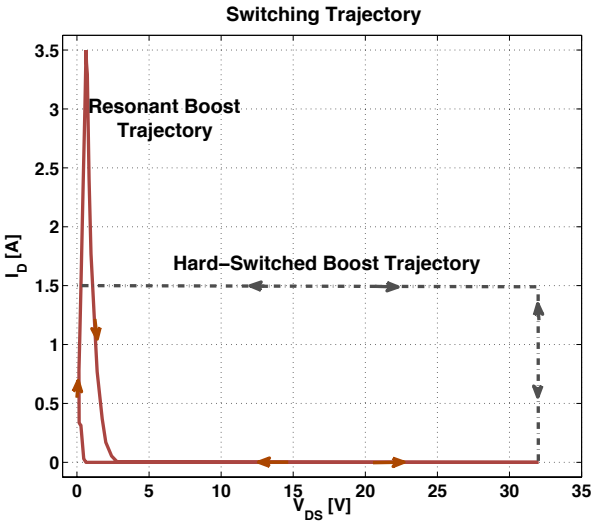


Fig. 8: Switching trajectory for Class-Φ_2 Boost converter and an ideal hard-switched boost for the same voltage and power level.

never has simultaneously high voltage and current, while under hard-switching the device experiences both high voltage and current simultaneously. The very different switch stress patterns that result have significant implications for the portions of the switch safe operating area that can be reached during operation.

Hot carrier effects result from the accumulation of damage in a device caused by high energy carriers [22]–[25]. For LDMOS devices, hot carrier effects manifest as shifts in threshold voltage, V_{TH}, or R_{DS-ON}. Threshold shifts are generally the result of hot carriers becoming embedded in the gate oxide. R_{DS-ON} shifts arise as hot carriers create interface traps in any of the lightly-doped drain region, the accumulation region under the gate, and/or the bird's beak region, located at the tip of the FOX-gate interface area. There is some overlap among effects.

Under normal operation, a small number of carriers will attain the energy necessary to cause damage. Over time, the damage accumulates and eventually the shift in V_{TH} or R_{DS-ON} becomes severe enough that the device is no longer useful. As the local electric fields increase, a larger fraction of the carrier population has sufficient energy and damage accumulates more rapidly. The simultaneous condition of high current and high fields is particularly bad, and ultimately requires a restriction on the safe operating area (SOA) to prevent operation in regions that will dramatically shorten the service life of the device. For LDMOS power devices hot carrier reliability, SOA, and R_{DS-ON} are tradeoffs [22], [23] controlled primarily via the drain drift region. To reach a desired safe operating voltage, while ensuring reliability, the device must have certain minimum dimensions and a carefully controlled doping profile. The consideration of hot carrier reliability thus imposes a tax on device design in the form of higher parasitic capacitance for a given R_{DS-ON}

In soft-switched VHF converters, device voltage and current are never simultaneously high. Without the conditions to create large numbers of hot carriers, device degradation does not occur, and we are free to extend the peak drain-source voltage towards the much higher avalanche limit. This extension of the SOA was validated through a set of experiments discussed in Section V. The result is significant in terms of VHF device performance. Without the need to constrain operating voltage in light of hot carriers, devices with a shorter drift region can be used. These devices will have substantially lower capacitance at a given R_{DS-ON}. Since frequency dependent loss in VHF resonant converters is square-law dependent on capacitance, the efficiency improvements are significant, as can be seen in Table V by comparing the HVx devices and MVx devices which have 5.5 μm and 3 μm gate lengths, respectively.

V. Experimental Results

A. Layout Optimization

Six LDMOSFETs fabricated in the same integrated power process are considered in this work. The process offers two different NLDMOS devices, one having a 2.5 μm active gate length and 3 μm drift region, the other having a 1.5 μm active gate length and a 1.5 μm drift region. The first device was fabricated using the 5.5 μm rules. It was provided by the process owner for VHF characterization purposes. The device was unable to be used at VHF owing to excessive gate resistance and very long gate fingers.

A second device was fabricated in 5.5 μm rules by the process owner in an attempt to be more compatible with the requirements of VHF operation. It is referred to as the "F" device in this paper. It has short gate fingers, a high aspect ratio, and interdigtated top-metal fingers, similar to the layout shown in Figure 7. These characteristics are typical of RF power devices, and the layout amounts to a hand optimization attempt for RF operation. The basic characteristics were greatly improved, including a reduction in gate resistance from 7Ω to 1.3Ω, allowing the device to used for VHF converter applications. The high aspect ratio and short finger lengths result in a device that is less area efficient than typical in this process where a hard-switched application is the target. However, it represents a starting point for VHF applications and it was used as a reference to assess the success of the layout optimization discussed in Section III.

While the F-device provides a control to establish the efficacy of layout changes within the process, the MRF6S provides a comparison to a high-performance discrete RF LDMOS power device. These devices, often used in the power amplifiers of cellular phone base stations, have been demonstrated to perform extremely well in VHF applications. Thus, the level of performance they achieve (the MRF6S, in particular) serves as a target against which the suitability of the process is baselined for VHF applications.

Optimization was performed on four separate devices for this work. Two 5.5 μm devices, the HV1 device with aluminum top metal and the HV2 device with copper top metal; and two 3 μm devices: the MV1 device with aluminum top metal and the MV2 device with copper top metal. The

TABLE IV: Measured Device Parameters

Device	R_{DS-ON}	R_{OSS}	R_{GATE}	C_{ISS}	C_{OSS}
MRF6S	175 mΩ	170 mΩ	135 mΩ	50 pF	110 pF
F	200 mΩ	400 mΩ	1300 mΩ	274 pF	132 pF
HV1	181 mΩ	145 mΩ	370 mΩ	266 pF	126 pF
MV1	113 mΩ	174 mΩ	300 mΩ	136 pF	97 pF
HV2	172 mΩ	165 mΩ	201 mΩ	268 pF	127 pF
MV2	112 mΩ	154 mΩ	133 mΩ	151 pF	108 pF

TABLE V: Calculated Loss Comparison

Device	Conduction	Displacement	Gating	Total
MRF6S	189 mW	93.8 mW	5.2 mW	288 mW
F	216 mW	310 mW	308 mW	835 mW
HV1	196 mW	102 mW	82.7 mW	381 mW
MV1	122 mW	72.9 mW	17.5 mW	213 mW
HV2	186 mW	118 mW	45.6 mW	350 mW
MV2	121 mW	79.9 mW	9.6 mW	211 mW

converter operating point requires the HVx devices to meet the peak V_{DS} excursions during normal operation if the hard-switching SOA rules are applied. However, under soft-switching the hot-carrier discussion in Section IV allows SOA extension, and the MVx devices were fabricated specifically to take advantage of the relaxed hot-carrier constraints. It should be clear that the latter devices with significantly shorter gate lengths benefit from a lower specific on resistance and smaller capacitance, which enhances their VHF performance. The parasitic parameters of the four optimized devices, the F-device, and the discrete RF device are detailed in Table IV.

The F, HV1, and HV2 devices have an effective width close to 7.2 cm. This was the as-provided width for the F device. The same width was chosen for HV1 and HV2 to provide a reasonable basis for comparison. Device optimization was performed on HV1 and HV2 as described above. Table IV shows that the optimization had the greatest effect on R_{GATE}, dropping from 1.3 Ω in the F-device to approximately 200 mΩ in the HV2 device. This is a direct consequence of changes to gate layout driven by the optimizer. The F-device has 13 1800 μm x 2.7 μm gate metal strips connected to a gate pad array at one end of the device. In contrast, the HV1 device has 3 gate pad arrays. One pad array is located at each end of the device and the third splits it into two halves. The nine gate strips in HV1 are nearly twice as wide and less than half as long at 800 μm x 5.7 μm. HV2 has a similar gate metal layout, but the top drain-source metal is copper allowing a more square device (F and HV1 are about 500 μm x 2 mm, where as HV2 is about 1.1 mm x 1.3 mm). This doubles the number of gate stringers dropping the total gate resistance to 201 mΩ. CAD drawings of the F-device, HV1 and HV2 are provided in Figure 9.

The HV1 and HV2 devices also have 35 μm cells in contrast with the F device's 25 μm cells. This slightly reduces input and output capacitance, which also shows up in Table IV. It additionally allows for wider metal-2 conductors (the largest source of resistance in the drain-source metal for these high aspect ratio devices) in the drain source path. In conjunction with a somewhat shallower metal-3 angle in the HV1 device, a modest reduction in metal resistance was achieved, contributing to a lower R_{DS-ON}. In the HV2 device, metal-2 and metal-3 are paralleled to further reduce the contribution from the drain and source stringers, and copper is used in place of metal-3 for the topmost layer.

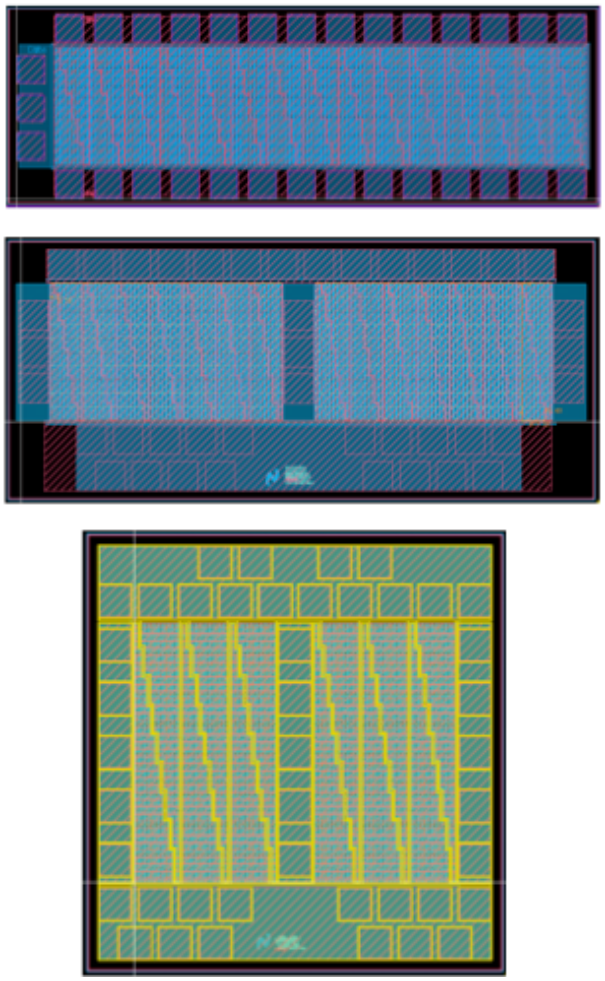


Fig. 9: The top device is the F-device originally hand-optimized for RF. The middle device is HV1, optimized using the algorithm in Section III. The bottom device is HV2. The copper top metal allows a much more square aspect ratio yielding substantial reduction in R_{GATE} as compared to the other devices.

The overall reduction in loss among the 50-V devices from layout optimization alone is substantial, as Table V shows. The losses are calculated from the experimental device parameter measurements using Equation 1 and the same example converter parameters provided in Section II. It should be noted that the F device is not a typical example of a power device in this process. The choice of high aspect ratio and short finger length was an attempt to achieve a device compatible with VHF operation. Full optimization allowed a further improvement of the $R_{DS-ON} \cdot C_{OUT}$ product. After layout optimization alone, the HV devices have a reduction in loss of up to 54%.

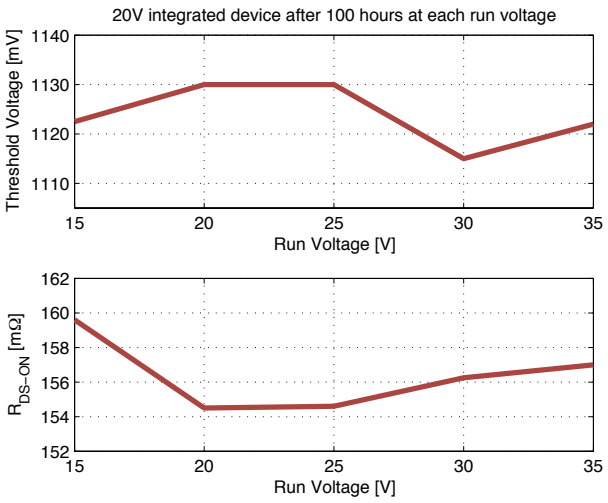


Fig. 10: The shifts in V_{TH} and R_{DS-ON} are well within the established testing criteria.

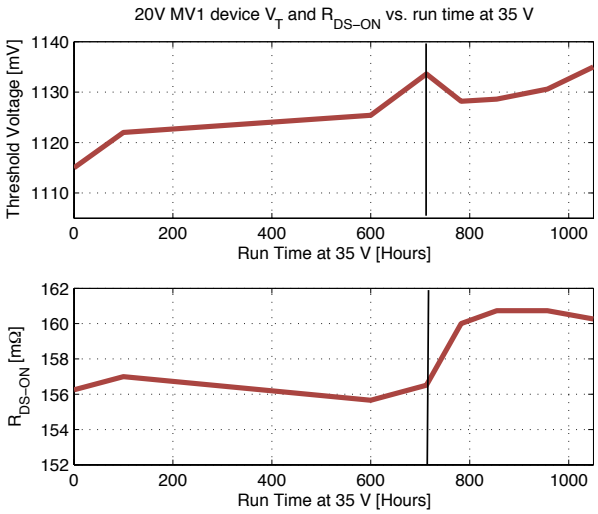


Fig. 11: After 1000 hours of operation at 35V, the 20V MV1 device has a total V_{TH} shift of around 20mV, and about a 4% change in R_{DS-ON}. The allowable maximums are 100mV and 10%, respectively.

B. Safe Operating Area

The MV1 and MV2 devices provide even better performance. The 3 um design rules allow for a shorter drift region and lower specific on resistance. When these devices are compared to the discrete MRF6S9060, in the example 50-MHz Φ_2 converter, they achieve the same total loss. This means that in the intended application at 50-MHz the integrated process can achieve parity with a discrete RF LDMOS device picked from among the best available.

While improved performance is expected from a device with a shorter gate length, the point of interest is that it can be used in this application at all. In the experimental converters constructed to test these devices, the peak drain voltage attained during operation is 35 V, a 75% increase over the rated voltage of the MV1 and MV2 devices. As discussed in Section IV, the mechanism that enables this is a switching trajectory that never has simultaneous high voltage and current. This minimizes hot carrier effects, allowing the MV1 and MV2 devices to be used at peak voltages closer to their avalanche voltage which is around 40 V. The result is that a 3 um device with lower capacitance and resistance at a given gate width can be substituted for a 5.5 um device and yield substantially better performance.

To assess hot carrier reliability in this process under soft-switching we used typical hot carrier reliability criteria. These require the device to run for 1 year at 10% duty ratio, or a total of about 876 hours. To meet standards R_{DS-ON} must shift by 10%, or less, and V_{TH} by 100 mV, or less. In order to evaluate our devices, we ran the device in a Class-Φ_2 resonant boost converter (see Figure 12 and Table VI) at successively higher voltages for 100 hour periods. The test started with a peak V_{DS} of 15 V. Once 35 V was reached, the converter was allowed to run for an additional 1000 hours. In terms of the test this is more than adequate, particularly in light of the fact that hot carrier damage occurs primarily at switching transitions. Since the test converter ran at 50 MHz, the total number of transitions is at least 50x what would be expected of a hard-switched converter. Therefore, were typical hot-carrier mechanisms operating, damage would have accumulated rapidly.

Testing began by measuring V_{TH} and R_{DS} of a new device, in this case an MV1 device. Threshold voltage was determined by holding V_{DS} at 100 mV and measuring the V_{GS} that results in a current density of 0.1 μA/μm. R_{DS-ON} was measured with V_{GS} = 5 V and V_{DS} = 100 mV. Over the course of testing, the converter was periodically stopped and the device measured. The plots of Figures 10 and 11 show the accumulated results. Both the threshold voltage and on-state resistance lie well within the requirements. The total threshold shift was approximately 20 mV after 1000 hours of running with a peak V_{DS} of 35 V, and the shift in R_{DS-ON} was on the order of 4%. At 712 hours the converter input voltage was doubled, stressing the devices and producing the steep rise in R_{DS-ON} demarcated by the black line in figure 11. Even with this additional stress, the total shift is well within the evaluation criteria.

As a control, a hard-switched boost converter was designed around an MV1 device to operate at the same voltage and device dissipation level. The converter was then connected to an electronic load so that average current through the switch could be maintained near 1.75 A, identical to the Φ_2 resonant boost converter when the peak V_{DS} is 35 V. After an initial run of 100 hours with a peak drain source voltage of 20 V, little change in V_{TH} or R_{DS-ON} was observed. After the initial run, the converter was then operated for 5 minute intervals at successively higher peak V_{DS}. This short interval was picked because shifts were expected to appear rapidly as the device voltage increased outside of the SOA. At a peak V_{DS} of 30 V, no changes were evident. Upon increasing the peak drain-source voltage to 35 V, the same voltage at which another MV1 device operated for over 1000 hours under soft-switching, the hard-switched device failed in 18 seconds.

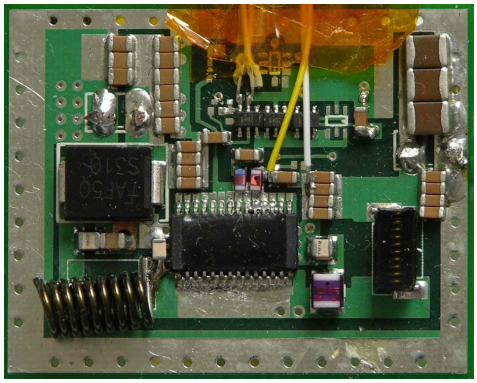


Fig. 12: A Class-Φ_2 boost converter built using the MV1 device and operated to 35V. It achieves 88% conversion efficiency at 12W, V_{IN}=12V, V_{OUT}=33V.

The soft-switching trajectory that permits SOA extension may not exist in the Φ_2 converter (or other VHF resonant converters) if the converter is not operating in steady state. For example, a typical method of controlling VHF soft-switching converters is full on-off modulation. [16]. During the start-up and shut-down transients, the switching trajectory will not always closely follow the voltage and current axes. During these periods, it is necessary that the trajectory does not leave the SOA defined for hard-switched converters, or significant hot carrier damage could occur. To assess the feasibility of operating an SOA-extended 20-V switch under these conditions, a Φ_2 converter was configured for modulation. Under modulation, the entire power stage is turned on and off at a frequency far below the switching frequency. In this case, a 50-kHz signal was used to modulate a 50-MHz converter. After running the converter with a peak V_{DS} of 35 V for 120 hours, there was no measurable shift in either V_{TH} or R_{DS-ON}.

The benefits of extending SOA are clearly delineated in Tables IV and V. The MVx devices enjoy a 76% reduction in loss over the original hand-optimized F device. The primary benefit comes from the lower specific R_{DS-ON}. This results in substantially lower capacitance and devices with an active area roughly 20% smaller than the HVx versions. The smaller dimensions also reduce the total interconnect length and the MV2 device, which has copper top metal and a small aspect ratio posts the lowest R_{GATE}, 133 mΩ. While the larger capacitances of the integrated devices over the discrete example (MRF6S9060) means that they won't scale as well in frequency, 50 MHz is sufficiently high to make converters with co-packaged energy storage a possibility.

C. Converters

To illustrate the gains from device optimization and SOA extension, two 50-MHz Class-Φ_2 resonant boost converters were constructed. The details are found in Table VI. One converter uses the hand-optimized F device with a 5.5 μm gate length. The other uses the MV1 device with a 3 μm gate length, which is layout optimized and operated with an extended SOA to a peak drain voltage of 35 V. The converter using the F-device achieves 75% conversion efficiency, and the converter with the MV1 device a substantially higher 88%. The device loss in the F-device converter and MITMV1 device converter is determined by using the device models described earlier. Respectively this is 1.62 W and 0.44 W. The models used to calculate these losses have been validated experimentally using thermal analysis as described in [26]. A photograph of the converter with the MV1 device appears in Figure 12.

TABLE VI: Experimental DC-DC Converter Specifications

Parameter	w/F LDMOSFET	w/ MV1 LDMOSFET
Device	5.5μm rules	3μm rules
Efficiency, V_{IN} = 14V	75%	88%
Loss in power device (model)	1.62 W	0.44 W
V_{IN} Range	8-18V	8-16V
V_{OUT}	33 V	33 V
P_{OUT}	17 W	17 W
D_1	Fairchild S310	Fairchild S310
L_F	22 nH	43 nH
L_{REC}	56 nH	90 nH
L_{2F}	22 nH	22 nH
C_{REC}	47 pF	24 pF
C_{EXT}	56 pF	47 pF
C_{2F}	115 pF	115 pF

VI. Conclusion

Through optimization of device layout significant improvement is possible for integrated power devices operating in the VHF regime. By further taking advantage of the switching trajectories inherent in soft-switched VHF designs, the hard-switching SOA for a device can be extended. This permits the use of devices at voltages higher than would otherwise be possible corresponding to the ability to use a 3 μm gate-length device in place of a 5.5 μm gate-length device. Extending the reach of a power process under soft-switching allows designers of VHF converters to take advantage of lower specific on-state resistance and the attendant performance benefits. In the 50-MHz example presented here, device loss is reduced by as much as 75% when layout optimization and SOA extension are used simultaneously. When hand-optimized and optimized devices are compared in a VHF converter application, conversion efficiency rises from 75% to 88%, similar to what has been achieved using RF-optimized discrete LDMOSFETS.

VII. Appendix 1: Thermal Loss Comparison

In order to validate the device loss model proposed above and to gain a better understanding of the power loss distribution in an example VHF converter, a thermal model of a Φ_2 converter was created. The thermal model starts by assuming a linear relationship between the power dissipated in a given element, and its temperature rise and the temperature changes of the surrounding components. In this case, an R-matrix reflecting the coupling from component to component is easily constructed. Once the R-matrix is known, taking the inverse and measuring the component temperatures during converter operation yields the power loss in each component. The system of equations is simply represented by:

$$\mathbf{T} = \mathbf{RP}$$

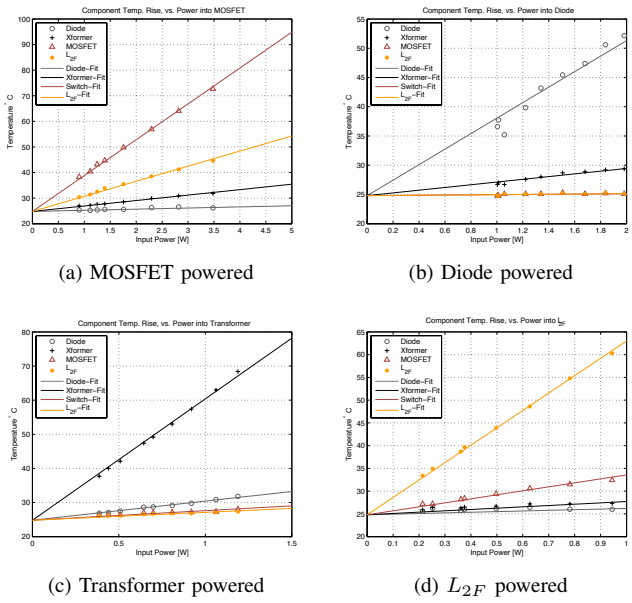
Where T is the vector of component temperatures, R is the thermal resistance matrix, and P is the power dissipation in each component.

The primary sources of power loss in the converter are the MOSFET, the diode, the transformer, and L_{2F}. A thermal camera was used to characterize the temperature rise of each of these components as a DC bias was applied to the component to simulate dissipation. For instance, in the case of the MOSFET small gauge wires were attached to the drain and source terminals and a current applied. The dc input power was measured and the temperature rise of the MOSFET, Diode, transformer, and L_{2F} were also measured. To check for linearity, the process was repeated for several values of input power. This provides the on-diagonal term in the resistance matrix for the MOSFET as well as coupling resistances to the other components. By repeating the procedure for the diode, transformer (the experiment was performed on the isolated Φ_2 prototype detailed in [26], and L_{2F}, the entire resistance matrix was populated. The R-matrix values are listed below for the second isolated Φ_2 prototype.

$$\mathbf{R} = \begin{bmatrix} 13.8 & 5.9 & 0.4 & 1.3 \\ 2.3 & 36.7 & 2.0 & 2.6 \\ 0.2 & 2.7 & 13.8 & 8.0 \\ 0.2 & 2.1 & 0.7 & 37.6 \end{bmatrix}$$

Figure 13 shows the plots of the temperature data and their curve fits as each device is successively swept over a range of drive powers. From the plots, it's clear that the behavior is quite linear over the range of interest. As a result, fitting to linear curves works well and the simple thermal resistance model is valid. Once the R-matrix was constructed, the inverse was calculated. The condition number of the R-matrix was low (the 2-norm condition is about 3.6) meaning that the system is not too numerically sensitive to invert.

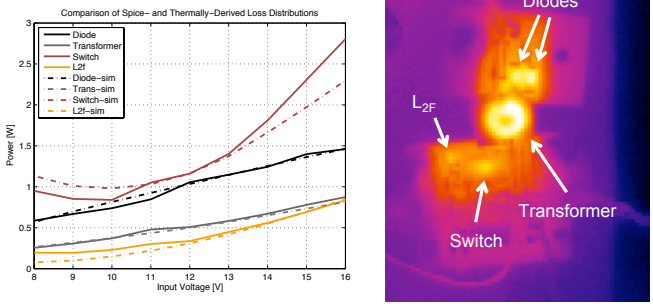
With R^{-1} available, the converter was operated over the input voltage range and temperature data taken via thermal camera. The temperature of each device was taken during operation once the system thermally stabilized. After the data was collected, power dissipation in each device was calculated according to the thermal model. Figure 14a shows the comparison of the loss distribution in the converter as measured thermally, versus the SPICE simulations. Agreement between the two is reasonably good over the operating range. In particular, the plots show that the agreement between the total MOSFET loss and the simulated loss is good over the entire power range of the converter. A thermal picture (Figure 14b) of one operating point shows the temperature measurement points used to determine the loss distribution.



(a) MOSFET powered (b) Diode powered

(c) Transformer powered (d) L_{2F} powered

Fig. 13: Power was injected to each major loss component successively and used to build a thermal model of the system. The linear behavior is evident from the plot and the successful curve fits to a linear model.



(a) Loss distribution SPICE vs. thermal (b) Thermal camera image of converter

Fig. 14: Results of thermal modeling show good agreement with SPICE and reveal the loss distribution in the converter. Data was obtained by repeated thermal imaging

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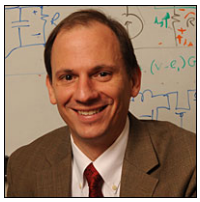

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