Design Methodology for a Very High Frequency Resonant Boost Converter

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Abstract—**This document introduces a design methodology for a resonant boost converter topology that is suitable for operation at very high frequencies. The topology we examine features a low parts count and fast transient response, but suffers from higher device stresses compared to other topologies that use a larger number of passive components. A numerical design procedure is developed for this topology that does not rely on time-domain simulation sweeps across parameters. This allows the optimal converter design to be found for a particular main semiconductor switch. If an integrated power process is used where the designer has control over layout of the semiconductor switch, the optimal combination of converter design and semiconductor layout can be found. To validate the proposed converter topology and design approach, a 75 MHz prototype converter is designed and experimentally demonstrated. The performance of the prototype closely matches that predicted by the design procedure, and the converter achieves good efficiency over a wide input voltage range.**

Index Terms - DC-DC power converters, Power transistors, RLC circuits, Tuned circutis, Schottky diodes.

I. Introduction

Increasing the switching frequency of DC/DC converters has the benefits of requiring less passive energy storage and providing improved transient performance. Since passive components typically dominate converter size, increasing the switching frequency is a crucial step in the development of a fully integrated or co-packaged power converter [1] and [3]. Among the challenges standing in the way of such developments, however, are loss mechanisms that grow with switching frequency [2]. Switching loss can be mitigated by using a circuit topology that operates with zero-voltage soft-switching to avoid both capacitive discharge and the overlap of voltage and current at the switching instants. Gating loss that arises from charging and discharging the gate capacitor each cycle can be reduced by using a resonant gate driver to recover a portion of the energy stored in the gate [2],[4]-[6],

and/or through transistor layout optimization [16]. Resonant rectification can be employed to mitigate rectifier switching loss [8], [9], and [18]. Once these frequency dependent device losses have been minimized, the converter can then be operated at a frequency high enough to use air core or low permeability RF core inductors to avoid the losses from high permeability magnetic materials.

This concept has been successfully demonstrated for boost conversion at frequencies up to 110MHz using a resonant boost Φ_2 converter topology in [6], [7], and [10]. This topology uses a multi-resonant network to shape the switch's drain-to-source voltage waveform to approximate a square wave with a peak value of $2V_{\text{IN}}$ (under ideal conditions). In this paper an alternative resonant boost converter topology is explored that uses fewer passive components but suffers from a higher peak drain-to-source voltage. We develop a design procedure for this topology that readily yields necessary component values. Unlike previous design methodologies for similar topologies [11],[12], the procedure introduced here is based on direct analysis of the topology and does not rely on lengthy time-domain simulation sweeps across circuit parameters to identify desirable design points.

Section II of the paper presents an overview of the topology and how it relates to previous RF converter designs. Section III of the paper details the proposed design method and illustrates how it is applied to design a converter. Section IV validates the proposed design methodology and presents experimental results from a 75 MHz converter. The performance of the prototype design is shown to closely match that predicted by the design procedure. Finally, section V concludes the paper.

II. Resonant Boost Converter Topology

A schematic of the power stage of the proposed converter is shown in Figure 1, and idealized waveforms illustrating its operation are shown in Figure 2. This converter topology operates with zero voltage switching by tuning the resonant

elements (L_F, L_R, C_E, and C_R) such that when the switch is opened, the drain-to-source voltage of the switch will naturally ring up and then back to zero half of a switching period later. The converter is designed to operate with fixed switching frequency and duty cycle. This makes available the use of highly efficient resonant gate drivers when desired. While varying the frequency or duty cycle is not used for control, an on-off modulation scheme can be employed in which the entire converter is switched on and off at a modulation frequency that is much less than the switching frequency of the converter [4]-[7],[12],[13], and [24].

It should be noted that aside from the important aspects of component values and control, the circuit of Figure 1 is topologically equivalent to the ZVS multiresonant boost converter of [14] and to the resonant boost converter of [13]. The difference in design between the converter of [14] and here is quite large owing to major differences in control (constant on-time variable frequency vs. burst mode control) and the resulting difference in the choice of component values. The design here is more similar to that of [13], but differs substantially from both [14] and [13] in that the inductor L_F in Figure 1 is a resonant inductor rather than a simple choke as in [14] and [13]. This design choice provides much faster response under on-off control than is achievable with a choke inductor and results in different design considerations and component selections.
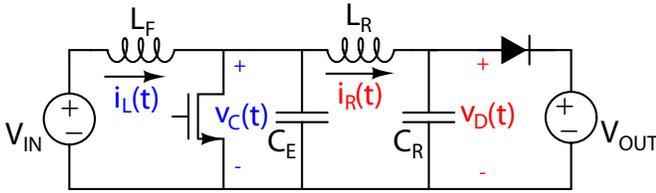
Fig. 1.   Power section schematic of the proposed boost converter

III. Design Methodology

Here we develop a design procedure for the proposed converter circuit that both provides insight into the converter's operation and is straight forward to use. Single-switch resonant power converters have often been designed through an iterative modeling approach, in which one starts from some approximate component values and searches for good designs through a series of time-domain simulations sweeping parameters (e.g. using SPICE simulations [12],[13],[24]). This approach is workable, especially for an experienced designer with good knowledge of a particular topology. However, due to the large number of parameters that can be varied, it is difficult for the designer to know if they have reached the optimal design. We seek to remedy this issue here. Additionally, when designing a converter where the main switching device will be fabricated from an integrated power process, the designer has the ability to change the layout of the device to vary the parasitics. Methods have been developed to find the optimal device layout
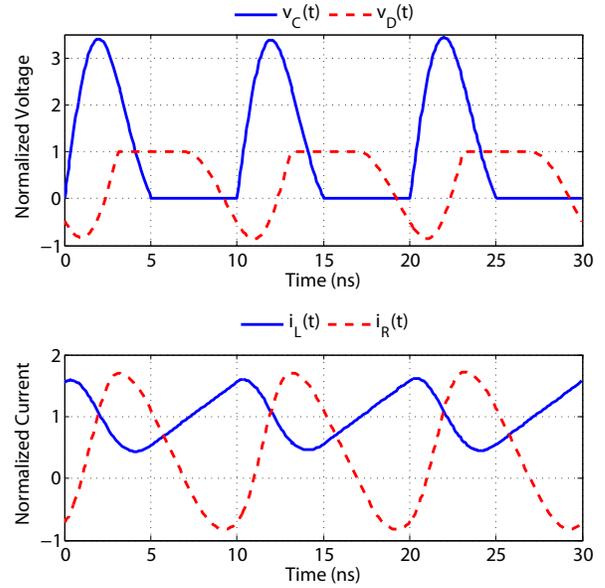
Fig. 2.   Idealized steady-state waveforms illustrating the operation of the converter shown in Figure 1. $v_C(t)$ is normalized to the V_{IN}, $v_D(t)$ is normalized to V_{OUT}, and the currents are normalized to the converter's input DC current.

for a particular converter design [16]. However, previous design methods for such circuits have not been sufficiently simple that one can easily vary both the device layout and the converter design to find the best possible combination. Enabled by the simplicity of this converter topology, a design procedure is developed here that aims to address these challenges.

With four energy storage elements, the converter is described by fourth order differential equations. Additionally, since the converter contains two switching devices, there are a four different circuit configurations possible. Thus, a comprehensive mathematical description of the converter requires four sets of fourth order differential equations. This is further complicated by the fact that the switching times of the diode are unknown. Clearly, deriving a complete set of closed form equations to directly describe the converter is a cumbersome and unfruitful task. For this reason, the simplifying assumption is made that the rectifier's LC tank, formed by L_R and C_R, is high Q and the current in inductor L_R, labeled i_{RECT}, is sinusoidal with a DC offset.

$$i_{RECT} = I_{AC} \sin\left(\omega_s t + \phi_1\right) + \frac{P_{OUT}}{V_{OUT}} \tag{1}$$

This allows the inverter and rectifier to be separated for analysis. The inverter design is then found by replacing the rectifier with a sinusoidal current source. Similarly, the rectifier design can then be found by replacing the inverter with a sinusoidal voltage source. Making this assumption simplifies the problem to the point where a converter solution is readily obtained, but at the cost of the accuracy. Since the current i_{RECT} is actually not purely sinusoidal, there will be some error in the solution. Typically the rectifier has a modest

loaded Q, and the error is small enough such that the designer can easily make small corrections to the resulting component values when simulating the converter in SPICE.
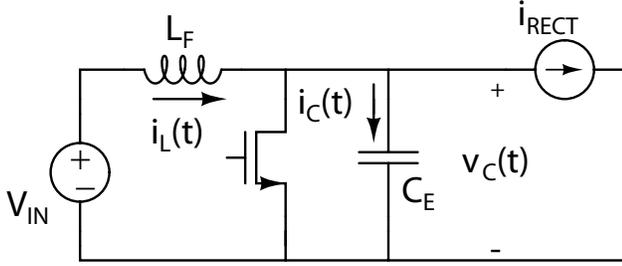
Fig. 3. Schematic of the inverter used for analysis with the rectifier modeled as a current source of value i_{RECT}

A. Inverter Analysis

In this analysis, the duty cycle of the inverter is set to 50% (a common design choice). This is not a fundamental limit, and is imposed in part to simplify the converter's equations. The reader can easily expand the design approach to accommodate arbitrary duty cycles. A schematic of the inverter is shown in Figure 3. With the duty cycle of a half, the time period $0 \leq t < T_S/2$ is defined as the period with the switch turned off, and $T_S/2 \leq t < T_S$ as the period with the switch on.

The analysis starts at $t = 0$, when the switch has just turned off. The node equations in this time period (with the switch off) form a second order differential equation for the voltage $v_C(t)$.

$$L_F C_E \frac{d^2 v_C(t)}{dt^2} + v_C(t) = V_{IN} - \omega_s I_{AC} L_F \cos(\omega_s t + \phi_1) \quad (2)$$

The general solution to this equation is:

$$v_C(t) = \frac{\omega_s L_F I_{AC}}{\omega_s^2 L_F C_E - 1} \cos(\omega_s t + \phi_1)$$
$$+ C_1 e^{-jt/\sqrt{L_F C_E}} + C_2 e^{jt/\sqrt{L_F C_E}} + V_{IN} \quad (3)$$

where C_1 and C_2 are constants. To solve for these constants, two initial conditions are required. The capacitor voltage at $t = 0^+$ is known to be 0 since the switch was turned on at $t = 0^-$. The initial inductor current is not known, and the constants are found in terms of the initial inductor current, $i_L(0)$, resulting in the following equation.

$$v_C(t) = Z_o \left[(r_o - 1) I_{AC} \sin\phi_1 + i_L(0) - \frac{P_{OUT}}{V_{OUT}} \right] \sin(\omega_o t)$$
$$- \left[\frac{Z_o \omega_s}{\omega_o} r_o I_{AC} \cos\phi_1 + V_{IN} \right] \cos(\omega_o t)$$
$$+ \frac{Z_o \omega_s}{\omega_o} r_o I_{AC} \cos(\omega_s t + \phi_1) + V_{IN}$$
$$\text{for } 0 \leq t \leq T_S/2$$
$$(4)$$

where

$$\omega_o = \frac{1}{\sqrt{L_F C_E}}, \quad Z_o = \sqrt{\frac{L_F}{C_E}}, \quad \text{and} \quad r_o = \frac{(\omega_s/\omega_o)^2}{(\omega_s/\omega_o)^2 - 1}$$

From Equation 4 we see that there are five unknown quantities that must be found: the resonant angular frequency and characteristic impedance of L_F and C_E (ω_o and Z_o), the magnitude and phase of the rectifier current (I_{AC} and ϕ_1), and the initial current in $L_F(i_L(0))$. (Hereafter, we refer to angle ϕ_1 as the "outphasing angle".) To solve for these unknowns, design constraints are applied to the system:

1) Since average power is only delivered by DC current from the source, the DC current in L_F is constrained by conservation of energy. (Averages are denoted with angled brackets, $\langle \rangle$.)

$$\langle i_L(t) \rangle = \frac{P_{OUT}}{V_{IN}} \quad (5)$$

where

$$i_L(t) = \frac{1}{L_F} \int_0^t (V_{IN} - v_C(t)) \, dt + i_L(0) \quad (6)$$

2) The inverter must operate in periodic-steady-state

- The average voltage across L_F must be 0.

$$\langle v_C(t) \rangle = V_{IN} \quad (7)$$

- The average current through C_E must be 0.

$$\langle i_C(t) \rangle = 0 \quad (8)$$

where

$$i_C(t) = \begin{cases} i_L(t) - i_{RECT} & 0 \leq t < T_S/2 \\ 0 & T_S/2 \leq t < T_S \end{cases} \quad (9)$$

Since the capacitor does not conduct any current when the switch is on and had an initial voltage of 0, this constraint is equivalent to setting the capacitor voltage to 0 at the switching instant. Thus, a separate constraint for zero-voltage switching is not required.

Application of these constraints to the circuit node equations results in three non-linear equations. Since there are five unknown quantities and only three constraints, the system has two free variables. An intuitive choice to illuminate of the design space is to leave ω_o and ϕ_1 unconstrained, and solve for the remaining unknown quantities (L_F, C_E, and $i_L(0)$) numerically in MATLAB. Figure 4 shows the solved values of L_F and C_E as a function of the current out-phasing angle ϕ_1 and the inverter's resonant frequency ω_o for a converter with input and output voltages of 12 and 30 Volts, an output power of 7 Watts, and a switching frequency of 75 MHz.
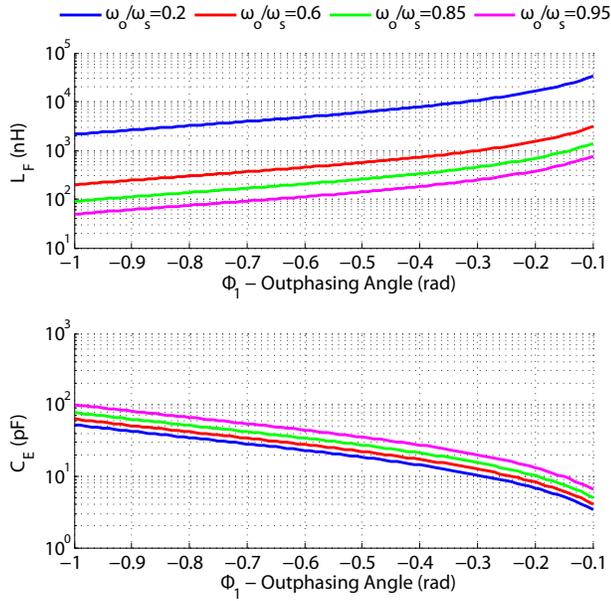
Fig. 4. Solved values of L_F and C_E as a function of the current out-phasing angle ϕ_1 and the inverter's resonant frequency ω_o for a converter with an input and output voltage of 12 and 30 Volts, an output power of 7 Watts, and a switching frequency of 75 MHz.

B. Rectifier Analysis

Similar to the approach taken for the inverter, the rectifier design is determined by replacing the inverter with a sinusoidal voltage source with a DC offset, labeled v_{INV} and shown in Figure 5.

$$v_{INV} = V_{AC} \sin(\omega_s t + \phi) + V_{IN} \quad (10)$$

V_{AC} and ϕ are the fundamental component and phase of $v_C(t)$ (the drain-to-source voltage of the inverter).
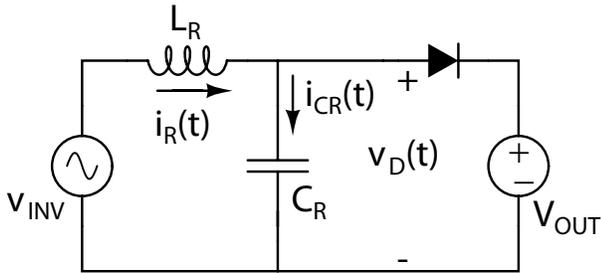
Fig. 5. Schematic of the rectifier used for analysis with the inverter modeled as a voltage source of value v_{INV}.

Unlike the inverter, the rectifier's duty cycle is unknown. When the diode turns on, the voltage $v_D(t)$ is held at V_{OUT}, and there is no current in the capacitor C_R. The diode turns off when $i_R(t)$ crosses zero, reversing the direction of current in the diode. While the diode is off the resonant circuit rings until $v_D(t)$ reaches V_{OUT} again and the diode turns back on.

For analysis the times that the diode turns on and off in a cycle are labeled t_{on} and t_{off}.

The following differential equation describes the rectifier voltage, $v_D(t)$, for the time period with the diode off, $t_{off} \leq t < t_{on} + T_S$:

$$L_R C_R \frac{d^2 v_D(t)}{dt^2} + v_D(t) = V_{IN} + V_{AC} \sin(\omega_s t + \phi) \quad (11)$$

The general solution to this differential equation is:

$$
\begin{aligned}
v_D(t) = &\frac{V_{AC}}{1 - (\omega_s/\omega_r)^2} \sin(\omega_s t + \phi) \\
&+ C_1 e^{(-j\omega_r t)} + C_2 e^{(j\omega_r t)} + V_{IN}
\end{aligned} \quad (12)
$$

where C_1 and C_2 are constants. With the rectifier, there are two known initial conditions that occur when the diode turns off.

$$V_D(t_{off}) = V_{OUT} \quad (13)$$

$$I_R(t_{off}) = 0 \quad (14)$$

Upon applying these initial conditions the rectifier voltage becomes:

$$
\begin{aligned}
v_D(t) = &(r V_{AC} \sin(\omega_s t_{off} + \phi) + V_{OUT} - V_{IN}) \cos(\omega_r (t - t_{off})) \\
&+ r(\omega_s/\omega_r) V_{AC} \cos(\omega_s t_{off} + \phi) \sin(\omega_r (t - t_{off})) \\
&- r V_{AC} \sin(\omega_s t + \phi) + V_{IN}
\end{aligned} \quad (15)
$$

where

$$\omega_r = \frac{1}{\sqrt{L_R C_R}}, \quad Z_R = \sqrt{\frac{L_R}{C_R}}, \quad \text{and} \quad r = \frac{1}{(\omega_s/\omega_r)^2 - 1}$$

From equation 15 it is found that the rectifier has four unknown quantities: the resonant frequency and characteristic impedance of L_R and C_R (ω_r and Z_R), and the times that the diode turns on and off (t_{on}, and t_{off}). As with the inverter, design constraints are applied to the voltages and currents in the circuit to solve for the unknown values.

1) Since average power is only delivered to the load by DC current, the DC current in L_R is constrained by conservation of energy.

$$\langle i_R(t) \rangle = \frac{P_{OUT}}{V_{OUT}} \quad (16)$$

where

$$i_R(t) = \frac{1}{L_R} \int_{t_{off}}^{t} (V_{AC} - v_D(t)) \, dt \quad (17)$$
$$\text{for } t_{off} < t < t_{off} + T_S$$

2) The rectifier must operate in Periodic Steady State
   - The average inductor voltage must be 0.

$$\langle v_D(t) \rangle = V_{IN} \quad (18)$$

   - The average capacitor current must be 0.

$$\langle i_{CR}(t) \rangle = 0 \quad (19)$$

where

$$i_{CR}(t) = C_R \frac{d}{dt} v_D(t) \qquad (20)$$

3) The phase of the fundamental component of $i_R(t)$ is constrained by the inverter

Application of these constraints results in four non-linear equations. Unlike the inverter, the rectifier has no free variables, and the resulting equations are solved using numerically in MATLAB for each inverter solution. Figure 6 shows the solved values of L_R and C_R that correspond with the inverter solution of Figure 4.
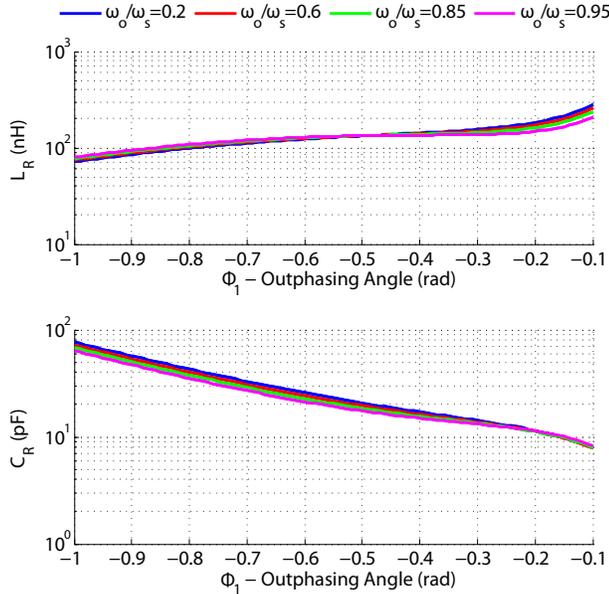
Fig. 6. Solved values of L_R and C_R that correspond with the inverter solution of Figure 4 for a converter with an input and output voltage of 12 and 30 Volts, an output power of 7 Watts, and a switching frequency of 75 MHz.

C. Converter Solution

A major advantage to having a mathematical description of the converter is visibility of the entire design space. In addition to the component values plotted in the previous sections, the converter solution also includes all of the converter's currents and voltages.

Figure 7 shows the current carried by the converter's inductors. From this plot we make a few observations: first, tuning the inverter more in-phase with the rectifier allows the power to be delivered with a smaller currents, thus implying a more efficient transfer, and second, increasing the resonant frequency of the inverter increases the AC component of current in L_F and reduces the rectifier current which indicates there will be an optimal value where losses are minimized.

Figures 8 and 9 show the device and capacitor currents. Currents carried by devices in their on-state are labeled conduction currents, and currents carried by capacitors are labeled displacement currents. Displacement currents are at least partially carried by device parasitic capacitance which
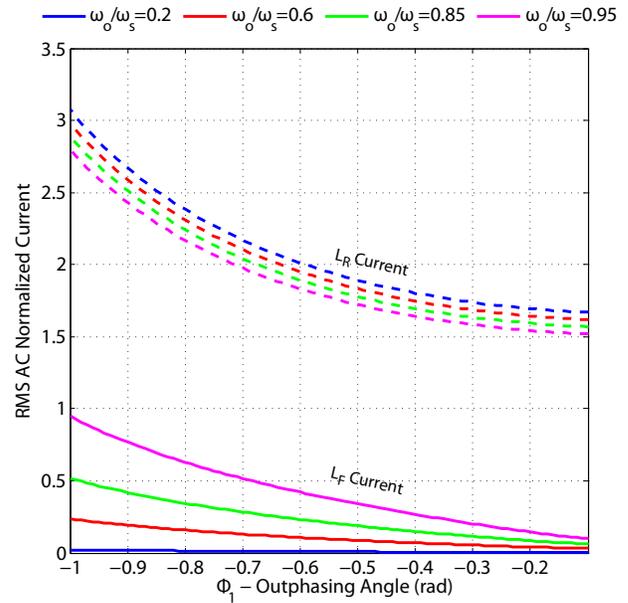
Fig. 7. RMS of the AC component of the current carried by the converter's inductors. L_F current is normalized to the converter's input DC current and L_R current is normalized to the converter's output DC current.

has a significant series resistance component, and as a result, represent a non-negligible loss component in converter's efficiency budget. From these figures we see that it is desirable to operate the inverter as in-phase with the rectifier as possible to reduce circulating currents.

Furthermore, in addition to zero-voltage switching, a desirable characteristic of the so-called "Class-E" switching waveform is for the switch's drain-to-source voltage have zero derivative at the switching turn-on instant. This is occurs when the capacitor C_E has zero current at the switching instant. Using the direct converter solution outlined here, this condition is easily plotted across the entire design space as shown in Figure 10. From this plot we observe that increasing the resonant frequency of the inverter, ω_o, has the effect of allowing this condition to be met with the inverter tuned more in-phase with the rectifier. This is an important aspect of the converter design space which implies that there is a value of ω_o that optimizes efficiency. Therefore using a resonant inductor rather than a simple choke inductor (as in a conventional Class-E circuit) results in a more efficient converter design. Figure 10 also shows us that tuning the inverter further in-phase than the point where the "Class-E" switching waveforms are obtained results in substantial increases in peak voltage stress. This, combined with the fact that the derivative of the drain-to-source voltage is positive at the switching instant demands that the drain-to-source voltage be negative for a portion of the switching period. Practical switching devices are unable to block negative voltages and these tuning points are not used.

Additionally, the sinusoidal assumption that was utilized to separate the inverter and rectifier into tractable problems does so at the cost of solution accuracy. To demonstrate this
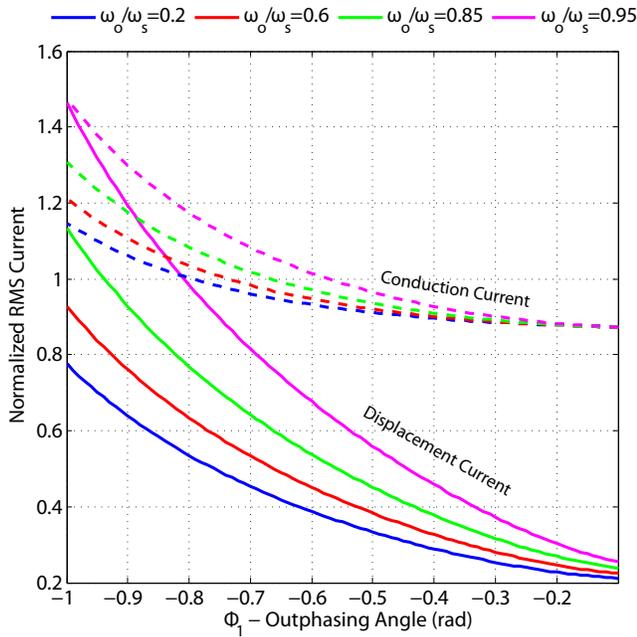
Fig. 8. Inverter switch and capacitor RMS currents normalized to the converter's input DC current. Conduction current is carried by the device's channel (an through its on-state resistance), and displacement current is carried by the parallel combination of the switch's drain-to-source capacitance and any additional capacitance in parallel with it.
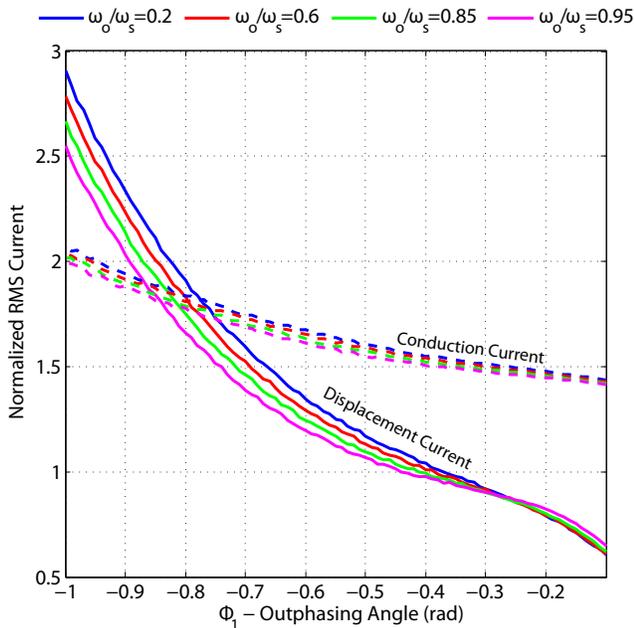
Fig. 9. Rectifier diode and capacitor RMS currents normalized to the converter's output DC current. Conduction current is carried by the diode's forward voltage, and displacement current is carried by the parallel combination of the diode's junction capacitance and any additional capacitance in parallel with it.
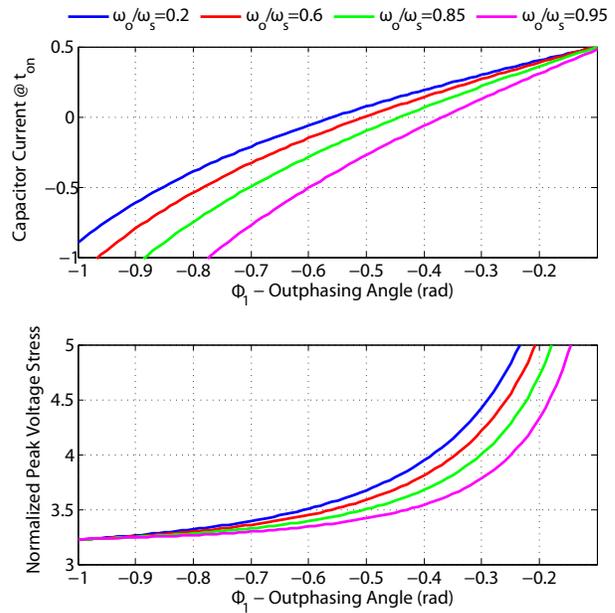
Fig. 10. The upper figure shows the current through C_E at the switching turn on instant normalized to the input DC current. The lower figure shows the peak device voltage normalized to the converter's input voltage.

effect, a converter design is selected from Figures 4 and 6 and simulated in SPICE. The SPICE output is plotted with the solved waveforms in Figure 11. While the two waveform sets do not match exactly, the error is small enough such that it can be easily corrected through a narrow parameter sweep while simulating in SPICE.
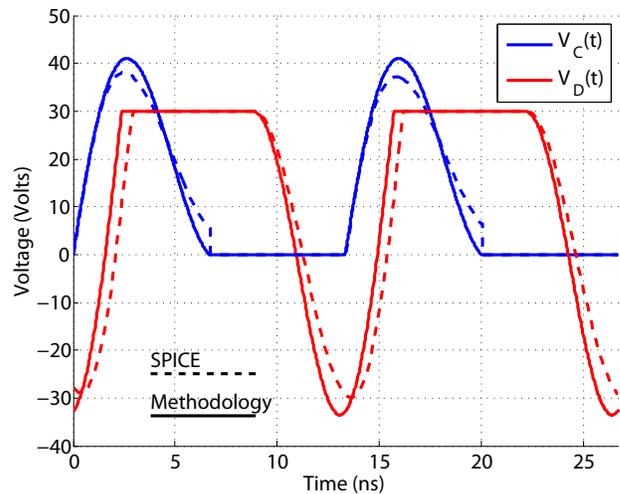
Fig. 11. Comparison of converter waveforms as calculated from the design methodology (solid) and as simulated in SPICE (dashed).

D. Device Layout Optimization

Additionally, with all of the converter's voltage and current waveforms described mathematically, the losses in the circuit

can be estimated. A loss model for each component in the circuit must be compiled. With these models the converter losses can then be calculated for the entire design space and then the best design chosen. If the semiconductor devices are integrated, then their layout can be optimized for a particular converter design. Thus, it is not necessary to use a single switch design to calculate loss. Rather, for each design point, the optimal switch layout can be calculated, and then the converter losses evaluated.

For example, a simplified model of a MOSFET that includes the parasitic components that are important to RF operation is shown in Figure 12 [16].
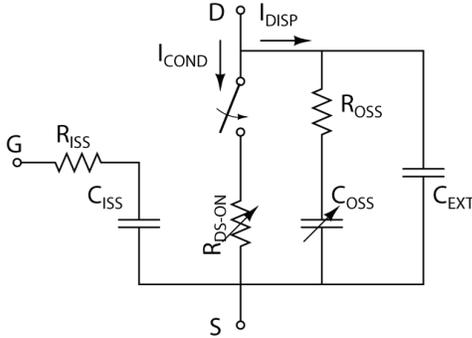
Fig. 12. Simplified MOSFET model showing device parasitics that are important to converter operation at radio frequencies.

To optimize the device, its parasitic components are parameterized by its geometry, and then space bounded by the process design rules and the available chip area is searched to find the device layout that results in the least amount of loss. (Reference [16] explores this approach in detail, but without the analytical models of converter behavior available here.) When varying the device size, three primary device losses trade with each other: gating loss, conduction loss, and displacement loss. For sinusoidal resonant gating, the total device loss is given by:

$$
\begin{aligned}
P_{TOT} = & 2R_{ISS}(\pi V_{G,AC} f_{SW} C_{ISS})^2 \\
& + \left(\frac{I_{DISP,RMS}}{C_{TOT}}\right)^2 C_{OSS}^2 R_{OSS} + I_{COND,RMS}^2 R_{DS}
\end{aligned}
\tag{21}
$$

Thus, by increasing the size of the device, the conduction loss is reduced, but the gating loss and displacement loss are increased. When designing a converter using the typical iterative modeling approach in which converter designs are found using time-domain simulations sweeping parameters, the designer would use values of $I_{DISP,RMS}$ and $I_{COND,RMS}$ that were found from simulation for the device optimization (as developed in [16]). With the design methodology proposed here, $I_{DISP,RMS}$ and $I_{COND,RMS}$ are described mathematically. This enables the design optimization to be run for each design point with little added effort. Figure 13 shows the result of such an optimization: transistor device losses (normalized as a fraction of the output power) and optimal device size are plotted across the entire design space.
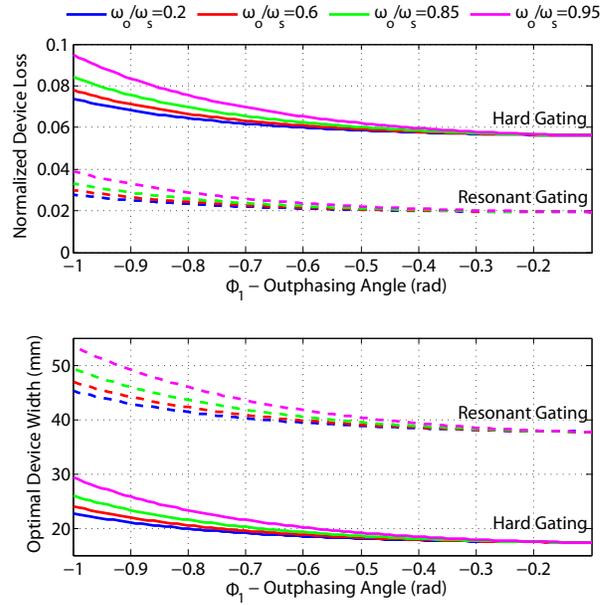
Fig. 13. Device optimization result across the entire converter design space. The upper figure shows the total transistor device loss normalized to output power for hard gating (solid) and sinusoidal resonant gating (dashed). The lower figure shows the optimal device width. Results are for a representative integrated BCD transistor process suited to the design space in question.

IV. EXPERIMENTAL RESULTS

A prototype power stage was constructed to evaluate this converter topology and design approach. The design was targeted at the general requirements of an LED driver for automotive applications, but as a first-generation test system was not held to all applicable specifications. LCD Backlights and other LED applications often have similar drive requirements. Aiming to validate the design methodology, the prototype was constructed with the same specifications used in the converter solution presented in the previous section, summarized in Table I. The switching frequency of 75MHz was chosen to demonstrate the highest switching frequency that the converter architecture can achieve while meeting a target efficiency near 85%, given the semiconductor process that was used; this general frequency range has been found to be effective in other designs as well (e.g., [2], [6], and [19]).

Vin	Vout	Pout	Fs
12V	30V	7W	75MHz

TABLE I
TARGET CONVERTER SPECIFICATIONS FOR THE EXPERIMENTAL IMPLEMENTATION.

A custom LDMOS device was optimized and fabricated for the prototype. It has an equivalent drain-to-source capacitance of approximately 34 pF and an on-state resistance of approximately 330 mOhms. Additionally, it was chosen to used the Fairchild S310 silicon Schottky diode for the rectifier device. This device is relatively oversized for the current rating of

the converter, owing to limits on available device sizes among discrete Schottky diodes that have been found to operate well under resonant operation at very high frequencies. (It has been observed in our laboratory that a degree of over-sizing is often needed to preserve low diode conduction losses under VHF operation [17], but this represents a much greater degree of over-sizing than we would ideally select.)

It is important to note that device parasitics can greatly constrain the available design space. In this case, the S310 has an equivalent reverse biased junction capacitance of approximately 55 pF. This capacitance is effectively in parallel with C_R at AC, since the output capacitor acts as an AC short. Note that with all capacitance provided by the parasitic capacitance of the diode, any diode package parasitic inductance can effectively be absorbed into L_R. From Figure 6 we see that this limits our choice of ϕ_1, the converter's out-phasing angle, to be less than around -1 radian. Had a diode of the same characteristic as the S310 with a smaller device area been available, then the converter could have been designed with the inverter and rectifier more in phase. This would allow the converter to deliver the same power with smaller currents and achieve an overall reduction in loss. This suggests that over-sizing of devices, whether due to availability or conservatism, has a major penalty on performance, and that there is an advantage to using integrated devices whose size can be optimized for a given design.

Due to the limits imposed by the S310, we chose to design the converter with $\phi_1 = -1$ radian to tune the inverter as in phase to the rectifier as possible to minimize the converter's losses. At this tuning point, the rectifier capacitor C_R is composed entirely of the diode parasitic junction capacitance. This allows parasitic inductance in the rectifier package to be absorbed into L_R, leading to more ideal performance. We additionally chose to design the converter with $\omega_o = 0.85\omega_s$. An optimal value of ω_o was introduced in the design methodology of the previous section, however, since the S310 is heavily constraining the usable values of ϕ_1, the optimal is unreachable for this design. Instead, ω_o was chosen to be high enough to provide good transient response under on/off modulation and not so high to incur excessive loss. With these design choices, the component values are read from Figures 4 and 6. Small adjustments are made to accommodate standard component values and to correct the small error in the solution due to the sinusoidal current approximation, resulting in the values shown in the schematic of the converter presented in Figure 14. The capacitor C_E is made up of the parallel combination of the transistor output capacitance (34pF) and a discrete 51.7pF capacitor.

A photograph of the converter is shown in Figure 15. The component sizes, packages, and layout were chosen for construction convenience to validate the design approach and do not necessarily represent the best method of achieving a minimum-sized design. In particular, the size of the output filter capacitor was sized much larger than strictly necessary for experimental expedience. Generally in this type of VHF design, the minimum sizing of the output filter capacitor is

based on the ripple at the on/off modulation frequency. The size of this filter capacitor can still be significantly smaller than for conventional converters having switching frequencies on the order of the modulation frequency, because the capacitor in the VHF converter needn't be sized for absorbing inductor energy or supporting the output during transients [2]. Likewise, for simplicity we have employed coreless inductors. With recently-available high-frequency magnetic materials and designs, however, significant miniaturization of the inductors is likely possible [20], [21], and [22]. Nonetheless, as recent work in a similar design space has shown, even with coreless magnetics, resonant VHF designs can achieve considerable reductions in overall passive component size and mass as compared to conventional PWM converters [2].

For experimental simplicity, the prototype converter employed a hard-switched gate drive based on the Fairchild NC7WZ04 discrete inverter, as indicated in Figure 16. We did not focus on the details of optimizing the gate drive, as successful low-loss resonant VHF gate drivers have been demonstrated in many of the cited references, including [4], [6], [7], [10], [11], [12], [17], and [23].

Figure 17 shows measured converter waveforms and a comparison to simulated SPICE waveforms. The close agreement of the waveforms validates the operation of the prototype. Output power and open loop efficiency over the input voltage range are presented in Figure 18. Based on these results, one can observe that the proposed topology and design approach lend themselves to good performance at very high frequencies.
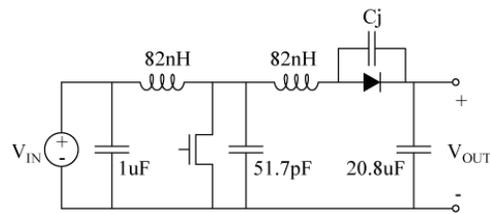
Fig. 14. Power Stage schematic of the experimental implementation. The inductors are from the midi-spring family from Coilcraft, and the Diode is a S310. The MOSFET is a LDMOS device fabricated from an integrated power process. The converter operates at 75MHz with a 50% duty cycle.
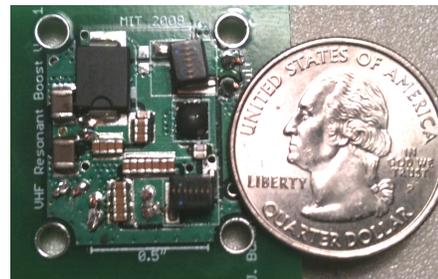
Fig. 15. Photograph of the converter prototype PCB.

Fig. 16.   Schematic of the gate drive circuit used in the experimental implementation. Output power is controlled by modulating the gate driver at frequency lower than the converter's switching frequency. These control and drive elements are placed on the back of the board, and cannot be seen in the photograph of Figure 15. The oscillator and modulation signal were provided externally for exprimental simplicity. For testing operating points having specified average power levels, the modulation duty ratio was controlled manually; closed-loop control of such systems is straightforward and has been extensively demonstrated in the past (e.g., [5], [6], [15], and [24])

Fig. 17.   Measured converter waveforms compared to simulated waveforms in SPICE.

Fig. 18.   Converter output power and measured efficiency (not including gate drive loss). Output power is controlled by on-off modulating the converter with a PWM signal at 1 MHz

V. CONCLUSION

This document presents a resonant boost converter topology that is suitable for operation at very high frequencies. The topology uses a small number of passive components and absorbs device and packaging paracitics. Moreover, only small-valued resonant inductors are used, enabling fast response under on-off control.

The paper further introduces a procedure to design the proposed resonant boost converter. Unlike previous design methods for similar converter types, the method here does not require extensive time-domain simulation sweeps across circuit parameters. Rather, the procedure is based on numerical solutions to closed-form circuit equations. This enables the designer to rapidly find the optimal converter design given a particular semiconductor switch, or the optimal combination of converter design and switch layout if an integrated power process is used.

To validate the converter topology and design procedure, an experimental implementation has been constructed. Measured waveforms from the prototype are in close agreement to simulated waveforms, and the converter achieves good efficiency over a wide input voltage range. It may be concluded that the proposed converter topology and design method yields effective converter designs at VHF frequencies.

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