Lossless Multi-Way Power Combining and Outphasing for High-Frequency Resonant Inverters

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***Abstract*—A lossless multi-way power combining and outphasing system has recently been proposed for high-frequency inverters and power amplifiers that offers major performance advantages over traditional approaches. This paper presents outphasing control strategies for the proposed power combining system that enable output power control through effective load modulation of the inverters. It describes a straightforward power combiner design methodology and enumerates various possible topological combiner implementations. Moreover, this work presents the first-ever experimental demonstration of the proposed outphasing system. The design of a 27.12 MHz, four-way power combining and outphasing system is described and used to experimentally verify the power combiner's characteristics. The proposed outphasing law is shown to be effective in controlling the output power over a 10 W to 100 W (10:1) power range.**

***Index Terms*—Outphasing, phase-shift control, LINC, power combining, Chireix combiner, RF power amplifier (RF PA).**

I. Introduction

High-frequency power amplifiers (PAs), or resonant inverters, find wide applicability in numerous areas including radio-frequency (RF) communications, industrial processing, medical imaging and power conversion among other areas (e.g., [1-9]). These applications are characterized by the need for power delivery at a particular frequency or in a narrow frequency range. At very high power levels and frequencies, it is often preferable to construct multiple low power PAs and combine their output power to form a high-power PA. Such PAs or inverters must often be able to provide dynamic control of their output power over a wide power range. Furthermore, it is usually desired that the PAs maintain high efficiency across their operating range so that high average efficiency can be achieved for highly modulated output waveforms.

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Conventional linear amplifiers such as Classes A, AB, B and C allow for a dynamic output power control over a very wide power range while providing high-fidelity power amplification. However, their peak efficiency is limited and degrades rapidly with output power back-off. On the other hand, switched-mode PAs (inverters), e.g., classes D [8-12], E [13, 14], F [15-17], E/F [17,18], Φ [19], etc., offer high peak efficiency (100% ideally), but at constant supply voltage they can only generate constant envelope signals while remaining in switched mode.

Proposed originally in the 1930's [20], *outphasing* (or phase-shift control) of power amplifiers (PAs) or inverters is a key technique (illustrated in Fig. 1) for simultaneously providing dynamic output power control while maintaining high average system efficiency [8,9,21-35]. Power from multiple small PAs (PA_1 - PA_n) is combined and delivered to a load, with power control achieved by appropriately adjusting the phases (Φ_1 - Φ_n) of the PAs. With an *isolating* combiner, the effective impedances loading the individual power amplifiers remain constant, and any power not delivered to the output is instead delivered to an "isolation port", where it is usually dissipated in an isolation resistor (though energy recovery with rectifiers has been demonstrated [25-27]). Such an isolating combiner must fundamentally divert power not delivered to the output elsewhere (usually causing loss). Alternatively, it is possible to implement lossless power combining [8, 9, 20-22, 24, 29, 30-35]. The lossless combiner and controls cause the power amplifiers to interact such that their power output is modulated. In particular, the real components of the effective loading admittances of the PAs ($Y_{in,1}$ - $Y_{in,2}$) vary with outphasing, changing the total delivered power.

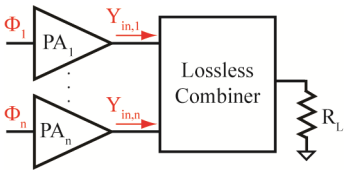


Fig. 1. Outphasing: controlling relative PA phases (Φ_1 - Φ_n) modulates the effective PA loading admittances ($Y_{in,1}$ - $Y_{in,n}$) and determines the power delivered to the load R_L.

The Chireix combiner (Fig. 2) is a traditional implementation of the lossless outphasing concept with two input power ports $P_{in,A}$ and $P_{in,B}$ and one output power port

P_{out} [8, 9, 20, 21, 29, 31]. The susceptive loading this combiner presents to the PAs varies considerably with outphasing (and power delivery). Although the Chireix *combiner* is ideally lossless, such susceptance variations often cause additional PA losses and reduce system efficiency. Fig. 3 shows an example of the effective loading of the PAs driving the Chireix combiner of Fig. 2 for various combiner loads R_L and reactance values X_C. As can be seen, for outphasing modulation of the effective PA loading conductance by a factor of ten, the corresponding loading susceptance may vary by more than 50% of the maximum conductance. Such large susceptance variations adversely impact the efficiency of the overall system owing to the sensitivity to reactive loads of inverters and power amplifiers suitable for very high frequency operation [21]. Moreover, due to the susceptive components of loading, significant circulating reactive currents are introduced in the PAs and combiner. This is a further source of loss with practical (non-ideal) components.

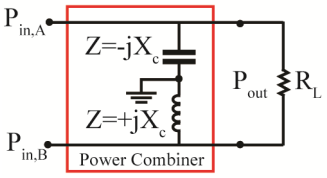


Fig. 2. The Chireix combiner with reactance values shown for the fundamental output frequency.

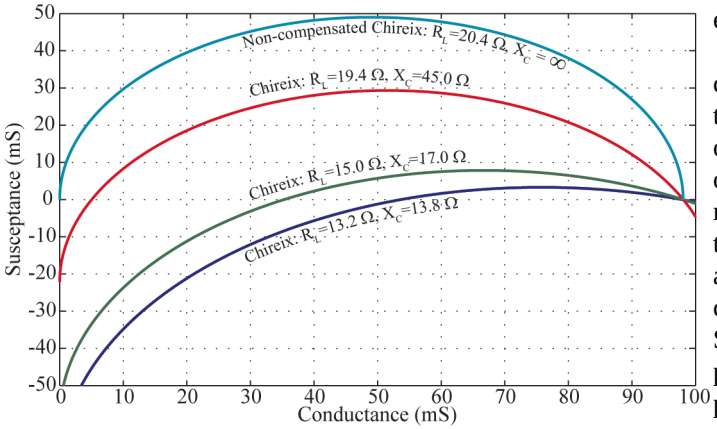


Fig. 3. Susceptive versus conductive components of the loading admittance seen by the PAs driving the Chireix combiner of Fig. 2 over the outphasing range for various designs (including reactances X_C and resistive loads R_L). Only the input admittance at input port A ($P_{in,A}$) is shown; the input admittances of port A and B are complex conjugates.

A new power combining and outphasing system has recently been proposed to overcome the loss and reactive loading problems of traditional outphasing approaches such as Chireix combining [30]. It provides ideally lossless power combining from four or more PAs along with nearly resistive loading of the individual PAs over a very wide output power range. Fig. 4 depicts one possible implementation of such a combiner for four PAs (four-way combiner). This is also the combiner topology which we have chosen to realize and whose performance we experimentally evaluate (see Section IV and V). As with the Chireix combiner, the output power it delivers is determined by the amount of phase shift (outphasing) between the PAs. [30] developed the underlying circuit structures and theoretical underpinning for this new technique along with a basic control law to achieve the desired characteristics, and it demonstrated the validity of the approach through detailed simulations.

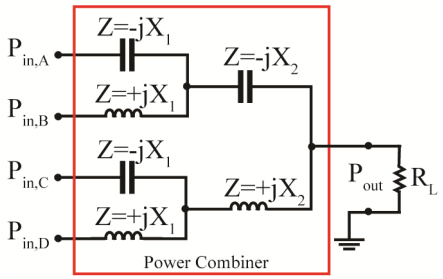


Fig. 4. A four-way implementation of the proposed multi-way combiner [30, 34, 35]. Reactance values are shown for the fundamental output frequency.

The present paper expands upon recent conference publications by the authors [34, 35] to further develop and experimentally validate this new technique. We introduce a design procedure for optimally selecting the combiner reactances X_1 and X_2 based on the desired output power range, develop improved outphasing control strategies that enable output power control while minimizing susceptive variations or phase variations in PA loading, establish alternative combiner implementations and present a complete experimental validation of the proposed technology in a high-efficiency inverter system operating at 27.12 MHz.

Section II of the paper provides a brief overview of the key combiner input and output port characteristics, describes how the combiner's output power can be controlled through outphasing of the PAs and introduces various optimized outphasing control strategies. Section III presents a methodology for designing the combiner network according to desired performance specifications. The detailed design and implementation of a 27.12 MHz, 100 W four-way power combining system prototype is discussed in Section IV, while Section V examines its experimental performance. Section VI presents other possible topological implementations of the proposed combiner network, while Section VII concludes the paper. The Appendix addresses the effect of combiner load variation on its power combining characteristics.

II. Combiner Outphasing Control

Consider the four-way combiner of Fig. 5 driving a resistive load R_L. To simplify analysis, the PAs or resonant inverters driving the combiner are treated as ideal sinusoidal voltage sources V_A - V_D with constant amplitude V_S. Expressing the drive voltages as phasors and assuming a zero-phase-referenced output, the drive can be expressed as:

Non-zero phase output can be synthesized as a common phase adjustment to all angles. A phasor diagram of the drive voltages in (1) is shown in Fig. 6. Here we describe a means to control output power and voltage through outphasing (or phase shift) control of the inverters driving the combiner, and

we summarize control laws that provide desirable loading characteristics for the PAs.

$$\vec{V} = \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = V_S \begin{bmatrix} e^{-j\phi}e^{-j\theta} \\ e^{+j\phi}e^{-j\theta} \\ e^{-j\phi}e^{+j\theta} \\ e^{+j\phi}e^{+j\theta} \end{bmatrix}. \quad (1)$$

Simple ac analysis reveals that the relationship between the input terminal voltages V_A-V_D and currents I_A-I_D in Fig. 5 is given by (2),

$$\begin{bmatrix} I_A \\ I_B \\ I_C \\ I_D \end{bmatrix} = Y \cdot \vec{V} = X_1^{-1} \begin{bmatrix} \gamma + j(1-\beta) & -\gamma + j\beta & \gamma & -\gamma \\ -\gamma + j\beta & \gamma - j(\beta+1) & -\gamma & \gamma \\ \gamma & -\gamma & \gamma + j(\beta+1) & -\gamma - j\beta \\ -\gamma & \gamma & -\gamma - j\beta & \gamma + j(\beta-1) \end{bmatrix} \cdot \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} \quad (2)$$

where $\gamma = R_L/X_1$ and $\beta = X_2/X_1$.

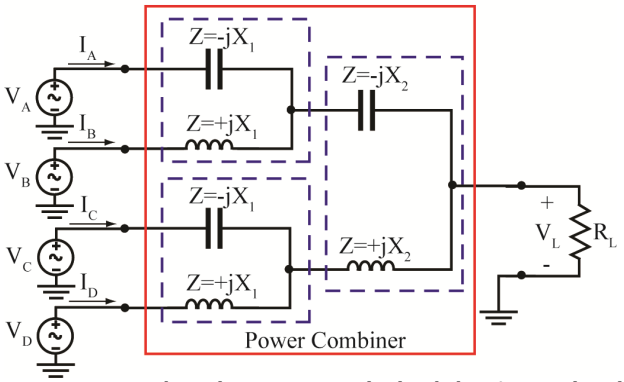


Fig. 5. Four-way combiner driving a resistive load with the PAs treated as ideal voltage sources [30].

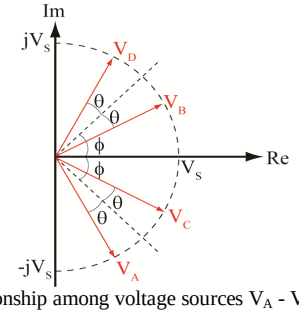


Fig. 6. Phasor relationship among voltage sources V_A - V_D driving the four-way combiner of Fig. 5 [30].

By utilizing (2) and (1), it can be demonstrated that the effective admittances seen by the PAs driving the combiner (the complex ratio of current to voltage at a combiner input port with all driving sources active) are a strong function of the outphasing angles θ and ϕ and are given by (3)-(6).

$$Y_{eff,A} = X_1^{-1}(\gamma - \gamma\cos(2\phi + 2\theta) - \gamma\cos(2\phi) + \gamma\cos(2\theta) - \beta\sin(2\phi)) + jX_1^{-1}(1 - \beta - \gamma\sin(2\phi + 2\theta) - \gamma\sin(2\phi) + \gamma\sin(2\theta) + \beta\cos(2\phi)) \quad (3)$$

$$Y_{eff,B} = X_1^{-1}(\gamma - \gamma\cos(2\theta - 2\phi) - \gamma\cos(2\phi) + \gamma\cos(2\theta) + \beta\sin(2\phi)) + jX_1^{-1}(-1 - \beta - \gamma\sin(2\theta - 2\phi) + \gamma\sin(2\phi) + \gamma\sin(2\theta) + \beta\cos(2\phi)) \quad (4)$$

$$Y_{eff,C} = X_1^{-1}(\gamma - \gamma\cos(2\theta - 2\phi) - \gamma\cos(2\phi) + \gamma\cos(2\theta) + \beta\sin(2\phi)) - jX_1^{-1}(-1 - \beta - \gamma\sin(2\theta - 2\phi) + \gamma\sin(2\phi) + \gamma\sin(2\theta) + \beta\cos(2\phi)) \quad (5)$$

$$Y_{eff,D} = X_1^{-1}(\gamma - \gamma\cos(2\phi + 2\theta) - \gamma\cos(2\phi) + \gamma\cos(2\theta) - \beta\sin(2\phi)) - jX_1^{-1}(1 - \beta - \gamma\sin(2\phi + 2\theta) - \gamma\sin(2\phi) + \gamma\sin(2\theta) + \beta\cos(2\phi)) \quad (6)$$

It is useful to know the load voltage V_L and the output power P_{out} that the combiner delivers to the load R_L (see Fig. 5) for a given pair of outphasing control angles [θ; ϕ]. By employing straightforward linear circuit analysis techniques, it can be shown that the load voltage V_L and the output power P_{out} are given respectively by (7) and (8).

$$V_L = j\frac{R_L}{X_1}(V_B + V_D - V_A - V_C) \quad (7)$$

$$P_{out} = \frac{8R_L V_S^2}{X_1^2} sin^2(\phi)cos^2(\theta) \quad (8)$$

Equation (8) is of great importance as it concisely expresses the exact relationship between the output power delivered to the load R_L and any pair of outphasing control angles [θ; ϕ]. This equation holds on the assumption that the combiner inputs are each driven with the specified voltage. As can be seen from (8), output power may be controlled either through phase modulation (adjusting the angles θ and ϕ), through amplitude modulation (adjusting the PA output signal amplitude V_S) or through both. Although in the present experimental work we consider output power control through phase modulation, in practice, one may choose to employ simultaneously both phase and amplitude modulation to achieve an even wider operating output power range [43]. It is readily observed from (8) that the maximum output power deliverable to the load by the power combiner, termed here the saturated output power $P_{out,sat}$, is given by (9) and corresponds to θ = 0° and ϕ = 90°.

$$P_{out,sat} = \frac{8R_L V_S^2}{X_1^2} \quad (9)$$

As can be inferred from (8), for a particular PA drive amplitude V_S, there are infinitely many possible control angle pairs [θ; ϕ] that will result in the same output power level. Thus, an additional constraint can be specified on θ and ϕ to allow for the selection of a particular control angle pair. Depending on the nature of the constraint, many possible outphasing control methodologies emerge. Reference [30] introduced a control methodology based on selecting the control angles as an approximation of the inverse of a resistance compression network. Here we introduce two alternative control methods, optimal-phase (OP) and optimal-susceptance (OS) control that are of particular relevance to various practical applications.

A. Optimal-Phase (OP) Control

Optimal-phase control entails the selection of θ and ϕ such that the phases of the effective combiner input admittances are minimized over a specified power range (i.e., the

constituent inverters/PAs each see an effective admittance having as near-zero phase as possible). In particular, we minimize the maximum phase seen by any of the PAs over the specified operating range. For the four-way combiner addressed here (see Fig. 5), the optimal-phase control angle pair [θ; ϕ] can be computed for a particular output power level P_{out} by numerically minimizing the largest effective input admittance phase φ_{max} seen by the PAs (at P_{out}) (10) subject to the constraint (11):

$$\varphi_{max} = max\left\{ tan^{-1}\left\{\left|\frac{Im\{Y_{eff,A}\}}{Re\{Y_{eff,A}\}}\right|\right\}, tan^{-1}\left\{\left|\frac{Im\{Y_{eff,B}\}}{Re\{Y_{eff,B}\}}\right|\right\}\right\} \quad (10)$$

$$P_{out} = \frac{8R_L V_S^2}{X_1^2} sin^2(\phi) cos^2(\theta). \quad (11)$$

It can be shown that for the range of output power levels given by (12), which includes the main operating range of practical interest, the solutions of the preceding optimization problem (10), (11) reduce to a non-linear system of equations (13) which can be solved for [θ; ϕ] by employing conventional numerical methods.

$$\frac{P_{out,sat}}{2}\left(1-\sqrt{1-\frac{X_1^2}{4R_L^2}}\right) \le P_{out} \le \frac{P_{out,sat}}{2}\left(1+\sqrt{1-\frac{X_1^2}{4R_L^2}}\right) \quad (12)$$

$$\frac{P_{out} X_1^2}{8R_L V_S^2} = \sin^2(\phi)\cos^2(\theta)$$
$$\sin(2\phi) = \frac{2\gamma\cos^2(\theta)}{\beta^2 + 4\gamma^2\cos^2(\theta) - 2\beta\gamma\sin(2\theta)} \quad (13)$$

B. Optimal-Susceptance (OS) Control

Another control methodology, optimal-susceptance (OS) outphasing control, is also proposed here, and is characterized with the following two main advantages: (1) it minimizes the effective susceptance seen by the PAs at each output power level over a specified power range, and (2) it achieves even susceptive loading of the PAs (all PAs see equivalent susceptive amplitudes) over the desired operating output power range. Such an outphasing control methodology is advantageous in systems driven by nonlinear, switched-mode inverters/PAs where susceptive variations in their loading is detrimental to the overall system efficiency (e.g., class E power amplifiers).

For the four-way combiner discussed here (Fig. 5), the optimal susceptance control angle pair [θ; ϕ] can be computed for a particular output power level P_{out} by numerically minimizing the largest effective input susceptance S_{max} seen by any of the PAs (at P_{out}) (14) subject to the constraint (15):

$$S_{max} = max\left\{\left|Im\{Y_{eff,A}\}\right|, \left|Im\{Y_{eff,B}\}\right|\right\} \quad (14)$$

$$P_{out} = \frac{8R_L V_S^2}{X_1^2} sin^2(\phi) cos^2(\theta) \quad (15)$$

Similar to the case of the OP control presented above, it can be demonstrated that for output power levels in the range given by (12), the solutions of the optimization problem of (14) and (15) reduce to a set of convenient analytical expressions for calculating the OS control angles (16):

$$\theta = cos^{-1}\left(\sqrt{\frac{4V_S^4 + P_{out}^2 X_1^2}{8P_{out} R_L V_S^2}}\right)$$
$$\phi = tan^{-1}\left(\frac{P_{out} X_1}{2V_S^2}\right) \quad (16)$$

Fig. 7 depicts the resultant OP and OS control angles for an example four-way combiner design with R_L = 50 Ω, X_1 = 36.69 Ω, and X_2 = 48.97 Ω. (This example combiner is specifically designed to operate well over a 10 dB output power range; a detailed combiner design procedure is presented in the following section.) We consider this combiner design example here since it is identical to the one we have chosen to realize and experimentally evaluate. As can be seen, both control strategies result in nearly identical control angles over most of the operating power range, suggesting that for all practical purposes OP and OS control are identical. This conveniently implies that outphasing the PAs in such a way as to minimize their susceptive loading (for a particular P_{out} level) results also in approximately minimizing the phase of their loading admittance, and vice-versa.

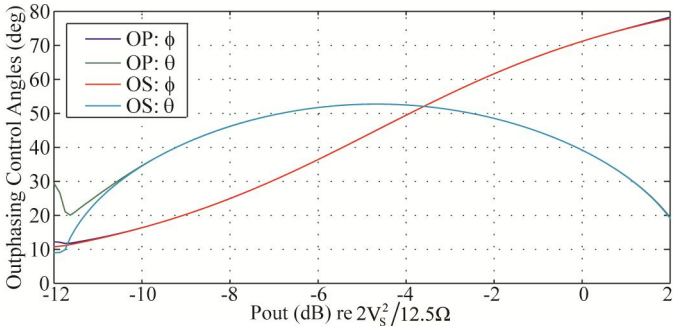


Fig. 7. Outphasing control angles θ and ϕ for the Optimal Phase (OP) and Optimal Susceptance (OS) control methods for an example four-way combiner design with R_L = 50Ω, X_1 = 36.69Ω, and X_2 = 48.97Ω.

The resultant effective input conductance, susceptance, and admittance phase seen by each of the four PAs over the operating power range for the above power combiner example design are illustrated in Fig. 8. As can be seen, the proposed OP/OS control effectively modulates the combiner input conductance in accordance with the output power, while limiting variations in the admittance phase to less than 2º over an output power range of approximately 10 dB (10:1 power range). It is important to note that for most of the output power range, the PAs see roughly the same conductance/susceptance and hence are loaded equally. As one can notice from the combiner's admittance characteristics (Fig. 8), the PAs see purely resistive loading at exactly four distinct output power levels (termed the *zero-points*) at which

the effective input admittance phase and susceptance at all combiner input ports are zero. The outer two zero-points span the intended operating range of the combiner. It is this power range that the combiner is designed to operate well over, and it is over this power range that the outphasing control angle expressions (13) and (16) are valid. Although Fig. 8 depicts the combiner admittance characteristics due to the OP outphasing control methodology, it can be shown that OS control results in practically undistinguishable combiner admittance characteristics from those associated with OP control. This is true over the combiner's operating power range (the power range bounded by the outer two zero-points in the admittance characteristic).

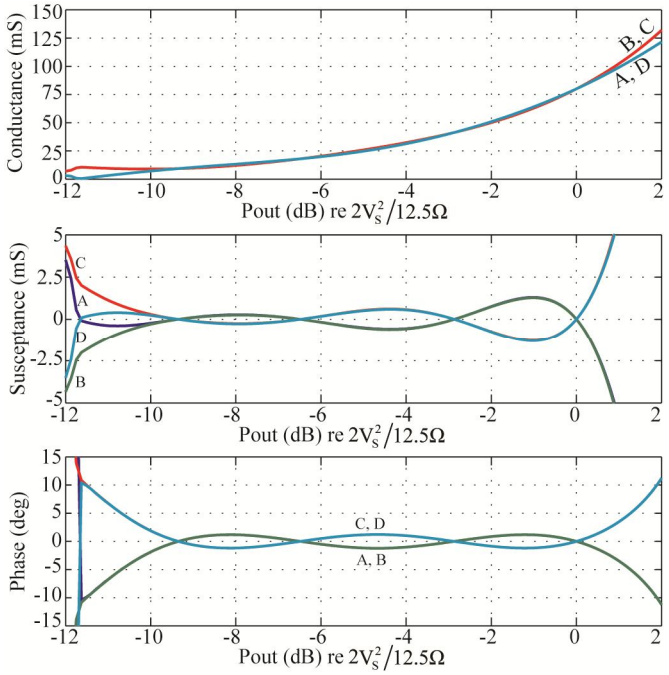


Fig. 8. Effective input conductance (top), susceptance (middle), and phase (bottom) seen by each of the PAs (A-D) driving the four-way combiner of Fig. 5 with R_L = 50 Ω, X_1 = 36.69 Ω, and X_2 = 48.97 Ω as a result of OP outphasing control.

These control techniques (OP and OS), when used with the proposed combiner, enable control of output power over a wide range while preserving desirable loading characteristics for the inverters. Over this range, the PAs/inverters can be designed to operate at relatively high efficiencies. Outphasing and power combining allows one to achieve both dynamic output power control and high system efficiency by modulating the effective loading of the PAs instead of controlling their individual output amplitudes. (This general technique is known as "load modulation", since one modulates the output power by varying the effective inverter loading.) It is important to note that the maximum permissible phase and susceptance variations at the combiner inputs depend on the particular PAs used to drive the combiner. Here we show the best that can be achieved over a desired output power range. Power control outside of the outphasing range can be achieved through various other techniques such as direct amplitude modulation (AM) of the individual PA outputs. Careful design of the combiner allows one to use outphasing to control the output power of a system over its main portion of the operating range, while reverting to other controls (e.g., conventional AM control, burst control, etc.) for operation at low power levels outside of this range. Such a hybrid power control scheme facilitates the operation of high-frequency power amplification systems over wide dynamic ranges at high average efficiencies.

III. Combiner Design

The two outphasing control laws presented above (OP and OS) are based on the assumption that the combiner reactances X_1 and X_2 (Fig. 5) are selected appropriately, i.e., the combiner is designed to operate over a particular output power range. The initial work on the underlying combiner fundamentals [30] suggested the selection of reactances X_1 and X_2 according to (17),

$$X_2 = \frac{2R_L}{k+1}$$
$$X_1 = \frac{X_2}{k+\sqrt{k^2-1}} \qquad (17)$$

where k is a design parameter that uniquely determines the performance and behavior of the power combiner. This section of the paper elaborates on [30] and proposes for the first time a methodology for selecting the value of k that provides the best performance for a specified operating power range. The parameter k directly controls the width of the output power operating range and the spread of the zero-points. Fig. 9 plots the maximum absolute value of the loading admittance phase seen among the PAs as a function of output power level for various values of k under OS control.

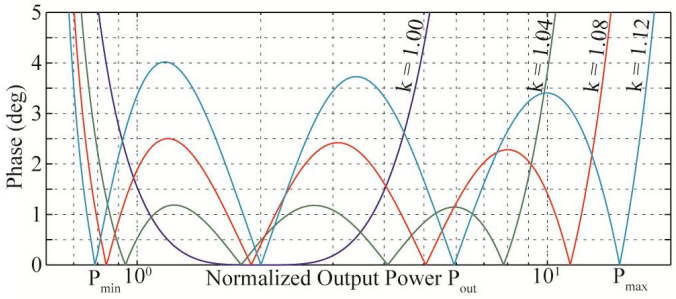


Fig. 9 Absolute value of the maximum effective input admittance phase seen at the input ports of a four-way power combiner versus the output power level for various k values. The plot is normalized to V_S = 1 V and R_L = 1 Ω; denormalize for a particular V_S and R_L by scaling the P_{out} axis by V_S^2/R_L.

The power axis is normalized to R_L = 1 Ω and V_S = 1V. To denormalize for a particular value of R_L and V_S, simply scale the axis by V_S^2/R_L. As can be seen from Fig. 9, a larger value of k results in a wider operating range at the cost of larger susceptive (and phase) variations of the combiner's input admittances. On the other hand, smaller k values reduce susceptive variations (and phase) but in turn narrow the

operating range of the combiner. A *k* value of unity (*k* = 1) corresponds to the degenerate combiner case in which $X_1 = X_2 = R_L$, and all zero-points coincide. It is important to clarify here that by talking about the operating range of the combiner, one refers to the power range between the outer two zero-points of the combiner's admittance characteristic. For example, in Fig. 9, the operating range for *k* = 1.12 will be [P_{min}, P_{max}]. It is over this power range that the peak variations of the combiner's input admittances are minimized. Of course, by selecting the appropriate outphasing control angles, one could make the combiner to operate outside of this power range (beyond the outer zero-points), although in this case, the PAs would see significant susceptive loading components which could adversely impact the overall system efficiency.

Fig. 10 provides a set of numerically-computed design curves which facilitate the selection of the optimal *k* value to minimize effective input admittance phase for a particular output power range ratio (PRR) under OP or OS control. PRR is the ratio of the maximum to the minimum output power over which peak admittance phase is to be minimized (and corresponds to the outer two power levels - *zero-points* - at which the input admittance phases become zero as in Fig. 8). The value of *k* is optimal in the sense that it results in the smallest worst-case input admittance phase over the specified operating PRR. The value of *k* can be determined by horizontally tracing from the specified PRR to the Power Ratio Curve and then vertically to the *k* axis. The corresponding worst-case admittance phase seen by the PAs can be obtained in turn by tracing the selected *k* to the Phase Curve and then horizontally to the Phase axis.

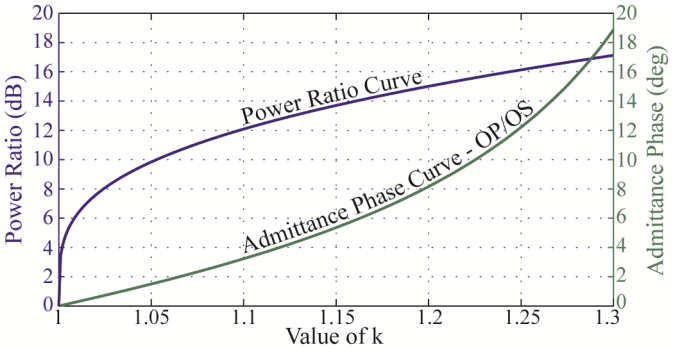


Fig. 10. Design curves minimizing effective input admittance phase for a four-way combiner under OP or OS control.

A similar plot (Fig. 11) gives the design curve for optimally selecting *k* to minimize peak effective input susceptance amplitude over a particular combiner power range ratio and also shows the peak susceptance for a particular selection of *k*. The peak susceptance axis is normalized to the combiner load; to denormalize, simply scale the values on the right vertical axis by $1/R_L$.

For the system implementation discussed in this paper, the combiner was designed to operate over an output power range ratio of approximately 10 dB (10:1 power range, PRR=10) and with a 50 Ω termination (R_L = 50 Ω). In accordance with Fig. 10, a *k* value of 1.042 was selected, which in turn yields combiner reactances X_1 = 36.69 Ω and X_2 = 48.97 Ω. As can bee seen from Fig. 8 through Fig. 11, the input admittance phases and susceptances are limited to less than 2º and 2 mS respectively over the suggested operating range.

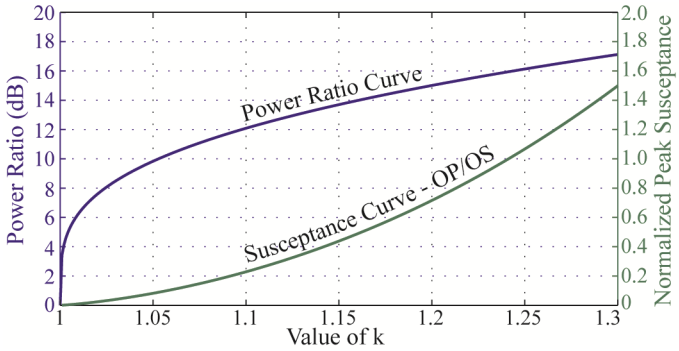


Fig. 11. Design curves for minimizing effective input susceptance for a four-way combiner under OP or OS control. To denormalize the peak susceptance, scale the axis by $1/R_L$.

Fig. 12 depicts the normalized output power levels corresponding to each of the four zero-points $P_{out,zp1}$ - $P_{out,zp4}$ in the combiner's admittance characteristic, with analytical expressions given by (18)-(21).

$$P_{out,zp1} = 2V_S^2\left(R_L + \sqrt{R_L^2 - X_2^2} - \sqrt{2R_L^2 - X_1^2 - X_2^2 + \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}}\right)^{-1} \quad (18)$$

$$P_{out,zp2} = 2V_S^2\left(R_L + \sqrt{R_L^2 - X_2^2} + \sqrt{2R_L^2 - X_1^2 - X_2^2 + \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}}\right)^{-1} \quad (19)$$

$$P_{out,zp3} = 2V_S^2\left(R_L - \sqrt{R_L^2 - X_2^2} - \sqrt{2R_L^2 - X_1^2 - X_2^2 - \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}}\right)^{-1} \quad (20)$$

$$P_{out,zp4} = 2V_S^2\left(R_L - \sqrt{R_L^2 - X_2^2} + \sqrt{2R_L^2 - X_1^2 - X_2^2 - \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}}\right)^{-1} \quad (21)$$

Note that the power axis is normalized to R_L = 1 Ω and V_S = 1V. To denormalize for a particular value of R_L and V_S, simply consider the vertical axis as dB re V_S^2/R_L. It is important to observe that selecting a larger value for the design parameter *k* results in a spreading of the zero-points and a wider operating power range at the cost of larger susceptive variations in the input admittances. Moreover, it can be shown that even wider operating power ranges can be achieved for a given allowed susceptance variation by constructing an eight-way (or higher) combiner based on similar principles [36].

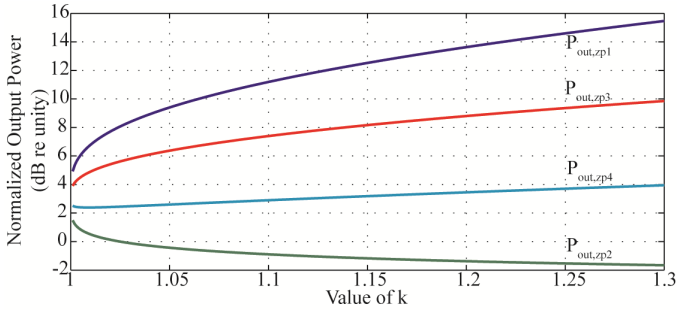


Fig. 12. The output power level corresponding to each of the zero-points $P_{out,zp1}$ - $P_{out,zp4}$ versus the *k* value for the four-way combiner. Output power is normalized to V_S = 1 V and R_L = 1 Ω; denormalize for a particular V_S and R_L by considering the vertical axis as dB re V_S^2/R_L.

IV. System Implementation

A block diagram of the entire power combining and outphasing system is shown in Fig. 13. The system operates at the ISM-band frequency of 27.12 MHz. The input power ports of the combiner are driven by four (ideally) identical class-E PAs based on the design in [37], which are designed to deliver 25 W of output power at a 12.5 Ω load (when powered from a 16 V dc supply) and operate over more than a 10:1 load modulation ratio (< 12.5 Ω to >125 Ω) [37]. For the results shown here, the PAs are operated over their full load-modulation and output power range. Each PA provides a peak output power of at least 25 W (amplitude of V_S = 25 V in Fig. 6), with a combiner peak output power of 100 W delivered to its 50 Ω load. Since the combiner is not 100% efficient in reality, the output power levels of the PAs have to be driven slightly above 25 W to achieve a total combiner output power of 100 W, and consequently, the PAs see a minimum loading impedance of slightly less than 12.5 Ω.

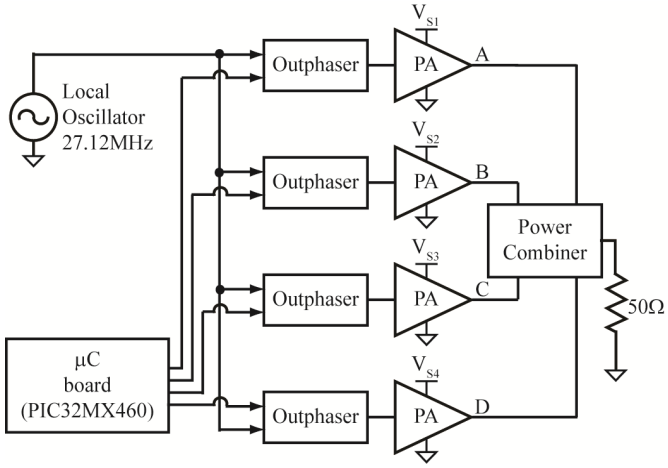


Fig. 13. Block diagram of the implemented power combining and outphasing system. Full details may be found in [36].

In order to control the output power sourced from the PAs and delivered to the load, the PAs are outphased according to the outphasing control strategy discussed above (see Fig. 7). This task is accomplished by employing specially designed outphasers that take a reference sinusoidal input from a 27.12 MHz local oscillator and output a phase-shifted version of the input, which in turn controls the PA drive signal. The amount of phase shift introduced by each outphaser is digitally controlled by a microcontroller (PIC32MX460, Microchip Technology Inc.) pre-programmed with a set of outphasing control angles (stored in a look-up table) corresponding to the desired output power levels. The design of the control system, the PAs, and the combiner are treated below.

A. Outphasing

The outphaser implementation discussed here is capable of providing any desired phase shift from -180º to 180º with an accuracy of approximately ±0.1º. The proposed design (see Fig. 14) comprises an In-phase/Quadrature (IQ) Modulator (LTC5598, Linear Technology Inc.), which outphases a local oscillator (LO) signal by an amount determined by the In-phase (I) and Quadrature (Q) components. Fig. 15 illustrates the phasor relationship between the LO signal and the output of the I/Q Modulator (the RF signal); by appropriately adjusting I and Q (within a range of -0.5 V to +0.5V), the RF signal can be phase-shifted by any arbitrary amount with respect to the LO signal. Controlled by the PIC32MX460 microcontroller, a 2-channel, 12-bit DAC (DAC5662, Texas Instruments Inc.) is utilized to synthesize the I and Q components.

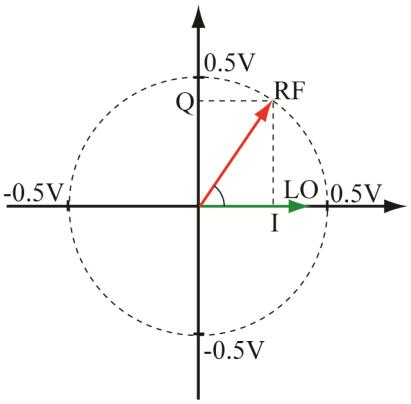


Fig. 15. Phasor representation of the I/Q modulator output signal (RF) and its local oscillator input (LO).

The I/Q modulator's RF output signal is coupled to an unbalanced-to-center-tap balun with a 1:2 impedance ratio to each secondary (T2-1T, Mini-Circuits) thus producing two complementary (180º apart) versions of the RF signal, each of which is further amplified by a 20 dB gain stage. This allows the outphaser to be used with PAs requiring complementary gate-driving signals (such as a push-pull stage). Note however that in the present work only one of the outputs is used (OUT1 in Fig. 14) while the other is terminated with 50 Ω. Due to the nonlinear mixing process used by the modulator to introduce the desired phase shift, its output contains significant harmonic content. A 27.12 MHz band-pass filter (part of the PA gate-driving circuit discussed in Section C) is used to extract the fundamental component from OUT1, which in turn is coupled directly to the PA gate drivers.

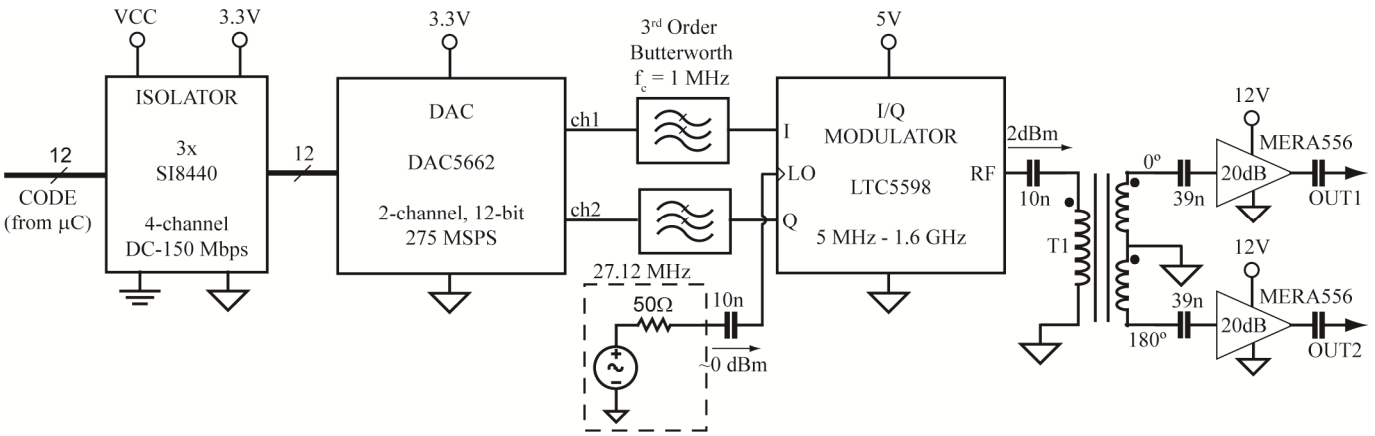


Fig. 14. Block diagram of a single outphaser: LO-Local Oscillator input.

B. The Power Amplifiers

In applications involving frequencies above 10 MHz, single-switch power amplifiers (or resonant inverters) such as the Class-E inverter are often preferred. However, the traditional Class-E inverter (e.g., [13, 14, 38]) is highly sensitive to loading variations and considerably deviates from zero-voltage switching for load resistance variations of more than about a factor of two. Since in the present application the inverter load resistance varies over a wide range (>10:1), a Class E design specifically developed for load modulation applications is employed [37]. In the design methodology of [37], the inverter components (L_s, C_s, L_p, C_p, and C_d in Fig. 16) are selected so as to maintain zero-voltage switching over a wide load-modulation range without necessarily ensuring a zero dv_{DS}/dt switch turn-on as loading resistance varies [37]. Fig. 16 depicts the topology of the 27.12 MHz Class-E amplifiers employed for driving the combiner. The input inductor L_f is resonant with the capacitance C_D at 1.5 times the switching frequency, and the series-tuned network L_S-C_S and parallel-tuned output filter network Lp-Cp are tuned at the switching frequency. (The parallel-tuned filter network Lp-Cp improves the output waveform quality at high load resistances by attenuating higher-frequency components.)

Table I lists the inverter component values along with their implementation. A gallium-nitride power transistor (EPC1007, Efficient Power Conversion Corp.) is used as a switch with an output capacitance C_{oss} of approximately 150 pF and channel on-resistance R_{on} of approximately 30 mΩ.

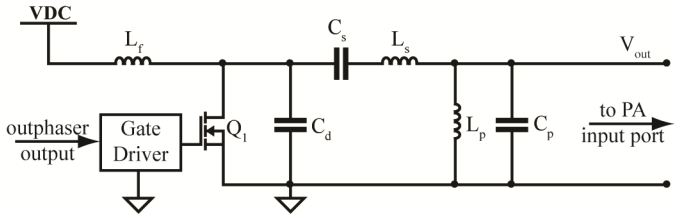


Fig. 16. Topology of the implemented Class-E power amplifier.

The gate-driver circuit is shown in Fig. 17. As already mentioned, due to its non-linear characteristics, the I/Q modulator introduces significant harmonic content in the phase-shifted signal (see Fig. 14), and so, the outphaser output signal is band-pass filtered at 27.12 MHz to isolate only the correctly phase-shifted fundamental component.

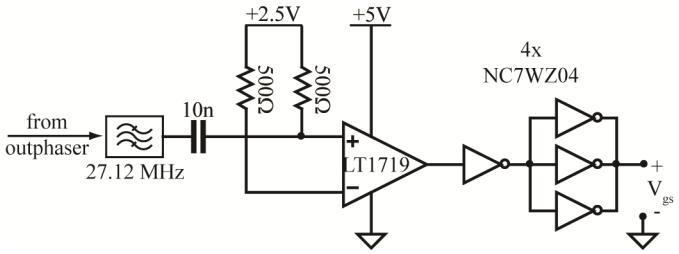


Fig. 17. Gate-driver circuit employed in the PA of Fig. 16.

The sinusoidal filter output is then "squared up" with a comparator (LT1719, Linear Technology Inc.) and fed to a 3:1 tapered inverter driver chain (NC7WZ04, Fairchild Semiconductor Inc.), which in turn drives the gate of the transistor. Note that the implemented gate-driver circuit conveniently ensures the same gate signal duty cycle regardless of the amplitude and phase of the outphaser's output signal.

TABLE I. COMPONENT VALUES FOR THE IMPLEMENTED CLASS-E PAS

Component	Value	Implementation
L_f	35.6 nH	3 parallel 132-09SMJL inductors (Coilcraft Inc.)
L_s	380 nH	132-17SMJL inductor (Coilcraft Inc.)
L_p	169 nH	132-12SMJL inductor (Coilcraft Inc.)
C_d	377 pF	ATC700A Capacitor Series (American Technical Ceramics Corp.)
C_s	90 pF	
C_p	203 pF	
Q_1	$C_{oss} \approx 150$ pF $R_{on} \approx 0.03$ Ω	EPC1007 (Efficient Power Conversion Corp.)

Fig. 18 shows a photograph of the implementation of a single Class-E PA clearly outlining the gate driver circuit. The outphaser's output (OUT1 in Fig. 14) is fed to the PA's IN port, while its OUT port connects directly to one of the four power combiner input ports.

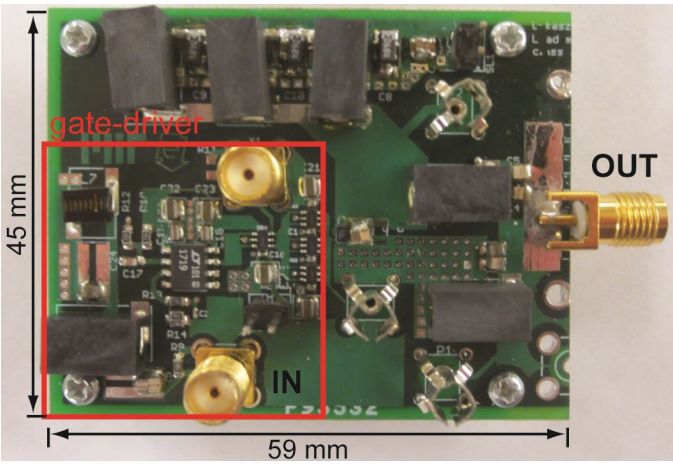


Fig. 18. Photograph of a single implemented Class-E PA.

C. The Power Combiner

Based on the earlier discussion on combiner design (Fig. 10 and Fig. 11, Section III), the required combiner reactances X_1 and X_2 for a 10 dB operating range are 36.69 Ω and 48.97 Ω, respectively. Each of the combiner reactances X_1 and X_2 (see Fig. 5) is realized with a series combination of an inductor and a capacitor. This implementation blocks any direct-current (dc) paths from the combiner's input ports to its output port and suppresses any harmonic content from the PAs. Moreover, it facilitates combiner tuning: any branch reactance can be easily adjusted by simply adding some extra capacitance in parallel with the already mounted branch capacitor. Fig. 19 depicts the actual combiner implementation. It is important to properly tune the combiner (adjust the X_1 and X_2 reactances to their intended values), as it has been shown that the combiner's performance is very sensitive to variations in the reactance values. Even a 5% deviation in the reactance values may result in noticeable degradations of the combiner's input admittance characteristic and considerable variation in the input admittance phase/susceptance. For example, a Monte-Carlo simulation of the admittance characteristics of the combiner considered in this work reveals that variation of the reactance values (X_1 and X_2 in Fig. 5) within 1% of their intended values can result in a peak input admittance phase of 10°. This is approximately five times larger phase variation than the one demonstrated by the theoretical analysis of the ideally-tuned combiner (see Section II and Fig. 8). A simple methodology employed in tuning the combiner is briefly described here.

Starting with an unpopulated combiner printed-circuit board (PCB), C5, C6, L5, and L6 are first populated (see Fig. 19). Initially, slightly lower values for C5 and C6 are used (for example, 5% less than what is required). Ports E and F are loaded with 50 Ω. A 27.12 MHz sinusoidal signal is injected into the output port (OUT) of the combiner, and the voltage waveforms at ports E and F are monitored. Small capacitance increments are added in parallel with C5 and C6 (for example, 1 pF increments) until the waveforms at ports E and F have the same amplitude and a relative phase shift determined by the desired branch reactance value. (We thus tune the combiner branch values by considering how they operate in reverse as a resistance compression network [30,42].) An analogous tuning procedure is applied to branches L1/C1 and L2/C2, and branches L3/C3 and L4/C4 with a sinusoidal signal injected respectively into ports E and F with ports A, B, C, and D terminated in 50 Ohms. Fig. 20 shows a photograph of the tuned combiner PCB, while Table II lists the utilized component values.

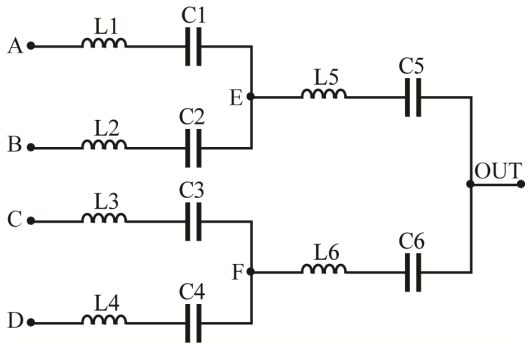


Fig. 19. Power combiner implementation. Component values are indicated in Table II.

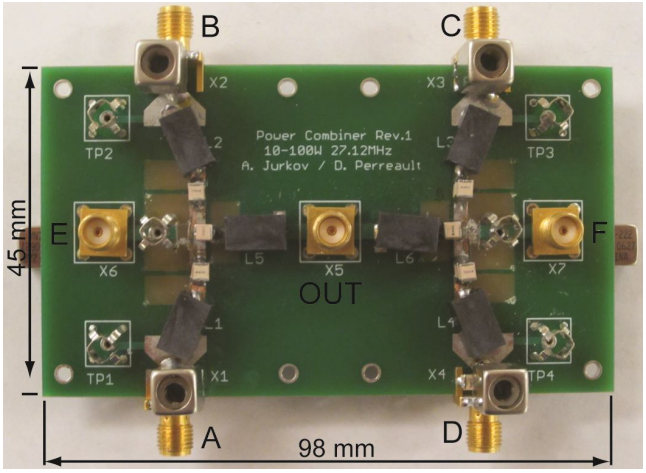


Fig. 20. Photograph of the power combiner.

TABLE II. POWER COMBINER COMPONENT VALUES

Component	Value	Part #	Manufacturer
L1, L3	222 nH	132-14SMJL	Coilcraft Inc.
L2, L4	422 nH	132-18SMJL	
L5	307 nH	132-16SMJL	
L6	538 nH	132-20SMJL	
C1, C3	78.8 pF	ATC100B Capacitor Series	American Technical Ceramics Corp.
C2, C4	167 pF		
C5	57.9 pF		
C6	137 pF		

It is of interest to monitor the voltage waveforms at the combiner's input ports, and so, oscilloscope probe connectors (Part #: 131-4244-00, Tektronix Inc.) are mounted in parallel with the SMA input-port connectors (TP1-TP4 in Fig. 20). However, the resultant parasitic capacitance (approximately 15 pF) at each of the combiner's input ports (the parallel combination of the SMA connector and the oscilloscope probe capacitances) can considerably affect the performance of the combiner and alter its input-impedance characteristics. To address this issue, tunable inductors (7M2-332, Coilcraft Inc.) with a nominal inductance of 3.3 μH are installed in parallel with the probe connectors (X1-X4, Fig. 20) to "resonate-out" the parasitic capacitances at 27.12 MHz. Although there is some small parasitic capacitance associated with the other nodes of the power combiner circuit, their value is measured to be no greater than 3 pF, and so, their effect on the combiner's characteristics is negligible. Note however that during the combiner tuning procedure described above, oscilloscope probes are temporarily connected to ports E and F to monitor the voltage waveforms. In order to "resonate-out" the probes' parasitic capacitances, similar tuning inductors are temporarily installed in parallel with the probes and are removed once the tuning procedure is completed.

Since the proposed power combiner is implemented entirely with reactive components, it is ideally lossless. However, due to the finite quality factor (Q) of the components used, some resistive combiner power loss is expected depending on the combiner's operating point and the respective combiner branch currents. Here we briefly examine the effect of the components' Q on the combiner's efficiency.

According to the respective manufacturer's component datasheets, at the current system operating frequency (27.12 MHz) inductors L1-L6 (see Fig. 19) have an approximate Q of 90, while the tunable inductors X1-X4 have a Q of 25. Capacitors C1-C6 have a much higher Q (greater than 10,000), and so, their losses are negligible compared to those of the inductors.

Fig. 21 depicts the simulated efficiency of the combiner due solely to losses associated with the components' quality factors. It can be seen that over an output power range of 10 W to 100 W (the 10 dB range over which the combiner is designed to operate), it exhibits efficiency above 94%. For output power levels below 10 W, the effective input-port impedances of the combiner are significantly dominated by reactive components (as can be also seen from Fig. 7), thus giving rise to considerable circulating currents (and resistive power losses) and hence resulting in a drop in efficiency.

D. System Control

A PIC32MX460 microcontroller (Microchip Technology Inc.) is utilized to control the four outphaser boards and thus adjust the relative phase shift between the PAs driving the combiner. In order to facilitate the rapid prototyping of various control schemes without the requirement for major hardware redesign, an off-the-shelf development board is used (LV32MX v6, MikroElektronika). The four outphaser boards are connected to the appropriate microcontroller pins through the factory-installed development board connectors.

A simple program is developed for the microcontroller that allows one to adjust the outphasing of the PAs to control the output power. The firmware allows pre-programmed sets of outphasing angles along with manual, real-time independent adjustments to the phase shift of each PA with increments of less than 0.1º.

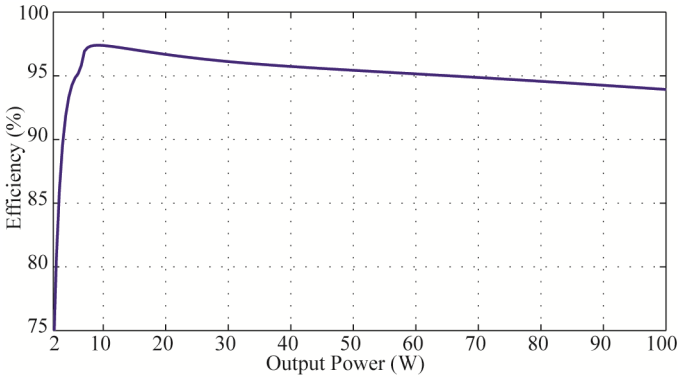


Fig. 21. Simulated combiner efficiency including component losses.

V. System Performance

In order to evaluate the performance of the power combiner and assess the validity of the proposed outphasing control law, the system is tested at various output power levels over approximately a 10 dB power range ratio. For a given desired output power (termed here "commanded" power), the PAs are outphased according to Fig. 6 with θ and ϕ selected for the corresponding power level from Fig. 7. All four PAs are powered from a 16 V dc power supply (HP6554A, Agilent Technologies, Inc.) resulting in a PA output amplitude V_S of approximately 25V. Of course, it is expected that with loading variation of the PAs, their output amplitude may vary slightly - a manifestation of the nonzero output impedance of the PAs. This variation in their output amplitudes is measured and taken in account when comparing the measured combiner output power to the commanded power.

A. Experimental Setup

Four 10 MΩ, 8 pF oscilloscope probes (P6139A, Tektronix Inc.) are connected respectively to test points TP1-TP4 (see Fig. 20) to monitor the input voltage waveforms at the combiner's input ports and ensure correct input signal phases (within ±1º) and fundamental harmonic amplitudes. As was already mentioned, to mitigate the effect of capacitive probe loading on the combiner, tunable inductors (7M2-332, Coilcraft Inc.) are installed in parallel with the probe connectors to "resonate-out" the probe and connector capacitances at 27.12 MHz.

A 100 W, 30 dB attenuator (Part #: 690-30-1, Meca Electronics Inc.) loaded with the input channel of an oscilloscope (TDS3014B, Tektronix Inc.), set to 50 Ω input impedance, is employed as a load for the combiner. The VSWR, as seen by the combiner's output port, is determined

to be approximately 1.04. The combiner output power is measured using a directional RF power meter (5010B, Bird Electronics Corp.). Fig. 22 shows a photograph of the entire experimental setup.

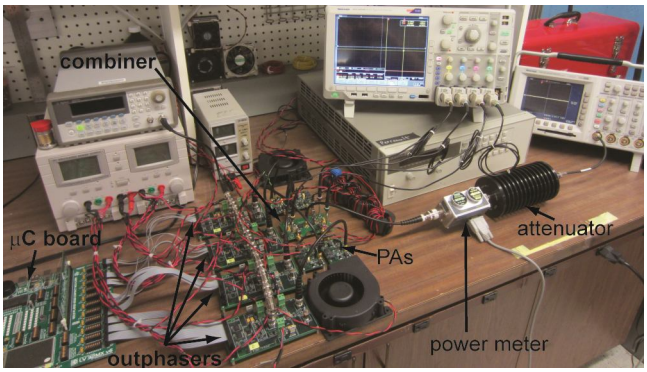


Fig. 22. Photograph of the experimental setup.

B. *Performance Measurements*

As was already mentioned, the output voltage amplitudes of the PAs decrease slightly as their output power is increased (nonzero output impedance). This is exactly demonstrated in Fig. 23 showing the measured output amplitudes of the four PAs (A-D) versus total output power. The loading that the combiner presents to each PA remains approximately evenly distributed among the four PAs as output power is modulated from 10 W to 100 W[1]. This can be inferred from Fig. 23 by noting that the PA output amplitude-power characteristic is approximately equivalent for all four PAs.

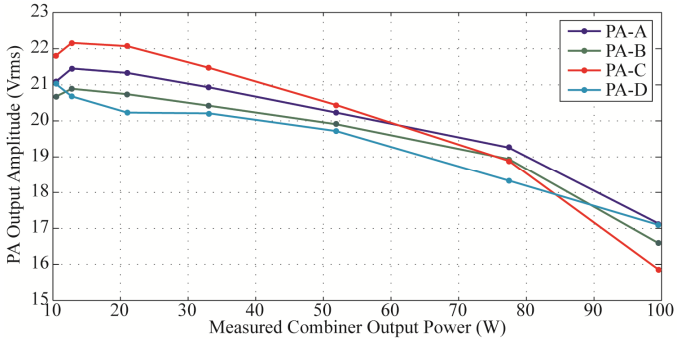
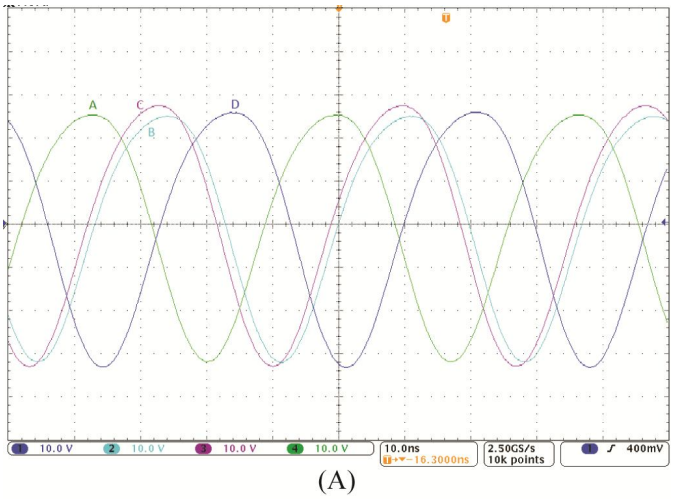
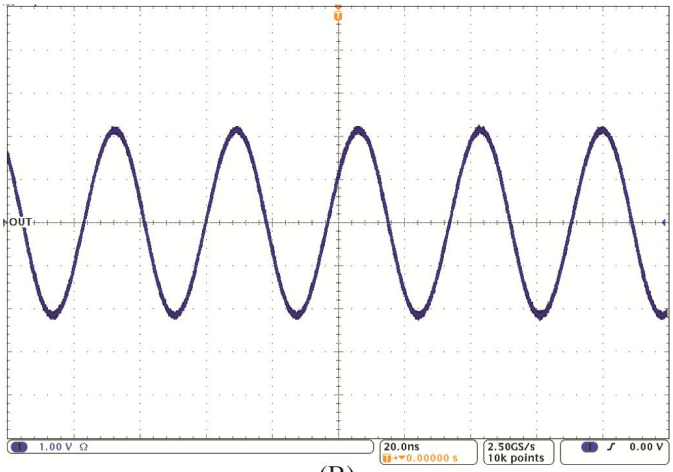


Fig. 23. The magnitude of the fundamental component of each of the PA's output voltage waveforms versus combiner output power.

Fig. 24(A) shows an example oscilloscope screenshot of the measured input terminal voltages V_A - V_D of the combiner for an output power level of 50 W. As can be seen, the voltage waveforms are appropriately outphased for the particular output power level. Although nearly sinusoidal at 27.12 MHz, the presence of significantly smaller higher-frequency harmonics can be noticed in the terminal voltages. These additional harmonics are due to the finite quality factor of the PA output resonant tank. On the other hand, Fig. 24(B) depicts the resulting combiner output voltage waveform for the driving voltages of Fig. 24(A). The purely sinusoidal output voltage waveform is a manifestation of the narrow band-pass implementation of the combiner due to the series LC reactance branches (see Fig. 19).



(A)



(B)

Fig. 24. Oscilloscope screenshot of (A) the combiner input terminal voltages V_A-V_D, and (B) the resulting combiner output voltage across the 50 Ω load (after a 30 dB attenuation) for an output power of 50 W.

The relationship between the combiner's output power and the commanded power is plotted in Fig. 25. It is important to describe the exact steps involved in obtaining the commanded output power characteristic. For each set of outphasing angles, the resulting combiner output power and PA output amplitudes (plotted in Fig. 23) are measured. A simulation is then performed on the ideal combiner (shown in Fig. 19) with its input power ports driven with purely-sinusoidal signals having exactly the same amplitudes as the ones measured from the real system. The combiner output power predicted from this simulation is effectively the commanded power. It is this commanded power that is compared in Fig. 25 to the combiner measured output power. (In effect, this method is a first step towards pre-distorting the PA outphasing control to compensate for the non-zero PA output impedance and the resulting variation in the PA output amplitudes.) As can be seen, the commanded and actual powers are in reasonable

[1] Unlike in the measurements of [37], only the fundamental component of the output is treated as desired output power. (Whether or not harmonic components are properly treated as output power or loss depends upon the application.)

agreement over the entire operating range.

To achieve a more accurate control of the system's output power in spite of the various non-idealities in the implemented system (such as non-zero PA output impedances, mismatches in the combiner reactances, parasitics, etc.), one can apply predistortion in which one observes the mapping between the command (and outphasing angles) and the actual output power and then pre-distorts the command input to achieve a linear input-to-output relationship [39]. This approach is often employed in the control of power amplifiers.

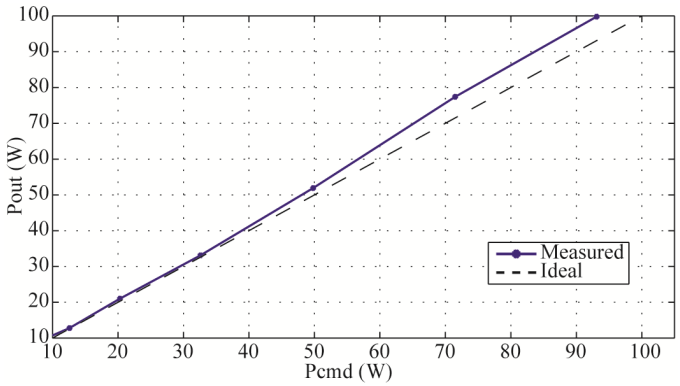


Fig. 25. Measured combiner output power P_{out} versus commanded power P_{cmd}. Reasonable linearity is achieved and can be increased with predistortion.

It is also of interest to examine the efficiency of the entire combining and outphasing system. Here, system efficiency is determined as the ratio of output power delivered to the load to the total PA dc drain input power (excluding PA gate-driving power). Fig. 26 shows the measured system efficiency over a 10 dB output power range (plotted in red) with the error bars representing a ±5% measurement error of the power meter measurements. This encompasses the efficiency loss owning to both the power amplifiers and the combiner. The measured average PA efficiency curve (shown in blue) is obtained by first measuring independently and then averaging the efficiencies of each of the four PAs loaded resistively over a range of output power levels. The PAs are powered from a 16V dc power supply. These efficiency measurements are consistent with the combiner driving methodology described earlier.

As can be seen from Fig. 26, the overall system efficiency is dominated by the PA losses and remains high over a wide power range. The load modulation effect of the combiner makes many of the conduction loss components in both the PA and the combiner reduce with output power. As was previously mentioned, variations in susceptive loading of the PAs (due to any susceptive components of the combiner's effective input admittances) can considerably mistune the output resonant tanks of the PAs and introduce additional losses (termed here combiner/PA interface losses). Neglecting such interface losses, one would expect the overall system efficiency to be determined by the product of the PA and power combiner efficiencies. Fig. 26 shows the expected system efficiency for the present system (ignoring combiner/PA interface losses) obtained by multiplying the measured average PA efficiency with the combiner efficiency of Fig. 21. As can be seen, the expected system efficiency is within the uncertainty of the overall system efficiency measurements, suggesting that indeed, the combiner does maintain an overall resistive loading of the PAs over most of the operating power range.

For the sake of comparison, Fig. 26 illustrates the overall system efficiency one would expect to achieve from a power amplification system employing an ideal class-B amplifier. (At its peak output power, an ideal class-B amplifier has an efficiency of $\pi/4$ or 78.5%, with efficiency falling as the square root of output power.) Clearly, the presently implemented outphasing amplifier system incorporating switched-mode amplifiers exhibits dramatic efficiency improvements compared to its class-B counterpart, especially considering that the idealized class-B efficiency curve shown in Fig. 26 is unattainable in reality.

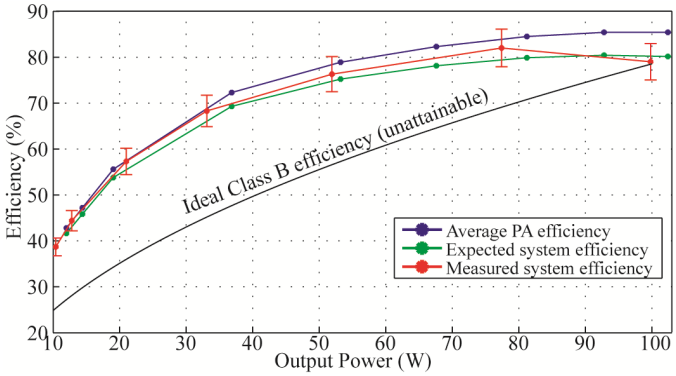


Fig. 26. Comparison among measured system power efficiency, expected system efficiency, average PA efficiency, and the efficiency that would be expected from a similar system if it were implemented with a single ideal linear class-B PA.

Finally, Fig. 27 shows the distribution of total PA input power among the individual PAs. As can be seen, the employed outphasing control law indeed results in a relatively even loading of the PAs over most of the considered operating range.

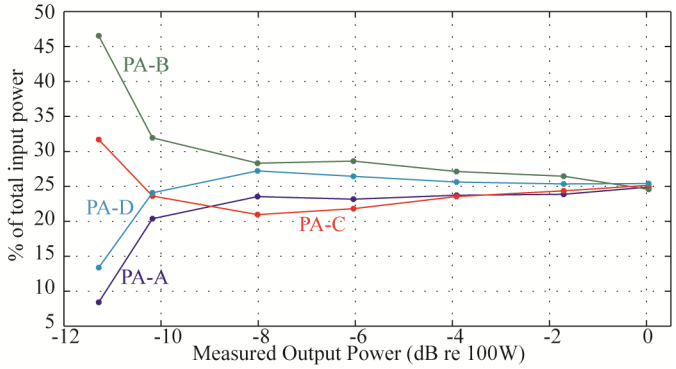


Fig. 27. Total input power distribution among PAs versus combiner output power.

The system is not evaluated for dynamic tracking of command signals (which is beyond the scope of this work). The expected performance would depend on the details of the combiner and PA design. Simulation results indicate the ability of the combiner to accurately track command inputs of

up to approximately 0.5% of the carrier frequency (e.g., AM modulation at 135.6 kHz bandwidth).

VI. Topological Variations of the Power Combiner Network

Although the present work focuses on the "binary-tree" implementation of the four-way combiner (Fig. 5), it is important to recognize that other possible topological implementations of the combiner network are possible. This section aims to enumerate some of them.

Fig. 28 (B) illustrates one possible four-way combiner implementation that can result from applying the T-Δ transformation to the various T-networks found in the basic "binary-tree" four-way combiner of Fig. 28(A). An important characteristic of this transformation is that it does not affect the transformed network's interface with other networks connected to its terminals. In other words, the current-voltage relationship at each terminal of the transformed network is preserved under the transformation. Although unnecessary, it is convenient to think of the basic combiner in Fig. 28(A) as the starting point for all the T-Δ transformations. For this reason, the reactance magnitudes in the implementation variant of Fig. 28(B) are given in terms of the reactance magnitudes of the basic combiner. The suggested reactance magnitude values for a particular implementation ensure that its input-port and output-port characteristics are identical to those of the basic combiner. It should be noted that the same transformations can be applied to the combiner and load networks in other power combiner implementations, and that for given achievable component quality factors there may be practical efficiency differences among various implementations. Other possible combiner implementations and their effect on the combiner efficiency are discussed in detail in [36].

Considering a different possibility, Fig. 28(A*)-(B*) show the corresponding topological duals of the combiner networks of Fig. 28(A)-(B). Specific component values may be found for the dual network as is well known [40]. As a result of this transformation, the PAs are now modeled respectively by current sources I_A-I_D having equivalent magnitude and phase relationship as the voltage sources of Fig. 28(A)-(B), though it is recognized that this is for modeling purposes and to show the connection ports of the power amplifiers - the power amplifiers need not to act as ideal voltage or current sources. Note that for any particular outphasing control method, the input admittance versus output power characteristic of the permutations shown in Fig. 28(A)-(B) is equivalent to the input *impedance* versus output power characteristic of their respective duals. Conveniently, the relationship between the output power delivered to the load and the outphasing control methodology is unaffected by the topological duality transformation. Thus, all of the presented outphasing control methods previously introduced are directly applicable to the implementation variants of Fig. 28(A*)-(B*), although, in this case, it will be more appropriate to refer to the optimal-susceptance control method as the optimal-reactance control method, in keeping with the effects of topological duality on interchanging voltages and currents, and admittances and impedances. The respective topological duals of other combiner implementations obtained from T-Δ transformations on Fig. 28(A) are summarized and discussed in [36].

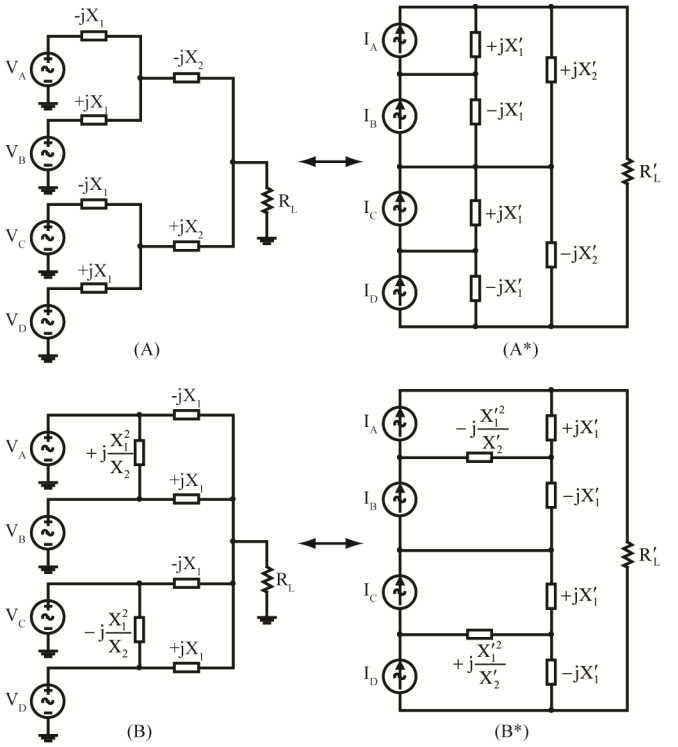


Fig. 28. Implementation variants of the basic "binary-tree" four-way combiner as a result of T-Δ transformations, and their corresponding duals.

VII. Conclusion

This paper presented the design, control and experimental validation of a new lossless multi-way outphasing system that offers major performance advantages over conventional outphasing and combining approaches.

A brief overview of the key combiner input and output port characteristics was provided. The paper described how the combiner's output power can be controlled through the outphasing of the PAs, and new, optimized outphasing control strategies were described. Furthermore, a straightforward methodology for designing the combiner network according to performance specifications was presented, and various combiner network topologies were listed.

Moreover, we presented the first-ever experimental demonstration of this new power combining and outphasing strategy. We described a 27.12 MHz combining and outphasing system and used it to experimentally evaluate its power-combining performance over a 10 dB output power range. It was demonstrated that the proposed outphasing control strategy is effective in controlling the system output power while evenly and resistively loading the power amplifiers over the operating range.

APPENDIX

A. *Combiner Sensitivity to Loading Variations*

Although the presented combiner above is ideally designed to deliver power to a fixed and well-known load impedance (at the operating frequency), in reality, its value may vary by a certain amount (both resistively and reactively). Consequently, this could result in significant variation to the PA loading characteristics from the ones described above. This section presents an intuitive approach for understanding the effect of such loading impedance variations on the combiner's input port characteristics.

Consider the four-way combiner of Fig. 5 designed to operate with a loading impedance $Z_L = R_L$. Now suppose that this impedance changes by a resistive increment ΔR_L and a reactive increment ΔX_L, i.e., $Z_L = (R_L + \Delta R_L) + j\Delta X_L$. To determine the effect of this load variation on the combiner's effective input admittances, one can first determine the resultant combiner input-port current increments ΔI_A - ΔI_D (sourced by the PAs).

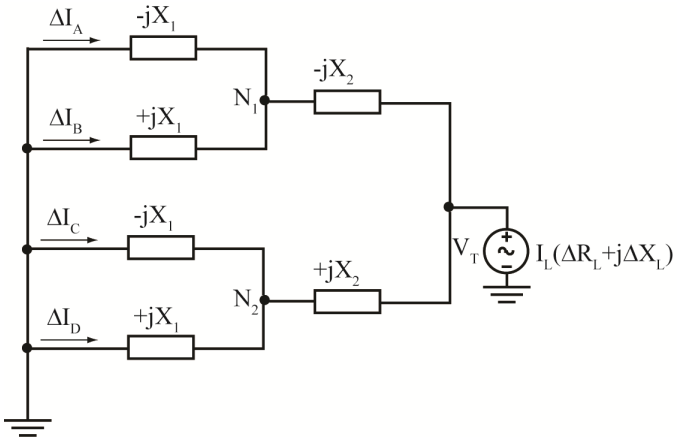


Fig. 29 Network utilized for analyzing the incremental change of sourced input currents by the power amplifiers (Fig. 5) for a given incremental resistive/reactive change in load impedance R_L by employing the Alteration Theorem [41]. I_L is the load current in Fig. 5 when $\Delta R_L = \Delta X_L = 0$.

Since the driving voltage waveforms at the combiner input terminals are maintained unchanged both in phase and amplitude by the PAs (treating the PAs as ideal voltage sources), the resultant effective input admittances can then be easily determined.

One possible way for calculating ΔI_A through ΔI_D is through application of the Alteration Theorem [41]: the PAs are short-circuited, and the modified load $Z_L = (R_L + \Delta R_L) + j\Delta X_L$ is replaced by a voltage source $V_T = I_L(\Delta R_L + j\Delta X_L)$, where I_L is the *original* load current (when $Z_L = R_L$). The modified circuit is illustrated in Fig. 29. By employing conventional linear circuit analysis techniques, it is readily shown that the incremental currents are given by (22).

This is easy to see since the effective parallel impedance of reactive branch pairs A/B and C/D is infinite, and so, the voltage at nodes N_1 and N_2 is $V_{N1} = V_{N2} = V_T = I_L(\Delta R_L + j\Delta X_L)$. Moreover, I_L can be further expressed in terms of the output power P_{out} delivered to the original load R_L ($\Delta R_L = \Delta X_L = 0$). The sign in (22) is selected depending on the nature of the X_1 reactive branch: (+) for an inductive branch and (-) for a capacitive branch.

$$\begin{aligned}\Delta I_{A-D} &= \pm j\frac{I_L(\Delta R_L + j\Delta X_L)}{X_1} = \\ &= \pm j\frac{(\Delta R_L + j\Delta X_L)}{X_1}\sqrt{\frac{2P_{out}}{R_L}} = \\ &= \pm\sqrt{\frac{2P_{out}}{R_L}}\frac{(-\Delta X_L + j\Delta R_L)}{X_1}\end{aligned} \quad (22)$$

A current increment ΔI_A - ΔI_D can introduce additional phase φ between a PA's output current and voltage waveforms and consequently alter its effective loading. Fig. 30 illustrates this in the case of the PA driving the capacitive branch A (Fig. 5). Originally (when $\Delta R_L = \Delta X_L = 0$), the PA's output voltage V_A and current I_A are approximately in phase (a reasonable approximation for narrow operating power ranges and over most of the operating range of interest). A variation in the combiner's load produces a current increment $\Delta I_A = \Delta I_{A,re} + j\Delta I_{A,im}$, which adds to the original PA output current I_A and results in an effective input admittance phase φ.

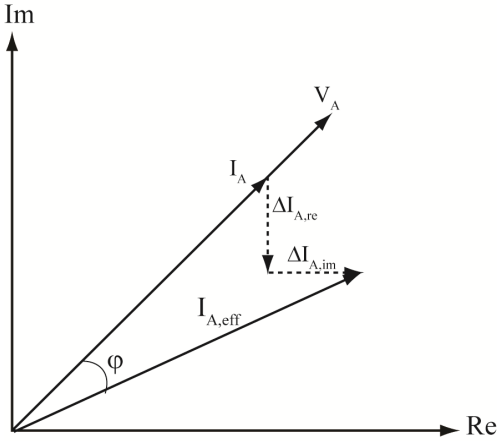


Fig. 30 Phasor diagram illustrating the effect of combiner load variation on its effective input admittance. The input terminal current increments $\Delta I_{A,re}$ and $\Delta I_{A,im}$ resulting from deviation of the combiner's load from its nominal value introduce additional input admittance phase.

As an example, consider Fig. 31 illustrating the effect of 2.5% and 5% resistive variations (top) and reactive variations (bottom) of the nominal 50 Ω, purely-resistive combiner load on the input admittance phase characteristic of the four-way combiner of Fig. 5 (X_1 = 36.69 Ω and X_2 = 48.97 Ω). As can be seen, even small variations of the combiner loading may have appreciable effect on the effective PA loading, although even for a +/- 5% combiner loading variation, the PA loading still remains mostly resistive. In cases where the combiner load varies, but the resultant input admittance variations are not tolerable, one can employ an isolator, a resistance compression network or other means of mitigating load resistance variation.

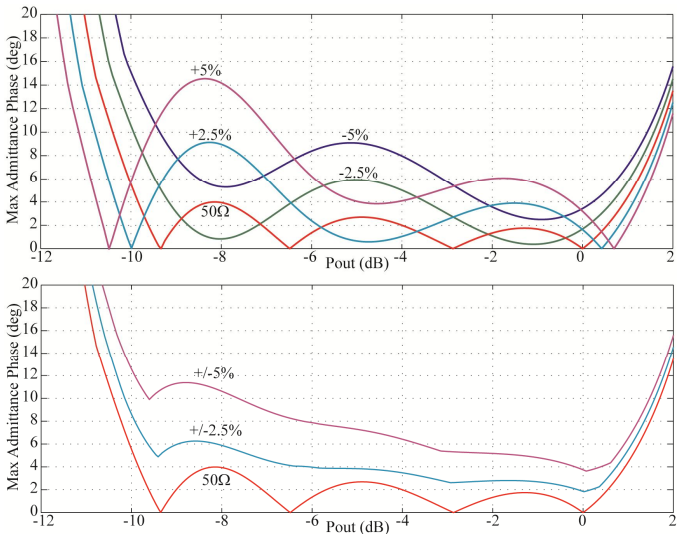


Fig. 31 Maximum admittance phase (absolute value) seen among the PAs driving the four-way combiner of Fig. 5 (R_L = 50 Ω, X_1 = 36.69 Ω, and X_2 = 48.97 Ω) versus output power back-off as a result of 2.5% and 5% purely-resistive (top plot) and purely-reactive (bottom plot) variations of the 50 Ω nominal combiner load.

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