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Integrated DC-DC boost converters using CMOS silicon on Sapphire Technology

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INTEGRATED DC-DC BOOST CONVERTERS USING CMOS SILICON ON SAPPHIRE TECHNOLOGY

A Thesis

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TO MY PARENTS

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ABSTRACT

Mohammad, Imaduddin. M.S.E.C.E., Purdue University, May 2014. Integrated DC-DC Boost Converters using CMOS Silicon on Sapphire Technology. Major Professor: Saeed Mohammadi.

With the recent advancements in semiconductor manufacturing towards smaller, faster and more efficient microelectronic systems, the problems of increasing leakage current and reduced breakdown voltage in bulk-CMOS transistors have become substantial in the sub-100-nanometer era. The Peregrine UltraCMOS Silicon-on-Sapphire (SOS) technology that uses highly-insulating sapphire substrate as insulator was introduced to meet the continually growing need for higher performance RF products. The electrically isolated circuit elements in the UltraCMOS technology lead to increased switching speeds and lower power consumption due to reduced junction and parasitic capacitances. Furthermore, the growing need for high-speed switching applications such as boosting a lower voltage level to a higher one gives the UltraCMOS technology an upper hand over the bulk-CMOS process.

The limitation to using an UltraCMOS transistor is that its maximum drain to source voltage (V_{DS}) swing is 2.5V. This thesis aims to address this limitation by studying and implementing various stacking techniques in high power switching applications where voltage switching of higher than 2.5V are required. Fully-integrated DC to DC boost converters with switching circuits based on dynamically self-biased stacked transistors are proposed. For high voltage and high power handling, the proposed stacking techniques equally distribute the overall output voltage to less than 2.5V across each stacked transistor in the switch (V_{DS} of 2.5V).

1. INTRODUCTION

1.1 Brief Evolution of CMOS Technology

In order to keep up with the ever-growing technological advancements over the past five decades, the semiconductor industry has gone under the hammer about every two to three years to develop smaller, faster and more efficient transistors [1]. Each technological juncture has evidenced continual changes in features of the metal-oxide-semiconductor field-effect transistor (MOSFET) where the transistor size was reduced approximately by 30%, while its density and speed were doubled [2] to facilitate the realization of integrated circuits (ICs) giving rise to better performances at lower costs.

However, scientists started facing difficulties in further reducing the transistor size, and thus lowering the effective costs, as research and technology entered the sub-100-namometer (nm) age. The scalability demands have given rise to a problem of increasing leakage current primarily because of two reasons: (i) The physical limits of thinning down the gate oxide thickness have been reached, and (ii) The non-uniformity in doping of impurities to form source/drain regions that causes a larger charge depletion region to form at the bottom of the source/drain-doped regions [2]. Scientists have been compelled to research beyond the down scaling of the transistor and look into modifications of transistor design and manufacturing process [2].

To overcome these challenges in scaling the complementary metal-oxide-semiconductor (CMOS), scientists began investigating the possibilities of minimizing the leakage current paths by depleting the entire silicon (Si) layer, which led to the introduction of the silicon-on-insulator (SOI) technology.

The idea of manufacturing the transistor with the SOI technology has been around for nearly four decades, but higher power consumption of scaled bulk CMOS technology has made the SOI technology a viable option primarily due to its low power consumption and higher performance characteristics [3], [4].

In a SOI transistor, a layer of silicon dioxide (SiO_2) is used as an insulator and is inserted between a top layer of thin silicon and a bottom layer of thick silicon for physical support [2]. The presence of a buried oxide and electrically isolated circuit elements reduces the parasitic or junction capacitances, which leads to higher switching speeds and notably lower power consumption at the same speed than those of bulk CMOS transistors.

Figure 1.1 depicts the cross-section of the bulk CMOS and SOI CMOS devices, and Figure 1.2 illustrates the lower leakage currents, by approximately three orders of magnitude, in SOI CMOS than that of bulk CMOS at minimum gate voltage levels required to turn the transistor on. As pointed out in figure 1, bulk CMOS device has a higher leakage current due to the depletion region extending out into the silicon substrate. On the other hand, the electrical isolation of the silicon substrate with the help of a buried SiO_2 layer minimizes the area for leakage current to prevail. This reduces the source/drain junction capacitances, resulting in lower RC (resistor-capacitor) delay, and thus leading to higher switching speeds in SOI CMOS devices.

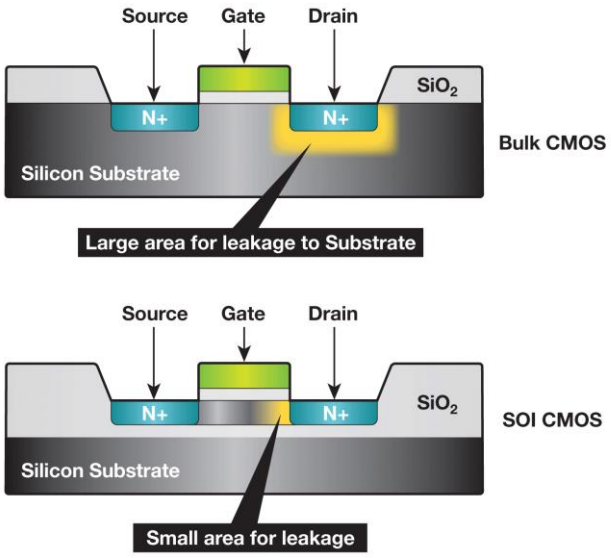


Figure 1.1 Comparison of leakage current paths in bulk CMOS and SOI CMOS [5]

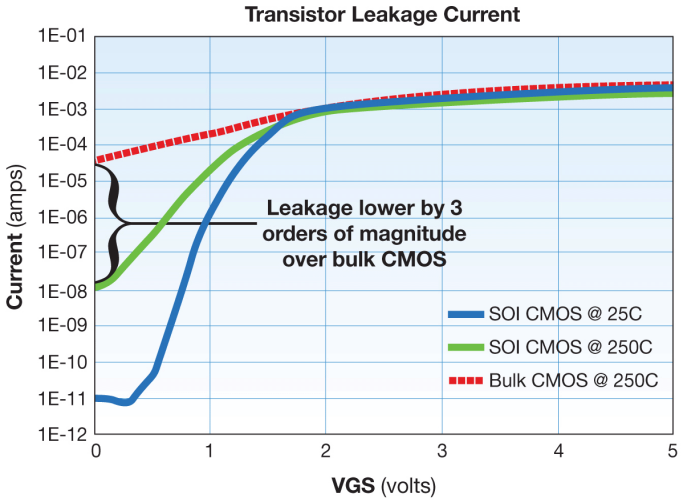


Figure 1.2 Leakage current (in amperes) in bulk CMOS and SOI CMOS [5]

Furthermore, the layout of SOI CMOS device does not require wells to separate the n-doped region apart from the p-doped region due to the electrical isolation provided by the SiO2 insulator layer [6]. As a result, a smaller layout area is required by SOI

transistors as opposed to larger area required for bulk CMOS transistors, which in turn leads to smaller leakage current and lower source/drain junction capacitances. Consequently, SOI CMOS circuits have a higher device density which leads to their advantageous characteristics of lower power consumptions at higher operating speeds.

These features of having lower power consumption at speeds going up into the gigahertz (GHz) range makes SOI CMOS technology the practical choice to use in high-speed wireless communications. One very useful application for such technology in this fast-growing wireless-multimedia-multifunctional *portable-device*-dominant world is to improve the battery lives of widely used mobile phones, tablets and phablets. Moreover, the SOI CMOS is also a very viable technology for all radio frequency (RF) applications that require high speeds, low power consumption and integration on a single chip.

1.2 Peregrine UltraCMOS technology (SOS)

There is continually growing need for higher performance, low power dissipation, less expensive and smaller RF products. Although the SOI CMOS technology has been satisfying present day requirements for such growing limitations, researchers have continued to investigate even better performing state-of-the-art CMOS designs and manufacturing processes. The UltraCMOS Silicon-on-Sapphire (SOS) process is a patented variation of the SOI technology produced by Peregrine Semiconductor that promises a ‘combination of high-performance RF, mixed-signal, passive elements, nonvolatile memory and digital functions on a single device’ [7]. SOS is one of the first of the SOI semiconductor manufacturing technologies that is manufactured by forming a thin layer of silicon onto a sapphire wafer [8]. The main advantage of the SOS technology for electronic circuits is the use of ‘the highly-insulating sapphire substrate’ [8]. Figure 1.3 illustrates the comparison of the cross-sections of Peregrine’s UltraCMOS and the bulk CMOS processes.

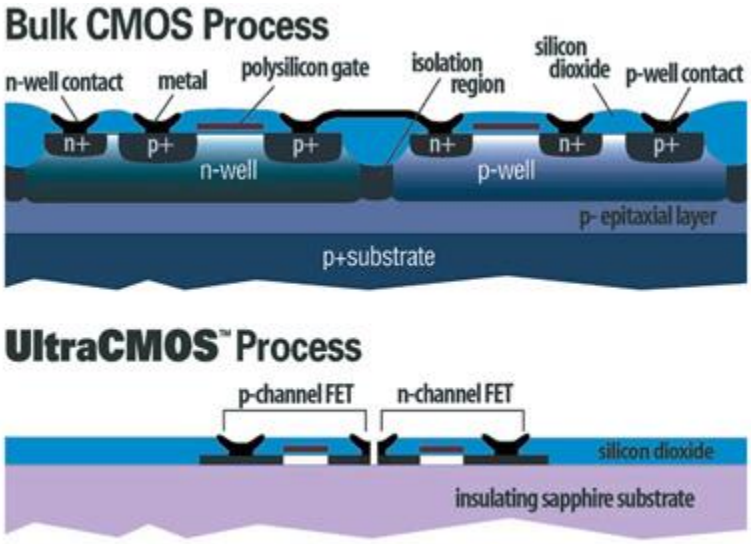


Figure 1.3 Comparison of cross-sections of UltraCMOS and bulk CMOS technologies [8]

By utilizing the insulating sapphire substrate, the UltraCMOS process benefits from higher operating speeds, lower power consumption and very low parasitic/junction capacitances when compared to the bulk CMOS technology.

All circuit designs to be discussed in this thesis have been implemented using the 0.25-µm UltraCMOS process. This particular process comprises of three n-channel MOSFET (NMOS) and three p-channel MOSFET (PMOS) threshold voltages, with one NMOS and one PMOS having a threshold voltage (V_{th}) of approximately zero volts. Furthermore, one limitation realized after running some device measurements is that the maximum voltage swing (drain-to-source voltage, or V_{DS}) of these transistors is 2.5V. These 0.25-µm transistors breakdown at swings greater than 2.5V. Stacking of these transistors in series so as to distribute the swing and limit the V_{DS} across each individual transistor to 2.5V by intelligent biasing is a key to utilizing these devices as high-voltage swing switches and drivers. Key features of the 0.25-µm UltraCMOS process are summarized in Table 1. Overall, Peregrine promises that monolithic integration of its UltraCMOS devices provides significant peak performance levels comparable to the

widely used non-CMOS technologies for RF applications such as gallium arsenide (GaAs) and silicon-germanium (SiGe) [8].

Table 1-1 Summary of features for 0.25-µm UltraCMOS process by Peregrine Semiconductor [8]

Features Summary	**Process details**
Generation	0.25-µm
Supply Voltage	2.5V/3.0V/3.3V
Interconnect Layout Layers	3
Transistor V_{th}	3 NMOS/3 PMOS
Ft (Zero-V_{th} Device)	30 GHz
f_{max}	90 GHz

1.2.1 Need for higher boosting voltages with high efficiencies

Portable devices – not limited to mobile phones, tablets, phablets and laptops – that form an integral part of today's wireless communications-dominated lives receive their power primarily from batteries. These electronic devices consist of smaller internal components and circuitry with each of them requiring their own individual power supplies, generally different voltage levels from what is supplied by the main batteries. Power management hence plays a key role in designing high performance and efficient electronic devices, where power supplies for the sub-components and circuitry need to be well orchestrated using the devices' batteries' supply voltage as the main source.

Direct current (DC) to DC converters emerge as the solution to solve the power management problems in portable devices because the converters can be used to regulate the supply voltages to each individual sub-circuitry either by generating increased voltage levels or reduced voltage levels from one single main battery supply. Commonly, these DC to DC converters regulate the output voltage to get the desired voltage levels.

Boost DC to DC converters increase a lower DC voltage level to a higher one. Such converters are utilized in RF applications that require higher supply voltage levels in order to operate at their optimum. For instance, RF power amplifiers (PAs) implemented using CMOS technology in [9] and [10] require DC voltage levels in the range of 4.5V up to 15 V in order to deliver the optimum output powers and efficiencies. However, the standard available supply voltage levels for wireless communications or electronic devices goes up to 3.0V or 3.3V. So for such PAs to be fully integrated into portable devices, highly efficient on-chip boost DC to DC converters are required to boost the DC voltages from 3.0V or 3.3V up to the desired power supply values.

1.3 Thesis Organization

The thesis mainly focuses on the use of a new CMOS technology from Peregrine Semiconductor called UltraCMOS that is very suitable for high speed applications. This thesis proposes circuits that can be used as drivers/switches for designing boost DC to DC converters.

Chapter 2 discusses the need for stacking of UltraCMOS transistors for high power applications. Then it briefly presents various stacking techniques that have been proposed and implemented in the literature. Next, a dynamically-biased switch/driver that can be used in place of power transistors for switching applications is proposed and its benefits and advantages over other stacking methods are presented for UltraCMOS technology.

Chapter 3 evaluates three different umbrella designs for boost converters: conventional boost DC to DC converter, charge pump converter, and an attempted AC to DC converter. First, a literature review of some previously proposed boost DC to DC converters is presented, which is followed by a sub-section on theoretical analysis of the conventional boost DC to DC converters. Next, a section on charge pump converters starts off by discussing a few different charge pump circuits proposed in the literature. This is followed by a sub-section that presents the analysis and simulation results of an implemented Dickson charge pump converter in the UltraCMOS technology. Second, a

brief section on the attempt made to design and simulate an AC to DC converter is presented. In the last section of chapter 3, implemented conventional boost DC to DC converters utilizing different dynamically self-biased switch stacking techniques in the UltraCMOS technology are proposed. Analyses and simulation results of the proposed converters are also presented.

Last, a summary and conclusion are presented in Chapter 4.

2. TRANSISTOR STACKING

2.1 Stacking of Switching Transistors

The transistors of the Peregrine UltraCMOS SOS technology being used in this thesis have a maximum safe voltage swing of 2.5V. So if any transistor's drain to source voltage exceeds 2.5V, the transistor breaks down. A typical solution to overcome the voltage swing limitations in CMOS transistors is to stack them on top of each other, where the source of one transistor in the stack is connected to the drain of the transistor that is right below it. Stacking helps to distribute the voltage swing and limit the individual swing of each stacked transistor to 2.5V or less. However, biasing (or applying the right DC voltage to the gate of a transistor) the stacked transistors is the key to having equal, both in phase and amplitude, distribution of larger voltage swings. Common applications that require higher voltage swings across the transistors are when the transistors are used for switching or as drivers to an electronic circuit [9-10].

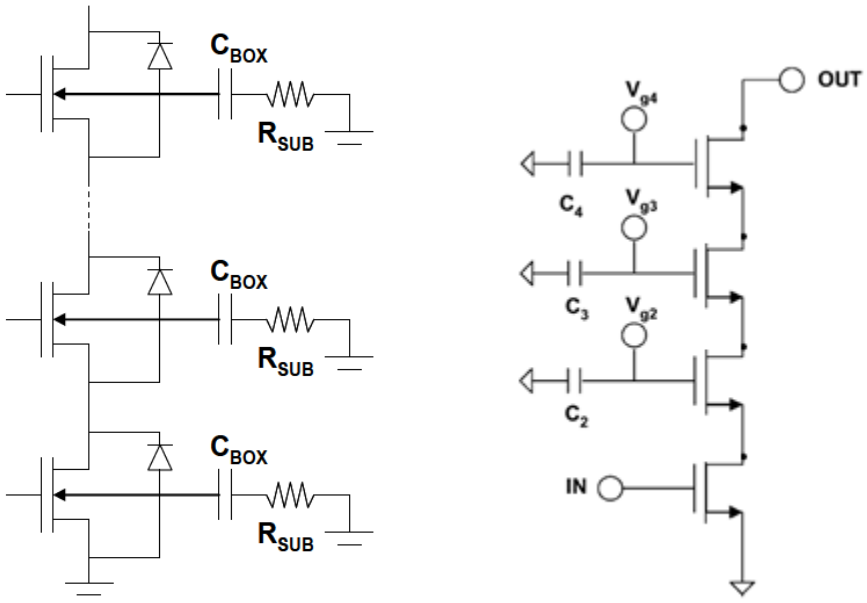
Different implementations of stacked transistors have been limited to a maximum of four transistors in a stack due to several reasons [11]. Some of the prime reasons are briefly discussed as follows:

(a) The top-most transistor in a stack of transistors experiences gate-oxide breakdown for large voltage swings when certain fixed bias voltages are applied to each transistor in the stack.

(b) Parasitic capacitances of the stacked transistors that are connected to a common ground disturb the symmetry of the stacking, resulting in varying phases and amplitudes for the drain to source voltages of the transistors in the stack. The discrepancies in the amplitudes of the drain to source voltages of individual

transistors in the stack result in the top-most transistor to have significantly higher voltage swing than the swings of the other transistors [12]. Furthermore, variations in the phases of the stacked transistors lead to inefficient addition of the individual voltage swings, resulting in a lower combined voltage swing [13]. Thus, the top-most transistor in the stack is highly prone to breakdown before the other transistors, causing circuit instability and malfunction.

Figure 2.1(a) shows the schematic of stacked transistors for the CMOS SOI technology. R_{SUB} represents the substrate resistivity seen by each transistor, and a small buried oxide capacitor C_{BOX} connects each of the CMOS SOI transistors to their respective substrates.



(a) (b)

Figure 2.1 Schematic showing (a) the substrate resistivity, R_{SUB}, and buried oxide layer capacitance, C_{BOX}, generally for the stacked CMOS SOI transistors, (b) implementation of capacitive loads at gate to adjust individual transistor voltage swings [14]

The RC combination of the R_{SUB} and C_{BOX} gives rise to some phase imbalance in the input impedance of each transistor. As a result, simple stacking of the CMOS SOI or SOS transistors would cause phase imbalance as one goes up the stack, and a lot of efficiency

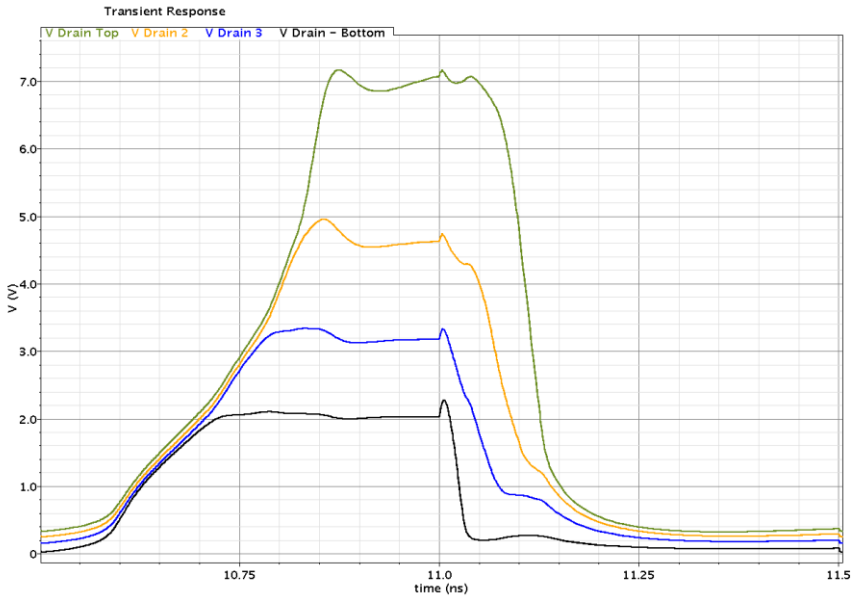
would be lost near the top-most transistor for applications that need large voltage swings or large stack of transistors.

The buried oxide layers in the SOI and SOS technologies ensure that these transistors are electrically isolated from the silicon substrates. Moreover, transistors in these technologies are electrically isolated from each other due to the trench oxide regions that surround each of them, preventing substrate breakdown and leakage currents [11]. Furthermore, reduced junction/parasitic capacitances in CMOS SOS technology aid in minimizing the phase and amplitude imbalances for transistors.

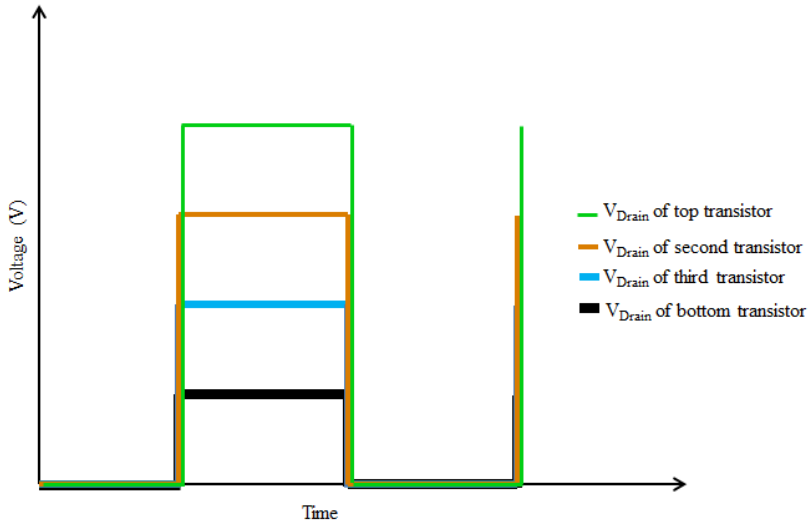
One solution that has been tried to adjust the voltage swings for a stack of multiple common-gate (CG) transistors was the adding of appropriate capacitance as capacitive loads at the gates of the individual transistors in the stack, as shown in Figure 2.1(b) [5]. However, the downside of this stacking technique is that as the number of transistors is increased upwards in the stack, the capacitance values for the capacitive loads decreases significantly and becomes comparable to the parasitic capacitances. Thus, the number of stacked transistors is limited to three to four transistors for this stacking method. Furthermore, significant phase and voltage swing differences occur among transistors from the bottom of the stack towards the top, as shown in Figure 2.2(a). Figure 2.2(b) illustrates what the ideal voltage swings would look like.

One stacking technique, widely implemented in the designs of power amplifiers (PA) [12-14], is to additively combine the output voltages of the multiple stacked single common-source (CS) transistors, as shown in Figure 2.3(a), as one output. The idea again is to equally distribute the voltage swing of each transistor in the stack. Figure 2.3(b) portrays the common structure of the voltage combiner using transformers [15]. The transformers help isolate the performances of the individual stacked transistors from each other, and their respective individual outputs are additively combined as the overall output. One downside with this stacking structure is that the insertion loss of on-chip implementation, mainly due to the transformers at high speeds, results in some loss in the

overall output voltage. Nevertheless, this structure is widely preferred over the one that uses stacked CG transistors.

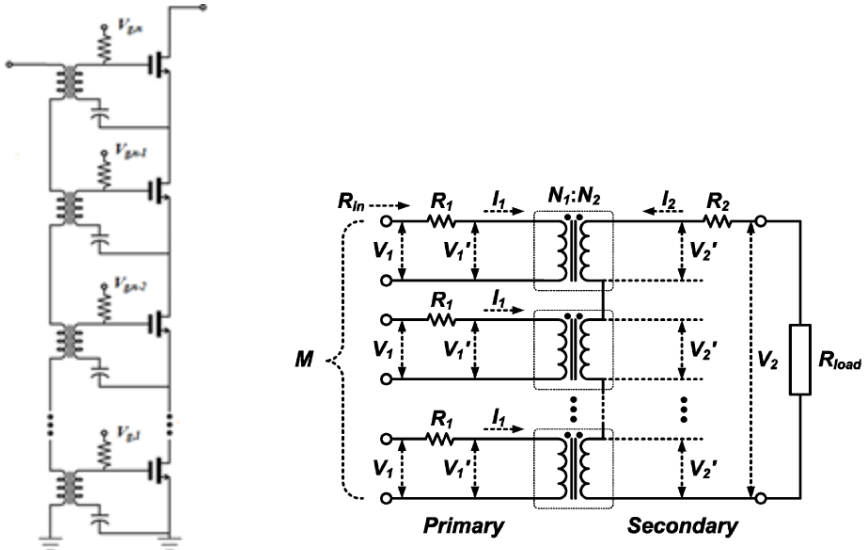


(a)



(b)

Figure 2.2 (a) Voltage phase and amplitude imbalances observed in a sample simulation for a 4-transistor stack of CG transistors, (b) Sample ideal drain voltages for the 4-transistor stack



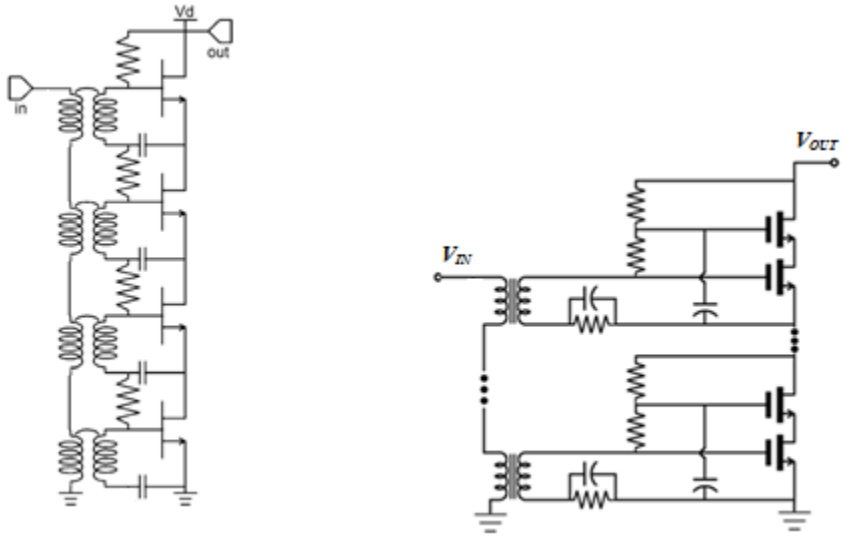
(a) (b)

Figure 2.3 Schematic depicting (a) the combining of output voltages of the multiple stacked single CS transistors, (b) the common structure of the voltage combiner using transformers [15]

The feedback by the gate to drain capacitance of the top transistor results in a large voltage swing across the gate of the top transistor in a stack. The added phase lead caused by the distributed RC nature of the stacked transistor mostly causes instability. Reducing parasitic capacitances to ground helps in reducing the phase differences and consequently improves circuit stability. In order to overcome the loss in output voltage in the voltage combining stacking technique, a stack with feedback gate to drain resistors and transformer coupled CS transistors where the transformers are connected in series has been proposed, as depicted in Figure 2.4(a) [12], [16].

Furthermore, cascode configurations can be used in place of the individual CS transistors as this eliminates the capacitive feedback path and helps in establishing a stable operation. Figure 2.4(b) shows the schematic of the stacked cascode transistors where the

input signal is coupled to the CS transistors within each cascode using on-chip transformers [11].



(a) (b)

Figure 2.4 Transformer coupled stacking techniques with feedback resistors when individual cells are (a) CS transistors [12], and (b) in cascode transistor configurations

The stacking technique proposed in Figure 2.4(b) is essentially a dynamically-biased stacking method where one cell consists of a cascode of two transistors – the top transistor is a CG and the bottom one is a CS – with one input transformer and a feedback biasing network formed through resistors between the drain and gate of the CG and between the gates of the CG and the CS in the cascode cell.

The feedback network imposes a self-biasing technique in each cascode cell and the gate bias of each transistor is allowed to float such that the bias values are always between the respective source and drain voltages. Furthermore, this self-biasing prevents gate-oxide breakdown in the stacked transistors, especially for the top-most transistor as it has a relatively larger drain voltage than all other transistors in the stack.

Replacing the CS stacked cells, shown in Figure 2.4(a), with dynamically-biased cascode transistor cells, as shown in Figure 2.4(b), decreases the capacitive feedback occurring through the gate to drain capacitance from input (gate terminal) to output (drain terminal) of each transistor. Moreover, this reduces the imbalances seen in voltage phases and amplitudes in a stack of transistors [11]. Again, the top-most transistor cell in the stack benefits from the cascode configuration as the coupling of its high drain voltage through the gate to drain capacitor and gate capacitor to ground is minimized. In addition, for a cascode configuration one transformer is shared by two transistors as opposed one transformer per transistor for the CS cell, and this allows each transformer to tolerate twice as much voltage swing.

3. BOOST DC-DC CONVERTERS

3.1 Introduction and Purpose

Highly efficient step-up or boost DC to DC converters are used for many applications such as fuel-cell and solar-cell energy conversion systems on the high voltage side and for RF and analog circuitry, especially RF PAs, on the low power-low voltage side.

Design of fully on-chip converters are a challenge as some of the passive analog components – inductors and capacitors that are mainly used for charge storage and discharge – used in various boost DC to DC topologies are large and lossy, and preferred to be as off-chip components in order to gain small area and high efficiency for the converters. However, operating at high speeds, in the RF range with frequencies in GHz range, helps reducing the values of passive components with sizes that can be easily implemented on-chip. The values of inductor and capacitor used are inversely proportional to the frequency according to:

$$L = \frac{X_L}{2\pi \times f} \tag{3.1}$$

$$C = \frac{1}{2\pi \times f \times X_C} \tag{3.2}$$

where X_L is the reactance for inductor L, X_C is the reactance for capacitor C and f is the switching or operating frequency.

The purpose of this chapter is to present designs and simulation results of possible boost DC to DC converters at an operating frequency of as high as up to 1 GHz with all of their respective components on-chip. Various challenges in meeting the on-chip requirement and technological limitations are addressed as well.

3.2 Literature Review

Flyback transformers are common go to circuit components when seeking higher voltages. DC to DC flyback converters have the advantage of being relatively simple in design and structure and provide high voltage gains, however, they suffer from high voltage stresses due to leakage inductance of the transformer and are usually designed using off-chip components [17], [18].

Research has been done on transformerless DC to DC converter topologies to eliminate the losses incurred through transformers and switching. The topology proposed in [19], shown in Figure 3.1, employs an adaptive gate switching controller (AGSC) in order to reduce non-ideal power losses due to gate switching. The AGSC proposed utilizes dead-time controller and zero-current detector to turn the synchronous switch on and off respectively. The AGSC proposed achieves 'near-optimal gate switching control' irrespective of other process parameters and variations [19]. The 0.18-µm 3.3V CMOS technology is used to implement a boost DC-DC converter. For an input voltage of 1.2V, an output voltage of 2.5V with an efficiency of 86% for a 30mA load current is presented for an operating frequency of 800 kHz. This existing solution achieves a high efficiency due to its proposal to tackle power loss due to gate switching, however the passive components of sizes 1µH and 10µF used are implemented as external components.

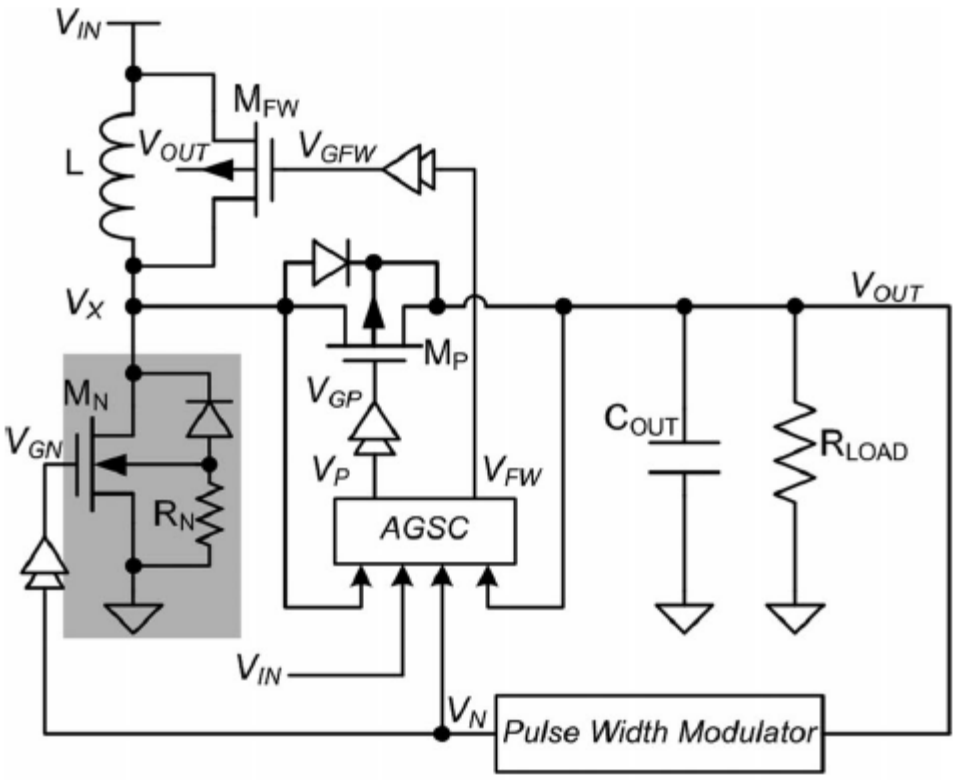


Figure 3.1 Schematic of the boost DC to DC converter proposed in [19] that employs adaptive gate switching controller to minimize gate switching losses

Next, a conventional DC to DC boost converter is proposed in [20] that utilizes a current-mode controller for the switching. This proposed current-mode boost converter employs a loop gain analysis in order to make the converter suitable for 'portable device applications as a driver' [20]. Using TSMC 0.25-µm 1P3M 5V model CMOS technology, an output voltage of 36V with an efficiency of 89% for an input of 4.3V at 1 MHz is presented for a 100mA current load. Figure 3.2 shows the boost DC-DC converter proposed in [29] with the current-mode controller. The reason for a high boost in voltage has been obtained by using a high duty cycle of 87%. Furthermore, large inductor of size 22µH with an internal resistance of only 50mΩ and a large capacitor of size 2.2µF with an internal resistance of only 30mΩ give this proposed converter the high efficiency it has presented.

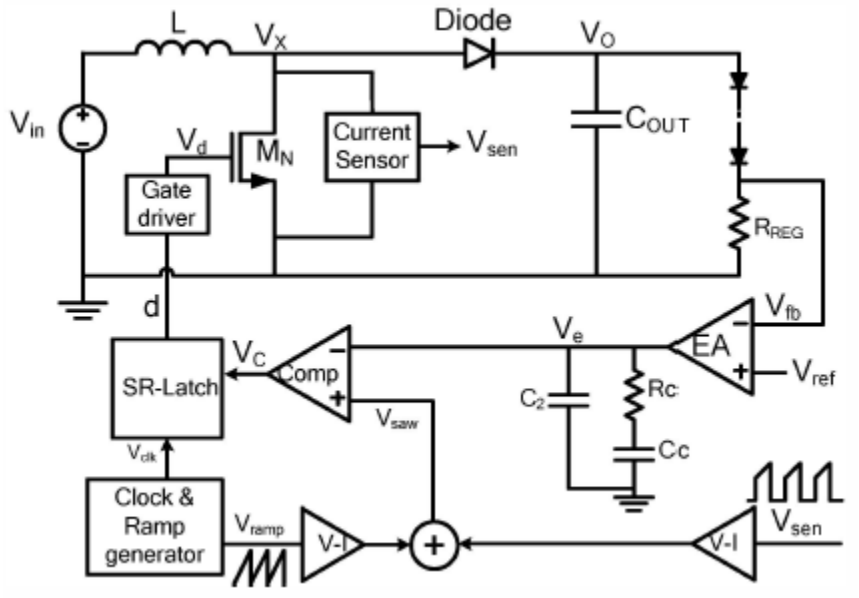


Figure 3.2 Schematic of the current-mode boost DC-DC converter proposed in [20]

Reference [21] proposes a fully-integrated switch-capacitor boost DC to DC converter that uses a switching scheme called non-overlapping rotational time-interleaving (NORI) which essentially helps reduce the dead times between successive charging and discharging phases of the converter [21]. This proposed converter has been fabricated on-chip using the 0.18-µm CMOS thick gate technology. For an input of 3.3V, an output of 5.5V with an efficiency of 83.5% for a current load of 15mA is presented for an operating frequency of 80 MHz. This proposed switch-capacitor boost converter uses an on-chip capacitor of size 440pF, but requires 11 stages of cross-coupled voltage doublers used as a part of the NORI scheme to achieve high efficiencies.

Theoretically, boost DC to DC converters rely on the duty cycle of the control signals applied to the transistor switches in order to achieve different levels of high voltage gains [19]. Practically, electrical features such as the equivalent series resistances of inductors and capacitors, performance of the transistor switches and the rectifier diodes also play heavy roles in determining the ability of a DC to DC converter to achieve high stepped up voltage levels.

Next, there have been fully-integrated DC to DC converters proposed in literature but they are usually buck converters, where a higher DC voltage reduced to a lower DC voltage. Reference [22] proposes an on-chip switched capacitor converter with high power density and high efficiency due to the availability of 'high capacitance density deep trench capacitors' with low parasitic bottom plate capacitor ratio [22]. This proposed converter, shown in Figure 3.3, employs two switched-capacitor power stages to enable the charge recycling circuit. With two stages, the input current ripple is reduced by two since both the switching phases draw current from the input supply. The converter is implemented using the 32-nm SOI CMOS technology, and due to the low transistor breakdown value of approximately 0.9V, stacking is used for the transistors in the gate driver to generate the clock signals for the two switching phases. For an input voltage of 1.8V, an output voltage of 0.836V at 15.6mW output power with an efficiency of 86% is presented. This 2:1 voltage conversion ratio fully-integrated converter comprises of a total on-chip capacitance of approximately 690pF, for an operating frequency of 100 MHz.

Another fully-integrated on-chip DC to DC converter is proposed in [23] that down-converts an input voltage of 1.2V to a maximum output voltage of 0.88V with an efficiency of 74.5% at an operating frequency of 300 MHz. Furthermore, this converter supplies power over a 450X output power range from 0.6mW to 266mW. Moreover, this converter is implemented using IBM 130-nm CMOS technology and it uses the technique of adaptively switching between two different modes of operation by detecting the output current in order to achieve high efficiency.

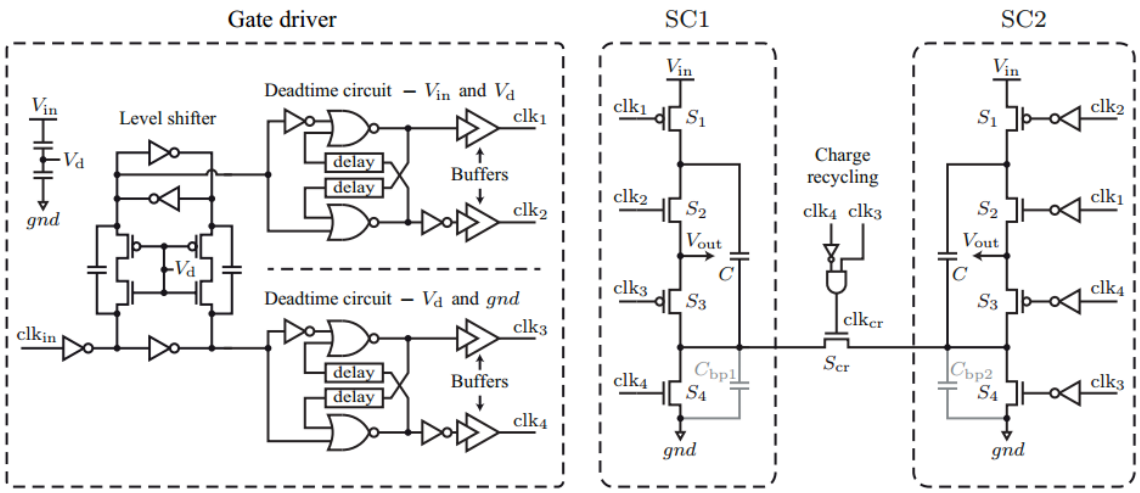


Figure 3.3 Schematic of the 2:1 voltage ratio down-conversion on-chip switched-capacitor converter proposed in [22]

3.3 Charge Pump Converters

3.3.1 Literature Review

A charge pump (CP) is an electronic circuit that generates an output DC voltage that is several times higher than the input DC voltage. In order words, a CP is a DC to DC converter that employs capacitors instead of inductors, which are used in the conventional DC to DC converters, in addition to switches to achieve boosted voltage levels. Dickson CP was the very first and fundamental CP to be implemented with the aim of achieving higher voltages from smaller voltages [24]. Detailed theoretical analysis and simulation results on Dickson CP will be presented.

Cross-coupled CPs have been designed with the intention of being used as voltage doublers [25-26]. They essentially are voltage doublers consisting of two CPs connected in parallel designed to give high efficiencies. Figure 3.4 depicts the schematic of a cross-coupled CP implemented in [26]. It comprises of four NMOS transistors (M1L, M1R, M4L and M4R), four PMOS transistors (M2L, M2R, M3L and M3R) and three large capacitors, where M3L, M3R, M4L and M4R are driven by two sets of non-overlapping clocks with complementary phases. Nodes A and B drive the rest of the four transistors, and the voltages at nodes A and B swing between the supply voltage (V_{DD}) and twice the

supply voltage ($2V_{DD}$) alternately and charge the load capacitor C_L to $2V_{DD}$. Thus, in steady state, the output voltage at the load is twice that of the supply voltage.

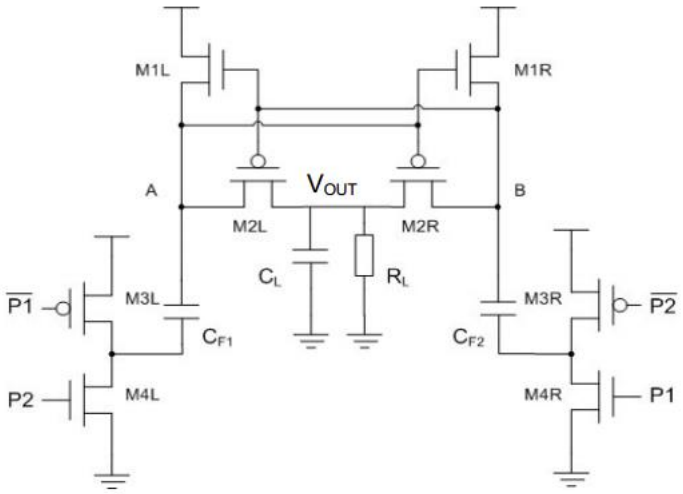


Figure 3.4 Schematic of the cross-coupled charge pump designed in [26]

There are four key design challenges to be considered when designing a cross-coupled CP: (i) sizes of transistors - to make sure the transistors operate in saturation region and provide high efficiency, (ii) switching frequency – to ensure that the right charging time is given for the load capacitor, (iii) the load and pumping capacitors – to ensure that the nodes A and B can reach up to $2V_{DD}$, and (iv) dead time of non-overlapping of driving clocks – to prevent shoot-through current that would be present if the clocks overlapped [26]. Furthermore, to generate four times the supply voltage cascading two cross-coupled CPs would lead to twice the power consumption and double the area-consuming pumping capacitors, in addition to the large area occupied by large transistor sizes required for low on-resistances in order to achieve high efficiency. Area-efficient CPs have been proposed to reduce the number of components required by two cascaded cross-coupled voltage doublers in order to get four times the boost voltage [26], as shown in Figure 3.5. Transistors M1 and M2 along with pumping capacitors C1 and C2 function as the standard cross-coupled voltage doubler. Next, when clock 1 (ϕ1) goes high, node B charges C3 to $2V_{DD}$, and when clock 2 (ϕ2) goes high, node A charges the lower plate of C3 to $2V_{DD}$, pushing the voltage at the upper plate of C3 to $4V_{DD}$ [27].

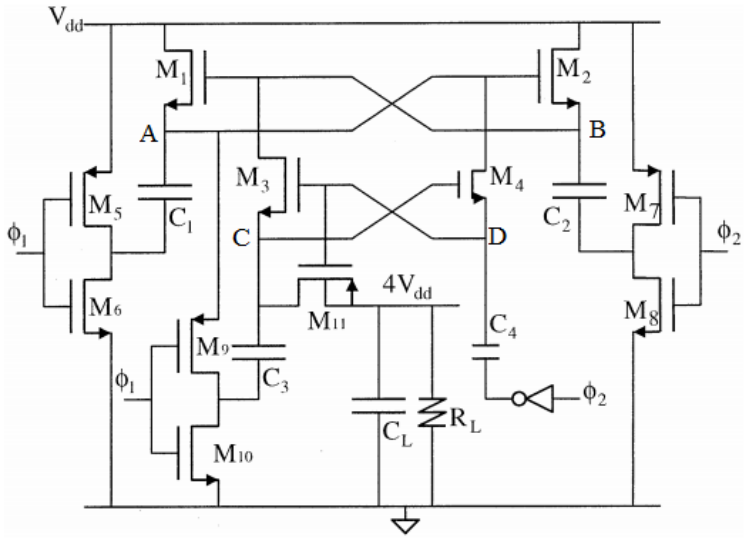


Figure 3.5 Schematic of a modified four-times cross-coupled CP proposed in [27]

One potential problem for the CP proposed in [27] was that there is a potential path for current to flow from the output of $4V_{DD}$ to supply of V_{DD} through M4 and M1. The solution proposed to avoid current shortage was to have a threshold voltage for M4 greater than the supply voltage of V_{DD}. This poses a hindrance to technologies that do not have high V_{th} transistors, especially for the Peregrine UltraCMOS technology that prides in carrying low V_{th} transistors with one variation having almost no V_{th}.

One reason why a lot of research has been done in the field of CPs on top of the Dickson CP is the voltage and efficiency loss incurred due to the diodes used in the architecture of Dickson CP [27]. Modifications to the Dickson CP led to the design of a structure known as charge-transfer switch (CTS), which essentially consists of the use of auxiliary transistors parallel to each diode (essentially diode-connected transistor) in the Dickson CP chain so that the feedback of high voltage from the next node counters the V_{th} loss incurred in the diodes [28], as shown in Figure 3.6. The auxiliary transistor uses the higher voltage from the next node (n+1) to charge the pumping capacitor at the previous node (n) while the node preceding it (n-1) is pumping.

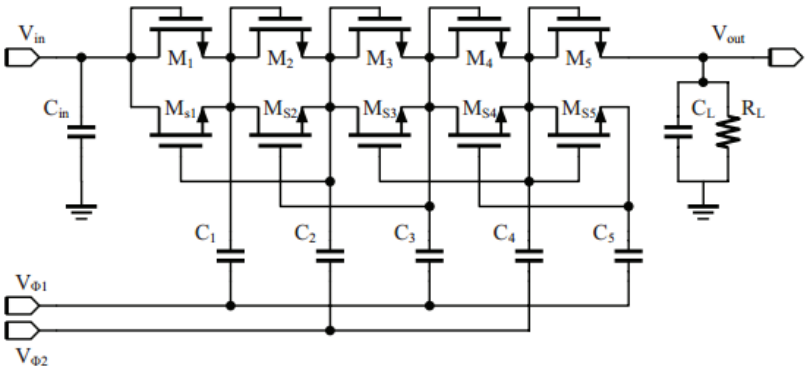


Figure 3.6 Schematic showing CTS CP, which is a Dickson CP with diodes modified to prevent voltage and efficiency loss due to V_{th} drop in the diodes

One practical disadvantage with the CTS architecture is the presence of unwanted reverse charge sharing that occurs due to the auxiliary transistor continuing to stay in its on-state while the node n is pumping, leading to a reverse loss of voltage from node n to the capacitor at node n-1 [29].

Research done to minimize the overall voltage losses within and at the output stage of the Dickson CP are presented in [28-29]. First, in order to minimize the reverse charge from occurring, [28-30] propose the use of control voltages at the gates of the auxiliary switches so that they can be turned on and off with respect to the appropriate functioning of the CP.

Another problem the standard Dickson CP and the CTS method suffer from is the additional voltage drop due to the V_{th} of the diode-connected transistor at the output stage. [29] and [30] propose the implementation of variations of the cross-coupled CP in place of the lone output diode-connected transistor to solve the voltage loss due to V_{th}. Figure 3.7 depicts the circuit schematic with modifications done to the traditional Dickson CP, which include the CTS technique, voltage control at the gates of auxiliary transistors and a cross-coupled CP to prevent V_{th} drop [29].

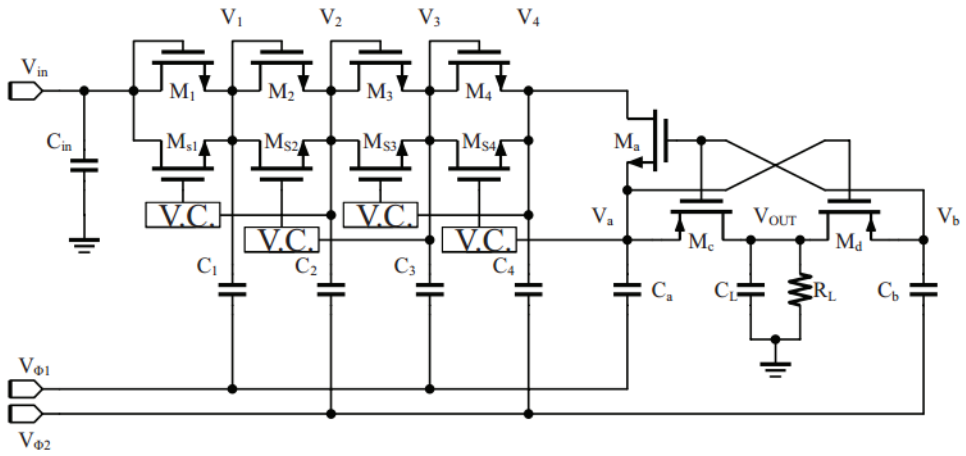
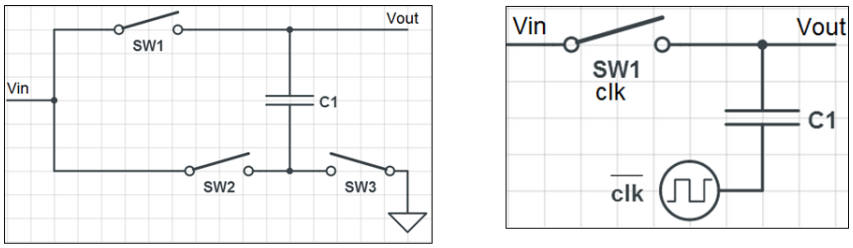


Figure 3.7 Circuit schematic of changes applied to the standard Dickson CP, which include the CTS technique, voltage control at the gates of auxiliary transistors and a cross-coupled CP to prevent V_{th} drop [29]

3.3.2 Implemented Dickson Charge Pump Converter

Dickson CP is implemented and simulated in the UltraCMOS technology. The presence of 'zero-V_{th}' transistors in the UltraCMOS technology eliminates the use of the CTS technique to recover voltage that is lost through transistor threshold voltage drops for a traditional Dickson CP. Furthermore, the fact that every one additional stage theoretically increases the output voltage by input voltage gives the freedom to design the Dickson CP for the desired output voltage.

The fundamental concept behind the Dickson CP is based on charging and discharging of the pumping capacitors. Figure 3.8(a) depicts the design of the generic charge pump.



(a) (b)

Figure 3.8 Illustrations of the schematic of (a) the generic charge pump and (b) its equivalent circuit with clock signal

When switches SW1 and SW3 are closed and SW2 is open, the pumping capacitor C1 charges up:

$$V_C = V_{in} \tag{3.3}$$

where V_C is the voltage across the C1.

When SW2 is closed and SW1 and SW3 are open, the bottom plate of C1 is charged to V_{in} and the result obtained is:

$$(V_{out} - V_{in}) \times C1 = V_{in} \times C1 \tag{3.4}$$

$$\Rightarrow \therefore V_{out} = 2V_{in} \tag{3.5}$$

Ideally, one stage of the generic CP can double the input voltage. Figure 3.8(b) shows the equivalent CP design that uses a square-wave/clock signal in place of SW2 and SW3.

The Dickson CP usually has an output capacitor (C_{out}) and a load (R_L). The ideal output voltage then becomes a result of the voltage division between the two capacitors:

$$V_{out} = \frac{C}{C + C_{out}} \times 2V_{in} \tag{3.6}$$

while C_{out} also reduces the ripple voltage that is present due to R_L.

In order to have higher output voltages, the Dickson CP can be extended to have a cascade of multiple stages, where ideally each stage increases the output voltage by the original input voltage. Figure 3.9 shows the circuit design of a Dickson CP with four stages. Considering N to be the number of stages, V_d to be the voltage drop across each diode and $V_\emptyset$ to be the on-voltage level of the clocks being applied, the ideal output voltage (V_{out}) can be formulated as:

$$V_{out} = V_{in} + N \times (V_\emptyset - V_d) - V_d \tag{3.7}$$

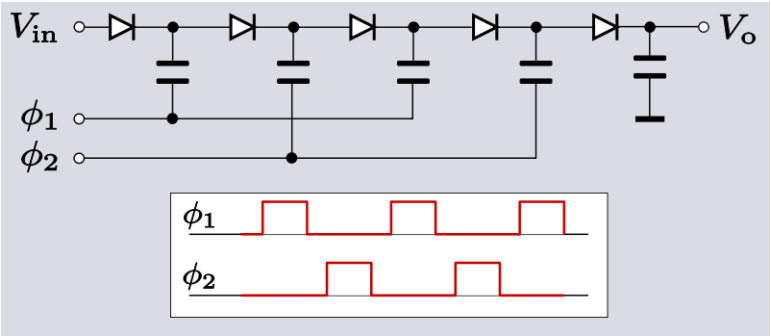


Figure 3.9 Schematic of the ideal Dickson CP along with the non-overlapping clock signals [31]

Further detailed study on the Dickson CP [32] reveals a more accurate equation for the output voltage taking into consideration the parasitic capacitances (C_s) associated with every stage:

$$V_{out} = V_{in} + N \times \left(\frac{C}{C + C_s} \times V_\emptyset - V_d\right) - V_d \tag{3.8}$$

Finally, considering the output load R_L [32] with the output current as $I_{out} = \frac{V_{out}}{R_L}$, the output voltage can be further written as:

$$V_{out} = V_{in} + N \times \left(\frac{C}{C + C_s} \times V_{\emptyset} - V_d - \frac{I_{out}}{(C + C_s) \times f} \right) - V_d \tag{3.9}$$

where f is the switching frequency of the CP and essentially $V_{\emptyset} = V_{in} = V_{dd}$.

Implementing a Dickson CP using the Peregrine UltraCMOS technology seemed feasible primarily due to the availability of 'zero-threshold' transistors, which would address the main issue of voltage drops due to V_{th} across the diode-connected transistors in the Dickson CP architecture. Furthermore, there should be no need to use the CTS modification to the Dickson CP, again, because of the presence of 'zero-V_{th}' transistors in UltraCMOS technology.

Figure 3.10 depicts the circuit simulated using the Peregrine UltraCMOS technology, using the 'zero-V_{th}' transistors for the nine diode-connected transistors. The top half of Figure 3.10 consists of an inverter chain designed to generate the two clocking signals for the Dickson CP. With the desired frequency of operation being 1 GHz, it is very difficult to generate square-waves using external signal generators at such high frequency. So a sinusoidal signal at RF frequency of 1 GHz is applied to a chain of inverters which have a supply voltage, or V_{DD}, of the on-voltage of the clock signals. L1 and C1 form a 'bias-T', which is an external RF measurement component that helps in adjusting the duty cycle of the generated square-wave clock signals via a bias DC voltage. The generated clock signals are then used as alternately charge and discharge the pumping capacitors in the Dickson CP circuit.

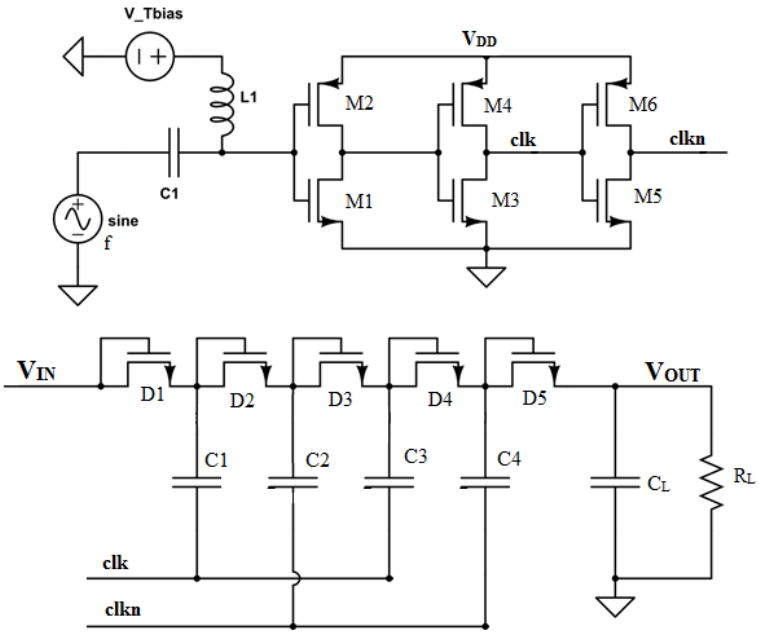


Figure 3.10 Schematic of 4-stage Dickson CP implemented in UltraCMOS technology; the circuit of inverters used to simulate 'on-chip' clock signals is also shown above the Dickson CP

For a four-stage Dickson CP, Eq. 3.9 calculates the output voltage (V_{out}) to be 8.4V. Simulating the four-stage implemented Dickson CP in UltraCMOS technology, as shown in Figure 3.10, with an input voltage (V_{in}) of 3V (and $V_{DD} = V_{in}$), a V_{out} of 7.8V with a very low power efficiency of approximately 20% is obtained. The results obtained are as follows: $V_{out,avg} = 7.8V$, $I_{out,avg} = 155mA$, and $P_{out,avg} = 1.21W$.

Following are the main factors that led to such low efficiency and V_{out} results:

(i) The ideal efficiency of the Dickson CP is calculated as follows:

$$\eta = \frac{V_{out} \times I_{out}}{V_{in} \times I_{consumed}} \tag{3.10}$$

where η is the efficiency and $I_{consumed}$ is the total current consumed by the CP and is given in [32] as:

$$I_{consumed} = (N + 1) \times I_{out} \tag{3.11}$$

With the desired set of parameters, the ideal power efficiency obtained with the Dickson CP using Eqs. (3.10) and (3.11) is *55%*. The reason for this is that the pumping capacitors essential waste half of the current they pump during one of the half cycles in one period. So no matter what is done, the best achievable power efficiency for the given parameters would be *55%* only.

(ii) There is a strict requirement that the two clock signals used by the pumping capacitors need to be non-overlapping. Generating non-overlapping square-waves at 1 GHz is very challenging especially if the entire design needs to be on-chip. As a result, the two non-overlapping square-waves obtained from the chain of inverters contributed to the low efficiency and V_{out} to an extent.

(iii) Since the target was to have the entire design to implemented on-chip, there was a need for relatively smaller than required pumping capacitor sizes. However, the higher the pumping capacitors, the faster and higher they charge at every stage. As a result, capacitors as large as 200pF were used in the design as trade-off between large capacitors which would barely fit the design area criteria.

The chain of inverters that generated the clock signals now had a very large capacitive load. This resulted in imperfect square-wave being generated and the best attempt to generate as perfect square-waves as possible by using strong inverters led to the inverter chain consuming a power of approximately 3.6W. This huge power consumption contributed to approximately 30% efficiency loss in the overall power efficiency of the simulated Dickson CP.

To summarize, the pros of implementing a Dickson CP are

- Theoretically, each additional stage increase V_{out} by V_{in}
- There is no need for stacking of transistors as the voltage increment in each stage is well within the drain to source breakdown voltage swing

while its cons of implementing it in UltraCMOS are

- Large pumping capacitors; on-chip implementation is very restricted
- Non-overlapping square-wave clock signals

- Power inefficient; as each stage wastes current while charging and discharging of its pumping capacitor

3.4 AC to DC Converter

Various alternating current (AC) to DC converters have been proposed in literature that utilize a full-bridge wave rectifier to convert an AC input signal to a boosted output DC voltage [33-35]. Most of the research for full-bridge AC to DC converters has been done for relatively lower frequencies (≤100 kHz) and higher voltage levels (≥ 40V).

Since the UltraCMOS transistors are fast enough to be used as diodes (diode-connected transistors), the idea of generating output DC voltages from an AC voltage seemed plausible with this technology at higher frequencies. Figure 3.11 shows the schematic of the AC to DC converter attempted using the UltraCMOS technology.

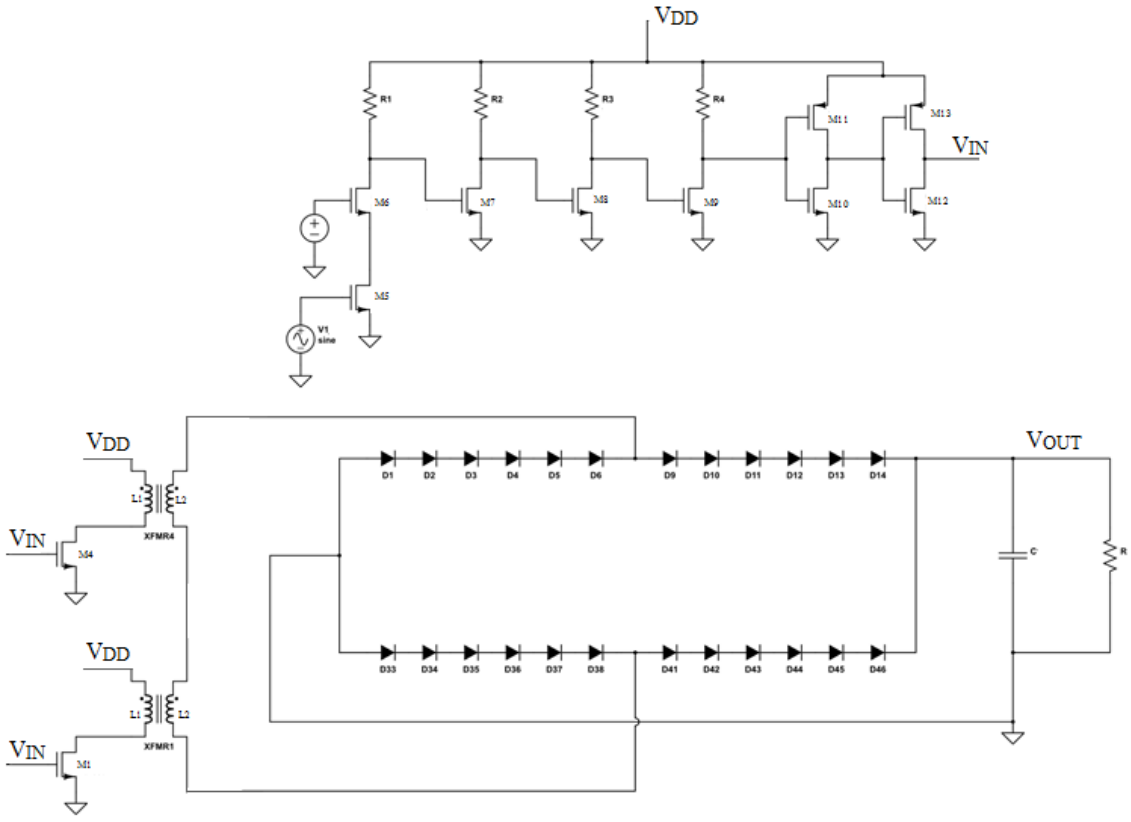


Figure 3.11 Schematic of the AC to DC converter implemented using the UltraCMOS technology

The idea behind the circuit was to use a series output combination of two transformers, with their inputs being switched individually using two similar switches having the same input square-wave signal and bias voltage. In order to generate the switching signal for the two switches, an AC signal with low power, meaning small amplitude, is amplified by using a cascade of a cascode and three CS amplifiers – with small sized transistors – in order to complete the amplification in stages by having these amplifiers consume relatively low power, and this slightly amplified AC signal is then passed through a chain of two inverters to get a square-wave-like output.

The amplified AC signal from the output of the two series-connected transformers is then passed through a full-bridge wave rectifier, which essentially converts an AC signal with a peak voltage of V_{pk} to a DC voltage equaling V_{pk} in an ideal case.

Following are the component sizes used in designing and simulating the AC to DC converter and the results achieved:

- Sizes of transistors used in the driver stage to generate a square-wave = 100's μm (except for CS stage in the cascode = 10 mm)
- Size of transistors used as switches = 20 mm
- Size of diode-connected transistors used in the full-bridge wave rectifier = 20 mm
- Load resistors in the amplifying stages = 1000's Ω
- Transformer ratio = 1.8 nH:7.2 nH (1:4)
- Output capacitor = 1 nF
- Output load = 50 Ω
- Switching frequency = 200 MHz
  - Average Output DC voltage = 8.5 V
  - Average Output current = 170 mA
  - Average Output power = 1.45 W
  - Input power = -10 dBm
  - Average power consumed by the driver (amplifying) stages = 60 mW
  - Average power consumed by the transformers = 4.2 W

- Efficiency (ratio of output power to total power consumed) = 30 %

The output voltage and output power achieved are well within the targeted values. However, an efficiency of 30% greatly lowers the attractiveness of the desired output voltage. As such, the attempted AC to DC converter does achieve the desired voltage levels, but performs poorly in terms of the efficiency obtained primarily due to the high power consumed within the circuit. The drain voltages at the two switching transistors observe oscillations with peak voltages of greater than 2.5V, and this could be due to the inductive loading of the transformers, in addition to influence from the parasitic capacitances of the transistors. A brief summary of the pros and cons of this implementation is presented below:

- Pros:
  - Very small input AC signal → -10dBm
  - Driver stage transistors relatively small → 100's μm, except for 1st input transistor → 10 mm
- Cons:
  - Large output Capacitance (≈ 1nF)
  - Bridge Full-wave Rectifier requires 4 x 6 = 24 diode-connected transistors, each 20 mm wide, in order to maintain a drain to source voltage of 2.5 V across each transistor (necessary for UltraCMOS technology)
  - Large transformers with large turns ratio transformers (1:4) with primary inductance, which consume a lot of power and reduce efficiency greatly

3.5 Conventional Boost DC to DC Converter

3.5.1 Theoretical Analysis

The generic boost DC to DC converter is based on the principle of switching and studies have shown that switching power supplies generally have higher efficiencies [36]. In transformerless DC to DC converters, inductor is the only magnetic component present [37]. The single inductor in the conventional boost DC to DC converter is used as a

means of energy storage and discharges during the on and off stages, respectively. Figure 3.12 shows the schematic for a conventional, ideal, boost DC to DC converter.

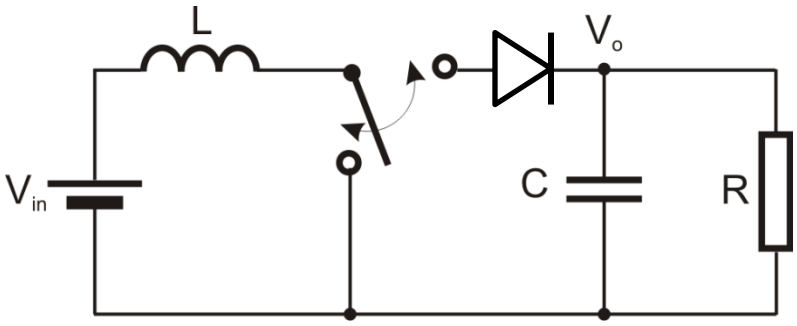


Figure 3.12 Schematic of the ideal conventional boost DC-DC converter

There are essentially two phases for the working of the circuit as illustrated in Figure 3.13.

- Charging Phase

a) Initially, it is assumed that the switch has been open for a long time, and the output voltage V_{OUT} equals the input voltage V_{IN}:

$$V_{OUT} = V_{IN} \tag{3.12}$$

b) When the switch turns on, or closes as depicted in Figure 3.13(a), the current across the inductor ramps up linearly (3.13) due to the V_{IN} and charges the inductor to a voltage V_L

$$\Delta I_{ON} = \frac{V_{IN} \times t_{ON}}{L} \tag{3.13}$$

where t_{ON} is the amount of time the switch is in the on state and L is the inductor.

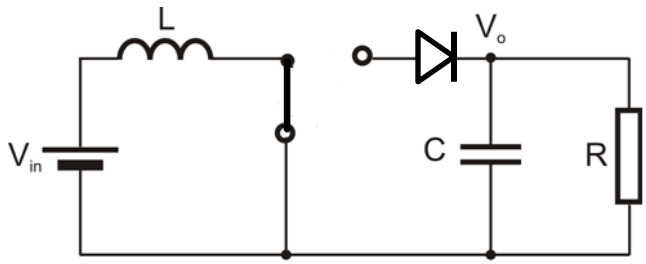
- Discharge Phase
  a) When the switch turns off, or opens as depicted in Figure 3.13(b), the polarity of the stored charge in the inductor changes and adds onto V_{IN}
  b) Now V_L and V_{IN} are in series and add up to have $V_{OUT} > V_{IN}$:

$$V_{OUT} = V_{IN} + V_L \tag{3.14}$$

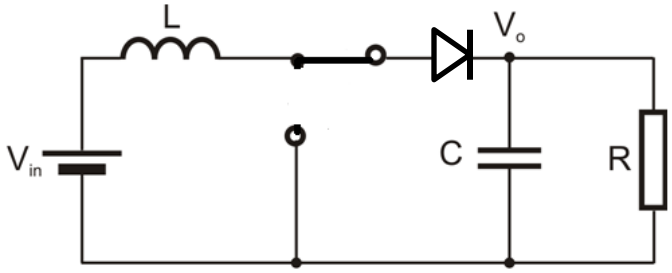
  c) As V_{OUT} increases, the change in current across the inductor decreases:

$$\Delta I_{OFF} = \frac{V_L \times t_{OFF}}{L} \tag{3.15}$$

where t_{OFF} is the amount of time the switch is in the off state.



(a)



(b)

Figure 3.13 The two phases, charge and discharge, of the conventional boost DC to DC converter

In steady state, the current increment (ΔI_{ON}) across the inductor must be equal to the current decrement (ΔI_{OFF}) in order to be able to continue a repetition of the charge and discharge cycles [38]. So the total current across the inductor during the charge phase must equal the current across the inductor in the discharge phase as:

$$V_{IN} \times t_{ON} = V_L \times t_{OFF} \tag{3.16}$$

which gives us:

$$V_L = V_{IN} \times \frac{t_{ON}}{t_{OFF}} \tag{3.17}$$

By substituting Eq. 3.17 in Eq. 3.14, the equation for the final ideal output voltage in terms of the input voltage and the switching times can be obtained as follows:

$$V_{OUT} = V_{IN} + V_{IN} \times \frac{t_{ON}}{t_{OFF}} \tag{3.18}$$

$$V_{OUT} = V_{IN} \times \frac{t_{ON} + t_{OFF}}{t_{OFF}} \tag{3.19}$$

Formulating the fraction of switching times in terms of duty cycle D gives us:

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} \tag{3.20}$$

Finally, using Eqs. 3.19 and 3.20, the equation for the final theoretically ideal output voltage in terms of the input voltage and duty cycle can be obtained as follows:

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \tag{3.21}$$

$$\therefore V_{OUT} = V_{IN} \times \frac{1}{1-D} \tag{3.22}$$

Thus in boost DC to DC converters it can be seen that the output voltage increases with increasing duty cycle, as Eq. 3.22 confirms. However, the output voltage is typically less than what Eq. 3.22 ideally presents primarily because of voltage drops in practical circuits occurring from the switching transistor and the diode. Considering V_D to be the voltage drop across the diode and V_{Sw} to be the voltage loss due to the switch, a more practical relation between the output voltage, input voltage and the duty cycle can be formulated as follows:

$$\frac{(V_{IN} - V_{Sw}) \times t_{ON}}{L} = \frac{(V_L + V_D) \times t_{OFF}}{L} \tag{3.23}$$

$$\frac{(V_{IN} - V_{Sw}) \times t_{ON}}{L} = \frac{(V_{OUT} - V_{IN} + V_D) \times t_{OFF}}{L} \tag{3.24}$$

$$V_{IN} - V_{Sw} \times D = (V_{OUT} + V_D) \times (1 - D) \tag{3.25}$$

$$\therefore V_{OUT} = \frac{V_{IN} - (V_{Sw} \times D)}{1-D} - V_D \tag{3.26}$$

The ideal waveforms of the switch input and current and voltage across the inductor during one time period (T) are illustrated in Figure 3.14. The inductor current shown in Figure 3.14 goes back to its minimum point at the start of every period. While there are some control techniques to have this minimum current value to be greater than zero amperes, boost DC to DC converters typically operate in a discontinuous conduction mode (DCM) where the minimum inductor current decreases down to zero amperes at the end of every period [38].

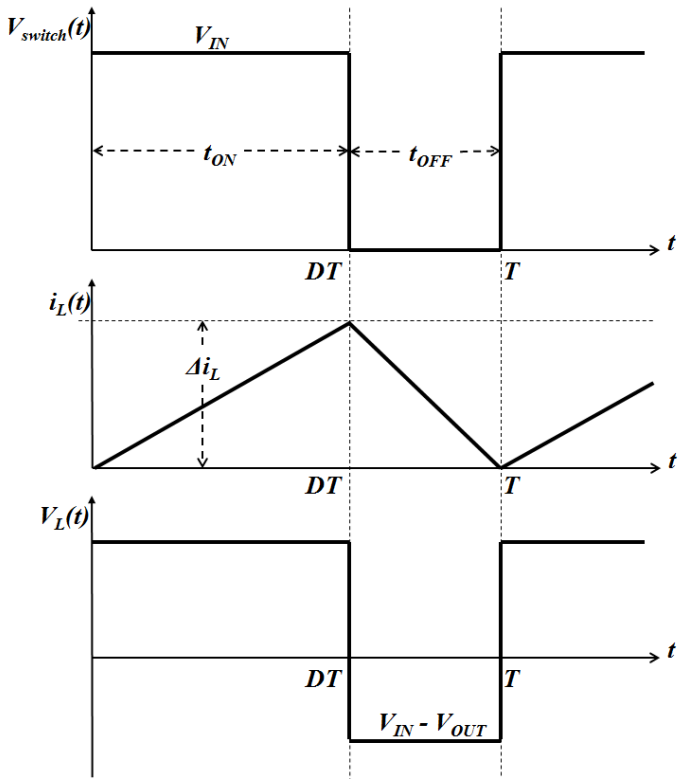


Figure 3.14 Ideal inductor current and voltage waveforms for a known input switch waveform for the boost DC to DC converter

For most applications that use DC to DC converters, the input voltage, output voltage and output current (or load) are dictated by the designs requirements and limitations. The inductor, along with the its ripple current, is one free parameter that needs to be chosen wisely depending on the acceptable ripple current, both by the inductor itself and the design requirement. Furthermore, the smaller the equivalent series resistance (ESR) of the inductor, higher the efficiency and output voltage are achieved [36]. For boost DC to DC converter, the inductor is chosen based on the maximum input ripple current that is acceptable. Considering the voltage drops stated in Eq. 3.24, a basic equation for the inductor value can be formulated as:

$$L = \frac{(V_{OUT} - V_{IN} + V_D) \times (1 - D)}{\Delta I_L} \tag{3.27}$$

As for the output capacitor, the primary criterion for selection is to meet the required output voltage ripple for the boost DC to DC converter design. Using the well-known equation for the current across a capacitor

$$i = C\frac{\Delta v}{\Delta t} \tag{3.28}$$

we can come to a rather general equation for the output capacitor as:

$$C = \frac{I_{OUT} \times (1 - D)}{\Delta v_{OUT}} \tag{3.29}$$

where Δv_{OUT} is the output ripple voltage that can be calculated to values with the range of approximately ±20% of output voltage.

The next important component of the boost DC to DC converter to consider is the diode. The diode's primary functions are to block any current crossing over to the output when the switch is in its on state and to allow current and voltage to pass over to the load when the switch is in its off state. The other important features the diode should have are low forward voltage drop to reduce voltage loss at output, and fast switching characteristics to be able to switch 'on' and 'off' depending on the switch's transitions.

Next, implementing an actual boost DC to DC converter requires some modifications to the conventional converter in terms of using practical and non-ideal components. For an implementation in CMOS technology, a power transistor is used in place of an ideal switch and a diode-connected transistor is used in place of the diode. Not all CMOS transistors can be used as diodes due to their lack of high switching speeds. A schottky diode is an ideal replacement for the diode in the boost converter.

In this thesis, the UltraCMOS SOS technology is used and its higher speeds and lower junction capacitances aid in utilizing its transistors as diodes. However, as mentioned earlier in chapter 1, the transistors by Peregrine Semiconductor that are made of CMOS SOS have drain to source breakdown voltage of slightly higher than 2.5V, thus the drain to source voltage swing across each transistors should be limited to about 2.5V.

In order to be able to have large swing across the switch in the boost converter, transistor stacking is commonly utilized to additively achieve the required voltage swing. With the Peregrine UltraCMOS technology, the diode-connected transistors can be stacked in series to equally distribute the total voltage swing across the diode in the boost converter. However, simply stacking transistors for switching is not the right approach as biasing comes in play with these transistors. Thus, in order to account for the voltage swing limitation, the stacking approaches discussed in chapter 2 could be used in place of a single power transistor.

3.5.2 Proposed Conventional Boost DC to DC Converters

In order to characterize the performance that could be achieved by using the UltraCMOS process for the boost DC to DC converter, an ‘ideal’ design is simulated with UltraCMOS transistors for the switch and the diode, ideal switch gate control and non-ideal input inductor, as shown in Figure 3.15.

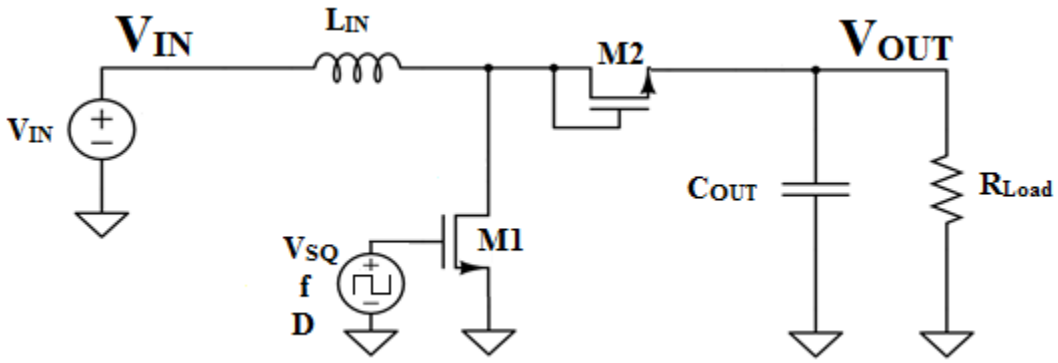


Figure 3.15 'Ideal' implementation of the boost DC to DC converter using Peregrine UltraCMOS transistors (disregarding the drain to source voltage breakdown limit) and non-ideal inductor

For an input of V_{IN} = 3V, output load of R_{Load} = 50Ω and a quality factor Q of 30 for the input inductor, table 3.1 shows the achieved output voltages (V_{OUT}) and efficiencies (η) – ratio of output power to total power consumed within the circuit – for a few varying input inductances (L_{IN}) and output capacitances (C_{OUT}) that can be implemented on-chip.

Table 3-1 Simulation results of the 'ideal' boost DC to DC converter using UltraCMOS technology for varying on-chip input inductances and output capacitances

L_{IN} (nH)	1.5	2.5	3.5	1.5	2.5	3.5
C_{OUT} (pF)	200			500		
V_{OUT} (V)	7.3	5.4	5.35	7.3	5.5	5.38
η (%)	76.65	78.35	76.5	70.6	72.88	71.07

Ideally, the efficiency of a boost DC to DC converter would be 100% and the output voltage would depend on the input inductance being used. An analysis of the drop in

efficiencies obtained in the simulation results depicted in table 3.1 concludes that there is power being internally consumed by the various components present in the circuit. Table 3.2 outlines the power being consumed by the various components in the circuit shown in Figure 3.15.

Table 3-2 Power consumptions internal to the boost DC to DC converter circuit that are contributing to the loss in ideal efficiency

Parameters	**L_{IN} (nH)**	1.5	2.5	3.5	1.5	2.5	3.5
	C_{OUT} (pF)	200			500		
Powers	**P_{IN} (W)**	1.369	0.770	0.750	1.422	0.833	0.807
	P_{OUT} (W)	1.049	0.603	0.574	1.015	0.607	0.574
	P_{Lin} (mW)	65.66	33.84	45.67	70.8	39.66	52.9
	P_{Switch} (mW)	35.91	14.06	19.95	35.32	16.01	20.86
	P_{Diode} (mW)	170	94.34	87	181	109.5	101.4
	P_{Cout} (mW)	5	2.5	2.3	11.9	6	5.8

One thing to note is that for inductor values of approximately less than 3.5nH, the boost DC to DC converter shown in Figure 3.15 operates under the discontinuous conduction mode (DCM). DCM occurs when the inductor discharges completely before the end of a periodic cycle, the current across it goes to zero and it needs that extra bit of push to start charging up again at the start of the next period [39]. The input inductance that pushes the converter to operate in DCM is given in [40] by:

$$L \leq \frac{(1-D)^2 \times D \times R_{Load}}{2 \times f} \tag{3.30}$$

where D is the duty cycle, R_{Load} is the load resistance and f is the switching frequency.

The equation formulated for the output voltage in Eqn. 3.17 is for the case when the converter operates in the continuous conduction mode (CCM). CCM is when the minimum current across the inductor is greater than zero amperes. The characteristics of the converter under DCM change significantly, and the output voltage becomes a function of the output load (R), switching frequency (f), duty cycle (D) and the input inductance (L). The boost DC to DC converter voltage gain in DCM mode is calculated using [39]:

$$G(D,K) = \frac{1+\sqrt{1+\frac{4D^2}{K}}}{2} \tag{3.31}$$

where

$$K = \frac{2fL}{R} \tag{3.32}$$

For L = 1.5nH and R = 50Ω operating at 1 GHz with a 50% duty cycle, Eqns. 3.31 and 3.32 estimate an ideal boost of 2.6 times, which closely represents the simulation result presented in table 3.1. Figure 3.16 shows a graph illustrating the dependence of the voltage gain on duty cycle and the factor K. Figure 3.17 shows the input current, output current and output voltage simulation results for 1.5nH input inductance. The ripple in the output voltage can be further reduced by increasing the output capacitance. Also, the input current plot confirms the DCM operation as the minimum input current. Moreover, note that the current across the input inductor is less than zero amperes.

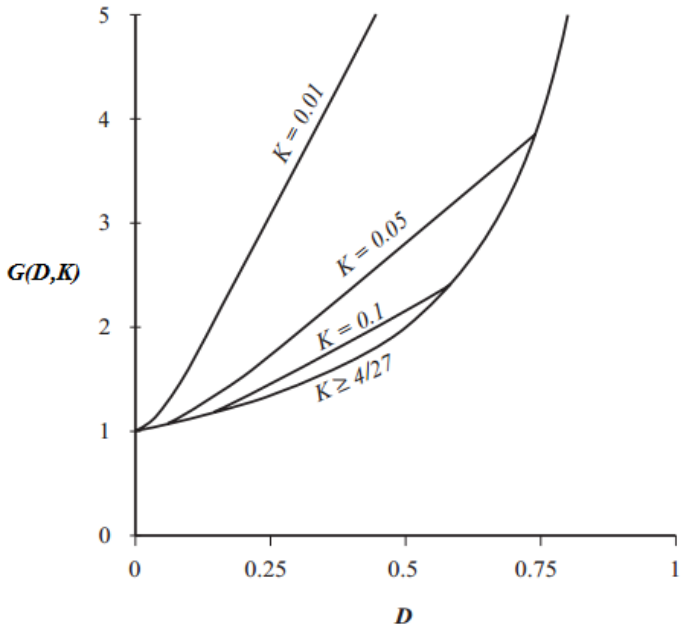


Figure 3.16 Voltage gain versus duty cycle and *K* for DCM operation of the boost DC to DC converter [39]

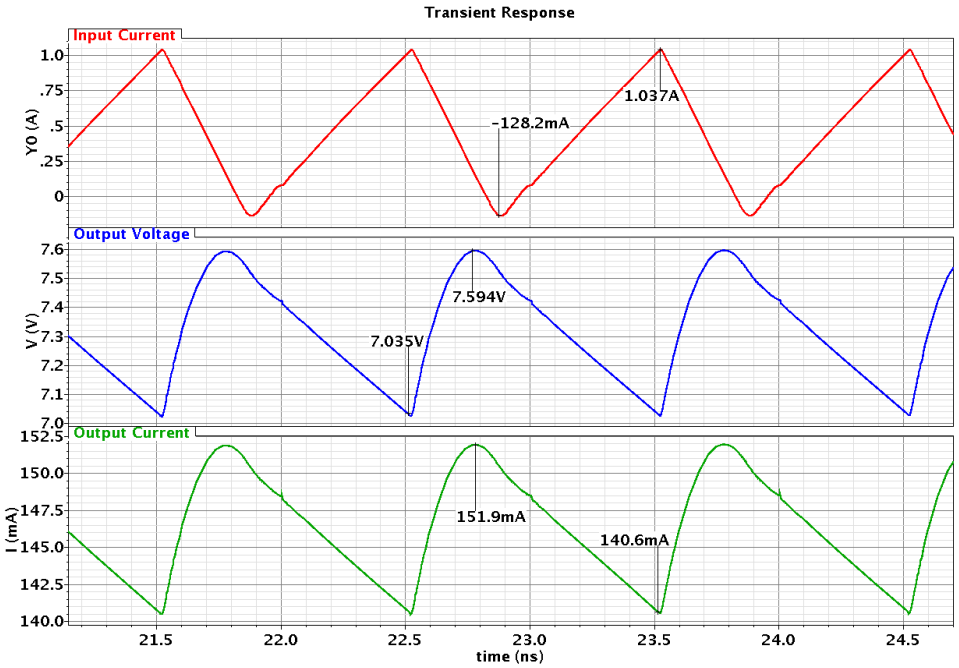


Figure 3.17 Simulation results of the 'ideal' boost DC to DC converter displaying the input current, output current and output voltage for an input inductance of 1.5nH

Furthermore, the simulation results presented in tables 3.1 and 3.2 do not take into consideration the breakdown voltage of the transistors. As a result, modifications are needed in order to account for the drain to source voltage swing limit of 2.5V for the UltraCMOS process. As discussed and presented in chapter 2, stacking is the answer to handle the transistor breakdown voltage. Out of the various stacking techniques discussed, the dynamic self-biasing stacking approach is the better one to use in place of the single transistor switch because this stacking technique makes sure that the gate bias voltage is floating between the drain and source voltages for non-zero threshold voltage transistors. The zero-threshold voltage UltraCMOS transistors turn on as soon as a non-zero gate voltage is applied and thus do not require additional biasing. Moreover, dynamically self-biased stacking approach ensures that the drain to source swing voltage of each transistor is maintained to below 2.5V.

In addition to accounting for the breakdown voltage in the switch transistor, the drain to source voltage swing across the diode-connected transistor also needs to be considered. As mentioned in chapter 2, the diode-connected transistors can be simply stacked in series because the gate of each transistor is biased via their respective drain terminals. Series stacking of diode-connected transistors simply distributes the overall voltage swing equally among each individual diode-connected transistor in the stack.

One evident influence the diode-connected transistors have on the performance of the boost DC to DC converter is that the threshold voltages across each diode-connected transistor lead to decrease in the output voltage. The solution to minimize output voltage loss due to V_{th} is to either use synchronous converter where the diode is replaced by another switch transistor, or employ very low V_{th} transistors. The presence of 'zero-V_{th}' transistors in the UltraCMOS technology makes them the apparent solution for the diode-connected transistors in the converter circuit.

3.5.2.1 Proposal #1 – with Dynamically Self-Biased Common-Source Stacking

Figure 3.18 demonstrates the circuit schematic of the proposed boost DC to DC converter, in Peregrine UltraCMOS technology, which employs a dynamically self-biased common-source (CS) stacking technique to account for the voltage swings limitations across each UltraCMOS transistor. Each stack consists of a CS topology with a transformer at the gate, a gate to drain feedback resistor and some source biasing. The transformers employed for each cell are used to isolate the dependence of one stacked CS cell from another. Furthermore, Figure 3.18 also shows the driver circuit implemented to generate the gate control signal for the switch stack. Since the desired frequency of operation is in the range of 1 GHz, it is difficult to generate square-waves using external signal generators at such high frequencies. As a result, a sinusoidal signal at RF frequency is applied to a chain of inverters that have an external supply voltage. The generator is connected to a 'bias-T', which is an external RF measurement component with 1mH inductance and 1μF capacitance, to help vary the DC bias of the generated

square-wave through an applied DC voltage. The generated signal is then applied to the dynamically self-biased switch stack of the boost DC to DC converter as its gate control.

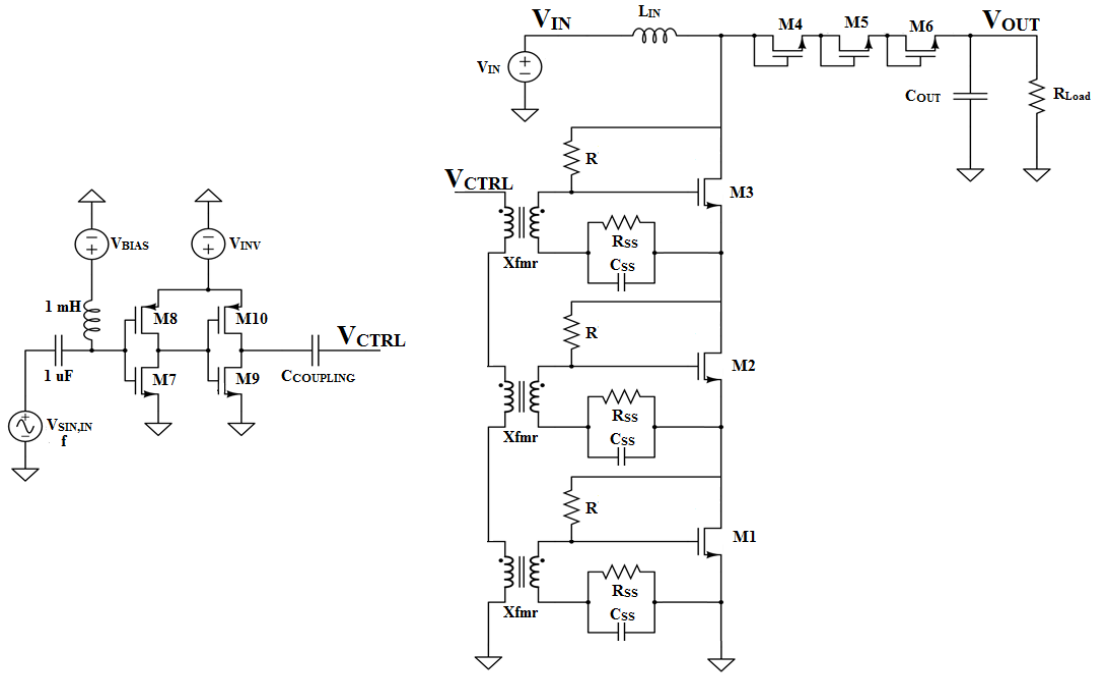
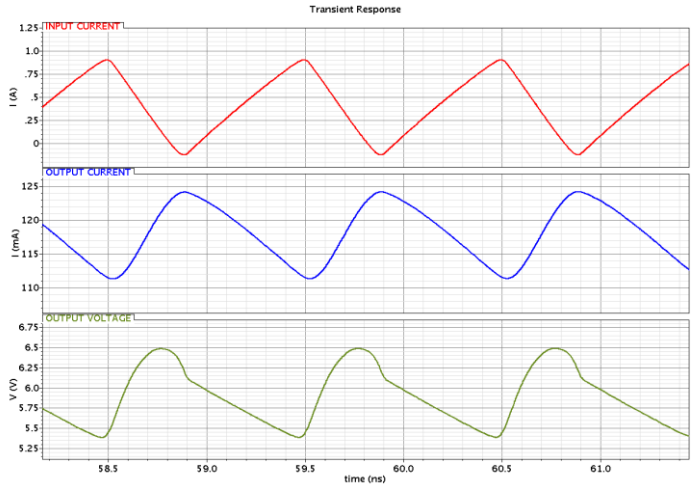
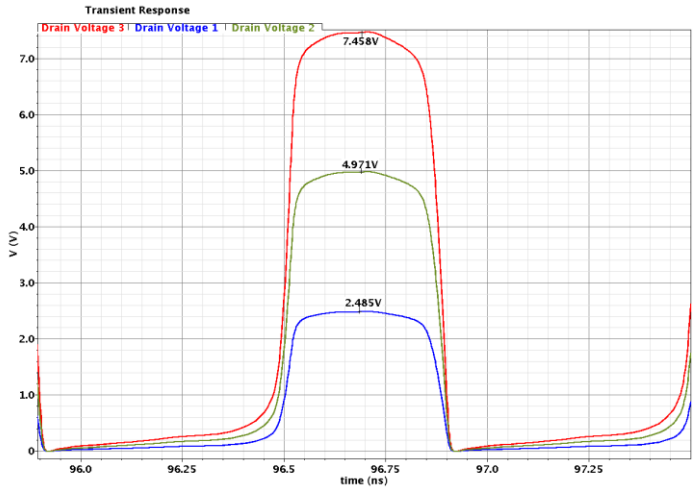


Figure 3.18 Schematic of the proposed boost DC to DC converter in Peregrine UltraCMOS technology with dynamically self-biased common-source stacking approach, in addition to the driver used to generate the gate control signal

After carefully choosing the resistor and capacitor values in the dynamically self-biased CS stack, the appropriate sizes of all the transistors – in terms of performance and layout, the driver supply and bias voltages, the output capacitor and the best available inductor in the UltraCMOS process, an average output voltage of approximately 6V with an efficiency of 50% is achieved for a load of 50Ω. Figure 3.19 shows the simulation results obtained by simulating the circuit shown in Figure 3.18. The output capacitor is primarily responsible for the output voltage ripple. The higher the output capacitance, the lower the ripple and the more DC the output voltage will appear.



(a)



(b)

Figure 3.19 Simulation results of the proposed boost DC to DC converter using dynamically self-biased CS stacking showing (a) input current, output current and output voltage, (b) an increase in drain voltage by approximately 2.49V at every stack

When comparing the results obtained for the 'ideal' boost DC to DC converter with those from Figure 3.19, an output voltage loss of approximately 1V and an efficiency decrease of approximately 25% are observed. These lower results can be attributed to the driver circuit and the stacking circuit, in addition to voltage drops across the transistors through their on-resistances.

The driver circuit consumes power when generating the control signal for the switch stack. This results in a loss in efficiency when considering the power consumed by every part of the converter in addition to the input power. Furthermore, a trade-off between the power consumed and how perfectly square the control signals comes out to be had to be made. When this not-so-perfect gate control square-wave passes through the isolating non-ideal transformers, it deteriorates further, and when it is distributed to all the individual gates of the transistors in the stack, these individual gate signals induce the self-biasing stack to not utilize the entire 2.5V gain across each individual transistor. Thus, the total added voltage at top drain terminal of the stack is lower, which eventually results in a lower output voltage.

Next, at high frequencies, the internal parasitic capacitances of the transistors affect their performance. Figure 3.20 illustrates the parasitic capacitances that need to be accounted for when simulating a circuit with transistors at high frequencies. At high frequencies, these parasitic capacitors present a path between the input and output and lower the output drain voltage and the amplifier gain in case of a CS topology.

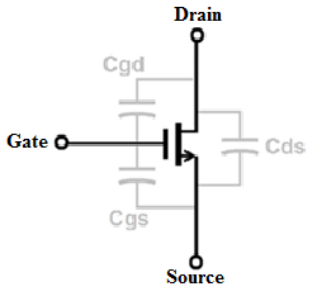


Figure 3.20 Parasitic capacitances present in a transistor that play key roles at high frequency operations

Figure 3.21 demonstrates the 'ideal' boost DC to DC converter with parasitic capacitances – gate to drain (C_{GD}), gate to source (C_{GS}) and drain to source (C_{DS}) – included. Simulation results for an input inductance of 1.5nH at 1GHz gives an output voltage of 6.2V and an efficiency of 51%.

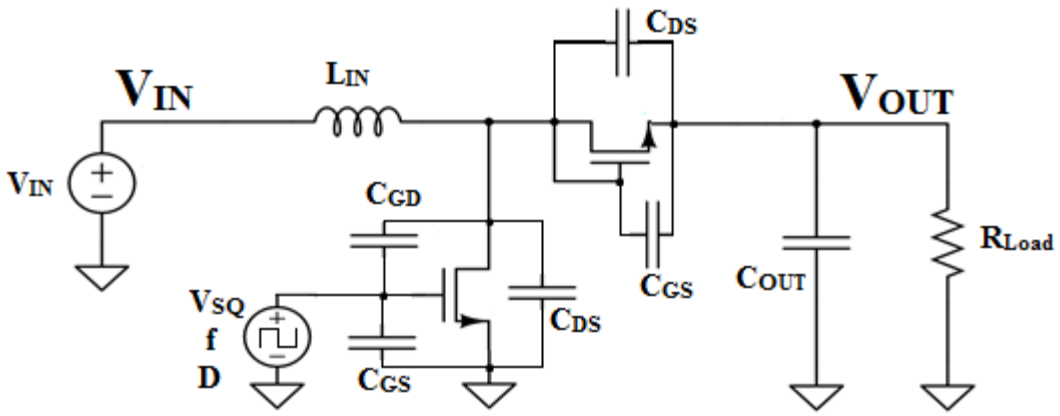
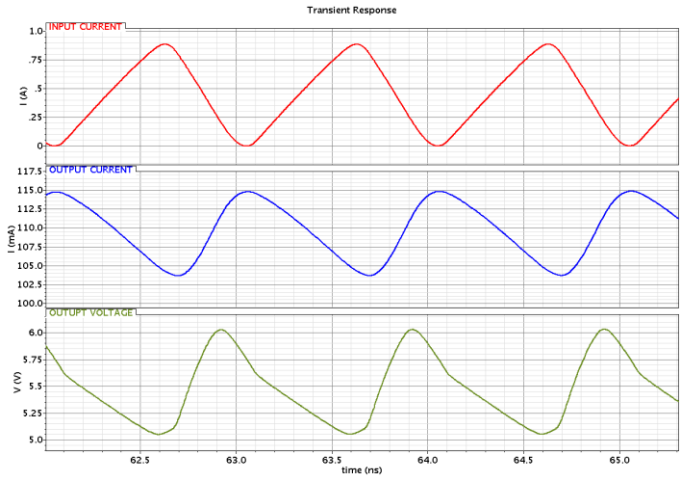
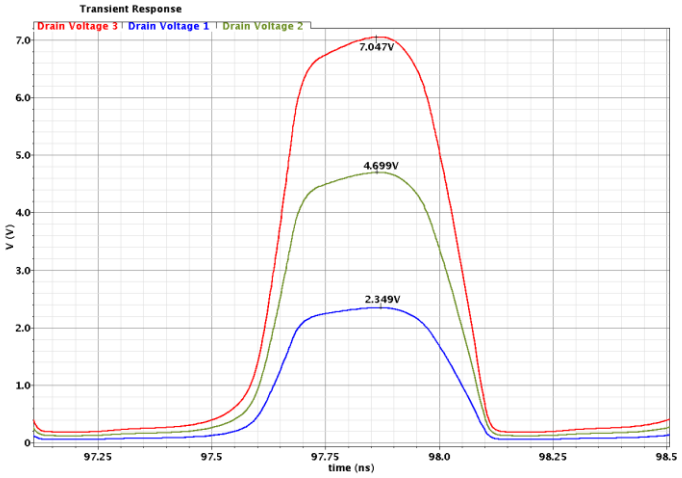


Figure 3.21 'Ideal' boost DC to DC converter with parasitic capacitances C_{DS}, C_{GD} and C_{GS}

Next, parasitic capacitances shown in Figure 3.20 are incorporated into Figure 3.19 for every transistor – the appropriate values of the capacitors were extracted from the layout of the UltraCmos transistor – and deterioration in the performance of the proposed converter with dynamically self-biased CS stacking is observed. After tuning the biasing, the best simulation results achieved are an average output voltage of approximately 5.5V with an efficiency of 37%. Figure 3.22 shows these achieved results. The loss is performance (output voltage and efficiency) due to the parasitic capacitances in the converter can clearly be seen from the lower drain voltages obtained. The phase imbalances seen in Figure 3.22(b) also play a role in the losses in the output voltage and efficiency.



(a)



(b)

Figure 3.22 Simulation results of the proposed converter using dynamically self-biased CS stacking with parasitic capacitances included, showing (a) input current, output current and output voltage, (b) drain voltages at every stack level

3.5.2.2 Proposal #2 – with Dynamically Self-Biased Cascode Stacking

Figure 3.23 demonstrates the circuit schematic of the proposed boost DC to DC converter, in Peregrine UltraCMOS technology, which employs a dynamically self-biased cascode stacking technique to account for the limited voltage swings across each UltraCMOS transistor. Using a cascode cell of two transistors decreases the capacitive

feedback occurring through the gate to drain capacitance from input (gate terminal) to output (drain terminal) of each transistor in the stack. The transformers used for each cell are used to isolate the dependence of one stacked cell from another. As such, the top transistors of two different stacked cascode cells technically display the same performance. Similarly, the bottom transistors of two different stacked cells show the same characteristics and performance. Moreover, the feedback resistors and the biasing capacitors of the two different stacked cascode cells have the same values. From a high level perspective, the two stacked cascode cells in Figure 3.23 are identical in terms of the parameters and performance. The only difference is that the top cell has non-ground reference and the bottom cell has ground as its reference.

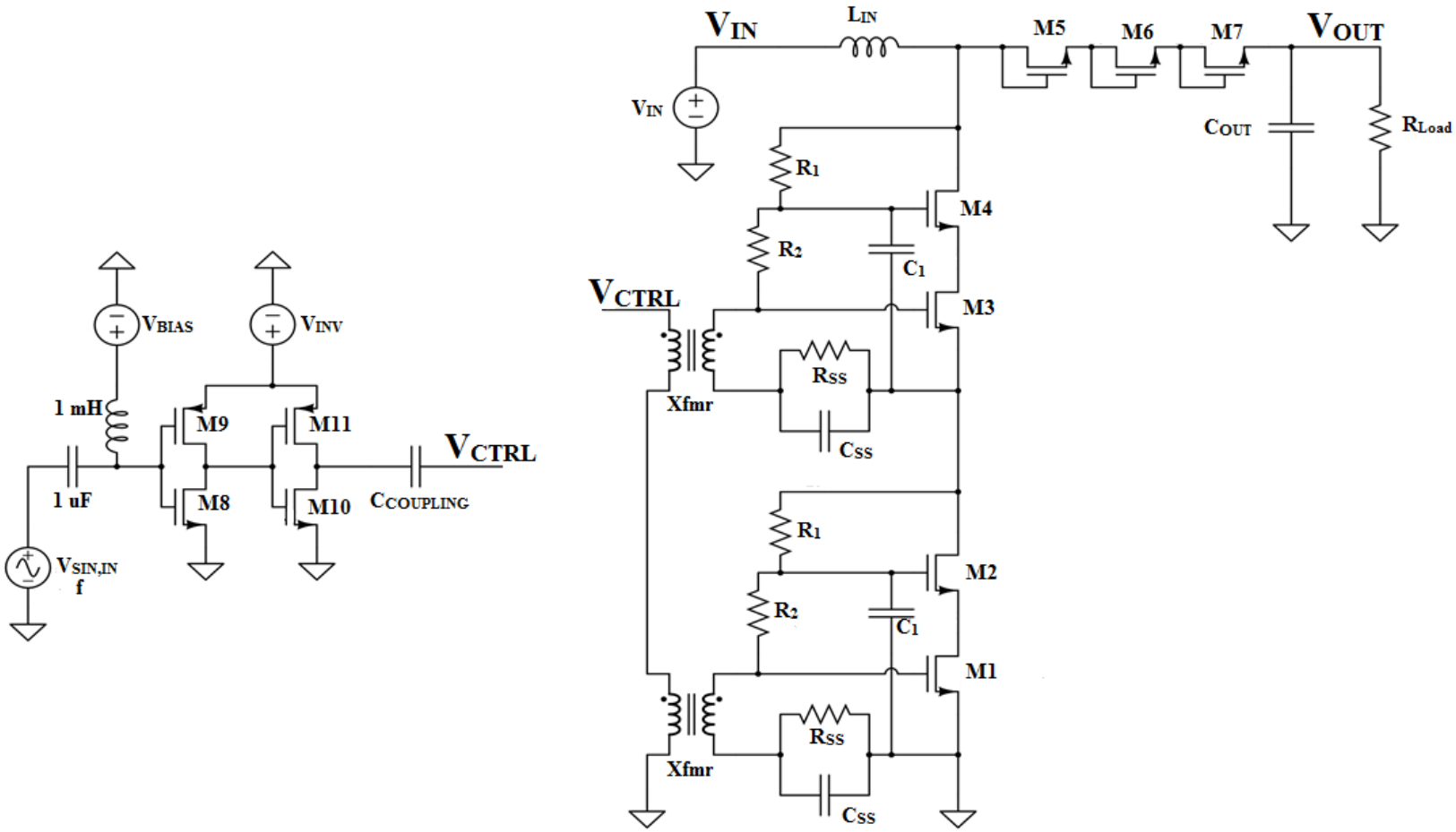


Figure 3.23 Schematic of the proposed boost DC to DC converter in Peregrine UltraCMOS technology with dynamically self-biased cascode stacking approach, in addition to the driver used to generate the gate control signal

After carefully choosing the resistor and capacitor values in the dynamically self-biased stack, the appropriate sizes of all the transistors – in terms of performance and layout, the driver supply and bias voltages, the output capacitor and the best available inductor in the UltraCMOS process, an output voltage of 5V with an efficiency of 40% is achieved for a load of 50Ω (transistor parasitic capacitances are considered). Figure 3.24 illustrates the layout designed for the converter that occupies a total chip area of 3mm by 1mm. Furthermore, Figure 3.25 shows how the output voltage and the efficiency vary with the load.

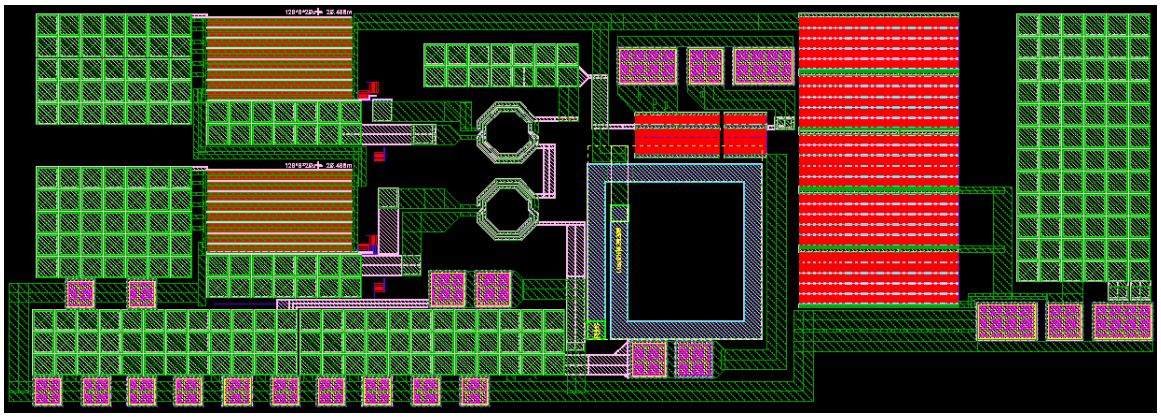
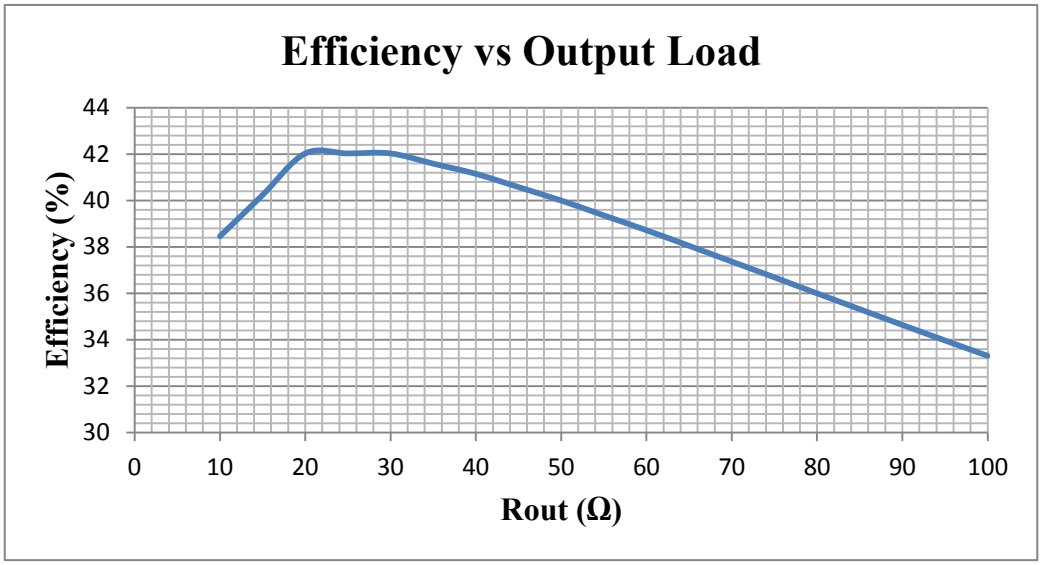
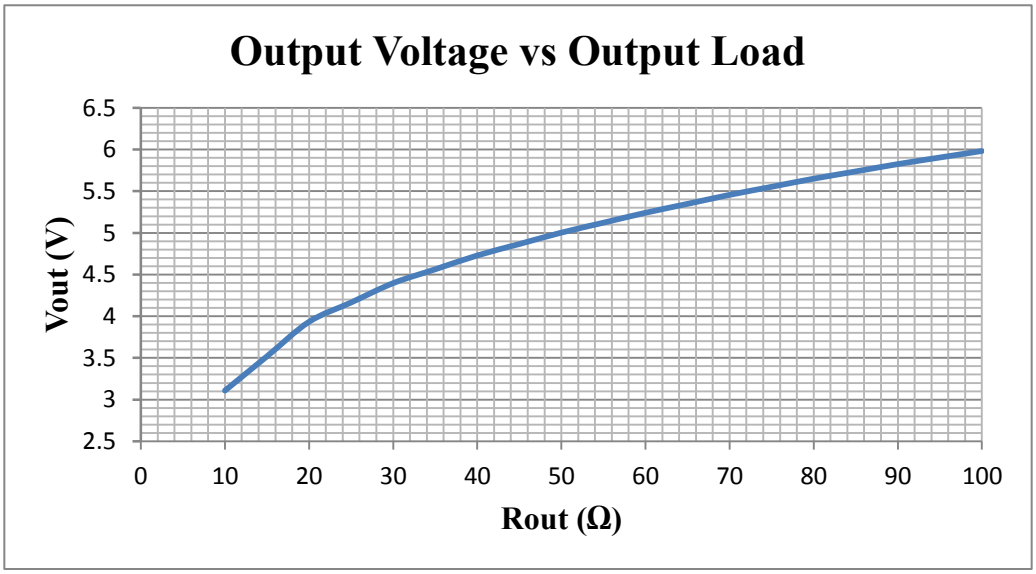


Figure 3.24 The 3mm×1mm layout designed for the proposed boost DC to DC converter in UltraCMOS technology



(a)



(b)

Figure 3.25 Simulation results demonstrating how the (a) output voltage and (b) efficiency vary with the output load

When comparing the results obtained for the 'ideal' boost DC to DC converter with those from Figure 3.25, an output voltage loss of approximately 2V and an efficiency decrease of approximately 35% are observed. These lower results can again be attributed to the driver circuit and the stacking circuit, as stated earlier.

3.5.2.3 Proposal #3 – with Dynamically Self-Biased CS Stacking with 0-V_{th} Transistors

Figure 3.26 demonstrates the circuit schematic of the proposed boost DC to DC converter, in Peregrine UltraCMOS technology, which employs a dynamically-biased CS stacking technique with zero threshold voltage (0-V_{th}) UltraCMOS transistors. The advantage of using 0-V_{th} transistors is that they turn on when the voltage at their gate terminals is greater than 0V, which in turn means that these transistors do not require any bias to turn on. However, negative voltage is required to turn such transistors off completely. As a result, the transistor stack in Figure 3.26 does not have drain to gate feedback resistors to bias the transistors. The transformers are again required to isolate each stack cell from the other, and to achieve the same voltage characteristics across all the stacked cells. The resistance R_{SS} and capacitance C_{SS} help improve the shape of the drain to source voltages across each transistor in the stack. In addition, C_{SS} to some extent counters the voltage degradation due to the gate to source parasitic capacitance and helps improve the overall performance of the stacking technique. Note that Figure 3.26 does not show the parasitic capacitances, but they are always taken into account for the simulations.

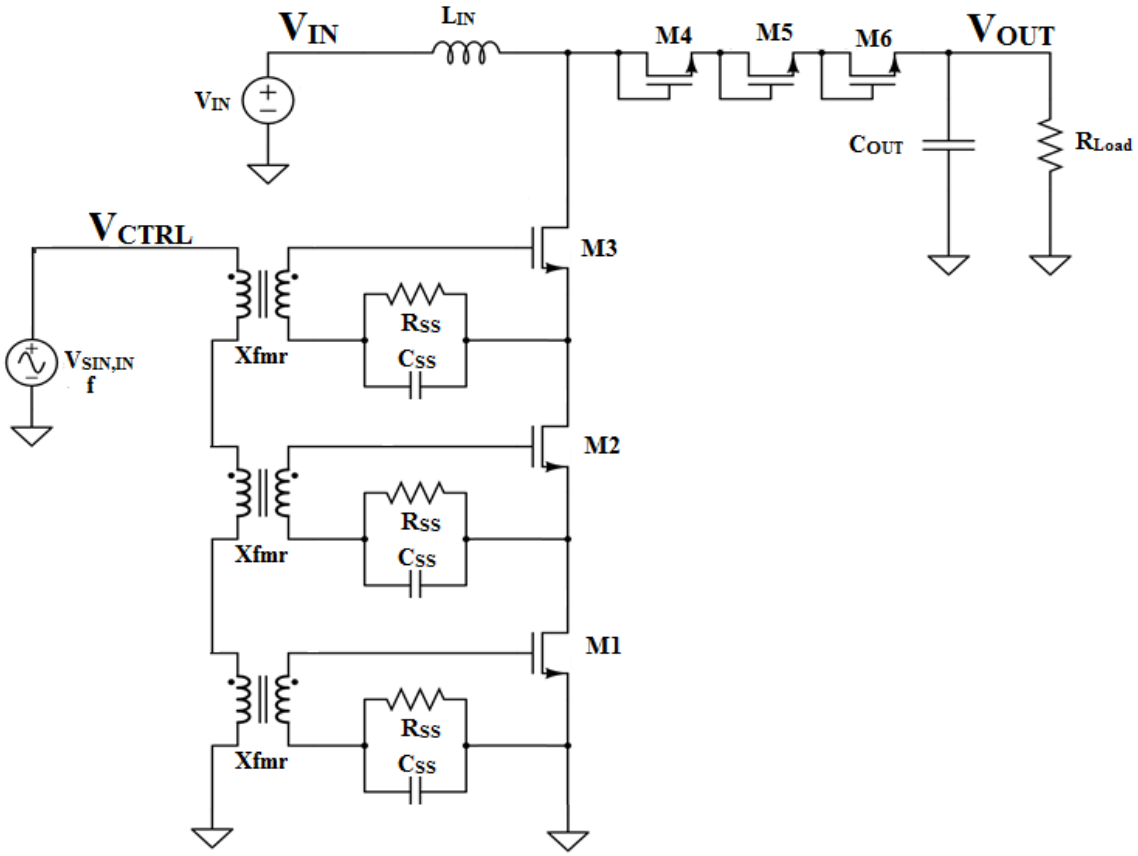
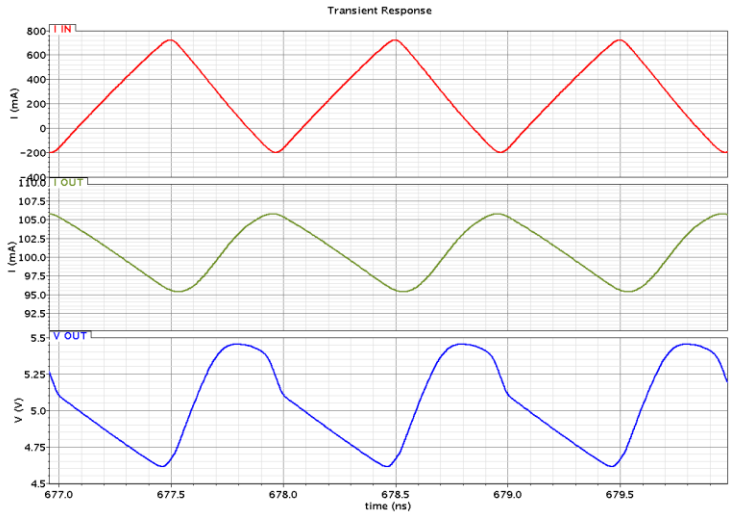
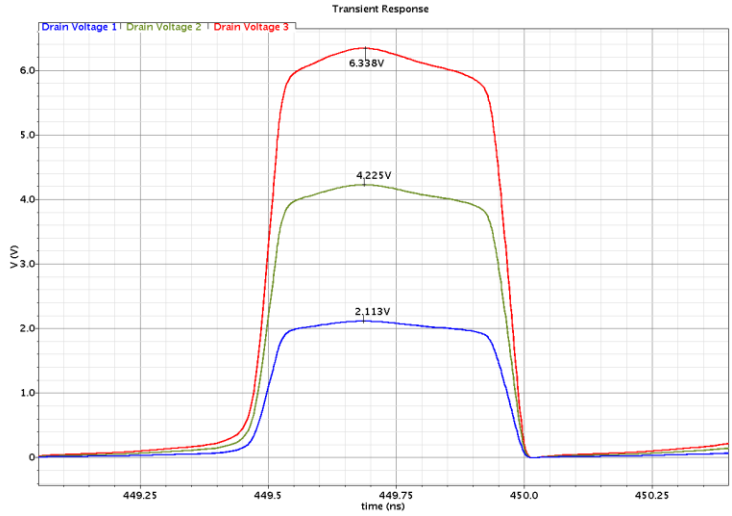


Figure 3.26 Schematic of the proposed boost DC to DC converter in Peregrine UltraCMOS technology with dynamically-biased CS stacking approach with 0-V_{th} UltraCMOS transistors

Since the stacked transistors in Figure 3.26 do not require biasing, two different inputs to the transformers (V_{CTRL}) are simulated. First, a square-wave generated from the output of an inverter chain driver, similar to the one shown in Figure 3.19, is applied to V_{CTRL}. After adjusting the transformer ratios and selecting the appropriate values for R_{SS}, C_{SS} and the transistor widths, an average output voltage of 5V with an efficiency of 51% is achieved. Figure 3.27 shows the simulation results obtained after simulating the circuit shown in Figure 3.26.



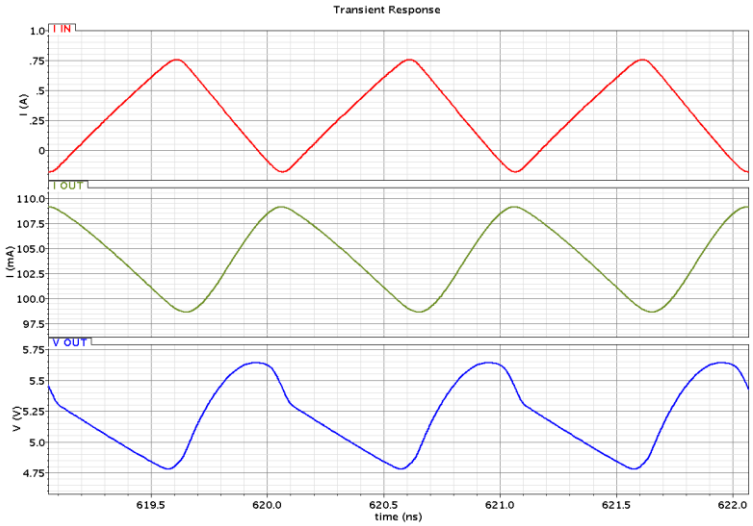
(a)



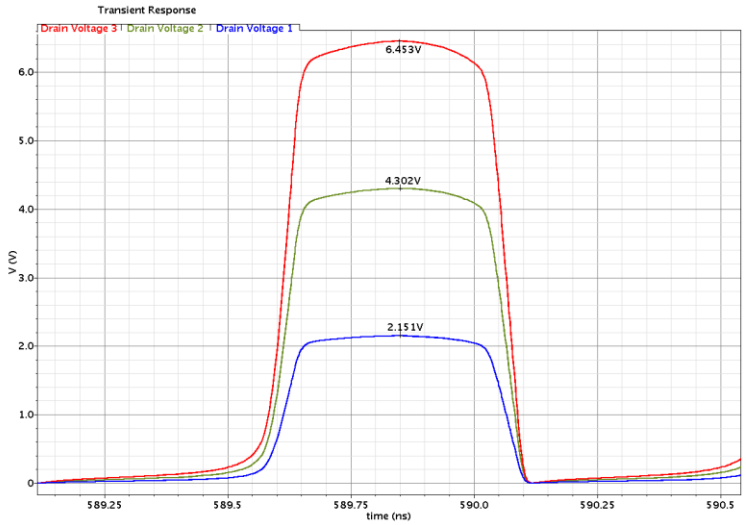
(b)

Figure 3.27 Simulation results of the proposed converter using dynamically-biased CS stacking of 0-V_{th} transistors, showing (a) input current, output current and output voltage, (b) drain voltages at every stack level

Second, sinusoidal signal is directly applied to V_{CTRL} and the transformer ratio is increased in order to account for the duty cycle of the signal at the 0-V_{th} transistor gate terminals. An output voltage of 5.2V is achieved with an efficiency of 55%. Figure 3.28 shows the simulation result obtained by simulating the converter in Figure 3.28 with a sinusoidal applied to V_{CTRL}.



(a)



(b)

Figure 3.28 Simulation results of the proposed converter using dynamically-biased CS stacking of 0-V_{th} transistors with sinusoidal V_{CTRL}, showing (a) input current, output current and output voltage, (b) drain voltages at every stack level

3.5.2.4 Proposal #4 – with Dynamically Self-Biased Cascode Stacking with 0-V_{th} Transistors

Figure 3.29 demonstrates the circuit schematic of the proposed boost DC to DC converter, in Peregrine UltraCMOS technology, which employs a dynamically-biased

cascode stacking technique with zero threshold voltage (0-V_{th}) UltraCMOS transistors. The advantage of 0-V_{th} transistors that they turn on when the voltage at their gate terminals is greater than 0V and the fact that a cascode cell minimizes the capacitive feedback paths present in a CS configuration are combined in this proposed converter design. Again, note that Figure 3.29 does not show the parasitic capacitances, but they are always taken into account for the simulations.

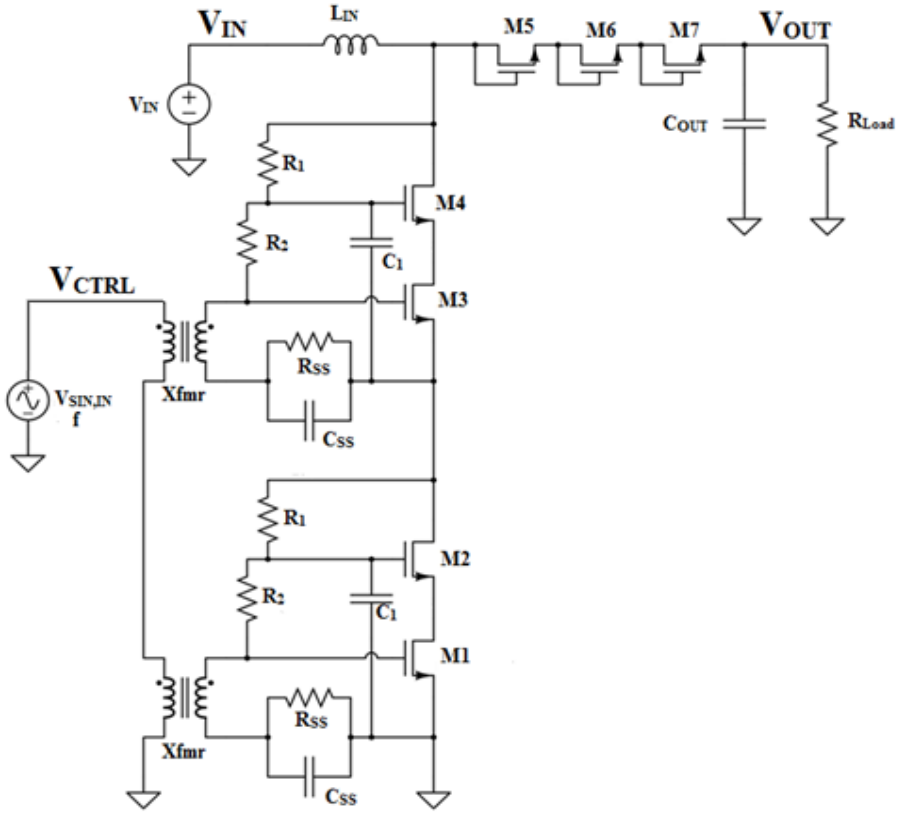
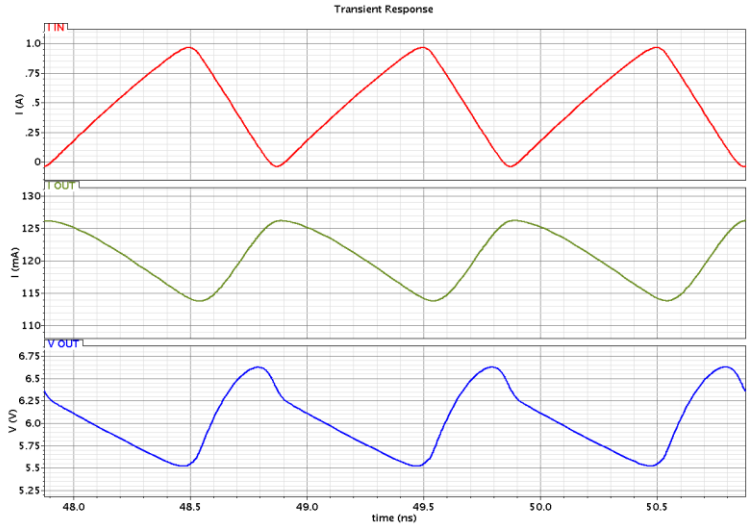
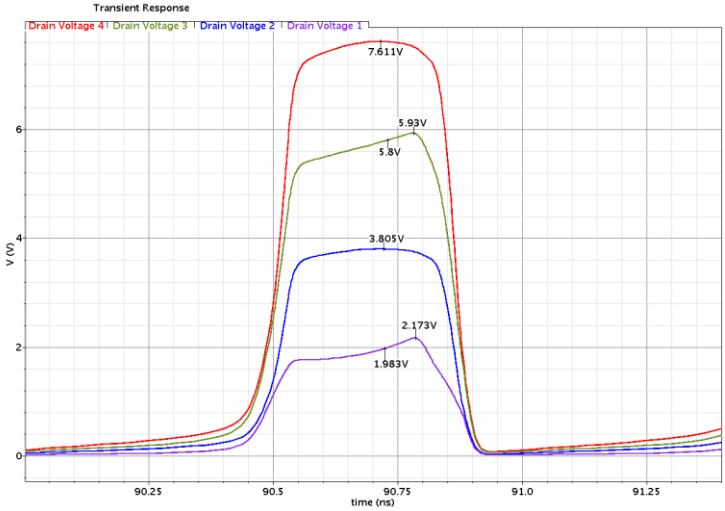


Figure 3.29 Schematic of the proposed boost DC to DC converter in Peregrine UltraCMOS technology with dynamically-biased Cascode stacking approach with 0-V_{th} UltraCMOS transistors

Since the stacked transistors in Figure 3.29 do not require biasing, as a result a sinusoidal signal is directly applied to V_{CTRL}. After adjusting the transformer ratios and selecting the appropriate values for feedback resistors, R_{SS}, C_{SS} and the transistor widths, an average output voltage of 6.1V with an efficiency of 46% is achieved. Figure 3.30 shows the simulation results obtained after simulating the circuit shown in Figure 3.29.



(a)



(b)

Figure 3.30 Simulation results of the proposed converter using dynamically-biased Cascode stacking of 0-V_{th} transistors, showing (a) input current, output current and output voltage, (b) drain voltages at every stack level

The reason for a higher output voltage and slightly lower efficiency is the fact that using cascode configurations of 0-V_{th} transistors with a transformer ratio of 1:2 leads to a higher duty cycle when to compared to the duty cycle achieved with 0-V_{th} CS transistor stacks.

Figure 3.31 illustrates a 3mm x 1.25mm layout designed for the boost DC to DC converter with cascode configuration of 0-V_{th} transistors.

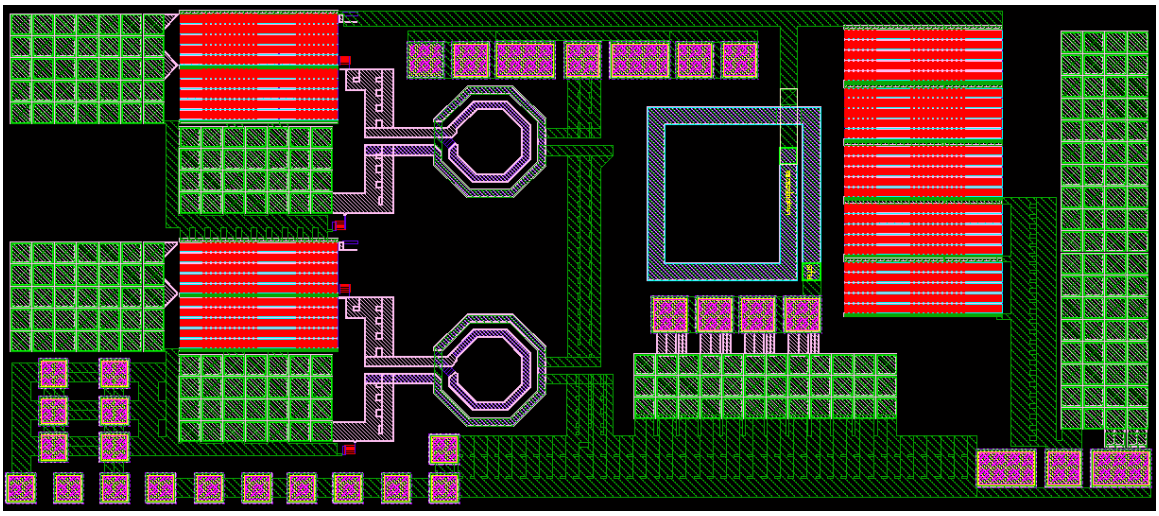


Figure 3.31 The 3mm x 1.25mm layout for the proposed boost DC to DC converter with dynamically self-biased cascode stacking technique with 0-V_{th} transistors

To summarize, the transformers and their ratios have a lot of say in shaping the signals applied to the gate terminals of the transistors in the stacks. The waveforms obtained at the secondary of the transformers are never perfect square-waves. For all the four proposals, the voltages' shapes at the secondary of the transformers are seen to be a mix of sinusoidal and triangular waveforms.

Furthermore, out of the results achieved from the four proposed boost DC to DC converters with dynamically-biased switching techniques, the ones with 0-V_{th} transistors in the stack give the better results in terms of both output voltage and efficiency. One of the main reasons for the third and fourth proposed approaches to give better result among the four proposals is the exclusion of the inverter driver stage to generate the square-wave for V_{CTRL}, but this is done at a trade-off of a higher transformer ratio. Table 3.3 summarizes the results achieved for the four proposed boost DC to DC converters.

Table 3-3 Summary of the results obtained for the three proposed boost DC to DC converters

Performance	Proposal #1	Proposal #2	Proposal #3	Proposal #4
V_{OUT} (V)	5.5	5	5.2	6.1
η (%)	37	40	55	46

To conclude, in defense of the proposed boost DC-DC converters on the whole, the dynamically-biased stacking techniques are the best suited method to avoid transistor breakdowns. They are also the best approaches for having equal voltage distribution in stacked transistors for high power and very high frequency applications. Furthermore, the proposed converters are entirely on-chip designs, facilitating their use for on-chip applications.

4. SUMMARY AND CONCLUSION

The bulk-CMOS technology has been vastly downscaled over the last few decades in order to meet the increasing speed requirements for switching circuits and applications. However, as transistor sizes have entered the sub-100-nm era, increasing leakage currents – due to having reached physical limits of thinning the gate oxide thickness and non-uniformity in doping to form source and drain regions – and reduction in breakdown voltage of devices in this technology have become points of major concern. The SOS technology – one of the first of the SOI semiconductor manufacturing technologies – utilizes highly-insulating sapphire as its insulator and has come out as the preferred choice over the bulk-CMOS technology. The electrically isolated devices in the SOS technology results in reduced junction and parasitic capacitances which in turn leads to higher operating speeds and lower power consumption.

With the growing requirements for high speed switches used in various switching applications such as the DC to DC boost converters, advanced processes such as the SOI and the SOS provide improved system performance when compared to that with bulk-CMOS technology. This thesis used the SOS technology provided by Peregrine Semiconductor known as UltraCMOS for all the proposed and implemented circuitry.

The circuits proposed in this thesis are fully-integrated on-chip DC to DC boost converters with switching circuits based on dynamically self-biased stacked transistors. Different stacking techniques were studied and discussed, and the reason for their failures to be used in place of the switch in the conventional boost converters was voltage amplitude and phase imbalances across the stacked transistors. The dynamically self-biased ensured that the V_{DS} across all the stacked transistors remained equal and did not

exceed the maximum allowed 2.5V. Three variations of the dynamic-biased stacking techniques were studied: common source (CS) stacking, cascode stacking, and CS stacking of almost zero-threshold voltage transistors (zero-V_{th}). One major advantage of the UltraCMOS technology was the presence of almost zero-V_{th} transistors that require very little gate bias voltage to turn on. As discussed, improved results, in terms of efficiency, were obtained for the cascode stacked transistors (V_{OUT} = 5V and η = 40%) as opposed to the CS stacked transistors (V_{OUT} = 5.5V and η = 37%) after the high-frequency parasitic capacitances were accounted for. The zero-V_{th} stacked transistors demonstrated the best results among the three dynamic-biasing techniques discussed with V_{OUT} = 5.2V and η = 55%.

In the context of fully integrated circuits, the SOI technology, and thus the SOS technology, studied in this thesis suffers from large losses of passive components along with the presence of large parasitic capacitances due to low resistivity substrate. The induced parasitic in the transistors and passive components play a major role in degrading the performance of the transistors and in lowering the quality factor of the passive elements used. However, SOS technology is preferred for on-chip designs because its parasitic and junction capacitances are very small compared to those in the bulk-CMOS technology.

For future considerations, there are many areas that can be looked into to help achieve improved performances of the proposed DC to DC boost converters. The idea of replacing the input inductor with a bond wire of appropriate length and quality can help remove the parasitic losses in the inductor and give an improved efficiency and output voltage. However, the PA designs are mostly flip-chipped and would not comply to use any off-chip elements in their power supplies. Furthermore, high-quality factor inductor-capacitor circuits have been recently proposed to obtain a higher quality factor, and such implementations can be looked into as a replacement for the input inductor. Moreover, ways to counter the input-output path created due to the high frequency parasitic capacitances in transistors can be looked into by, for instance, cancelling the negative

reactance with a positive one using inductors. Also, the inductors available in the UltraCMOS process have been used in this thesis only. Optimization of inductors can be looked into to target better quality factor for the input inductor in the DC to DC boost converter.

Additionally, the lack of schottky diodes in the UltraCMOS process required the use of diode-connected transistors in the proposed DC to DC boost converters. The bulk-CMOS technology has schottky diodes available in its process package and their very low forward voltage drops could benefit the boost converters. However, the lack of fast switching transistors in the bulk-CMOS process is a disadvantage.

Most of the DC to DC boost converters proposed in literature so far have been for frequencies far lower than 1 GHz – the target operating frequency in this thesis – and have shown efficiencies of as high as 90% to 95%. The reasons why the proposed converters in this thesis could not achieve such high efficiency are: (i) the very high frequency of operation, 1 GHz, and (ii) fully-integrated on-chip designs. First, large sized transistors start to lose their perfect switching capabilities at high frequencies and the high-frequency parasitic capacitors cause square-wave-shaped drain to source voltages to have higher rise and fall times, leading to lower than ideal voltages. Next, the boost DC to DC converters with high efficiencies proposed in literature utilize off-chip passive components, inductors and capacitors in the range of μH and μF, respectively, which give them the advantage of very low losses due to very high quality factors of the off-chip components. The target of proposing completely on-chip designs at very high frequency in this thesis limited the use of passive elements to those available in the UltraCMOS technology used, and low quality factors of these passive elements contributed to lower achieved efficiencies and output voltages.

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