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Entitled
Advanced III-V / Si Nanoscale Transistor and Contact Modeling and Simulation

For the degree of Doctor of Philosophy

Is approved by the final examining committee:

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ADVANCED III-V / SI NANO-SCALE TRANSISTORS AND CONTACTS: MODELING AND ANALYSIS

A Dissertation

Submitted to the Faculty

of

Purdue University

by

Seung Hyun Park

In Partial Fulfillment of the

Requirements for the Degree

of

Doctor of Philosophy

December 2014

Purdue University

West Lafayette, Indiana

This thesis is dedicated to my family.

ACKNOWLEDGMENTS

I would like to sincerely express my gratitude and appreciation to my advisor, Professor Gerhard Klimeck who is the Reilly Director of the Center for Predictive Materials and Devices (c-PRIMED) and the Network for Computational Nanotechnology (NCN) at Purdue University. He gave me great opportunities to work on various research topics with valuable insights and guidance since the beginning of my graduate year. I also thank to Professor Mark Lundstrom for providing invaluable vision and motivation towards research, and his insightful lectures at Purdue Univerisity and nanoHUB.org have helped me to understand device physics. I would like to give my appreciation to Professor Mathieu Luisier at the Swiss Federal Institute of Technology, Zurich for his guidance and all the knowledge I gained from him.

I also like to thank to Dr. Neerav Kharche and Dr. Rajib Rahman for the valuable scientific discussions and advices as colleagues and friends. I am also grateful to Dr. Yang Liu at IBM Research for his collaboration in our modeling work. I want to appreciate all the members of Prof. Klimeck's group. I am especially grateful for useful comments and discussions with Dr. Saumitra Mehrotra, Dr. Ganesh Hegde, Zhengping Jiang, Yaohua Tan, Kai Miao, Daniel MeJia, Yu He, Hesameddin Ilatikhameneh, Pengyu Long, and James Charles.

I appreciate Professor David B. Janes and Professor Peide Ye for serving on my Ph.D advisory committee. Special thank to Professor Supriyo Datta who leads me to this area through his lecture 'Fundamentals of Nanoelectronics' in undergraduate at Purdue University. I would also like to thank Dr. T. Rakshit and his colleagues at Intel Corporation and Prof. D. Antoniadis and Prof. J. del Alamo at MIT for many valuable discussions.

Research projects were supported by Intel Corporation and MSD/FCRP. The computational support for this research was provided by nanoHUB.org operated by the Network for Computational Nanotechnology and funded by NSF.

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ABSTRACT

Park, Seung Hyun. Ph.D, Purdue University, December, 2014. Advanced III-V / Si Nano-scale Transistors and Contacts: Modeling and Analysis. Major Professor: Gerhard Klimeck.

The exponential miniaturization of Si CMOS technology has been a key to the electronics revolution. However, the continuous downscaling of the gate length becomes the biggest challenge to maintain higher speed, lower power, and better electrostatic integrity for each following generation. Hence, novel devices and better channel materials than Si are considered to improve the metal-oxide-semiconductor field-effect transistors (MOSFETs) device performance. III-V compound semiconductors and multi-gate structures are being considered as promising candidates in the next CMOS technology. III-V and Si nano-scale transistors in different architectures are investigated (1) to compare the performance between InGaAs of III-V compound semiconductors and strained-Si in planar FETs and triple-gate non-planar FinFETs. (2) to demonstrate whether or not these technologies are viable alternatives to Si and conventional planar FETs. The simulation results indicate that III-V FETs do not outperform Si FETs in the ballistic transport regime, and triple-gate FinFETs surely represent the best architecture for sub-15nm gate contacts, independently from the choice of channel material.

This work also proves that the contact resistance becomes a limiting factor of device performance as it takes larger fraction of the total on-state resistance. Hence, contact resistance must be reduced to meet the next ITRS requirements. However, from a modeling point of view, the understanding of the contacts still remains limited due to its size and multiple associated scattering effects, while the intrinsic device performance can be projected. Therefore, a precise theoretical modeling is required to advance optimized

contact design to improve overall device performance. In this work, various factors of the contact resistances are investigated within realistic contact-to-channel structure of III-V quantum well field-effect transistors (QWFET). The key finding is that the contact-to-channel resistance is mainly caused by structural reasons: 1) barriers between multiple layers in the contact region 2) Schottky barrier between metal and contact pad. These two barriers work as bottleneck of the system conductance. The extracted contact resistance matches with the experimental value. The approximation of contact resistance from quantum transport simulation can be very useful to guide better contact designs of the future technology nodes.

The theoretical modeling of these nano-scale devices demands a proper treatment of quantum effects such as the energy-level quantization caused by strong quantum confinement of electrons and band structure non-parabolicity. 2-D and 3-D quantum transport simulator that solves non-equilibrium Green's functions (NEGF) transport and Poisson equations self-consistently within a real-space effective mass approximation. The $sp3d5s^*$ empirical tight-binding method is employed to include non-parabolicity to obtain more accurate effective masses in confined nano-structures. The accomplishment of this work would aid in designing, engineering and manufacturing nano-scale devices, as well as next-generation microchips and other electronics with nano-scale features.

1. INTRODUCTION: III-V / Si NANO-SCALE TRANSISTORS

Nanoelectronic systems represent the past expertise of the semiconductor industry in scalable system design and manufacture. However, as aggressive down scaling by Moore's law, there have been challenges such as gate-channel tunneling, high-k dielectric selection, electrostatic control ability, and low carrier mobility in planar bulk or silicon-on-insulator (SOI) MOSFETs.

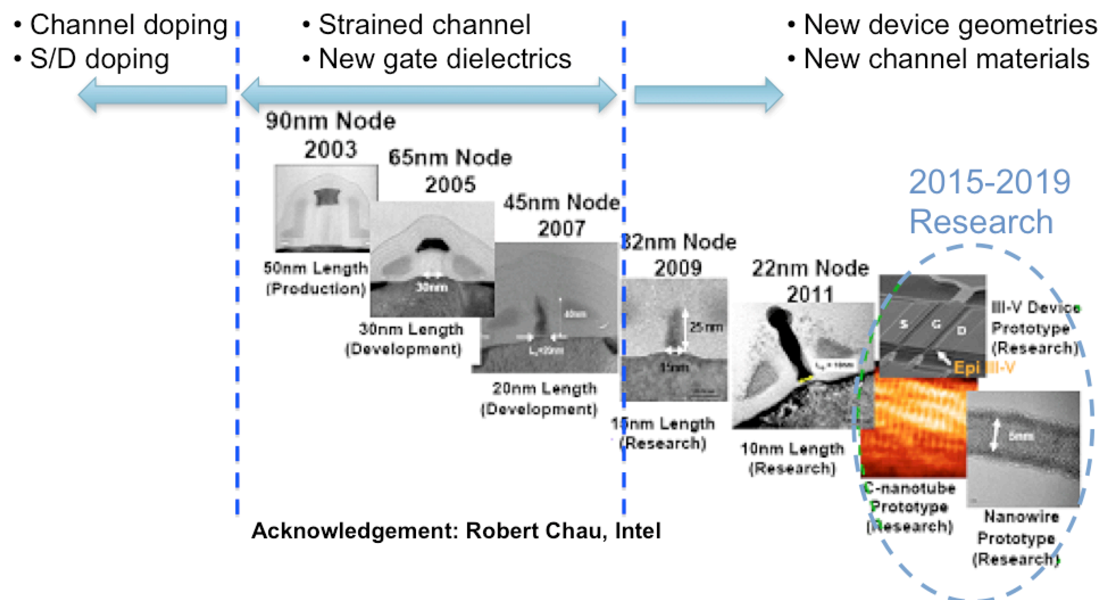

Figure 1.1 CMOS device downscaling and future projections

To keep improving device performance novel concept devices and alternative channel materials are considered and studied for further scaling in high performance CMOS technology in both academia and industry [1-62]. Among semiconductor compound materials, the extraordinary electron transport properties of III-V compound semiconductors like InGaAs, InAs, and InSb make them ideal candidates to replace conventional Si MOSFETs, because III-V FETs benefit from a very high carrier mobility

compared to Si, which enables high speed and low power logic applications such as high electron mobility transistor (HEMT), heterojunction bipolar transistor (HBT), and resonant tunneling diode (RTD). For example the electron mobility of an InSb quantum well reaches a value of 20,000-30,000 $cm^2V^{-1}s^{-1}$ at a sheet carrier density of 1.3×10^{12} cm^{-2} [29], while an InGaAs-InAs-InGaAs multi quantum well (MQW) structure shows an electron mobility of 13,200 $cm^2V^{-1}s^{-1}$ at room temperature and sheet carrier density of 2.9 $\times 10^{12}$ cm^{-2} [39]. Consequently, the energy-delay product of field-effect transistors with an InSb or InAs quantum well as active region can be significantly reduced in comparison to conventional planar Si MOSFETs, making III-V devices faster and more energy efficient.

The III-V technology, which has been present in optoelectronic devices for many years due to a direct band gap, and it has recently undergone considerable progresses in the electronic field to become a viable option for future nano-scale MOSFETs. From 2005 to 2008 a group led by Prof. J.A. del Alamo at MIT has been able to shrink down the gate length of n-channel InGaAs and InAs HEMTs to 30nm [39.51], while keeping excellent device characteristics like low subthreshold slope (SS), drain induced barrier lowering (*DIBL*), and high peak transconductance (>1,000 μS/μm). HEMTs are particularly interesting test beds to study the scaling behavior of III-V channels, but they suffer from relatively high gate leakage currents due to the poor electrical properties of their insulator layer and will therefore not make good low power switches.

In 2006 Freescale in collaboration with the University of Glasgow went beyond the HEMT structure and fabricated an n-channel enhancement-mode GaAs-based MOSFET with an $In_{0.3}Ga_{0.7}As$ channel, a Ga_2O_3 high-κ insulator layer, a 1μm gate length, and a record transconductance of 475 μS/μm, much higher than other research groups. However, to reach low cost mass production and to potentially allow the development of multi-functional chips, III-V MOSFETs must be integrated on large silicon wafers, and not on small GaAs or InP wafers. Intel and QinetiQ demonstrated in 2007 a high-performance 80nm enhancement-mode $In_{0.7}Ga_{0.3}As$ HEMT on silicon, proving that integrating III-V on Si is possible if a composite buffer is used between the Si substrate and the III-V channel.

The comprehension of the bandstructure properties, injection velocities, and quantum confinement effects in III-V compound semiconductors also has carried on a lot of attention since the mid 2000's. Using a top-of-the-barrier ballistic model and a very accurate bandstructure model based on the $sp^3d^5s^*$ tight-binding model, the NCN pointed out in 2005 that the low conduction band density-of-states of III-V materials tends to annihilate the benefit of their very high electron injection velocities [34]. The importance of having a complete description of the bandstructure of III-V materials, especially the non-parabolicity of the conduction subbands in quantum wells and the increase of the transport effective masses due to quantum confinement, has been later confirmed in another study [14-16].

Despite promising improvement in the fabrication process of III-V MOSFETs, however, there remain several technical challenges. The most important one consists in growing an insulator layer with a high dielectric constant on top of the III-V channel to reduce the gate leakage currents and the power consumption. Possible candidates are HfO_2, ZrO_2, or Al_2O_3, all grown by atomic layer deposition (ALD) on top of the III-V material. The trap density at the semiconductor-insulator interface has to be minimized to avoid Fermi level pinning and to keep good electrical performances. At the International Electron Device Meeting (IEDM) in 2008, research groups in academia and industry showed significant improvement in the growth and the quality of the high-κ insulator [4-5].

Si is still the most popular material and is widely used and studied for CMOS channel material. As one of innovative technology, strained-Si is used to obtain higher carrier mobility in Si FETs [6, 20-21]. Also, experimentally the contacts of III-V semiconductors have always been characterized by much larger series resistances than those of Si so far. To improve the performance of III-V FETs optimization process of the extrinsic part of the device is essential [8, 22]. Recently Intel Corporation studied improved contact model by removing thick upper barriers and Si δ-doping in the source and drain region, and it is applied to the InGaAs quantum well field effect transistor (QWFET) non-planar architecture to achieve significant reduction in parasitic resistance [8].

As recently introduced by Intel for the 22nm technology node [25] as shown in Fig. 1.2., to use III-V and Si in the below 30nm technology node might require a change of the device structure, from a single-gate, planar configuration to a multi-gate, 3-D configuration, resulting in a better electrostatic control and scaling performances, because the biggest challenge associated with the downscaling of transistors is the poor electrostatic control of a single-gate contact over the channel of ultra-scaled devices - so-called short channel effects (SCE). Multi-gates architectures [2-3, 8, 11, 24-25] can help suppress SCE, even at short gate lengths, deliver near-ideal sub-threshold slopes, and reduce drain induced barrier lowering (*DIBL*) [2-3].

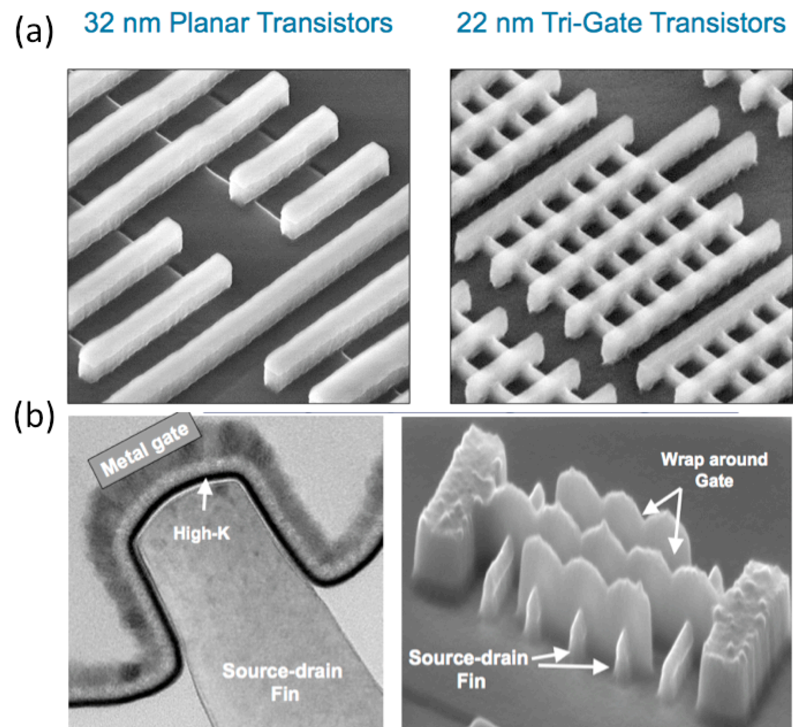

Figure 1.2 (a) Top view of planar and tri-gate transistors (b) cross-sectional and top view of tri-gate transistor

While downscaling, conventional device researches have been focusing on the device channel region as it determines overall system conductance. There is still significant power dissipation in the channel region. However, recent researches show that contact series resistance starts dominating the overall device performance as it takes

larger fraction of the total on-state series resistance. Hence, the contact resistance must be reduced to meet ITRS requirements of future technology nodes. It concludes that the boundary between contacts and channel can be no longer separated. To aid the development of improved contact design, a precise theoretical modeling of contact region is essential to advance optimized contact design.

However, since the exact performance of the III-V and Si FETs as well as the achievable contact series resistances are unknown yet, it is difficult to determine what will be the best material for nano-scale transistors. Hence, the impact of the channel material property, device architecture, and device contact on the ultimate performance of nano-scale transistors needs to be theoretically analyzed.

Our research focuses on studying III-V and Si nano-scale transistors in different architectures at ultra-short gate lengths. However, at near atomic dimensions, conventional silicon device operations are strongly affected by quantum phenomena in the solid-state. Theoretical modeling of two-dimensional (2-D) and three-dimensional (3-D) nano-scale transistors is a challenge due to quantum effects such as the energy level quantization due to the strong quantum confinement of electrons and bandstructure effects due to band non-parabolicity as shown in Fig. 1.3. To address these quantum mechanical issues the state-of-art Nanoelectronic Modeling Tools (OMEN and NEMO5), real-space Schrödinger and Poisson solver, have been used. The real-space effective mass approximation [16, 18] and the tight-binding method have been adapted [14, 26-27], and both approaches showed good agreement with experimental data in previous works of nano-scale transistors [16, 18].

Thesis body is composed of four chapters. In chapter 2, we investigate the performance assessment and analysis of single-/double-gate planar ultrathin-body (UTB) FETs and non-planar triple-gate FinFETs employing $In_{0.75}Ga_{0.25}As$ as a channel material and compares them to strained-Si channel FETs. The high-k gate dielectric (HfO_2) is used as an insulator to circumvent the gate leakage current caused by tunneling across the gate oxide [8, 10, 26].

It should also be noted that the results are based on the same low series resistance assumed in the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs simulation. However, to deliver

similar parasitic resistance, III-V FETs require optimization or better design of the extrinsic part.

Hence, in chapter 3, we model the realistic contact-to-channel region of an InAs/InGaAs high electron mobility transistor (HEMT) and explore the physics of the contact resistance from 2-D InAs HEMT simulations to find various series resistance factors such as the hetero-barrier layers, contact pad, and electron-phonon scattering. The extracted contact resistance is very close to the experimental value. The key finding of this work is that contact-to-channel resistance of InAs HEMT is mainly coaused by structural reasons: 1) thick $In_{0.52}Al_{0.48}As$ barrier between InP etch stopper and $In_{0.53}Ga_{0.47}As$/InAs channel and 2) Schottky barrier between metal and $In_{0.65}Gs_{0.35}As$ contact pad. These two barriers work as bottleneck of the whole system conductance. However, due to thick $In_{0.52}Al_{0.48}As$ barrier between InP etch stopper and $In_{0.53}Ga_{0.47}As$/InAs channel, electrons can flow over the $In_{0.52}Al_{0.48}As$ barrier with thermal assistance from electron-phonon interactions. The electron-phonon scattering also occurs the mobility degradation which is directly related to the device performance. In chapter 4, the effect of electron-phonon scattering is studied to provide performance projections according to the ITRS specifications by extracting the effective mobility.

The series resistance is composed of metal-semiconductor contact resistance, spacer extension resistance, tip resistance, and spreading resistance. Speicific contact resistivity is one of the important factors, and it is determined by factors such as Schottky barrier height and doping concentration. It is expected that the ITRS requirements on the contact resistivity can be met by appliying higher doping concentrations to the semiconductor contact pad region. However, if the contact region reaches to the certain scaling limit (sub-10nm), it is questionalble the resistivity still can meet the ITRS requirements. In chapter 5, the effect of contact geometry is investigated with a presence of Schottky barrier on the specific contact resistivity. Finally, conclusion and summary are described in chapter 6.

2. III-V / STRAINED-SI PLANAR FETS AND NON-PLANAR FINFETS AT ULTRA-SHORT GATE LENGTH

2.1 Abstract

The exponential miniaturization of Si CMOS technology has been a key to the electronics revolution. However, the downscaling of the gate length becomes the biggest challenge to maintain higher speed, lower power, and better electrostatic integrity for each following generation. Both industry and academia have been studying new device architectures and materials to address this challenge. In preparation for the 12nm technology node, this work assesses the performance of the $In_{0.75}Ga_{0.25}As$ of III-V semiconductor compounds and strained-Si channel nano-scale transistors with identical dimensions. The impact of the channel material property and device architecture on the ultimate performance of ballistic transistors is theoretically analyzed. 2-D and 3-D real-space ballistic quantum transport models are employed with band structure non-parabolicity. The simulation results indicate three conclusions: 1) the $In_{0.75}Ga_{0.25}As$ FETs do not outperform strained-Si FETs, 2) triple-gate FinFETs surely represent the best architecture for sub-15nm gate contacts, independently from the material choice, and 3) The simulations results further show that the overall device performance is very strongly influenced by the source and drain resistances.

2.2 Introduction

Novel materials and device architectures are required that will outperform conventional Si-based FETs at ultra-scaled dimensions to keep improving the performance of nano-scale transistors while scaling down their dimensions [1-16]. In particular, it has been demonstrated that InGaAs FETs can exhibit performance superior

to Si FETs because of their very high electron mobility. This may enable high speed and low power logic applications beyond Si-CMOS technology [2, 4, 8-10, 14-19, 27-28]. However, due to recent innovations in strain engineering which have boosted its electron and hole mobilities, Si is still the most popular material and is widely used as the CMOS channel material in both academia and industry [6, 20-21].

A significant challenge associated with the downscaling of transistors is the poor electrostatic control of a single-gate contact over the channel of ultra-scaled devices - so-called short channel effects (SCE). Multi-gate architectures [2-3, 8, 11, 22-24], as recently introduced by Intel for the 22nm technology node [22], can help suppress SCE, even at short gate lengths, deliver near-ideal sub-threshold slopes, and reduce drain induced barrier lowering (*DIBL*) [2-3].

In preparation for the 12nm technology node, this work investigates the performance of single-/double-gate planar ultrathin-body (UTB) FETs and triple-gate FinFETs employing $In_{0.75}Ga_{0.25}As$ as a channel material and compares them to strained-Si channel FETs. The high-k gate dielectric (HfO_2) is used as an insulator to circumvent the gate leakage current caused by tunneling across the gate oxide [8-10, 16, 26].

Since fabricating III-V and Si nano-scale transistors with identical dimensions and electrical properties is very difficult, time consuming, and expensive, the performance of all the devices considered in this work are simulated using a state-of-art computer aided design tool [16-17, 26-30] and not extracted from an experimental setup. Numerical device simulations provide a comprehensive way to capture the electrical behavior of different devices with different materials and structures for performance assessment as long as the same set of approximations is used in all cases.

The theoretical modeling of two-dimensional (2-D) and three-dimensional (3-D) nano-scale transistors demands for a proper treatment of quantum effects such as the energy level quantization caused by strong quantum confinement of electrons and bandstructure non-parabolicity. To address these issues, a single multi-dimensional quantum transport solver based on a self-consistent solution of the Schrödinger and Poisson equations in the real-space effective mass approximation [18] with a tight-binding extraction of the effective mass values is used to simulate III-V and strained-Si

devices in planar and non-planar architectures [17, 27]. With this simulation approach, the *I-V* characteristics of realistic III-V high electron mobility transistors could be accurately reproduced [16-18]. Electron-phonon scattering [28], surface roughness [29], alloy disorder [30], and tunneling gate leakage [26] can in principle be included in the simulations. However, they are not included due to high computation cost in real-space modeling and all the FETs are simulated in the ballistic limit of transport.

This work is organized as follows. Section II describes the single-/double-gate planar UTB FETs and triple-gate FinFET structures, and introduces the simulation approach. The performance of devices employing $In_{0.75}Ga_{0.25}As$ and strained-Si channels are compared and analyzed in Section III. Finally, Section IV summarizes the main findings of this work and concludes it.

2.3 Device Description and Simulaiton Approach

The device schematics of the single-/double-gate UTB FETs and triple-gate FinFETs modeled in this work are shown in Fig 2.1. An $In_{0.75}Ga_{0.25}As$ layer on an $In_{0.52}Al_{0.48}As$ buffer is used as the channel material for III-V FETs [14-16]. The source and drain regions are n-doped with a donor concentration N_D=5×10^{19} cm^{-3} and a length of 20nm. Transport occurs along the <100> crystal axis. A 1% uniaxial stress is applied to the <110>-oriented Si channels with a SiO_2 substrate. Strain is used to achieve a higher electron velocity resulting from a reduction of the effective mass (m*) parallel to the stress direction [6, 20-21]. The source and drain regions of the Si transistors are n-doped with a donor concentration N_D=1×10^{20} cm^{-3} and a length of 20nm.

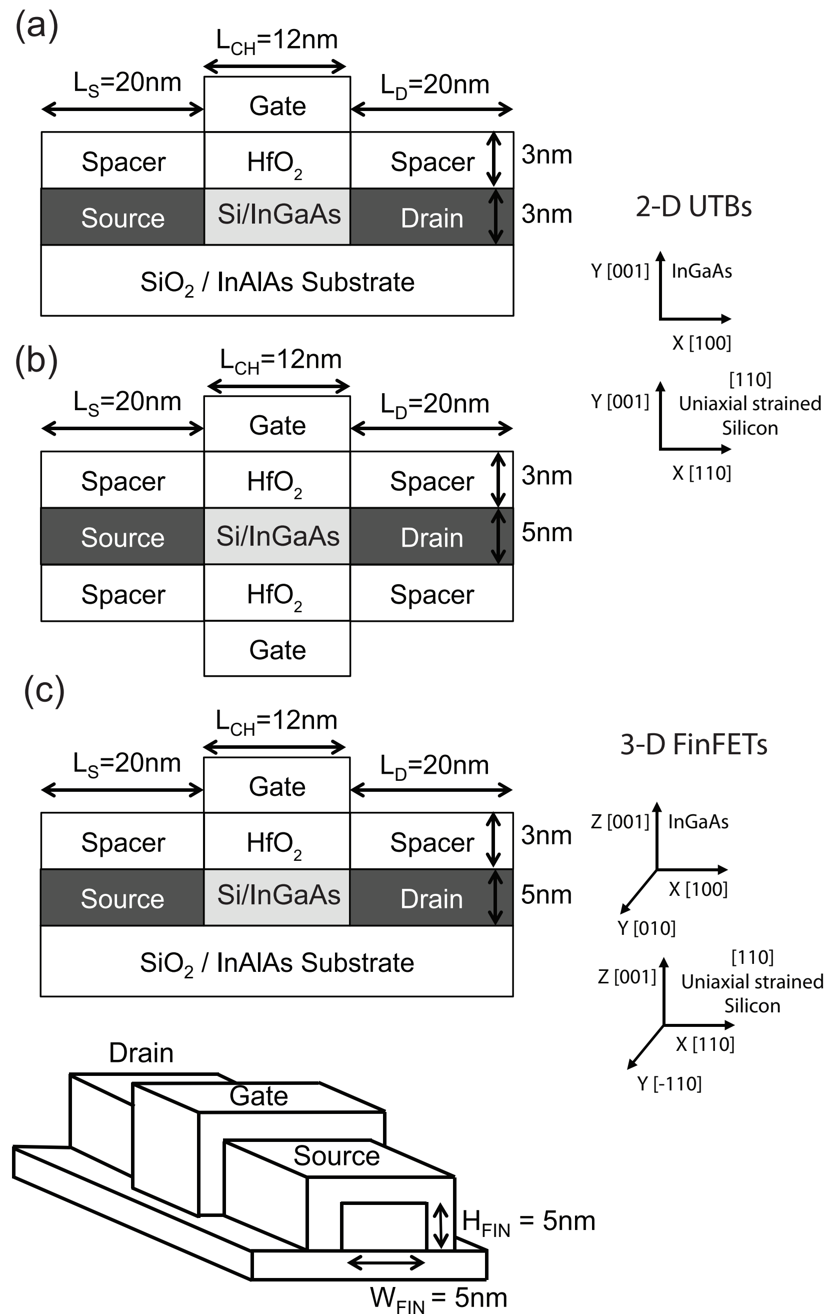

Figure 2.1 Schematics of the simulated devices (a) Single-gate planar UTB FET (b) Double-gate planar UTB FET (c) 2-D and 3-D schematics of triple-gate FinFET.

All architectures use an HfO_2 high-k gate stack with a relative dielectric constant ε_R = 20, a thickness t_{OX}=3nm, and a conduction band gap offset ΔE_C = 2.3 eV and 2.48 eV for $In_{0.75}Ga_{0.25}As$ and Si, respectively [31-32]. This corresponds to an equivalent

oxide thickness EOT of 0.585nm, consistent with the ITRS specifications for the 12nm technology node [1]. To reduce the electric fields coupling the gate to the source and drain regions, the latters are covered by spacers made of a low dielectric material ($\varepsilon_R = 5$).

The simulated III-V and Si UTB FET and FinFET devices have the same geometry and gate stacks, but different channel materials and doping concentrations. The OFF current of all the devices is set to 0.1 μA/μm by varying the work function of the metal gate contact.

To reduce the computational burden, the device structures are simulated in two steps. First, only the intrinsic domain, as illustrated in Fig. 2.1, is considered. Then, the source (R_S = 80 Ω-μm) and drain (R_D = 80 Ω-μm) series resistances taken from the ITRS are added in a post-processing step to the intrinsic *I-V* characteristics. This procedure was described previously in Ref. [13].

The real-space quantum transport solver (OMEN) is used to simulate the 2-D and 3-D FETs in Fig. 1 in the ballistic transport regime. The Schrödinger and Poisson equations are solved self-consistently using the effective mass approximations and a finite difference grid. To account for the strong non-parabolicity of III-V materials, the effective masses of the the $In_{0.75}Ga_{0.25}As$ based transistors are extracted from a $sp^3d^5s^*$ tight-binding (TB) band structure calculation including spin-orbit coupling [14-16].

The transport effective masses (m_t) for the $In_{0.75}Ga_{0.25}As$ transistors are obtained by fitting the curvature of the lowest tight-binding conduction band with a parabola. The confinement effective masses (m_c) are chosen so that the energy difference between the two lowest tight-binding conduction bands is correctly reproduced by the effective mass model. The layers around the $In_{0.75}Ga_{0.25}As$ channel are taken into account when the effective masses are extracted from the tight-binding bandstructure so that the electron wavefunction can deeply penetrated into them, resulting into a larger transport effective masses. This method delivers structure-dependent effective masses which are quite different from their bulk value and are in good agreement with experimental data [16].

Table 2.1. Transport and confinement effective masses and subband degeneracy for the $In_{0.75}Ga_{0.25}As$ and strained-Si planar UTB FETs and triple-gate non-planar FinFETs.

Architecture	Channel Material	m_X	m_Y	m_Z	Degeneracy
Single-gate	$In_{0.75}Ga_{0.25}As$	0.066	0.0159	0.066	1
UTB FETs	[110] 1% Uniaxial	0.16	0.9	0.22	2
2-D	Strained Silicon	0.5	0.19	0.31	4
Double-gate	$In_{0.75}Ga_{0.25}As$	0.059	0.0109	0.59	1
UTB FETs	[110] 1% Uniaxial	0.16	0.9	0.22	2
2-D	Strained Silicon	0.5	0.19	0.31	4
Triple-gate	$In_{0.75}Ga_{0.25}As$	0.0706	0.0769	0.0769	1
FinFETs	[110] 1% Uniaxial	0.16	0.22	0.9	2
3-D	Strained Silicon	0.5	0.31	0.19	4

There are two sets of effective masses for the stained-Si devices with transport along the <110> crystal axis covering the six-fold-degenerate valleys of Si. First, there is a group of four-fold-degenerate valleys with the same transport and confinement effective masses extracted as in Ref. [33-34]. Since the corresponding energy quantization levels are relatively high in energy, strain is not considered for these bands. The second group of two-fold-degenerate valleys requires more attention because by applying a uniaxial tensile stress strain strongly influences the value of their transverse effective masses strongly decreases, leading to better transport properties. The effective masses in this case were taken from Ref. [20] and were verified using the Vienna Ab-initio Simulation Package (VASP) [35]. All the effective masses used in this work are summarized in Table 2.1.

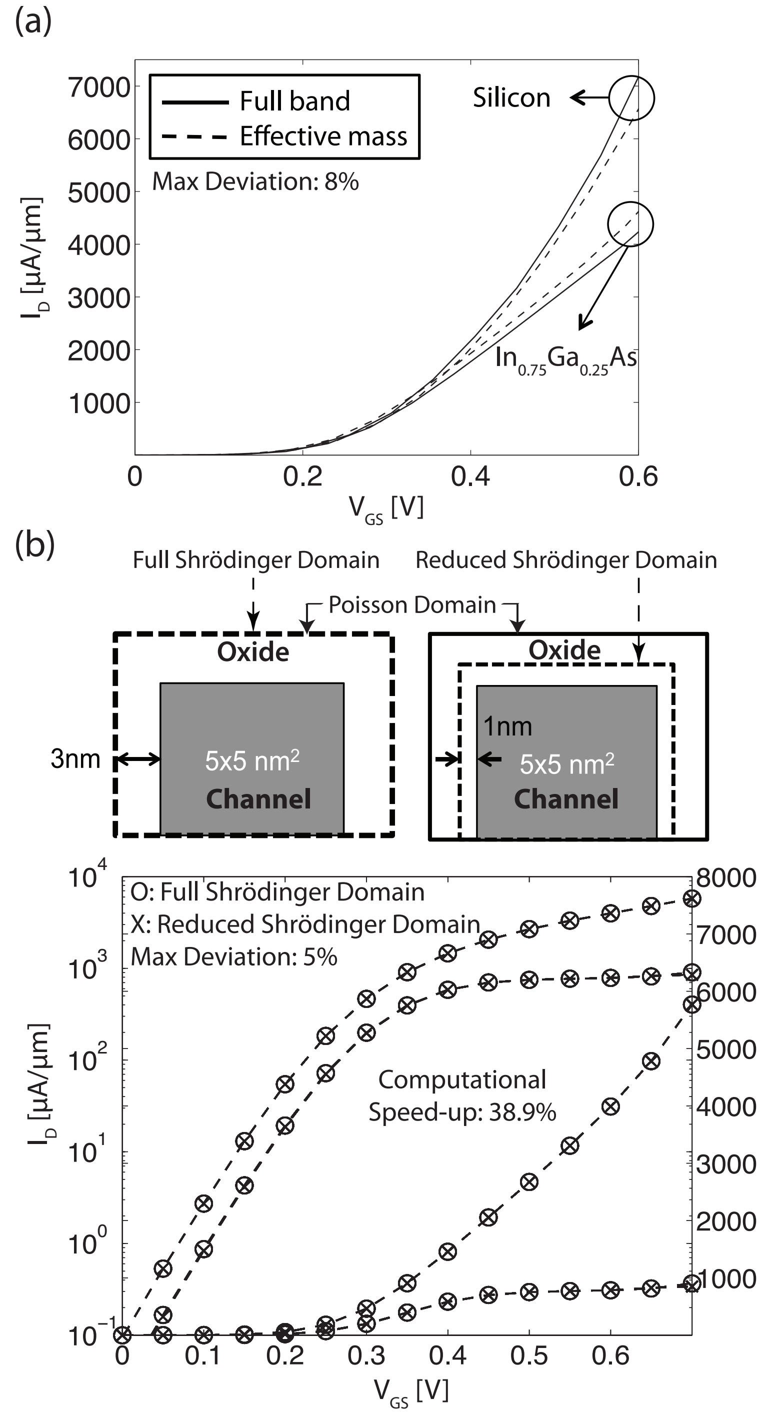

Figure 2.2 (a) Comparison of the full-band (solid lines) and effective mass (dashed lines) I_D-V_{GS} characteristics at V_{DS}=0.7V (b) Comparison of I_D-V_{GS} characteristics at V_{DS}=0.05V and V_{DS}=0.7V simulated using the entire Fin cross section (crosses) and only a part of it (circles).

Full-band atomistic simulations are too computationally expensive to be applied to the complete full I-V characteristics of large 3-D device structures as shown in Fig. 1. However, to verify that our method that extracts effective masses from tight-binding bandstructures works well, the intrinsic I_D-V_{GS} of the $In_{0.75}Ga_{0.25}As$ and strained-Si 3-D FinFETs are simulated in the effective mass approximation and compared to the atomistic tight-binding model [27] at a single V_{DS}=0.7 V. The results in Fig. 2 (a) show that both methods exhibit identical trends with values of drain current very close to each other when I_D < 3000 μA/μm. This corresponds to the domain of interest and demonstrates that a simulation approach based on the effective mass approximation can be used when well-calibrated against a full band model. We note here again that the effective masses used for such agreement are significantly different from the bulk values and heavily influenced by device geometry and confinement details. The use of uncalibrated bulk-based effective masses would yield significantly different results and would not enable a realistic comparison between the Si and InGaAs material systems.

Apart from the bandstructure model, another severely limiting factor in the simulation of 3-D FinFETs is the size of their cross-section which increases the solution time for the Schrödinger equation in real-space. While the entire cross section needs to be included to solve the Poisson equation, the simulation domain of the Schrödinger equation can indeed be reduced. In effect, the electron wave function does not extend all along the surrounding dielectric layers and the Schrödinger domain can therefore be restricted to 1nm around the $In_{0.75}Ga_{0.25}As$ and Si channel. This is illustrated in Fig. 2.2 (b). The I_D-V_{GS} transfer characteristics of the strained-Si FinFET at V_{DS}=0.05 V and 0.7 V are shown in Fig. 2.2 (c) in logarithmic and linear scale. A maximum deviation between the full and the reduced Schrödinger domain solutions of 5% is observed. Consequently, by reducing the simulation domain for the Schrödinger equation, the simulation time for the whole I_D-V_{GS} characteristics consistent of 16 bias points decreases about 39% from 90 hours to 55 hours on 256 cores on 2.5GHz quad core AMD 2380 processors [36].

2.4 Results and Discussion

Based on the methodology presented in Section II we have simulated the III-V and strained-Si UTB FETs and FinFETs shown in Fig. 2.1. From the resulting transfer I_D-V_{GS} and output I_D-V_{DS} characteristics, some key technology parameters such as, *SS*, *DIBL*, ON-current (I_{ON}), ballistic injection velocity (V_{INJ}), and inversion charge density (N_{INV}) were extracted for each device.

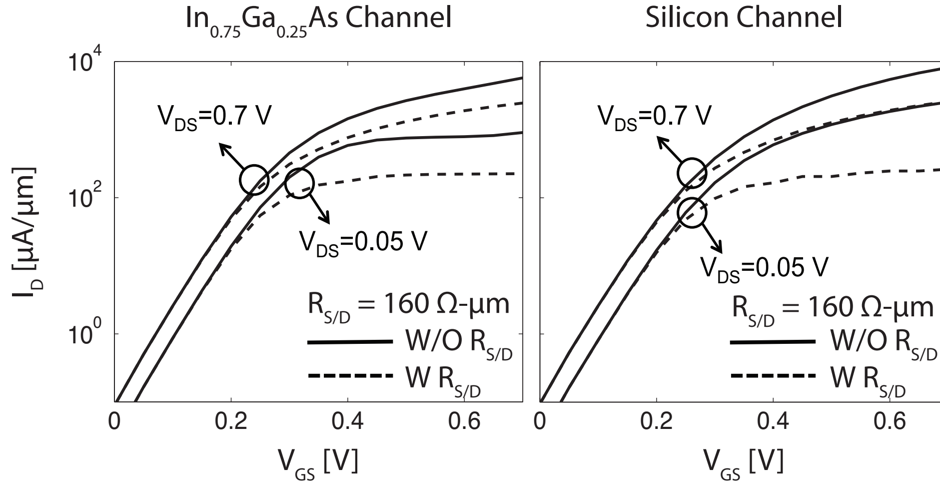

Figure 2.3 Intrinsic (solid lines) and extrinsic (dashed lines) I_D-V_{GS} characteristics of triple-gate FinFETs for (a) $In_{0.75}Ga_{0.25}As$ and (b) strained-Si channels.

As explained earlier, the source and drain contact regions extending beyond the intrinsic device are excluded from the quantum transport simulation. These extrinsic source and drain regions are characterized by two series resistances (R_S and R_D) included as a post-processing step where the intrinsic $V^*_{GS,in} = V_{GS,ext} - I_D R_S$ and $V^*_{DS,in} = V_{DS,ext} - I_D (R_S + R_D)$ account for the correction. For example, the simulated ON-current of $In_{0.75}Ga_{0.25}As$ triple-gate FinFET is extracted at $V_{GS} = V_{DS} = 0.7$ V and amounts to $I_{ON}/W = 2490$ µA/µm, but the intrinsic biases are $V_{GS,in} = 0.5$ V, $V_{DS,in} = 0.3$ V with $R_S = 80$ Ω-µm $= R_D = 80$ Ω-µm. This method has been applied previously and showed good agreement with experimental data [16-18]. Note that drain current of the triple-gate FinFET is normalized by the Fin-height of $H_{Fin} = 5$nm [37]. Fig. 3 shows the intrinsic I_D-V_{GS} and the post-processed I_D-V_{GS} transfer characteristics of the $In_{0.75}Ga_{0.25}As$ and strained-Si triple-

gate FinFETs at V_{DS}=0.05 V and V_{DS}=0.7 V. The source and drain series resistances have a negligible effect on the OFF-state, but they significantly reduce the drain current in the ON-state, by more than 50% in both FETs: the ON-current of the $In_{0.75}Ga_{0.25}As$ triple-gate FET decreases from 5768 μA/μm to 2490 μA/μm after the post-processing. It is clear that the extrinsic source and drain contact regions dominate the overall performance of both device types. Careful and low resistance of contact designs may turn out to be even more important than the optimization of the central device in future device architectures, regardless of the channel material.

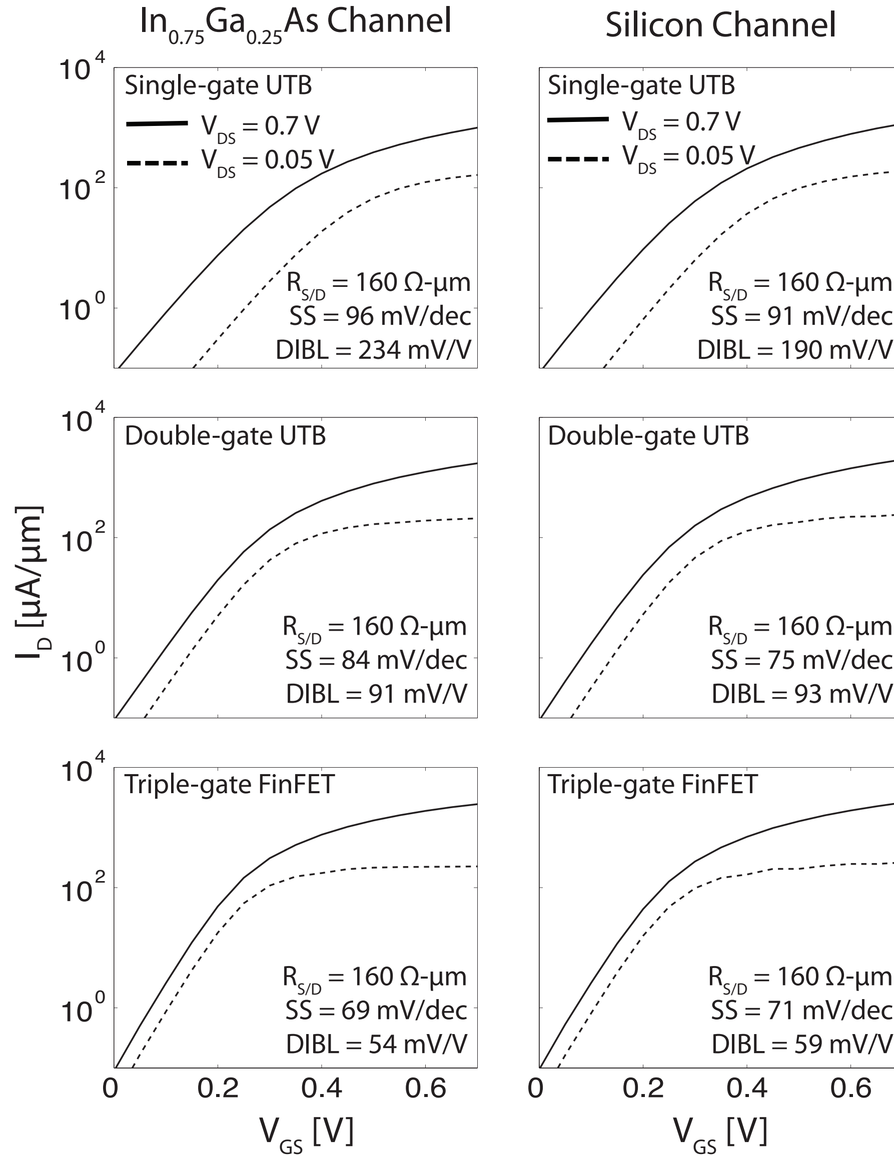

Figure 2.4 I_D-V_{GS} characteristics for the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs for two given drain voltage V_{DS} = 0.05 V and V_{DS} = 0.7 V with different gate voltages V_{GS} from 0.0 to 0.7 V (steps of 0.05 V) in semi-log scale.

Figures 2.4 and 2.5 show the ballistic transfer and output characteristics of the simulated devices after the inclusion of the series resistances. All the performance parameters (*SS*, *DIBL*, I_{ON}, V_{INJ} and N_{INV}) are extracted from *I-V* characteristics shown in Fig. 2.4 and Fig. 2.5. The values are reported in Table 2.2, where the effect of the contact series resistances are taken into account. The power supply voltage for each device is set to 0.7 V to meet the ITRS ON-current requirements for III-V and Si devices [1, 9], and

the metal gate workfunctions are tuned to obtain the same OFF current (I_{OFF}=0.1 μA/μm). Note that for the single-gate transistors a body thickness (T_{body}) of 3nm is needed, because severe SCE are observed with T_{body}=5nm.

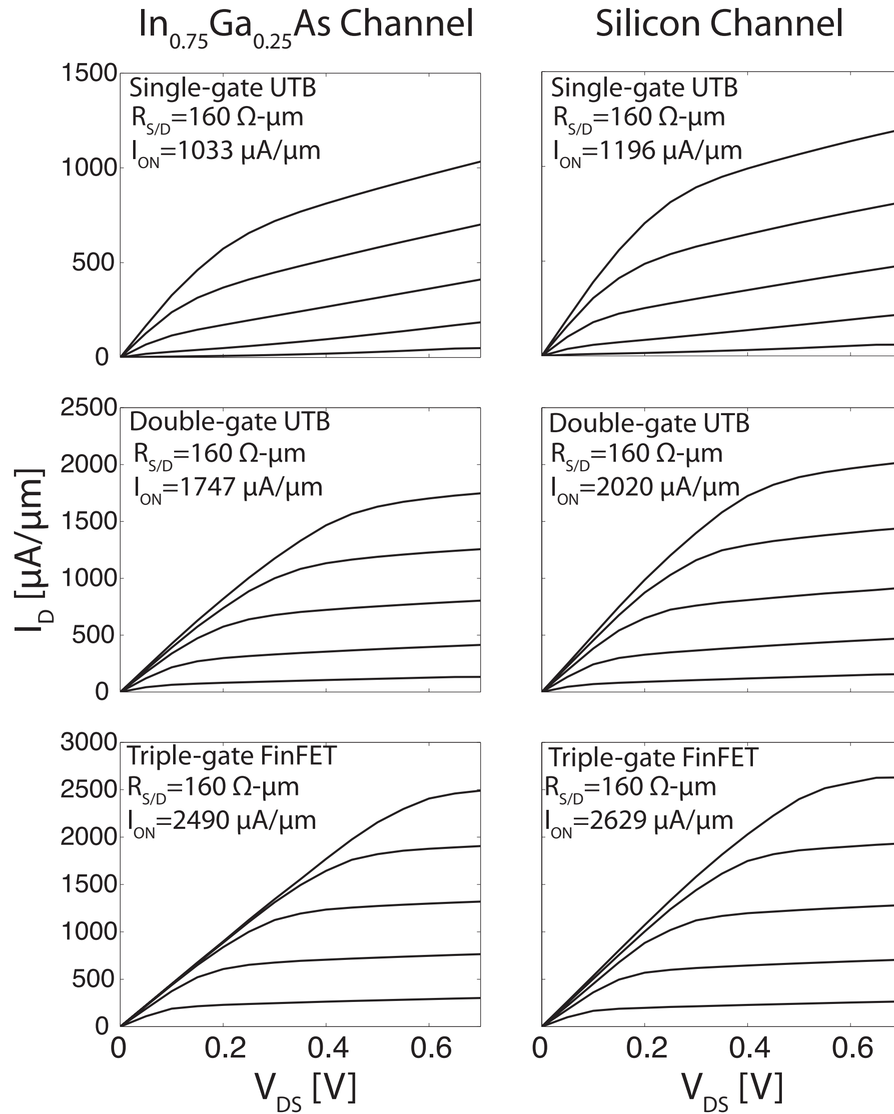

Figure 2.5 I_D-V_{DS} characteristics of the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs at six different gate voltages V_{GS} = 0.0V, 0.3V, 0.4V, 0.5V, 0.6V and 0.7V.

For example, the $In_{0.75}Ga_{0.25}As$ based single-gate FET shows a *SS* of 148 mV/decade and *DIBL* of 441 mV/V when T_{body}=5nm while these values are reduced to 97 mV/decade and 234 mV/V when T_{body}=3nm. Also, to maintain a full substrate depletion

in the single-gate structure the body thickness should be about 1/3 of the gate length. In the case of double-gate and triple-gate transistors the same body thickness (T_{body}=5nm) is employed for comparison under the same conditions. From the extracted performance parameters, the impact of the channel material property and device architecture on the ultimate performance of ballistic transistors is examined theoretically.

Most III-V compound semiconductors such as $In_{0.75}Ga_{0.25}As$ (E_G = 0.53 eV, m^* = 0.032m$_0$, ε_R = 14.4), InAs (E_G = 0.36 eV, m^* = 0.023m$_0$, ε_R = 15.15), and InSb (E_G = 0.18 eV, m^* = 0.014m$_0$, ε_R = 16.8) have a significantly lower band gap (E_G), smaller electron effective mass (m^*), as well as higher relative dielectric constant (ε) than Si. These properties make devices employing III-Vs more prone to SCE compared to Si. Multi-gate architectures become important to reduce SCE in ultra-scaled devices especially for III-Vs.

Table 2.2 Device performance parameters for the $In_{0.75}Ga_{0.25}As$ and strained-Si in single-/double-gate planar FET and triple-gate FinFET configuration.

Structure	Single-gate		Double-gate		Triple-gate	
Material	InGaAs	Si	InGaAs	Si	InGaAs	Si
SS [mV/dec]	97	91	84	75	69	71
DIBL [mV/V]	234	190	91	93	54	59
I_{ON} [μA/μm]	1033	1196	1747	2020	2490	2629
V_{INJ} [cm/s]	3.3×10^7	1.1×10^7	4.5×10^7	9.5×10^6	4.7×10^7	1.1×10^7
N_{INV} [/cm^2]	1.5×10^{12}	5.7×10^{12}	2.1×10^{12}	1.1×10^{13}	3.7×10^{12}	1.8×10^{13}

As shown in Table 2.2, SCE are significantly suppressed in terms of *SS* and *DIBL* in multi-gate structures while single-gate structures can not achieve decent performance parameters, even with a 3nm of body thickness: planar double-gate structures lead to a *SS* improvement of about 13% for the $In_{0.75}Ga_{0.25}As$ FET and 18% for the strained-Si FET as compared to the single-gate devices. The *SS* of the triple-gate FinFET is improved by about 29% for the $In_{0.75}Ga_{0.25}As$ FET and about 22% for the strained-Si FET as compared to their single-gate planar counterparts.

More impressive results are the improvements of *DIBL* when going from planar single-gate to planar double-gate structures and non-planar triple-gate FinFETs: for the $In_{0.75}Ga_{0.25}As$ FET, *DIBL* decreases from 234 mV/V (single-gate) to 91 mV/V (double-gate) and further down to 54 mV/V when used as a FinFET. In strained-Si, the same trend can be observed, *DIBL* is reduced from 190 mV/V to 93 mV/V for the double-gate structures and finally down to 59 mV/V for the triple-gate FinFET. From these results, it can be concluded that only multi-gate structures, and especially triple-gate FinFETs provide a good enough electrostatic channel control and minimize the short channel effects as the transistor gate lengths are scaled down below the 15nm technology node.

The observed trends in *SS* and *DIBL* can be explained by invoking the concept of the geometric screening length for fully depleted (FD) SOI MOSFETs from D. J. Frank et al. [38]. The geometric screening length (λ) gives a measure of SCE inherent to a device structure [11, 21, 39]. It represents the penetration distance of the electric field lines from the drain into the body of the device or the amount of control the drain region has on the depletion zone in the channel, as both the gate and the drain compete for that control. The SCE are proportional to the geometric screening length. A shorter geometric screening length reduces the influence of the drain contact on the channel region and suppresses SCE. In addition, an increased number of gates with the same dimensions of body thickness (T_{Body}) and oxide thickness (T_{OX}) reduce the geometric screening length, as shown in Equation (2.1) [11, 19], where the subscript of each λ represents the number of gates.

$$\lambda_1 = \sqrt{\frac{\varepsilon_{Body}}{\varepsilon_{OX}} T_{Body} T_{OX}}\,,\ \ \lambda_2 = \sqrt{\frac{\varepsilon_{Body}}{2\varepsilon_{OX}} T_{Body} T_{OX}}\,,\ \ \lambda_3 = \sqrt{\frac{\varepsilon_{Body}}{3\varepsilon_{OX}} T_{Body} T_{OX}} \qquad (2.1)$$

Fig. 2.6 illustrates the behavior of the geometric screening length in the $In_{0.75}Ga_{0.25}As$ FET and strained-Si single-, double-, and triple-gate devices. As it can be seen, the non-planar triple-gate FinFET exhibit the lowest geometric screening length and best electrostatic control among all three architectures in terms of *SS* and *DIBL*. The behavior of the geometric screening length also captures the higher improvement rate of SCE in the $In_{0.75}Ga_{0.25}As$ transistors as the number of gates increases. In effect, the difference between the geometric screening length of the $In_{0.75}Ga_{0.25}As$ and strained-Si

FETs ($\Delta\lambda_{\text{number of gates}} = |\ \lambda_{\text{InGaAs}} - \lambda_{\text{Silicon}}\ |$) decreases as the number of gates increases showing that III-V FETs see a larger benefit from multi-gate structures than Si FETs.

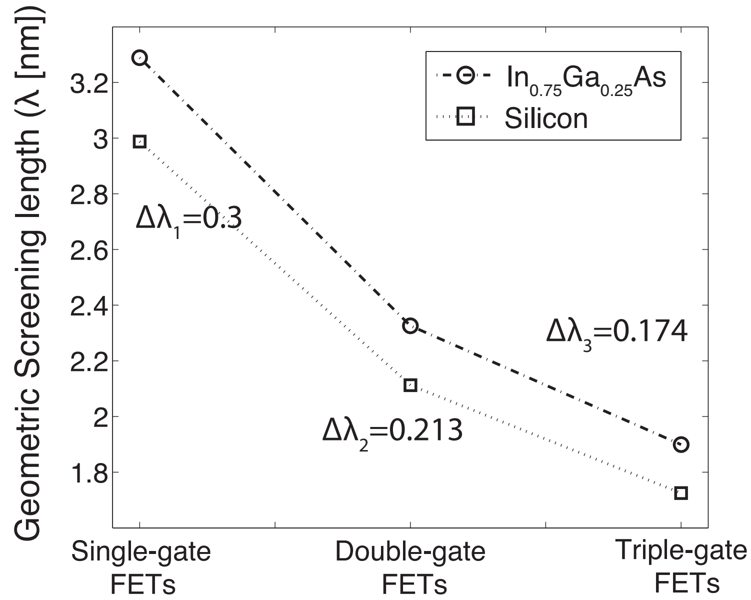

Figure 2.6 The geometric screening length (λ) of the $In_{0.75}Ga_{0.25}As$ and strained-Si planar and non-planar FETs.

Beside the electrostatic control, the properties of the channel materials strongly influence the performance of different FETs. The injection velocity at the top-of-the-barrier (ToB), V_{INJ}, provides a remarkable insight into the transport properties of a given transistor design [44]. Fig. 2.7 summarizes the method to extract this important metric from quantum transport simulations. The $In_{0.75}Ga_{0.25}As$ transistors benefit from a significantly smaller transport effective mass compared to strained-Si, as summarized in Table 2.1, resulting in a ballistic injection velocity at the top-of-the-potential barrier 3 to 4.7 times higher than strained-Si, depending on the device architecture.

However, due to the low effective mass, III-V FETs suffer from a lower density-of-states (*DOS*), which generally reduces the effective gate capacitance and the maximum achievable inversion charge density (N_{INV}). Under the same bias condition, the strained-Si transistors exhibit a 3.8 to 5.2 times higher inversion charge density at the ToB compared to the $In_{0.75}Ga_{0.25}As$ transistors. The increase of the inversion charge at the ToB overwhelm the benefit of a high injection velocity since the drain current can be

expressed as $I_D = q\ V_{INJ} N_{INV}$, where q is the elementary charge. Therefore, the strained-Si FETs have slightly higher ballistic ON-currents than the $In_{0.75}Ga_{0.25}As$ FETs, as shown in Table 2.2.

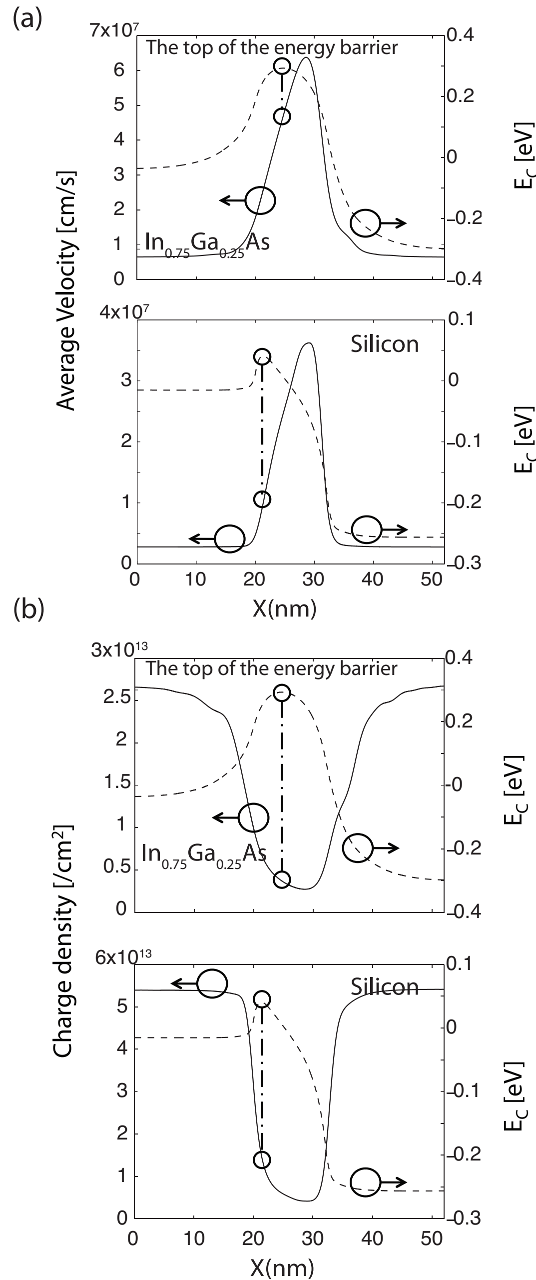

Figure 2.7 (a) Ballistic injection velocity in the $In_{0.75}Ga_{0.25}As$ and strained-Si double-/triple-gate FinFETs extracted at the top of the energy barrier (b) ON-state carrier density in the $In_{0.75}Ga_{0.25}As$ and Si double-/triple-gate FinFETs extracted at the top of the energy barrier.

The inversion charge and injection velocity are not only affected by material properties, but also by the device architecture. In Table 2.2, an increase of the injection velocity and inversion charge density can be observed in multi-gate architectures which deliver higher current drives than single-gate devices. Hence, the ON-current of the double-gate structures is improved by about 1.7 times in both the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs as compared to the single-gate structures. The ON-current of the triple-gate FinFET increases about 2.4 times in the $In_{0.75}Ga_{0.25}As$ FET and 2.2 times in the strained-Si FET again compared to the single-gate architectures.

The $In_{0.75}Ga_{0.25}As$ FETs see a higher performance improvement than the strained-Si in devices as the number of gates increases, because the III-V materials are more sensitive to SCE and take advantage of the better electrostatic control provided by the multi-gate architecture. As a consequence, and this is the key finding of our work, Table 2 demonstrates that the $In_{0.75}Ga_{0.25}As$ and strained-Si triple-gate FinFETs exhibit almost identical performance metrics: a low *SS* and *DIBL* as well as a large ballistic ON-current.

However, it should be emphasized that the ballisticity of ultra-short III-V and strained-Si nano-transistors is currently unknown and difficult to estimate. So far, Si-based FETs have always operated at about 50% of their ballistic limit, mainly due to surface roughness scattering at the $Si\text{-}SiO_X$ interface [41]. This number has not changed much for many successive technology generations. In addition, recent reults of Si and III-V transistor simulation prove that electron-phonon scattering plays a more important role in Si than in III-V [42], because many more subbands are available in Si than in III-V for electrons to scatter out of the original state.

In contrary, specific III-V FETs seem to operate very close to their ballistic limit [16, 18, 39] since surface roughness scattering is extremely small in these devices. Especially, growing a high-κ layer directly on the top of a III-V channel might significantly increase surface roughness and remote Coulomb impurity scattering in these transistors and deteriorate their ballisticity. There are number of proposed processing techniques such as interfacial passivation layer (IPL) and atomic layer deposition (ALD) to address the interfacial chemistry on III-V compound semiconductors [2, 10, 43]. In effect, their insulator layer is often made of another III-V material with a larger band gap

or a wide band gap III-V material / high-κ gate stack so that the channel-insulator interface is very smooth. Such insulator layers work well for relatively large EOT, but it is not clear yet what will happen when the EOT must be reduced below 1nm.

It should also be noted that simulation results are based on the same low series resistance assumed in the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs simulation. The contacts of FETs based on III-V semiconductors are often characterized by higher series resistance compared to Si [8, 16, 18, 39, 46]. However, some studies indicate that the contact resistance of n-type InGaAs can be significantly reduced by using innovative processing techniques [44, 45]. Experimentally, the contacts of III-V semiconductors have always been characterized by much larger series resistances than those of Si due to structural reasons [8-9, 16, 18, 39, 46]. The analysis presented here emphasizes the need to optimize the extrinsic part of the device by incorporating such novel processing techniques in order to reduce the contact resistance and improve the performance of III-V FETs. [8, 44, 45, 46].

Since the exact ballisticity of the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs as well as the achievable contact series resistances are uncertain yet, it is difficult to determine what will be the best material for nano-scale transistors. However, numerical device simulations are required to provide performance projections according to the ITRS specifications without complicated fabrication processes of multiple device prototypes. The simulation results indicate that at 12nm gate length, $In_{0.75}Ga_{0.25}As$ FETs deliver very similar performance as strained-Si FETs. The contact resistances dominate the behavior of both device types. Triple-gate FinFETs surely represent the best architecture for sub-15nm gate contacts, independently from the choice of the channel material.

2.5 Conclusion and Outlook

This work assesses the performance of the $In_{0.75}Ga_{0.25}As$ and strained-Si channel nano-scale transistors in single-/double-gate planar FETs and non-planar triple-gate FinFETs configurations in preparation for the 12nm technology node. The device structure, doping concentration, OFF-current, and normalization conditions are defined according to the ITRS specifications and with the help of Intel Corporation. The impact

of the channel material property and device architecture on the ultimate performance of ballistic transistors is theoretically analyzed.

The simulation results indicate that III-V FETs do not outperform Si FETs in the ballistic regime, but deliver very similar performance. However, III-V is still one of the most promising candidates, because they could operate closer to their ballistic limit than Si FETs under certain circumstances and therefore provide higher ON-current due to less performance degradation from electron-phonon and surface scatterings. Ultra-short III-V FETs need multi-gate structures to overcome the weakness of SCE caused by their narrow band gap, small electron effective mass, and high relative dielectric constant. Multi-gate architectures represent a very consistent way to reduce *SS* and *DIBL* while increasing the ON-current. Also, to keep improving the performance of both III-V and Si FETs in the future technology nodes, their source and drain regions should be optimized to minimize their contact series resistance, since the overall device performance will be dominated by the contact resistance. © [2012] IEEE. Reprinted, with permission, from [S. H. Park, Y. Liu, N. Kharche, M. S. Jelodar, G. Klimeck, M. S. Lundstrom, M. Luisier, "Performance Comparisons of III-V and Strained-Si in Planar FETs and Nonplanar FinFETs at Ultrashort Gate Lengh (12nm)," *IEEE Trans. Electron Devices*, vol. 59, no. 8, Aug. 2012]

3. CONTACT-TO-CHANNEL REGION MODELING AND SIMULATION IN III-V HETERO-STRUCTURE DEVICE

3.1 Abstract

While the performance of III-V devices looks promising, actual device prototypes are negatively influenced by high contact resistances. The understanding of the contacts remains quite limited due to factors such as structural complex and size of the simulation domain. Physics-based modeling is required to advance optimized contact design to improve the overall performance. This work investigates computationally the effects of hetero-contact geometry on the contact resistance of InAs QWFET. The contact resistance is calculated using a 2-D / 3-D quantum transport simulator that solves non-equilibrium Green's functions (NEGF) transport and Poisson equations self-consistently within a real-space effective mass approximation. The sp3d5s* empirical tight-binding method is employed to include non-parabolicity to obtain accurate non-linear effective masses in confined nano-structure. The key findings of this work are that the contact-to-channel resistance is dominated by structural reasons: 1) $In_{0.52}Al_{0.48}As$ barrier between InP etch stopper and $In_{0.53}Ga_{0.47}As$/InAs channel and 2) Schottky barrier between metal and $In_{0.65}Ga_{0.35}A$ in 2-D simulation domain.

3.2 Introduction

The progressive downscaling has allowed semiconductor industries to continue improving the performance of integrated circuits (ICs) [1]. Short channel effects associated with the downscaling degrade the performance of the intrinsic transistor device [2-4]. The downscaling also adversely affects the performance of contact series resistance. The contact series resistance acts as a parasitic source and drain contact

resistance of a device, and it is becoming an important performance limiting factor [49-50] as it takes larger fraction of the total on-state resistance. Hence, contact resistance must be reduced to meet the international technology roadmap for semiconductors (ITRS) performance requirements of future technology nodes [1, 16, 49-50].

Both industry and academia have been studying new device architectures and materials to keep improving device performance. The usage of III-V materials has turned out to be one of the promising candidates for a post Si era due to extremely high electron mobility. For instance, it was shown that III-V high electron mobility transistors (HEMT), which are mostly used as an excellent testing bed for III-V compound semiconductors, could achieve very high-speed operation at low supply voltage for future logic applications [8, 9, 16, 36, 49, 50-54].

While the intrinsic device performances of current III-V device prototypes look promising, they appear to suffer from significantly higher contact series resistance compared to regular MOSFETs. The contact series resistance is composed of many factors: Schottky barrier between metal-semiconductor contact, multiple barriers between different III-V semiconductor layers, L-shaped area from contact pad to channel region, alloy disorder, electron-electron scattering, electron-phonon scattering, and surface roughness. While the performance of intrinsic devices can be directly projected, the understanding of the contacts still remains limited due to the size and many illustrated factors. Hence, a precise theoretical approach is required to characterize the contact series resistance. The development of accurate, physics-based contact models is becoming a critically needed topic.

In this work, the contact resistance is directly extracted from our quantum transport simulations, and the main factors determining the series contact resistance within realistic 2-D contact-to-channel structure of InAs quantum-well FET (QWFET) are investigated.

3.3 Device Description and Simulation Approach

To understand the basic physical process contributing to the contact resistance we chose to isolate the contact region explicitly from the intrinsic, central device. The L-shaped contact-to-channel region of a state-of-the-art InAs QWFET is separated as its own independent device. The contact series resistance (R_S) is directly extracted in this explicit contact simulation domain. This new approach is in contrast to conventional device simulations where the intrinsic device domain as shown in Fig. 3.1 (b) is modeled first, and the source (R_S) and drain (R_D) series resistances taken from experiments or ITRS are added to the intrinsic *I-V* characteristics in a post-processing step. This lumped circuit treatment of the contacts is widely applied and showed great agreement with experimental data [16, 49]. However, such lumped circuit approach hides the critical physics that lead to resistance. In this work we aim to help to understand the contact resistance as a critical part of the overall device and open opportunities for future improvements. We show that a state-of-the-art computer-aided design tool [55] can calculate the contact series resistance from the isolated contact simulation domain and also capture the electrical behavior in the nano-scale contact region.

The simulated InAs QWFET device structure has exactly same thickness of III-V layers as used in the experimental work [53-54] with a height of 90 nm, and it is composed of 10 different layers from the substrate to the semiconductor contact pad: highly doped $In_{0.65}Ga_{0.35}As$ / $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ n+ cap, InP etch stopper, $In_{0.52}Al_{0.48}As$ barrier, delta-doped layer, $In_{0.53}Ga_{0.47}As$ / InAs / $In_{0.53}Ga_{0.47}As$ channel, and $In_{0.52}Al_{0.48}As$ substrate. The $In_{0.65}Ga_{0.35}As$ / $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ n+ cap layer is n-doped with a donor concentration N_D=3×10^{19} cm^{-2}. A delta-doped layer is n-doped with a donor concentration N_D=5×10^{19} cm^{-2} with 0.5nm thickness, and it is placed below gate contact to induce the electrons for channel conduction. The L-shaped simulation domain is chosen from the InAs QWFET structure and the width of the contact region is set to 30 nm instead of 2.0 μm of the real device. 30 nm of the contact width is not only the effective length to provide enough current, but it is also small enough such that the system can be treated computationally.

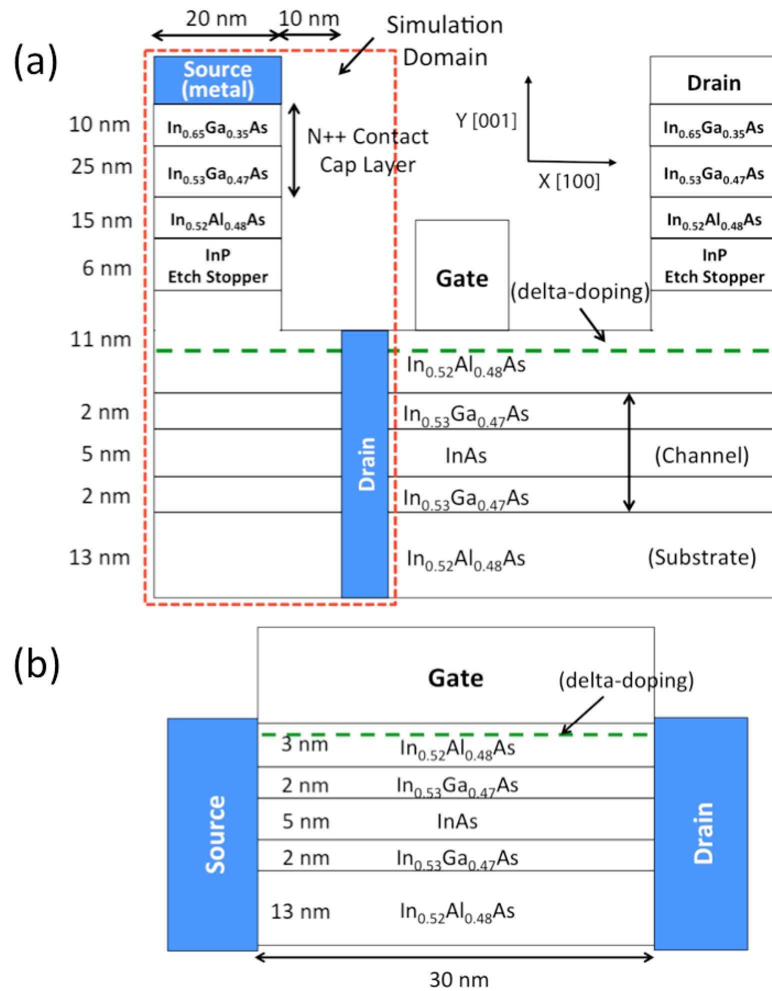

Fig. 3.1 (a) Device schematic of InAs QWFET device structure, and 2-D simulation domain of L-shaped hetero-contact structure. (b) The intrinsic device simulation domain with a gate length of 30 nm.

Since the theoretical modeling of nano-scale structures demands a proper treatment of quantum effects such as the energy-level quantization caused by quantum confinement and band structure non-parabolicity, a 2-D / 3-D quantum transport solver based on a self-consistent solution of the non-equilibrium Green's function (NEGF) and Poisson equations using the real-space effective mass approximation is used. To treat electron-phonon scattering the scattering self-energy is calculated in the self-consistent Born approximation assuming bulk phonon parameters based on deformation potential

theory [55]. Also, the non-parabolicity of the band structure is accounted for by extracting the effective masses from a sp3d5s* tight-binding (TB) band structure calculation including spin-orbit coupling for confined thin layers such as InP and InAs. For example, 5nm thickness of InAs channel layer where the electrons are strongly confined has $m_t = 0.0488m_0$ and $m_l = 0.096m_0$ instead of the bulk masses ($m_{bulk} = 0.023m_0$).

In the L-shaped structure, electron transport occurs along the <010> crystal of y-axis to the <100> crystal direction of x-axis at room temperature, 300K. The Schottky barrier height (Φ_B) between metal and $In_{0.65}Ga_{0.35}As$ contact pads is set to 0.2 eV. To calculate the contact resistance, a very small bias of 10 mV is applied across the device to drive the electron flow near to the equilibrium. The metal region is not included in the Poisson equation because the potential variation inside the metal region becomes insignificant due to very high electron concentrations. This modeling approach has been employed in recent works, which provided good agreement with experimental results [49, 51-52]. Fig. 3.2 shows the electrostatic potential profile of semiconductor contact pad model, and Schottky barrier height (Φ_B) is set to 0.2 eV with $N_D = 3\times10^{19}$ cm^{-3}. The typical parallel processing computation time is about 360 hours on 512 cores on two 2.1 GHz 12-core AMD Opteron 6172 processor [36] for each single bias point for the whole L-shaped simulation domain. This modeling approach is extremely time consuming.

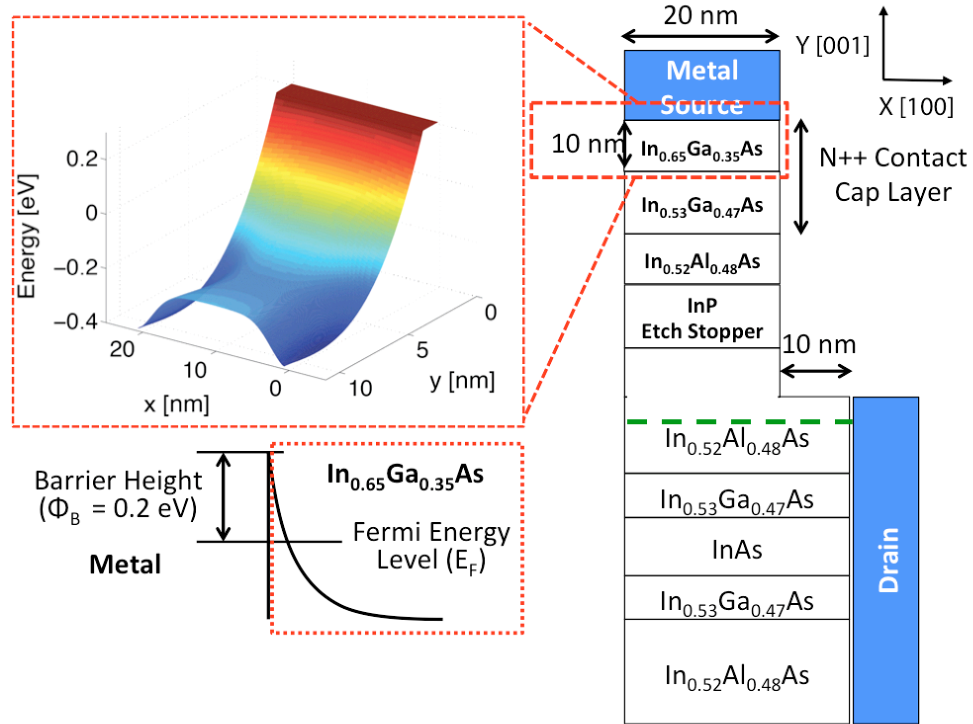

Fig. 3.2 Schottky barrier between metal and $In_{0.65}Ga_{0.35}As$ contact pad - electrostatic potential profile of semiconductor contact model, and Schottky barrier height (Φ_B) is set to 0.2 eV with $N_D = 3\times10^{19}$ cm^{-3}.

3.4 Results and Discussion

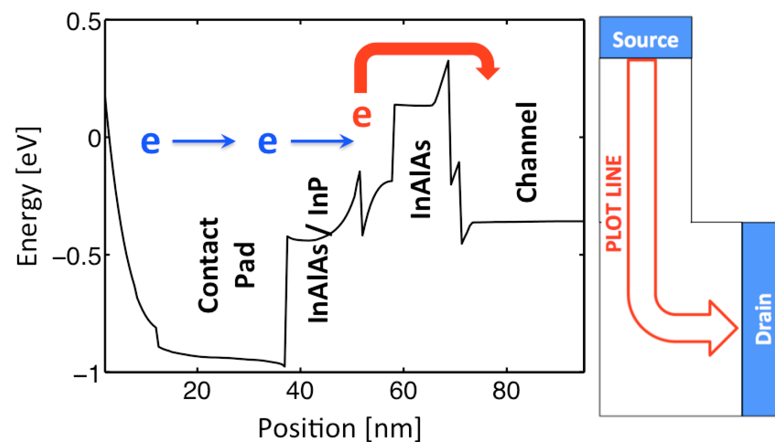

Fig. 3.3 Energy band diagram of 2-D contact-to-channel region simulation domain along electron marked as ‘e’ transport direction (plot line is shown in the right).

Various layers stacked in the L-shaped contact-to-channel region of InAs QWFET result in different band offsets, and they create multiple barriers along the electron transport direction as shown in Fig 3.3. The energy band diagram starts from the top $In_{0.53}Ga_{0.47}As$ contact pad (the left end) to the bottom $In_{0.53}Ga_{0.47}As$ / InAs / $In_{0.53}Ga_{0.47}As$ channel (the right end) as electrons flow from the contact to the channel. Due to the thick and high $In_{0.52}Al_{0.48}As$ barrier between InP etch stopper and $In_{0.53}Ga_{0.47}As$ / InAs channel, thermal assistance is required to fill states over the barrier in hetero-structure device. With the thermal assistance from the electron-phonon interactions, electrons could flow over the $In_{0.52}Al_{0.48}As$ barrier.

Fig. 3.4 (a) shows electron density profile and energy band diagrm with electron-phonon interactions and drain bias = 10 mV with Schottky barrier height = 0.2 eV, and Fermi energy level (E_F) is set to 0 eV in source. The electron density profile shows that most electrons reside the regions above the thick $In_{0.52}Al_{0.48}As$ barrier between InP etch stopper and $In_{0.53}Ga_{0.47}As$ layers, and electrons are strongly confined within the $In_{0.53}Ga_{0.47}As$ / InAs quantum well. Electron density spectrum in Fig. 3.4 (b) describe that electrons are well-thermalized, and their presence is observed in the overall contact-to-channel simulation domain.

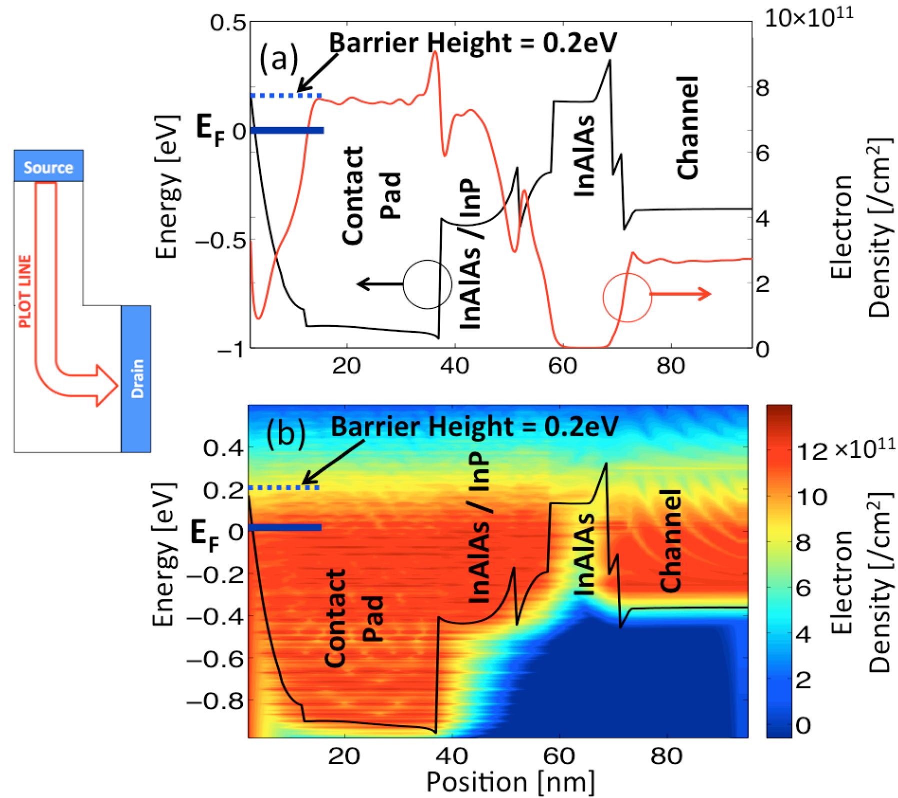

Fig. 3.4 (a) electron density profile and energy band diagram. (b) electron density spectrum and energy band diagram along electron transport direction (plot line in the left).

One can expect that the behavior of electron carriers is different at the low and high bias conditions. Fig. 3.5 (a) shows that high drain bias indeed lowers the $In_{0.52}Al_{0.48}As$ barrier between InP etch stopper and $In_{0.53}Ga_{0.47}As$ / InAs channel regions. The lowered barrier results the flow of electron carriers over the barrier as shown in electron density spectrum in Fig. 3.5 (b). This simulation results indicate that high contact resistance of InAs QWFET is mainly caused by the $In_{0.52}Al_{0.48}As$ barrier. It is clear that to make a thinner $In_{0.52}Al_{0.48}As$ barrier will result lower contact resistance, but the $In_{0.52}Al_{0.48}As$ barrier naturally exists as an insulator. Hence, as the insulator layer becomes thinner, the electron tunneling probability from the gate into the InAs channel region in the intrinsic device simulation domain shown in Fig. 3.1 (b). In short, it must result the severe gate leakage current [16].

Another important factor is Schottky barrier between metal and $In_{0.65}Ga_{0.35}As$ contact pads, because it is now clear that both $In_{0.52}Al_{0.48}As$ barrier between InP and $In_{0.53}Ga_{0.47}As$ layers and the Schottky barrier, which have the first and second highest barrier heights, are main factors determining the overall system conductance. As a consequence, this structural effect on the contact series resistance is a key finding of this paper.

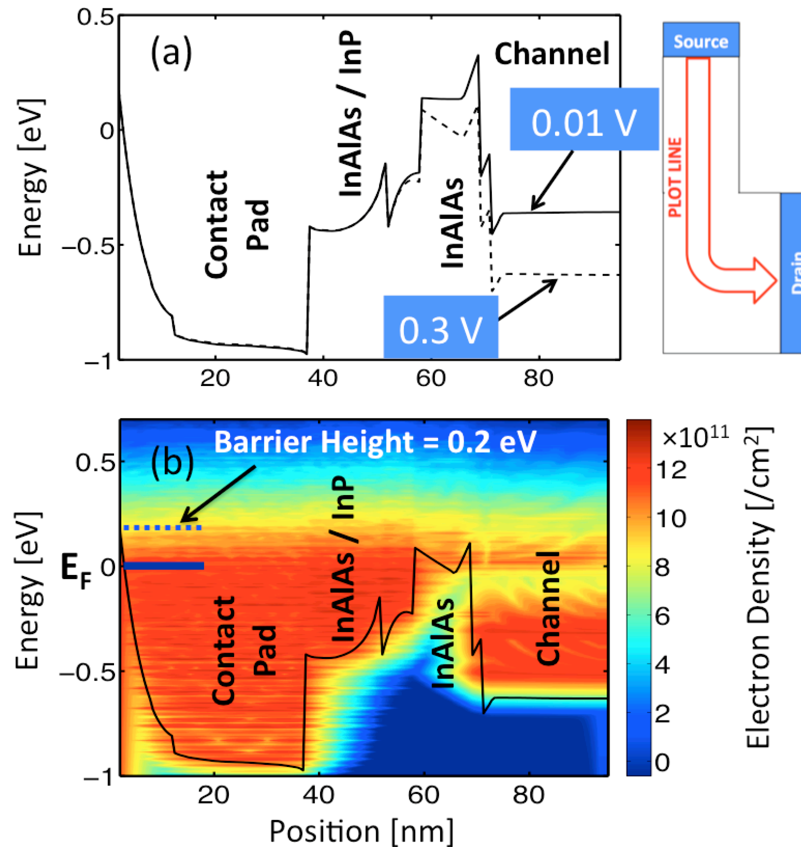

Fig. 3.5 (a) Energy band diagram in the curved contact geometry at low drain bias, 0.01 V (left) at high drain bias, 0.3 V (right) (b) electron density spectrum at low drain and high drain biases.

In this III-V QWFET, the $In_{0.52}Al_{0.48}As$ barrier between InP and $In_{0.53}Ga_{0.47}As$ layers is used as an insulator of InAs QWFET, and the Schottky barrier between metal and $In_{0.65}Ga_{0.35}As$ contact pads becomes the only factor can be engineered.

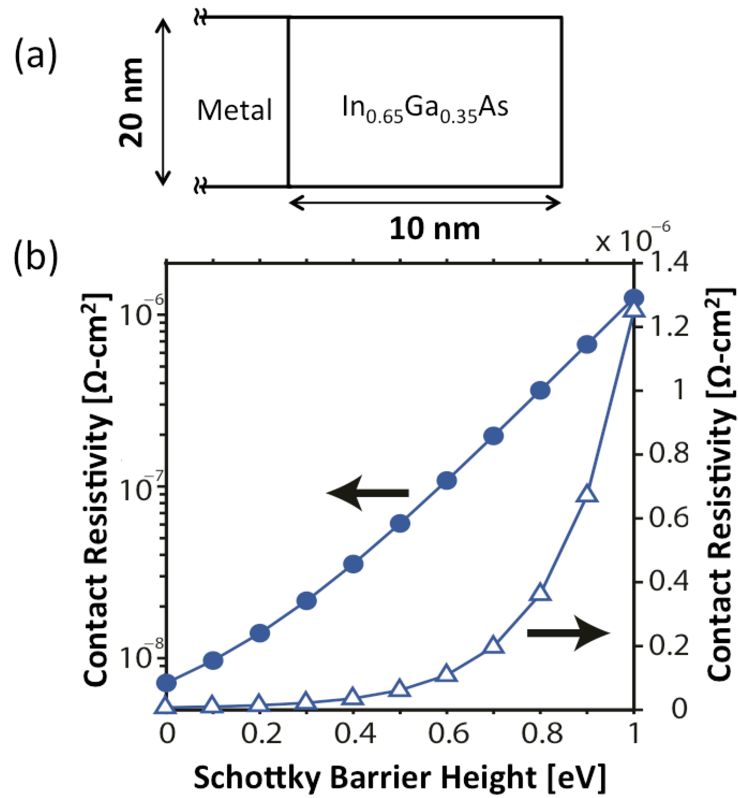

Fig. 3.6 (a) Schematics of simulated 2-D metal-semiconductor junction structure (b) Simulated contact resistivity vs. different Schottky barrier heights (0.0 eV, 0.2 eV, 0.4 eV, 0.6 eV, 0.8 eV, and 1.0 eV) with applied bias = 10 mV and $N_D = 3\times10^{19}$ cm^{-3}. (log scale in the left on y-axis - solid label and linear scale in the right on y-axis - open label)

It is known that the Schottky barrier height between metal and semiconductor contact pads can be varied by changing the doping concentrations near the metal-semiconductor interface region or by applying the new metal material facing to the semiconductor pad. To check the impact of the barrier height, a simple 2-D metal-semiconductor junction structure is chosen as shown in Fig. 3.6 (a). The length of the junction structure is 10 nm, and the width is set to 20 nm. Electron transport occurs along <100> crystal axis at room temperature, 300K. The doping concentration (N_D) in the semiconductor pad is set to 3×10^{19} cm^{-3}, which is equal to the experimental doping concentration,. The Schottky barrier height (Φ_B) is varied from 0 eV to 1.0 eV. As shown in Fig. 3.6 (b), as the barrier height increases, current is exponentially reduced. The lower

Schottky barrier height indeed drives higher current injection from the metal into the semiconductor.

In this work, the Schottky barrier height is initially set to 0.2 eV in the L-shaped contact, and the extracted contact resistance from the numerical simulation is 203 Ω-μm which is close to experimental value of source contact resistance, 230 Ω-μm [52-53]. As discussed earlier, the extracted series resistance can be included in a post processing step to the acquired I_D-V_{GS} characteristics from the intrinsic device simulation domain shown in Fig. 3.1 (b) where the intrinsic $V_{GS}{}^{*}{}_{,in}$ = $V_{GS,ext}$-I_DR_S and $V_{DS}{}^{*}$=$V_{DS,ext}$-$I_D(R_S+R_D)$ account. From a modeling perspective, two extrinsic parts of source and drain sides have the equal structures. Hence, the equal source and drain contact resistances (R_S=R_D) can be assumed. This method is applied, and achieved results show a good quantitative match with experimental I_D-V_{GS} data obtained from the InAs QWFET with gate lengths of 30 nm as shown in Fig. 3.7 [53].

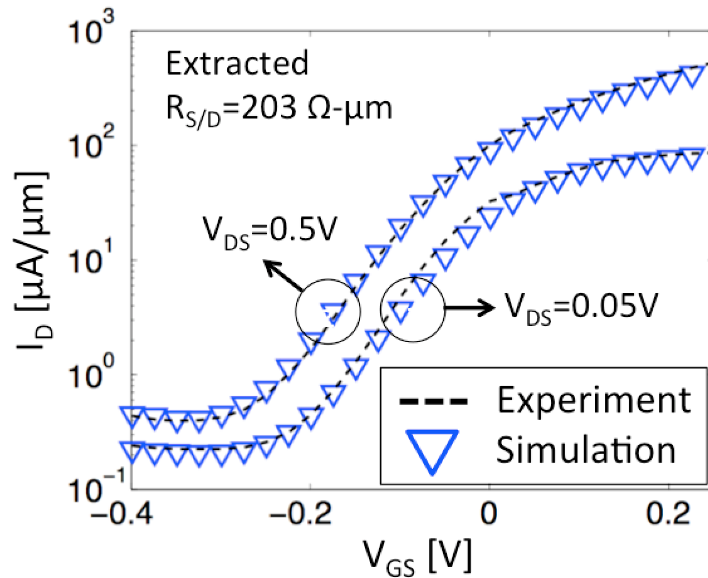

Fig. 3.7 Simulated I_D-V_{GS} characteristics for 30nm channel length of InAs QWFET with measured series resistance ($R_{S/D}$) for two given drain voltage V_{DS} = 0.05 V and 0.5 V with different gate voltages V_{GS} from -0.4 V to 0.3 V.

3.5 Conclusion and Outlook

This work offers an alternative approach to the conventional assumption of a lumped contact resistance that is assumed from experimental data or the ITRS roadmap. Here the contact series resistance is directly computed in a complex heterostructure-based, L-shaped contact-to-channel region. A computationally intense physics-based non-equilibrium quantum transport formalism (NEGF) is used to model phonon mediated electron flow across heterostructures and different carrier directions. The key finding for the specific devices is that the contact-to-channel resistance in InAs QWFET is mainly caused by structural reasons: 1) $In_{0.52}Al_{0.48}As$ between InP etch stopper and $In_{0.53}Ga_{0.47}As$/InAs channel and 2) Schottky barrier between metal and $In_{0.65}Ga_{0.35}As$. The extracted contact resistance is close to experimental value. However, there is still a gap between simulated and experimental contact resistance values because of yet unaccounted factors such as surface roughness and electron-electron interaction within actual size of contacts (1-2 μm). The inclusion of all these additional effects is at this stage prohibitively expensive in the computational requirements, and electron-electron scattering specifically has not been treated ever in NEGF based simulations. Despite the incompleteness of the present scattering model, we believe we are able to provide significant insight into the carrier flow through contact regions and guide experimental designs.

4. LOW FIELD EFFECTIVE MOBILITY EXTRACTION OF III-V ULTRA-THIN-BODY WITH DEFORMATIONAL POTENTIAL PHONON SCATTERING

4.1 Introduction

To keep improving the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs) as channel lengths shrink, novel device concepts and/or better materials than Si are required. The extraordinary electron transport properties of III-V compound semiconductors like InGaAs or InSb make them ideal candidates to replace conventional Si MOSFETs in low power and high frequency logic applications at the end of the road map [1]. However, the exact ballisticity of the III-V compound semiconductor is uncertain yet, it is difficult to determine what will be the best material for nanoscale transistors.

4.2 Modeling and Simulation Approach

In this work, we aim to extract effective mobility and the effective mobility will be used for the projection of ballisticity of III-V nano-scale transistors from numerical device simulations without complicated fabrication processes of multiple device prototypes. $In_{0.53}Ga_{0.47}As$ double-gate planar ultra-thin-body (UTB) is used, and the device schematic is shown in Figure 4.1.

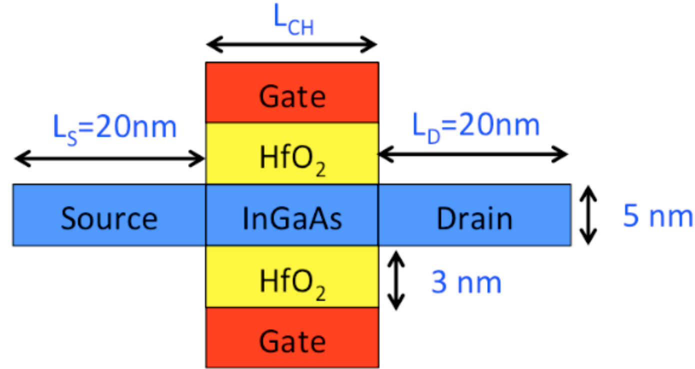

Figure 4.1 The schematic diagram of III-V ultra-thin-body nano-scale transistor. EOT is set to 0.595 nm, and source / drain regions are n-doped with a donor concentration N_D = 5×10^{19} cm^{-2}. Channel length (L_{ch}) is varied in the simulation.

The two-dimensional real space effective mass simulation model of the nano-scale transistor includes a proper treatment of quantum effects such as the energy-level quantization and band structure non-parabolicity. The transport effective masses m_t (0.064 m_0) for the $In_{0.53}Ga_{0.47}As$ channel layer are extracted by fitting the curvature of the lowest TB conduction band with a parabola. The confinement effective masses m_C (0.087 m_0) are chosen so that the energy difference between the two lowest TB conduction bands is reproduced by the effective mass model. Quantum transport simulation is operated in the presence of deformation potential electron-phonon scattering within the non-equilibrium Green's function (NEGF) and the Poisson equation self-consistency [55] at very low drain-to-source bias $V_{DS}=1\times10^{-5}$V and different gate-to-source biases V_{GS}.

When electron-phonon scattering is enabled, electrons in the device are well-thermalized and scattered in the source and drain regions as shown in Figure 4.2. Since a scalar deformation potential for the phonon scattering is used [56], and the scattering rate for acoustic deformation potential scattering can be expressed as shown in the equation (4.1),

$$\frac{1}{\tau(p)} = C\frac{q\pi V_t D_A^2}{\hbar\rho u_l^2} g_C(E) \tag{4.1}$$

The scattering rate is composed of the sound velocity (u_l), mass density (ρ), deformation potential (D_A) and V_t equals to kT. g_C(E) is the density of states. In the simulation, C works as a fitting constant to adjust coupling strength at very low drain bias condition. The optical deformation potential scattering can be expressed as below equation (2). However, only carriers with any energy exceeding a phonon energy ($\hbar\omega_O$) can emit optical phonons, and the simulations in this work are operated at very low field ($V_{DS}=1\times10^{-5}$V) which stays at far below $\hbar\omega_O$.

$$\frac{1}{\tau(p)}=\frac{q(\hbar/q)\pi D_O^2}{2\rho\hbar\omega_O}(N_O+1/2\mp1/2)g_C(E\pm\hbar\omega_O) \quad (4.2)$$

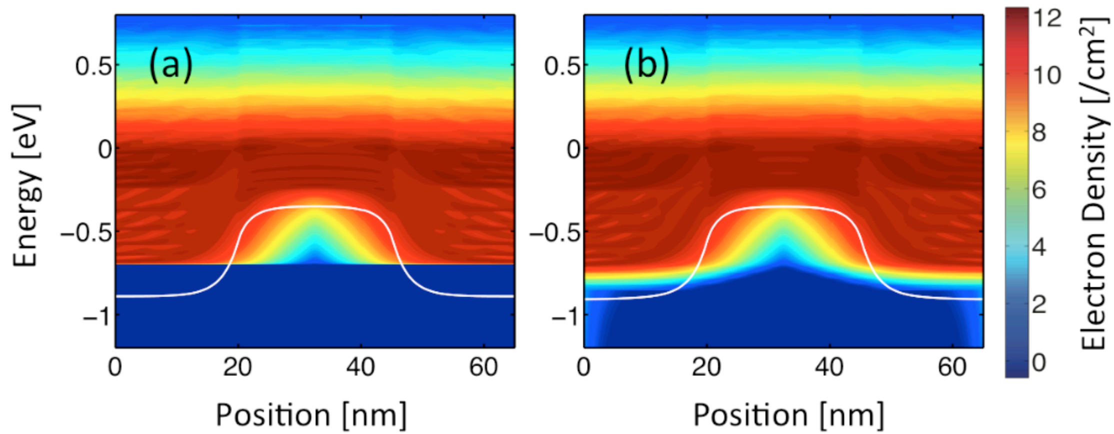

Figure 4.2 The electron density and conduction band edge of InGaAs UTB transistors from the source to the drain at L_{ch}=25nm (a) in ballistic regime (b) with electron-phonon scattering.

To extract phonon-limited and ballistic resistances is essential to calculate effective mobility. Total resistance (R_T) is the sum of ballistic resistance (R_0) and phonon-limited resistance (R_{ph}), and R is proportional to the effective mobility (cm^2/V.s) as shown the below equation (4. 3),

$$\mu=\frac{L_{ch}}{R}(\frac{1}{qN_{inv}}) \quad (4.3)$$

q is elementary electron charge of 1.602×10^{-19} C. The calculated resistance (R) is in unit of Ω-μm, and the inversion charge (N_{inv}) is extracted at the top of the energy barrier as shown in Figure 4.3.

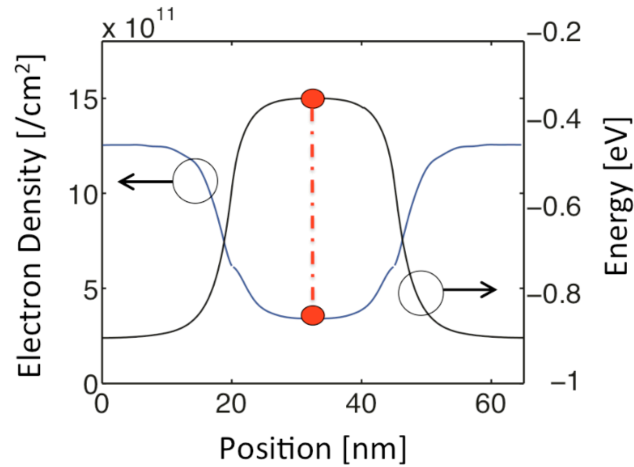

Figure 4.3 The electrostatic potential along the transport direction and electron density profile at the top of the energy barrier in InGaAs UTB transistors with L_g=25nm at V_{GS}=0.7V and V_{DS}=1×10^{-5}V.

4.3 Results and Discussion

The extracted ballistic resistance (R_0) and total resistance (R_T) are shown in the Figure 4 (a). When channel length (L_{ch}) becomes shorter than 25 nm, the R_0 starts decreasing due to source-to-drain tunneling and short channel effects in the InGaAs double-gate planar FET. Hence, it is important to keep device channel length longer than 25nm to exclude tunneling effects for precise effective mobility extraction, and it demands high computation cost.

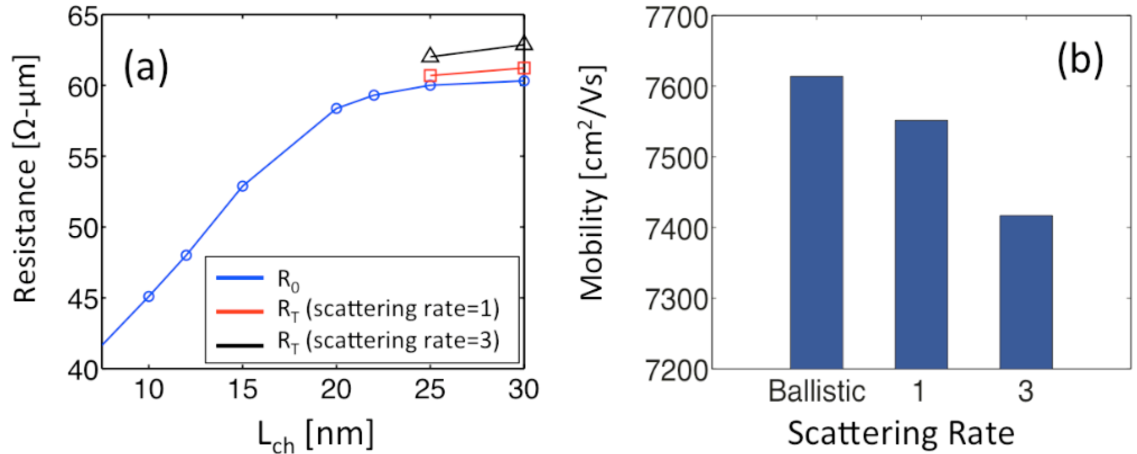

Figure 4.4 (a) Ballistic resistance (R_0) and total resistance (R_T) as a function of the device length (L_{ch}) at V_{GS}=0.7V and V_{DS}=1×10^{-5}V. (b) Calculated effective mobility per fitting constant (C) in equation (1) to adjust coupling strength with n-type InGaAs DG UTB at Lg=25nm.

The total resistance as scattering rate increases, and Figure 4.4 (b) shows that the mobility degradation occurs when total resistance increases in n-type InGaAS DG UTB at L_g=25nm. The average computation cost for a simulation is about 48 hours with 480 cores on two 2.1 GHz 12-core AMD Opteron 6172 processor for each point of I-V characteristics [57].

The effect of electron-phonon scattering is being studied to project the device performance and to find a way to improve the mobility for the future technology nodes. The electron-phonon scattering can impact the mobility degradation which is directly related to device performance. The simulation results can be used for the effective mobility calibration with available experimental data. However, it should be noted that the simulated device is simple compared to realistic structure, and only electron-phonon scattering is included.

5. SCALING EFFECT ON SPECIFIC CONTACT RESISTIVITY IN NANO-SCALE METAL-SEMICONDUCTOR CONTACT

5.1 Abstract

As devices are downscaled to nanoscale dimensions, contact series resistance takes larger fraction of the total on-state series resistance. To aid the development of improved low contact resistance technologies, there is a need to understand the factors affecting the interface resistance of the nanometer scale contacts. This work investigates the effects of contact geometry with a presence of Schottky barrier on the specific contact resistivity of the metal-semiconductor interface. The contact resistivity is calculated using a 2-D / 3-D quantum transport simulator that solves non-equilibrium Green's functions (NEGF) transport and Poisson equations self-consistently within a real-space effective mass approximation. The sp3d5 empirical tight-binding method is employed to obtain the ballistic conductance of pure metal nanowire (Cu). The key finding of this work is that the specific contact resistivity increases when metal-Si interface area reaches to certain limit (under 5 nm in 2-D and 5×5 nm^2 in 3-D) due to the reduced number of discrete modes available for conduction across the Schottky barrier. The key finding of this work is that the downscaling of metal-semiconductor actually does not affect the specific contact resistivity reduction once the quantum effects are correctly treated in the ballistic transport regime. The absolute magnitude of this scaling effect can be mitigated by reducing the Schottky barrier.

5.2 Introduction

As aggressive downscaling of Si CMOS technology reaches to sub-10 nm technology nodes, it results various challenges characterized as short channel effects such

as DIBL and source-to-drain tunneling. Recent researches show that the contact series resistance is becoming a performance limiting factor in nano-scale electronics as it adversely takes larger fratction of the total on-state resistance while downscaling [1, 13, 16, 49]. Hence, the contact resistance must be reduced to meet ITRS requirements of future technology nodes [1].

The series resistance is composed of metal-semiconductor contact resistance, spacer extension resistance, tip resistance, and spreading resistance. Specific contact resistivity (ρ_C) is one of the important factors affecting the total contact resistance, and it is determined by important factors such as metal-semiconductor Schottky barrier height and semiconductor doping. It is expected that the ITRS requirements on the specific contact resistivity can be met by applying high doping concentrations to the contact pad region. However, if metal-semiconductor (M-S) contact region reaches to the certain scaling limit (sub-10 nm) for further downscaling, it is questionable the contact resistivity still can meet the ITRS requriements. In addition, the effect of additional dimensionality on the contact resistivity is expected to be different in 2-D and 3-D structures, especially when 3-D structures are scaled down to sub-10 nm sizes. These various effects on specific contact resistivity should be studied from the modeling perspective prior to designing optimized contact structure for future technology nodes.

In this work, the specific contact resistivity is calculated with a presence of Schottky barrier and the highly doped semiconductor contact pad at the M-S junction structure in the ballistic transport regime. We investigate factors affecting the specific contact resistivity when metal interconnect wire is downscaled under 10 nm in 2-D and 10×10 nm^2 in 3-D.

5.3 Device Description and Simulation Approach

To understand the basic physical processes contributing to the contact resistivity, simple 2-D and 3-D M-S junctions are chosen as shown in Fig. 5.1 (a). The length of the M-S junction structure is 5 nm, and electron transport occurs along <100> crystal axis at room temperature, 300K. The doping concentration (N_D) in the semiconductor pad is

varied from 1×10^{20} cm^{-3} to 5×10^{20} cm^{-3}. The Schottky barrier height (Φ_B) is varied from 0 eV to 0.5 eV. In 2-D structures, the width of metal wire, which determines the contact area, is changed from 10 nm to 2.4 nm while the width of silicon wire is fixed at 15 nm. The cross-section of metal wire is varied from 10×10 nm^2 to 2.4×2.4 nm^2 while silicon wire cross-section is fixed at 10×10 nm^2 in 3-D structures.

The theoretical modeling of nanoscale structures demands a proper treatment of quantum effects such as the energy-level quantization caused by quantum confinement. Hence, a 2-D / 3-D quantum transport solver based on a self-consistent solution of the non-equilibrium Green's function (NEGF) and Poisson equations using the real-space effective mass approximation is used to simulate the M-S junctions. To calculate the specific contact resistivity (ρ_C), a small bias of 10 mV is applied across the device. The specific contact resistivity is calculated by multiplying the interface cross-section area to the resistance extracted from the ballistic transport simulation. Non-parabolicity effects are negligible and the standard effective mass model is sufficiently accurate at dimensions which are set to 15 nm for 2-D and 10×10 nm^2 for 3-D of Si contact pad.

The metal region is not included in the Poisson equation because the potential variation inside the metal region becomes negligible due to very high electron concentrations. This modeling approach has been employed in recent works, which provided good agreement with experimental results [3, 5-6]. Fig 5.1 (b) shows the electrostatic potential profile of semiconductor contact model, and Schottky barrier height (Φ_B) is set to 0.5 eV with $N_D = 2\times10^{20}$ cm^{-3}.

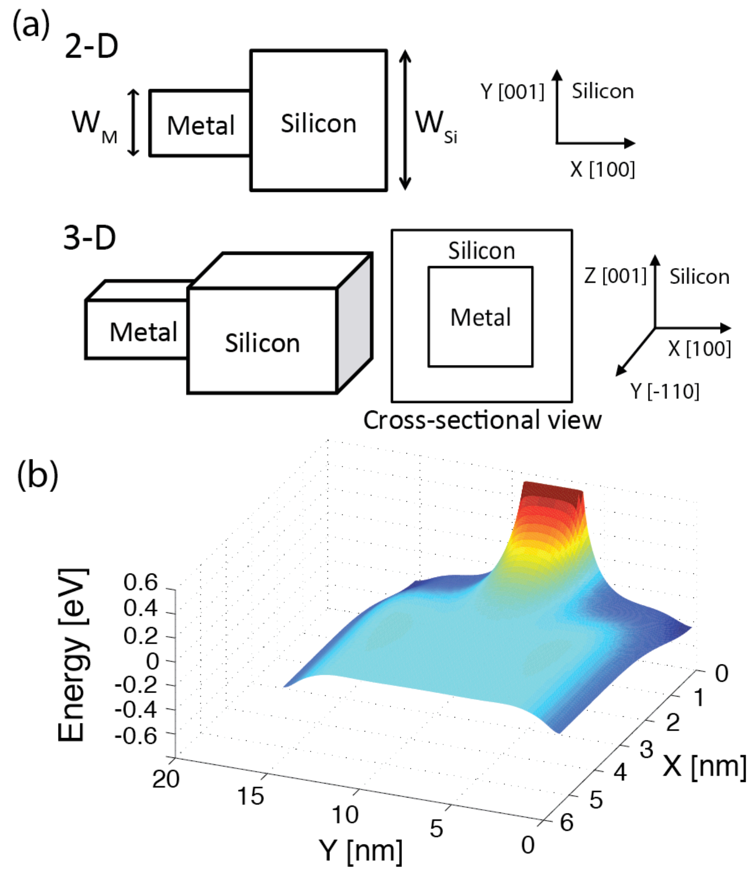

Figure 5.1 (a) Schematics of the simulated contact structures (b) Potential profile of a contact model (W_M = metal-silicon interface width = 3 nm, W_{Si} = silicon width = 15 nm) and Φ_B is set to 0.5 eV with $N_D = 2\times10^{20}$ cm^{-3}.

Fig. 5.2 indicates that a variation in the transport effective mass of m_X=0.4 from the typically expected value of 1.0 does not affect the transport results with different drain biases from 10 mV to 100 mV, and the calculated contact resistivity shows less than 10% deviation within the range of applied biases.

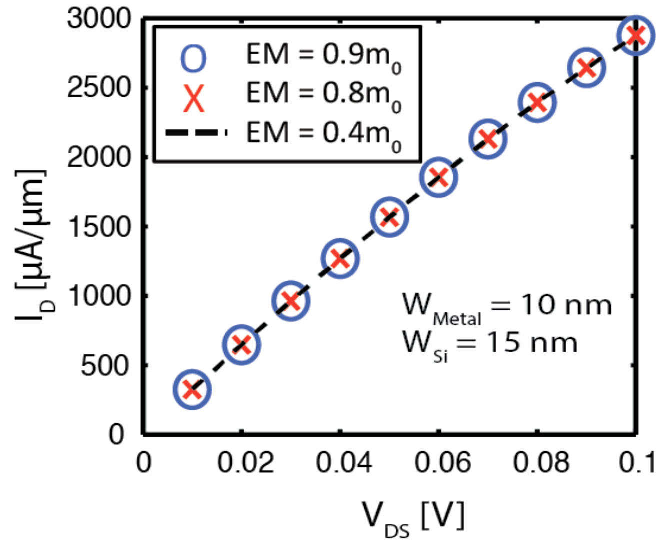

Figure 5.2 Current linearity check with different metal effective masses with the metal-semicondcutor structure (W_{Metal} = 10 nm and W_{Si} = 15 nm) with for $N_D = 2\times10^{20}$ cm^{-3}.

Electrons in bulk metals such as copper (Cu), silver (Ag), and aluminum (Al) behave as nearly free electrons, which can be described well using the effective mass model with free electron effective mass. To evaluate the validity of the nearly free electron model in the nanoscale metal wires, the sp^3d^5 second-nearest neighbor tight-binding model is used. The tight-binding model is fitted to the first principles augmented plane wave (APW) band structures of bulk Copper (Cu) [60-61]. The validity of the free electron model for other commonly used contact materials such as tungsten and silicides needs careful investigation but it is beyond the scope of the present work. Results presented here are therefore most relevant for free electron like metals such as Cu, Ag, and Al.

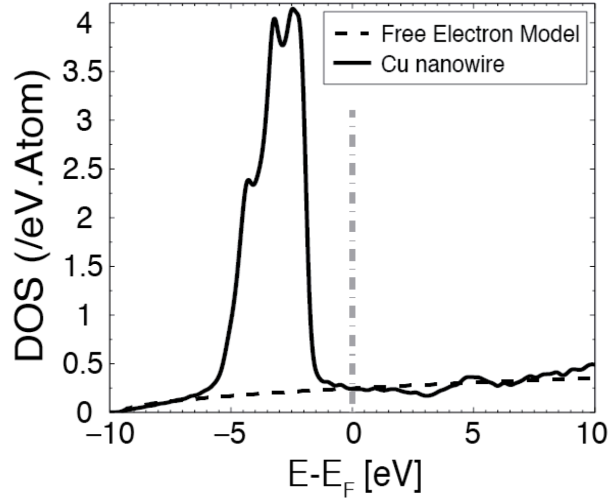

Figure 5.3 The density of states of a 2.4×2.4 nm^2 Cu wire from TB simulation.

Fig. 5.3 shows the density of states (DOS) of a 2.4×2.4 nm^2 Cu wire, which corresponds to the smallest metal contact studied in this work. The free electron DOS agrees well with the DOS calculated using the tight-binding model except in the energy range from [E_F − 6 eV] to [E_F − 2 eV], where the DOS is dominated by d-like electrons not accounted for in the free electron model. Hence, the electrons near the Fermi level mostly participate in the low bias transport regime indicating that the free electron model is a good approximation in the low bias transport regime.

In 3D nano-scale structures, the different dispersion relationship is resulted by the stronger quantum confinement. It means that the quantum transport simulation allows the specification of different directional effective masses and band degeneracies. Fig. 5.4 shows that the conductance decreases as the size of the metal wire decreases.

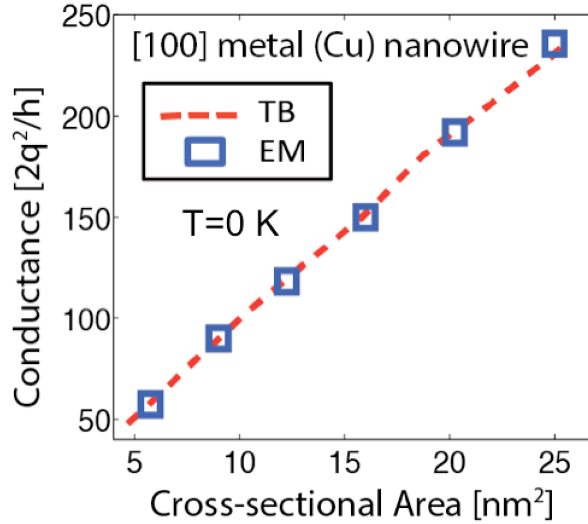

Figure 5.4 The ballistic conductance of [100]-oriented Cu wires as a function of cross sectional area calculated using the sp^3d^5 tight-binding model (TB) and effective mass model (EM).

Since the effective mass model used in the metal is properly tuned to a physically reasonable model as shown in Fig 5.4., it captures the linearity pattern of metal wire conductance while downscaling. For a fixed transport effective mass of m_X=0.4 we use the transverse confinement effective masses $m_Y = m_Z$ as fitting parameters. For metal wire cross sections of 2.0 nm, 3.0 nm, 3.5 nm, and 4.0 nm we find best fits to the number of modes for masses of m_Y=m_Z = 0.15, 0.13, 0.12, and 0,102, respectively. It should be noted that valley degeneracy was not varied across the channel. Since valley degeneracy for Si is 2 for each of the 3 valleys, same valley degeneracies for metal region was used as well. Nevertheless, the number of modes and DOS will be comparable to TB results.

5.3 Results and Discussion

The higher doping concentrations in the Si contact pad and lower Schottky barrier indeed result in a lower specific contact resistivity as shown in Fig. 5.5. This is because of the higher doping concentration in the Si contact pad results in a thinner Schottky barrier width as shown in Fig. 5.5 (a). The lower Schottky barrier height drives higher current density from the metal interconnect into the semiconductor as shown in Fig. 5.5

(b). Fig. 5.5 (b) also shows that the total current flow to the system is determined by the dimensions of the M-S interface.

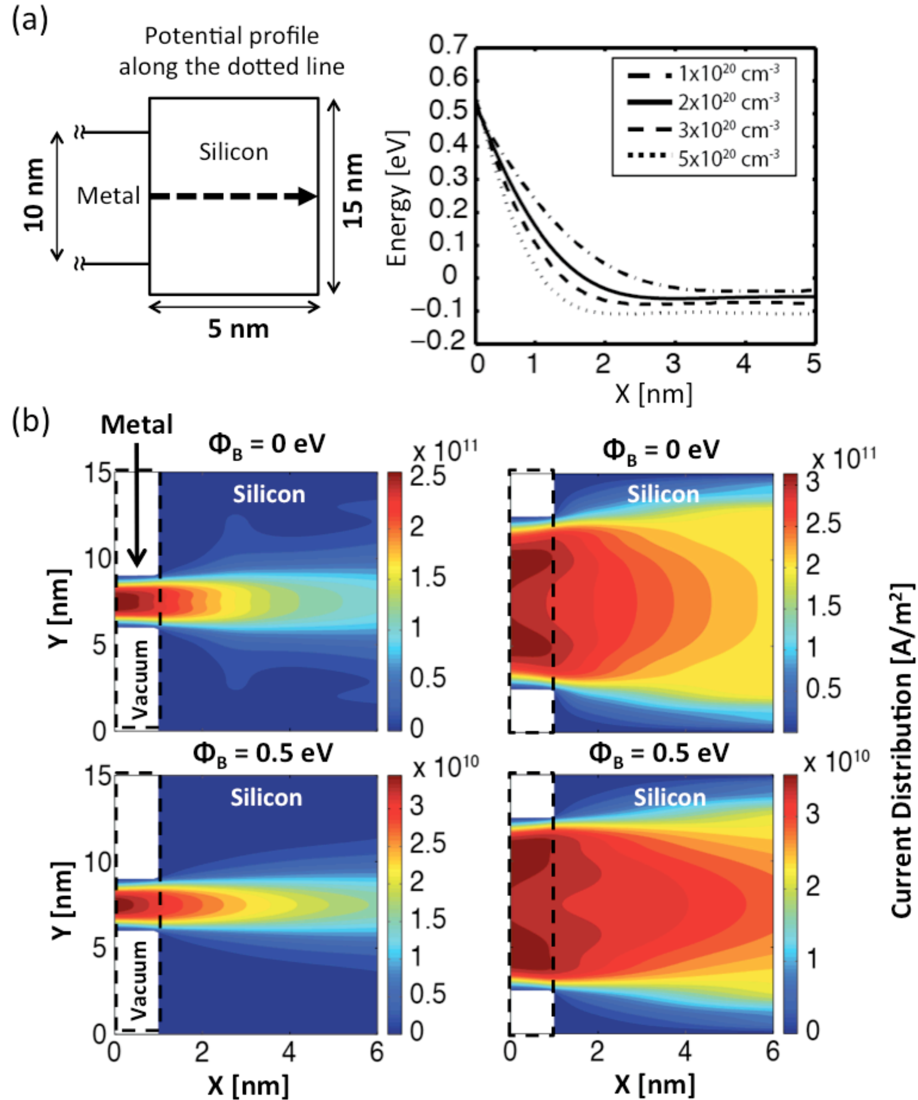

Figure 5.5 (a) The potential profiles along the middle of structure in the transport direction in different doping concentrations: $N_D = 1\times10^{20}$ cm^{-3}, 2×10^{20} cm^{-3}, 3×10^{20} cm^{-3}, and 5×10^{20} cm^{-3} with $\Phi_B = 0.5$ eV (b) The current density spectrum from metal wire (W_M = 3 nm (left) and 10 nm (right) with fixed W_{Si} = 15 nm) to silicon pad with Φ_B=0 eV and 0.5 eV and $N_D = 2\times10^{20}$ cm^{-3}.

However, it is important that the measured specific contact resistivity is not varied when the dimensions of the metal-semiconductor interface is decreased as shown in Fig.

5.6. The observed trend of scaling effect on the specific contact resistivity can be explained by invoking the concept of the total transmission. As a measure of conductance, the net current flowing from source to drain is computed as following equations,

$$I = \frac{2q^2}{h} \int dE \sum_n T(E) M(E) f(E_{FS} - E_{FD}) \tag{5.1}$$

where $2q^2/h$ is the quantum conductance. T(E) is the transmission probability, and M(E) is the number of transverse modes. Since a small bias, 10 mV, is applied across the device, the conductance can be expressed to the total transmission, ΣT(E)M(E). The transmission probability is not unity due to the Schottky barrier at M-S junctions. However, in structures with same barrier height, the only difference maker becomes M(E).

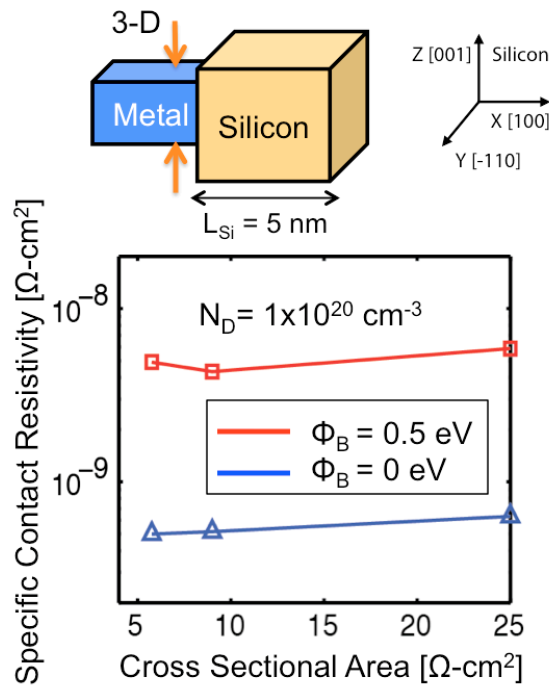

Figure 5.6 Simulated specific contact resistivity for 2-D and 3-D structures for two given doping concentration $N_D = 1 \times 10^{20}$ cm^{-3} with Φ_B=0 eV sand 0.5 eV in semi-log scale.

In short, this result can simply be explained by the concept of conductance between two different materials as following equation [9],

$$G = \frac{2q^2}{h} \int dE \sum_n T(E) \left(\frac{1}{\frac{1}{M_2(E)} - \frac{1}{M_1(E)}} \right) \tag{5.2}$$

When $M_1(E) > M_2(E)$, the total system conductance depends on M_2. Since metal is treated as an ideal carrier reservoir in the system, the number of modes of the affecting conductance of the system can be set to $M_{1,\ Si}$ in the Si contact pad and $M_{2,\ Metal}$ in the metal region. The number of modes, M(E), is approximately equal to the number of half electron wavelength (λ/2) that fit into the cross-section area (W). This fact gets rid of $M_{1,\ Si}$ from ρ_C scaling factors due to sufficient dimension of Si contact pad in the simulation model, and $M_{2,\ Metal}$ remains.

As shown in Fig 5.4., as the ballistic conductance of metal wire decreases linearly, $M_{2,\ Metal}$ does not affect the variation of conductivity reduction which results contact resistivity (ρ_C) reduction under the ballistic transport condition excluding all scattering mechanisms. If the effective mass model used in the metal was not properly tuned to a physically reasonable model, it is imposible to capture the conductance linearity pattern while downscaling of metal wire. Also, the absolute magnitude of this scaling effect can be mitigated by reducing the Schottky barrier. These are the key findings of this work. However, it is important to note that scattering effects such as surface roughness of metal wire and grain boundary condition mainly actually cause the conductivity degradation in the experimental study, but these scattering effects are excluded in this modeling work [62]. In order to obtain more qualitative observation, the interface should be treated in the atomic level, and the precise M-S interface parameters should be extracted by fitting the full-band TB band structures with band structures acquired from the density functional theory (DFT) [61, 64].

5.3 Conclusion and Outlook

Conventional device simulation with quantum transport model focuses on the device channel as it determines overall system conductance. There is still significant power dissipation in the channel region, but it is clear that contacts starts dominating the

overall device performance. It concludes that the boundary between contacts and channel can no longer be separated, and the contacts need to be included in the trajectory of future device simulations with proper treatments of quantum effects. Therefore, a precise theoretical modeling is required to advance future contact design to improve the overall performance. This work investigates the downscaling effect of metal-Si contact geometry on the specific contact resistivity. The key findings of this work are is that the downscaling of metal-semiconductor actually does not affect the specific contact resistivity reduction once the quantum effects are correctly treated in the ballistic transport regime. The absolute magnitude of this scaling effect can be mitigated by reducing the Schottky barrier.

6. CONCLUSIONS AND SUMMARY

6.1 Concluding Remarks

This thesis focuses on studying III-V and Si nano-scale transistors and nano-scale contacts. First, in preparation for the next technology node beyond 22nm technology node, this report assesses the performance of the $In_{0.75}Ga_{0.25}As$ of III-V semiconductor compounds and strained-Si channel nano-scale transistors with identical dimensions and electrical properties at 12nm technology node and below. The impact of the channel material property and device architecture on the ultimate performance of ballistic transistors is theoretically analyzed from a modeling point of view.

III-V MOSFETs make them ideal candidates to replace conventional Si MOSFETs, because III-V FETs benefit from a very high carrier mobility compared to Si, which enables high speed and low power logic applications. However, simulation results indicate that the $In_{0.75}Ga_{0.25}As$ FETs do not outperform strained-Si FETs, and triple-gate FinFETs surely represent the best architecture for sub-15nm gate contacts, independently from the material choice. This result proves that low density of states (DOS) of III-V FETs known as DOS bottleneck issue limits high charge density and high ON-current even with low effective masses resulting extremely high injection velocity. However, surface orientation can be engineered to obtain higher DOS. Electron transport in mixed Γ-L-valleys to III-V semiconductor compounds such as GaAs, GaSb, and AlSb has been proposed recently [64-65]. However, the impact of higher DOS still need to be investigated, because many more bands leads higher scattering rate as a trade-off.

The simulation results in chapter 2 further show that the overall device performance is strongly influenced by the source and drain resistances. The source and drain series resistances were negligible in the OFF state, but they significantly reduce the drain current in the ON state, by more than 50% in both III-V and Si nano-scale

MOSFETs. To improve the performance of III-V and Si FETs, optimization process of the extrinsic part of the device is essential. Experimentally, source and drain contact regions of III-V semiconductors have always been characterized by much larger series resistances than those of Si so far. Then, a precise theoretical approach is required to model the contact characteristics prior to the optimizaiton, and the basic physical behavior of contact region in InAs HEMT transistor is explored. The key result is that the contact-to-channel resistance is mainly caused by structural reasons such as barriers between multiple layers of the contact domain and Schottky barrier between metal and semiconductor contact pad. However, there are multiple scattering events such as surface roughness and electron-electron interaction within realistic contact size (1-2 μm). Once all these effects are counted, it is quite difficult to solve by using quantum transport solver due to extremely high computation cost. It may require more efficient way of contact region simulations to reduce the high computation cost and to account uncertainties from the multiple scattering events.

However, it is clear that the approximation of contact resistance from quantum transport simulation can be useful in the future technology nodes due to further downscaling of device contact region. While downscaling of central part of nano-scale devices reaching to its limit, contact region might a promising candidate which can contribute to the further downscaling. So far, conventional device simulation with quantum transport model focuses on the device channel as it determines overall system conductance. There is still significant power dissipation in the channel region, but it is clear that contacts start dominating the overall device performance. It concludes that the boundary between contacts and channel can not be separated, and the contacts need to be included in the trajectory of future device simulations with proper treatments of quantum effects.

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VITA

VITA

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