Fall 2014

Material and device aspects of semiconducting two-dimensional crystals

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Graduate School ETD Form 9
(Revised 01/14)

PURDUE UNIVERSITY
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By Han Liu

Entitled

MATERIAL AND DEVICE ASPECTS OF SEMICONDUCTING TWO-DIMENSIONAL CRYSTALS

For the degree of Doctor of Philosophy

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MATERIAL AND DEVICE ASPECTS OF SEMICONDUCTING TWO-DIMENSIONAL CRYSTALS

A Dissertation

Submitted to the Faculty

of

Purdue University

by

Han Liu

In Partial Fulfillment of the

Requirements for the Degree

of

Doctor of Philosophy

December 2014

Purdue University

West Lafayette, Indiana

To my parents,

Dajian Liu and Bingyi Pan

ACKNOWLEDGMENTS

First and foremost, I would like express my deepest gratitude to my thesis advisor, Prof. Peide D. Ye. Looking back to the day I arrived at Purdue, every single step of my progress I have made in the past years is with his continuous support and efforts. He is one of the smartest people I have ever met in my pursuit of knowledge. His kind and cheerful demeanor has been an inspiring guidance to my life. Remarkably, I was fully impressed by his encouragement for the students to explore a range of new topics. I have been very fortunate to have been part of his illustrious research group. The years with his group has been an enjoyable experience in my life.

I would also like to express my sincere gratitude to Prof. Mark S. Lundstrom, Prof. Muhammad A. Alam and Prof. Yong P. Chen, who have been serving as my committee members. I have been greatly benefited from their experimental help and valuable discussions during my graduate study at Purdue.

I am indebted to Prof. Xianfan Xu, Prof. Jun Lou (Rice University), Prof. David Tománek (Michigan State University) and Prof. Lance Li (Academia Sinica) for their support in experiments and simulations. I really enjoy the collaborations.

I have been fortunate to have the support of all my group members I have been working with: Dr. Min Xu, Dr. Jiangjiang Gu, Dr. Chen Wang, Dr. Lin Dong, Dr. Xuefei Li, Dr. Adam T. Neal, Kun Xu, Nathan J. Conrad, Heng Wu, Jingyun Zhang, Mengwei Si, Yuchen Du, Hong Zhou, Lingming Yang, Yexin Deng and Wei Luo. It has been a good memory for me to share the years with you at Purdue.

Finally, no words would ever do justice to express my deepest thanks and gratitude to my parents and my family. Their unconditional love, tolerance, sacrifice and encouragement have been the best supports in my life ever.

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ABBREVIATIONS

TMD	transition metal dichalcogenides
SCE	short channel effect
MOSFET	metal-oxide-semiconductor field-effect transistor
ALD	atomic layer deposition
FLP	Fermi-level pinning
CVD	chemical vapor deposition
CMOS	complimentary metal-oxide-semiconductor
EOT	equivalent oxide thickness
CNT	carbon nanotube
SS	subthreshold swing
S/D	source/drain
UTB	ultra-thin body
EOT	equivalent oxide thickness
h-BN	hexagonal boron nitride
TMA	trimethylaluminum
AFM	atomic force microscope
SEM	scanning electron microscope
DFT	density function theory
NEGF	non-equilibrium Green function
CNL	charge neutrality level
DIBL	drain induced barrier lowering
BOE	buffered oxide etchant
TLM	transmission line method
SBH	Schottky barrier height

MBE	molecular beam epitaxy
DIBN	drain induced barrier narrowing
PL	photoluminescence
VTC	voltage transfer characteristics

ABSTRACT

Liu, Han Ph.D., Purdue University, December 2014. Material and Device Aspects of Semiconducting Two-Dimensional Crystals. Major Professor: Peide D. Ye.

Two-dimensional (2D) crystals have attracted much attention in recent years due to their unique physical, chemical, and mechanical properties. Semiconducting 2D crystals with van der Waals structures, such as transition metal dichalcogenides, are considered promising candidates for future device applications, as many have large band gaps, high carrier mobilities, and enable devices with immunity to short channel effects in addition to compatibility with silicon CMOS processes.

In this thesis, the fundamental device implications of using semiconducting 2D crystals are investigated. This includes: 1) the optimization of device fabrication processing for better device performance, 2) comparing the device physics in 2D semiconductors based transistors and silicon MOSFET, and 3) circuit-level integration of devices using 2D semiconductors. A direct atomic layer deposition process was developed and investigated on various 2D crystals which allowed for the development of 2D semiconductor transistors. N-type MoS_2 transistors with top and back gates were fabricated. The device performance of MoS_2 transistors with various channel lengths down to 50 nm was studied. Metal contacts on MoS_2 and other TMD materials were also studied. They showed a strong Fermi-level pinning at the metal MoS_2 interface. Device performance based on single layer CVD MoS_2 channel was studied and the device on/off switching was revealed to be dominated by Schottky barriers at metal contacts. Finally, the transport properties and device performance of p-type phosphorene crystals were investigated. Semiconducting 2D crystals are very promising candidates for future electronic and optoelectronic device applications.

1. INTRODUCTION

This chapter provides an introduction to the motivation of research on 2D crystals, the current status of device research on 2D crystals, and key findings in this thesis.

1.1 Scaling of Si MOSFETs

In the past several decades, the development of semiconductor industry has tremendously changed the lifestyles of human beings. The size of our electronic devices, such as cellphones, laptops, tablets, is getting smaller, while more functionalities are implanted. This is benefited from the more advanced fabrication techniques, where more transistors can be integrated in one chip. This trend was predicted early in the 1960s by Gordon Moore, one of the co-founder of the Intel Corporation. The "Moore's Law", described as "the number of transistors on integrated circuits doubles approximately every two years", has been serving as the guideline of semiconductor industry in the past fifty years. The number of transistors in a processor has been ramped up from 2,300 with a feature size $\sim$10 μm (Intel 4004, 1969) to 5 billions with a feature size down to 22 nm (Intel Core i7, 2013).

As the feature size of silicon transistors is approaching the quantum limit, new approaches have been made to further extend the "Moore's Law". Figure 1.1 shows the process technologies as we continue the pace in scaling down of the transistors from the ITRS road map. [1] Three changes have been made on the device level. The first change is the gate stack, where metal gate and high-k dielectric has replaced conventional poly-Si/SiO_2. This decreases equivalent oxide thickness (EOT) while maintain similar physical oxide thickness to restrain leakage current. Second, the device structure has been changed from planar devices to 3D transistors, or FinFETs, to enhance the electrostatic control. The third change comes from the substitution

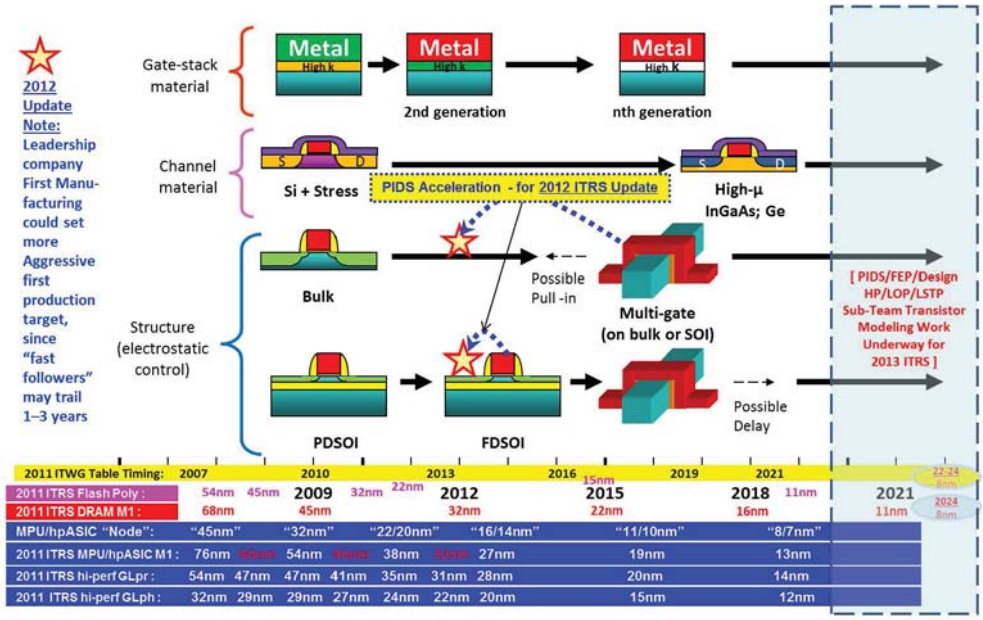

Fig. 1.1. Scaling trend of Si MOSFETs from ITRS 2012

of channel material. Given the ITRS prediction, Ge and InGaAs will replace stressed silicon in 2018, due to their higher carrier mobilities than those in silicon.

1.2 Semiconducting 2D Crystals

The layered material family has provided more options to the channel material for future electronics. The typical example of 2D material is graphene, first discovered in 2004, and has been demonstrated with ultra-high carrier mobility up to 200,000 $cm^2/V{\cdot}s$. [2, 3] However, the absence of a band gap in graphene limits its further application in digital circuits. Semiconducting 2D crystals, such as transition metal dichalcogenides, have bridged this gap. They usually appear in the form of MX_2, where M represents a transition metal, such as Sc, Ti, Mo, or Ni; and X represents an element from column VI: either S, Se or Te. The physical and chemical properties of TMD materials are greatly diversified. They can be either metallic, semiconducting, or even superconducting. [4]

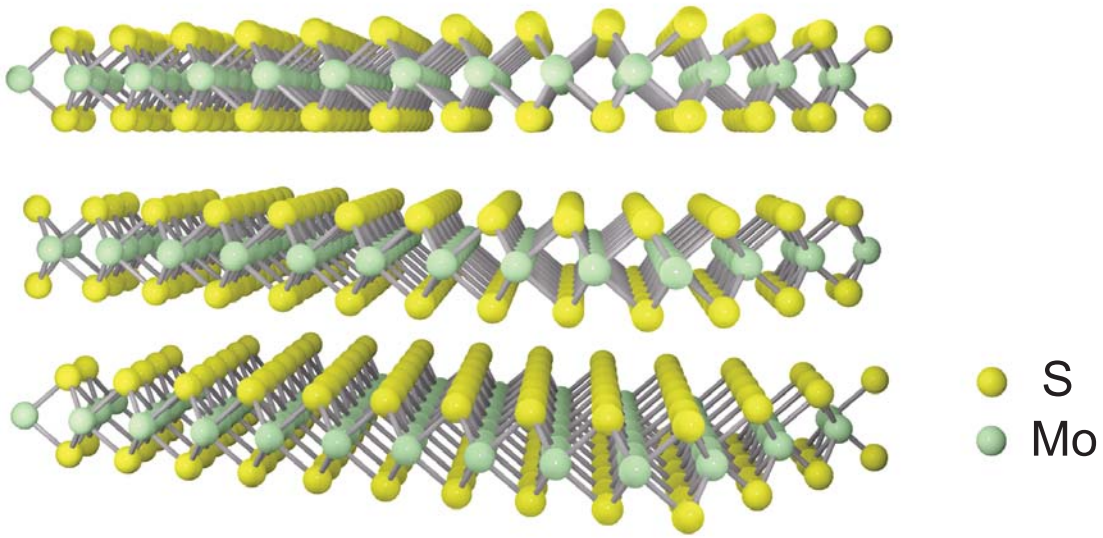

Fig. 1.2. Crystal structure of MoS_2

Figure 1.2 shows the crystal structure of a typical 2D semiconductor, MoS_2. The bulk crystal is consisted of individual layers. These layers are bonded by van der Waals force instead of covalent bonds. In each layer, a sandwiched structure can be identified, consisting with S-Mo-S atoms. The thickness of each layer is 0.65 nm. Due to the weak van der Waals force between the layers, the bulk crystal can be easily cleaved into thinner layers. Single layer MoS_2 transistors was first demonstrated in 2011 by Radisavljevic *et al.* [5] High electron mobility up to 200 $cm^2/V{\cdot}s$, high current on/off ratio up to 10^8, and small subthreshold swing (SS) down to 74 mV/dec was determined. Despite the possibility of mobility overestimation due to capacitance coupling, these results were still inspiring, as it first demonstrated a high-performance transistor based on single-layer crystal instead of bulk semiconductor. [6] In the meantime, researches also revealed that single-layer MoS_2 has different properties than its bulk counterparts. Single layer MoS_2 was determined to be a direct gap semiconductor with a 1.8 eV band gap, where bulk MoS_2 had an only 1.2 eV indirected one. [7,8]

Shifts in Raman peaks and different vibration modes were also identified between single layer and bulk MoS_2. [9]

These 2D semiconductors are much favored in device aspects. To take MoS_2 as an example, first of all, it has a large band gap between 1.2 to 1.8 eV, thus it is also considered as "graphene with a band gap". Though graphene has a much higher carrier mobility, the absence of a band gap places a serious restraint in digital applications. [10] This large band gap guarantees low off-state current for the transistors, hence reduce the static power consumption in logic circuits. Second, MoS_2 has a moderate mobility. A typical value would be around several dozens to a hundred $cm^2/V{\cdot}s$ at room temperature, and this can be further boosted up to 1000 $cm^2/V{\cdot}s$ at low temperature. [2, 11–13] Thirdly, the 2D semiconductors are innately resistive to SCE. Generally speaking, SCE happens when the channel length is comparable to the depletion width in S/D junctions. In this case, the S/D capacitance is comparable to the gate capacitance,

$$C_{sd} = C_{ox}$$

consider the geometry in a transistor, this can be further written as,

$$C_{sd} = \frac{\epsilon_o \epsilon_s}{L_{ch}} t_{ch} W_{ch} = \frac{\epsilon_o \epsilon_{ox}}{t_{ox}} L_{ch} W_{ch} = C_{ox}$$

Here, ϵ_0 is the vacuum permittivity, ϵ_s and ϵ_{ox} are the dielectric constant of that in semiconductor and gate oxide, L_{ch}, t_{ch} and W_{ch} are the channel length, thickness and width. The above equation can be simplified as,

$$L_{ch} = \sqrt{\frac{\epsilon_s}{\epsilon_{ox}} t_{ch} t_{ox}} = \lambda \tag{1.1}$$

This λ is defined as "characteristic screening length". [14] It represents a feature size where S/D electrostatic control starts to overshadow gate control in further scaling down of the channel length of transistors. With lower λ the device is expected to have better performance at shorter channel length. A conventional method to lower λ is to increase the dielectric constant of gate oxide, ϵ_{ox}, or to reduce the thickness of the gate oxide, t_{ox}, which is the reason that high-k material is used. However,

the advent of 2D semiconductors have provided a new approach in this issue. On one hand, the physical thickness of the channel can be greatly reduced. In UTB Si MOSFETs, the devices will suffer from a drastic mobility degradation and V_T shift due to strong surface roughness once body thickness is reduce to sub-5 nm. [15] However, the body thickness of MoS_2 can be continuously reduced down to atomic scale level with perfectly flat surface. [5] On the other hand, the dielectric constant in MoS_2 is as low as ∼3.3, approximately a quarter of that in silicon, which further reduces the characteristic screening length in MoS_2 based transistors. [16] This means, for a single layer MoS_2 transistor, if we have an equivalent oxide thickness (EOT) down to 1 nm, the characteristic screening length would only be 0.8 nm. This is a surprising low number that has never been seen in transistors based on conventional bulk semiconductors.

1.3 MoS_2 Transistors: Opportunities and Challenges

Owing to the great potentials for electronic/optoelectronic applications, MoS_2 transistors have been intensively studies in the past years. Not only limited in transistors, a variety of applications, such as integrated circuits, photo detectors, chemical sensors, have been widely investigated. [17–21] However, in order to achieve real industrial applications, there is still a long way to go for MoS_2 transistors, as it still suffers from a list of bottlenecks that need to be urgently addressed.

The first problem comes from dielectric integration on 2D surface. In conventional CMOS process for bulk semiconductors, this is realized by ALD process. Due to the lack of dangling bonds on the 2D surface, the nucleation of ALD precursors is getting harder at the initial stage, resulting in the difficulty in direct ALD growth. [22,23] To avoid this problem, a practical way is to insert a seeding layer, such as Al, prior to ALD growth. [24] Though this utilizes a uniform dielectric layer on top of 2D crystals, this seeding layer enhanced the dielectric thickness, and further makes it difficult to achieve a low EOT for aggressively scaled devices.

The second issue is related with metal contacts. For silicon MOSFETs, the low contact resistance is realized by heavy doping of the S/D regions, leading to a direct tunneling from metal contacts to the semiconductor. However, no mature doping technique, such as ion implantation, has been developed for 2D semiconductors. Therefore, the contact resistance strongly depends on the Schottky barrier height at the metal/2D interface, leading to a large contact resistant. [11, 12] Various methods have been applied to lower the contact resistance, including molecular doping of the 2D crystal, heterojunction contact, insertion of an oxide layer, and etc. [25–30] But still there is a long way ahead to reduce the contact resistance down to 0.1 Ω·mm to meet the requirement for industrial applications.

The third question is how to achieve wafer scale, high quality MoS_2 thin film. There have been numerous attempts so far to synthesis single- or multi-layer MoS_2 thin films on various substrates *via* CVD process. [31–35] These CVD synthesized films show similar physical and transport properties as exfoliated ones. However, they are still restrained by limited grain size, and lack of mature doping during synthesis.

1.4 Main Achievements

This dissertation will be focusing on the device aspects on MoS_2 and other semiconducting 2D crystals to address the challenge mentioned in previous section. The main results achieved in this thesis are listed as follows:

Chapter 2 will focus on dielectric integration on MoS_2 and other semiconducting crystals. For the first time, a direct ALD process is realized on 2D crystals.

Chapter 3 will report on n-type MoS_2 transistors and its dimension scaling properties. Resistivity to SCE is demonstrated with channel length scaling, while a V_T adjustment technique will be demonstrated with channel width scaling.

Chapter 4 will briefly go through metal contacts on semiconducting 2D crystals. Fermi-Level pinning is identified at metal/2D interface.

Chapter 5 will summarize the CVD process for single layer MoS_2 synthesis. A

statistical study of the transistor behavior will be performed. Also, the switching mechanism in single layer MoS_2 transistor will be investigated to show its difference from conventional Si MOSFETs.

Chapter 6 will present a novel p-type 2D semiconductor, black phosphorus and phosphorene. Transport properties will be studied and a simple CMOS inverter based on 2D channel materials will be demonstrated.

2. INTEGRATION OF HIGH-K DIELECTRIC ON 2D CRYSTALS

In this chapter, the integration of Al_2O_3 high-k dielectric by ALD on 2D crystals of h-BN and MoS_2 will be investigated. The feasibility of direct ALD growth with trimethylaluminum (TMA) and water as precursors on both 2D crystals will be demonstrated. Both theoretical and experimental studies will be performed to show the initial ALD cycles play the critical role, during which physical adsorption dominates precursor adsorption at the semiconductor surface. The initial ALD growth stages at the 2D surface will be modeled by analyzing Lennard-Jones Potentials, which could guide future optimization of the ALD process on 2D crystals.

2.1 Introduction

The application of ALD techniques to metal gates and high-k dielectrics in the past decade has triumphantly extended Moores Law for the continued scaling down of silicon based CMOS devices. [36] In addition, the integration of high-k materials on other semiconductors, such as Ge, GaAs, InGaAs, GaSb, etc., has also been comprehensively studied in the pursuit of alternative channel materials to replace silicon at the 10 nm node and beyond. [37] In 2004, graphene, a fascinating material labeled as a perfect 2D crystal with an electron mobility approaching 200,000 $cm^2/V{\cdot}s$ at room temperature, was realized and has shown promise as a silicon replacement. [2,3] Furthermore, following research has unveiled other similar materials that exist as layered 2D-materials, including BN, Bi_2Te_3, Bi_2Se_3, MoS_2, and etc. These other materials can also be isolated to a single atomic layer via mechanical exfoliation. [5, 38–40] However, researchers have noticed that the deposition of high-k dielectric onto 2D crystals, such as graphene, is not as easy as deposition onto Ge or III-V bulk mate-

rials. A typical example is the failure of Al_2O_3 deposition on graphene basal plane with trimethylaluminum (TMA) and water as ALD precursors, which is the most reliable ALD process with a wide process window. This failure has been understood to be caused by the difficulty of forming chemical bonds on the graphene basal plane due to existing global sp^2-hybridation. [41, 42] Despite several successful attempts to integrate high-k dielectrics onto 2D systems, the integration of high-k dielectric onto such 2D crystals has not been thoroughly studied. [5, 43, 44]

2.2 Growth Mechanism of ALD

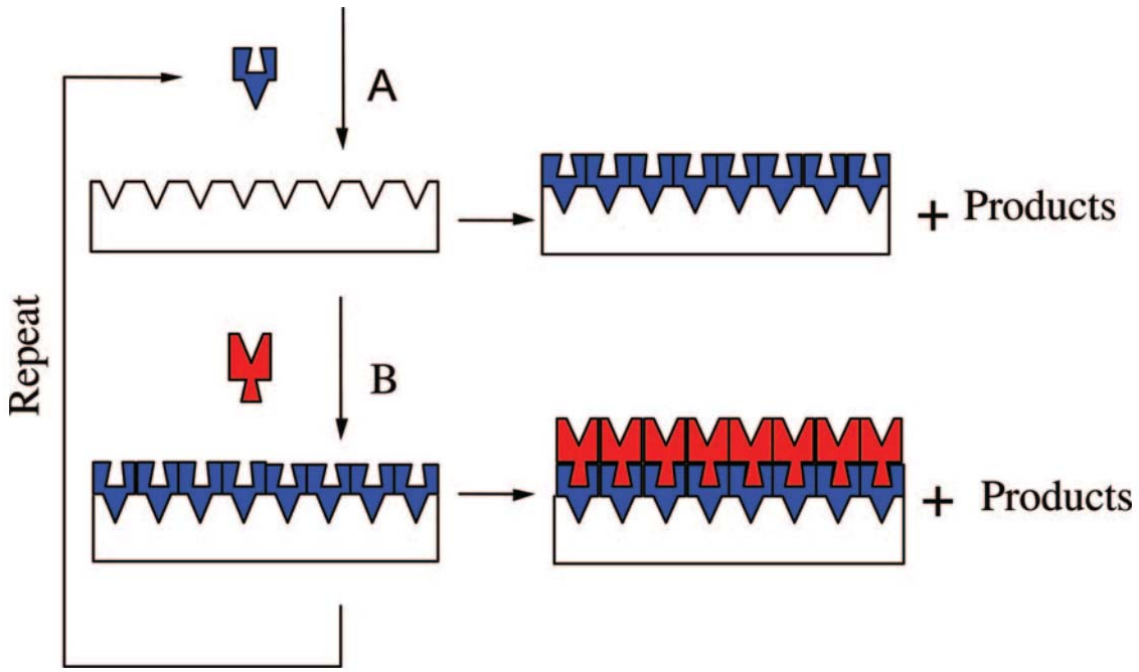

Fig. 2.1. A schematic illustration of ALD growth mechanism [45]

First of all, the growth mechanism of ALD will be briefly discussed. A schematic showing the sequential, self-limiting surface reactions during ALD process is shown in Figure 2.1. [45] In such an ALD cycle, precursor A is first introduced into the

reaction chamber. Due to the existence of surface dangling bonds of the substrate, an atomic layer of precursor A is adsorbed on the substrate. Extra precursors will be purged by nitrogen. After that, precursor B is introduced into the chamber. It reacts with precursor A and then forms an atomic layer of the products. Extra precursor B and by-products would be purges by nitrogen again. By repeating this cycle, a uniform, thickness-controlled layer will be achieved. Figure 2.2 shows the cross-section SEM image of an ALD Al_2O_3 layer with perfect edge coverage on a silicon trenched structure. [46]

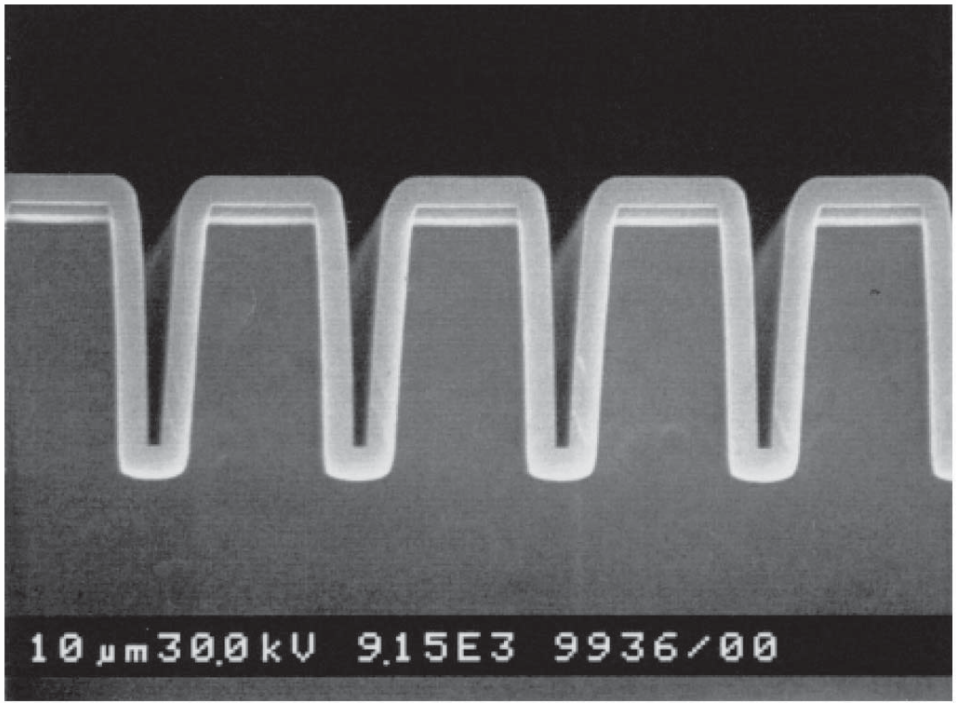

Fig. 2.2. Cross-sectional SEM image of an Al_2O_3 ALD film with a thickness of 300 nm on a Si wafer with a trench structure [46]

2.3 ALD Growth on 2D Crystals

In this section, the growth of ALD Al_2O_3 on two typical 2D materials is studied: hexagonal boron nitride (h-BN), a sister material of graphene and previously used as a

graphene dielectric; and MoS_2, a promising layer-structured semiconducting material with a satisfying band gap. [47] h-BN and MoS_2 2D crystals were thinned from bulk crystals by mechanical exfoliation, and then transferred to 300 nm SiO_2 covered Si substrates. After being cleaned in solvents to remove tape residue, the samples were loaded into an ASM F-120 ALD system. TMA and water were used as precursors. Pulse times of 0.8 and 1.2 seconds were used for TMA and water, respectively, with a purge time of 6 seconds for both. Al_2O_3 was deposited with a range of substrate temperatures from 200 °C to 400 °C by 50 °C steps.

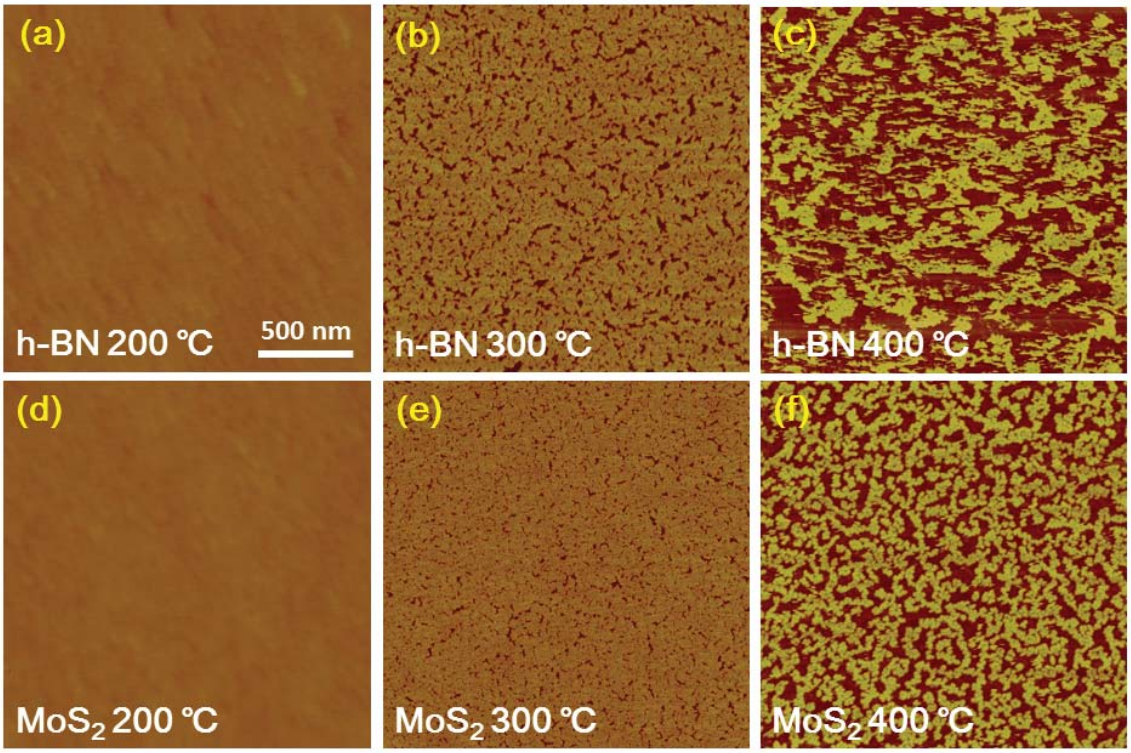

Fig. 2.3. AFM images of h-BN or MoS_2 surface after 111 cycles of ALD Al_2O_3 at 200 °C, 300 °C and 400 °C

Figure 2.3 shows selected AFM images on h-BN and MoS_2 surfaces after 111 ALD cycles at 200 °C, 300 °C and 400 °C, with an expected Al_2O_3 thickness of ∼10 nm. The Al_2O_3 growth rate on SiO_2 substrates remained similar at various tem-

peratures; however, its growth on h-BN and MoS_2 flakes was strongly temperature dependent. A uniform Al_2O_3 layer formed at 200 °C on both h-BN and MoS_2 substrates is observed. Previous study have shown that the leakage current density was relatively small ($\sim 2\times10^{-4}$ A/cm^2 under 1 V gate bias) for MoS_2 based metal-oxide-semiconductor structure, suggesting that the ALD Al_2O_3 thin film on MoS_2 was of good quality [48]. With elevated growth temperatures, it was obvious that the Al_2O_3 film was not uniform on both h-BN and MoS_2 substrates. When the growth temperature was increased to 250 °C, pinhole defects started to appear at the 2D surface. With further increase of growth temperatures, these pinholes tended to expand and finally connect with each other, leaving island like Al_2O_3 clusters on the 2D basal plane. In contrast to the growth on basal plane, the growth on edges remain constant at the range between 200 °C to 400 °C, due to the existence of dangling bonds at the basal edges. [17, 41]

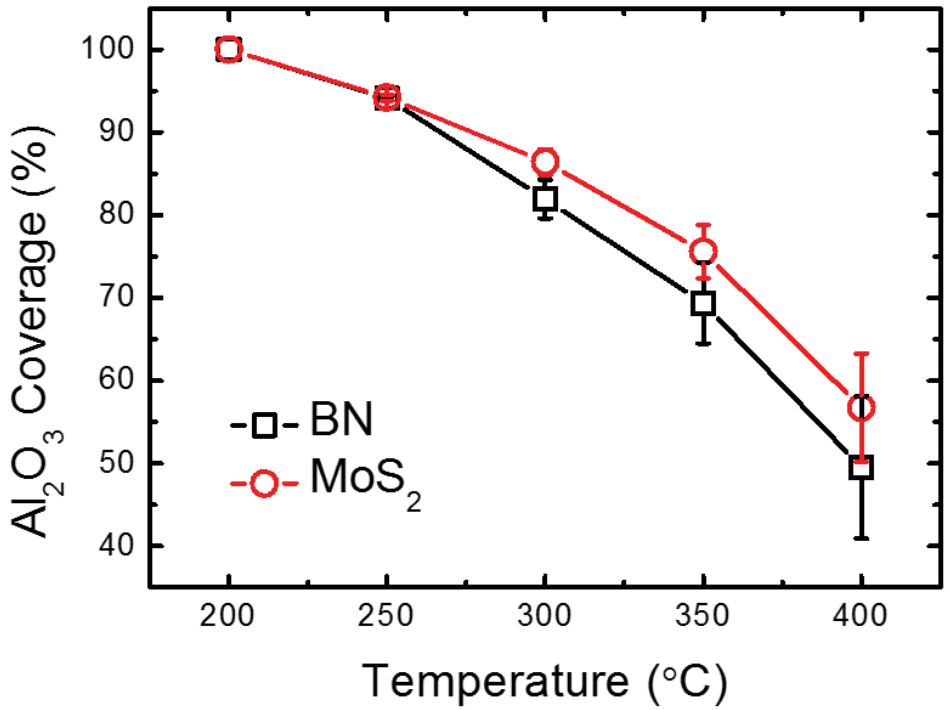

Fig. 2.4. Al_2O_3 coverage estimation from MATLAB analysis by Otsu method

The AFM data is further analysed with a MATLAB script to quantify the Al_2O_3 coverage, and used this as a metric for the ease of ALD growth, although the coverage percentage may have evident run-to-run variance due to fluctuations of chamber pressure, which has a significant impact to the surface adsorption. The Otsu method was applied to distinguish the boundary between the regions on h-BN or MoS_2 flakes "with" or "without" Al_2O_3 growth. [49] As shown in Figure 2.4, the Al_2O_3 coverage was monotonically decreasing with increased temperature, and had a slightly increased coverage ratio on MoS_2 than that on h-BN at higher temperatures. Such temperature dependent growth indicates that the growth is controlled by physical adsorption of the precursors at the substrate surface, and will be further discussed later.

Table 2.1.
Binding Energy ($E_{ads} = E_a + E_b - E_{ab}$) in kcal/mol

Adsorption	E_{ads}
hBN + H_2O → hBN-H_2O	4.1
hBN + TMA → hBN-TMA	12.8
MoS_2 + H_2O → MoS_2-H_2O	11.1
MoS_2 + TMA → MoS_2-TMA	33.0

In order to achieve insight in the understanding of the interactions at the substrate surfaces and hence understand the initial ALD cycles for 2D crystals, density function theory (DFT) studies were performed by using the M06-2x method with basis sets 3-21G(d) for Mo and 6-311G+(d,p) for H, O, C, B, N, and Al. [50] Table 2.1 shows the calculated adsorption energies of the two ALD processes. It can be seen that the binding energy of TMA on h-BN is 8.7 kcal/mol greater than that of H_2O on h-BN and the binding energy of TMA on MoS_2 is 21.9 kcal/mol greater than that of H_2O on MoS_2. This implies that TMA is more easily physically absorbed on both types of crystals.

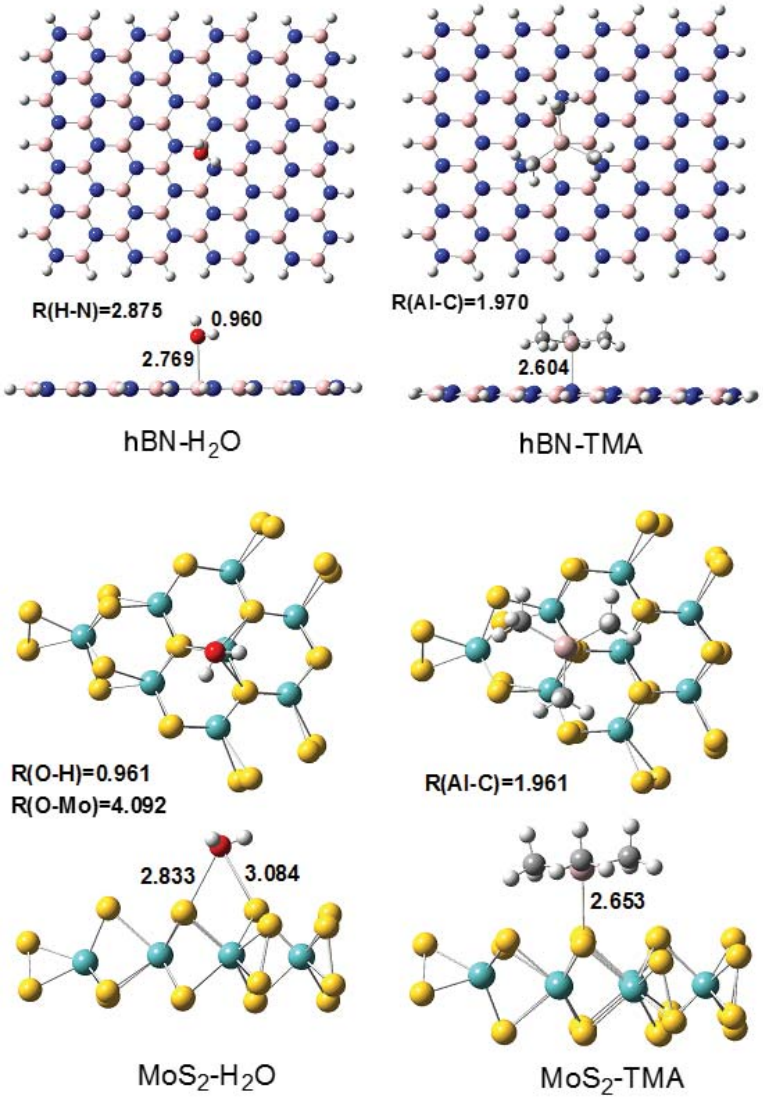

Fig. 2.5. Binding structure models of H_2O and TMA on h-BN and MoS_2

Figure 2.5 shows the four adsorption structural models. For the h-BN system, the O atom of H_2O is adsorbed at the B atom while the Al atom of TMA is adsorbed at the N atom. The calculated distances of O-B and Al-N are 2.769 and 2.604 Å, respectively. These distances are greater than the corresponding covalence bonds. Therefore, the adsorption energies include the front molecular orbital interaction and van der Waals contribution. For MoS_2, H_2O and TMA are all adsorbed at the S

atom. The length of Al-S bonds is predicted to be 2.653 Å while the shortest length of O-S bonds is 2.833 Å. Apparently the distances of Al-S and Al-N are shorter than that of O-S and O-B, respectively, though the atomic volume of Al is greater than that of O. Therefore, compared to the H_2O adsorption, the TMA adsorption is more stable. Table 2 lists the atomic charges, polarizabilities, and frontier molecular orbital levels of the interaction atoms in H_2O, TMA, h-BN, and MoS_2. It can be seen that O atoms with negative charges would have electrostatic interactions with the positively charged B and Mo atoms, while Al atoms with positive charges would be interacting with the negatively charged N and S atoms. Also, one can see that the polarizability of TMA is much greater than that of H_2O, while the polarizability of MoS_2 is much greater than that of h-BN. This implies that the interactions of TMA-MoS_2 would have the largest dispersion energy and the interactions of H_2O-hBN would have the least. In addition to this van der Waals interaction, the frontier molecular orbitals of these model molecules may take an important role in the combination.

Table 2.2.
Atomic charges, polarizabilities, and frontier molecular orbital levels of the interaction atoms in H_2O, TMA, h-BN, and MoS_2 in atomic unit.

	H_2O		TMA		h-BN		MoS_2	
ϵ_i(LUMO)	0.1933		-0.0068		0.0363		-0.1672	
ϵ_i(HOMO)	-0.4009		-0.3210		-0.2972		-0.2823	
P_i	6.140		48.996		34.666		112.316	
	O	H	Al	C	B	N	Mo	S
Q_α	-0.582	0.291	1.337	-0.481	0.991	-0.924	2.176	-1.088

From Table 2, the gaps between the LUMO and HOMO level are 0.5942 au for H_2O, 0.3142 au for TMA, 0.3335 au for h-BN, and 0.1151 au for MoS_2. Thus, the orbital interactions of H_2O with h-BN and MoS_2 would be less than that of TMA with h-BN and MoS_2, respectively. This analysis supports the predicted result of

adsorption energies. In classical ALD theories, deposition with precise thickness control is determined by self-limited precursor adsorption at substrate surfaces, and is classified into two types: physical and chemical adsorption surface. During the initial ALD cycles on 2D crystals, excepting a few chemically active materials such as the topological insulators Bi_2Te_3 and Bi_2Se_3 which are easily oxidized at growth temperatures and hence facilitate the formation of chemical bonds for precursors at the surface, chemical adsorption is rarely observed. [22] This is due to the absence of dangling bonds at their basal planes. Consequently, physical adsorption is the dominant adsorption method at the 2D surface. This view is also supported by the result that such deposition is strongly temperature dependent. It is interesting to note that ALD Al_2O_3 can be deposited on h-BN at 200 °C, while Al_2O_3 can only grow at graphenes edges, even though h-BN is extremely structurally similar to graphene. Such a difference between Al_2O_3 deposition on graphene and BN can be explained using the framework of the Lennard-Jones potential model, which has been generally used to model the molecular adsorption on graphene and carbon nanotube surfaces. [51–53]

As shown in Figure 2.6, for each ALD pulse-purge cycle, the pulse action pushes the precursor molecules to the vicinity of substrate where the molecule has the lowest potential energy; while the purge action pushes the molecule away from the substrate, to the x-axis infinity, where the molecules encounter an energy barrier. There are two factors that determine the ultimate molecular state: One is the depth of the potential well, shown as the adsorption energy and determined by the polarizability of the substrate and molecules. Using h-BN as an example, nitrogen serves as a positive charge center while boron serves as a negative charge center, while graphene has no polarization due to perfect symmetry, the interaction between the h-BN molecule and ALD precursors would be stronger than that of graphene and ALD precursors. That is to say, the depth of the potential well in the h-BN system will be larger than that in the graphene counterpart. The other reason is the growth temperature, which is near the thermal energy of the precursor molecules. At lower temperatures, the thermal energy that the precursors can obtain from the environment is not large enough so that the

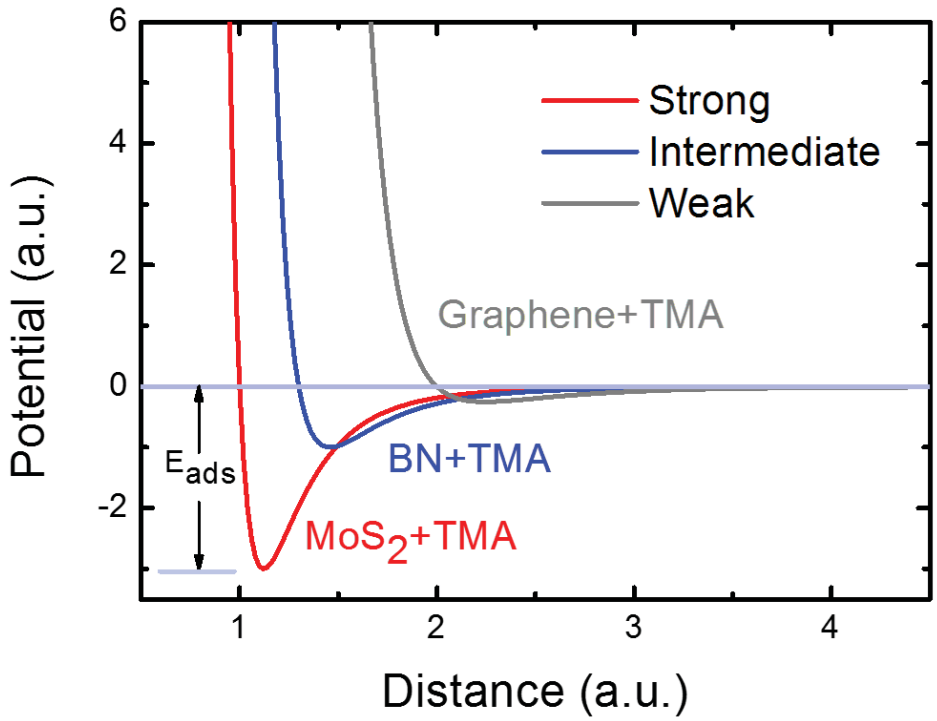

Fig. 2.6. An illustrative Lennard-Jones potential Model for physical adsorption at 2D crystal surfaces

molecules are trapped in the potential well, despite the purge action; while at higher temperatures where the thermal energy is greater than the depth of the potential well, the excited molecule can escape, thus resulting in incomplete ALD cycles. Therefore, the ALD window for deposition on 2D crystals is different from previous studies on bulk materials. For bulk substrates, the lower temperature limit of the ALD growth window is determined by precursor condensation and incomplete reaction at lower temperatures, and the high temperature limit is determined by precursor decomposition as well as desorption. [54] For 2D substrates, the low temperature limit still remains similar as it is only related to the precursors, regardless of the substrate material. However, the high temperature limit, since desorption is much easier at 2D surfaces, is at a dramatically lower temperature. This creates a large challenge to dielectric integration for high performance devices, such as V_T shifts observed in the study on MoS_2 top-gated MOSFETs. [48] Given the discussion above,

it is clearly seen that the first several ALD cycles is critical, not only for properties related to interface quality, but to allowing further deposition as Al_2O_3 can provide dangling bonds for the chemical adsorption of the precursors. One way to optimize the ALD process is to change the pulse and purge times in to better control the surface adsorption/desorption at the initial stages of deposition. Alternatively, a seeding layer, such as an ultrathin Al film, or Al_2O_3 film deposited by ALD at lower temperature, can also provide a solution for high quality dielectric growth as played with graphene. [55] Another related question is the "interface" issue, as it has been generally accepted that the origin of interface states is attributed to unpassivated dangling bonds. [56] In the absence of dangling bonds at surface of 2D crystals, the definition of "interface states" between 2D crystals and dielectrics may need to be reconsidered, and such an issue may need further investigation.

2.4 Summary

In summary, a direct ALD growth of Al_2O_3 with TMA and water as precursors on 2D crystals of h-BN and MoS_2 is demonstrated. A DFT study is also performed on surface adsorption of 2D crystals at different geometric substrate locations. Both experimental and theoretical results show that the ALD growth on 2D crystals is determined by physical absorption, and is enhanced by in-plane polarization of the substrate. These results have shown provided insight into growth mechanisms and will allow better solutions for high-quality dielectric integration to be found, and provides a big step forward for novel devices based on 2D crystals in the future.

3. N-TYPE MOS_2 TRANSISTORS AND DIMENSION SCALING

Research in MoS_2 electronics is still in its infancy. The first experimentally demonstrated single-layer MoS_2 transistor has already shown a mobility of over 200 $cm^2/V{\cdot}s$, a SS of 74 mV/decade and on/off ratio of 10^8. [5] Following NEGF simulations theoretically predicted the perfect performance limits of MoS_2 thin film transistors. [16] In this chapter, the device properties of MoS_2 transistors will be investigated. A top-gated MoS_2 MOSFET with Al_2O_3 as gate dielectric will be demonstrated. Furthermore, scaling properties, such as channel length scaling and width scaling will also be discussed.

3.1 N-type Double-Gate MoS_2 Transistors

After a successful demonstration of direct ALD process, as discussed in chapter 2, MoS_2 transistors with top gate dielectric is going to be fabricated. To begin with, MoS_2 thin flakes were mechanically exfoliated by the classical scotch-tape technique and then transferred to a heavily doped Si substrate capped with 300 nm SiO_2. Al_2O_3 was deposited on MoS_2 flakes within an ASM F120 ALD reactor. TMA and water were used as precursors. A 16 nm ALD Al_2O_3 was deposited on MoS_2 flakes at 200 °C. After Al_2O_3 growth, source and drain regions were defined using optical lithography with a spacing of 9 μm. After source/drain regions etched with BOE, a 20/50 nm Ni/Au was deposited as the source/drain contacts and Ti/Au was used for gate. The gate length is $\sim$3 μm with $\sim$3 μm spacings to source/drain.

The MoS_2 MOSFET was fabricated on a $\sim$15 nm thick flake which contains about 23 individual MoS_2 layers. Final device structure is shown in Figure 3.1. The flake thickness was not reduced to a single layer since the band gap of MoS_2 crystal increases

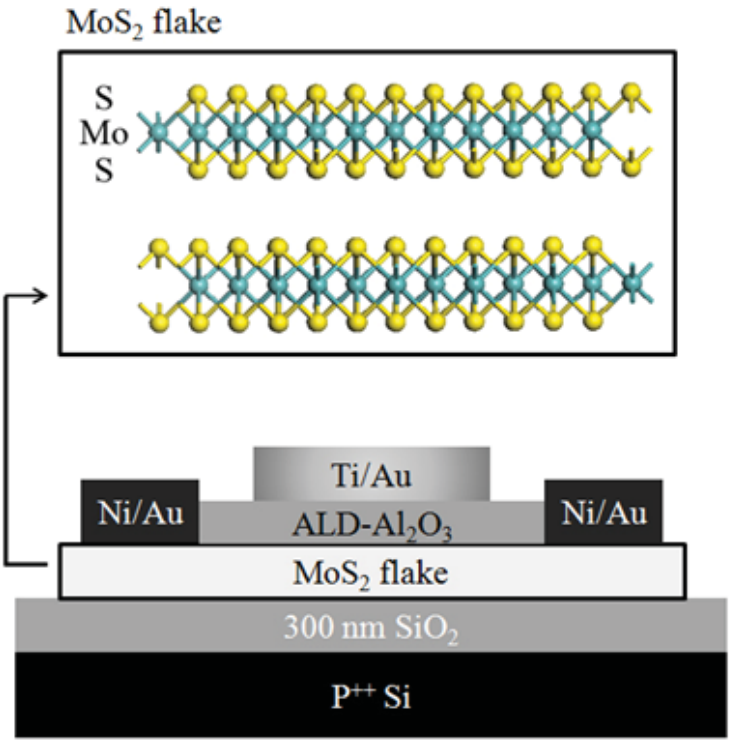

Fig. 3.1. Device structure of MoS_2 double gate MOSFET

to 1.8 eV for single layer, leading to a reduced density of states. [7] C-V measurement was carried out in order to evaluate the interface quality between ALD Al_2O_3 and MoS_2 crystals, as shown in Figure 3.2. Source and drain were grounded, while a voltage bias on the top-gate is applied. The area of the capacitor was only $\sim$12 μm^2, making the low frequency C-V curve rather noisy. The high frequency C-V at 1 MHz showed a clear transition from accumulation to depletion for a typical n-type MOS capacitor. A moderate hysteresis of $\sim$80 mV exhibited in the curves, showing that the ALD Al_2O_3 film grown at 200 °C on MoS_2 and the interface were both of good quality.

Figure 3.3 show the transfer characteristics and transconductance of the device from both the top-gate and the back-gate. The charge neutrality level (CNL) of MoS_2 is located slightly under the conduction band, thus making it easy for an accumulation-type nMOSFET. [57, 58] The transfer characteristics of the top-gate

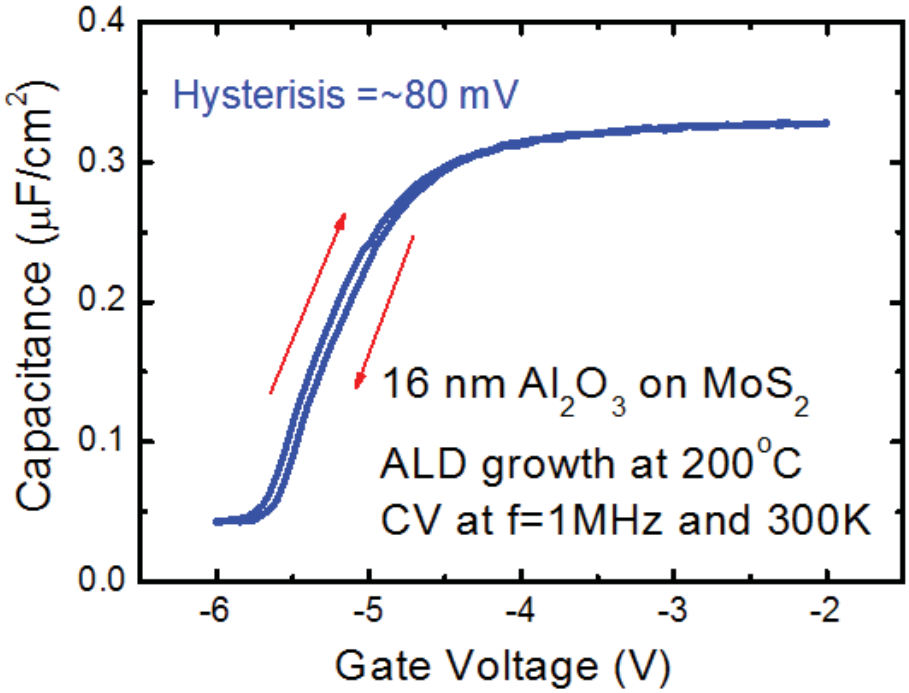

Fig. 3.2. 1 MHz high-frequency C-V characteristic of the MOSFET device measured at room temperature in darkness

suffer from a very large negative threshold voltage (V_T) shift, as attributed to the existence of large amount of positive fixed charges in the bulk oxide, due to the comparatively lower deposition temperature. [59] The leakage current was also measured in the same device, and was determined to be less than 2×10^{-4} A/cm^2 in the measurement range from -6 V to 3 V. The highest drain current density achieved at $V_{ds} = 1\ V$ using back-gate modulation is 7.07 mA/mm and an on/off ratio greater than 10^8. This superior on/off ratio compared to graphene is attributed to the 1.2 eV large band gap. The greatest current density from top-gate is about 2 orders of magnitude smaller than that from the back-gate. This big difference comes from the non-self-aligned top-gate device structure. From Figure 3.1, it can be seen that the heavily doped Si substrate has a "global" control over the entire flake. With increasing back-gate voltage, the carriers in the MoS_2 flake are accumulated and thus

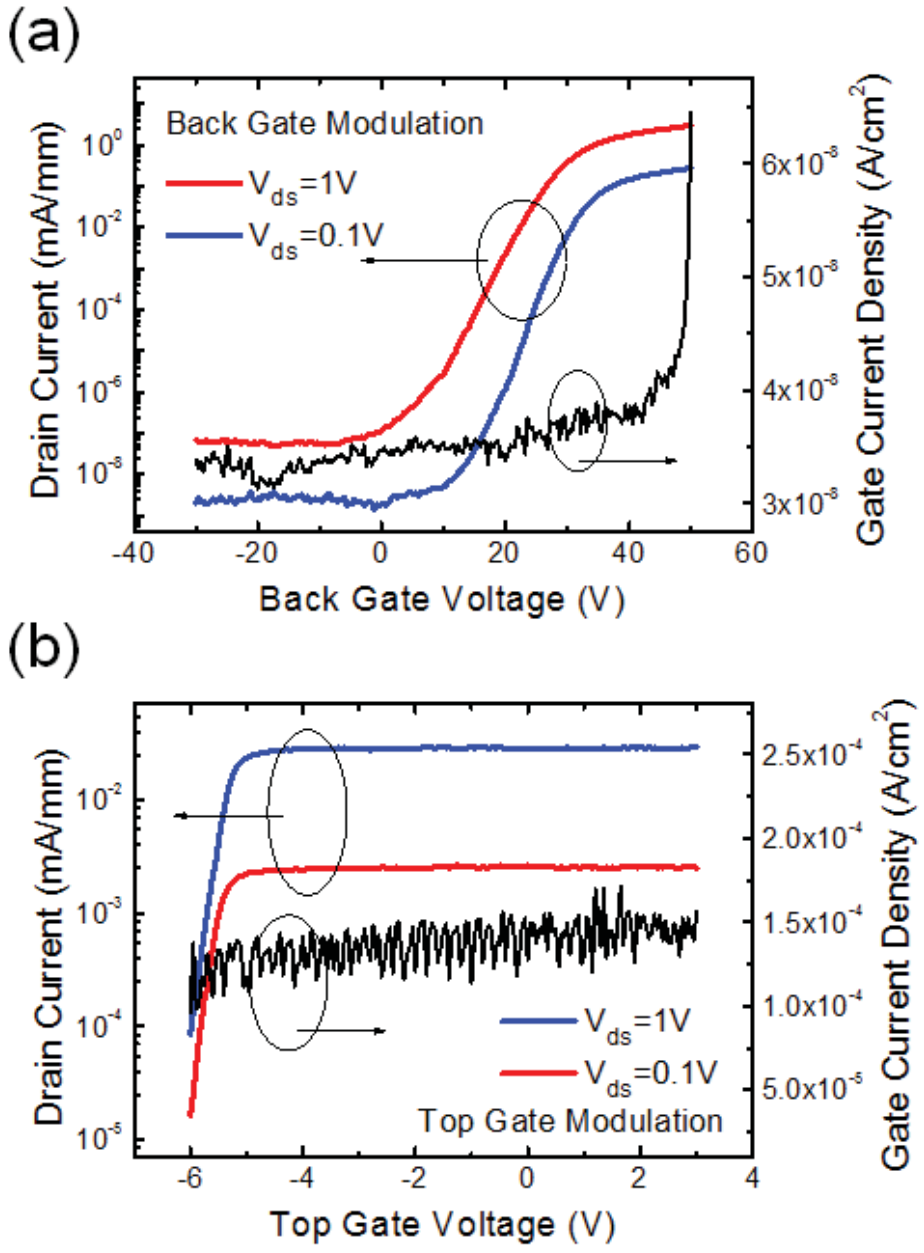

Fig. 3.3. Transfer characteristics of the MoS_2 double gate MOSFET from back-gate and top-gate controls with leakage current density from 300 nm SiO_2 and 16 nm Al_2O_3

the contact resistance between the Ni/Au source/drain and the MoS_2 flake would be reduced, as the flake is electrostatically doped by the electric field, while the top-

gate can only modulate part of the channel under the top-gate. The peak extrinsic transconductance (g_m) from back-gate control is 0.165 mS/mm at $V_{ds} = 1\ V$. The hysteresis of the top-gate transfer curves is much smaller than that of the back-gate curves, similar to the C-V curves. The subthreshold swing (SS) for top-gate is ∼140 mV/dec at $V_{ds} = 1\ V$. The interface trap density is estimated to be $2.4\times10^{12}/\text{cm}^2\cdot\text{eV}$ at MoS_2 and ALD Al_2O_3 interface and would be further reduced by optimizing the process. Considering that there is minimal process refinement, such as no surface passivation and the low ALD growth temperature, this may imply the interface states issue between 2D crystals and ALD high-k dielectrics is very forgiving.

Figure 3.4 shows the drain current versus drain voltage under a variety of back- and top-gate biases. The gate biases range from 50 V to 20 V with a -5 V step for back-gate, and from -3 V to -6 V with a -0.5 V step for top-gate. For the top-gate measurement, a back-gate voltage of 50 V is applied to reduce the contact resistance and access resistance. Consequently, the maximum current density for top-gate modulation has now been increased to 6.42 mA/mm, back to the same level of that from back-gate modulation. The maximum extrinsic g_m at $V_{ds} = 2\ V$ are 0.318 mS/mm and 2.83 mS/mm for back-gate and top-gate modulation, respectively.

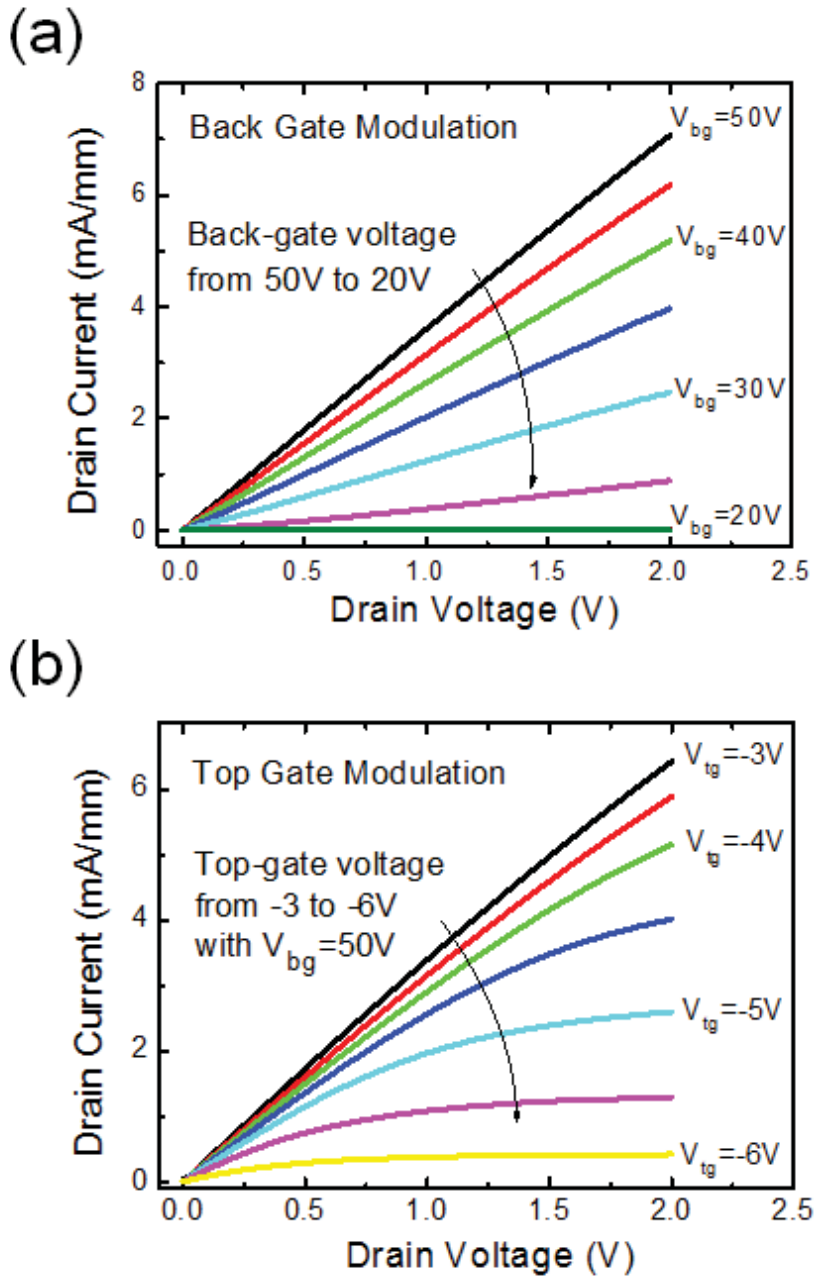

Fig. 3.4. Output characteristics of the MoS_2 double gate MOSFET from back-gate and top-gate controls

3.2 Channel Length Scaling of MoS_2 Transistors

In this section, device performance of MoS_2 transistors with various channel length will be presented. Immunity to SCE of MoS_2 transistors will be evaluated at short channel regions.

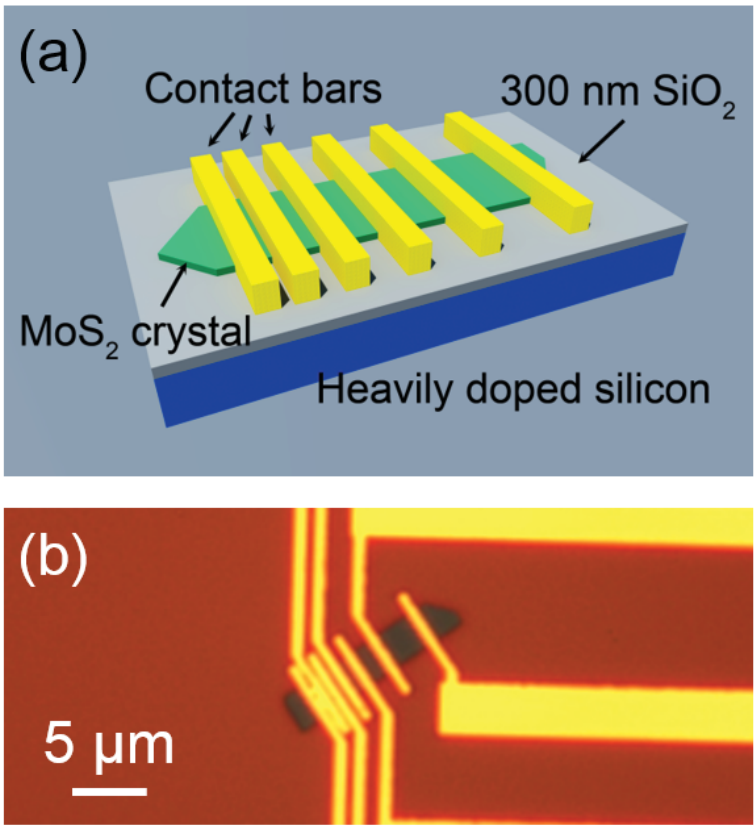

Fig. 3.5. Schematic diagram and optical image of the back-gated MoS_2 MOSFETs with various channel length

Sets of MoS_2 devices with various channel length were fabricated on exfoliated MoS_2 crystals. Each set of the device was fabricated on the same rectangular MoS_2 flake, so the scaling effect can be directly observed and compared without the correction for geometry and thickness variations. The MoS_2 flakes were mechanically exfoliated with 3M scotch tapes from a bulk ingot purchased from SPI Inc. A heavily p-doped silicon wafer (0.01–0.02 Ω·cm) with 300 nm SiO_2 capping layer was used as back gate and gate dielectric. After flake transfer, the samples were soaked in acetone for overnight to remove the tape residues on SiO_2 substrate, followed by methanol and isopropanol rinse. The thickness of the flakes was measured by Dimension 3100 AFM systems. MOSFETs structures were defined by electron beam lithography, followed by the electron beam evaporation of Ni/Au for 30/50 nm or only 50 nm Au

for different sets of devices with the deposition rate of ∼1 Å/s. Metallization was performed by electron beam evaporation afterwards. The width of the contact bars are 500 nm. Electrical characterizations were carried out with Keithley 4200 system at room temperature. The schematic and corresponding optical microscope image of the 5 nm thick devices are shown in Figure 3.5.

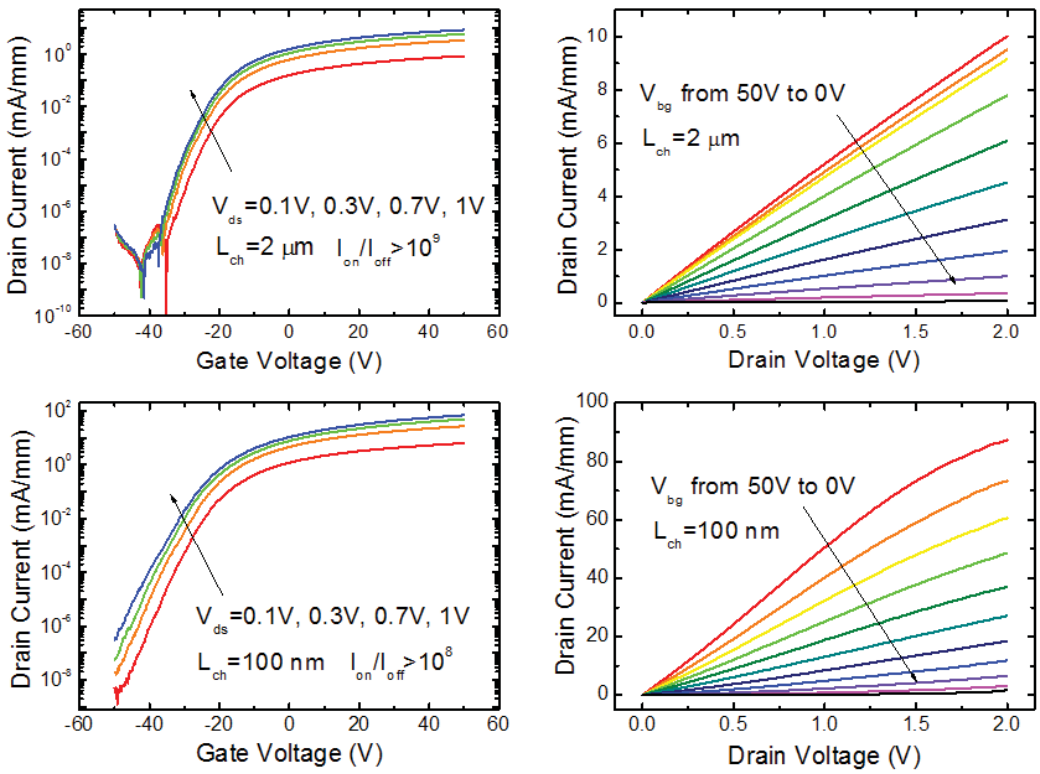

Fig. 3.6. Device performance of long channel and short channel MoS_2 transistors

First, the transistor characteristics of both long-channel and short-channel MoS_2 MOSFETs are examined. Considering that the single layer MoS_2 has a larger band gap and hence a lower mobility and larger contact resistance, the devices on a few-layer crystal were fabricated for a better trade-off between the on/off ratio and device performance. Note that the dielectric constant of MoS_2 is only around 3.3, a 5 nm thick crystal would be thin enough for short channel devices to turn off completely. [16]

Figure 3.6 shows the transfer and output curves for the 2 μm and 100 nm channel length (L_{ch}) devices. Because of the large band gap of 1.2 eV of MoS_2, these devices, unlike graphene, can be easily turned off. Even though the thickness of gate dielectric is extremely large (300 nm), which results in a much degraded electrostatic control, still no evident short channel effects were observed with channel lengths down to 100 nm. For this short channel device, the on-current is reaching 70 mA/mm at $V_{ds} = 1\ V$, and the current on/off ratio is over 10^7 for $V_{ds} = 1\ V$, and is able to maintain an on/off ratio of 10^9 at $V_{ds} = 0.1\ V$. Benefiting from its ultrathin body, the on/off ratio does not drop much compared to the 2 μm long device which has a current on/off ratio up to $\sim 10^{10}$, showing good immunity to short channel effects. Note that significant short channel effects could be observed on other planar devices, such as InGaAs or Ge, when the gate length was scaled down to 150 nm. [60] The intrinsic mobility extracted from the 2 μm long device is $\sim$28 $cm^2/V{\cdot}s$. It could be further increased up to several hundred by dielectric passivation on the top. [5, 48] The observation of transistor behavior without evident short channel effects with 300 nm SiO_2 indicates that the enhancement of electrostatic control by reducing the gate dielectric thickness down to several nanometers would significantly push the scaling of channel length down to sub-10 nm for MoS_2 devices. This is beyond the range of conventional semiconductors. The superior immunity to short channel effects of MoS_2 not only originates from its ultrathin body nature, but is also due to the low dielectric constant of MoS_2 itself. The characteristic length of short channel transistors with planar structures is:

$$\lambda = \sqrt{\frac{\epsilon_s}{\epsilon_{ox}} t_{ch} t_{ox}} \tag{3.1}$$

where λ is the characteristic screening length, ϵ_s and ϵ_{ox} are the permittivity of semiconductor and gate oxide, t_{ch} and t_{ox} are the thickness of semiconductor channel and gate oxide. The characteristic length for this 5 nm thick MoS_2 transistor is 35.6 nm, much shorter than the channel length of the shortest device. If the 300 nm SiO_2 gate oxide is replaced by 6 nm HfO_2 with an EOT of $\sim$1 nm, the characteristic length

would be expected to be reduced to only 2 nm, which is far beyond the technical consideration of 10 nm node with alternative channel materials for logic applications. This formula was first proposed by Yan *et al.* to calculate the characteristic lengths of silicon MOSFETs, where the carrier transport is almost isotropic. [14] For layered structures, the layer-to-layer transport is less efficient as in-plane transport. [12] Therefore, the effective t_{ch} for 2D crystals could be even smaller, further reducing characteristic screening length of MoS_2 transistors.

To make a comparison of the short channel effects related to the MoS_2 flake thickness, another set of devices on a 12 nm thick MoS_2 crystal was fabricated. The characteristic length of this transistor is calculated to be ∼55.2 nm, on the same 300 nm SiO_2 as back gate dielectric. The channel length is further scaled down to 50 nm, so that the channel length would be comparable to λ. The transfer and output characteristics of the device with 50 nm channel length are presented in Figure 3.7. Short channel effects start to appear in this device. The drain current on/off ratio (I_{on}/I_{off}) dropped down to $\sim 10^7$ at $V_{ds} = 0.1\ V$, and $\sim 5\times 10^4$ at $V_{ds} = 1\ V$. A severe drain induced barrier lowing (DIBL) was also observed. The upward bending in the output characteristics in Figure 3.7(b) at high drain biases also indicates a degraded electrostatic control from the gate. However, the MoS_2 transistors differ from traditional silicon transistors as they are majority carrier transistors, also they do not have heavily implanted source/drain regions, as mentioned above. These two features makes the MoS_2 transistor slightly different from bulk silicon or silicon on insulator transistors for their short channel behaviors. Since no space charge region are formed between source/drain and channel, there should be much less threshold shift. Meanwhile, due to the absence of heavily doped source/drain regions, the hot electrons degradation at drain end can be eliminated and would not be a severe problem. Also, the atomic flat surface of the 2D crystal would greatly reduce surface scattering. Therefore, in this section, the SCE would be mostly focused in DIBL and current on/off ration as criteria for short channel degradation of the MoS_2 transistors.

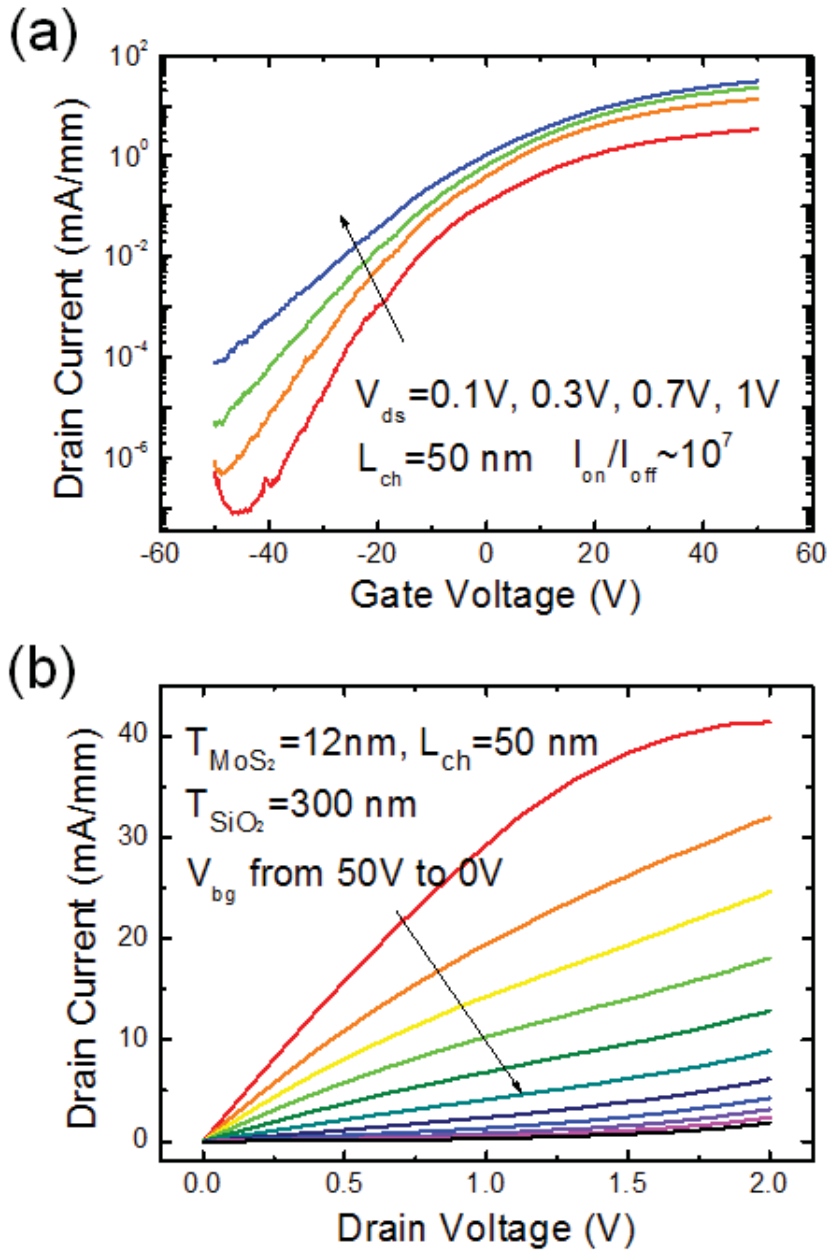

Fig. 3.7. Device performance of the MoS_2 transistors of 50 nm channel length

The channel length dependent I_{on}/I_{off} and DIBL of the two sets of devices are plotted in Figure 3.8. For the set of devices with 5 nm thick MoS_2 crystal, the I_{on}/I_{off} ratio is nearly constant, with a minor decrease as the channel becomes shorter, while

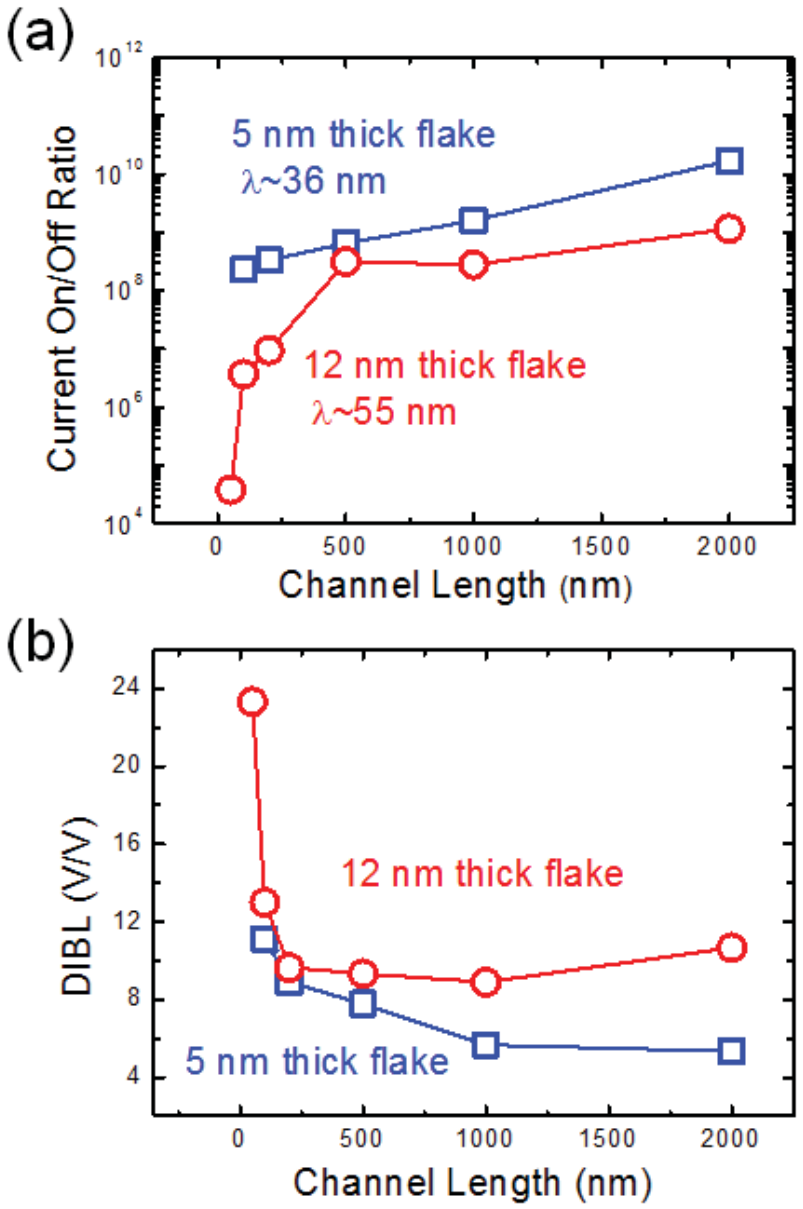

Fig. 3.8. Current on/off ratio and DIBL in MoS_2 transistors at various channel length

the total change remains within one order of magnitude of its long-channel value. The set of devices on the 12 nm thick crystal was observed to have a lower I_{on}/I_{off} ratio as expected, following the same slightly decreasing trend with scaling down, until the channel length approaches the characteristic length, where it experiences a

sharp drop down to less than 10^5. Similar behavior was also observed in the DIBL. Due to the weaker electrostatic control from the global back gate with 300 nm gate dielectric, the DIBL is relatively large even at long channel devices compared to top gate devices with sub-10 nm high-k dielectric. It is observed from Figure 3.8(b) that the DIBL for the sets of devices fabricated on the 5 nm thick flake is smaller than that of devices with 12 nm thick crystal. At long channel lengths, (e.g. $L_{ch} = 2\ \mu m$), it is ∼4 V/V for the thinner devices and ∼10 V/V for the thicker ones. However, these values are not completely correlated with short channel effects because the channel lengths are long enough at this region but could be attributed to the shifts in threshold voltage. In Chapter 2, it was pointed out that the MoS_2 is very sensitive to polarized molecules (such as H_2O) in the environment, and these molecules would be physically adsorbed as MoS_2 surface, and causing threshold voltage shift. That is to say, the DIBL measurement is also influenced by the hysteresis in MoS_2 transistors. Though several attempts were made to eliminate this factor, which included maintaining the temperature and humidity at a constant level in the measurement, and also the transfer curves were measured all through the fixed direction of voltage change (constantly from depletion to accumulation), but still minor fluctuations are existed in the extraction of DIBL, where the DIBL starts to increase at larger channel length for the sets of transistors fabricated on the thinner flake. Another observation from Figure 3.8(b) is that the DIBL from both sets of devices experience a rapid increase once the channel length approaches the characteristic length. If the 300 nm gate oxide be replaced with state-of-art high-k dielectric and scaled down to an EOT of 1–3 nm, one would expect that there would be no short channel effects even the L_{ch} is reduced to sub-10 nm, which shows the superior immunity to short channel effects of MoS_2 transistors, as discussed above. Though these sets of devices have large contact resistance which is comparable to the channel resistance at short channel length scales (which will be discussed later), which will reduce the lateral electric field in the transport direction, the weak electrostatic control of the gate (a

maximum of 1.67 MV/cm) compared to top gate devices (∼4–6 MV/cm) still makes the immunity to short channel effects convincing.

For long channel devices, where L_{ch} is much larger than the length of electron mean free path, the transistors are fully operated in the diffusive regime, where field-effect mobility should remain constant, while the maximum drain current and the transconductance keep increasing with continuous scaling, which is inversely proportional to L_{ch}. Both extrinsic/intrinsic field dependent mobility and maximum on-state current at $V_{gs} = 50\ V$ and $V_{ds} = 2\ V$ for all devices with various L_{ch} are plotted in Figure 3.9. The peak transconductance is extracted by differentiating the transfer curve, and then calculated the extrinsic field-effect mobility by simply using the equation:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ds} \tag{3.2}$$

where μ_n is the electron mobility, C_{ox} is the MOS capacitance, W and L are the width and length of the channel, and V_{ds} is the drain voltage. The intrinsic values of the field mobility are further corrected by calculating the channel resistance at the voltage point where transconductance is at its peak, and then amended the drain voltage $V'_{ds} = V_{ds}(R_{tot} - R_c)/R_{tot}$, where V'_{ds} is the actual drain voltage applied on the channel, R_{tot} is the total resistance and R_c is the contact resistance, as both R_{tot} and R_c are known. Here, if diffusive transport for all sets of devices regardless of their channel lengths is assumed, the change of field-effect mobility at different channel length scale can be observed. It can be seen from Figure 3.9 that in the long channel regions ($L_{ch} > 500\ nm$), μ_n remains constant at around 28 cm^2/V·s. With further scaling, μ_n starts to decrease, and drops to around 17 cm^2/V·s at 100 nm channel length. Also, it can be learned from the classical square-law model that the drain current is inversely proportional to channel length, which means, the I_d-L_{ch}^{-1} relationship should present a linear characteristic. However, in Figure 3.9(b), as indicated by the red dashed line, this linear relationship applied only at long channel region ($L_{ch} > 500\ nm$). With continuous scaling down, it comes to saturate at ∼90 mA/mm at $L_{ch} = 100\ nm$. The decrease of field-effect mobility and non-

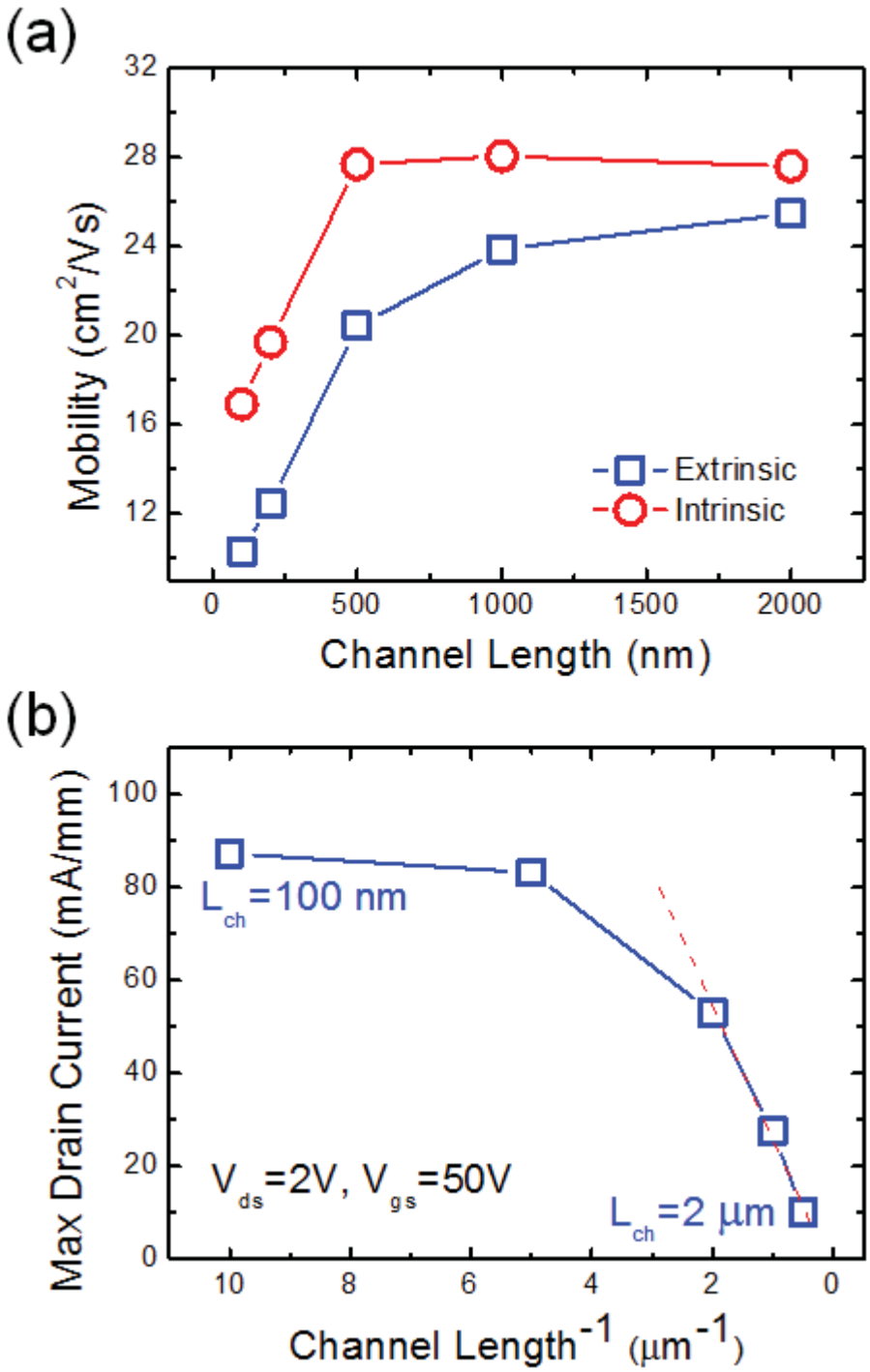

Fig. 3.9. Mobility and maximum drain current at various channel length

linearity of drain current could be attributed to two reasons. One reason is the substantial contact resistance which does not scale with channel length but is present in the device when the contact resistance is comparable to channel resistance. The second reason, if the contact resistance is ignored, is that mobility decreases since the carriers are approaching their saturated velocities at shorter channel length. [61] In general, the electric field in the channel is reversely proportional to the channel length, leading to higher carrier velocities at reduced channel length, as defined by $\nu = \mu E$. As a result, the drain current increases with reduced channel length, while field effect mobility remains constant. However, at very short channel lengths, the velocity of the carrier is getting saturated even with increase electric field. Therefore, as the velocity is approaching saturation with increased electric field, the field effect mobility calculated from the same formula would result in a decreased number, as well as the drain current is also getting saturated. By excluding the contact resistance, the field-effect mobility still shows a descending trend when L_{ch} is less than 500 nm, indicating that the contact resistance is not the only dominant factor for the scaled short channel devices, and that these short channel transistors with $L_{ch} < 500\ nm$ are showing carrier velocity saturation behaviors, which is consistent with what was observed in classical short channel silicon devices.

3.3 Channel Width Scaling of MoS_2 Transistors

In this section, the width scaling properties of MoS_2 transistors by forming nanoribbon channels will be investigated. Also, by proper width selection, the V_T of the MoS_2 transistors can be modulated to be both positive and negative will be demonstrated.

The fabrication process of sets of MoS_2 transistors is shown in Figure 3.10, as described below. MoS_2 flakes were first mechanically exfoliated and transferred to a heavily p-doped silicon substrate (0.01–0.02 Ω·cm) with a 300 nm SiO_2 capping layer. The silicon substrate served as a global back gate, while the 300 nm SiO_2 served as the gate dielectric. After the flake transfer, electron beam lithography was

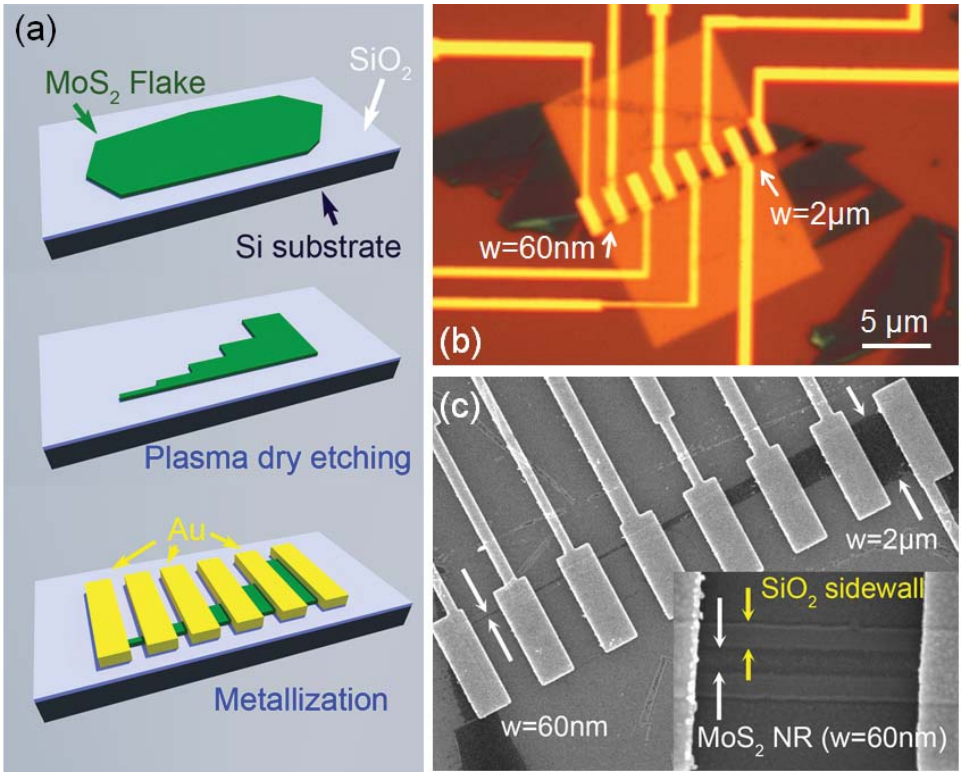

Fig. 3.10. Fabrication process and device images of MoS_2 transistors with various channel width

used to pattern the flake, followed by plasma dry etching (BCl_3: 15 sccm, Ar: 60 sccm, Pressure: 0.6 Pa, RF source power: 100 W, RF Bias Power: 50 W, time: 5 min) to remove the excess parts of the flakes, leaving connected rectangles with a fixed length (2 μm) but various widths to be used as device channels. The widths of these rectangles varied from 2 μm down to 60 nm. Finally, contacts were defined by electron beam lithography, followed by a 50 nm Au metallization by electron beam deposition. The contact bars were 1 μm wide, centered on the edge between two neighboring channel areas. The final set of devices have a fixed channel length of 1 μm and widths of 2 μm, 1 μm, 500 nm, 200 nm, 100 nm, 80 nm and 60 nm. Three sets of devices were fabricated on three large flakes with thickness of 6, 6 and 11 nm, as determined by AFM. The optical image and SEM image of these sets of devices are shown in Figures 3.10(b) and (c). Over-etching of the MoS_2, in order to guarantee

complete removal of excess MoS_2 crystals, created a rectangular step in the SiO_2 capped substrate surrounding the flake, and also created SiO_2 sidewalls at the edges of the MoS_2 channels (Figure 3.10(c) inset). Smooth edges without obvious damage by dry etching was observed at the MoS_2 nanoribbons.

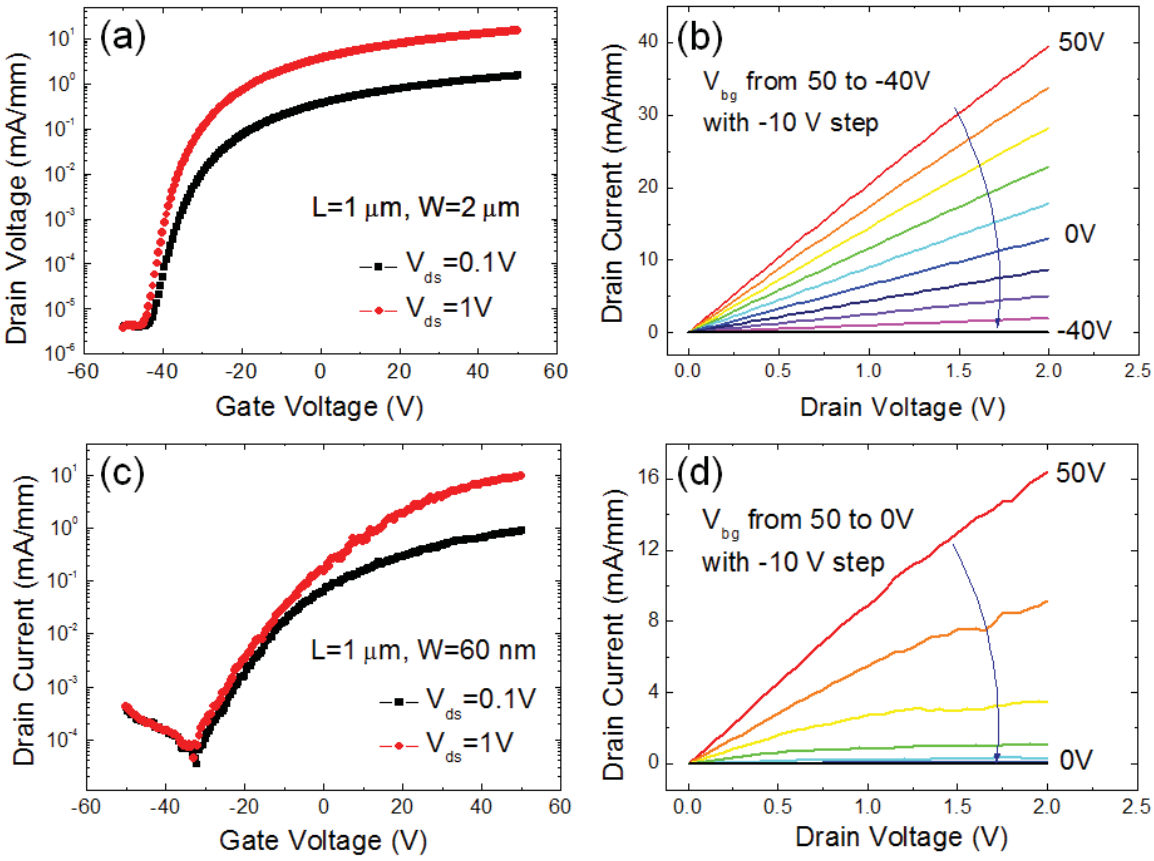

Fig. 3.11. Transfer and output characteristics of 2 μm and 60 nm channel width devices

Figure 3.11 show the transfer and output characteristics of the devices with 2 μm and 60 nm widths, selected from one of three sets of devices. These devices were fabricated using one of the 6 nm thick crystals (D1). Figure 3.11(a) shows well-behaved transfer curves from the 2 μm wide transistor. The current on/off ratio is approximately 10^7, as the ultrathin MoS_2 crystal can be easily depleted at negative

gate biases. The extrinsic field-effect mobility of this device is 21.8 $cm^2/V{\cdot}s$, which can be further improved by high-k dielectric passivation. The transfer curve of the 60 nm wide nanoribbon device is shown in Figure 3.11(c). Compared to Figure 3.11(a), the transfer curves are noisy, due to fewer conduction modes in the nanoribbons, as well as an increased leakage current at negative bias. This increased gate leakage could be ascribed as more defects are induced in the vicinity of etching windows in the SiO_2. A larger SS is also observed. The SS for the 2 μm wide device is around 2 V/dec, however for the 60 nm wide device, this value increases to almost 10 V/dec. The SS value of the 2 μm wide device indicates a reasonably good interface (interface trap density $D_{it} \sim 2.3{\times}10^{12}/cm^2{\cdot}eV$) between the MoS_2 crystal and SiO_2 dielectric. If the 300 nm SiO_2 layer is replaced with 5 nm of Al_2O_3, while assuming that D_{it} remains unchanged, the SS would be significantly reduced to ~75 mV/dec by simply applying:

$$SS = \frac{kT}{q}(1 + \frac{C_{it}}{C_{ox}}) \tag{3.3}$$

where k is the Boltzmann constant, T is the temperature and C_{ox} and C_{it} are capacitances modelling the oxide and interface traps, respectively. The differences in SS for the two devices are expected because edge roughness and defects play more important roles in nanoribbon transistors. A large difference in threshold voltages for these two devices is observed. At a 2 V drain voltage with zero gate bias, the drain current for the 2 μm wide device is 13.0 mA/mm, showing typical depletion-mode operation. However, for the 60 nm channel width device, the drain current is near zero with zero gate bias, indicating an obvious V_T shift to the positive side, signalling enhancement-mode operation. At the same $V_{ds} = 2\ V$ and $V_{gs} = 50\ V$, the highest drain current density to be 39.4 mA/mm is achieved for the 2 μm channel width device and 16.4 mA/mm for the 60 nm channel width device. This difference in normalized drain current suggests that V_T is different for these two devices, assuming that the current scales linearly with the channel width, which is verified below.

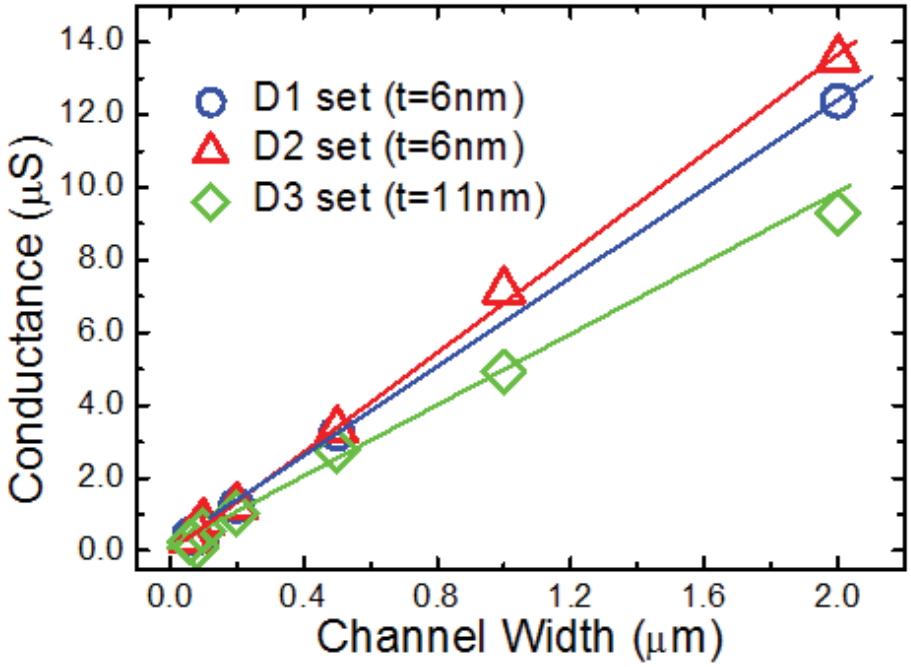

Fig. 3.12. Channel conductance of all sets of devices versus channel width

In order to confirm that the current scales linearly with various channel width, the total conductance (1 over on-resistance) versus channel width for all three sets of devices is plotted, as shown in Figure 3.12. The on-resistance (R_{on}) of the transistor has contributions from the contact resistance and channel resistance. Since the contact area and width for all transistors scales with channel width, the contact resistance should scale linearly with the channel width. The same is true for the channel resistance. After determining V_T *via* linear extrapolation from transfer characteristics, R_{on} is extracted at the same reference voltage point $V_{gs} = V_T + 26V$. It is shown that the R_{on} scales linearly with channel width. As expected, MoS_2 acts as a conventional semiconductor. The width dependent conductance is about 6-7 μS/μm for the two 6 nm thick devices (D1 and D2) and 5 μS/μm for the 11 nm device (D3).

Lastly, the V_T shift of all devices associated with the channel width is studied. The V_T is extracted from the linear extrapolation method at a low drain voltage. V_T is calculated by $V_T = V_{GSi} - V_{ds}/2$, where V_{GSi} is the intercept gate voltage,

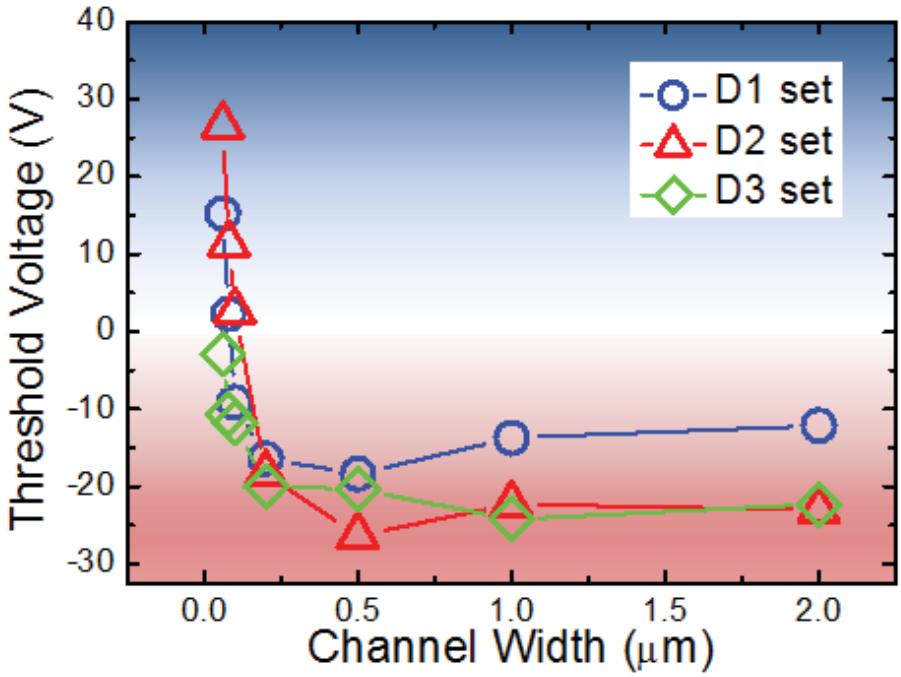

Fig. 3.13. Threshold voltage of all sets of devices versus channel width

and V_{ds} is the drain voltage. [56] Threshold voltages for all three sets of devices are plotted in Figure 3.13. Similar trends can be observed for all sets of devices. The V_T remains constant for transistors with wider channel width ($W > 0.5\ \mu m$). As the width of the channel is narrowed down to 200 nm, it appears that the V_T shift to positive values. Apparently, transistors with thinner bodies (D1 and D2) are more likely to be influenced by this effect. For one of the 6 nm thick set of transistors (D2), the threshold voltage ultimately shifts from -20 V to 30 V, indicating a clear transition from being a depletion-mode transistor to being an enhancement-mode operation just by trimming down the channel width. The geometry of these nanoribbon transistors with channel width less than 100 nm has a similar structure to Si FinFETs. Same trends of V_T shift have also been observed in Si FinFETs as well as InGaAs nanowire transistors. This narrow channel effect was ascribed to the lateral expansion of depletion layer due to fringing field effect or quantum confinement in device channels. [62–64] However, the channel widths are strictly defined in the MoS_2

transistors thus they cannot have a lateral expansion in depletion layer. Also, they are much wider than those of these Si FinFETs and InGaAs nanowire MOSFETs. This V_T shift is expected to be due to edge depletion, similar to what has been observed in majority carrier GaN nanoribbon devices. [65] The edge depletion could be induced by either electric fields or ambient molecules (e.g. H_2O) adsorbed at the MoS_2 surface. Given previous surface study of ALD growth on 2D crystals, these polarized molecules can be strongly adsorbed at MoS_2 surface and even persist at 300–400 °C. As expected, the V_T of the devices fabricated on the thicker crystal (D3) show relatively minor shifts compared to the devices with thinner flakes, as shown in the same figure. The observation of V_T shifts for MoS_2 transistors with width scaling is important. The 2D nature of MoS_2 and other TMD based transistors makes them difficult to engineer the channel through doping. This demonstrated approach, using the width to achieve V_T adjustments on the same starting channel material in order to realize both enhancement-mode and depletion-mode operation, is a simple and favorable method for circuit designs such as to realize an enhancement-mode/depletion-mode based inverter.

3.4 Summary

In this chapter, MoS_2 MOSFET with ALD Al_2O_3 as top-gate dielectric is experimentally demonstrated. AFM, C-V and I-V studies show that ALD high-k dielectrics can be directly deposited on MoS_2 at low growth temperatures and the MoS_2/Al_2O_3 interface is of good quality. For short channel devices, despite the devices being fabricated on a 300 nm thick SiO_2 gate dielectric, the results show the superior immunity to short channel effects down to 100 nm channel length. Transport studies are were also performed, where the calculated field-effective mobility degradation and maximum current saturation are observed at short channel lengths attributed to carrier velocity saturation. In addition, the effect of the channel width scaling is investigated. A significant threshold voltage shift from negative to the positive for transistors with

channel widths of less than 200 nm is observed, showing a clear transition from depletion-mode to enhancement-mode operation simply by channel width trimming.

4. METAL CONTACTS ON 2D SEMICONDUCTORS

In this chapter, the properties of metal contacts on 2D semiconductors will be discussed. In the first part, contact resistance of metal contact on MoS_2 will be extracted by classical transmission line method (TLM). Also, Schottky barrier heights (SBH) would be determined by a temperature dependent study. With a comparative study with metal contacts on WSe_2, Fermi-level pinning is revealed at the metal/2D interface.

4.1 Contact Resistance on MoS_2

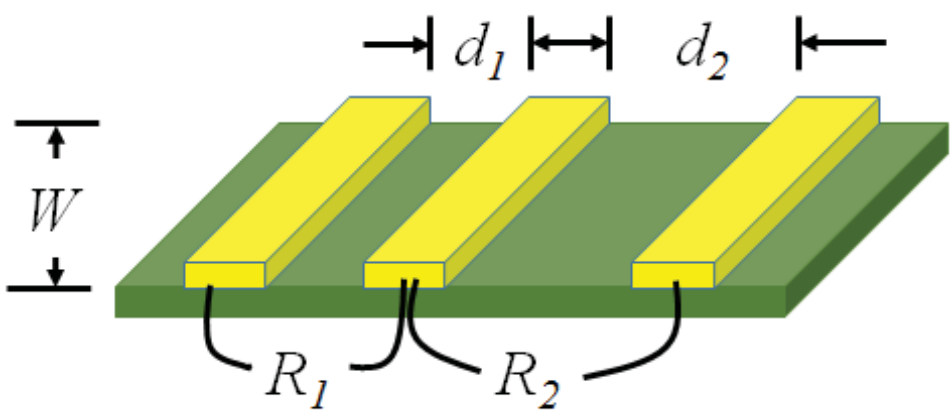

Fig. 4.1. Illustrative picture of transmission line method

The contact resistance at metal/MoS_2 interface can be extracted with classical transmission line method. Figure 4.1 shows the simplest three-terminal device structure to extract both sheet resistance as well as contact resistance. In this test structure, metal contacts with different spacing d_1 and d_2 are defined on a piece of semiconductor crystal with constant width W. The total resistance between the contacts

are measured with R_1 and R_2, assuming $d_2 > d_1$, thus the contact resistance can be determined as: [56]

$$2R_c = \frac{W \times (R_2 d_1 - R_1 d_2)}{d_2 - d_1} \tag{4.1}$$

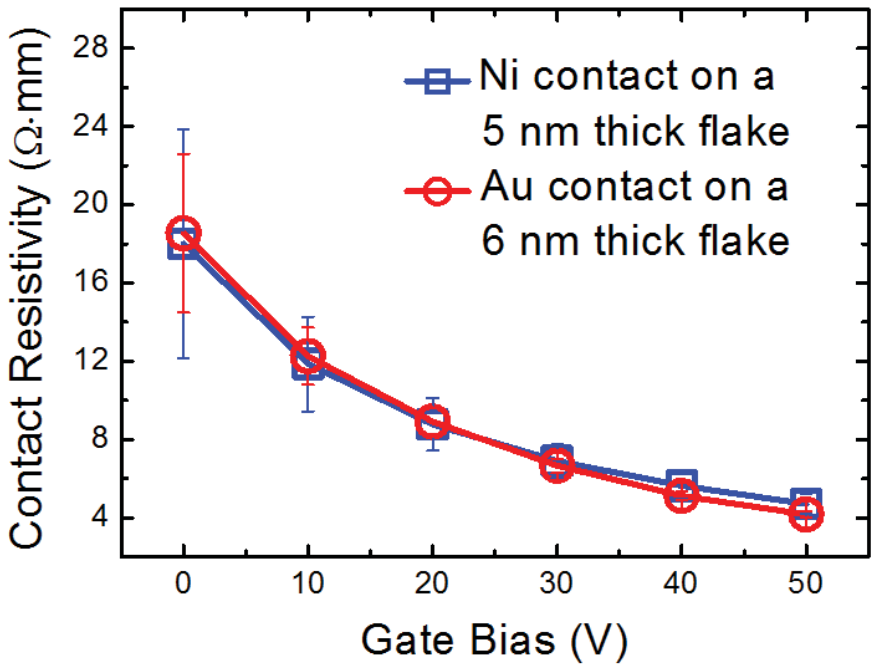

Fig. 4.2. Gate voltage dependent contact resistance of Ni and Au on MoS_2

To estimate metal contact resistance on Mos_2, similar test structure was used as shown in Figure 3.5. The width of the contact bars was defined as 500 nm. Ni or Au contact on MoS_2 were studied. No annealing is performed after lift-off process. Low-field ($V_{ds} = 50\ mV$) contact resistance from devices with larger channel length ($L_{ch} > 200\ nm$) were studied. This is much larger than the carrier mean free path in the channel, and the electron transport is in the diffusive regime. The measurement was performed at room temperature. As depicted in Figure 4.2, the contact resistance shows a strong dependent on the back gate bias, as the MoS_2 is electrically-doped under high gate bias, leading to a smaller contact resistance. The

smallest R_c measured in the Ni/MoS_2 junction is 4.7±0.5 Ω·mm at 50 V back gate bias, and increases to 18.0±5.9 Ω·mm at zero back gate bias. The contact resistance is about 40 times larger than the Pd/graphene contact, mostly attributed to the lack of SBH at metal/graphene junction. Note that the error bars on the left side are significantly larger than those on the right, where the channel is heavily doped, attributed to a large contact resistance on MoS_2 at lower gate bias, leading to an enhanced absolute error, which is also observed in former graphene TLM study. [66] This gate dependent R_c can be attributed to two reasons. One is the existence of Schottky barrier at the Ni and MoS_2 interface, as gate bias would change the tunneling efficiency due to band bending at the semiconductor surface, and the other can be understood as the change in the number of the conduction modes in low-dimensional systems, as which can be seen in the graphene examples. [66, 67] In this case, the Schottky barrier is the dominant factor, as MoS_2 is not a material with low density of states at the conduction band edge. As a comparison, an Au/MoS_2 TLM structure is also fabricated on another flake with similar thickness (∼6 nm), while contact resistance is shown in the same figure. Despite the variance in different flakes, these results reveal close contact resistance under the same range of field dependence. The Schottky barrier between MoS_2/Au junction is also confirmed by previous temperature dependence study, where the measured mobility was showing strong degradation at lower temperature. It could be understood as the increasing contact resistance at lower temperatures due to the reduced thermionic emission. [68]

To further understand the influence of the contact resistance in device performance, the output curves of all sets of devices with various channel lengths in their "ON" state. The I_d-V_d characteristics in Figure 4.3 show how scaling affects the on-resistance (R_{on}) and drain current at a fixed gate voltage. The R_{on} has contributions from both the channel resistance and the contact resistances. Ideally, R_{on} should decrease linearly with the scaling of channel length. Such a decrease would be characterized by the increase of the I_d-V_d slope at low drain bias, where acoustic phonon scattering is dominant.However, this trend fails to hold for short channel devices, as

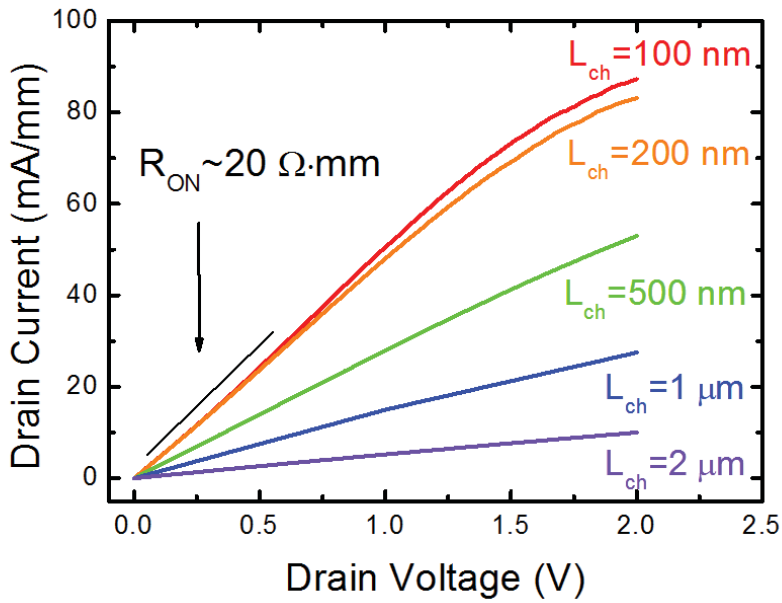

Fig. 4.3. Output curves at the same 50 V gate bias with different channel length

seen by comparing the 100 nm and 200 nm devices. For these short channel devices, R_{on} saturated at ~20 Ω·mm at $V_{ds} < 0.5\ V$. The actual saturated R_{on} would be lower than this value if run-to-run variations is considered in measurement of the V_T, mostly originating from fixed charges in the oxide. [48] In the meantime, it can be seen from Figure 4.3 that the contact resistance at 50 V gate bias is around ~5 Ω·mm, which equals to 10 Ω·mm for the total contact resistance. This indicates that R_{on} with $L_{ch} \leq 200\ nm$ is largely composed of the contact resistance, since the channel resistance is be small or even negligible at these channel lengths. R_c dominance is not desirable for short channel transistors, which can be understood from two ways. One is that it makes further aggressive scaling worthless, for the R_{on} no longer has a substantial dependence on the channel and thus the drain current does not increase with scaling. And the other reason is that the drain voltage applied would be mostly loaded by the contact resistance instead of the channel resistance and result in a degraded lateral electric field in the channel, making it difficult for the drain current

to reach the current saturation regime unless a very large drain voltage is applied, as observed in Figure 4.3. Slight current saturation occurs only at 100 and 200 nm channel length near the 2 V drain bias. That is to say, due to the large contact resistance at metal/MoS_2 junction, which overshadows the gradual change in the channel resistance, these transistors are operating way below their intrinsic performance limit.

For MoS_2, the charge neutrality level is aligned at the vicinity of the conduction band, making it easy to fabricate an n-channel MOSFET on this material. [58] It is assumed that the metal contact on MoS_2 is weakly pinned at 100 to 200 meV below the conduction band, so to understand that both high work function metal (Au, Ni) and low work function metal (Ti) worked well for a reasonable contact to MoS_2 at room temperature, as show in this and some other previous studies. [5,48,68] To investigate the metal contact on MoS_2, temperature-dependent current density of Ni/MoS_2 Schottky contact is measured to determine the effective Schottky barrier height (SBH). The current of the pure Schottky diode is:

$$I = A^* A T^2 exp(q\Phi_B/kT)[exp(qV/nkT) - 1] \tag{4.2}$$

where A^* is the Richardson constant, A is the area of the metal contact, T is the temperature, q is the electron charge, Φ_B is the effective SBH, k is the Boltzmann constant, n is the ideality factor, and V is the applied forward voltage. For Schottky diodes biased at $V > 3kT/q$, the effective SBH Φ_B can be accurately extracted from the slope of temperature dependence of $ln(I/T^2)$ versus T, as shown in the inset of Figure 4.4. Figure 4.4 plots the extracted SBHs as a function of back gate bias, which electrostatically dopes MoS_2. It is not surprising to see that the effective SBH is sensitive to the doping concentration of MoS_2 and decreases from maximum 100 meV to near 0 eV (Ohmic). The existence of a small Schottky barrier between metal and MoS_2 is confirmed by this experiment. A transparent Ohmic contact scheme on MoS_2 must be developed before the realization high-performance short channel MoS_2 transistors with a competitive contact resistance with the state-of-the-art semiconductor device technology, that is, 0.1 Ω·mm. A comprehensive study of

the metal/MoS_2 interface is critical to understand the origins and limitations for the metal/MoS_2 contacts.

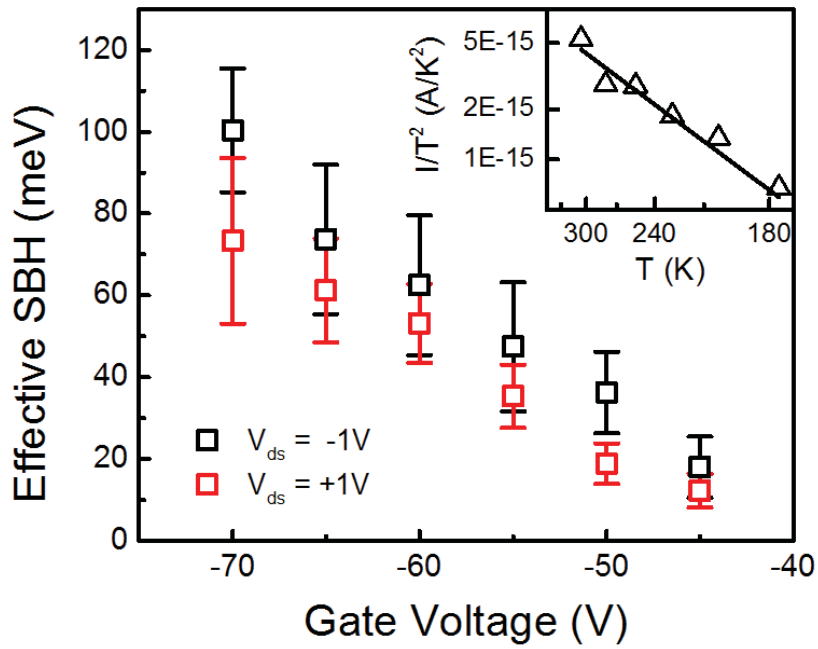

Fig. 4.4. Effective Schottky barrier height Ni/MoS_2 as a function of back gate voltage

4.2 Metal Contacts on WSe_2

Besides MoS_2, WSe_2 is another promising 2D semiconductor for optical and electronic applications. Bulk WSe_2 is an indirect band gap semiconductor with E_g = 1.2 eV with carrier mobility (both electrons and holes) up to 500 cm^2/V·s. [69] In this section, the role of metal contact on WSe_2 thin flakes will be studied, and hence to reveal how polarities of the transistors are determined with metal contacts.

WSe_2 flakes were mechanically cleaved from bulk crystals as described in previous sections. These thin crystals (∼20 nm) were then transferred to heavily doped silicon substrates which are capped with 90 nm SiO_2. A 2-hour acetone bathing was carried

afterwards to remove tape residues. Metal contact regions were defined by electron beam lithography. Ti/Au of 30/50 nm and Pd of 40 nm were separately deposited by electron beam evaporator. The samples were then annealed in argon at 350 °C for 30 seconds for better contacts. Device characterization was carried with Keithley 4200 Semiconductor Characterization System.

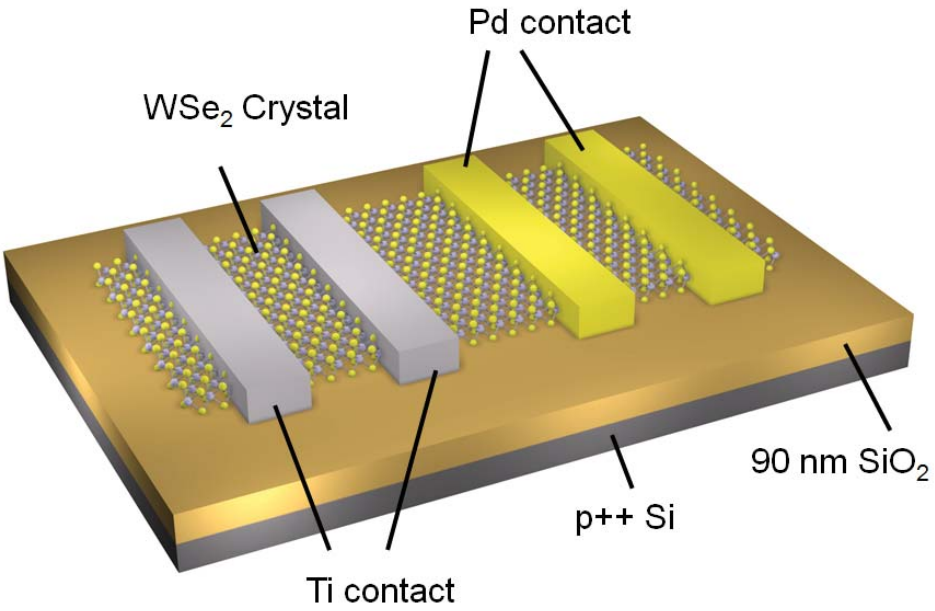

Fig. 4.5. Schematic image of WSe_2 devices with Ti and Pd contacts

Figure 4.5 shows the schematic diagram of fabricated device. Heavily doped silicon was used as the back gate and the 90 nm SiO_2 served as the gate dielectric. Ti and Pd electrodes were deposited on same flakes for comparison to avoid variance in different crystals. The width of the contact metal was 1 μm and the channel length of the devices is 500 nm for both Ti and Pd contacted devices.

The work functions of Ti and Pd are 4.33 eV and 5.2 eV, respectively. The ionization potential of WSe_2 is 4.8–4.9 eV. [70] The band alignment of Ti and Pd contacts on WSe_2 is qualitatively shown in Figure 4.6, if FLP at metal/crystal interface is ignored, or there is a thin air gap between the metal and semiconductor. In comparison, the band edge alignment of MoS_2 is also depicted for later reference. By simple

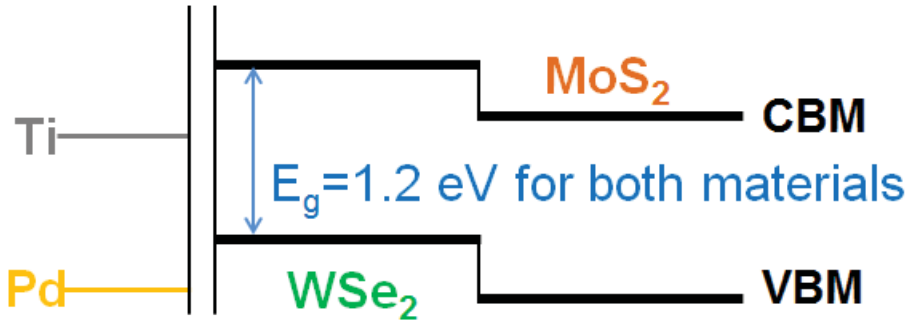

Fig. 4.6. Band edge alignment for Ti and Pd contacts on MoS_2 and WSe_2

calculation it can be seen that the Ti is aligned at ∼0.1 eV above the mid-gap, while Pd is aligned deep in the valence band. This indicates that WSe_2 transistors with Ti contact should behave as an ambipolar transistor, with higher electron current than hole current (if simply assume the mobility of the two carriers are close), while they would be p-type transistors for Pd contact.

The transfer curves of a typical device are shown in Figure 4.7. The drain biases in this measurement for the transfer curves were 0.05 V and 1 V respectively. The orange curves represent the device performance of Pd contacted transistors and the grey ones represent devices with Ti contacts. Away from the assumptions, both Ti and Pd contact devices show ambipolar behavior. At 1 V bias, highest electron current of 0.7 mA/mm was achieved for Ti contact, and this number decrease to 0.14 mA/mm for the Pd contact device. On the other hand of hole current, the Pd contact device shows a maximum of 4.9 mA/mm at -50 V gate bias, however this number drops to 0.01 mA/mm at same bias for Ti contact devices. The ratio between electron and hole current is less than three orders. This implies the assumption that FLP does not exist at metal/2D crystal interface is probably not correct. Instead, the Fermi levels of Ti and Pd contacts are both weakly pinned in the vicinity of the mid gap. Nevertheless, the maximum electron current is ∼100 times larger than the maximum hole current for Ti contact devices, while for Pd contacts, maximum hole current is ∼20 times larger than the electron current. If mobility for both carriers are

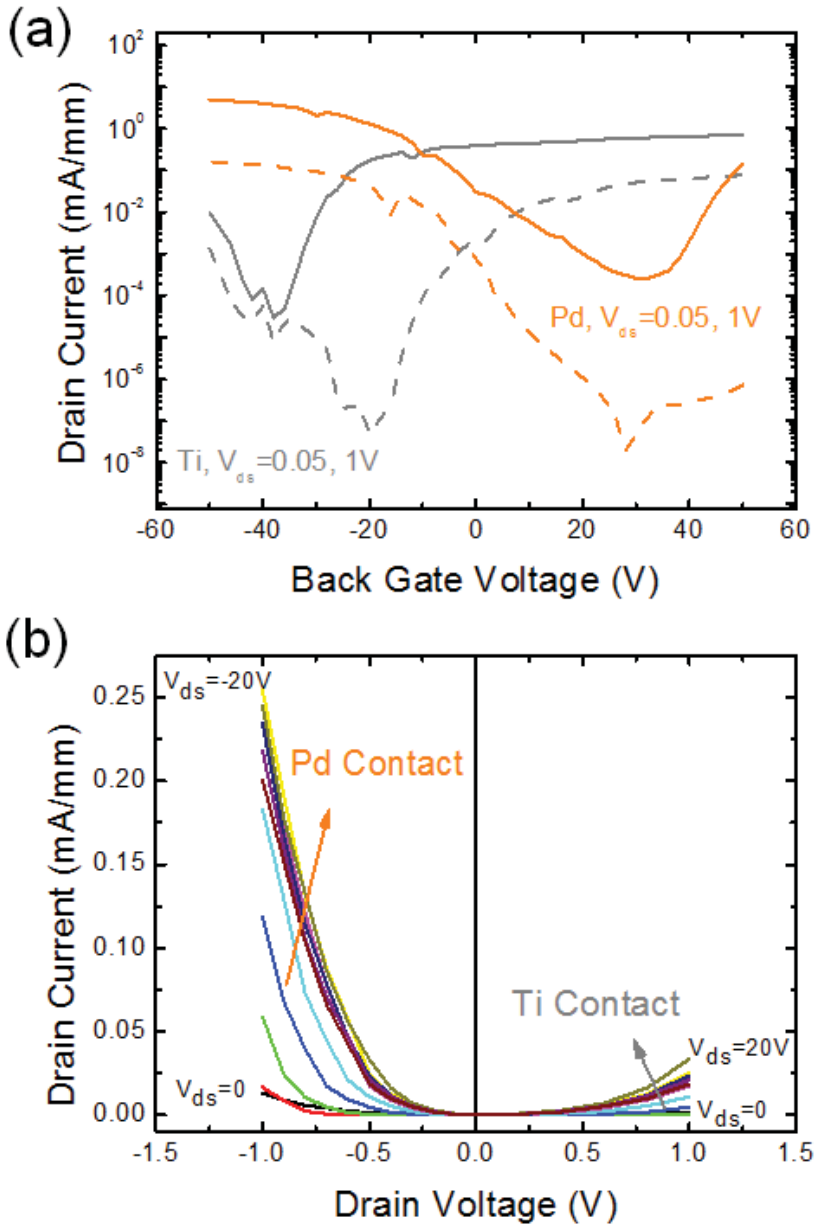

Fig. 4.7. Device characteristics for Ti and Pd contacted WSe_2 transistor

close to each other is assumed, then it is clear that the Fermi-level position for both contacts are not exactly at the same place, while the alignment of Ti is slightly higher than the Pd counterpart, in the same trend of their work functions. But still, large Schottky barriers heights are expected for both carriers, even for the hole barrier in

Pd contact devices and electron barrier in Ti contact devices This is also confirmed by the non-linearity in output curves shown in Figure 4.7(b), where large Schottky barriers of electrons to Ti contacts and holes to Pd contacts are observed.

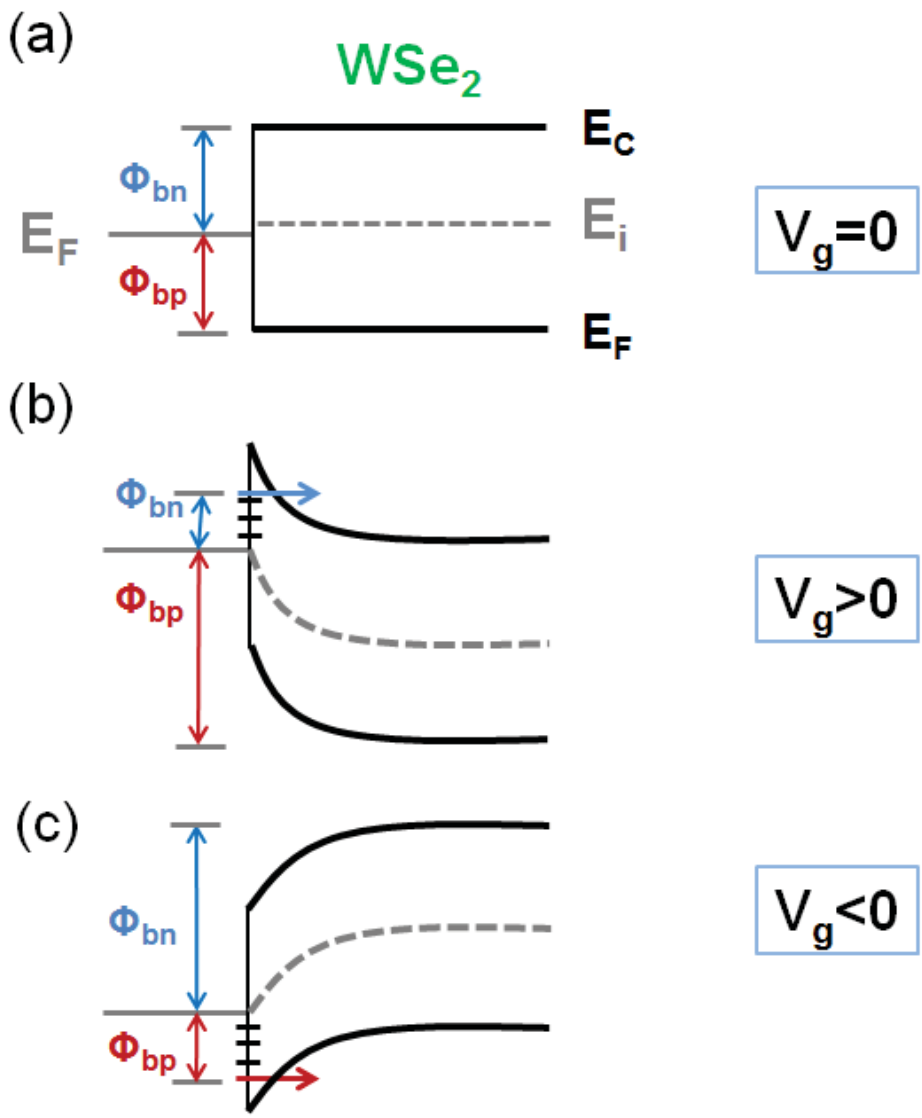

Fig. 4.8. Schematic diagram of carrier transport at metal/WSe_2 interface

4.3 Fermi-level Pinning at Metal/2D Interface

The carrier transport across the metal/2D crystal interface of these ambipolar transistors can be illustrated in Figure 4.8 under three regimes of gate biasing. If the electric field originated from charges and traps in the gate oxide or at the interface is ignored, at zero gate bias, the effective Schottky barrier heights are strictly determined by the position of the Fermi Level, for electrons, the barrier height can be written as: [71]

$$\Phi_{bn} = \Phi_{bn0} + D = E_C - E_F + D \tag{4.3}$$

where Φ_{bn0} is the electron barrier height without the effect of FLP, E_c and E_F are the energy of the conduction band edge and Fermi level in the barrier region near the interface, D is the dipole at the interface created by the finite density of states throughout the band gap of the semiconductor near the interface. This dipole definitely raises or lowers the actual barrier (Φ_{bn0}). At positive bias, the bands bend downwards at the interface, resulting in an increase of the Schottky barrier heights of the holes. On the other side, the effective Schottky barrier height of electrons is decreased due to thermal assisted Fowler-Nordheim tunnelling. Also, the gap states of the semiconductor near the interface help the tunnelling as well. Therefore, the hole current is eliminated, while the electron current is dominating. *Vice versa* for the enhanced hole current and reduced electron current at negative bias. This indicates that the device performance completely relies on Schottky barrier heights of carriers, which is determined by the position of the FLP. This may not be a serious problem in conventional semiconductors, where a heavy source/drain doping would significantly facilitate the tunnelling from metal to semiconductor, hence contact resistance is negligible unless channel length is scaled to ballistic regimes. However, for 2D semiconductors, FLP could be serious barrier to improve device performance due to the absence of an effective doping method. If the Fermi levels of the metal contacts are pinned at mid gap, the device would behave more like an ambipolar transistor with large SBHs for both electrons and holes. For mid gap pinning, these transistors

are more sensitive to the minor change in the position of the Fermi level change, as observed in the Ti and Pd contact WSe_2 devices. Though the carrier transport properties of both electrons and holes can be observed in an ambipolar transistor, the existence of a large contact resistance hinders the extraction of the important parameters, such as carrier mobilities. The low current level ($I_d < 10\ mA/mm$) also prevents them from further application in some areas, e.g. logic circuits. If the Fermi level is pinned near the conduction (valence) band edge, the device would behave as a n-(p-)type transistor, and this would be more favorable from device aspects, where large current and small contact resistance would be much easier to achieve.

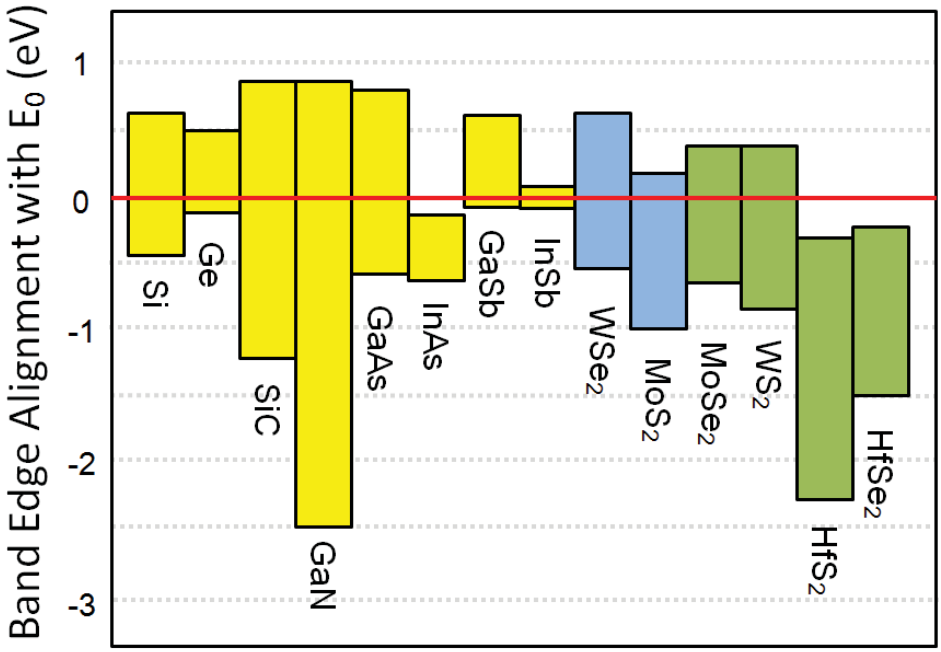

Fig. 4.9. Band edge alignment of conventional semiconductors and layered semiconductors

Some previous research has already studied the band edge alignment in layered semiconductors. [72] The charge neutrality level still prevails if the band edge alignment of metals on 2D semiconductors is incorporated to the classical picture. Figure 4.9 shows the band edge alignment of both conventional (yellow squares) and layered

semiconductors (blue and green squares). The red line represents the charge neutrality level. It is long recognized that some materials are more favorable for n-type transistors (InAs) while some others are better for p-type transistors (Ge, GaSb). This is up to the charge neutrality level that determines the pinning position. For other materials with charge neutrality level in mid gap, they can be fabricated in both n- or p-type transistors with less difficulty (Si, GaAs). The band edge alignment of the semiconductor materials has revealed such nature in those conventional semiconductors. For 2D semiconductors, the law of charge neutrality level is still applicable. In WSe_2, the charge neutrality level is deep in the mid gap, which predicts an ambipolar behavior for WSe_2 transistors, in good agreement of the experimental observations. Comparatively, the charge neutrality level in MoS_2 indicates the metal contact to MoS_2 will be pinned near the conduction band edge, with a $\sim$0.2 eV Schottky barrier height for electrons. Hence there will be only n-type MoS_2 transistors with a much reduced contact resistance.

With understanding the Fermi-level pinning at metal/2D semiconductor interface would further help to increase the device performance. With a partial Fermi-level pinning, low-work function metals such as titanium would be a more suitable metal for S/D contact in n-type MoS_2 transistors. Figure 4.10 shows the output and transfer curves of a dual gate MoS_2 transistor of similar structure to WSe_2 transistors with Ti contacts. The gate length of MoS_2 transistors is 500 nm as well for both top and back gates. A 16 nm Al_2O_3 was used as gate dielectric and Cr/Au of 20/60 nm as metal gates in MoS_2 transistors. Transconductance is also plotted. The current on/off ratio is over 10^{10} for back gate device and 10^7 for top gate ones in the measurement range. Maximum drain current is 268 mA/mm at $V_{ds} = 4\ V$ for back gate n-type MoS_2 transistor, and 200 mA/mm and transconductance of 15 mS/mm for top gate biasing. As a matter of fact, in top gate devices, the contact resistance cannot be reduced at high gate bias due to lack of a global gate. Nonetheless, the small gap in drain current between top and back gate devices indicates the contact resistance is much smaller than the channel resistance at ON-state. This is mostly due to the

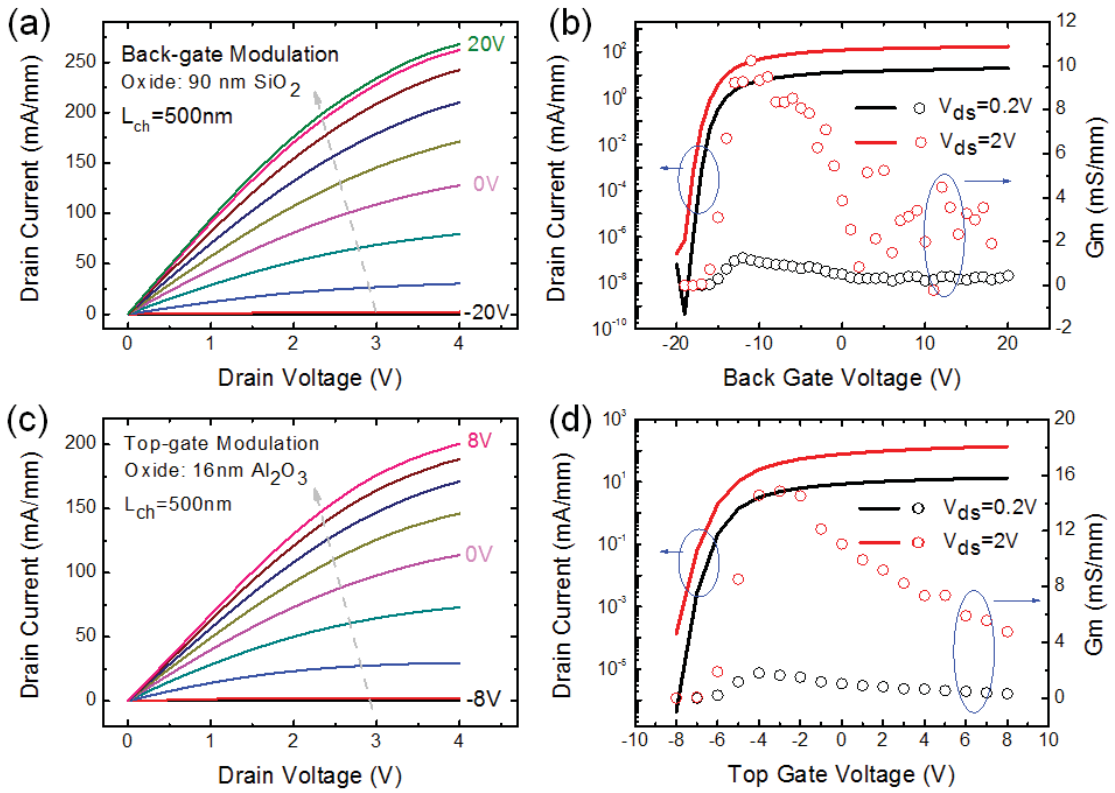

Fig. 4.10. High performance MoS_2 transistor with low work-function Ti contacts

position of charge neutrality level in MoS_2. The Fermi-level pinning me metal/MoS_2 interface near the conduction band minimum was also observed in a previous study, which is consistent with both this data and the theoretical results as well. [12] The charge neutrality level also predicts that the FLP in HfS_2, $HfSe_2$, ZrS_2, $ZrSe_2$ would be in the conduction band and WTe_2 in the valence band (some of those are not plotted). These materials would gain more advantage over MoS_2 in device applications, as a better ohmic contact for electrons or holes would be easier to achieve.

4.4 Summary

In summary, contact resistance between MoS_2 and metal is studied. A weak Fermi-level pinning at metal/2D semiconductor interface is determined in both MoS_2 and WSe_2 transistors. The energy level of FLP is determined by the position of charge neutrality level in the band edge alignment. High performance dual gate MoS_2 transistors were realized by using low-work function titanium as metal contacts.

5. DEVICE PERFORMANCE AND SWITCHING MECHANISM IN CVD MOS_2 TRANSISTORS

In this chapter, transport properties in CVD single layer MoS_2 will be focused. MOSFET devices will be faricated on CVD single layer MoS_2 samples. A statistical study on the device performance will be investigated. Also, metal contacts will be discussed and the switching mechanism in CVD single layer MoS_2 transistors will be revealed.

5.1 CVD Synthesis of Single Layer MoS_2 Crystals

Chemical vapor deposition (CVD) has been proved to be a good method for 2D crystal growth. Typically, this synthetic route provides a low cost path to high-quality, large-area and thin films. A variety of 2D crystals, such as graphene, boron nitride, topological insulators, and MoS_2 have been successfully synthesized by CVD methods. [73–75] The early attempts to obtain large area MoS_2 have relied on the solid state sulfurization of molybdenum metal and molybdenum compounds, such as $(NH_4)_2MoS_4$. [31, 32] However, they suffer from nonuniformity in thickness, small grain-sizes, and difficulty in precursor preparation. In addition, the reported lower charge carrier mobility in these CVD films is not favorable for device applications. Additionally, the sulfurization of MoO_3 has been comprehensively studied and is a main approach in MoS_2 synthesis, as MoO_3 has a lower melting and evaporation temperature. Several studies have shown the feasibility of CVD MoS_2 synthesis from sulfurization of MoO_3 on Si/SiO_2 or sapphire, and this method has been adopted in this study. [33, 34]

The synthesis of MoS_2 thin films was carried out in a vapor phase deposition process. As shown in Figure 5.1, the precursors, MoO_3 nanoribbons, and sublimated

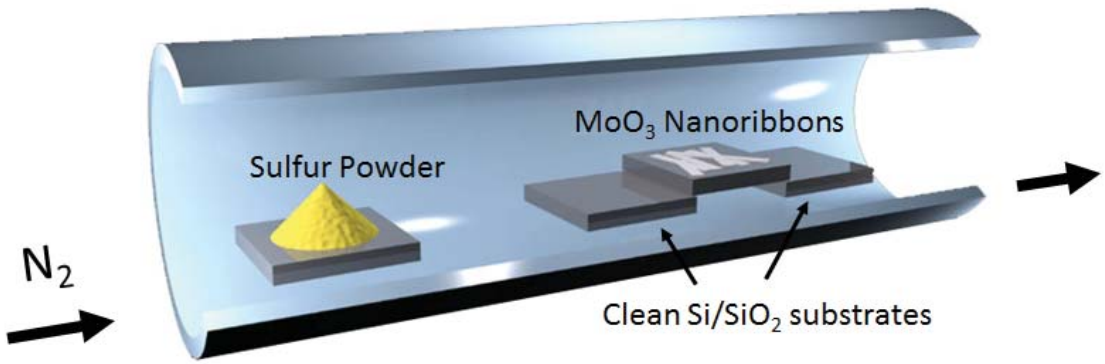

Fig. 5.1. CVD setup for MoS_2 growth

sulfur were placed separately in a quartz tube. MoO_3-covered silicon substrates, along with several clean substrates designated for the growth of MoS_2, were placed close to each other at the center of the furnace, flushed with nitrogen at a constant flow of 200 sccm. Clean heavily doped silicon substrates coated with 285 nm of SiO_2 were used, which also facilitate the direct device fabrication. A container with 0.8–1.2 g of sublimated sulfur was placed at a location reaching an approximate maximum temperature of 600 °C at the opening of the furnace. The center of the furnace was gradually heated from room temperature to 550 °C at a ramping rate of 20 °C/min. At 550 °C, the sulfur slowly evaporated and the chamber was then heated to 850 °C at a slower ramping rate of 5 °C/min. The temperature of chamber was then maintained at this temperature for 10–15 min, and then the chamber was naturally cooled back to room temperature. The chamber pressure are closely related with sulfur concentration and were monitored to optimize the growth of large triangular single crystals. [34] These materials are convenient for device fabrication and allow us to avoid complexities in transport caused by grain boundaries. A more detailed description of the synthesis process and growth kinetics can be found in earlier reports. Figure 5.2(a) represents an image of these single crystalline single layer MoS_2 samples under optical microscope. Typical triangular domain side lengths vary between 10 to

20 μm. The AFM image of the CVD MoS_2 is shown in Figure 5.2(b). The thickness of the flake is measured to be 0.85 nm, showing single layer MoS_2 with a good thickness uniformity.

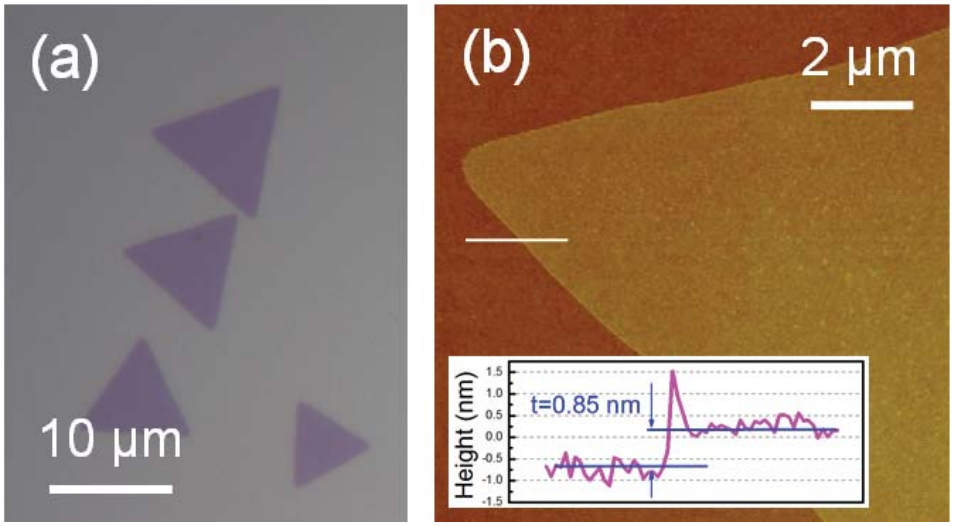

Fig. 5.2. Optical and AFM image of CVD single layer MoS_2 crystal

5.2 Device Characteristics in MoS_2 Transistors on Single Layer CVD Crystals

Previous studies on MoS_2 transistors and other devices were mostly done with the exfoliated single crystals. This gives a glimpse of the transport properties of MoS_2 and device characteristics, however, due to a large flake-to-flake variation, they suffer from a large performance deviation. In order to solve this issue, a statistical study is introduced in this section by quantitatively measuring a large number of transistors. From the statistical view, the fundamental properties of this novel electronic material will be revealed. The average values, distributions, and maximum values of the material and devices, including on-current, field-effect mobility, contact resistance, and so forth, will be shown. These parameters reflect the general information about the carrier transport of the synthesized material, the uniformity of the material, as

well as the best device performance. The information is equally important for the understanding of the potential and limitation of CVD MoS_2 films and transistors.

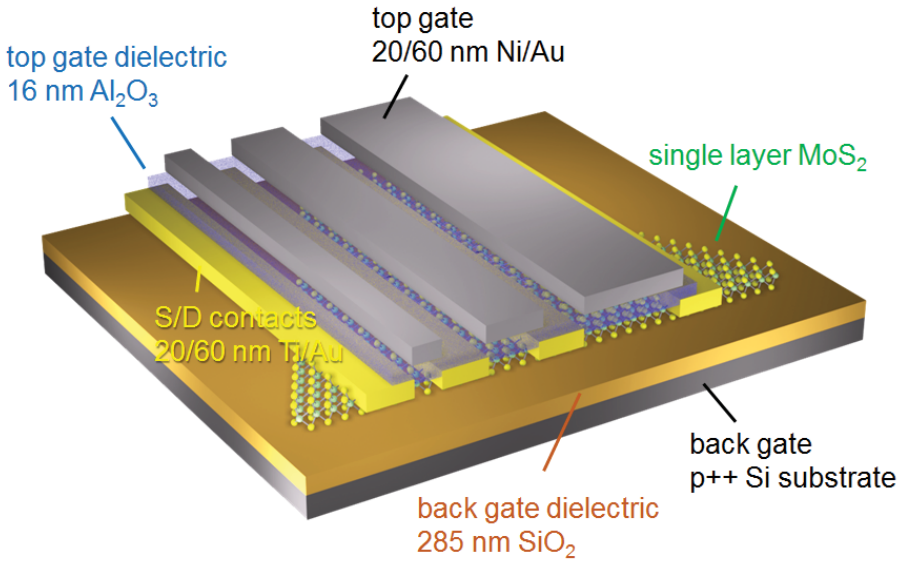

Fig. 5.3. Double gate device structure on CVD single layer MoS_2 crystal

The single layer CVD MoS_2 samples were then used for device fabrication. To start, source/drain regions were defined by e-beam lithography. The contact width of source and drain was 2 μm. The source and drain spacings, which were the channel lengths, were chosen as 100, 200, 500 nm, and 1 μm so that they cover the ranges from long channel to short channel. Ti/Au of 20/60 nm was then deposited by e-beam evaporator as the metal contacts. After the lift-off process, a 0.8–1 nm Al seeding layer was deposited at the rate of 0.1 Å/s on the whole sample to facilitate dielectric growth. The samples were then aged overnight in atmosphere to secure a complete oxidation of 1 nm Al_2O_3 as the seeding layer. After that, a 15 nm Al_2O_3 was deposited by ALD at 200 °C using TMA and water. Pulse times were 0.8 and 1.2 s for TMA and water, and purge times were 6 and 8 s, respectively. Though a temperature-dependent study on direct ALD growth on 2D crystals was discussed in Chapter 2, the insertion of the seeding layer would significantly enhance the yield of devices and minimize the leakage currents. Finally, the top gate regions were defined

by e-beam lithography again. The length of the top gate was chosen to be similar to the channel length, that is, $L_g = L_{ch}$, which reduces the access resistance of the top-gated devices. E-beam evaporated Ni/Au of 20/60 nm was deposited as the top gate metal. The final device structure is shown in Figure 5.3. A total of 120 devices were fabricated and a statistical study of their transport properties was performed using a Keithley 4200 Semiconductor Characterization Systems.

By using the double-gate structure, carrier density in the channel can be modulated by either gate. Figure 5.4(a) shows typical output characteristics of a 100 nm channel length device from back-gate modulation. The top-gate is grounded during the measurement to eliminate the capacitance coupling effect. The linear current-voltage relationship at low drain bias indicates good "ohmic" contact at source/drain regions. At 2 V drain voltage, the highest drain current of 62.5 mA/mm is achieved at 100 V back gate voltage, which is equivalent to a vertical field of 3.5 MV/cm. This is the highest drain current for CVD MoS_2 based transistors ever reported. [76] However, suffering from the thick back gate dielectric and a large interface trap density ($1.6\times10^{13}/cm^2\cdot eV$) at the SiO_2/MoS_2 interface, the transconductance is only 0.83 mS/mm. The higher interface trap density than devices based on exfoliated samples is possibly introduced from the synthesis process. [5, 17, 48] In the material growth, due to the absence of proper seeding particles, the as-grown MoS_2 films are randomly bonded with the amorphous SiO_2 substrate. [77] This not only results in difficulty in film transfer to other substrates but also resulting in a large interface trap density. This significantly jeopardizes the interface quality between the semiconducting 2D crystal and dielectric and possible transport mobility. Previous optimism on interface properties due to the nature of 2D crystal without dangling bonds needs to be investigated experimentally. With a better control of interface quality, an enhanced switching behavior in transistors can be expected. Remarkably, unlike transistors based on bulk semiconductors, which have only one semiconductor-to-oxide interface, the transistor based on layered semiconductors has two: one with top dielectric and the other with the substrate. The environment with two interfaces separated by an

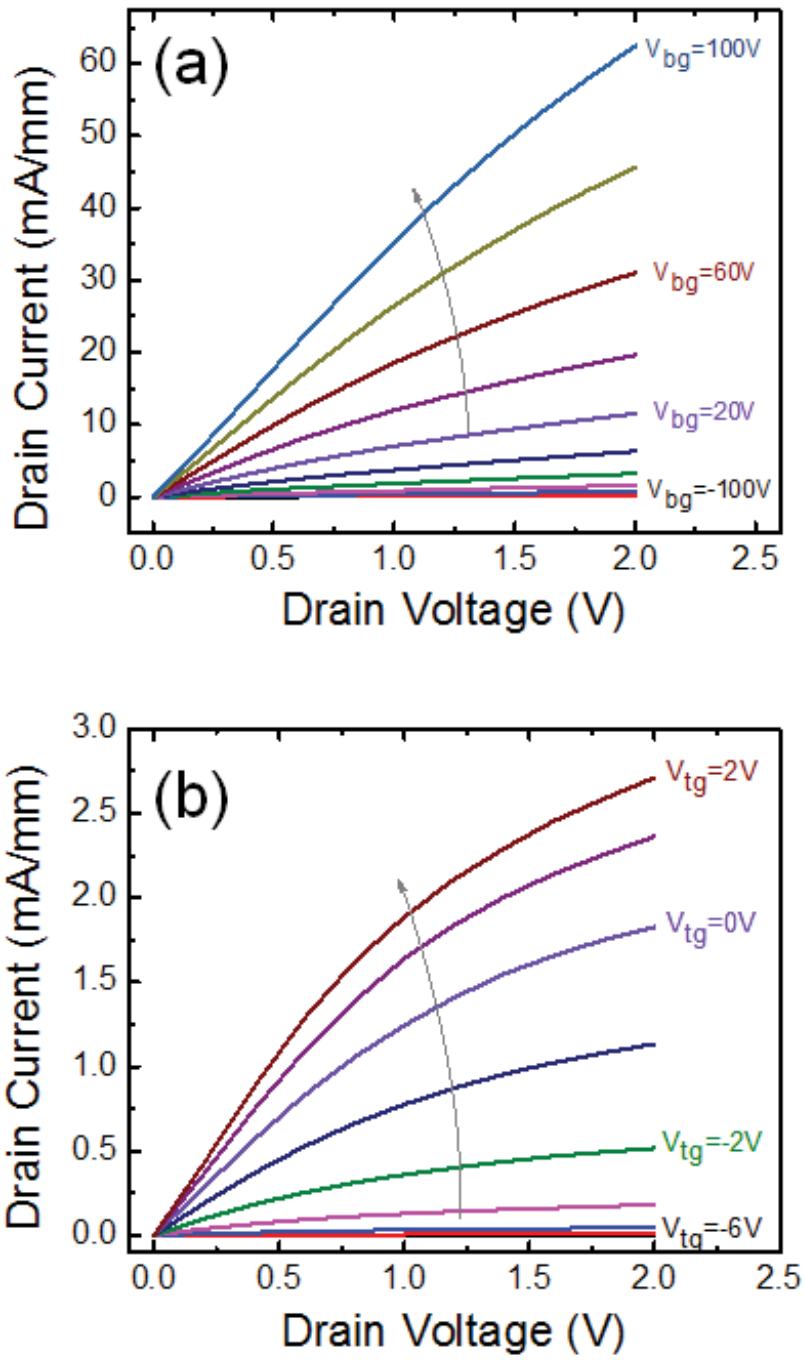

Fig. 5.4. Output characteristics of single layer CVD MoS_2 transistors

atomic layer thick semiconductor is expected to impose a strong impact to transport properties of MoS_2. A big difference between top-gate and back-gate modulations is also noticed in the same double-gate device here. The family of output curves of a top-gated device is shown in Figure 5.4(b). During this measurement, the back-gate is grounded. [6] Channel length of this device is 1 μm. Long-channel device is compared here where the device is operated in the diffusive regime and carrier velocity saturation can be ignored so as to neglect the nonideal factors. The highest on-current is 2.71 mA/mm only for the top-gate modulation where top gate bias and drain bias are 2 V. The highest drain current of this device under the same 2 V drain bias at 100 V back-gate bias is 14.9 mA/mm, 5 times larger than the drain current from top-gating. Since the channel region is fully gated by either top or back gates, this current difference is mostly originated from the variance in contact resistance. For back-gated devices, the carrier density in MoS_2 under source/drain metal contacts will be increased at higher positive gate bias. Since the source/drain regions are not heavily doped, as in conventional semiconductors, the contact resistance is mainly determined by the effective Schottky barrier height at metal/semiconductor interface. [11, 12] With large gate bias, the conduction band bends downward at the metal/semiconductor interface to enhance tunneling current thus reduce contact resistance. Therefore, it facilitates carrier injection from metal contacts to MoS_2. It also can be easily understood by electrostatic doping of MoS_2 underneath source/drain contacts to reduce contact resistance with positive back-gate bias. On the contrary, the top gate has no effect on the carrier density of MoS_2 under the source/drain thus the contact resistance remains constant even at large positive bias. The contact resistance issue would be further discussed in later parts.

Compared to MBE grown crystals, devices made on CVD samples are usually with larger performance variance. Usually, CVD samples have small domain size, random crystal orientation, the existence of grain boundaries and large defect density. These nonideal phenomena have been observed in both graphene and MoS_2 CVD films. [34, 78] Therefore, a statistical study of the key parameters of devices is necessary in

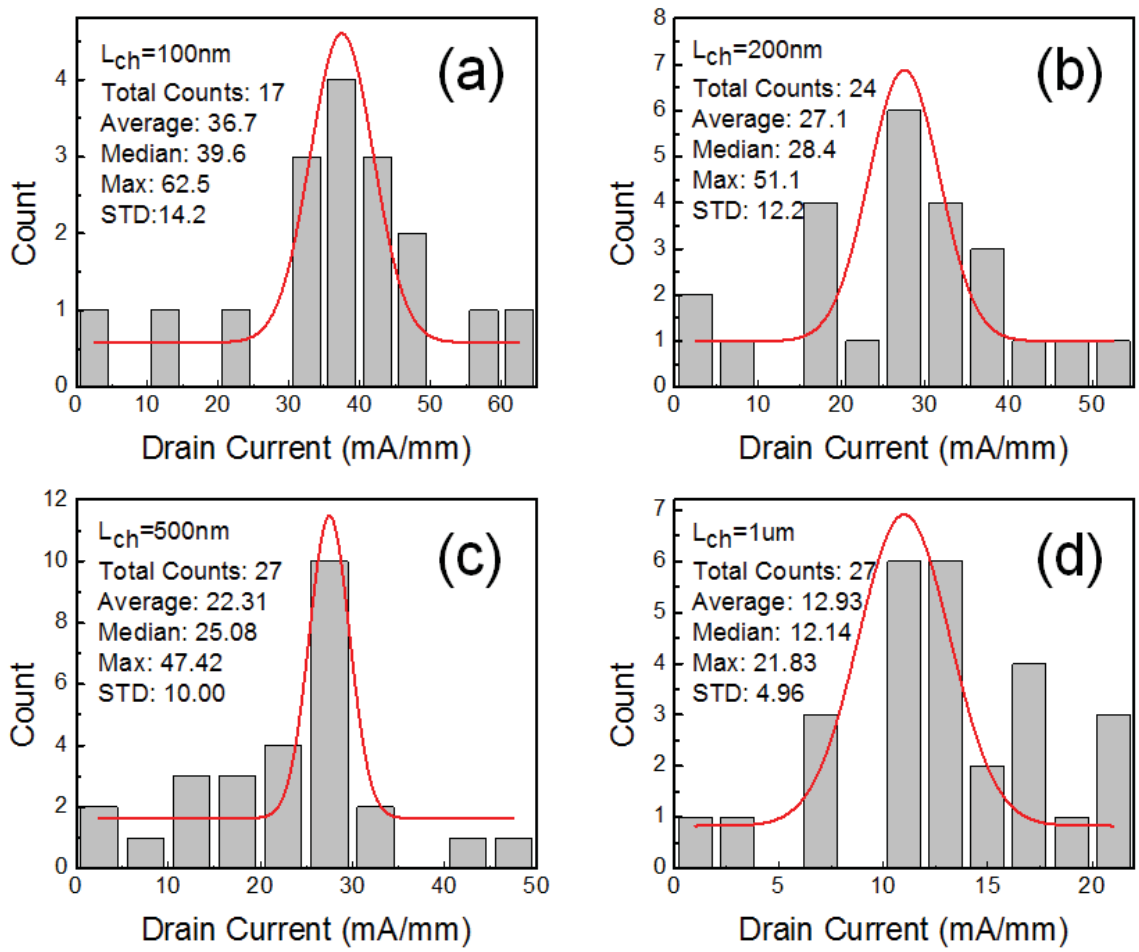

Fig. 5.5. Maximum drain current distributions of the devices with various channel length

order to gain a comprehensive understanding of the electrical properties of the CVD grown samples. Figure 5.5 shows the distributions of the maximum drain currents at different channel lengths. All values are extracted at 2 V drain bias and back-gate voltage of 100 V. The variance in device threshold voltages is ignored in the context of this statistical study. A total of 17–27 devices are studied for each channel length. As expected, these figures show a broad distribution for the maximum drain current at all channel lengths. This can be attributed to the nonuniformity of material synthesis and device fabrication; however they show a normal distribution in all sets

of data. The average and standard deviation of the measured drain currents are $36.7 \pm 14.2, 27.1 \pm 12.2, 22.3 \pm 10.0$, and 12.9 ± 5.0 mA/mm for 100, 200, 500 nm and 1 μm channel lengths, respectively.

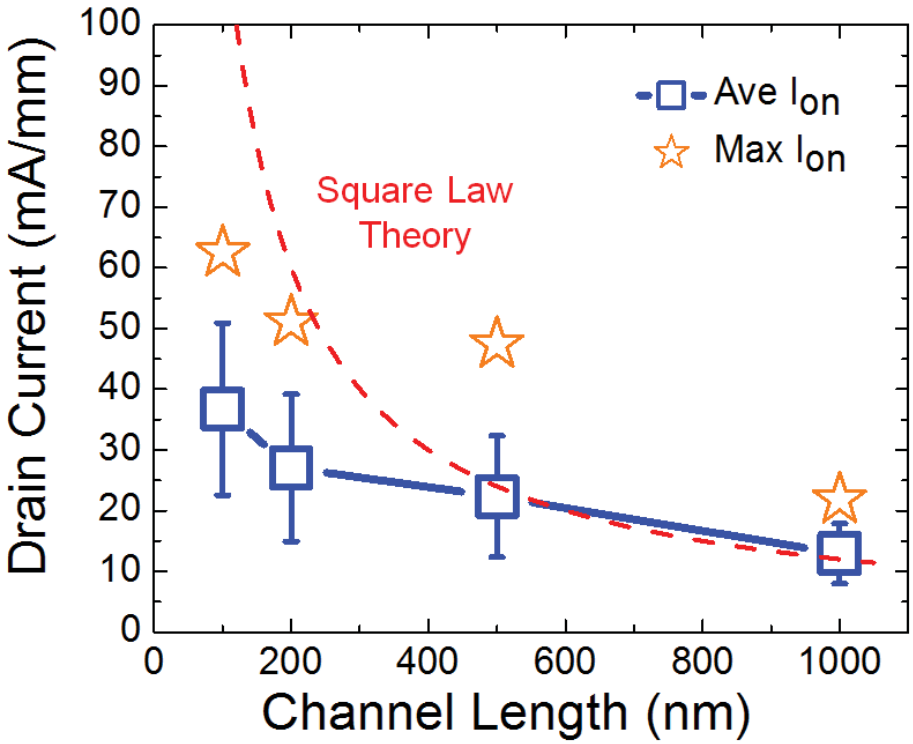

Fig. 5.6. Averaged values of maximum drain current at all channel lengths

The channel-length dependent average value with standard deviation and the maximum value measured are plotted in Figure 5.6. From long channel to short channel devices, the increase in drain current indicates the scaling properties in CVD MoS_2 transistors. Assuming the carriers follow the diffusive transport in all channel lengths, the saturated drain current exhibits as:

$$I_{ds,sat} = \frac{1}{2}\mu_{FE}C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{5.1}$$

by Square Law Theory, where μ_{FE} is the field-effect mobility, C_{ox} is the gate oxide capacitance, W and L are the width and length of the channel, and V_{gs} and V_{th} are the gate bias and threshold voltage. [79] This shows that drain current is inversely

proportional to the channel length, and this trend is drawn by the red dashed line in Figure 5.6. The deviation of drain current at shorter channel lengths is associated with two factors. One is that contact resistance does not scale with channel length, and the impact of this factor is magnified in transistors with ultrathin body semiconductor due to the larger contact resistance. [11] Another reason is the velocity saturation in CVD MoS_2 transistors, where carriers have been approaching the maximum drift velocity in short channel devices, as observed in most conventional semiconductor transistors.

5.3 Extraction of R_c in Single Layer CVD MoS_2 Transistors

As stated in Chapter 4, the major issue for 2D semiconductor based transistors is the existence of a large R_c, which drastically restrains the drain current. The fundamental reason for the large R_c is that the Fermi level pinning at the metal/semiconductor interface that results in a notable Schottky barrier height. However, their atomically thin body makes it difficult for the realization of source/drain engineering such as ion implantation, as a common approach to dope the source/drain regions and reduce contact resistance in traditional semiconductor devices. Thus, it is important to study the contact properties, especially in transistors based on single layer MoS_2. Here, a simple and effective method is developed to extract the intrinsic contact resistance, or the contact resistance without electrostatic doping, in CVD MoS_2 transistors. The total resistance of the transistor, R_{tot}, is the sum of the contact resistance and channel resistance, that is, $R_{tot} = 2R_c + R_{ch}$. Here $2R_c$ represents the contact resistance of both source and drain leads. For each double-gated device, the on-currents from back-gate modulation and top-gate modulation are very different, even though they cover the same area of channel region. This is mostly due to the difference in contact resistance. The global back gate is able to modulate the carrier density of MoS_2 under source/drain metal contacts, thus reducing the contact resistance by electrostatic doping. However, this effect from top gate is screened by

source/drain contact metals thus the carrier density in MoS_2 at source/drain regions and the contact resistance remain constant during top-gate sweeping.

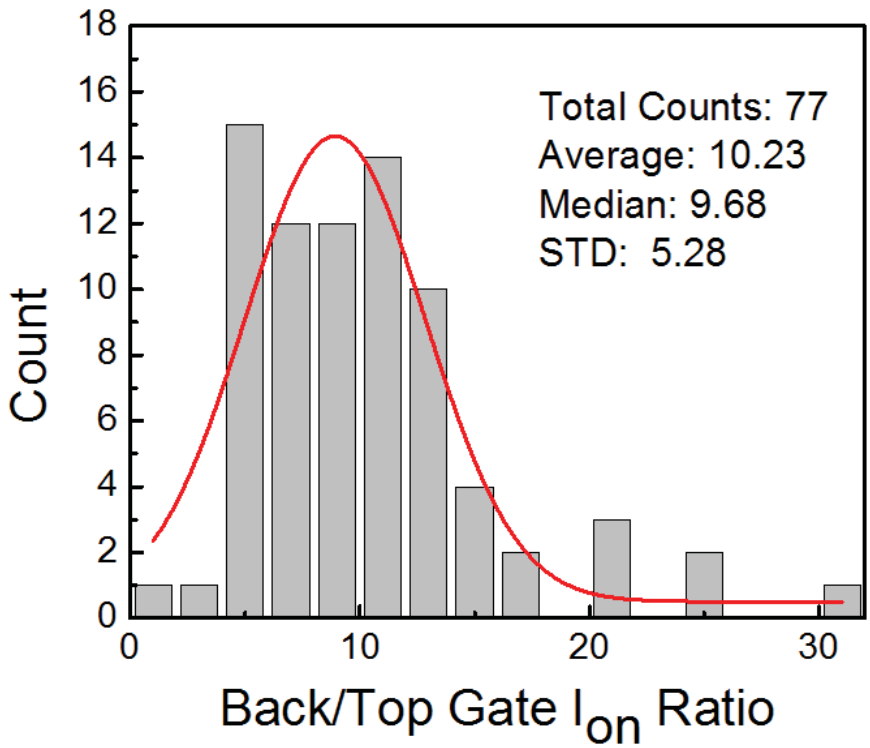

Fig. 5.7. Distribution of on-current ratio from back/top gate devices

In order to extract intrinsic contact resistance, i.e. contact resistance without gate bias, the total resistance is compared at on-state of 500 nm and 1 μm channel length transistors. The observed current ratio between back-gate and top-gate modulation is around 10, as shown in Figure 5.7. This means that for top-gate modulation, the contact resistance is over 10 times larger than the channel resistance, that is, $2R_c \gg R_{ch}$. By assuming the channel resistance is similar from top- and back-gate modulation, this can be written as:

$$2 \times R_{c,tg} + R_{ch} = 10 \times (2R_{c,bg} + R_{ch}) \tag{5.2}$$

$$2 \times R_{c,tg} = 20 \times R_{c,bg} + 9 \times R_{ch} \tag{5.3}$$

consider even under gate bias, $R_{c,bg}$ is still considerably large, therefore,

$$2 \times R_{c,tg} \gg R_{ch} \tag{5.4}$$

This means, for top-gated devices, the early saturation of drain current in transfer curves (inset of Figure 5.8) is attributed to the large contact resistance. In other words, even channel resistance can be further decrease by gate biasing, the large contact resistance is dominant and the drain current cannot be further improved.

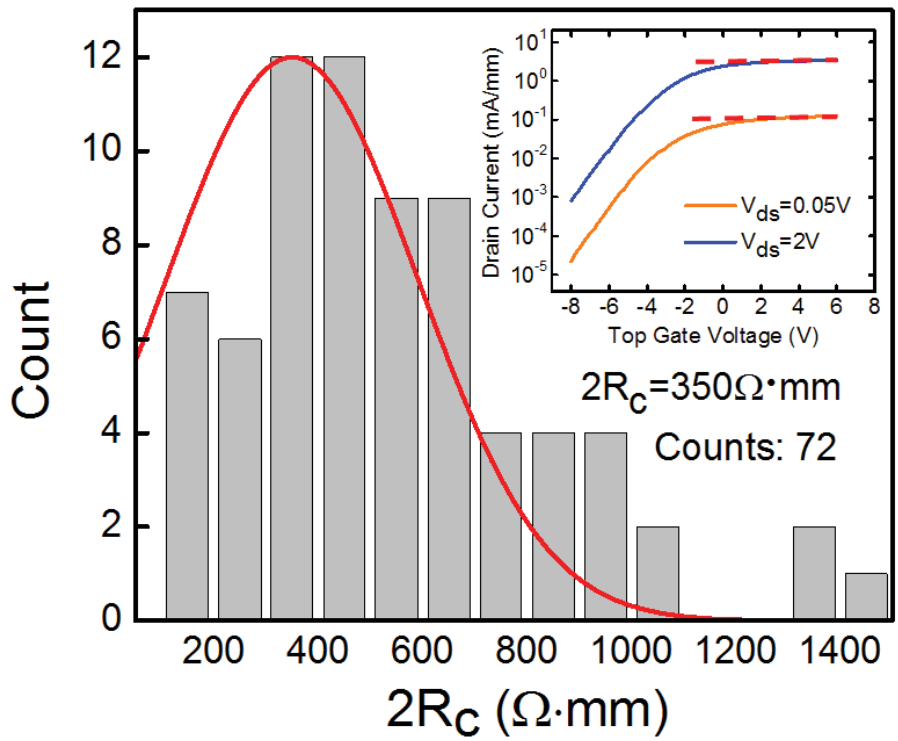

Fig. 5.8. Intrinsic contact resistance distribution in all top-gated MoS_2 devices

In top-gated devices, R_c is fixed at a large and constant value. Once the R_{ch} is much smaller than $2R_c$ during top-gate sweep, R_{tot} does not change much any more even if the top-gate bias is increased. Beyond this point, one can assume $R_{tot} \approx 2R_c$. The total resistance in all top-gated devices is extracted and plot the distributions in Figure 5.8. The expectation value of $2R_c$ is approximately around 350 Ω·mm at zero back-gate bias or without electrostatic doping from back-gate. This huge number is

almost two to three orders larger than the desired value in conventional semiconductor devices. Besides the Schottky barrier issue stated before, the single layer nature also has a remarkable contribution to the large contact resistance. Previous study about metal contacts on graphene has revealed that the contact resistivity (ρ_c) is determined by contact width instead of the contact area, that is, $\rho_c = R_c W$. [80] This means that in the case of graphene, the current flows mainly along the edge of the graphene/metal contact. In other words, the current crowding takes place at the edge of the contact metal. This may also apply to single layer MoS_2 since it is more resistive with lower mobility than graphene. The contact resistance R_c could be reduced to 10 Ω·mm at 100 V back-gate bias, which would be discussed in later parts. The consequence of the large contact resistance can be reflected in two ways. First, the on-current is significantly limited, and this effect is significantly magnified for short channel devices, where the portion of channel resistance over total resistance shrinks with scaling down. On the other hand, large transfer length is expected, which barricades high-density device integration. Although the contact resistance can be greatly decreased by applying a large bias on the global back gate, it is not a practical method for real device applications. Previous studies have proposed different approaches to realize doping on 2D semiconductors, such as gaseous and potassium doping. [25, 26] However, these methods could be hard to be implemented in real integrated circuits. Better solutions are still under investigation, such as formation of MoS_2 based alloy, or contact engineering for Fermi-level depinning at metal to 2D semiconductor interface. This is possible from fundamental physics due to a reduced material dimension and a perfect 2D surface without the termination of a periodic crystal structure. [81] It also requires for defect-free material to eliminate disorder induced gap-states, which has been recognized as a major factor to cause Fermi-level pinning. [82] It is obvious that transport mobility and contact study provides the right information on defect level in CVD MoS_2 films. A comprehensive study on the metal/single layer MoS_2 contact will be discussed in later sections in this chapter.

5.4 Field Effect Mobility in Single Layer CVD MoS_2 Transistors

The carrier mobility in single layer CVD MoS_2 field-effect transistors will be investigated in this section. In classical theories, the carrier mobility in the bulk and at the interface is different, thus the field-effect mobility is dependent on the gate voltage, which can be written as:

$$\mu_{FE} = \frac{\mu_{FE}^0}{1 + \theta(V_{gs} - V_{th})} \tag{5.5}$$

where μ_{FE}^0 and θ are two constants. Since increasing the gate bias would push the carriers to the boundary of semiconductor and gate oxide, the carrier mobility would be lowered due to surface scattering. However, in our case the channel material is only atomic layer thick and this effect would have a much smaller impact, hence the mobility is nearly a constant value during gate sweep or $\theta = 0$. As a common approach, the field-effect mobility is extracted from the maximum transconductance on the transfer characteristics, which follows:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \mu_{FE} C_{ox} \frac{W}{L} V_{ds} \tag{5.6}$$

Field-effect mobility at various lengths is calculated and the distributions are plotted in Figure 5.9. The average values of extrinsic field-effect mobility are extracted to be 2.67 ± 0.91, 4.58 ± 1.71, 8.52 ± 2.97, and 10.52 ± 3.41 $cm^2/V{\cdot}s$ for 100 nm, 200 nm, 500 nm, and 1 μm channel lengths, respectively. The decrease in mobility at shorter channel lengths is mostly because of the assumption that the drift velocity ν_d increases linearly with drain bias by applying $\nu_d = -\mu E$. However, because of velocity saturation the product of carrier mobility and lateral electric field is fixed at a constant number. The electric field in the channel increases with channel length down scaling, thus the calculated mobility decreases. This is consistent with the observation of drain current saturation even when channel length is pushed down to smaller values.

Finally, the intrinsic carrier mobility in CVD single layer MoS_2 transistors is estimated by subtracting the contribution from the significant contact resistance. Because of the large contact resistance, the intrinsic mobility could be very different

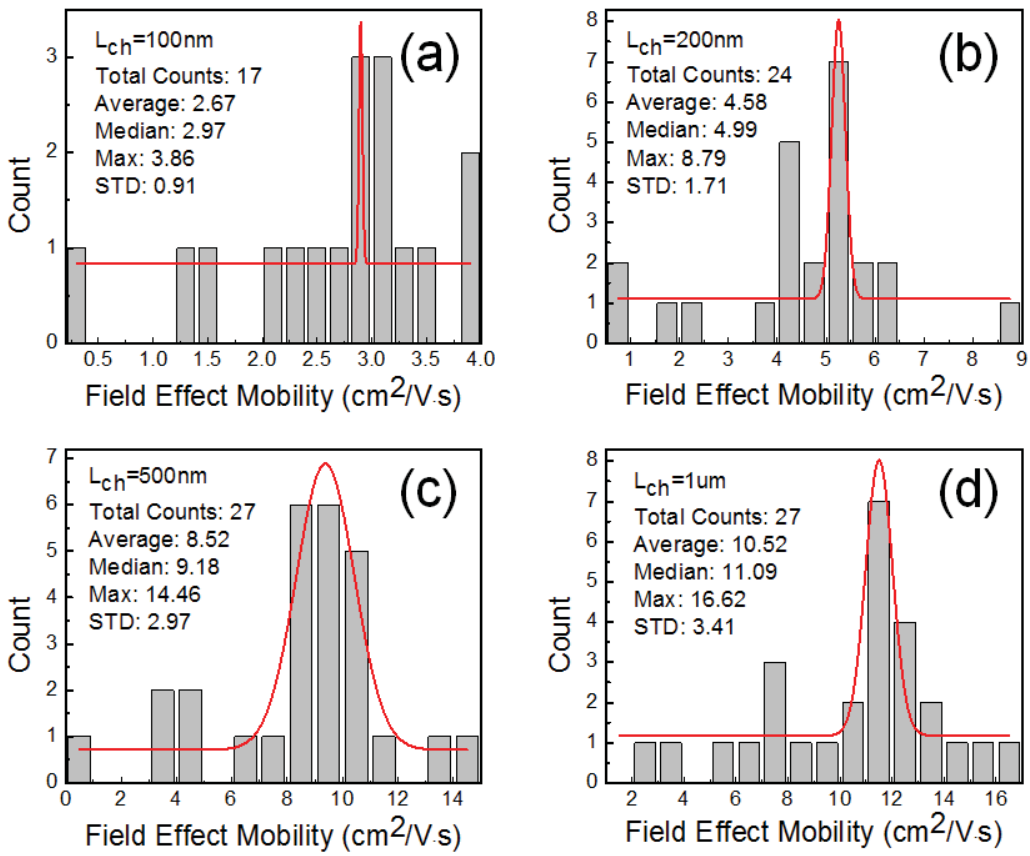

Fig. 5.9. Extrinsic field-effect mobility distributions in devices with various channel length

from the extrinsic values. Therefore, it is necessary to give a reasonable estimation of the contact resistance under gate bias and correctly estimate the intrinsic field-effect mobility. The back-gated maximum transconductance achieved in our measurement range is at 100 V gate bias. By assuming there is no velocity saturation in devices channel length of 500 nm or above so as to ignore the difference in mobility between 500 nm and 1 μm channel length devices. For back-gated devices, the contact resistance is a function of gate bias, and the channel resistance is a function of both gate bias and channel length, that is, $R_{tot} = 2R_c(V_{gs}) + R_{ch}(V_{gs}, L)$. Because

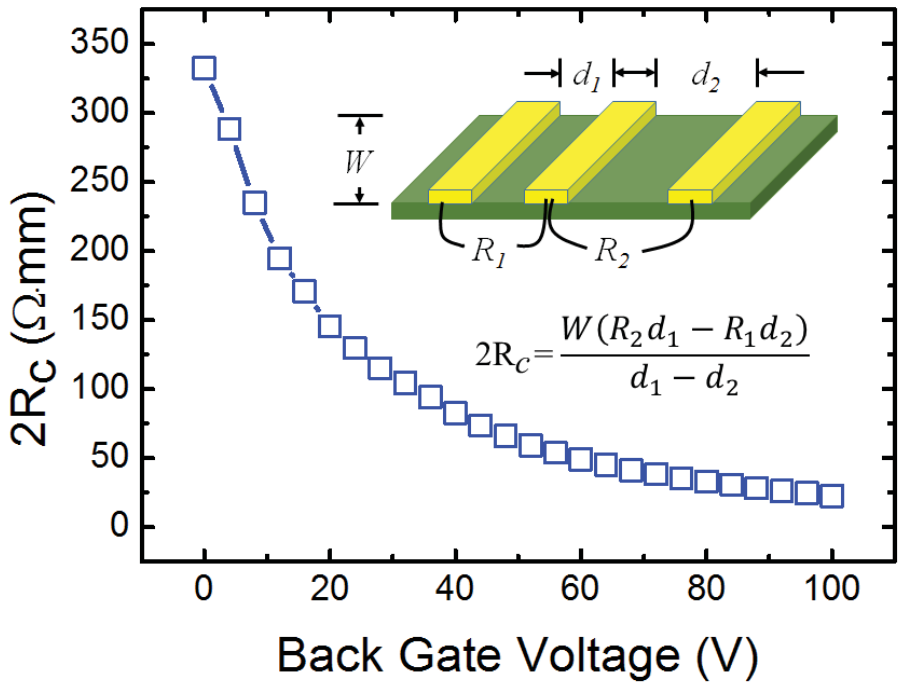

Fig. 5.10. Contact resistance on CVD single layer MoS_2 at various gate bias

$R_{ch}(V_{gs}, L)|_{L=1\ \mu m} \approx 2R_{ch}(V_{gs}, L)|_{L=500\ nm}$ at fixed V_{gs}, therefore R_c can be extracted at a certain V_{gs}.

The contact resistance can be obtained by connecting the two total resistance in the coordinate and extend the line reversely to when channel length equals zero. By using the following equation, the contact resistance can be estimated.

$$2R_c = \frac{W(R_2 d_1 - R_1 d_2)}{(d_1 - d_2)} \tag{5.7}$$

In this case, if x- and y-axis are the channel length and total resistance, $2R_c$ would be the intercept on y-axis. Contact resistance in dependence of the back-gate bias is plotted in Figure 5.10. At 100 V gate bias, this value is saturated at around 20 Ω·mm, as shown in Figure 5.11. However, due to large device-to-device variance, and this quasi-TLM method is limited by only two data points, it suffers from large standard deviation which is not plotted in the figure.

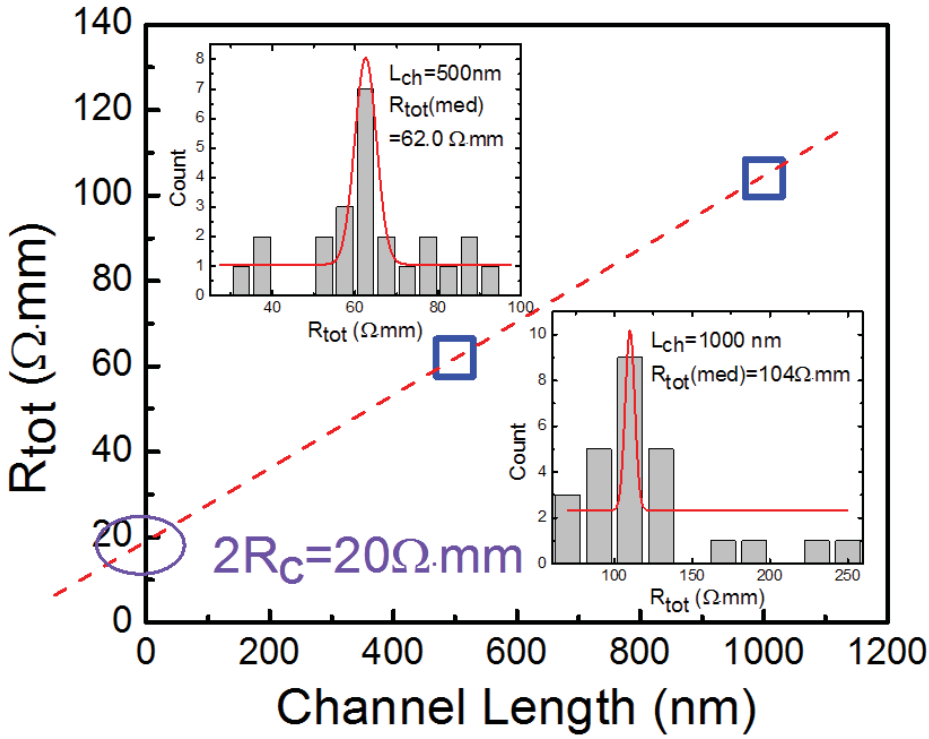

Fig. 5.11. Saturation of contact resistance on CVD single layer MoS_2 at $V_{gs} = 100\ V$

By applying this method, the intrinsic carrier mobility is estimated by dividing the ratio between total resistances over channel resistance, that is:

$$\mu' = \mu(\frac{R_{ch}}{R_{tot}})^{-1} = \mu(1 - \frac{2R_c}{R_{tot}})^{-1} \tag{5.8}$$

Averaged values of 6.11±2.07, 7.72±2.89, 12.59±4.38 and 13.02±4.22 $cm^2/V{\cdot}s$ are achieved for 100 nm, 200 nm, 500 nm, and 1 μm channel length and a maximum value of 21.6 $cm^2/V{\cdot}s$ at long channel regions of the CVD single layer MoS_2 transistors, as plotted in Figure 5.12. These mobility values provide the low limit for the CVD MoS_2 films. The significant interface trap density, which degrades the measured g_m, has not been considered in this estimation.

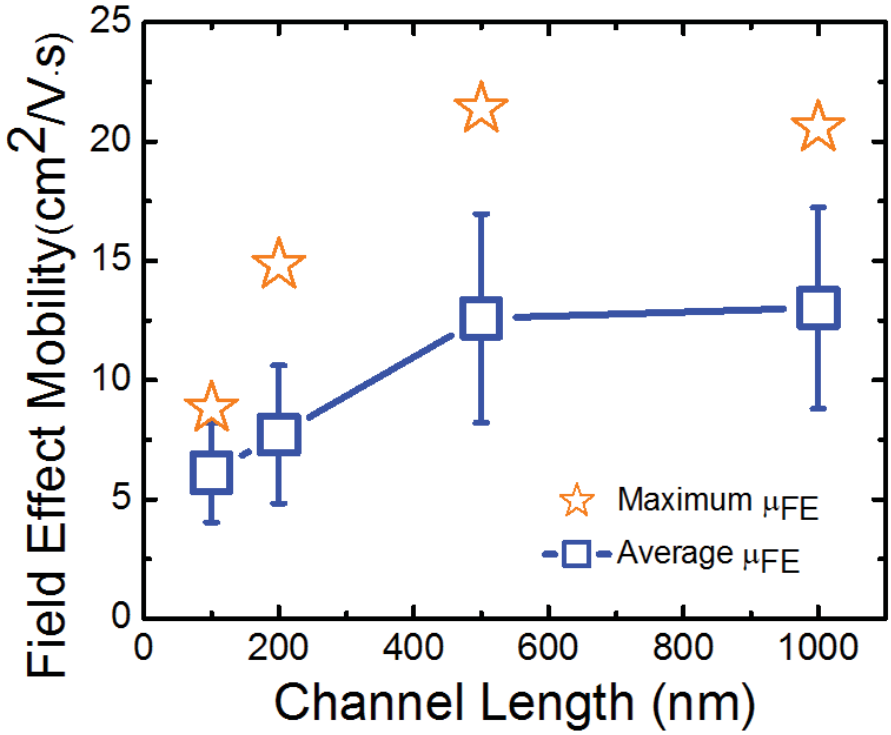

Fig. 5.12. Intrinsic field effect mobility in MoS_2 transistors at various gate length

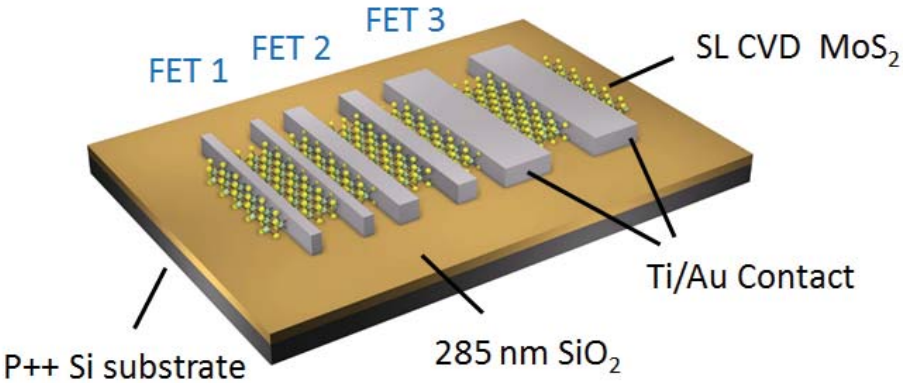

Fig. 5.13. MoS_2 transistors with various contact length

5.5 Transfer length in CVD MoS_2 Transistors

In this section, metal contacts on single layer MoS_2 is further investigated. Prior to device fabrication, triangular MoS_2 flakes, as shown in Figure 5.2, were patterned

by e-beam lithography and dry-etched by BCl_3/Ar plasma into rectangularly shaped channels all having a channel width of 2 μm. Contact bars with lengths of 0.2, 0.5, 1, and 2 μm were defined with e-beam lithography. Each pair of contact bars has a fixed spacing of 1.1 μm; thus, long channel approximation can be used in the following discussions of device performance. Ti/Au was used as the contact metal here as Ti is a low work function metal and has been used to create high performance MoS_2 transistors based on single layer crystals. No annealing was performed after the metallization process. Due to the 2D nature of single layer MoS_2 crystals, the metal/MoS_2 interface is unperturbed by chemical reactions. The final device structure is illustrated in Figure 5.13. Global back gate is used to modulate these devices instead of the top gate because the global back gate can better modulate both carrier density in the channel and the Schottky barrier across the contact. This provides a more direct view of how contact resistance and channel resistance change individually under the same gate voltage, in order to better reveal how the MoS_2 transistor operates at different bias conditions.

Each pair of contact bars with same contact length was taken as the source/drain pair for an individual back-gated transistor. The transfer curves of devices measured at 2 V drain bias with various contact length are compared in Figure 5.14(a). All devices show clear switching behavior with a current on/off ratio over 10^6. Similar V_T and SS are observed as well. Meanwhile, all devices show similar off-current level around 10^{-6} to 10^{-7} mA/mm, regardless of the contact length. However, there is an obvious change in the dependence of on-current with contact length. Contact length dependent on-current is shown in Figure 5.14(b). At 100 V back gate bias, the 0.2 μm contact length device has the on-current of 2 mA/mm. If the contact length is expanded to 0.5 μm, the on-current increases up to 5.1 mA/mm, almost proportional to the contact length. However, with further expansion of contact length, the current does not increase proportionally and gets saturated at 7.3 mA/mm. This phenomenon is rarely seen in conventional Si MOSFETs at micrometer dimensions, where a low resistive contact impacts the on-current in only a minor way. This phenomenon can

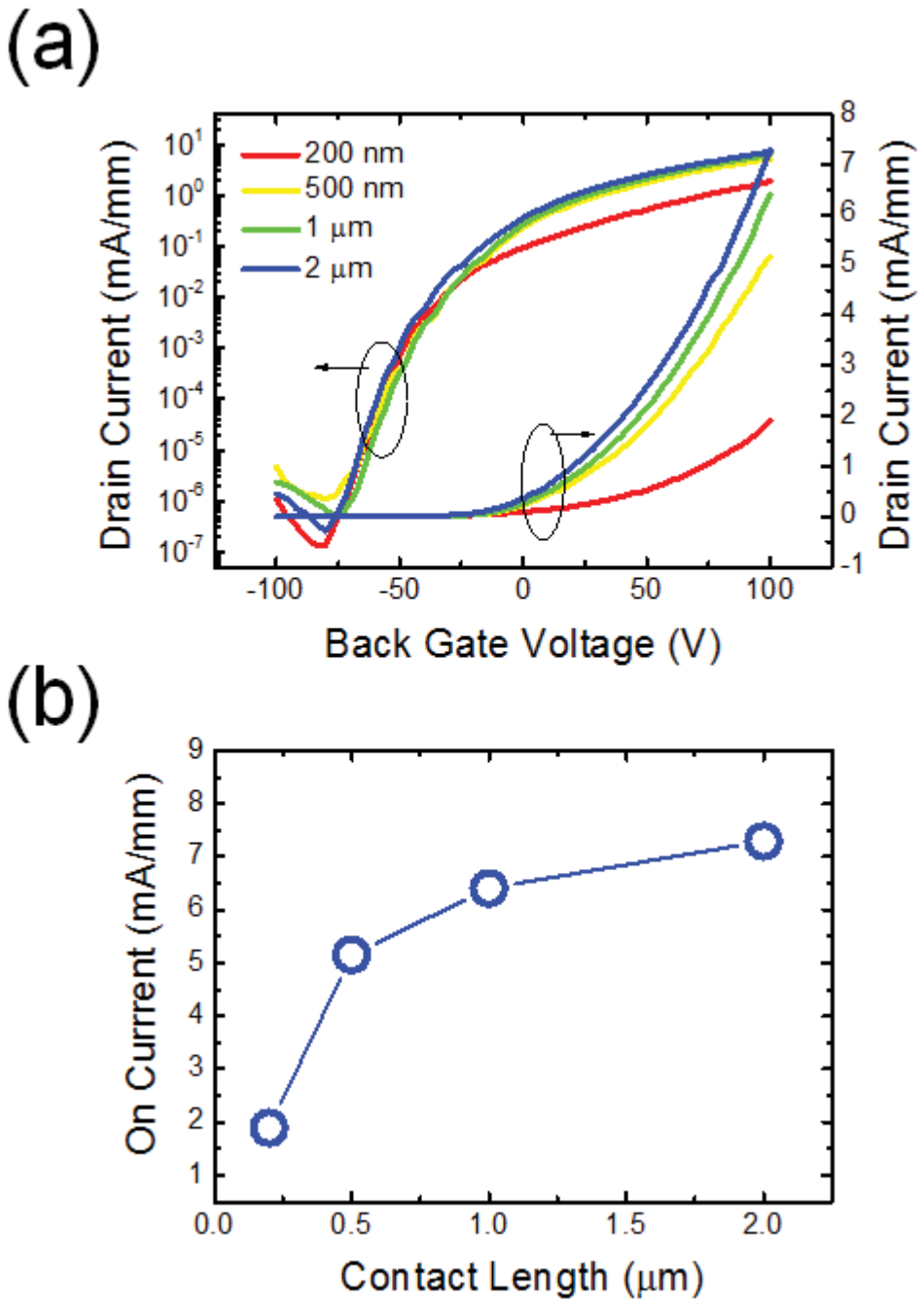

Fig. 5.14. Transfer characteristics and maximum drain current in MoS_2 transistors with various contact length

be roughly explained as a large contact resistance in MoS_2 transistors which accounts for a larger portion of the total device resistance. The large contact resistance was

also observed in our previous study, where the drain current saturated at shorter channel lengths with channel length scaling. However, a further examination of the contact resistance allows us to understand switching mechanism for MoS_2 transistors, as discussed in the later parts of this section.

The total resistances is extracted for different contact lengths at various back gate biases, as plotted in Figure 5.15, where a low drain bias of 50 mV was applied for all measurements. The back gate was biased from 0 to 100 V. Clearly, by changing the gate voltage, the total resistance changes by two-orders of magnitude, independent of the contact length. Meanwhile, the impact of contact length on total resistance can be seen at each gate voltage. This impact is quite different at various gate voltages. For example, at zero gate bias, the total resistance for 0.2 μm contact is 25 MΩ and this resistance is reduced to 15, 14, and 10 MΩ when the contact length is increased to 0.5, 1, and 2 μm. This drop can be clearly seen in both log scale and linear scales shown in Figure 5.15. However, with further increase of the gate bias, the reduction of total resistance is not as strong as it was for low gate biases. For 100 V gate bias, the total resistances are 0.29, 0.12, 0.11, and 0.11 MΩ for 0.2, 0.5, 1, and 2 μm contact length, respectively. The total resistance seems to approach a minimum value at 0.5 μm, and the difference cannot be identified even with the log scale of Figure 5.15(a). Considering the two gate voltages discussed above, one sees that the dependence of the total device resistance on contact length changes as a function of gate voltage or, equivalently, the carrier density in the semiconductor at the metal/semiconductor junction. When the carrier density is low in the semiconductor, the total resistance depends more strongly on the contact length, but when carrier density is increased, the dependence weakens. This contact-length dependent transport behavior grants insight into the nature of current flow across the metal/atomically thin semiconductor junction and the operational mechanism of single layer MoS_2 transistors at different bias conditions, both of which will be discussed in more detail.

First of all, how current flows across the metal/single layer MoS_2 junction will be discussed. Starting with the conventional metal/bulk silicon junction, as shown

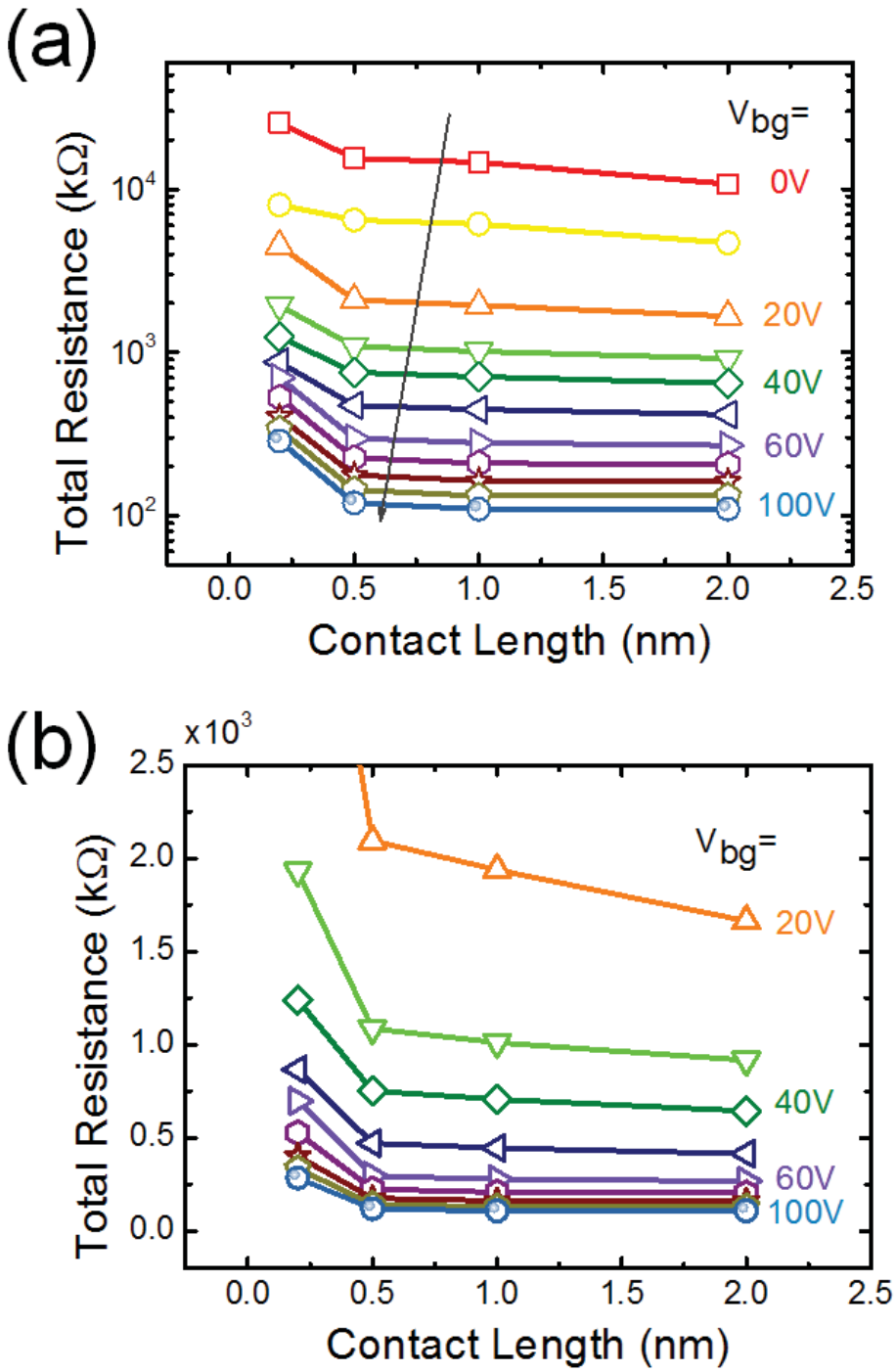

Fig. 5.15. Gate dependent total resistance in MoS_2 transistors with various contact length

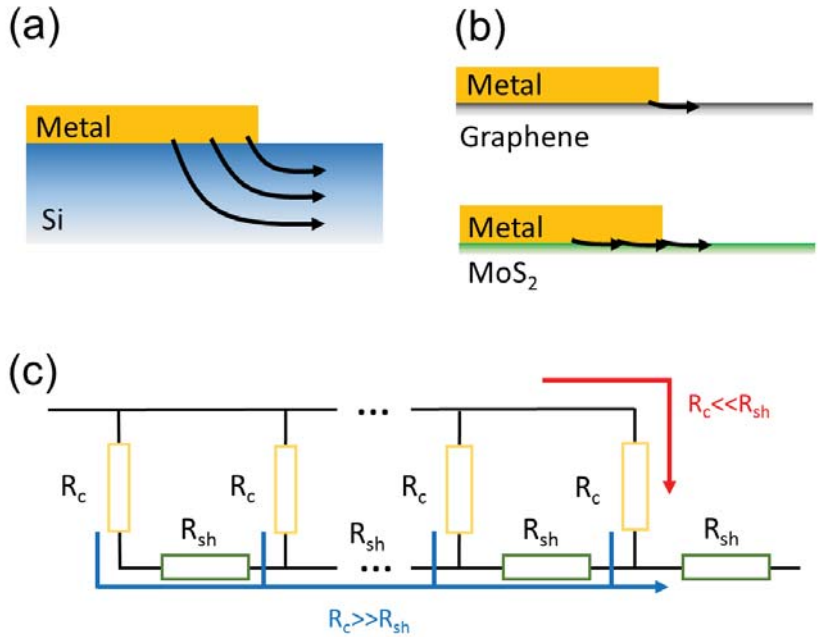

Fig. 5.16. Current flow path in metal/semiconductor junction

in Figure 5.16(a), the carriers injected into silicon from the metal contacts flow not only at the semiconductor surface but also deep into the bulk. [56] The depth of the current flow in this case is primarily determined by the junction depth of the implanted region of the semiconductor. Now considering two-dimensional materials, since the penetration depth of current flow is limited by the body thickness when the bulk crystal is reduced to atomic thickness, an intuitive description of current flow across the junction would be that the current only flows across the junction at the contact edge, as shown in the top of Figure 5.16(b). This assumption was proved to be true in graphene. [80] It has been shown that the contact resistivity (ρ_c) of the metal/graphene junction is defined by $\rho_c = R_c \times W$ instead of $\rho_c = R_c \times A$, where R_c is the contact resistance, W is the contact width, and A is the contact area. Though there are still some controversies on the graphene contact properties, experimental studies show similar results and large currents have been obtained with

narrow metal contacts in graphene transistors. However, our results show that current flow strictly at the edge of the metal contact, as in graphene, may not hold true for other semiconducting 2D crystals. In the case of MoS_2, the carriers usually need a larger contact length to realize adequate carrier injection, depending on the gate bias, as shown schematically in the bottom of Figure 5.16(b). A resistor network is usually applied to model the metal/semiconductor junction, as shown in Figure 5.16(c). When current flows across the junction, it encounters two resistances. One is the impedance from the Schottky barrier, where it is simplified as a resistor R_c, and a sheet resistor R_{sh}. [56] The current would choose the least resistive path from the metal to the semiconductor. The potential distribution under the contact is determined by both resistors and can be written as follows:

$$V(x) = \frac{I\sqrt{R_{sh}\rho_c}}{W}\frac{cosh[(L-x)/L_T}{sinh(L/L_T)} \tag{5.9}$$

where x is the lateral distance from the contact edge, L and W are the contact length and width, and I is the current flowing into the contact. The voltage is highest near the contact edge and drops nearly exponentially with distance. Usually, the "1/e" distance of the voltage drop is defined as the transfer length L_T and can be expressed as $L_T = (\rho_c/R_{sh})^{1/2}$. In conventional Si MOSFETs, both ρ_c and R_{sh} are almost fixed numbers for implanted regions, while in MoS_2 transistors, they are modulated by gate voltage, therefore, the carrier transport across the metal/MoS_2 junction is determined by both the gate-dependent contact resistance ($R_c = \rho_c \times A$), and gate-dependent sheet resistance. In the resistor network in Figure 5.16(c), if R_c is much larger than R_{sh}, the least resistive path would be all routes in the network, marked as blue lines in Figure 5.16(c). This situation would correspond to infinite transfer length. In contrast, if R_{sh} is much larger than R_c, then all current flows through the into the channel region at the junction edge, as noted in the red direction. In this case, the contact length would be very small. Metal contacts on graphene are best described by the second case, while MoS_2 lies in between. Both R_{sh} and R_c are modulated by the back gate bias and lead to the behavior of L_T in MoS_2 which is discussed below.

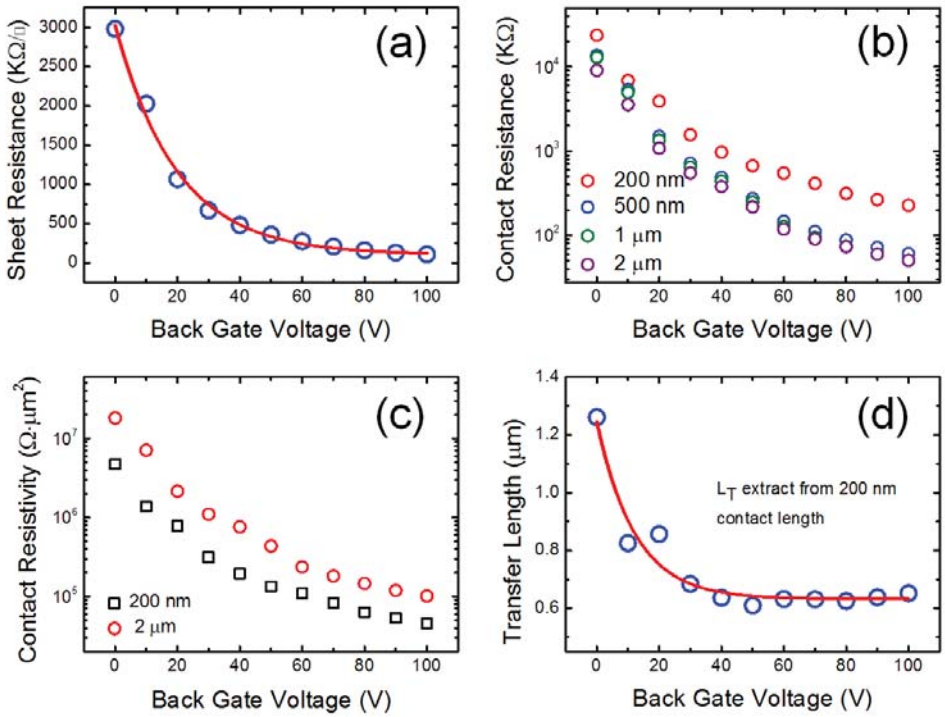

Fig. 5.17. Gate dependent sheet resistance, contact resistance, contact resistivity and transfer length

Before discussing the mechanisms of single layer MoS_2 transistor operation at different bias conditions, it is necessary to know how L_T changes with gate voltage. As shown in Figure 5.15, the L_T is not a constant number in MoS_2 transistors, as both R_{sh} and ρ_c at the contact regions are dependent on the back gate bias. Actually, the drain bias has an impact on them as well, but how gate voltage changes the L_T is examined. To determine L_T, both R_{sh} and ρ_c are calculated. To begin, R_{sh} is determined and plotted in Figure 5.17(a), using TLM structure fabricated on the same sample. At 0 V back gate bias, the sheet resistance is 3MΩ/□. With increasing gate bias, the sheet resistance reduces to 106 KΩ/□. This can be easily understood as the Fermi level in MoS_2 is raised up by back gate biasing, inducing higher carrier density and hence reducing the sheet resistance. With the sheet resistance determined, R_c can be calculated and discussed as an intermediate step in determining ρ_c and L_T. R_c is calculated by subtracting the sheet resistance times the geometry factor from

the total device resistance. The R_c for the different contact lengths are plotted in Figure 5.17(b). The decreasing trend in R_c can be attributed to the increasing carrier density in MoS_2 under the metal contacts. The higher carrier density induced by the electric field leads to a narrower Schottky barrier, facilitating thermal-assisted carrier tunnelling to the semiconductor. In this case, the semiconductor can be viewed as being "electrostatically doped" by gate biasing. As expected, shorter contact length yields a higher R_c. As Figure 5.17(b) shows, the extracted R_c depend more strongly on contact length for low gate voltage bias. As the gate voltage is increased, with the exception of the 0.2 μm contact length, the contact resistance of the other contact lengths become more and more similar. This behavior indicates that, at lower gate biasing, the contact metal needs a larger contact length to realize a full carrier injection. However, at high gate biasing, a smaller contact area is adequate.

The contact resistivity is calculated by $\rho_c = R_c \times A$ as mentioned above. At this point, it is important to choose the right contact dimension to estimate the contact resistivity. The 2 μm contact length shows 2 times larger contact resistivity than 0.2 μm contact length, as shown in Figure 5.17(c). This difference is primarily from larger potential drop along the contact length for the 2 μm contact as compared to 0.2 μm contact. This change in potential causes the contact resistivity calculated from larger contact length to be overestimated. The more precise transfer length $L_T = (\rho_c/R_{sh})^{1/2}$ is determined by using ρ_c calculated from smaller contact dimensions as shown in Figure 5.17(d). At 0 V gate bias, the transfer length for Ti/Au contacts on single layer MoS_2 is 1.26 m, which drops to around 0.63 μm at the high gate biases. This suggests that, for single layer MoS_2 transistors, the contact length should be at least 1 μm (1.5 L_T) to guarantee the least contact resistance when device is in the on-state.

5.6 Switching mechanism in single layer CVD MoS_2 transistors

Now that how L_T changes with gate voltage is discussed in previous section, the switching mechanism in MoS_2 transistors can be discussed. As mentioned above,

$L_T = (\rho_c/R_{sh})^{1/2}$ is determined by both ρ_c and R_{sh}. With increasing the gate bias, all three parameters, L_T, ρ_c and R_{sh}, are decreasing. This indicates ρ_c drops faster than R_{sh} when increasing gate bias. From Figure 5.17(a) and (c), it can be seen, for the 2 μm contact transistor, a 100 V change in gate voltage results in a factor of 30 times decrease in sheet resistance, while the contact resistance decreases almost a factor of 200 times. In other words, it is the contact rather than the channel that is more sensitive to the change in gate voltage. This means that the on/off switching in MoS_2 transistors are not primarily achieved by accumulating/depleting the carrier density in the channel, but by tuning the Schottky barrier width or the effective Schottky barrier height at source/drain junctions. [83, 84] This is the fundamental difference between MoS_2 transistors and Si MOSFETs. At negative gate bias, the conduction band moves upward, resulting in an enlarged effective Schottky barrier height for electrons, impeding carrier injection from the contact metal to MoS_2, which corresponds to the off-state of the device. On the other hand, at positive gate bias, the conduction band moves down. In spite of the absolute height for this barrier remaining intact, the narrowed barrier width facilitates thermally assisted tunnelling or even direct tunnelling, thus the device is switched to the on-state. Because this switching mechanism is completely different from that of Si MOSFETs, the extraction of device parameters using the classical methods may not be appropriate. A typical example is the estimation of field-effect mobility in MoS_2. In Si MOSFETs, when the transistor is turned on, the surface potential and carrier density has no significant change. In the linear region, by using long channel approximation, the I-V characteristics can be written as:

$$I_{ds} = \mu_{eff}\frac{W}{L}C_{ox}(V_{gs} - V_{th})V_{ds} \tag{5.10}$$

where μ_{eff} is the effective mobility, W and L are the channel width and length, C_{ox} is gate oxide, V_{gs}, V_{th}, and V_{ds} are the gate voltage, threshold voltage, and drain voltage.(20) Once the transistor is turned on, the device can be modelled as a resistor with $R_{on} = 1/[\mu_{eff}(W/L)C_{ox}(V_{gs} - V_{th})]$. However, for MoS_2 transistors, even when the device is in the on-state, the transistor cannot be modelled as a resistor, since

(1) there are still two Schottky barriers at the contact, and the effective height of the Schottky barrier changes with the V_{gs}, and (2) for the MoS_2 channel, the on-state in the transistor is mainly triggered by the reduced Schottky barriers; meanwhile, the surface potential in MoS_2 channel may still be varied by gate bias. Therefore, the precision of field-effect mobility extraction simply from the transconductance peak is questioned in previous studies in light of the Schottky barriers discussed in this chapter. This explains why field-effect mobility calculated from single- or few-layer MoS_2 transistors are lower than those values obtained from Hall mobility measurements. [13, 85]

In the previous paragraph, how gate bias changes the effective barrier height and hence controls the switching in MoS_2 transistors are discussed. Now, how drain bias influences the Schottky barriers at drain and source will be discussed additionally. Here our discussion is limited to long channel devices only. In MoS_2 transistors, since there are two metal contacts that serve as source and drain, there will be two Schottky barriers, the source barrier and the drain barrier. These two barriers are usually asymmetric. If electron flow path is defined as from source to drain, the electrons would encounter the source barrier first, where they would undergo a thermal-assisted tunnelling process from the metal Fermi level to the conduction band. On the other side of the transistor, a tunnelling process may take place again depending on the drain bias of the device, and the electrons would go from the conduction band to the metal drain. In accordance with the long channel approximation, output curves measured from a 2 μm contact length transistor is shown to illustrate the band diagrams at 4 different on-state bias conditions, as depicted in Figure 5.18. To first look at the high gate bias situation (point A and B), where gate is biased at 100 V, both conduction and valence bands are pulled down, facilitating thermal-assisted tunnelling from source metal to conduction band in MoS_2. At point A, when drain voltage is low, both source and drain barriers impede the electron transport. Note that the gate bias has an opposite impact on these two barriers. With higher gate bias, the effective barrier height for source barrier, Φ_S, is reduced due to a sharper triangular

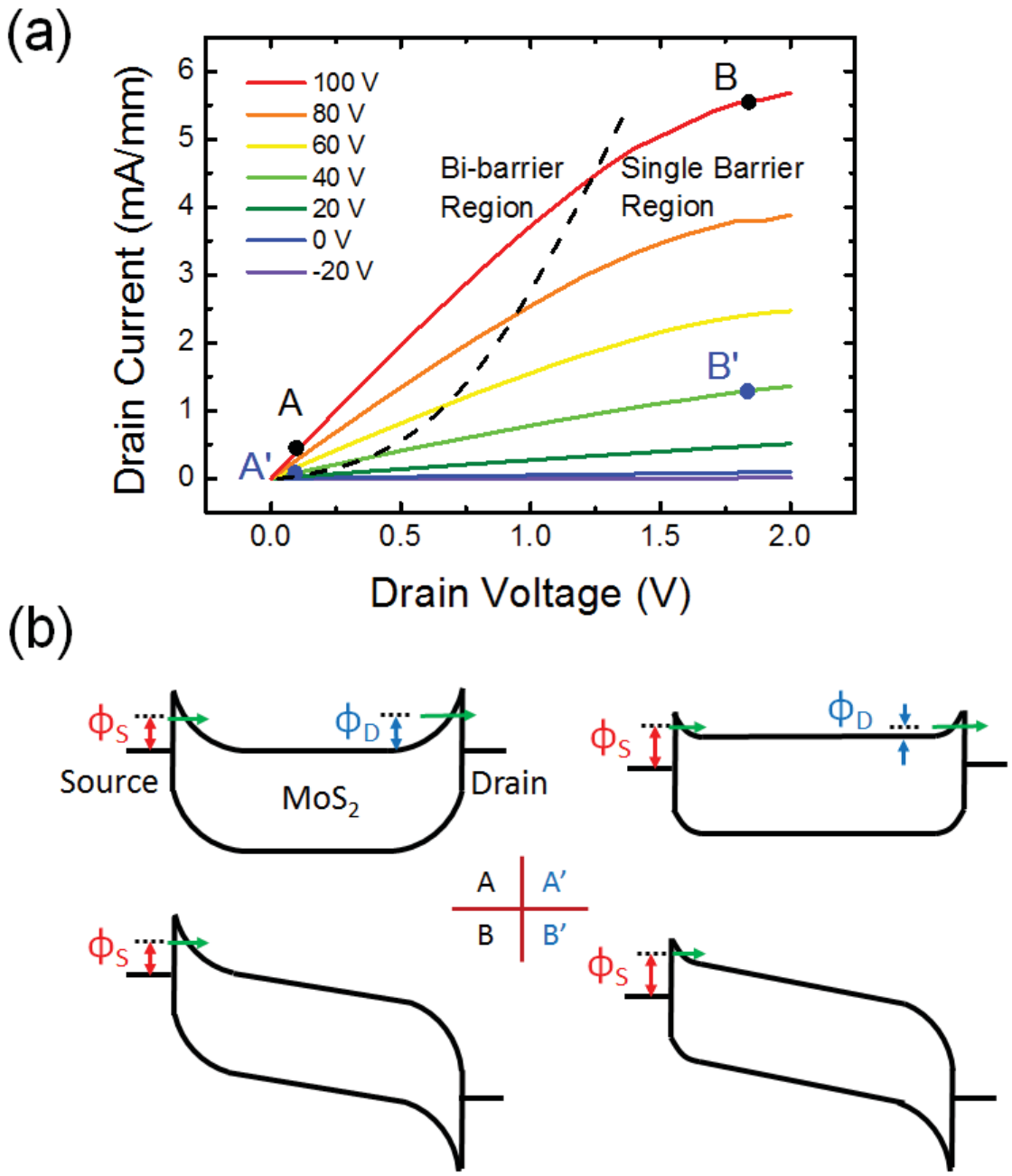

Fig. 5.18. Schematic of switching mechanism in CVD MoS_2 transistors

barrier; meanwhile, the barrier height for electrons injected from the semiconductor to the metal drain, Φ_D, is enhanced due to the lowering of the conduction band, as

compared to the low gate bias condition. However, with further increase of the drain bias, Φ_S remains constant, as it is fixed by the gate bias; however, Φ_D keeps reducing and finally diminishes, leaving only one barrier and the device's diffusive channel, as shown in point B in Figure 5.18(b). As discussed previously, the modulation of the barrier heights is the dominate mechanism which changes the device conductance. At point A, since the increase in drain bias is lowering Φ_D, the current has a sharper increase. After Φ_D is reduced to zero, the drain bias only acts on the device's diffusive channel so that current increase is not as fast at point B as it is at point A. This looks like current saturation in Si MOSFETs, but the difference is that the current saturation in MoS_2 transistors is caused by the changes in the barrier heights rather than pinch-off of the channel. For the lower gate bias situation (point A' and B'), where the gate bias is 40 V, the conduction band is not as low as the previous case, making Φ_D much lower. With increasing drain bias, Φ_D will be quickly reduced to zero. That is to say, in the lower gate bias case, the drain barrier is expected to have less of an impact on the output curves, making the I_d-V_{ds} relationship look more linear. The barrier controlled output characteristics in MoS_2 transistors are completely reversed as compared to Si MOSFETs output curves. In n-type Si MOSFETs, the output curves at lower V_{gs} saturate easier, where $V_{d,sat} = V_{gs} - V_{th}$ is smaller. In the top curves, where V_{gs} is higher, the output curves are usually straighter in the same drain bias range, as a higher V_{ds} is needed for current saturation. However, in MoS_2 transistors, output curves at lower V_{gs} look more linear while they are more curving at high V_{gs}. In summary, the device performance in long channel MoS_2 transistors is simply controlled by two Schottky barriers. The gate voltage controls both barriers to switch the device between on- and off-states, while the drain voltage has a larger impact on the drain barrier. Through its action on the drain barrier, the increase in V_{ds} shifts the device from the "bi-barrier region" to the "single-barrier region" in the on-state, similar to the linear and saturation regions of Si MOSFETs.

Finally, the device performance of MoS_2 transistors at short channel regions will be briefly discussed, to understand how these barriers influence the device performance.

The existence of barriers is not desirable, as it introduces a large contact resistance which limits the on-current in the transistor. However, when channel length is aggressively reduced and it is comparable to the barrier width, the drain bias would influence Φ_S as well. In the on-state, an increased drain bias would reduce the source barrier width, hence reducing the source contact resistance. It is similar to DIBL in short channel Si MOSFETs, where the drain bias lowers the barrier in the channel at off-state, making the device difficult to turn off. Hence, in the Si MOSFET case, DIBL is undesirable as it degrades the off-state of the transistors. However, in MoS_2 transistors, the drain-induced barrier narrowing (DIBN) would be a "favorable" short channel effect as it reduces the Schottky barrier width and enhances the on-state current. This means that one of the bottlenecks for MoS_2 transistors, the large contact resistance, may act only in long channel regions and diminish at the short channel length. Therefore, short channel MoS_2 transistors would be potentially a competitive technology once the channel length is aggressively scaled down to the level of barrier width. The source barrier can be increased in the off-state to impede current flow; however the barrier width can be narrowed at larger drain bias to increase on-state current, due to the DIBN effect. In other words, the contact resistance at shorter channel length would be significantly reduced, making contact dimensions scalable as well.

5.7 Summary

In this section, first, single layer MoS_2 crystals were synthesized by CVD method. Transistors were fabricated on these crystals with channel length down to 100 nm and their device characteristics were statistically analysed. A maximum drain current of 62.5 mA/mm was achieved at 2 V drain bias for 100 nm channel length device. Also, a large contact resistance for metal contacts on single layer CVD MoS_2 films up to R_c=175 Ω·mm was revealed at zero gate bias, which could be reduced to 10 Ω·mm under 3.5 MV/cm vertical field. The field effect mobility was extracted

and the maximum value of intrinsic field-effect mobility in single layer CVD MoS_2 is calculated to be 21.6 $cm^2/V{\cdot}s$. In addition, MoS_2 transistor behavior with various contact lengths was studied. The device performance is strongly related to the contact dimensions. Sheet resistance, contact resistivity and transfer lengths at various gate voltages are extracted. Switching behavior of MoS_2 transistors is revealed to be modulated by two Schottky barriers. The MoS_2 transistor would potentially be a very promising device at short channel regions after optimizing the device design.

6. PHOSPHORENE: A NOVEL P-TYPE 2D SEMICONDUCTOR

Preceding the current interest in layered materials for electronic applications, research in the 1960s found that black phosphorus combines high carrier mobility with a fundamental band gap. Its counterpart, dubbed phosphorene, as a new 2D p-type material will be introduced in this chapter. Same as graphene and MoS_2, single layer phosphorene is flexible and can be mechanically exfoliated. It is stable and, unlike graphene, to have an inherent, direct and appreciable band-gap that depends on the number of layers. Optical and transport properties will be discussed. Phosphorene transistors will be characterized and a CMOS inverter with 2D channel materials will be demonstrated.

6.1 Crystal and Band Structures of Black Phosphorus and Phosporene

Black phosphorus, the bulk counterpart of phosphorene, is the most stable phosphorus allotrope at room temperature that was first synthesized from red phosphorus under high pressure and high temperature in 1914. [86, 87] Similar to graphite, its layered structure is held together by weak inter-layer forces with significant van der Waals character. [88–90] Previous studies have shown this material to display a sequence of structural phase transformations, superconductivity at high pressures with T_c above 10 K, and temperature dependent resistivity and magnetoresistivity. [91–96] 2D phosphorene is, besides graphene, the only stable elemental 2D material that can be mechanically exfoliated.

The equilibrium structure and bonding of black phosphorus, few-layer and single layer phosphorene is determined by using *ab-initio* density functional theory calculations based on the PBE and HSE06 functionals as implemented in the SIESTA

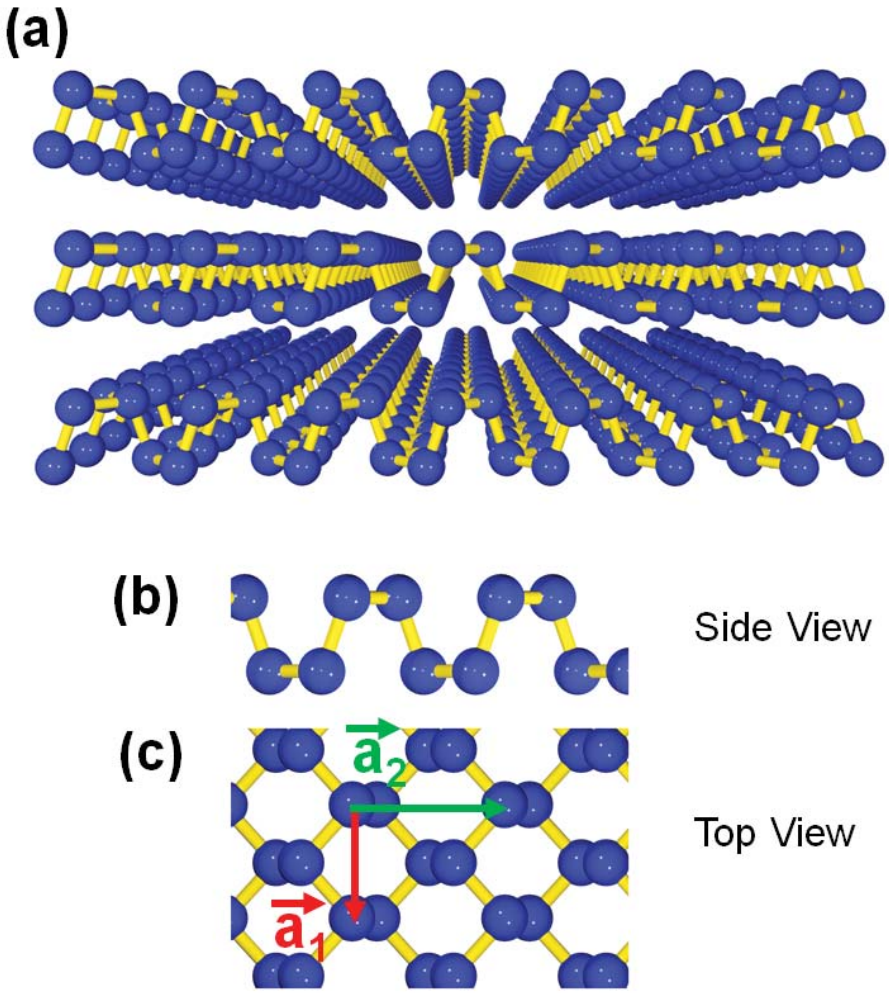

Fig. 6.1. Equilibrium structure of black phosphorus

and VASP codes. [97–99] As seen in the optimized structure depicted in Figure 6.1, phosphorene layers share a honeycomb lattice structure with graphene with the notable difference of non-planarity in the shape of structural ridges. The bulk lattice parameters a_1=3.36 Å, a_2=4.53 Å, and a_3=11.1 Å, which have been optimized by DFT-PBE calculations, are in good agreement with the experiment. The relatively large value of a_3 is caused by the nonplanar layer structure and the presence of two AB stacked layers in the bulk unit cell. The orthogonal lattice parameters a_1=3.35 Åand a_2=4.62 Åof the monolayer lattice, depicted in Figure 6.1(b) and (c), are close to

those of the bulk structure, as expected in view of the weak 20 meV/atom interlayer interaction that is comparable to graphite. It is found that the ridged layer structure helps to keep orientational order between adjacent phosphorene monolayers and thus maintains the in-plane anisotropy; this is significantly different from graphene with its propensity to form turbostratic graphite.

The band structure results based on the HSE06 functional in Figure 6.2(a) indicate that a free-standing phosphorene monolayer is a semiconductor with a direct band gap of 1.0 eV at Γ. This is significantly larger than the calculated band gap value $E_g = 0.31$ eV for the bulk system, which reproduces the observed value 0.31–0.36 eV. [88, 90, 91] Of particular interest is the finding that the band gap depends sensitively on the number of layers N in a few-layer slab, as shown in Figure 6.2(b). Given the calculation results, E_g scales as the inverse number of layers and changes significantly between 1.0 eV in a single layer and 0.3 eV in the bulk, indicating the possibility to tune the electronic properties of this system. Equally interesting is the sensitive dependence of the gap on in-layer stress along different directions, shown in Figure 6.3. Of particular importance is the finding that a moderate in-plane compression of 5% or more, possibly caused by epitaxial mismatch with a substrate, will change phosphorene from a direct-gap to an indirect-gap semiconductor with a significantly smaller gap.

6.2 Evolution of Optical Characteristics of Single to Few-layer Phosphorene

Atomically thin single layer or few-layer phosphorene was achieved *via* mechanical exfoliation of commercially available (Smart-elements) bulk black phosphorus. A 300 nm SiO_2-coated silicon wafer was used as the substrate. Figure 6.4 shows the AFM image of an exfoliated single layer phosphorene crystal. A step height of 0.85 nm measured at the crystal edge confirms the presence of single layer phosphorene. Even though the step height is slightly larger than the theoretical value of 0.6 nm for single

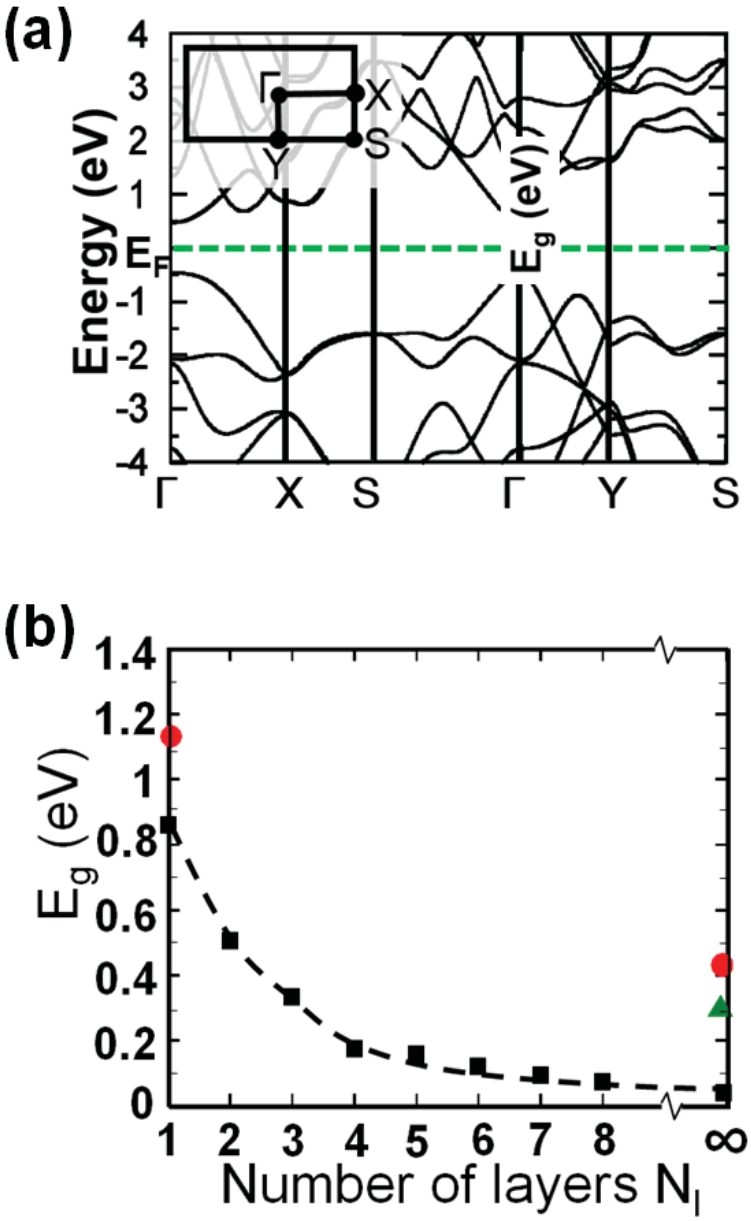

Fig. 6.2. Band structure and band gap evolution in phosphorene and few-layer black phosphorus

layer phosphorene, it is generally expected that the AFM-measured thickness value of a single layer 2D crystal on SiO_2/Si substrate is higher than the theoretical value; this is widely observed in graphene and MoS_2 cases. [100] Photoluminescence (PL) of exfoliated single layer phosphorene is observed in the visible wavelengths as shown

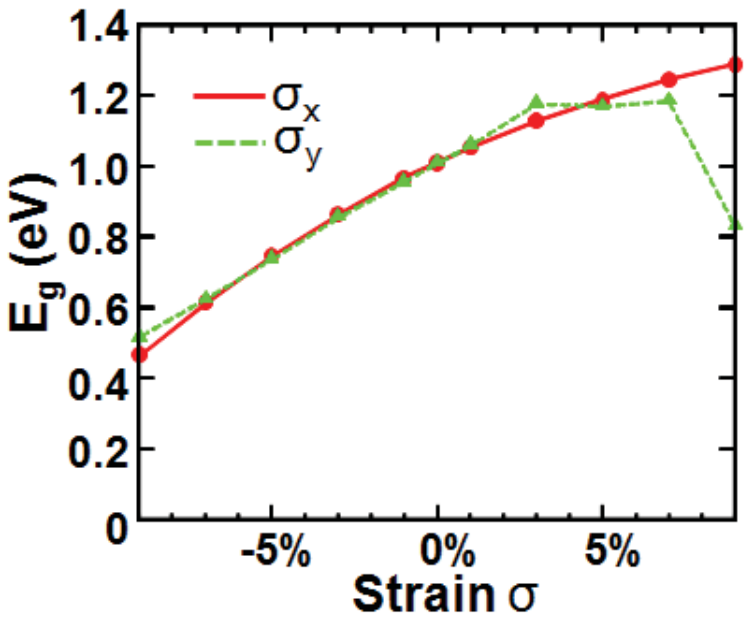

Fig. 6.3. Strain along the x- and y-direction related band gap evolution within single layer phosphorene

in Figure 6.5(a). For 10 nm thick black phosphorus flakes, no PL signal is observed within the detection spectrum range because the expected band gap of bulk black phosphorus is as low as 0.3 eV, falling in the infrared wave region. In contrast, a pronounced PL signal centered at 1.45 eV with a 100 meV narrow width is obtained on a single layer phosphorene crystal. This observed PL peak is likely of excitonic nature and thus a lower bound on the fundamental band gap value. The measured value of 1.45 eV indirectly confirms that the band gap in the monolayer is significantly larger than in the bulk. Further studies are required to properly interpret the PL spectra, which depend on the density of states, frequency-dependent quantum yield, the substrate, and the dielectric environment. The predicted increased band gap value in single layer phosphorene, caused by the absence of interlayer hybridization near the top of the valence and bottom of the conduction band, is consistent with the observed photoluminescence signal. The expected position of the PL peak for bilayer phosphorene is outside the spectral detection range. The Raman spectra of single

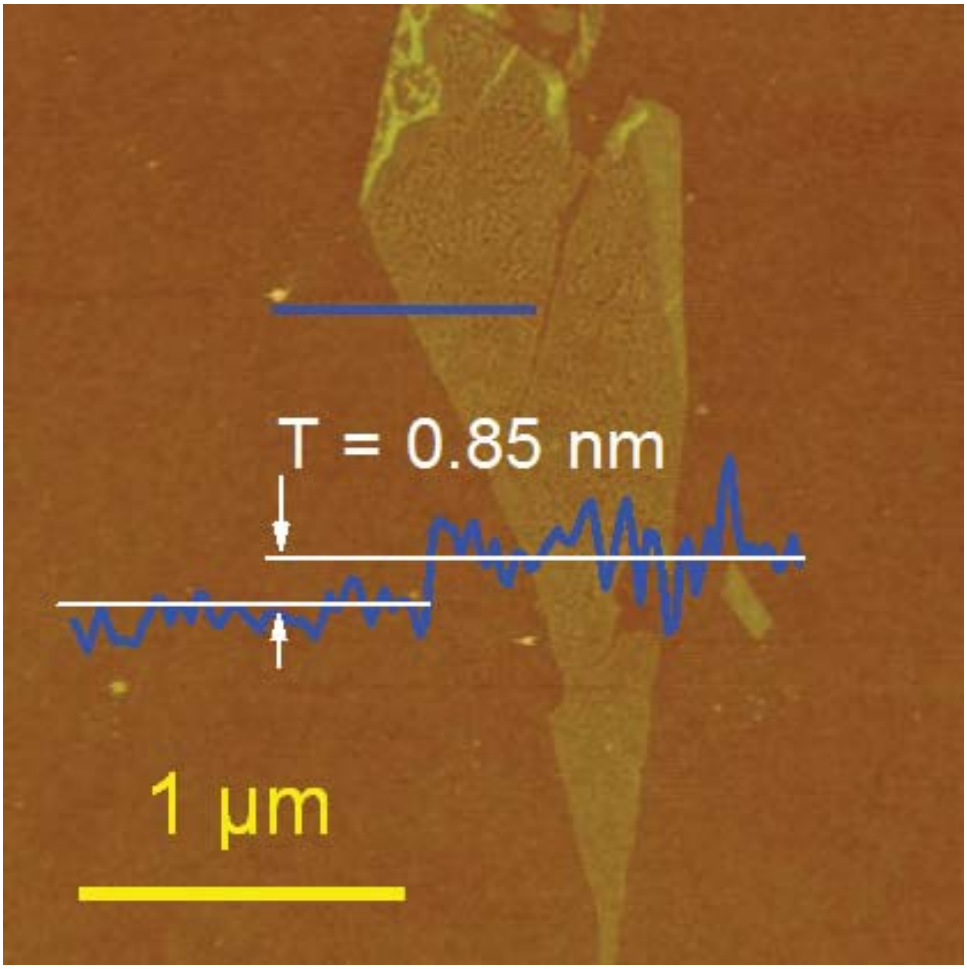

Fig. 6.4. AFM image of a single layer phosphorene

layer, bilayer, and bulk black phosphorus are presented in Figure 6.5(b). The Raman spectra show a well-defined thickness dependence, with the A_g^1 and A_g^2 modes shifting toward each other in frequency when the thickness is increased, similar to what has been observed in MoS_2. [9]

6.3 Transport Properties in Few-layer Phosphorene

Although single layer or bilayer phosphorene can be physically realized by exfoliation, it is more sensitive to the environment compared to graphene or MoS_2. All attempts to study transport properties or device performance on phosphorene films

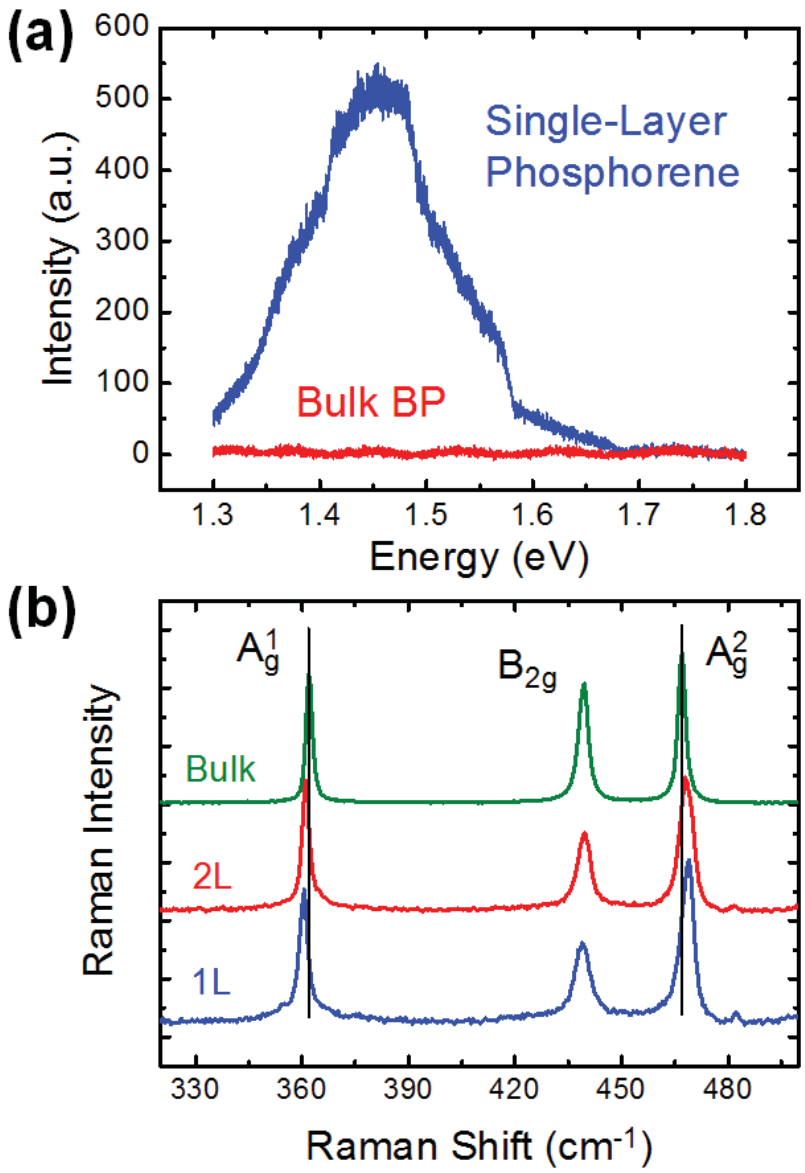

Fig. 6.5. PL and Raman spectra of single to few layer phosphorene

less than ∼2 nm thick were not successful. Since single layer phosphorene is one atomic layer thick, it should be more stable and display a lower defect density than transition metal dichalcogenides such as MoS_2. The processes to significantly reduce the defect density in back phosphorus and phosphorene films and to passivate the

defects and surfaces need to be further developed. Few-layer phosphorene thicker than 2 nm would be focused in the following transport and device experiments.

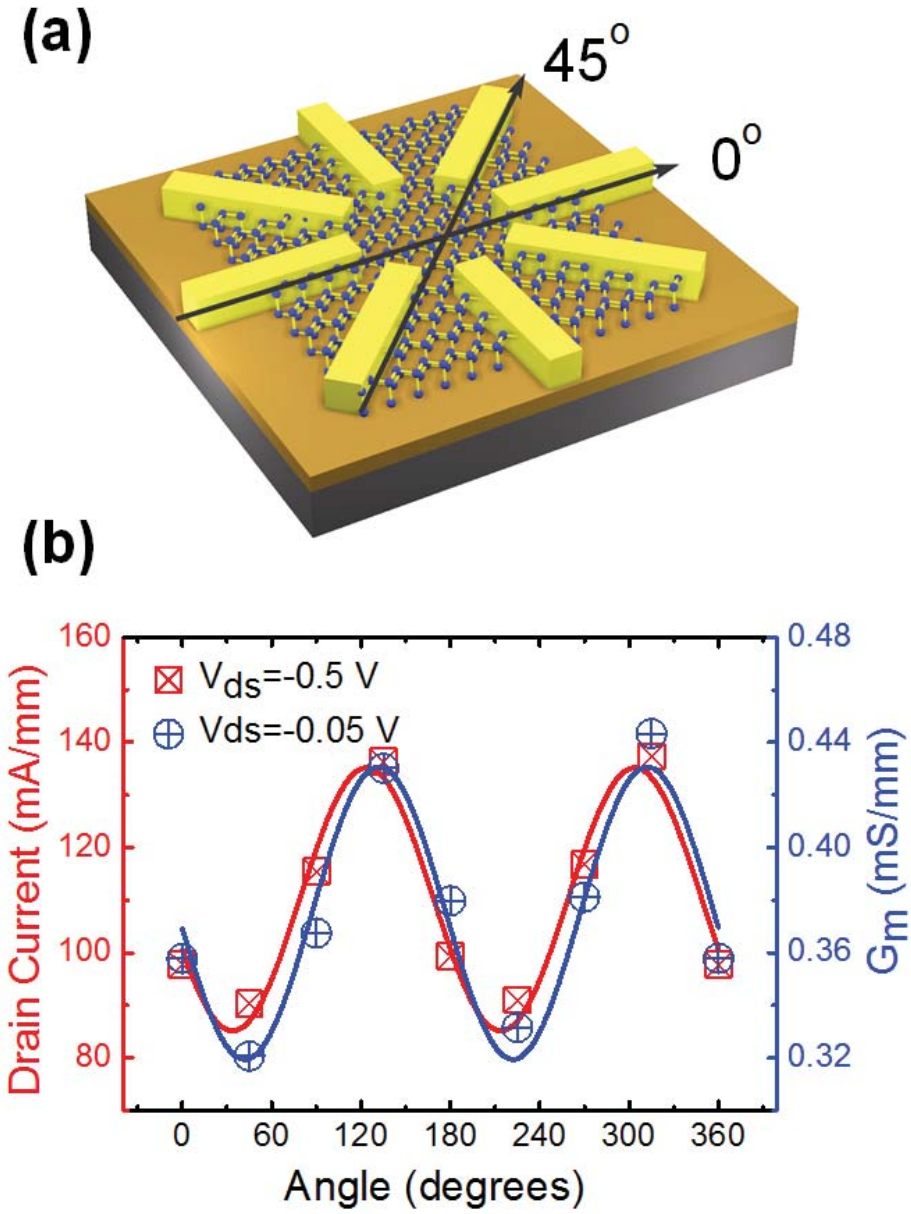

Fig. 6.6. Anisotropic transport in few-layer phosphorene

Anisotropic transport behavior along different directions is a unique property for few-layer phosphorene. A black phosphorus crystal with the thickness of 10 nm was

peeled and transferred onto a 90 nm SiO_2 capped Si substrate. Metal contacts were symmetrically defined around the crystal with 45° as the angular increment of the orientation, as shown in Figure 6.5(a). 1 μm wide 20/60 nm thick Ti/Au contacts to few-layer phosphorene were fabricated so that the spacing between all opposite bars was 5 μm. The four pairs of diametrically opposite bars are used as source/drain contacts for a transistor geometry and measured the transistor behavior for each of these devices. The maximum drain current at -30 V back gate bias and -0.5 V drain bias, which is displayed in Figure 6.5 (b) as a function of the orientation of the contact pair, shows clearly an angle-dependent transport behavior. The anisotropic behavior of the maximum drain current is roughly sinusoidal, characterized by the minimum value of ∼85 mA/mm at 45° and 225°, and the maximum value of ∼137 mA/mm at 135 and 315°. In spite of the limited 45° angular resolution, the observed 50% anisotropy between two orthogonal directions is significant. The same periodic trend can be found in the maximum value of the transconductance, which could be partially related to a mobility variation in the x-y plane of few-layer phosphorene. This large mobility variation is rarely seen in other conventional semiconductors. It could be partially related to the uniquely ridged structure in the 2D plane of few-layer phosphorene, seen in Figure 6.1, suggesting a different transport behavior along or normal to the ridges. On the basis of the band dispersion plotted in Figure 6.2(a), perpendicular to the ridges, corresponding to the Γ–X direction, the effective mass of electrons and holes $m_e \approx m_h \approx 0.3\ m_0$ is a fraction of the free electron mass m_0. Parallel to the ridges, along the Γ–X direction, the carriers are significantly heavier, with the effective mass of holes amounting to $m_h \approx 8.3\ m_0$ and that of electrons to $m_e \approx 2.6\ m_0$, suggesting anisotropic transport behavior. The observed anisotropy is less pronounced than the prediction because the angle resolution is as large as 45° and the fringe current flow in the real device averages out partly the anisotropy.

In order to investigate the nature of the metal/phosphorene junction, a three-terminal method, similar to the Kelvin probe, was used to measure the forward bias I-V characteristics of the Ti/phosphorene metal/semiconductor junction at the con-

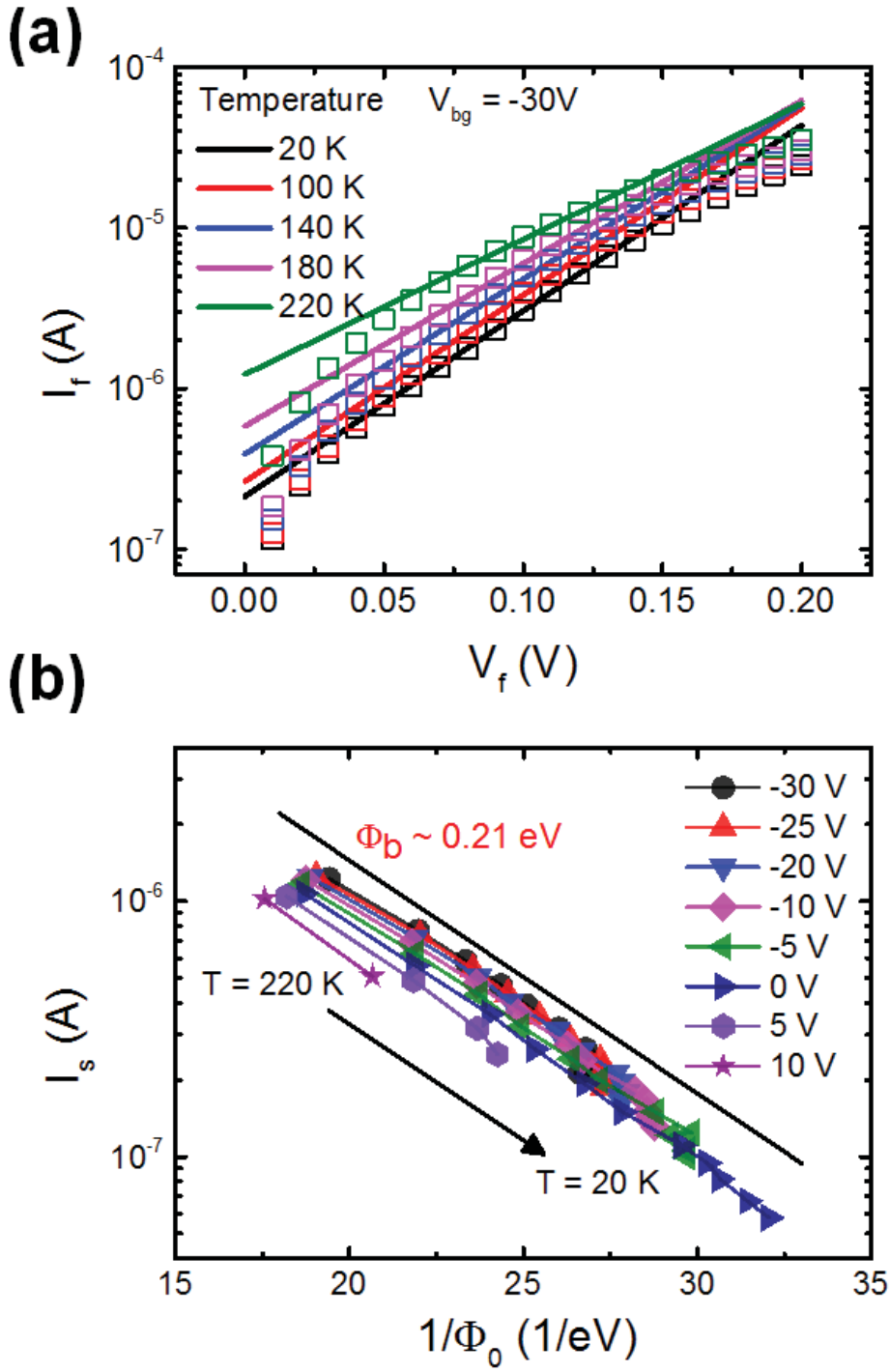

Fig. 6.7. Schottky barrier determination of Ti/black phosphorus junction

stant back gate voltage $V_{bg} = -30\ V$ and display the results in Figure 6.7(a). [101] Current was passed between two Ti/phosphorene contacts of a multi-terminal device with contacts around the perimeter of the phosphorene flake. Voltage was measured between the forward biased contact and a third contact adjacent to it with zero current flowing through the third contact. Under these conditions, the measured voltage difference is equal to the voltage across the forward biased Ti/phosphorene contact. These data show an exponential increase in the current I_f as the voltage V_f across the junction increases from 70 to 130 mV. In view of the degenerate doping of the phosphorene sample and the exponential I-V characteristics across this junction at temperatures as low as 20 K, thermally assisted tunnelling through the Schottky barrier is responsible for the transport through the junction. To determine the Schottky barrier height of the Ti/phosphorene contact, the exponential I-V characteristics is fitted by the equation:

$$I_f = I_s exp(V_f/\Phi_0) \tag{6.1}$$

where I_s is the characteristic current and Φ_0 is the characteristic energy, which characterizes transport across the junction at a particular temperature. Fits of the semilogarithmic plots in a wide temperature range are shown in Figure 6.7(a). The temperature-dependent characteristic current I_s can be furthermore viewed as proportional to $exp(\Phi_b/\Phi_0)$, where Φ_b is the height of the Schottky barrier at the metal-semiconductor junction and Φ_0 is a temperature-dependent quantity. This provides a way to use the temperature-dependent I-V measurements to determine Φ_b from the slope of the quantity log I_s as a function of $1/\Phi_0$. Figure 6.7(b) shows the corresponding plot, where each data point has been determined by fitting the I-V characteristic curve at a particular gate voltage and temperature. The slope of all curves shows an impressive independence of the measurement conditions, indicating the Schottky barrier height $\Phi_b \approx 0.21\ eV$ for holes at the Ti/phosphorene junction. The barrier height determined here is the true Schottky barrier height at the metal/phosphorene junction, not an effective Schottky barrier height that is commonly determined for metal/semiconductor junctions via the activation energy method. [11]

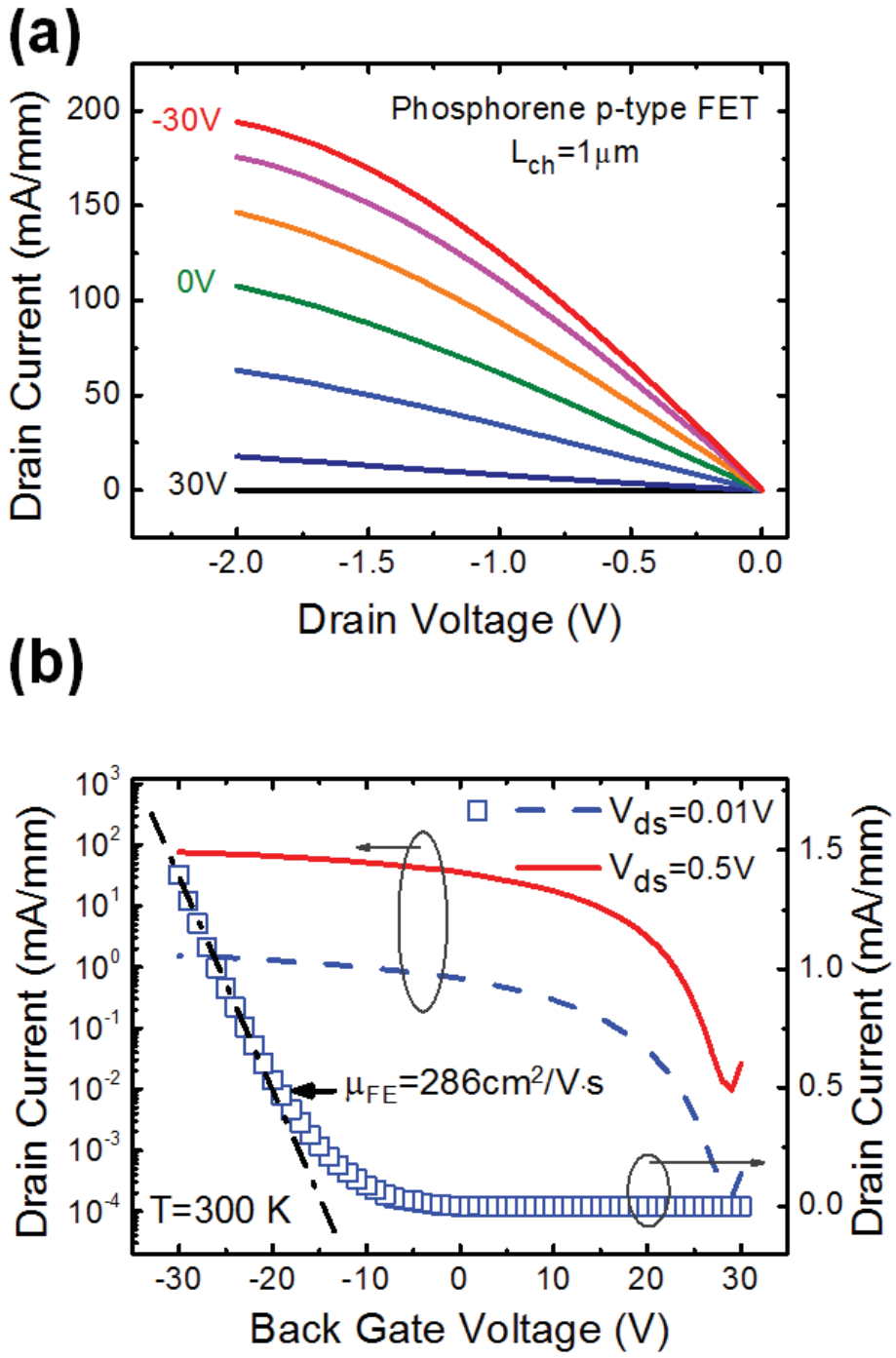

Fig. 6.8. Output and transfer characteristics of few-layer phosphorene transistors

6.4 Device Performance of Phosphorene Transistors

Transistors were fabricated on this novel 2D material in order to examine its performance in actual devices. Few-layer phosphorene was used with a thickness

ranging from 2.1 to over 20 nm. The I-V characteristic of a typical 5 nm thick few-layer phosphorene field-effect transistor for back gate voltages ranging from +30 to -30 V, shown in Figure 6.8(a), indicates a reduction of the total resistance with decreasing gate voltage, a clear signature of its p-type characteristics. Consequently, few-layer phosphorene is a welcome addition to the family of 2D semiconductor materials since most pristine TMDs are either n-type or ambipolar as a consequence of the energy level of S vacancy and charge-neutral level coinciding near the conduction band edge of these materials. [11,12] In only a few cases, p-type transistors have been fabricated by externally doping 2D systems using gas adsorption, which is not easily practicable for solid-state device applications.fang1,fang2 The observed linear I-V relationship at low drain bias is indicative of good contact properties at the metal/phosphorene interface. Good current saturation is also observed at high drain bias values, with the highest drain current of 194 mA/mm at 1.0 μm channel length at the back gate voltage $V_{bg} = -30\ V$ and drain voltage $V_{ds} = -2\ V$. In Figure 6.8(b), transfer curves are shown for drain bias values $V_{ds} = 0.01$ and $0.5\ V$, which indicate a current on/off ratio of 10^4, a very reasonable value for a material with a bulk band gap of 0.3 eV.

Inspecting the transfer curves in Figure 6.8(b), the maximum transconductance is found to range from $G_m = 45\ \mu S/mm$ at $V_{ds} = 0.01\ V$ to $2.28\ mS/mm$ at $0.5\ V$ drain bias. Using simple square law theory, it can estimated that the field-effect mobility μ_{FE} from $G_m = \mu_{FE} C_{ox}(W/L)V_{ds}$, where C_{ox} is the capacitance of the gate oxide, W and L are the channel width and length, and V_{ds} is the drain bias. These results for $V_{ds} = 0.01\ V$ indicate a high field-effect mobility $\mu_{FE} = 286\ cm^2/V{\cdot}s$ at room temperature, and the four-terminal measurements suggest a factor of 5 improvement at low temperatures. These values are still smaller than those in bulk black phosphorus, where the electron and hole mobility is ~1000 cm^2/V·s at room temperature and could exceed 15,000 cm^2/V·s for electrons and 50,000 cm^2/V·s for holes at low temperatures. [102] This might be due to the following factors to cause the mobility reduction in few-layer phosphorene. (i) The exposed surface of few-layer phosphorene is chemically unstable. Chemisorbed species from the process and the

environment change the electronic structure and scatter carriers, thus degrading the mobility. (ii) In a particular transistor, the current flow may not match the direction, where the material has the highest in-plane mobility. (iii) The Schottky barrier at the metal/phosphorene interface induces a large contact resistance within the undoped source/drain regions. The real mobility of few-layer phosphorene is expected to increase significantly upon appropriate surface passivation and in a high-k dielectric environment. [103]

The field-effect mobility in few-layer phosphorene transistors is further compared with various crystal thicknesses. Field-effect mobilities extracted from devices fabricated on phosphorene crystals with various thicknesses are displayed in Figure 6.9(a). Similar to previous studies on MoS_2 transistors, the field-effect mobility shows a strong thickness dependence. It peaks at around 5 nm and decreases gradually with further increase of crystal thickness. Such trend can be modelled with screening and interlayer coupling in layered materials, as proposed in several previous studies. [12] A more dispersive mobility distribution is observed for few-layer phosphorene transistors. This is due to the fact of anisotropic mobility in few-layer phosphorene or black phosphorus as discussed in previous parts and the random selection of crystal orientation in device fabrication. Thus carrier transports along at any directions between the two orthogonal ones in the x-y plane. Therefore, two curves are modelled for phosphorene transistors, as shown in Figure 6.9(a), where the red and green curves show the fittings with mobility peak and valley, respectively. The current on/off ratio is shown in Figure 6.9(b). It shows a general decreasing trend with increasing crystal thickness, steeply dropping from 10^5 for a 2 nm crystal to less than 10 once the crystal thickness exceeds 15 nm. This suggests the importance of crystal thickness selection of phosphorene transistors from the point of view of device applications. Transistors on a 4–6 nm crystal display the best trade-off with higher hole mobility and better switching behavior.

6.5 CMOS Logic based on All-2D Channel Materials

Finally, a CMOS logic circuit containing 2D crystals of pure few-layer phosphorene as one of the channel materials is demonstrated. Since phosphorene shows well-behaved p-type transistor characteristics, it can complement well n-type MoS_2 transistors. the simplest CMOS circuit element, an inverter is constructed, by using MoS_2 for the n-type transistor and phosphorene for the p-type transistor, both integrated on the same Si/SiO_2 substrate. Few-layer MoS_2 and phosphorene flakes were transferred onto the same substrate successively by the scotch tape technique. Source/drain regions were defined by e-beam lithography, similar to the PMOS fabrication described above. Different channel lengths of 0.5 μm for MoS_2 and 1 μm for phosphorene transistors were chosen to compensate for the mobility difference between MoS_2 and phosphorene by modifying the width/length ratio for NMOS and PMOS. Ti/Au of 20/60 nm was used for both MoS_2 and phosphorene contacts. Prior to top growth of a high-k dielectric, a 1 nm Al layer was deposited on the sample by e-beam evaporation. The Al layer was oxidized in ambient conditions to serve as the seeding layer. A 20 nm Al_2O_3 grown by ALD at 250 °C was used as the top gate dielectric. Finally, 20/60 nm Ti/Au was used for the top gate metal electrode and interconnects between the transistors. The final device structure is shown in Figure 6.10(a) and the corresponding circuit configuration in Figure 6.10(b). In the CMOS inverter, the power supply at voltage V_{DD} is connected to the drain electrode of the phosphorene PMOS. The PMOS source and the NMOS drain are connected and provide the output voltage signal V_{OUT}. The NMOS source is connected to the ground (GND). Both top gates of the NMOS and the PMOS are connected to the source of the input voltage V_{IN}. The voltage transfer characteristics (VTC) are shown in Figure 6.10(c). The power supply voltage was set to be 1 V. Within the input voltage range from -10 to -2 V, the output voltage shows a clear transition from V_{DD} to 0. A maximum gain of 1.4 is achieved. Due to the generally large contact resistance exhibited in 2D materials

and less obvious current saturation for Schottky barrier transistors, much more work is needed to improve the gain and move the 2D CMOS circuit research forward.

6.6 Summary

In summary, the optical and electrical properties and potential device applications of exfoliated single- and few-layer phosphorene films as a new p-type semiconducting 2D material with high hole mobility have been investigated. *Ab-initio* calculations were used to determine the equilibrium structure and the interlayer interaction of bulk black phosphorus as well as few-layer phosphorene with 1-4 layers. Theoretical results indicate that the band gap is direct, depends on the number of layers and the in-layer strain, and is significantly larger than the bulk value of 0.31–0.36 eV. A single layer phosphorene film was successfully achieved. The observed photoluminescence peak in the visible wavelength from single layer phosphorene indirectly confirms the widening of the band gap as predicted by theory. Substantial anisotropy was found in the transport behavior of this 2D material, which is associated with the unique ridge structure of the layers. The overall device behavior can be explained by considering a Schottky barrier height of 0.21 eV for hole tunneling at the junctions between phosphorene and Ti metal contacts. P-type transistors of few-layer phosphorene was fabricated with a high on-current of 194 mA/mm at 1.0 μm channel length, a current on/off ratio over 10^4, and a high field-effect mobility up to 286 $cm^2/V{\cdot}s$ at room temperature. A CMOS inverter was constructed by combining a phosphorene PMOS transistor with a MoS_2 NMOS transistor, thus achieving heterogeneous integration of semiconducting phosphorene crystals as a novel channel material for future electronic applications.

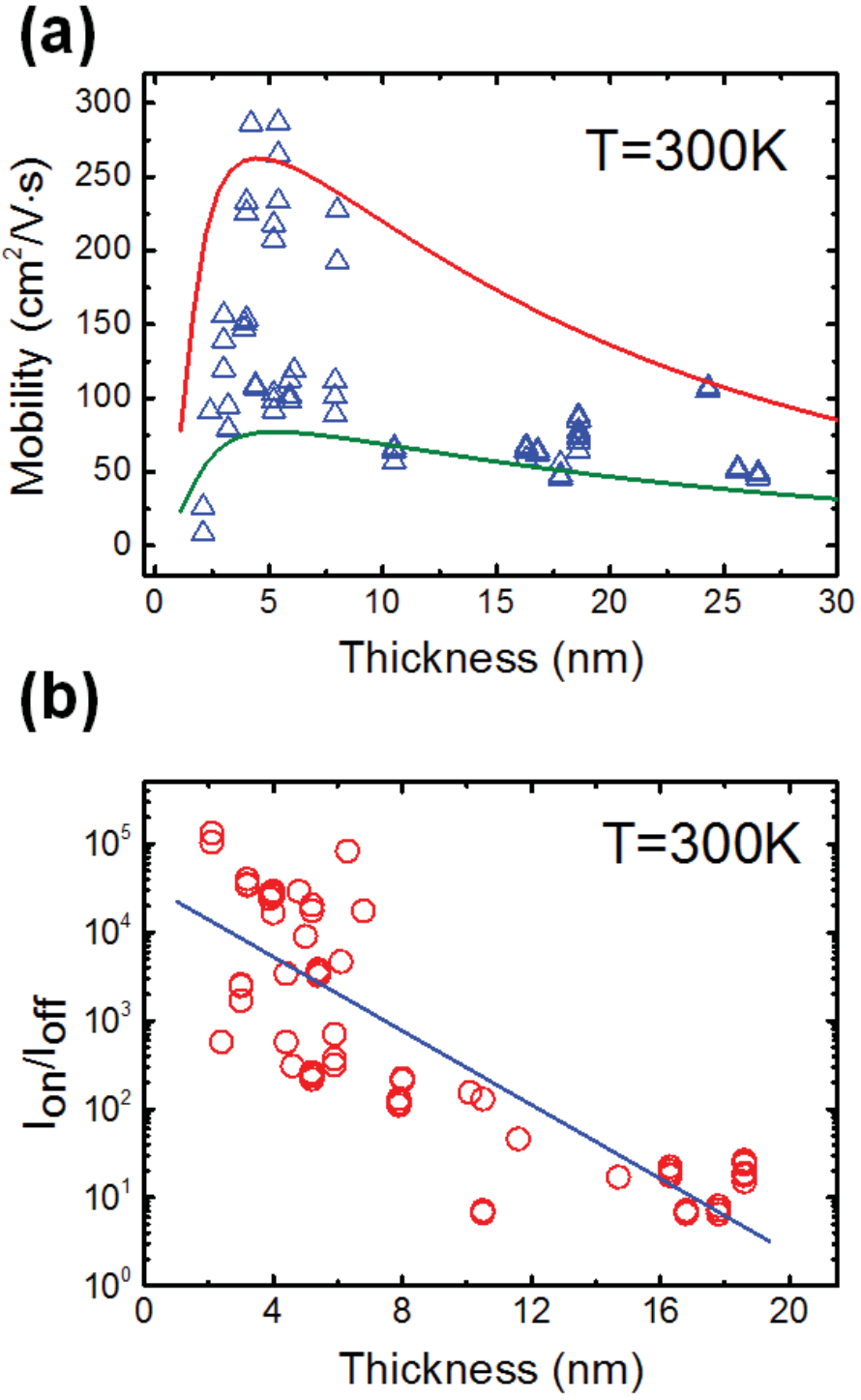

Fig. 6.9. Channel thickness dependent field-effect mobility and current on/off ratio in phosphorene transistors

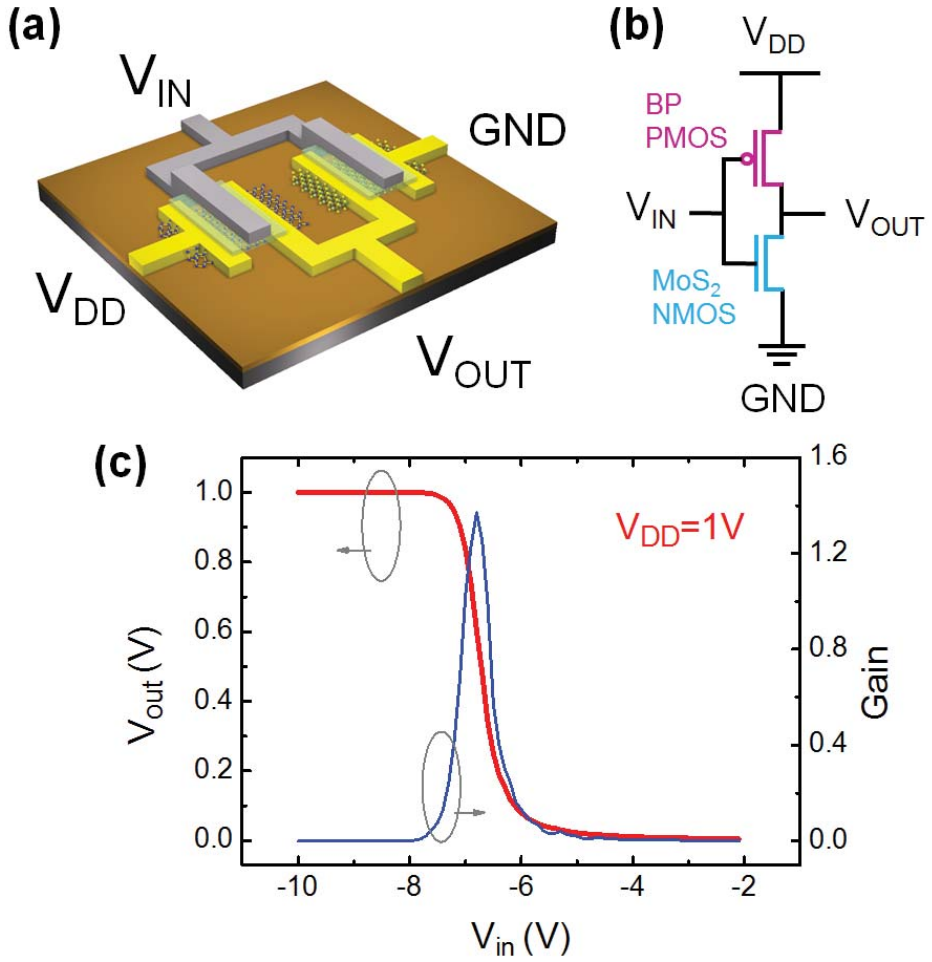

Fig. 6.10. CMOS inverter based on 2D channel materials

7. CONCLUSIONS

In Chapter 2, dielectric integration was studied on various 2D crystals. ALD Al_2O_3 were grown on MoS_2 and h-BN at different temperature. A direct ALD growth was demonstrated on both crystals at lower growth temperature. DFT study was performed to show ALD growth on 2D crystals rely on physical adsorption of the precursors instead of chemical adsorption, and this physical adsorption is enhanced by in-plane polarization of the 2D substrate.

In Chapter 3, n-type MoS_2 transistors were demonstrated and studied. Double-gate MoS_2 transistors were achieved with ALD Al_2O_3 dielectric. Dimension scaling of the transistors was investigated. Short channel MoS_2 devices down to 50 nm show strong immunity to short channel effects. In addition, channel width scaling of the devices results a clear change from depletion to enhancement mode transistors when width of the transistors is less than 200 nm.

In Chapter 4, metal contact on 2D crystals was discussed. Contact resistance between MoS_2 and metal is studied. A weak Fermi-level pinning at metal/2D semiconductor interface is determined in both MoS_2 and WSe_2 transistors. The energy level of FLP is determined by the position of charge neutrality level in the band edge alignment. High performance dual gate MoS_2 transistors were realized by using low-work function titanium as metal contacts with on-current up to 268 mA/mm.

In Chapter 5, single layer MoS_2 crystals were synthesized by CVD method. Transistors were fabricated on these crystals with channel length down to 100 nm and their device characteristics were statistically analysed. In addition, MoS_2 transistor behavior with various contact lengths was studied. The device performance is strongly related to the contact dimensions. By extracting the transfer length, switching behavior of MoS_2 transistors is revealed to be modulated by two Schottky barriers.

In Chapter 6, a novel p-type 2D semiconductor, black phosphorus and phosphorene, are investigated. *Ab-initio* calculations were used to determine the equilibrium structure and the interlayer interaction of bulk black phosphorus as well as few-layer phosphorene. Transistors based on few-layer phosphorene show good device performance with on current up to 194 mA/mm and hole mobility up to 286 $cm^2/V{\cdot}s$. A CMOS inverter was demonstrated by combining MoS_2 NMOS and phosphorene PMOS.

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VITA

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PUBLICATIONS

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