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To my family and friends near and far.

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ABSTRACT

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In contrast to conventional bulk-silicon technology, polysilicon (poly-Si) thin-film transistors (TFTs) can be implanted in flexible substrate and can have low process temperature. These attributes make poly-Si TFT technology more attractive for new applications, such as flexible displays, biosensors, and smart clothing. However, due to the random nature of grain boundaries (GBs) in poly-Si film and self-heating enhanced negative bias temperature instability (NBTI) , the variability and reliability of poly-Si TFTs are the main obstacles that impede the application of poly-Si TFTs in high-performance circuits. The primary focus of this dissertation is to develop new design methodologies and modeling techniques for facilitating new applications of poly-Si TFT technology. In order to do that, a physical model is first presented to characterize the GB-induced transistor threshold voltage (V_{th}) variations considering not only the number but also the position and orientation of each GB in 3-D space. The fast computation time of the proposed model makes it suitable for evaluation of GB-induced transistor V_{th} variation in the early design phase. Furthermore, a self-consistent electro-thermal model that considers the effects of device geometry, substrate material, and stress conditions on NBTI is proposed. With the proposed modeling methodology, the significant impacts of device geometry, substrate, and supply voltage on NBTI in poly-Si TFTs are shown. From a circuit design perspective, a voltage programming pixel circuit is developed for active-matrix organic light emitting diode (AMOLED) displays for compensating the shift of V_{th} and mobility in driver TFTs as well as compensating the supply voltage degradation. In addition, a self-repair design methodology is proposed to compensate the GB-induced variations

for liquid crystal displays (LCDs) and AMOLED displays. Based on the simulation results, the proposed circuit can decrease the required supply voltage by 20% without performance and yield degradation. In the final section of this dissertation, an optimization methodology for circuit-level reliability tests is explored. To effectively predict circuit lifetime, accelerated aging (i.e. elevated voltage and temperature) is commonly applied in circuit-level reliability tests, such as constant voltage stress (CVS) and ramp voltage stress (RVS) tests. However, due to the accelerated aging, shifting of dominant degradation mechanism might occur leading to the wrong lifetime prediction. To get around this issue, we proposed a technique to determine the proper stress range for accelerated aging tests.

1. INTRODUCTION

1.1 Overview

Recently, TFTs have drawn increasing attention due to their unique advantages over the mono-crystalline silicon counterpart, such as low process temperature and low manufacturing cost. The low process temperature of TFT technology leads to flexibility in selection of the substrate material. Hence, TFTs can expand the application space of traditional silicon technology by enabling both fabrication of large-area electronics and device integration directly on transparent, light-weight and flexible substrates. Furthermore, the manufacturing cost of TFT-based circuit is significantly lower compared to conventional bulk CMOS technology because of the low temperature process, cheap and large substrate, and low-mask count [1]. These attributes make TFT technology attractive and suitable for several new applications including bio-sensors for real time personal health monitoring, flexible displays for portable electronic devices, radio frequency identification (RFID) for inventory and supply chain management, and smart clothing for home healthcare [2]- [5]. In particular, poly-Si TFT technology is expected to be one of the most promising candidates for such applications because of the higher mobility and the better reliability as compared with other TFT technologies [1]. However, suffering from the nature of the diverse and complicated grain distribution, a spread in the electrical characteristics of individual poly-Si TFTs (e.g., V_{th} and mobility) is unavoidable [6] [7]. This not only results in high leakage and low drivability transistors, but also leads to large variations between adjacent poly-Si TFTs. Furthermore, since NBTI-induced degradation is triggered by the combined effects of high channel temperature and electric field, the device degradation due to NBTI in poly-Si TFT is more severe as compared to mono-crystalline silicon devices because of the low heat conductance of TFT substrates (e.g. glass and

polyimide substrates). The heat generated from the device on silicon substrate can be easily spread and dissipated due to the excellent heat conductivity of the silicon substrate and the presence of heat sink. Conversely, the heat generated by a poly-Si TFT, is hard to exchange or diffuse through the substrate due to the poor heat conductivity of substrate and the absence of heat sink. Consequently, the temperature of poly-Si TFTs is expected to be higher, more localized and sensitive to device geometry, as verified by experiments [8]- [11]. Besides, it is experimentally observed that the spread of device characteristics due to GBs and NBTI deteriorates with device scaling [12]. Accordingly, such severe device variations and reliability concern not only limit the application of poly-Si technology in high performance circuits, but also inhibit the TFT scaling for low power, higher density, and higher integration. The purpose of this dissertation is to facilitate the poly-Si TFT technology for future applications by proposing new modeling and design methodologies in different levels of hierarchy (device and circuit).

1.2 Poly-Si TFT Variation due to GBs

As we mentioned in the previous subsection, aggressive transistor scaling has aggravated the GB-induced V_{th} variation in poly-Si TFTs. These fluctuations are attributed to the random number, location and orientation of GBs in the device channel. This means that, GB-induced V_{th} modeling not only requires the knowledge of the number of GBs, but also the location and orientation of the individual GBs in the channel region. Hence, development of a V_{th} model considering GB in 3-D space is essential to capture the effects of GB on V_{th} of TFTs.

The existing simulation methods, which are based on drift-diffusion model [13] and ignore the impact of GB location [12], fail to meet efficiency and accuracy. In this work, we proposed a modeling framework which captures the effect of GBs on the V_{th} variations considering the number, the position, and the orientation of GBs and is based on fundamental laws of physics [14]. Compared to the existing literature,

the salient features of the proposed model are as follows: 1) it takes into account the position of GBs in the channel, 2) it is applicable to both long and short channel devices, 3) the model can consider different crystallization methods (i.e. periodic or randomly distributed GBs), 4) it is analytical (i.e. the threshold voltage are derived in closed form) and, 5) it is computationally fast (200x faster compared to 3-D device simulator [15]).

1.3 Poly-Si TFT Degradation due to NBTI

In addition to GB-induced V_{th} variations, NBTI causes severe time-dependent V_{th} degradations due to the low heat conductivity of TFT substrate. Therefore, to ensure robust and stable functionality for future poly-Si TFT-based circuits, it is essential to properly model and mitigate the effects of self-heating induced NBTI. In this thesis, an electro-thermal model which helps in accurately modeling NBTI degradation in poly-Si TFTs is developed [16]. One of important features of the proposed model is self-consistency. To have more accurate degradation prediction, self-consistency in degradation prediction model is needed. This is due to the fact that self-heating power and electrical field in the oxide decrease with time as the threshold voltage increases. Using the proposed framework, the significant impacts of device geometry, substrate material and thickness, and supply voltage on NBTI in poly-Si TFTs are shown. The simulation results reflect on the main obstacles for future flexible electronics and validate the need for integration of thermal-diffusion model and NBTI model for precisely predicting NBTI-induced degradation in poly-Si TFTs.

1.4 AMOLED Pixel Circuit Design for Variation Compensation

AMOLED display features light weight, slim form factor and fast response time as compared to AMLCD. However, AMOLED is limited to small-sized applications due to 1) OLED degradation and 2) the high sensitivity of the drive current to the device variation and degradation of driving TFTs. OLED degradation refers to the

progressive and spatial loss of efficiency over time during operation. To improve OLED degradation, research groups focus on (i) thermal stability, (ii) trap luminescence quencher formation, (iii) interface degradation, and (iv) anode instability of OLED [17]. On the other hand, to tackle the variation and degradation of driving TFTs, various compensation approaches have been investigated at the circuit level. Voltage programming methodology (VPM) is one of most common techniques for addressing the non-uniformity issue associated with AMOLED displays [18]. Although this methodology can effectively eliminate the effect of V_{th} shift in driving TFTs (DTFTs) and supply voltage degradation, it fails to mitigate the current variation induced by the mobility variation in DTFTs. The dependence of drive current to the mobility variation in poly TFTs is approximately 10% [19], and hence, is not acceptable for high performance display applications. To cope with this problem, an improved VPM pixel circuit, which is capable of addressing mobility variation, V_{th} shift and supply voltage degradation, is proposed and verified [20]. Consequently, the immunity to device variations, fast programming time, and the simplicity of peripheral circuits, make the proposed VPM pixel circuit a promising candidate for large sized and high resolution AMOLED display applications.

1.5 Self-repair Design Methodology for Variation Compensation

To ensure sufficient drivability in all pixel switches of LCD and AMOLED, increasing the supply voltage is the most commonly applied technique to account for the worst-case combination of variabilities. However, high supply voltage greatly increases the power consumption and worsens the reliability of TFTs [21]. Moreover, as the panel size or resolution is increased, yield loss, due to GBs and global variation, becomes more and more significant, even with a high supply voltage. Therefore, it is important to develop a new design methodology to properly deal with the variations in charging time of pixel switches and to reduce the resultant yield loss. In this thesis, a self-repair circuit is proposed to detect the locations and extend the charging time

of defective pixels (i.e. pixels with insufficient drivability) at the expense of slight increase in the operating frequency of peripheral circuits [22]. In other words, to maintain the same refresh rate, the charging time of each row of pixel array is slightly decreased for creating timing slacks which allow a few rows to execute two-cycle operation. Therefore, a lower supply voltage can be used while maintaining the same yield since defective pixels are allowed to have longer charging time. Consequently, with the proposed circuit, reliability and power consumption of LCD and AMOLED display can be improved.

1.6 Circuit-Level Reliability Test Optimization

In nominal operating conditions, NBTI is expected as the dominant mechanism for circuit performance degradation, while hot carrier injection (HCI) can be neglected. However, accelerated aging which is commonly applied in reliability tests, such as constant voltage stress (CVS) and ramp voltage stress (RVS) tests [23]- [24], might shift the dominant degradation mechanism from NBTI to HCI leading to the wrong lifetime predictions. To distinguish HCI effects on a differential voltage controlled oscillator (VCO), different stress voltages and frequencies are applied in CVS and RVS tests [25]. Based on the results, we validated that the dominant degradation mechanism shifts from NBTI to HCI as stress voltage and frequency increase. Furthermore, a methodology defining proper stress conditions for accelerated circuit reliability tests is proposed for better lifetime prediction. Note that, although the tested circuit is based on SOI technology, the conclusions and the proposed optimization methodology in this study should also apply to TFT-based circuits.

1.7 Organization

The rest of this thesis is organized as follows. In chapter 2, the physics-based 3-D model for GB-induced V_{th} variation is presented and statistical analysis for different electrical quantities and device and grain size is provided. Chapter 3 describes the

self-consistency electro-thermal model for NBTI effect in p-type poly-Si TFT with different substrate materials and device geometries. The proposed enhanced VPM pixel circuit for AMOLED display is discussed in Chapter 4. In Chapter 5, a new self-repair design methodology to compensate the GB-induced variations for poly-Si TFT based LCD and AMOLED display is reported. A methodology for optimizing circuit-level reliability tests is proposed in Chapter 6. Finally, Chapter 7 summarizes the contributions of this research and concludes the dissertation.

2. A PHYSICEL MODEL FOR GRAIN BOUNDARY INDUCED THRESHOLD VOLTAGE VARIATION IN POLY-SILICON THIN-FILM TRANSISTORS

Grain boundaries (GBs) in the channel region of poly-silicon thin-film transistors (Poly-Si TFTs) lead to large variations in the performance of TFTs (delay and power). In this work, we present a physical model to characterize the GB-induced transistor threshold voltage variations considering not only the number but also the position and orientation of each GB in the 3-D space. The estimated threshold voltage variations show a good agreement with experimental data and simulations performed by a numerical 3-D drift-diffusion device simulator. Using the proposed model, the impact of GBs on TFTs for various grain sizes, device sizes and source-drain voltages, is discussed in detail. Specifically, when the grain size is comparable to the size of the device, we observed that threshold voltage (V_{th}) variations increase significantly and V_{th}-distributions are non-Gaussian. Finally, using our model we predict and demonstrate the GB-induced variations under different crystallization methods, such as sequential lateral solidification.

2.1 Introduction

In contrast to conventional bulk-silicon technology, TFT features low manufacturing cost and flexibility in selection of the substrate material (i.e. glass and plastic). These attributes make TFT technology more attractive for new applications, such as flexible displays, bio-sensors and smart clothing [1]. In particular, poly-Si TFT technology is expected to be one of the most promising candidates for such applications because of higher mobility and better reliability as compared with other TFT technologies [1]. However, due to the random nature in the number, the position and the

orientation of grain boundaries (GBs) in poly-Si films, the device variation between adjacent poly-Si TFTs is large and cannot be modeled using current compact models. This can impede the application of poly-Si TFTs in high performance circuits and advanced displays (e.g. active matrix organic lighting diode display). Furthermore, it is evident that the continuing demand for device and supply voltage scaling aggravates GB-induced variations [12]. As a result, to design circuits with poly-Si TFTs for future applications, fast and accurate models that predict the GB-induced statistical fluctuations are essential [12].

For the analysis of statistical variations induced by GBs, there have been several models proposed by different research groups. The authors in [12] and [27] estimate mobility and V_{th} variations assuming that each GB has the same impact independent of the position and the orientation in the channel region. However, this assumption is valid only when the device size is larger than the average grain size. When the grain size is comparable to the device size, the number of GBs in the channel region decreases making the position of GBs more significant in determining the characteristics of a poly-Si TFT [28]. Thus, modeling threshold voltage variations accounting only the number of GB underestimates the real distribution [12]. For solving this issue, authors in [13] investigated the influence of GBs using a 2-D drift-diffusion device simulator. Although the position dependence of GB-induced variations can be precisely predicted, this methodology is not suitable for large-scale circuits due to significant computational cost to simulate a device. Furthermore, a 2-D device simulator is not able to capture the effects of GB orientation, which is a 3-D effect. Hence, there is a need for a new model which can efficiently capture the GB-induced statistical variability in scaled poly-Si TFTs.

In this section, a physics-based model is proposed for characterizing the threshold voltage variations for poly-Si TFTs which simultaneously takes into account the number, the position and the orientation of GBs [14]. The highlights of this model are: 1) it takes into account the exact position of GBs in the 3-D space, 2) it is applicable for both long and short channel devices, 3) the model is adaptive and can consider

different crystallization methods (i.e. different distribution of GBs, such as periodic or random distribution), 4) it is analytical, since expressions for the threshold voltage are derived in closed form, 5) it is computationally fast (200x faster) compared to 3-D drift-diffusion simulator [15]. The above features make the proposed model suitable for estimation of the parametric yield of poly-Si TFT-based circuit at the early design phase.

The rest of the paper is organized as follows. In subsection II we present in detail the proposed simulation framework. Then, the fundamental laws of physics and detailed statistical modeling methodology for evaluating GB-induced potential barrier, surface potential, and threshold voltage are explained. In subsection III, we verify the proposed model with both numerical 3-D drift-diffusion simulator [15] and experimental data [12]. The simulated statistical results for different device sizes, supply voltages and crystallization processes are also presented and discussed. Finally, we conclude this work in subsection IV.

2.2 The Framework

The proposed approach determines the GB-induced threshold voltage variation by the evaluation of surface potential in the channel. The estimation of surface potential in this work is divided into two parts; a contribution that comes from the effect of the applied voltages, and a contribution, which is from the charge traps in the distributed GBs. Note that, the trap states in the grain and oxide-silicon interface are neglected, since the threshold voltage of poly-Si TFT is dominated by GBs in the channel region [1]. The flowchart of the proposed simulation framework is shown in Fig. 2.1. The details of the individual steps are presented in the following subsections.

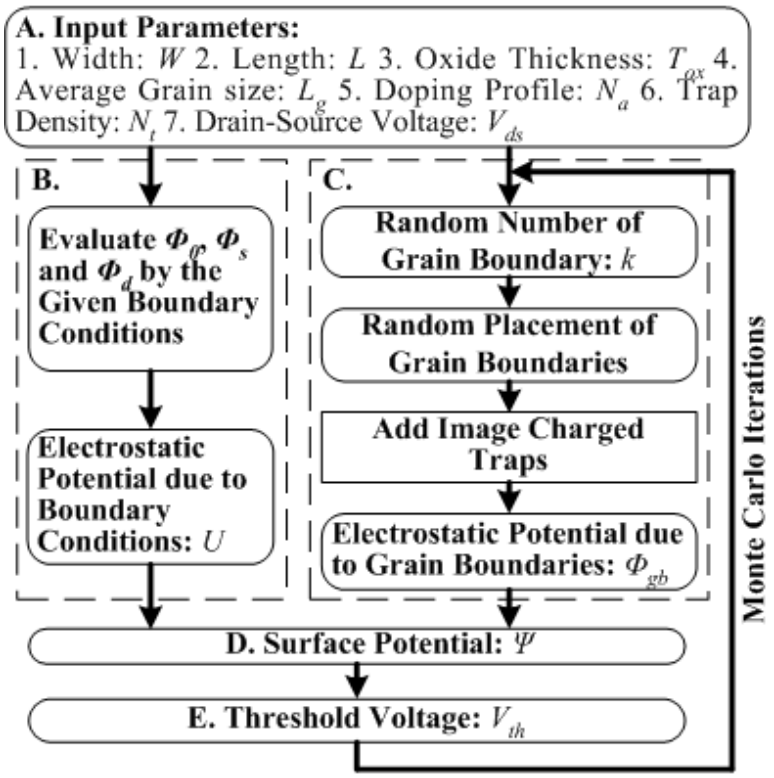


Fig. 2.1. Flowchart showing the simulation methodology for statistical analysis of V_{th} variation induced by GBs.

2.2.1 Input Parameters

In the beginning of the simulation, basic input parameters are necessary to define the geometry and the characteristic behavior of a poly-Si TFT. These input parameters include: 1) device width W, 2) device length L, 3) oxide thickness T_{ox}, 4) average grain size L_g, 5) doping profile N_a, 6) trap density of GBs N_t and 7) drain-source voltage V_{ds}.

2.2.2 Modeling Electrostatic Potential due to Boundary Conditions

In this sub-section, the analytical solution of the electrostatic potential, which satisfies the boundary conditions at the gate, source and drain electrodes, is pre-

sented. The solution technique makes use of the superposition principle and divides the solution into the following terms [29]:

$$U(x,z) = \Phi(x,z) + \Phi_s(x,z) + \Phi_d(x,z) + \Phi_b(x,z) \tag{2.1}$$

where x is along the direction of device length, z is along the direction of substrate thickness, Φ is the solution of the Poisson equation that satisfies the boundary conditions in the gate electrode, Φ_s, Φ_d and Φ_b are the solutions to Laplace equation that satisfy the boundary conditions at the source, the drain and the body electrodes, respectively. Note that Φ_b is neglected in this work, since it is one order smaller than Φ_s and Φ_d [30]. By solving the following two equations, one can obtain Φ [29]:

$$\Phi(x,z) = \Phi_0 \left(1 - \sqrt{\frac{qN_a}{2\varepsilon_{si}\Phi_0}} z\right)^2 \tag{2.2}$$

$$\frac{V_g - V_{fb} - \Phi_0}{3t_{ox}} = \sqrt{\frac{2qN_a\Phi_0}{\varepsilon_{si}}} \tag{2.3}$$

where Φ_0 is the long channel surface potential, V_g is the gate voltage and V_{fb} is the flatband voltage. The solutions for Φ_s and Φ_d are derived in [29] and can be expressed in the following forms:

$$\Phi_s(x,z) = \frac{b_1 \sinh\left(\frac{\pi(L-x)}{W_d+3t_{ox}}\right) \sin\left(\frac{\pi(z+3t_{ox})}{W_d+3t_{ox}}\right)}{\sinh\left(\frac{\pi L}{W_d+3t_{ox}}\right)} \tag{2.4}$$

$$\Phi_d(x,z) = \frac{c_1 \sinh\left(\frac{\pi x}{W_d+3t_{ox}}\right) \sin\left(\frac{\pi(z+3t_{ox})}{W_d+3t_{ox}}\right)}{\sinh\left(\frac{\pi L}{W_d+3t_{ox}}\right)} \tag{2.5}$$

$$b_1 = \frac{4}{\pi}\Phi_{bi} - \frac{2}{\pi}\left(1 - \frac{4}{\pi^2}\right)\left(1 + \frac{6t_{ox}}{W_d}\Phi_0\right) \tag{2.6}$$

$$c_1 = \frac{4}{\pi}\left(\Phi_{bi} + V_{ds}\right) - \frac{2}{\pi}\left(1 - \frac{4}{\pi^2}\right)\left(1 + \frac{6t_{ox}}{W_d}\Phi_0\right) \tag{2.7}$$

where Φ_{bi} is the built-in potential and W_d is the depletion width. Although these are the analytical solutions for 2-D devices, we applied it in 3-D devices by assuming identical electrostatic potential along y-axis (device width direction).

2.2.3 Modeling Electrostatic Potential due to GBs

The GBs in the channel statistically affect the device performance through the concurrent fluctuations in the number, the position and the orientation [12]. Hence, for accurate prediction of threshold voltage variation, one of the most important steps is to determine the statistical distribution of GBs in the device channel since it dominates the statistical behavior of the device ensemble. In this subsection, we first model the number of GBs in the channel. Then, we present a statistical modeling methodology to capture the random placement of GBs. Finally, the method for evaluation of the electrostatic potential contributed by GBs (Φ_{gb}) is introduced.

Random Number of GBs

The number of GBs in the channel is statistically modeled using Poisson distribution which is normally used to express the probability of a given number of events occurring in a given area. Accordingly, the probability of having exactly k GBs (where k is a non-negative integer) in the channel can be expressed as:

$$P(k,\lambda) = \frac{e^{-\lambda} \cdot \lambda^k}{k!} \tag{2.8}$$

$$\lambda = \frac{L}{L_g} + \frac{W}{L_g} \tag{2.9}$$

where λ is the expected mean of the number of GBs in the channel, L and W are the device length and width respectively, L_g is the average grain size.

Random Placement of GBs

The GBs degrade the channel conductance by capturing free carriers in the trap states inside the GB area and creating a repulsive Coulomb blockade well surrounding the trap (i.e. potential barrier) [31]. Furthermore, the height of the potential barrier is not uniform along GB and depends on the applied voltage and the position of the

GB along the channel. This is attributed to the fact that, when large drain voltage is applied, the bottom of conduction band is lower near the drain edge [31]. As a result, the potential barrier formed by the GBs closed to the drain side becomes insignificant and has less impact on the peak of band diagram in the channel. On the other hand, if GB is positioned in the middle of channel, the peak of band diagram will increase significantly by the potential barrier induced by the GB. Hence, GBs near the center of channel have the largest influence on the current degradation [31]. In addition, different orientation of GBs resulting in different length and position of GBs in the channel would also cause different impact. As a result, we can expect that each GB in the channel has different effect on the device degradation due to its own position and orientation and should be taken into account for precise modeling of GB-induced degradation. To simulate the random placement of GB, a sequence of four random numbers (V_i) is generated. Three random numbers (V_1, V_2 and V_4) are responsible for deciding the direction of the GB. Specifically, V_1 and V_2 decide the angle between the vector and x-axis (θ), while V_4 is responsible for the incline direction of the vector (as illustrated in Fig. 2.2). The other random number (V_3) is for the location of the cross point between the GB and x-axis. The randomly distributed GBs are, therefore, related to these computer-generated random numbers by:

$$V_1 x + (1 - 2K) \cdot V_2 y = -K V_2 W + (V_2 W + V_1 L) \cdot V_3 \tag{2.10}$$

$$0 < V_4 \leq 0.5 : K = 0 \tag{2.11}$$

$$0.5 < V_4 \leq 1 : K = 1 \tag{2.12}$$

The above plane equation describes the random position and direction of grain boundaries inside the channel region. Note that, V_1, V_2, V_3 and V_4 are random numbers uniformly distributed between 0 and 1. Hence, Eqs. 2.11-2.12 for V_4 imply that the probability that the vector inclines to positive x-direction is the same as that for negative x-direction.

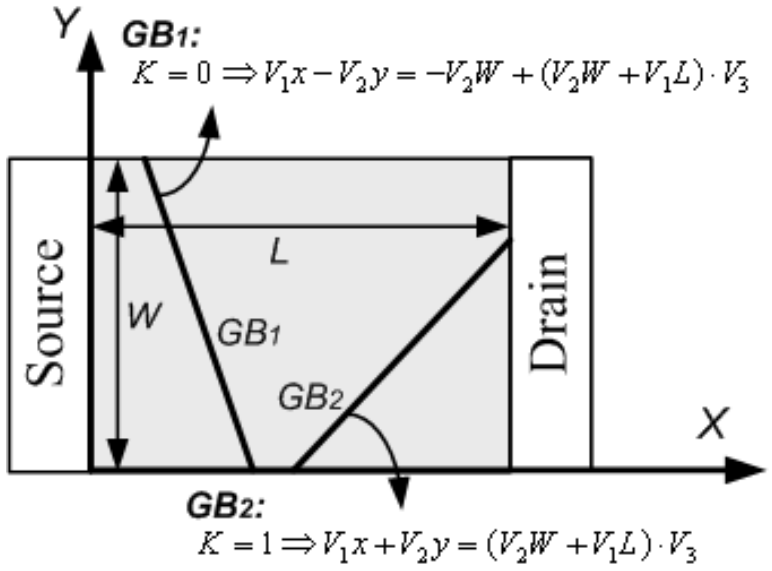


Fig. 2.2. Illustration of the randomly assigned plane equations for GBs in the channel of poly-Si TFT.

Evaluation of Φ_{gb}

Having specified the location of each GB in the device channel, we can evaluate the electrostatic potential contributed by GBs (Φ_{gb}). Different from Φ, Φ_s, and Φ_d, Φ_{gb} is calculated using Coulomb's Law. By applying the method of images in which mirror charges are symmetrically added in the gate side (as illustrated in Fig. 2.3), the sum of the potential contribution of each charge trap to the evaluated point can be obtained [32]- [33]:

$$\Phi_{gb}(x,y,z) = \sum_{i=1}^{N} \left(\Phi_i(x,y,z) + \Phi_i'(x,y,z)\right) \tag{2.13}$$

$$\Phi_i(x,y,z) = \frac{-qD_{tr}}{4\pi\varepsilon_{si}R_i(x,y,z)} \tag{2.14}$$

$$\Phi_i'(x,y,z) = \frac{qD_{tr}}{4\pi\varepsilon_{si}R_i'(x,y,z)} \tag{2.15}$$

where R_i is the distance of the charge trap in the GB to the evaluated point, R_i' is the distance between the image charge trap and the evaluated point, and D_{tr} is

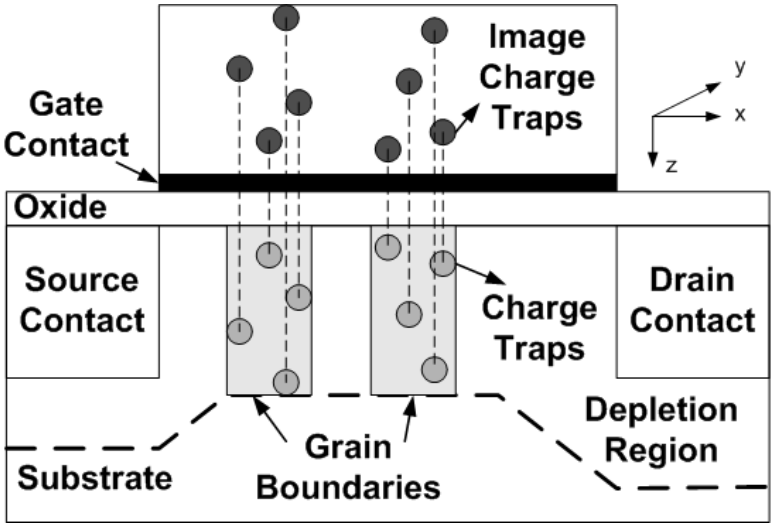


Fig. 2.3. Vertical cross section of TFT illustrating real and image charge traps in randomly distributed GBs.

the density of the charge trap. The assumption of δ-function energy distribution for trap in GB is applied because of its efficiency and simplicity in addressing the essential features of poly-Si films [34]. However, it should be noted that other energy distributions for trap, such as exponential and Gaussian distribution [35]- [38], can easily be applied in the proposed framework. Fig. 2.4b shows the evaluated Φ_{gb} with the specific placement of GBs (Fig. 2.4a). One can observe that the higher value of potential barrier in the intersection of two GBs which reflects the higher charge trap density of the crossing point.

2.2.4 Modeling Surface Potential

Having determined the electrostatic potential induced by the applied voltages and the charge traps in GBs, we are now able to evaluate the surface potential. By applying superposition principle, the surface potential (Ψ) can be expressed as:

$$\Psi(x, y) = U(x, y, 0) + \Phi_{gb}(x, y, 0) \tag{2.16}$$

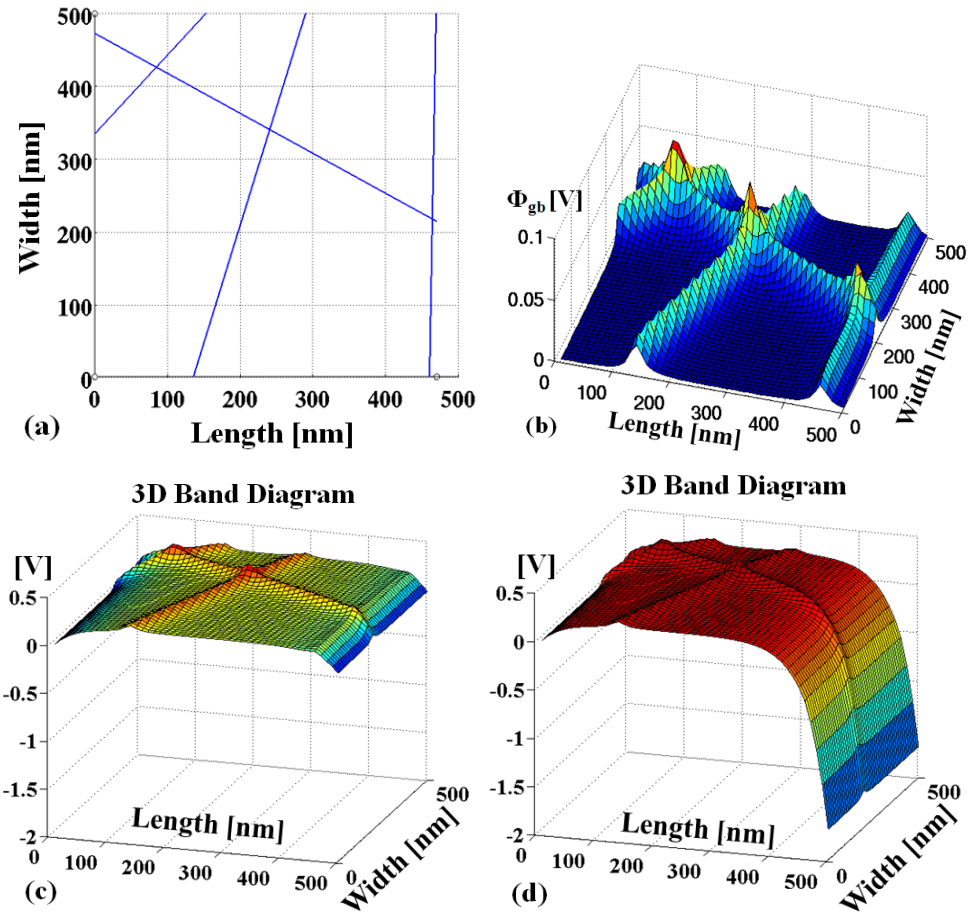


Fig. 2.4. (a) Vectors in random location and direction indicating the random orientation of four GBs in the TFT channel (W=L=0.5μm), (b) surface potential due to charged traps in the GBs (Φ_{gb}) evaluated by Coulomb's law. 3-D Band diagram evaluated using the proposed model for (c) low V_{ds} and (d) high V_{ds}.

The evaluated band diagram with low and high V_{ds} are shown in Fig. 2.4c and 2.4d, respectively. It can be observed that, for high V_{ds}, the potential barrier induced by GB_4, which is located close to the drain contact, is nullified by the lateral drain-source electric field. As a result, the contribution of GB_4 is negligible with regard to threshold voltage determination with high V_{ds}, which also verifies the position dependence of GB effect in our proposed model.

2.2.5 Modeling Threshold Voltage

After obtaining the surface potential of a TFT (Fig. 2.4), the transistor threshold voltage can be determined. To define threshold voltage, the channel is divided into parallel "lanes" where the electrons move from source to drain contact laterally. Note that, if the current along the width direction becomes comparable to the current along the length direction (can occur if the device sizes are aggressive scaled), then the assumption that the current in each channel maintains the same direction from source to drain has to be corrected [39]. With such 1-D channel model (Gate slicing method [39]- [42]), the local threshold voltage (V_t) is determined by the maximum surface potential across the "lane".

$$V_t(y) = \max_{x=(0...L)} \left(\Psi(x,y) + \frac{\sqrt{2\varepsilon_{si} q N_a \Psi(x,y)}}{C_{ox}} \right) \tag{2.17}$$

Finally, threshold voltage is defined as the average of all the local threshold voltage and can be described mathematically by the following equation:

$$V_{th} = \frac{1}{W} \int_0^W V_t(y) dy \tag{2.18}$$

This process is repeated for all the samples (Monte Carlo analysis) which have different number and location of GBs in the channel region. Thus, the distribution of threshold voltage in ploy-Si TFTs is acquired.

2.3 Simulation Results & Discussions

In this subsection, we first demonstrate the efficacy of the proposed framework with 3-D drift-diffusion device simulator [15] and experimental data [12]. The comparison with the previous statistical model [12] is also shown. Then, the discussions for simulated statistical results under various conditions are presented.

In Fig. 2.5 the conduction band diagrams (with one GB located close to the drain) obtained by our model and 3-D drift-diffusion simulator [15] are compared. It

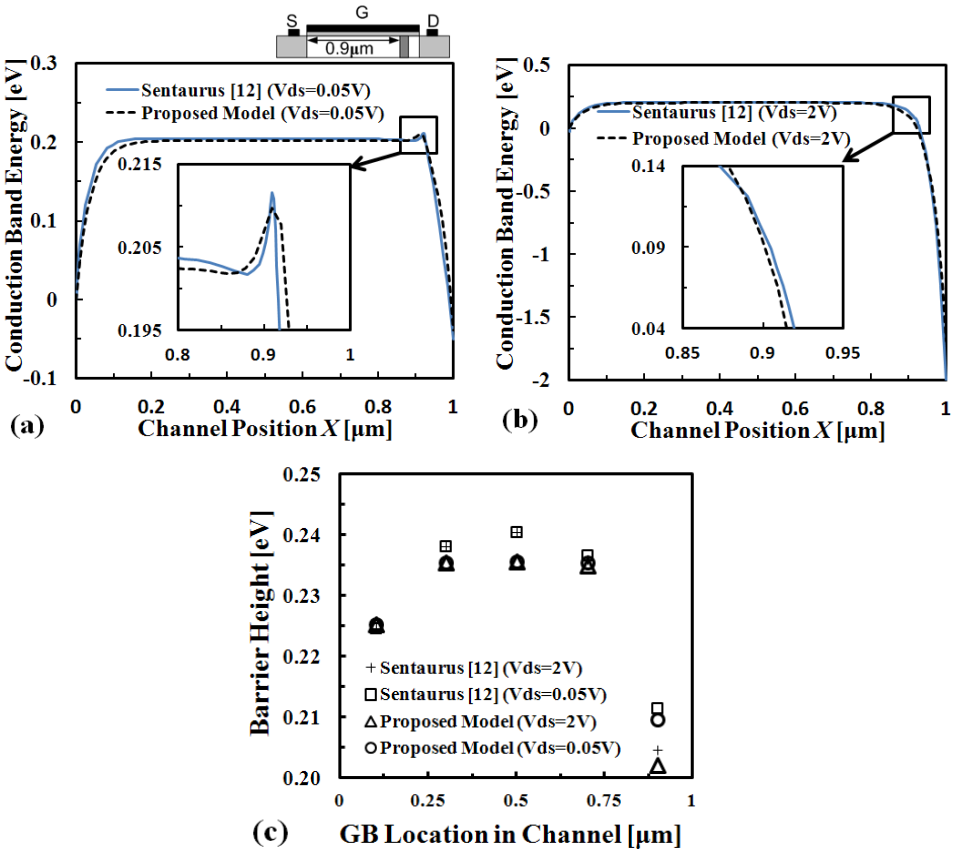


Fig. 2.5. Comparison of conduction band obtained from the proposed model and 3-D device simulator [15] for (a) low V_{ds} and (b) high V_{ds} with a GB 0.9μm from the source. (W=L=1μm) (c) Comparison of maximum barrier height from the proposed model and 3-D device simulator [15] for various V_{ds} and locations of a GB.

is evident that, as shown in Fig. 2.5a and 2.5b, the band diagram from the proposed model agrees well with that of a 3D device simulator under different V_{ds}. Furthermore, as depicted in Fig. 2.5c, the location dependence of barrier height is evident in both models; the lower barrier height can be observed when the GB is close to the source or drain side while the barrier heights are higher and have relatively the same value as the GB's move closer to the center of the channel. In addition, to demonstrate the applicability of the proposed model, we compared the conduction band diagrams for a wide range of technology nodes, sweeping the gate length from 250nm to 1μm. It

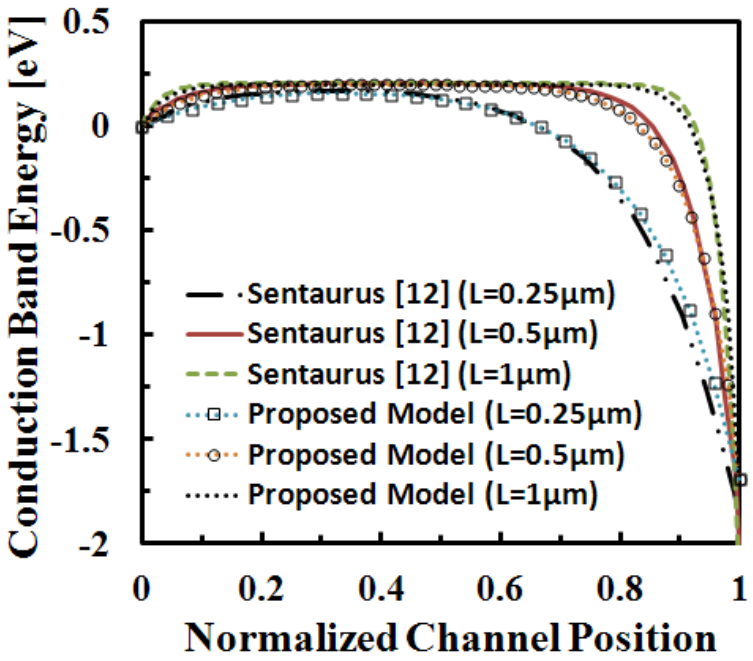


Fig. 2.6. Comparison of conduction band obtained from the proposed model and 3-D device simulator [15] with different device length L.

is evident that the proposed model can be applied for both long and short channel devices, as shown in Fig. 2.6.

In Fig. 2.7, we show our statistical analysis in comparison with the analysis by previous works [12] and experimental data [12]. It is evident that the distribution and standard deviation of V_{th} from the proposed model follow the trend of experimental data closely for different device lengths with the same parameters (as shown in Fig. 2.7a). On the other hand, in Fig. 2.7b, the results obtained by the previous work show significantly smaller standard deviation in both large and scaled TFTs. This is attributed to the fact that the position dependence of GB-induced variation is not included in the previous model.

In addition, due to the large number of transistors in modern circuits, the knowledge of third order moment of the threshold voltage distribution is needed. Using the proposed model with statistical ensembles of 4500 TFTs, the real shape of threshold voltage distribution is observed. In Fig. 2.8, the results show that the GB-induced

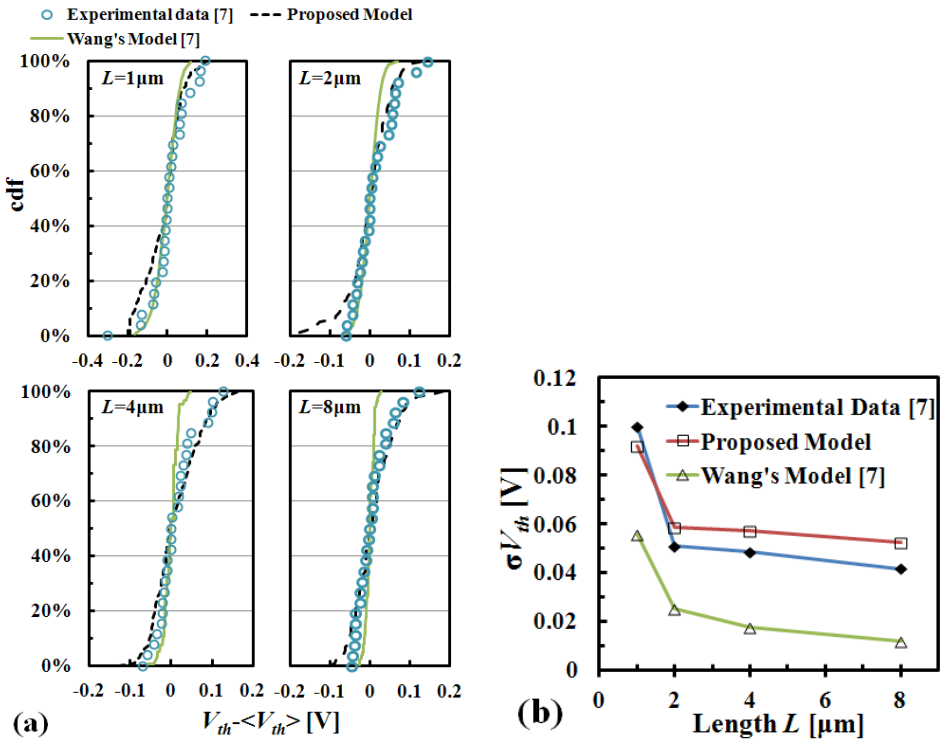


Fig. 2.7. Comparison of (a) cumulative distribution function and (b) standard deviation of V_{th} obtained from the proposed model, experimental data [12] and Wang's model [12] with various device length L. (t_{ox}=30nm, W=8μm, mean L_g=0.4μm, V_{ds}=2V)

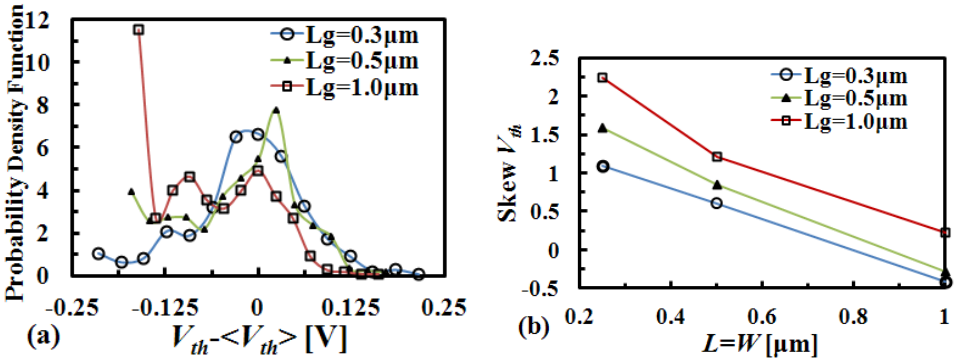


Fig. 2.8. (a) Comparison of threshold voltage distributions with different grain sizes using the proposed model. (L=W=1μm) (b) Comparison of skew of threshold voltage with different grain sizes and device sizes for a sample set of 4500 TFTs using the proposed model.

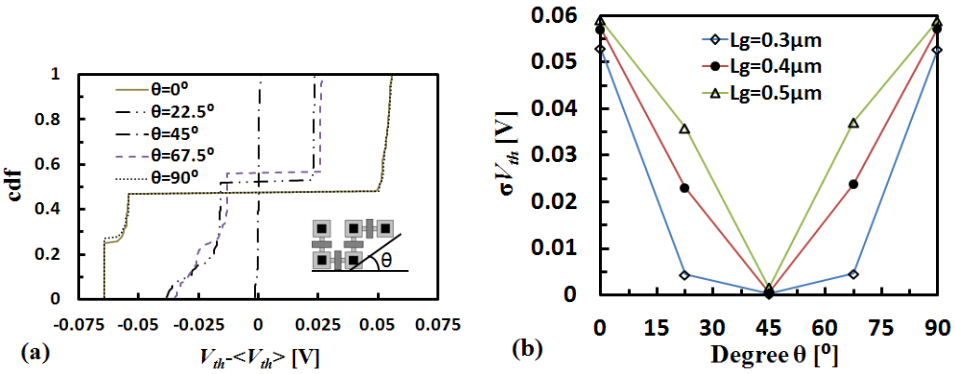


Fig. 2.9. Comparison of (a) cumulative distribution and (b) standard deviation of V_{th} with different angle of periodic GBs and grain sizes using the proposed model.

threshold voltage distribution is positively skewed with increasing asymmetry as the grain size increases. The same situation occurs when the device size shrinks as shown in Fig. 2.8b. This analysis leads to the conclusion that the assumption of Gaussian distribution of threshold voltage may not be valid as we further scale the device size or enlarge the grain size.

The above simulation results (Fig. 2.8) indicate that the threshold voltage distributions are non-Gaussian when the device and grain size are comparable. For solving this issue, considerable research has been carried out for non-random grain growth [43]- [46], such as sequential lateral solidification (SLS) [43], μ-Czochralski method [44], optical phase shift mask [45], and excimer laser irradiation with a-Si spacers [46]. Although these novel crystallization techniques are expected to suppress the device variation due to the spread in the number of GBs, the variation induced by different position and orientation of GBs cannot be avoided. As a result, it is crucial to predict the effect of the position and the orientation of the non-random GBs on device variation for ensuring the robust and stable functionality of poly-Si TFT circuitry. Due to the flexibility of proposed methodology, the effect of non-random GBs to V_{th} variation can be predicted by simply using periodic vectors for modeling the placement of GBs. Fig. 2.9 shows the cumulative distribution function (cdf) and

standard deviation of V_{th} for different orientation (θ) and grain sizes of periodic GBs induced by SLS process. It is evident that V_{th} variation has minimal value when θ=45°, which agrees with the experimental results observed by the authors in [43].

2.4 Conclusions

An efficient physical model for GB-induced threshold voltage variations in poly-Si TFTs has been developed by simultaneously considering the impact of the number, the position and the orientation of GBs. We verified the proposed model with 3-D drift-diffusion device simulator and experimental data and showed the effectiveness of the proposed model for different technology nodes and supply voltages. Using the proposed model, we have shown that, when the device size is comparable to the size of grain, the spread of threshold voltage increases significantly and the distribution is not Gaussian. These statistical attributes pose an intrinsic barrier to further scaling of the supply voltage and channel length. Furthermore, we have shown that the proposed simulation framework is flexible and can predict the effect of GBs for different crystallization process. The fast computation time of the proposed model makes it suitable for evaluation of GB-induced transistor V_{th} variation in the early design phase.

3. A SELF-CONSISTENT ELECTRO-THERMAL MODEL FOR ANALYZING NBTI EFFECT IN P-TYPE POLY-SI THIN-FILM TRANSISTORS

The electrical performance of low-temperature poly silicon (LTPS) thin-film transistor (TFT) has improved considerably in the last decade, due to the flourishing AMLCD (active-matrix liquid crystal display) industry. However, there is a need to further scale down LTPS TFT devices on flexible substrates to explore other application domains. In order to realize this goal, self-heating induced negative bias temperature instability (NBTI) in LTPS TFTs needs to be modeled to determine its effect on transistor degradation and to develop mitigation techniques. Although the characteristics of NBTI for TFTs are widely known, the effects of device geometry and substrate on temperature-dependent NBTI have not been considered. In this section, for the first time, a self-consistent electro-thermal model that considers the effects of device geometry, substrate, and stress conditions on NBTI is proposed. With the proposed modeling methodology, we show the significant impact of device geometry, substrate, and supply voltage on NBTI in LTPS TFTs.

3.1 Introduction

It is obvious that, to facilitate LTPS TFT technology for new applications, further device scaling and integration of robust LTPS TFTs on flexible substrates are required [47]- [51]. Although several techniques have been explored for device scaling and fabrication processes allowing integration of LTPS TFTs directly on flexible substrates, degradation of LTPS TFTs due to self-heating induced NBTI [52] and ambient light [53] remains a critical issue. One of the most crucial reliability issues related to device scaling and flexible substrates is attributed to NBTI [54]- [57]. Experimen-

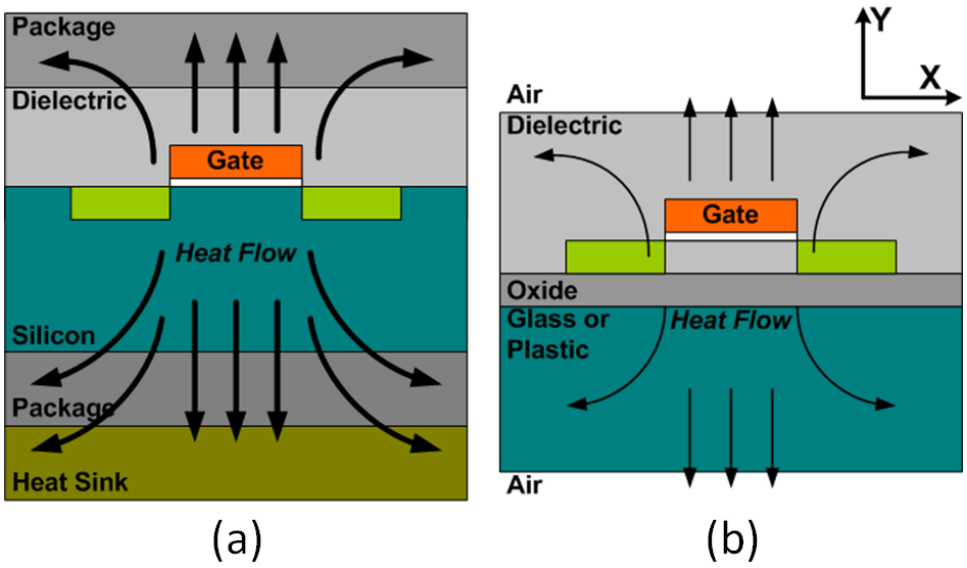


Fig. 3.1. Schematic of heat flow, denoted by arrows in (a) conventional bulk CMOS and (b) TFT technology.

tal data for TFTs has shown that the NBTI-induced degradation is triggered by the combined effect of high channel temperature and electric field [54]- [57]. Hence, as dimensions of TFTs are reduced to the submicron regime, the NBTI effect is expected to be more pronounced due to self-heating because of the increased power density. Furthermore, the flexible substrates, which usually have lower heat conductance (e.g. the heat conductance of plastic is about two orders of magnitude lower than that of silicon), aggravate the heat dissipation from the device, and therefore, the transistors show worse NBTI-induced transistor degradation. As shown in Fig. 3.1(a), the heat generated from the device on silicon substrate can be easily spread and dissipated due to the excellent heat conductivity of the silicon substrate and the presence of heat sink. Conversely, the heat generated by an LTPS TFT, as shown in Fig. 3.1(b), is hard to exchange or diffuse through the substrate due to poor heat conductivity of the substrate and the absence of heat sink. Consequently, the temperature of LTPS TFTs on flexible substrate is expected to be higher, more localized, and sensitive to device geometry, as verified by experiments [8], [9]- [11]. Therefore, to ensure robust

and stable functionality for future LTPS TFT-based circuits, it is essential to properly model and mitigate the effects of self-heating induced NBTI.

In this section, we develop a self-consistent electro-thermal model which helps in accurately modeling NBTI degradation in LTPS TFTs [16]. The impact of different substrate material and thickness, device geometry, and stress conditions on NBTI are incorporated in this model by integrating a 2D thermal-diffusion model and an empirical NBTI model [58]. Using the proposed framework, we investigate the impact of: (a) device geometry, (b) substrate, and (c) supply voltage on NBTI induced transistor degradation.

The rest of the work is organized as follows. The proposed self-consistent electro-thermal model is described in subsection II. Subsection III introduces and validates the 2D thermal-diffusion model for LTPS TFTs with experimental data. Subsection IV briefly describes the empirical NBTI model which is used in this work for estimating the threshold voltage degradation in LTPS TFT due to NBTI. This model has been fitted to experimental data. The simulation results for different device geometries and substrate followed by optimization techniques to mitigate the impact of NBTI-induced degradation in circuits are presented and discussed in subsection V. Finally, in subsection VI we draw the conclusions.

3.2 The Framework for Modeling LTPS TFTs

In the proposed framework, the electrical characteristics of LTPS TFT (e.g. threshold voltage (V_{th}), drain current (I_{DS}) and oxide electric field (E_{ox})) are captured by a device level LTPS TFT model (for this study we used Taurus device simulator [59]). Further, the effects of TFT geometry, material parameters, and stress conditions on device temperature are determined by a 2D thermal model. Finally, the threshold voltage shift with respect to time due to NBTI is predicted using an empirical power-law model for LTPS-TFT devices [58].

Fig. 3.2 shows the flowchart of the proposed self-consistent electro-thermal NBTI modeling methodology. In the first step, the 2D geometry of the transistor and the supply voltage are set. In step 2, the corresponding current and the oxide electric field are extracted from LTPS TFT device model in order to be used by both 2D thermal-diffusion and NBTI models. In step 3, the 2D thermal-diffusion model evaluates channel temperature for the given stress conditions, device geometry, and the initial current obtained from LTPS TFT device model. Having the obtained channel temperature and the electric field from LTPS TFT device model, in step 4, the threshold voltage is calculated using the NBTI model which has been fitted to experimental data. In step 5, the degradation of LTPS TFT is evaluated based on the calculated V_{th}. The new I_{DS} (due to new V_{th}) is provided as feedback to thermal-diffusion model in order to determine the new temperature. This new temperature results in a new threshold voltage due to degradation (NBTI) which is used in the next iteration. This process is repeated until convergence is achieved. After convergence, time-dependent V_{th} is obtained, which can be used by circuit simulator (e.g. HSPICE [60]) to predict the degradation and lifetime of any LTPS TFT-based circuit. Let us now describe in detail the framework presented in Fig. 3.2 starting with the thermal model.

3.3 Thermal-Diffusion Model

As we described in subsection II, in order to predict the temperature distribution across the TFT device during voltage bias stress, a 2D thermal-diffusion model can be used, described by the following partial differential equation:

$$\rho C \frac{\partial T(x,y)}{\partial t} - \nabla[k \nabla T(x,y)] = H \tag{3.1}$$

where ρ is the mass density, C is the heat capacity of the material, $T(x,y)$ is the position dependent temperature, k is the heat conductivity of material, x is position in the width direction, y is the position in the thickness direction and H is the heat source. Note that, in this 2-D thermal-diffusion model, device length is neglected since

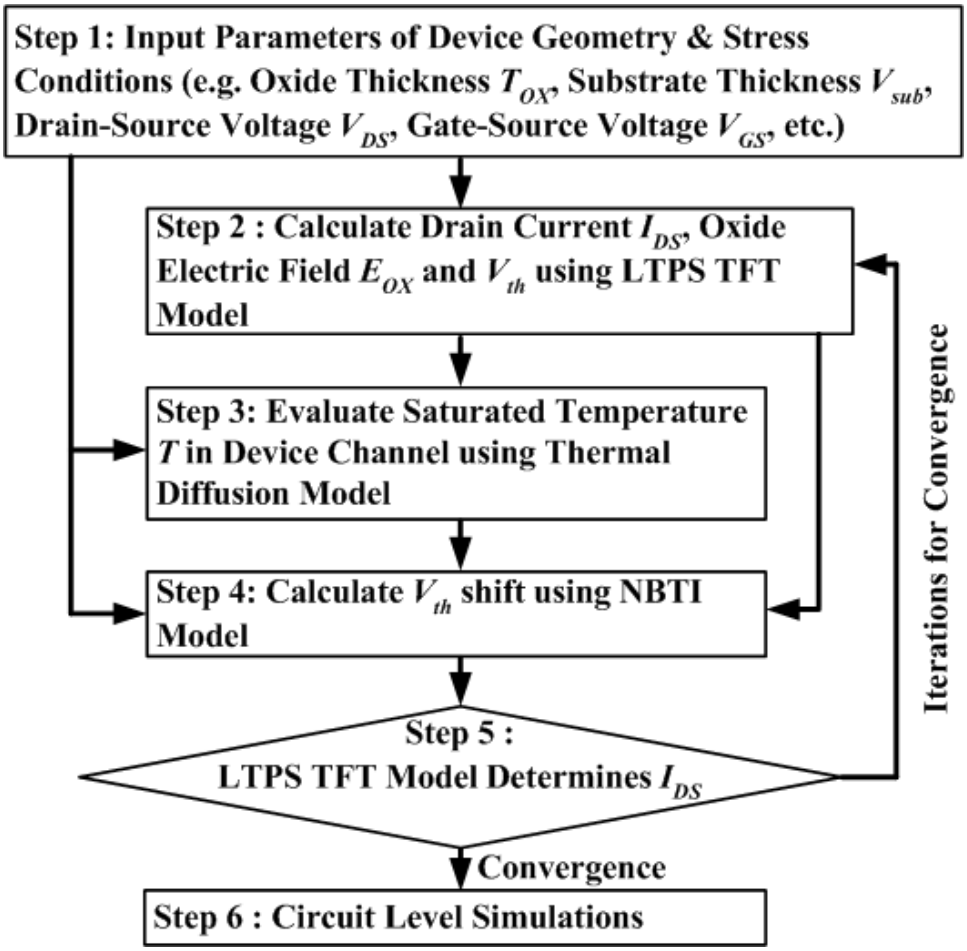


Fig. 3.2. Flowchart of the proposed self-consistent electro-thermal modeling methodology.

device width is normally the parameter which can be controlled by circuit designers, and hence, play a significant role in determining channel temperature. The heat source is calculated as the product of the applied drain-source voltage (V_{DS}) and the drain current (I_{DS}), and hence, $H = V_{DS} \cdot I_{DS}$. H represents the Joule heating generated by the channel of the device. We assume that the effect of self-heating mainly originates from it [61]. Indeed, other heat sources, such as lattice heating, are neglected since their contribution is comparatively small [61]. The 2D thermal-diffusion equation (Eq. (3.1)) is solved numerically after appropriate discretization in space and time using Finite Element Analysis (FEA).

Table 3.1.
Material Parameters for Thermal Analysis

	Density ρ $(kg \cdot m^{-3})$	Heat Capacity C $(J \cdot kg^{-1} \cdot K^{-1})$	Heat Conductiveity k $(W \cdot m^{-1} \cdot K^{-1})$
Poly Silicon	2330	716	45
Aluminum	2707	896	250
SiO_2	2200	1000	1.3
Glass	2540	707	0.91
Polyimide	1430	1150	0.52
Copper	8960	390	400

To obtain a unique solution from Eq. (3.1) the appropriate initial and boundary conditions should be set up. In the proposed model, Neumann boundary conditions are used in the top and the bottom boundaries for the heat exchange between the TFT devices and its surrounding environment. These conditions can be expressed mathematically as [62]:

$$uk\nabla T(x,y) = G - h\Delta T \tag{3.2}$$

where u is the outward unit length vector normal to the device boundaries, h is the heat transfer coefficient, G is the heat flux and ΔT is the temperature difference between the two sides of each boundary. The heat transfer coefficient of the air adjacent to the top and bottom boundaries is $50\mathrm{Wm}^{-1}\mathrm{K}^{-1}$. The ambient temperature for the left and the right of the simulation domain is held at 27^oC. The material parameters used in our thermal-diffusion model are summarized in Table 3.1. Note that, for simplicity, temperature dependence of the material properties is not included in our analysis.

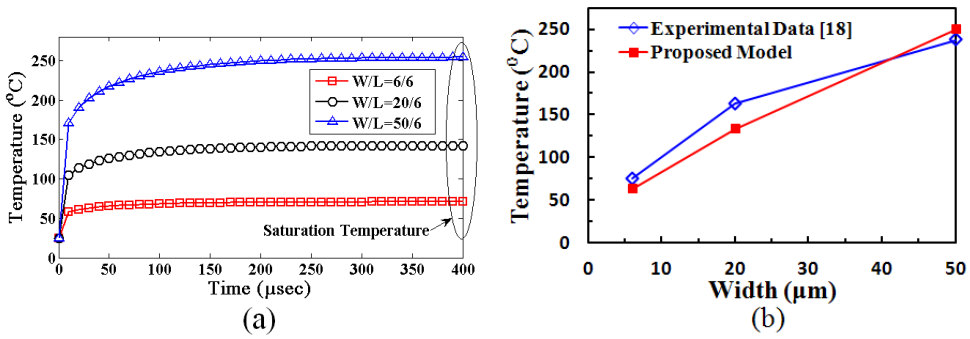


Fig. 3.3. (a) Transient temperature of device channel with three different device widths. Under the same stress condition (V_g=V_d=−15V), the channel temperature increases as the device width increases and saturates within microseconds. (b) Comparison of simulated channel temperature and experimental data [11] with different device width.

To benchmark and validate the efficacy of the proposed 2D thermal-diffusion model, we perform simulations for three different device widths: $W = 6\mu$m, 20μm and 50μm. The stress conditions and the thickness of each layer of TFTs are adjusted according to the actual value used in the experiments in [11]. As shown in Fig. 3.3, the temperature in the device channel region is in good agreement with the measured experimental data in [11]. In addition, the strong temperature dependence on the channel width can be readily observed when the power density is kept the same. This is because, the heat generated in the center of the device channel is difficult to dissipate as the width of the device increases and hence, results in higher temperatures.

3.4 NBTI Model for TFTs

Negative bias temperature instability (NBTI) is the phenomenon where transistor characteristics degrade when they are stressed under negative gate voltage and/or elevated temperatures. Although, NBTI in bulk silicon technology has been widely studied for years, the physical origin is still under debate due to the different char-

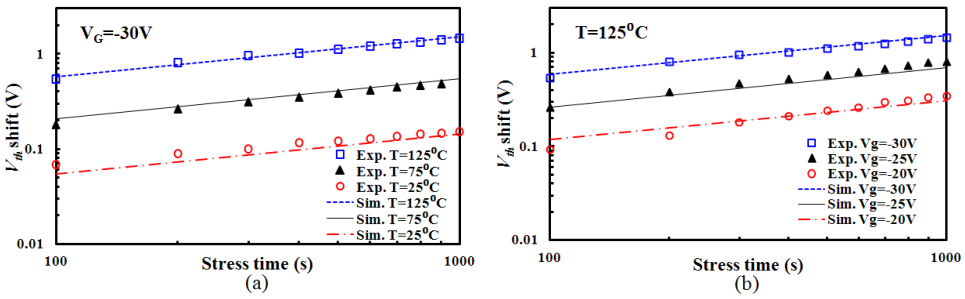


Fig. 3.4. Experimental [71] and simulated time evolution of threshold voltage shift for various temperature (a) and supply voltage (b). The used parameters are $n = 0.42$, $E_a = 0.404$eV and $K_{ox} = 3.84$ x 10^{10}.

acteristics reported by different research groups using their respective measurement techniques and devices [63]- [68]. On the other hand, though NBTI mechanism in LTPS TFTs is found to be similar to that of bulk silicon technology, the existence of grain boundaries (GBs) makes NBTI modeling more complicated [69]- [70]. Instead of using physical models such as drift-diffusion model, in this work we use an empirical NBTI model for LTPS TFT for evaluating threshold voltage degradation as we discussed in subsection II. However, it should be noted that the empirical model is used only as an instructive example for modeling the effect of NBTI on TFT devices; that is, if more accurate NBTI models are proposed in future, the same framework is still valid and can be used. Thus, the threshold voltage shift in LTPS TFT, experimentally found to be associated with temperature, electric field and time, can be empirically expressed as [58]:

$$\Delta V_{th} \propto t^n \cdot \exp(-\frac{E_a}{kT}) \cdot \exp(\frac{K_{ox}E_{ox}}{kT}) \tag{3.3}$$

where n is the time exponent, E_a is the activation energy, E_{ox} is oxide electric field and K_{ox} is a technology dependent parameter. The validity of the used parameters for the empirical model is verified by comparison with experimental data [71]. As shown in Fig. 3.4, the threshold voltage shift under different stress conditions agrees with the measured experimental data [71].

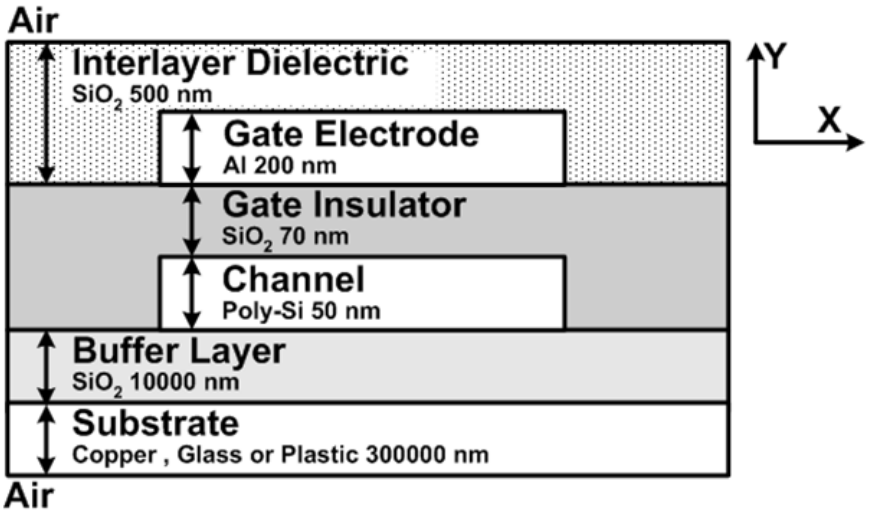


Fig. 3.5. Cross-sectional view of the simulated LTPS TFT. (X: width direction, Y: thickness direction)

3.5 Simulation Results & Discussions

In this subsection, we extensively investigate the impact of: (a) device geometry, (b) substract, and (c) supply voltage on NBTI-induced degradation in LTPS TFTs using the proposed self-consistent electro-thermal model. Note that, the parameters used in the proposed framework have been fitted to the experimental data as shown in the previous subsections.

The cross-sectional view of the simulated LTPS TFT device is illustrated in Fig. 3.5. The gate oxide thickness of this device is 70nm, the poly silicon thickness is 50nm, the back oxide thickness is 10μm, and the substrate thickness is 300μm. For simplicity, LTPS TFTs with fixed grain size (200nm for our experiments) and only latitudinal GBs are assumed. We apply DC stress conditions of -15V to evaluate the worst-case degradation for a given device, unless it is specifically mentioned. The threshold voltage degradation after 10^4sec is used for comparison in this study. The material parameters used by the thermal-diffusion model are listed in Table 3.1 . For simplicity, the channel temperature is assumed to be uniform due to the small temperature difference in the channel as compared to the temperature difference

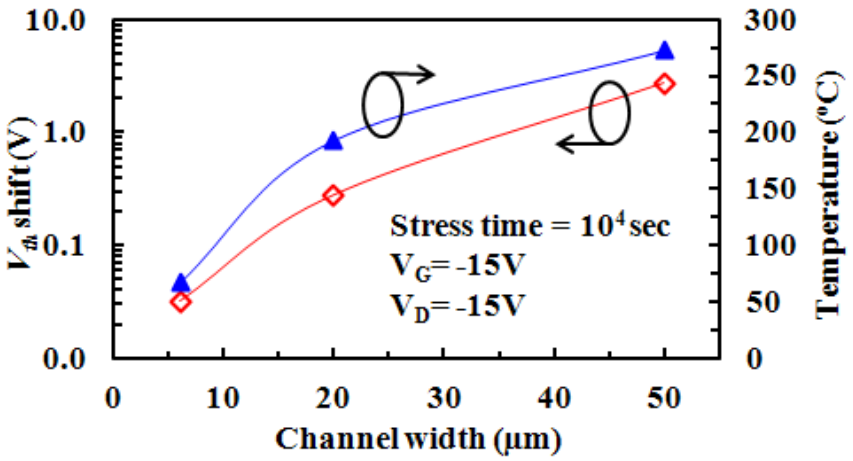


Fig. 3.6. Temperature and threshold voltage shift as a function of channel width. The dependence of channel temperature on channel width affects overall threshold voltage shift and must be taken into account for proper estimation of the lifetime of TFT-based circuits.

caused by other factors (e.g. device width, substrate material) [72]- [73]. In addition, for the NBTI model we keep the temperature constant. This assumption is reasonable because the device channel reaches a steady state temperature within microseconds, which is short enough compared to NBTI induced transistor degradation.

In Fig. 3.6, we demonstrate the temperature dependence on device width. Specifically, we observe that the temperature reaches higher levels when the width is larger because the heat in the center of the channel is more difficult to diffuse. Moreover, it is also observed that devices with larger width result in larger V_{th}-shift as shown in Fig. 3.6. The substantial difference of V_{th}-shift indicates that a significant error in lifetime evaluation would occur if the effect of device width on NBTI is neglected in our simulations. Hence , the significant degradation dependence on temperature (due to device width) emphasizes the need to include the thermal model for evaluating effect of NBTI on LTPS TFTs. Based on the above observations, the maximum device width for a LTPS TFT-based circuit should be carefully decided. In addition, multi-finger structures (set of transistors connecting in parallel), which are usually

used to reduce the effects of parametric variations (due to GBs) in LTPS TFTs [74], can also be used to suppress aging effects and increase circuit lifetime.

The impact of different substrates in TFTs is also included in our study. Although TFTs have been successfully fabricated on several substrates, it is widely known that the lifetime has a strong dependence on substrate material [9], [49]. Therefore, it is necessary to know the effect of substrate material on the self-heating induced NBTI degradation. The channel temperatures for three different substrates (polyimide, glass and copper foil) with various substrate thicknesses are compared in Fig. 3.7(a). It is evident that the channel temperature increases as the substrate thickness decreases. This can be attributed to the fact that, as substrate thickness reduces, the surrounding area that participates in cooling of device channel also reduces. Furthermore, it can be observed that for the same substrate thickness (i.e. 50 μm), the temperature of a TFT with polyimide substrate can be 220^{o}C while a TFT with copper substrate can be as low as 60^{o}C. Note the strong dependence of channel temperature to the substrate material is mainly attributed to large heat conductivity difference between polyimide and copper. To further understand this phenomenon, we plot the temperature distributions for different substrates. Under same stress and boundary conditions, the temperature gradient inside a polyimide substrate is notably gentler compared to a copper foil substrate, as shown in Figs. 3.7(c) and 3.7(d). For such a case, it is apparent that the copper foil substrate acts as a cooling source for devices since the generated heat can be easily transferred and dissipated throughout the whole die. Conversely, the heat generated in a TFT grown on plastic substrate is more difficult to diffuse, and hence, results in more localized and higher device temperature. Accordingly, the threshold voltage degradation in a TFT on a plastic substrate is relatively severe compared to TFTs on glass and copper foil substrates, as verified in Fig. 3.7(b).

In Fig. 3.8, we investigate the effect of device scaling on TFT devices. Specifically, we compare the channel temperature and threshold voltage degradation (V_{th}-shift) for different technology nodes under the same stress conditions. Interestingly, we observe

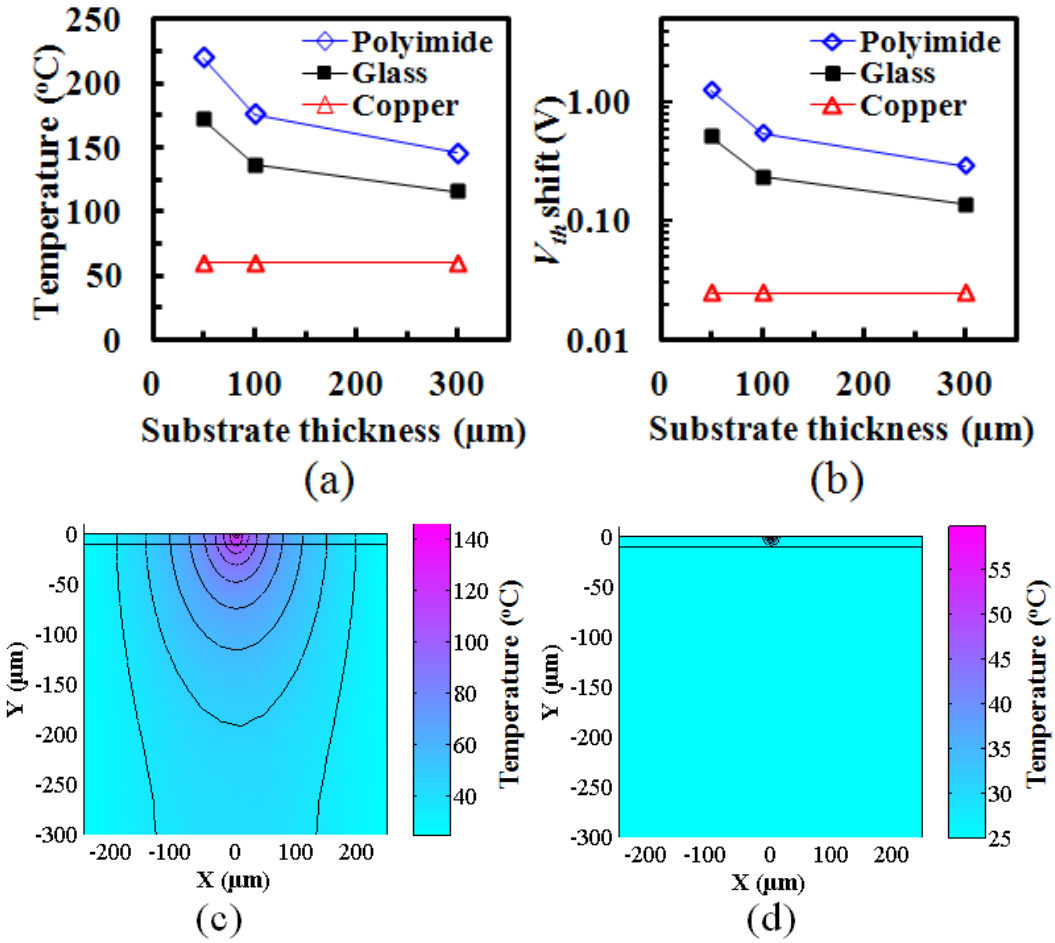


Fig. 3.7. Substrate material and thickness dependence of (a) channel temperature and (b) threshold voltage degradation of TFT with W/L=6μm/6μm under a dc bias stress (V_G=V_D=−15V, stress time=10^4s). Spatial distribution of temperature in an LTPS TFT on (c) polyimide and (d) copper substrate with thickness of 300 μm. (X: width direction, Y: thickness direction)

higher temperature for devices at scaled technology nodes because of larger power density in the channel. This effect is illustrated in Fig. 3.8(a). In addition, large threshold voltage shift at 1.5μm technology node, as revealed in Fig. 3.8(b), confirms that severe degradation in small device length can be one of the main obstacles in scaling. In light of the above simulation results (Fig. 3.6 and Fig. 3.8), one large sized device would not be preferable and should be replaced by parallel but smaller devices

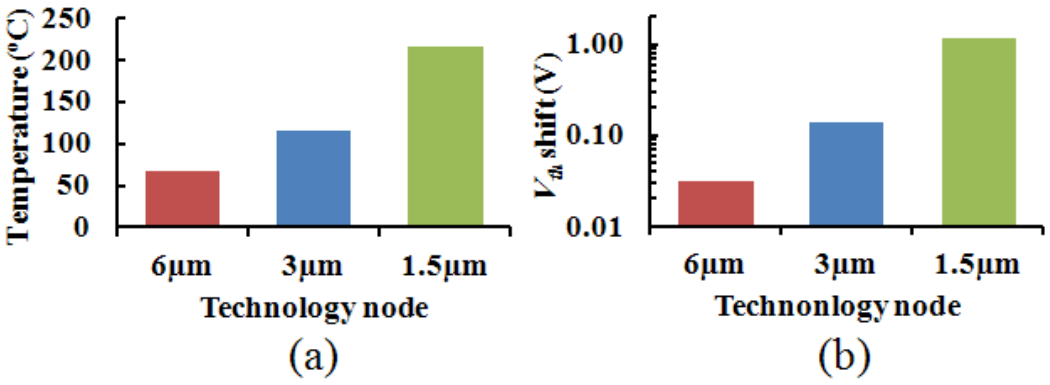


Fig. 3.8. Technology dependence of (a) temperature and (b) threshold voltage degradation of TFT with W/L=1 under a DC bias stress (V_G=V_D=−15V, stress time=10^4s).

(i.e. Multi-finger structure) as we move to smaller technology nodes. Additionally, instead of using the minimum channel length for all TFTs in a circuit, we can choose longer devices for critical transistors (i.e. transistors which have to drive large loads or have to be operated under high duty cycle).

The supply voltage is an important parameter for LTPS-TFT based circuits because it is normally increased to suppress threshold voltage and mobility variations due to GBs [22]. However, increased supply voltage worsens NBTI degradation in terms of temperature and electric field. Hence, supply voltage is one of the most important factors to determine the NBTI-induced degradation. However, previous research does not simultaneously consider the above two factors [70]- [73]. Using the proposed model (which takes into account the effect of supply voltage on both electric field and channel temperature of TFTs), we investigate the effect of supply voltage on device degradation with three different supply voltages (−12V, −15V and −18V). As shown in Fig. 3.9(a), when the supply voltage is increased, a substantial rise in the temperature is observed due to large heat energy accumulation. It is obvious that this phenomenon becomes even more significant as we move to scaled technologies. Fig. 3.9(b) demonstrates that the degradation would be largely underestimated if we

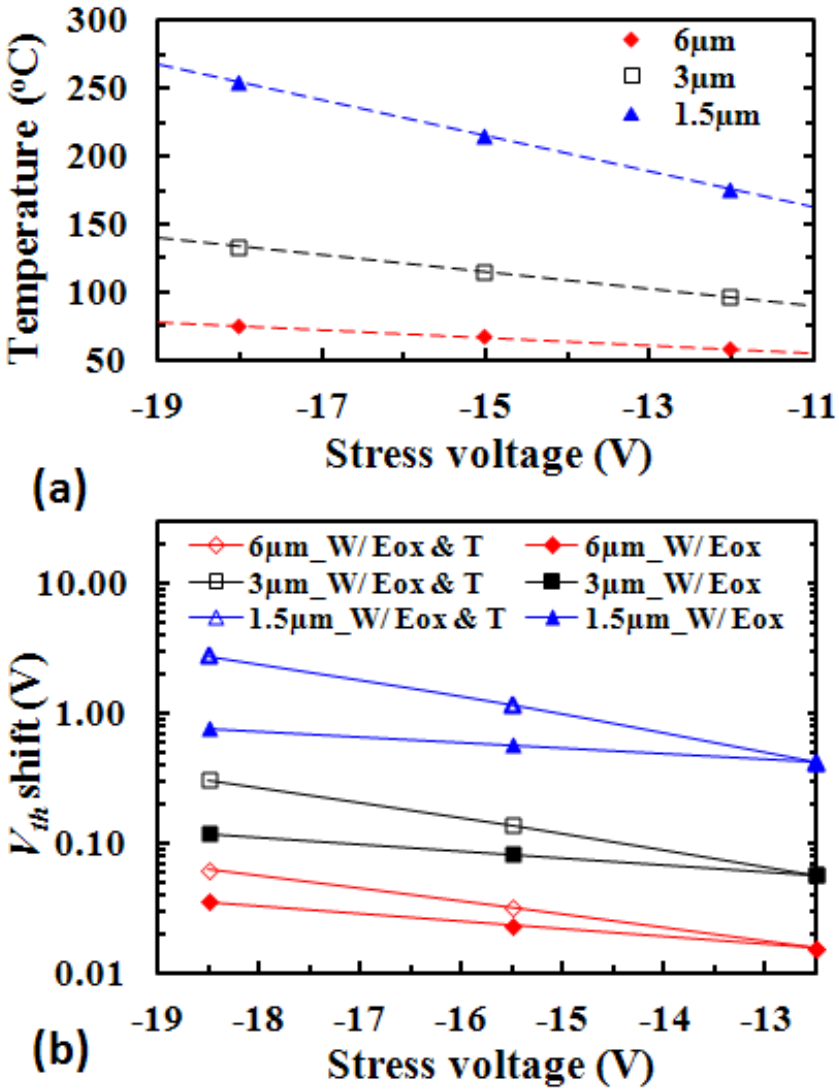


Fig. 3.9. (a) Stress voltage dependence of the temperature in LTPS TFTs (W/L=1) at different technology nodes. (b) Comparison of threshold voltage shift under various stress voltages (i.e. −12V, −15V and −18V) considering the effect of temperature and electric field.

consider only the effect of electric field, clearly showing the need for the self-consistent thermal and NBTI model for prediction of NBTI induced degradation in LTPS TFTs.

The above simulation results demonstrate the sensitivity of NBTI-induced degradation on device geometry and substrate for LTPS TFTs. Hence, though the empirical model and physical NBTI frameworks (e.g. drift-diffusion model or hole trapping

model) are sufficient to model NBTI for conventional CMOS technologies, it is necessary to supplement it with the thermal model in order to evaluate the degradation in LTPS TFTs.

3.6 Conclusions

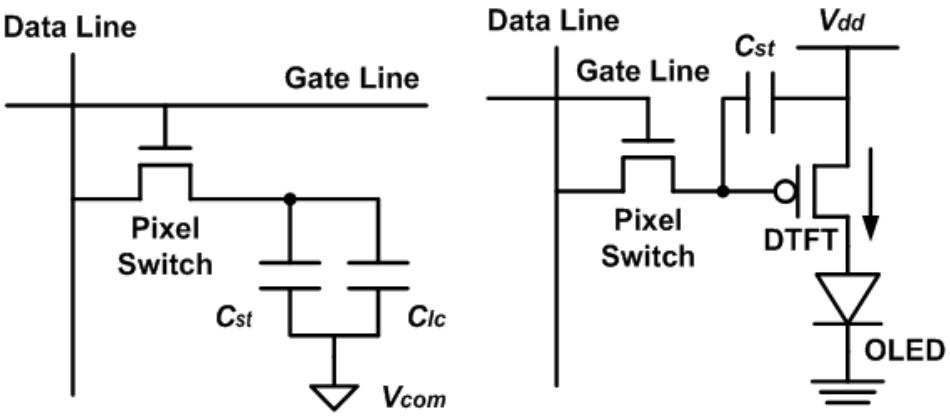
In this section, we have proposed a self-consistent electro-thermal model for evaluating the impact of self-heating induced NBTI in LTPS TFTs. The proposed framework consists of a LTPS TFT device model, NBTI model and 2D thermal-diffusion model. Hence, the proposed model is able to incorporate device degradation and lifetime prediction dependence on substrate and device structure. To show the validity of the proposed framework, we verified that the predicted temperature and threshold voltage shift closely follow experimental data. Based on this framework, we also show the significant impact of device geometry, substrate material and thickness, and supply voltage on NBTI in LTPS TFTs. This study reflects on the main obstacles for future flexible electronics and validates the need for integration of thermal-diffusion model and NBTI model for precisely predicting NBTI induced degradation in LTPS TFTs.

4. AN ENHANCED VOLTAGE PROGRAMMING PIXEL CIRCUIT FOR COMPENSATING GB-INDUCED VARIATIONS IN POLY-SI TFTS FOR AMOLED DISPLAYS

The variation and reliability issues of display backplane pose major challenges for poly silicon (poly-Si) active matrix organic light emitting diode (AMOLED) displays. Adjacent poly-Si thin-film transistors (TFTs) exhibit different threshold voltages and mobilities due to random distribution of grain boundaries (GBs). Furthermore, the threshold voltage and mobility of TFTs have noticeable shift in time because of electrical stress. In this study, we propose an improved voltage programming pixel circuit for compensating the shift of threshold voltage and mobility in driver TFTs (DTFTs) as well as compensating the supply voltage degradation. HSPICE simulation results demonstrate that the drive current for OLED has a deviation of less than $\pm 2\%$ *for a mobility variation of* $\pm 40\%$ *and a maximum deviation of* $30nA$ *when the threshold voltage varies from* $0.3V$ *to* $-0.3V$*. Moreover, if the supply voltage degrades from* $10V$ *to* $8.5V$*, the drive current shift is less than* 15%*.*

4.1 Introduction

AMOLED displays are promising for future display applications, due to their superior properties compared to active matrix liquid crystal display (AMLCD), such as wide viewing angle, light weight, slim form factor and fast response time [75]. However, AMOLED display is limited to small-sized applications due to the high sensitivity of the drive current to process variations and degradations in DTFT of AMOLED pixels [76]- [78]. In AMLCD pixels, the TFTs generally act as switches, as shown in Fig. 4.1(a). Hence, the electrical parameter variations in TFTs can easily be compensated by a large gate voltage. Accordingly, the brightness of each



(a) (b)

Fig. 4.1. Conventional pixel structure of (a) AMLCD and (b) AMOLED display.

pixel can be controlled precisely by the data voltage delivered from the data driver. However, TFTs in AMOLED pixel circuit, as shown in Fig. 4.1(b), are used not only in switching, but also in analog control of OLED currents. Therefore, the variation and degradation of electrical characters in DTFT directly correspond to the luminance shift of OLEDs [76]- [78]. As a result, the electrical parameter variations and degradations in backplane TFTs are the main obstacle for developing AMOLED display.

The most common backplane technologies for AMOLED display are amorphous silicon (a-Si) and poly-Si. Compared to a-Si TFT, poly-Si TFT features higher drive current and better stability against biased stress voltage and allows complementary TFTs [79]- [80]. These properties make poly-Si TFT a better option for driving OLEDs compared to a-Si TFTs. However, the electrical parameter mismatches between neighboring poly-Si TFTs, including mobility and threshold voltage, are inevitable due to randomly oriented and distributed GBs formed during the excimer laser annealing process [81]. Such device variations directly lead to fluctuations in the brightness throughout a panel. In addition, the supply voltage for a specific pixel decreases with the increase in the number of pixels between the supply voltage source

and the target pixel, due to IR drop [18]. The supply voltage degradation impacts the V_{gs} of DTFTs and, thus, the brightness of the displays. Consequently, a proper current stabilization methodology is needed to achieve acceptable image uniformity in AMOLED display.

Various compensation approaches have been investigated for mitigating the electrical parameter variations in DTFT and the shift in supply voltage. Voltage programming methodology (VPM) is one of most common techniques for addressing the non-uniformity associated with AMOLED displays [18]. The idea of this methodology is to store the threshold voltage of DTFT and the corresponding supply voltage in a capacitor for creating an adaptive gate voltage. Although this methodology can effectively eliminate the effect of threshold voltage shift and supply voltage degradation [18], it fails to mitigate the current variation induced by the mobility variation in DTFTs.

Current programming methodology can compensate the threshold voltage, the mobility, and the supply voltage shifts, since the drive current is basically copied from the data current [82]. However, programming time can be large at the low current level, because the pixel capacitance and the parasitic capacitance of the data line need to be charged to the required voltage by a small data current [83]. Consequently, the current programming methodology is only applicable for low resolution and small sized displays.

Feedback-type pixel circuits, such as optical feedback and current feedback, were presented to compensate the threshold voltage and mobility variations, as well as the supply voltage degradation [77], [84]. Current-feedback pixel circuit, although able to properly compensate the device variations, requires complex and elaborate peripheral compensation circuits (voltage and current DACs, high-speed Op-Amp, current sensing and comparator circuits, feedback controller etc.) that increases the difficulty for implementation [84]. Besides, the compensation circuits themselves may also need to be compensated. For optical-feedback circuits, which compensate the variations by the embedded photo-diode, the shift in the drive current is not able to compen-

sate correctly because of the variation and aging of photo-diode [77]. Furthermore, the interference of ambient light and neighboring pixels would also cause incorrect compensation [85].

Among the aforementioned techniques, the short programming time and the exclusion of complex and elaborate peripheral circuits make VPM the most feasible approach for realizing large sized and high resolution AMOLED displays [86]. Although self compensation between threshold voltage and mobility decreases the impact of mobility variation [87], the dependence of drive current to the mobility variation is approximately 10% [19], and hence, may not be acceptable for high performance display applications. To cope with this problem, an improved VPM pixel circuit, which is capable of addressing mobility variation, is proposed and verified in this scetion [20]. This work makes the following contributions:

(1)We present a new VPM pixel circuit, which compensates not only the shift in the threshold voltage and supply voltage but also the mobility variation in DTFTs. The key idea for compensating the mobility variation is to apply an adaptive compensation voltage at the gate of DTFT with the help of an extra capacitor. The adaptive compensation voltage, created out of the drive current, depends on the mobility of DTFT and, hence, can be used as a feedback voltage to mitigate the mobility deviation.

(2)We derive equations for estimating the appropriate design parameters for optimizing the compensation. Furthermore, the relative error of the drive current is also modeled to verify the efficacy of the proposed pixel circuit.

(3)We validate the proposed pixel circuit by HSPICE simulations and Monte Carlo based statistical analysis using the RPI Poly-Si TFT model [60]. The simulation results demonstrate the insensitivity of the proposed pixel to the device variations and supply voltage degradation.

The remainder of this section is organized as follows. Subsection II elaborates on the issues and the limitations of conventional pixel circuit (Fig. 4.1b), and describes the proposed pixel structure. Subsection III derives the appropriate design parame-

ters for the proposed pixel circuit and the relative error for the drive current of the proposed pixel circuit. Various HSPICE and Monte Carlo simulation results that validate our proposed methodology are presented in subsection IV, while subsection V concludes the work.

4.2 Conventional and Proposed Pixel Structure

In this subsection, we first derive the drive current equation for the conventional pixel circuit, as shown in Fig. 4.1(b), so as to illustrate the impact of the electrical parameter variations and the supply voltage degradation to the drive current. In general, DTFTs are operated in the saturation region for better control of drive current. This can be achieved by choosing proper range for the data voltage applied at the gate of DTFTs. The drive current (I_{DTFT}) of the conventional AMOLED pixel circuit thus follows:

$$\begin{aligned} I_{DTFT} &= K\mu_{eff}\left(V_{gs} - V_{th,DTFT}\right)^2 \\ &= K\mu_{eff}\left(V_{data} - V_{dd} - V_{th,DTFT}\right)^2 \end{aligned} \tag{4.1}$$

where K is $(W/2L)C_{ox}$. W and L are the channel width and the length of DTFT, respectively. C_{ox} is the gate insulator capacitor per unit area. μ_{eff} is the effective field-effect mobility. V_{dd} is the supply voltage. V_{data} is the data voltage delivered from data driver while $V_{th,DTFT}$ is the threshold voltage of DTFT. From Eq. 4.1, it can be noted that the threshold voltage, the mobility and the supply voltage variations can directly affect the drive current which in turn causes brightness non-uniformity over the display area.

Fig. 4.2(a) depicts the structure of the proposed circuit. The proposed pixel circuit is composed of seven TFT switches, one DTFT, two capacitors and two control signals. The drive sequence of the proposed pixel circuit can be divided into four phases: (1) reset phase, (2) detection phase, (3) compensation phase, and (4) display phase. Fig. 4.2(b) shows the timing chart for the applied signals, while Fig. 4.2(c)

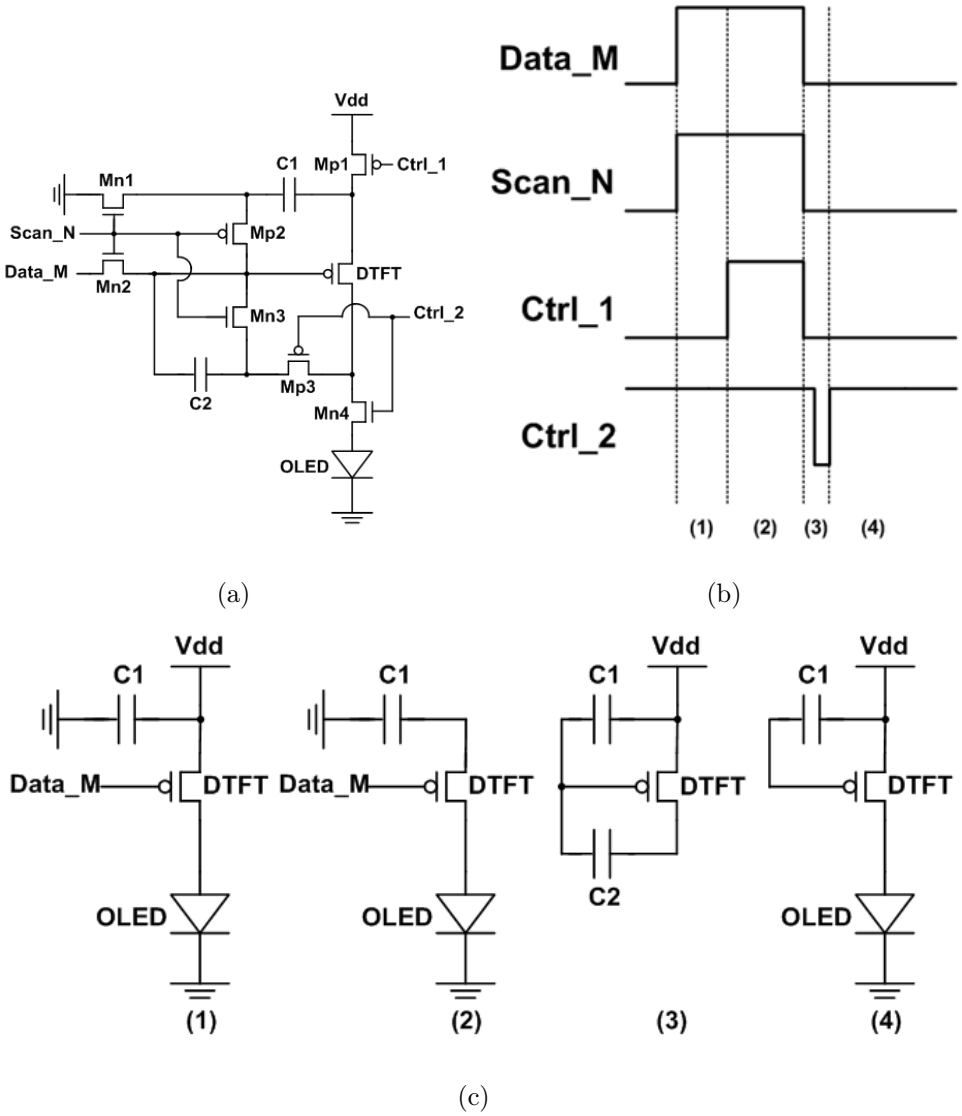


Fig. 4.2. (a) Proposed VPM pixel structure (b) Timing chart for the applied signals (c) Equivalent circuit of the proposed VPM pixel in each phase.

illustrates the equivalent circuit of the proposed pixel in each phase. The detail operating principle for each phase is described as follows.

(1) Reset phase: The main purpose of this phase is to eliminate the influence of the prior frame (i.e., to reset the voltage stored in C1 and C2). In this phase, Scan_N and Ctrl_2 are set to high, while Ctrl_1 is set at a low level. The source and gate

of DTFT are, therefore, precharged to V_{dd} and V_{data} respectively, due to which the voltage stored in C1 and C2 is reset and the influence of prior frame is excluded.

(2) Detection phase: In the second phase, the source voltage of DTFT drops from V_{dd} to V_{data}-$V_{th,DTFT}$ because Mp1 is turned off; meanwhile, the other node of C1 is fixed at ground since Scan_N remains in high. Accordingly, the value of $V_{th,DTFT}$ is detected and stored in C1 for adjusting the gate voltage of DTFT in the next stage.

(3) Compensation phase: In this phase, the deviation of threshold voltage, mobility and supply voltage are compensated. Scan_N and Ctrl_1 are pulled down in the beginning of this phase such that the gate of DTFT is floating and connected to C1. As a result, the gate voltage of DTFT is coupled to V_{dd}-V_{data}+$V_{th,DTFT}$ by C1 when the source voltage of DTFT is charged from V_{data}-$V_{th,DTFT}$ to V_{dd}. Therefore, in the beginning of this phase, the drive current can be expressed as:

$$\begin{aligned} I_{DTFT} &= K\mu_{eff}\left(V_{gs} - V_{th,DTFT}\right)^2 \\ &= K\mu_{eff}[(V_{dd} - V_{data} + V_{th,DTFT}) \\ &\quad -V_{dd} - V_{th,DTFT}]^2 \\ &= K\mu_{eff}V_{data}^2 \end{aligned} \tag{4.2}$$

From Eq. 4.2, the drive current in the beginning of this phase is apparently independent of the threshold voltage of DTFT and the supply voltage. Furthermore, it is worth noting that the difference in the drive current between different pixels depends mainly on the deviation of mobility. Accordingly, the drive current is used to create an (adaptive) compensation voltage in the gate of DTFT to mitigate the effects of mobility variation. To achieve this, Ctrl_2 is set to low after the coupling is completed such that drive current is able to charge C2 through Mp3. As a result, a compensation voltage at the gate of DTFT is created through the coupling from C2. By assuming that the charging time (t) is small and the value of C1 and C2 are of equal strength (C), the compensation voltage (ΔV_g) can be approximated as:

$$\Delta V_g \simeq \frac{I_{DTFT} t}{C} \tag{4.3}$$

It can be noted from Eqs. 4.2 and 4.3 that ΔV_g depends on the mobility of DTFT and data voltage with chosen C and t. For example, ΔV_g in DTFT with higher mobility is larger compared to ΔV_g in DTFT with typical mobility for the same data voltage. Although the gate voltages of DTFTs are initially equal, they are adjusted according to their own mobility to generate the target current. Detailed derivation of the design parameters (i.e., C and t) will be presented in the next subsection.

(4) Display phase: In this phase, Ctrl_2 goes high such that drive current stops charging C2 and OLED is reconnected to the drain of DTFT. Since the gate voltage of DTFT is increased by ΔV_g in the compensation phase, the drive current in this phase is given by:

$$I_{DTFT} = K\mu_{eff} \left(V_{data} - \Delta V_g\right)^2 \tag{4.4}$$

According to Eq. 4.4, it is evident that the inter-pixel threshold voltage deviation and the supply voltage drop are canceled while the mobility variation is compensated by ΔV_g. Consequently, a better compensation can be achieved.

4.3 Derivation of Design Parameters

Since ΔV_g depends on the capacitances and the applied charging time, inappropriate design parameters would result in over or insufficient compensation, and hence, worsen the non-uniformity in display. In this subsection, the appropriate design parameters for the proposed pixel circuit and the relative error equation for the drive current of the proposed pixel circuit are derived. We compare two pixels with different DTFTs. One has a nominal mobility while the other is with a shifted mobility. According to Eq. 4.2, the drive current in the beginning of the compensation phase can be expressed as:

$$\begin{aligned} I_{DTFT} &= K\mu_{eff}V_{data}^2 \\ I_{DTFT,\Delta\mu} &= K\left(\mu_{eff}+\Delta\mu\right)V_{data}^2 \end{aligned} \tag{4.5}$$

where I_{DTFT} is the current of DTFT with typical mobility and $I_{DTFT,\Delta\mu}$ represents the current of DTFT with shifted mobility in the beginning of compensation phase. Hence, from Eq. 4.3, compensation voltage for each DTFT can be written as:

$$\begin{aligned} \Delta V_g &= \frac{I_{DTFT}t}{C} \\ \Delta V_{g,\Delta\mu} &= \frac{I_{DTFT,\Delta\mu}t}{C} \end{aligned} \tag{4.6}$$

from Eqs. 4.4 and 4.5, the drive current in the display phase is given by:

$$\begin{aligned} I'_{DTFT} &= K\mu_{eff}\left(V_{data}-\Delta V_g\right)^2 \\ I'_{DTFT,\Delta\mu} &= K\left(\mu_{eff}+\Delta\mu\right)\left(V_{data}-\Delta V_{g,\Delta\mu}\right)^2 \end{aligned} \tag{4.7}$$

where, I'_{DTFT} is the current of DTFT with typical mobility and $I'_{DTFT,\Delta\mu}$ is the current of DTFT with shifted mobility in the display phase. The difference of the drive current between these two pixels can be approximately expressed as:

$$I'_{DTFT}-I'_{DTFT,\Delta\mu} = -K\left[2\alpha\beta\left(\mu_{eff}+\Delta\mu\right)+\Delta\mu\beta^2\right] \tag{4.8}$$

where $\alpha = \Delta V_g$-$\Delta V_{g,\Delta\mu}$ and $\beta = V_{data}$-ΔV_g. To determine the optimal value for t and C, the current difference in Eq. 4.8 is set to zero. By solving the equation, we can obtain the optimal C/t as:

$$\frac{C}{t} = 3K\mu_{eff}V_{data}+2K\Delta\mu V_{data} \tag{4.9}$$

Note that, the optimal C/t would change with V_{data} and $\Delta\mu$, as indicated in Eq. 4.9. Therefore, the current difference between these two pixels would be zero only for

one specific value of V_{data} and mobility. Since the largest relative error is observed in the largest I_{DTFT} [84] and most of TFTs have nominal mobility, the maximum data voltage (V_{data_max}) and nominal mobility (i.e., $\Delta\mu$=0) are chosen and applied in Eq. 4.9 to get the optimal value of C/t. Therefore, by substituting C/t with the optimal value ($3K\mu_{eff}V_{data\_max}$) into Eq. 4.8, the relative error of drive current is given as:

$$\frac{I'_{DTFT} - I'_{DTFT,\Delta\mu}}{I'_{DTFT}} = \frac{\Delta\mu}{\mu_{eff}}\left[1 + \frac{2\left(\mu_{eff} + \Delta\mu\right)}{\mu_{eff} + \frac{-\left(3\mu_{eff}+2\Delta\mu\right)V_{data\_max}}{V_{data}}}\right] \tag{4.10}$$

As inferred in Eq. 4.10, the relative error of drive current is zero when $V_{data} = V_{data\_max}$, and increases gradually as V_{data} decreases. Moreover, the relative error approaches $\Delta\mu/\mu_{eff}$ as V_{data} is close to zero. This is due to the fact that the difference in ΔV_g is too small to compensate the mobility variation when V_{data} approaches zero. Furthermore, the relative error is small when $\Delta\mu/\mu_{eff}$ is small.

4.4 Simulation Results and Discussion

In this subsection, we verify the insensitivity of the proposed VPM pixel circuit to the variation of threshold voltage and mobility of DTFT and the degradation of supply voltage. HSPICE simulations and Monte Carlo based statistical analysis have been carried out using RPI Poly-Si TFT model [60]. The poly-Si TFT characteristics were determined using the device simulator, Taurus [59], and the SPICE model parameters were extracted by Aurora [88]. The target maximum drive current is 1μA in this work. The layout for the proposed pixel circuit is shown in Fig. 4.3. The subpixel size is 64μm $\times$ 192μm which is suitable for 9.7 inches display with the resolution of 1024 $\times$ 768 (i.e., the target display panel for the following simulations). The estimated aperture ratio for the subpixel is approximately 41%. The timing diagrams for the applied signals for the proposed panel are shown in Fig. 4.4. Note that, instead of regular pulse signal, saw tooth wave signal is applied for Ctrl_2 for minimizing the

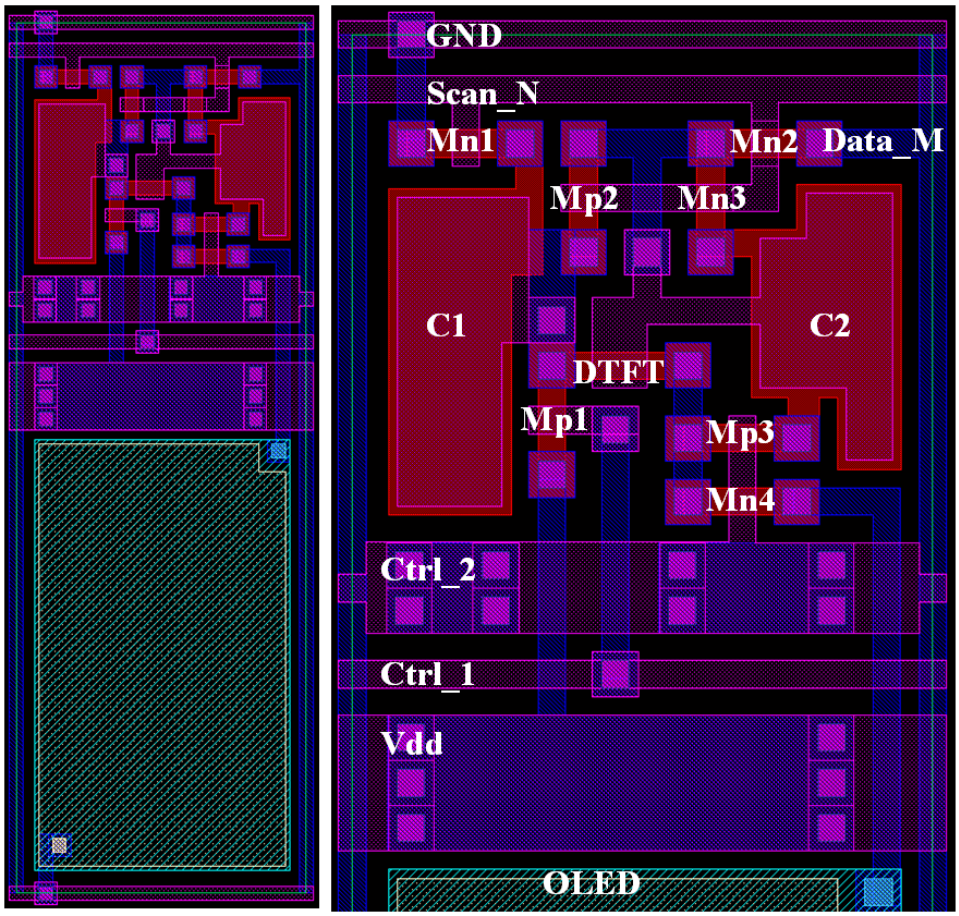


Fig. 4.3. The layout for the proposed pixel circuit. The subpixel size is 64μm x 192μm which is suitable for 9.7 inches display with the resolution of 1024 x 768. The estimated aperture ratio is approximately 41%. Note that some layers have been hided for better illustration (e.g., n+ and p+).

effect of parasitic capacitance and resistance of busline. For verifying the effectiveness of the proposed circuit, the simulation results from the prior VPM pixel circuit [18] are also shown for comparison. The prior pixel circuit in [18] is shown in Fig. 4.5. The Scan_N and Ctrl_1 for the prior VPM circuit [18] are set to be the same with that of the proposed circuit. Table 4.1 shows the values of the circuit parameters used in the HSPICE simulations for both circuits. The mobility of typical p-channel is $100cm^2/V \cdot s$, and is assumed to have a worst case deviation of 40% ($\pm 40cm^2/V \cdot s$)

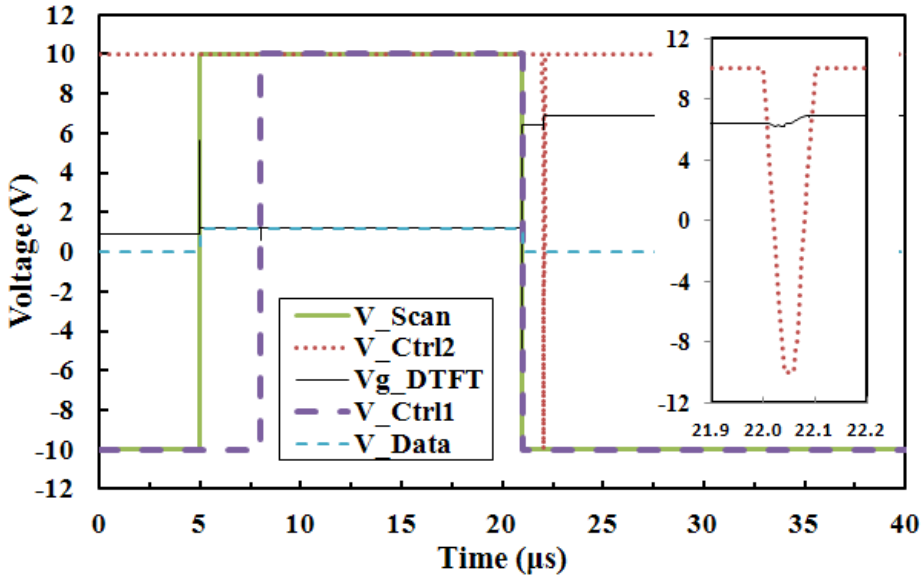


Fig. 4.4. The timing diagrams for the applied signals and V_{g_DTFT} for the proposed pixel circuit.

Table 4.1.
Values of Circuit Parameters for the Proposed and Prior Pixel Circuits

Parameters	Values
Mn1-Mn4	$W/L = 3\mu m/3\mu m$
Mp1-Mp3	$W/L = 3\mu m/3\mu m$
DTFT	$W/L = 3\mu m/6\mu m$
C1, C2	$200fF$
Scan_N	$-10V/10V$
Ctrl_1, Ctrl_2	$-10V/10V$

according to the experimental data in [12]. The threshold voltage of a typical p-channel TFT is $-2.0V$ with a worst case deviation of $\pm 0.3V$.

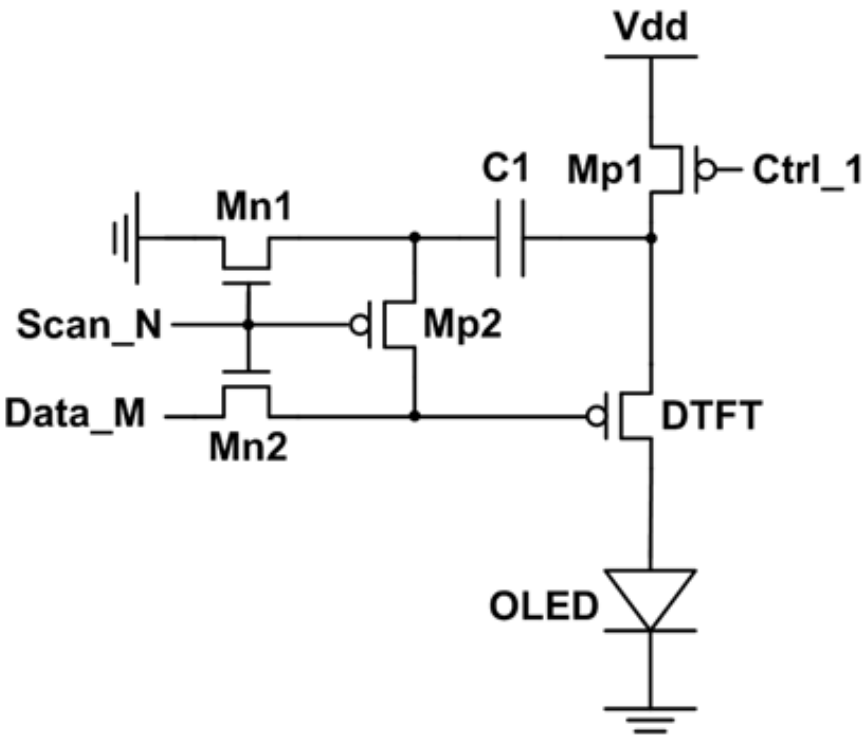
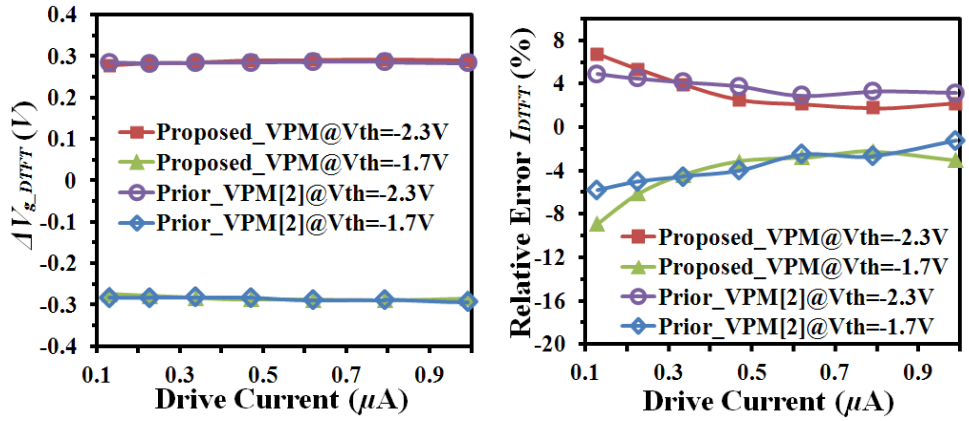


Fig. 4.5. Prior VPM pixel structure in [18]

The compensation results for a $\pm 0.3V$ threshold voltage shift in DTFT are plotted in Fig. 4.6 where ΔV_{g_DTFT} represents the gate voltage difference between DTFT with and without V_{th} shift in the display phase (i.e., ΔV_{g_DTFT}=$\Delta V_{g,\_\Delta\mu}$-ΔV_g). The gate voltage of DTFT, in Fig. 4.6(a), is changed corresponding to the shift of threshold voltage in different current levels for both the proposed and the prior pixel circuit. This indicates that the drive current of the proposed and prior VPM pixel is independent of threshold voltage deviation. As verified in Fig. 4.6(b), the relative error in the both pixel circuits is within $\pm 3\%$ ($30nA$) at high current level. Although the relative error of the proposed pixel circuit is higher than that of the prior VPM pixel circuit at low current level, the current difference between them in the lowest current level is only $4nA$. Hence, the proposed pixel circuit has similar efficacy to the threshold voltage variation compared to the prior VPM pixel circuit.



(a) (b)

Fig. 4.6. (a) ΔV_{g_DTFT} in the proposed and prior VPM pixel [18] with respect to nominal drive current for different threshold voltage shift. ΔV_{g_DTFT} is the gate voltage difference between DTFT with and without V_{th} shift in the display phase. (b) Relative error of drive current as a function of nominal drive current for different threshold voltage shift in DTFT of the proposed and prior VPM pixel [18].

The simulation results for the relative error with different supply voltage degradations are shown in Fig. 4.7. Note that, the simulation results for the conventional pixel (Fig. 4.1b) are included for comparison to see the impact of the supply voltage degradation. From Fig. 4.7, as the supply voltage drops from $10V$ to $8.5V$ (i.e., the worst case for the target panel), a drive current deviation of around 99% in the conventional pixel circuit can be observed. On the other hand, the proposed and the prior VPM pixel circuits can maintain a stable drive current with deviation within 15%. The simulation results suggest the feasibility of applying the proposed pixel circuit in large sized and high resolution display applications.

In Fig. 4.8, we examine the impact of the mobility deviation on the drive current. The gate voltage shift of DTFT (ΔV_{g_DTFT}) is plotted with different drive current and mobility deviation in Figs. 4.8(a) and 4.8(b). As explained in subsection II, the compensation voltage is supposed to depend on the mobility and current of DTFT. As verified in Fig. 4.8(a), the gate voltage decreases as the drive current decreases

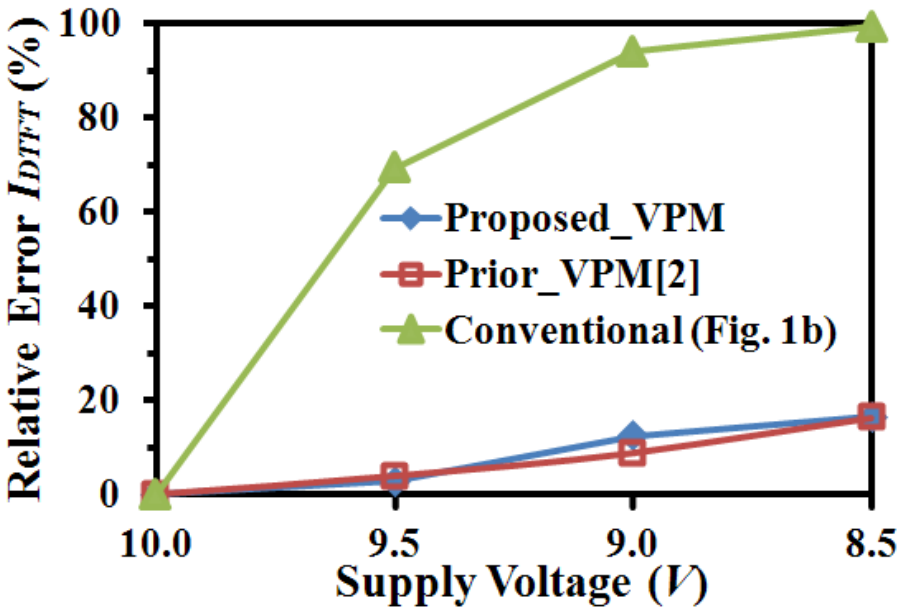


Fig. 4.7. Relative error of drive current as a function of supply voltage for the conventional, the prior VPM [18], and the proposed VPM pixel circuit.

under iso-mobility condition. Furthermore, Fig. 4.8(b) shows that the gate voltage in the proposed pixel circuit also changes corresponding to the mobility deviation, whereas the gate voltage in the prior VPM pixel remains relatively constant. As depicted in Fig. 4.8(c), it is evident that the proposed pixel circuit is capable of compensating the mobility variation with an error range from -2% to 1% depending on the mobility deviation and I_{DTFT}. However, the prior VPM pixel circuit has a corresponding error range from 4% to -8%. Note that, the simulation results match with the mathematical proof shown in Eq. 4.10. The relative error of the proposed pixel circuit is close to 0%, when the current is $1\mu A$ and gradually increases as drive current decreases as shown in Fig. 4.8(c). Moreover, the relative error of the proposed pixel circuit is close to the prior VPM pixel circuit (i.e., the pixel circuit without compensating the mobility variation) at low current level as predicted by Eq. 4.10.

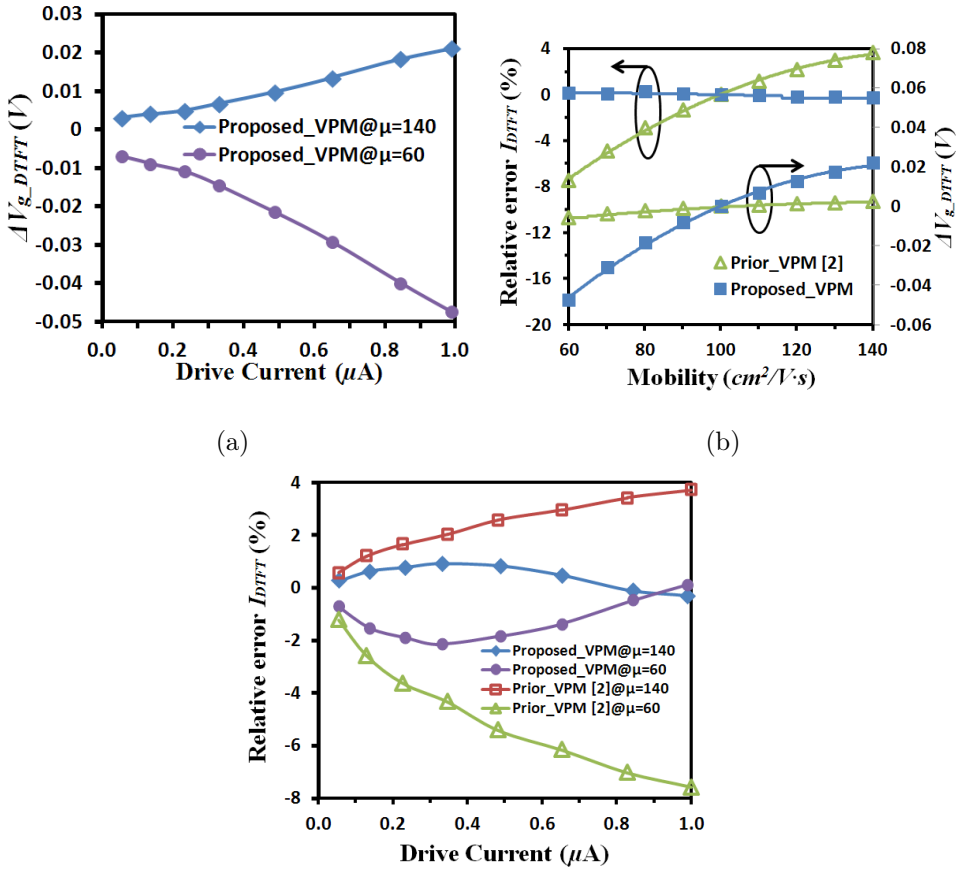


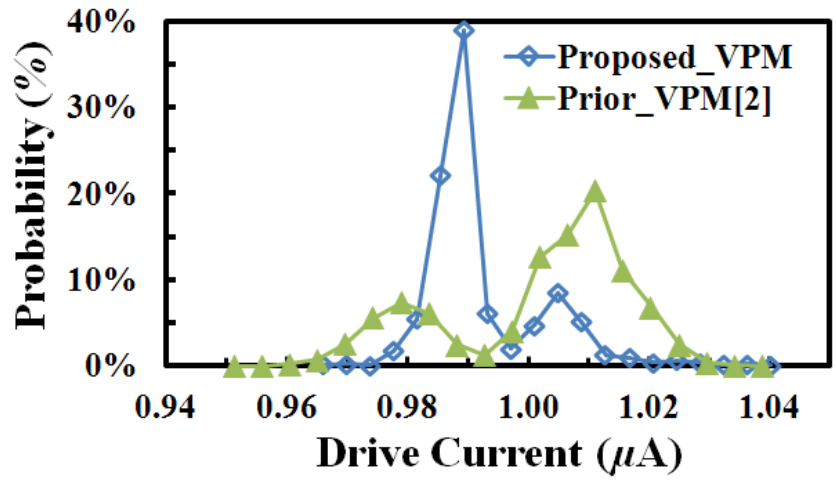
Fig. 4.8. (a) ΔV_{g_DTFT} with respect to nominal drive current for different mobilities (60 and $140 cm^2/V \cdot s$) of DTFT in the proposed VPM pixel circuit. (b) ΔV_{g_DTFT} and the relative error of drive current as a function of mobility for the proposed and prior VPM pixel circuit [18]. (c) The relative error of drive current with respect to drive current for different mobility shift (60 and $140 cm^2/V \cdot s$) of DTFTs in the proposed and prior VPM pixel circuit [18].

To simulate the situation in a real display panel, 10000 Monte Carlo simulations were performed under the combined effect of threshold voltage and mobility shift. Gaussian statistical distribution functions were adopted for modeling fluctuations of threshold voltage and mobility in the analysis. The 3σ of threshold voltage and mobility are $\pm 0.15V$ and $\pm 20 cm^2/V \cdot s$ respectively. As shown in Fig. 4.9(a), less spread of drive current is observed in the proposed VPM pixel compared to that of

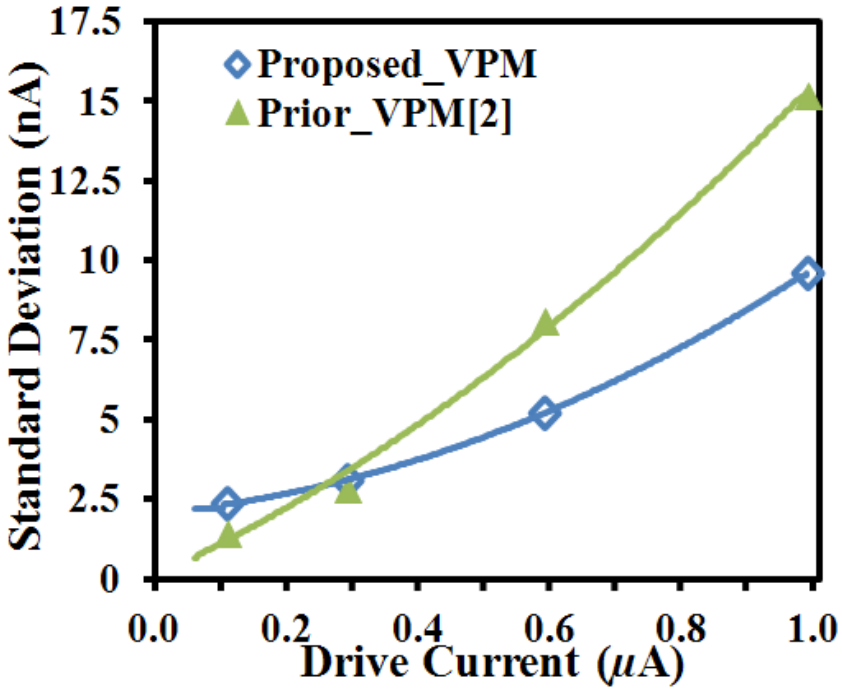
prior VPM pixel when nominal drive current is $1\mu A$. Fig. 4.9(b) reveals the standard deviation of drive current with respect to the nominal drive current. The proposed VPM pixel circuit shows a comparatively smaller deviation than the prior pixel circuit, although the difference shrinks as the drive current strength goes down. Accordingly, an improved uniformity of AMOLED displays (with less probability of observable dot defects) can be obtained with the application of the proposed compensation technique.

Finally, since the charging time for the compensation phase is short, the parasitic capacitance and resistance of busline for Ctrl_2 may induce non-uniformity luminance across display. To verify the effect of parasitic capacitance and resistance of Ctrl_2 on drive current, we simulated the variation of the drive current with respect to the number of pixels. The RC loading of Ctrl_2 is evaluated based on the pixel layout shown in Fig. 4.3. We assume that the sheet resistance for metal is 0.3 Ω/sq, unit capacitance of gate oxide is $0.58fF/\mu m^2$ and Ctrl_2 is driven from both side of pixel array. As shown in Fig. 4.10, the maximum deviation of drive current due to the RC loading of Ctrl_2 is only about 6% when the nominal $I_{DTFT} = 1\mu A$. Furthermore, it should be noted that the predictable and regular change of luminance across display can be easily taken care of by image processing techniques and should not be a big concern for the proposed circuit.

The simulation results in this subsection confirm that the proposed pixel circuit has much better consistency of drive current against the device variations and supply voltage drop compared to the conventional (Fig. 4.1b) and the prior VPM pixel [18] circuits. Although the proposed pixel circuit might limit the aperture ratio because of the increased number of devices, the issue would be less important for large sized display applications, where the pixel area is large. Furthermore, when top emission process is applied (i.e., the light is extracted from the top of the pixel circuits by making the cathode of OLED transparent [89]), the proposed pixel structure can also be used in small sized display applications without the concern for small aperture ratio.



(a)



(b)

Fig. 4.9. (a) Statistical drive current distribution and (b) standard current deviation as a function of nominal drive current for DTFTs of the proposed and prior VPM pixel circuit [18], under combinational effect of threshold voltage and mobility shift.

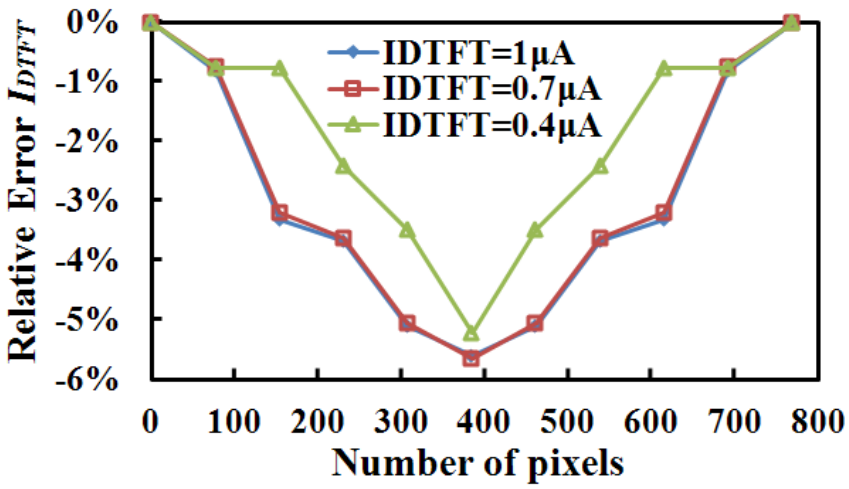


Fig. 4.10. The deviation of drive current with respect to the pixel number due to the parasitic capacitance and resistance of Crtl_2.

4.5 Conclusions

In this work, an improved VPM pixel circuit is proposed for AMOLED displays to address the threshold voltage shift, the mobility deviation, and the supply voltage degradation. The efficacy of the proposed approach was verified both analytically and using HSPICE simulations. The simulation results show that the maximum deviation of drive current is $30nA$ for the threshold voltage shift of $\pm 0.3V$ and the deviation range is within 2% for mobility variation from $60cm^2/V \cdot s$ to $140cm^2/V \cdot s$. Furthermore, if the supply voltage degrades from $10V$ to $8.5V$, the maximum drive current variation is below 15%. Monte Carlo based statistical analysis shows a smaller spread of drive current in the proposed VPM pixel compared to that of the prior VPM pixel (under the combined effect of threshold voltage and mobility shift). Consequently, the immunity to the device variations, fast programming time, and the simplicity of the circuits, make the proposed VPM pixel circuit a promising candidate for large sized and high resolution AMOLED display applications.

5. VARIATION-TOLERANT AND SELF-REPAIR DESIGN METHODOLOGY FOR LOW TEMPERATURE POLYCRYSTALLINE SILICON LIQUID CRYSTAL AND ORGANIC LIGHT EMITTING DIODE DISPLAYS

In this section, from a system and circuit design perspective, we propose a new self-repair design methodology to compensate the GB-induced variations for LTPS liquid crystal displays (LCDs) and active-matrix organic light emitting diode (AMOLED) displays. The key idea is to extend the charging time for detected low drivability pixel switches, hence, suppressing the brightness non-uniformity and eliminating the need for large voltage margins. The proposed circuit was implemented in VGA LCD panels which were used for prediction of power consumption and yield. Based on the simulation results, the proposed circuit decreases the required supply voltage by 20% *without performance and yield degradation.* 7% *yield enhancement is observed for high resolution, large sized LCDs while incurring negligible power penalty. This technique enables LTPS-based displays either to further scale down the device size for higher integration and lower power consumption or to have superior yield in large sized panels with small power overhead.*

5.1 Introduction

Conventionally, the peripheral and control circuits of an LTPS-based display use bulk silicon and are integrated externally, due to which they are less susceptible to variations when compared to the LTPS pixel array. Hence, variation in pixel switches is the root cause of the brightness non-uniformity of LCD and AMOLED display. Several techniques for decreasing the variation of leakage current in pixel switches have been proposed. By mitigating the electric field near the drain region,

lightly doped drain (LDD) and dual-gate structure can effectively reduce the leakage current induced by the field emission via trap states [94]- [95]. However, techniques for suppressing the variation in drivability of pixel switches have been rarely discussed. To ensure sufficient drivability in all pixel switches, increasing supply voltage is the most commonly applied technique to account for the worst-case combination of variabilities. However, high supply voltage greatly increases the power consumption and worsens the reliability of TFTs [21]. Moreover, as the panel size or resolution is increased, yield loss, due to GBs and global variation, becomes more and more significant, even with a high supply voltage. Therefore, it is important to develop a new design methodology to properly deal with the variations in charging time of pixel switches and to reduce the resultant yield loss. In this section, we propose a circuit to detect and extend the charging time for defective pixels (i.e. pixels with insufficient drivability) at the expense of slight increase in the operating frequency of peripheral circuits [22]. In other words, to maintain the same refresh rate, the charging time of each row of pixel array is slightly decreased for creating timing slacks which allow a few rows to execute two-cycle operation. Therefore, a lower supply voltage can be used since defective pixels are now allowed to extend charging time. Consequently, the proposed circuit is capable of not only improving the yield, but also the reliability under low voltage operation.

5.2 Related Work

Previous research works for minimizing variation of TFT characteristics have been primarily conducted from device and process optimization perspective [74], [43]. In [74], the authors proposed a multi-finger (MF) structure to effectively decrease the variation of charging time. The idea is to split one large transistor into several parallel smaller transistors with the same geometry. The random charging time between each smaller transistor can be compensated by each other. As a result, the spread in variation is decreased in contrast to an equivalent single large device. Note, consid-

ering the limitation of leakage current and aperture ratio, minimum size transistors are preferable for pixel switches in conventional design. Hence, when a MF structure is applied, leakage current will correspondingly get multiplied by the number of MFs. Furthermore, the overall layout area required by the fingers and the spacing between fingers increases. It is therefore not suitable for application in pixel design. Tile alignment is another technique to reduce the variation of threshold voltage and mobility by taking advantage of periodic GBs in a sequential lateral solidification process [43]. Since the shifting of electrical characteristics between neighboring transistors is mainly due to the GBs in the channel [6], uniform number of GBs is expected to reduce the variation of electrical characteristics. With proper control of grain size, the channel of transistors, tilted by 45° to the direction of GB, can have identical number of GBs in different positions of the substrate. This leads to better uniformity in device characteristics. However, this technique does not account for the variations caused by position differences of GBs. It is reported that the drivability of transistor varies with different position of GBs in the channel [31]. Furthermore, uniformity is expected to be worse when size of transistors is comparable to the grain size. Since it is apparent that GB-induced variation is unavoidable, significant reduction in variation cannot be achieved solely by process and device optimizations. Hence, an investigation of circuit-level variation compensation techniques is required to resolve the uniformity issue.

5.3 Proposed System

Figure 5.1 shows the conventional pixel structure of LCDs and AMOLED displays. It is to be noted that the requirements for pixel switches in LCDs and AMOLED displays are identical. Pixel switches need to charge the storage capacitor (Cst) close to the data voltage on the data line during the short charging time. Furthermore, during the long hold time, leakage current through the pixel switches must be minimized for retaining the same brightness. Although recent researches on AMOLED focus mainly

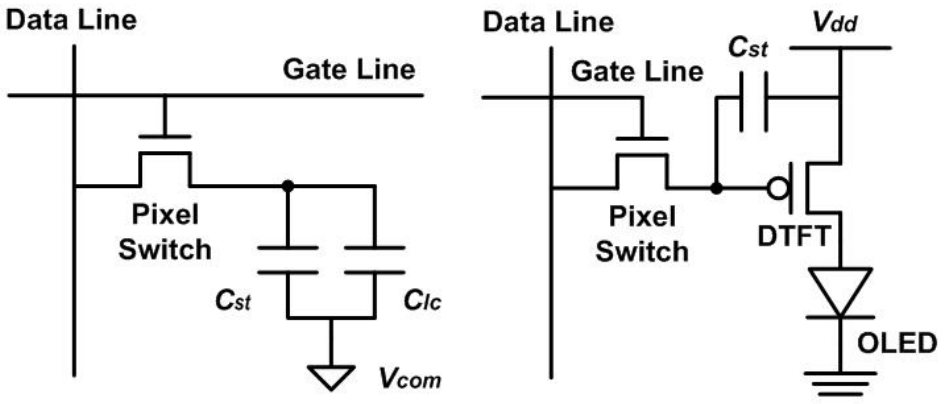


Fig. 5.1. Pixel structure of (a) LCD and (b) AMOLED display

on compensating the variation effects on the driving TFT (DTFT) [96], the variation in pixel switches is also one of the root causes of uniformity issue. The proposed compensation technique is expected to improve the uniformity issue caused by insufficient drivability in both LTPS-based LCDs and AMOLED displays. However, due to the similar structures of LCDs and AMOLED displays, only implementation for LCDs is presented in this work.

The system block diagram of the proposed circuit for the LCD panel is illustrated in Figure 5.2. This circuit consists of three sub-circuits, namely detector, memory unit and CLK generator. The detector detects the defective pixels and generates the signals for the memory unit and CLK generator circuit. The memory unit stores the detected signals and generates two-cycle enabling signals for the CLK generator. The CLK generator is responsible for determining the CLK frequency from the output of the detector and then generating a modified clock signal which gives defective pixels two-cycle charging time.

Operations of proposed circuits can be described in three phases: set-up phase, detection phase, and display phase. In the set-up phase, the data pattern, which requires the longest charging time, is used for determining the locations of defective pixels. It is achieved by discharging pixel voltage to the minimal level in the first frame time and recharging it to the maximum level in the following frame time.

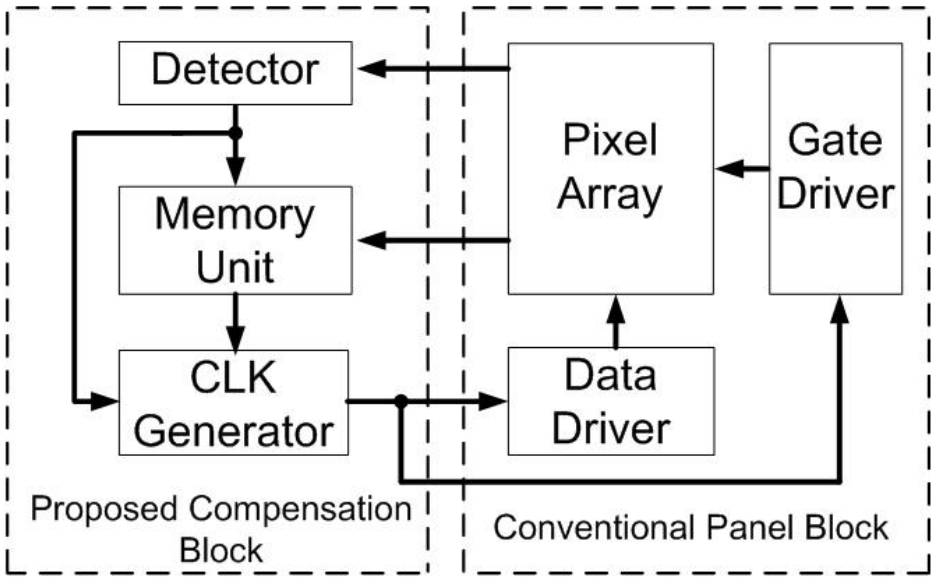


Fig. 5.2. Block diagram of proposed LTPS LCD panel

In the detection phase, the detector is responsible for defect detection. Detection results are stored in the memory unit and forwarded to the CLK generator. The CLK generator selects the proper clock signal according to the number of faulty rows (i.e. rows in pixel array containing defective pixels) recorded in a multi-bit counter (e.g. four-bit counter). In the display phase, an adaptive clock signal is produced by processing the output of the memory unit and the selected clock signal with CLK generator. The detailed operation of each circuit block is described as follows.

As shown in Figure 5.3, the detector block is comprised of comparators and multi-input OR gate while considering the detector block, we make the assumption that the comparator circuitry is designed to be variation tolerant by proper design techniques (e.g. the MF structure). In the set-up phase, the detection enable signal, ENA, is set to be low. The detector is, hence, independent of the memory unit and pixel array. In the detection phase, ENA is set to high. Data lines are precharged to the maximum level. After gate driver turns on one row of pixel switches, charge sharing starts between data lines and pixels. Data line voltage will either stay at the same level with normal pixels or at a lower voltage level due to the defective pixels. The amount

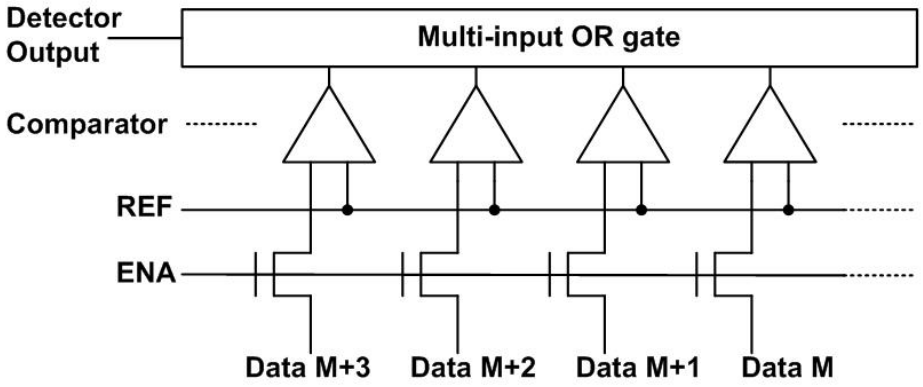


Fig. 5.3. Detector block

of voltage drop depends on the ratio of the parasitic capacitance of data line and the storage capacitance of the pixel. The comparators compare the voltage level of each data line with a reference voltage, REF, to judge the existence of the defective pixels. A row of pixel array is defined to be faulty if the voltage in any of the pixels in that row is lower than the reference voltage. This is done by processing the output results of each comparator in the multi-input OR gate. Thereafter, an output signal for the detected row is generated by multi-input OR gate and then delivered to memory unit and CLK generator. In the display phase, ENA is again set to low, thereby, isolating detector from the memory unit and pixel array.

The memory unit circuit is composed of static random access memories (SRAMs) and transmission gates (TGs), as shown in Figure 5.4. In the detection phase, ENA is set to high, that allows the memory cell to be connected to the detector, and blocks the output to CLK generator. Since access transistors of SRAM are controlled by specific gate line, the output signals of detector are written in the corresponding SRAM. In the display phase, the memory unit stops receiving signals from the detector and connects to the CLK generator since ENA is set to low. The values stored in SRAMs are forwarded sequentially to the CLK generator and used for modulating the CLK period. Hence, the additional cycles (two-cycle operation) for charging the faulty rows are accommodated within the available refresh rate.

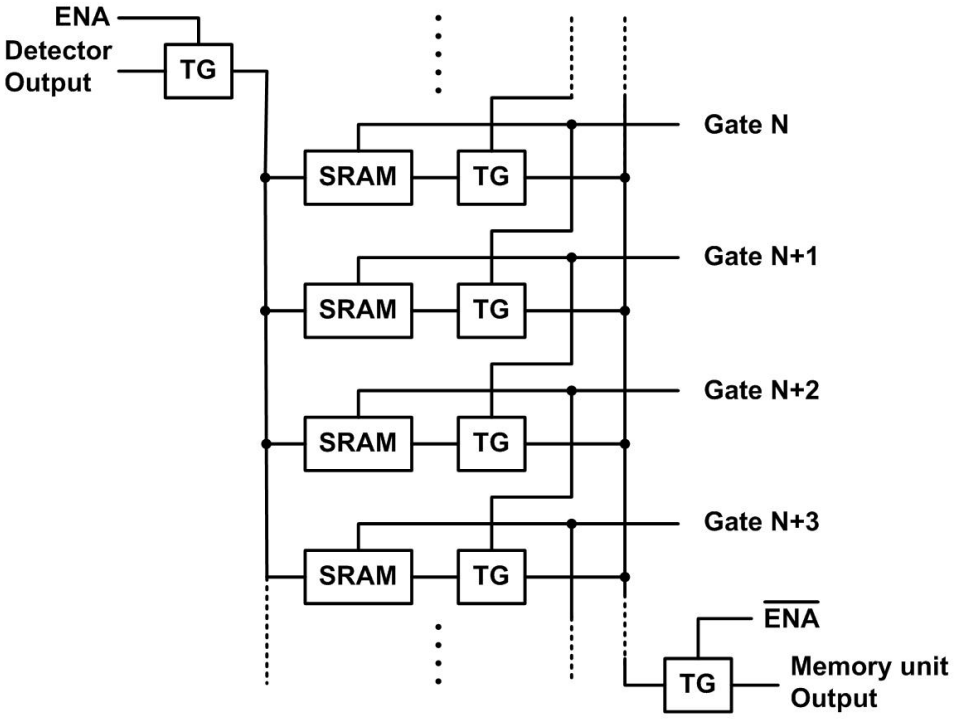


Fig. 5.4. Memory unit block

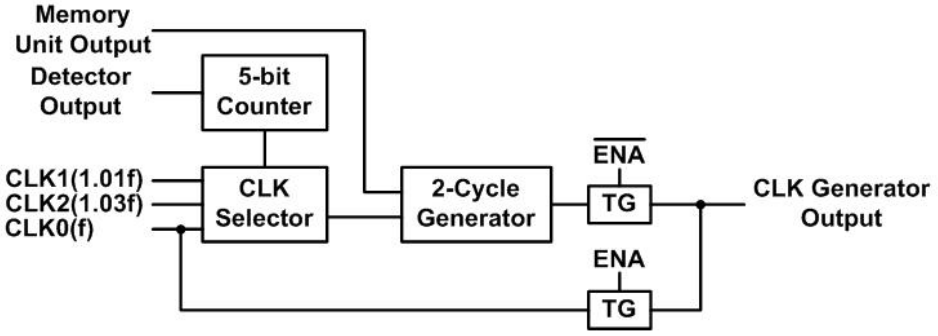


Fig. 5.5. CLK generator block

The CLK generator, depicted in Figure 5.5, consists of a four-bit binary counter, a CLK selector and a two-cycle generator. The difference among CLK0, CLK1 and CLK2 is the operating frequency. CLK0, with the lowest frequency, is set to be the default clock used in the detection phase, while CLK1 or CLK2 are used when faulty rows exist. Higher clock frequency enables more timing slacks which allows more two-

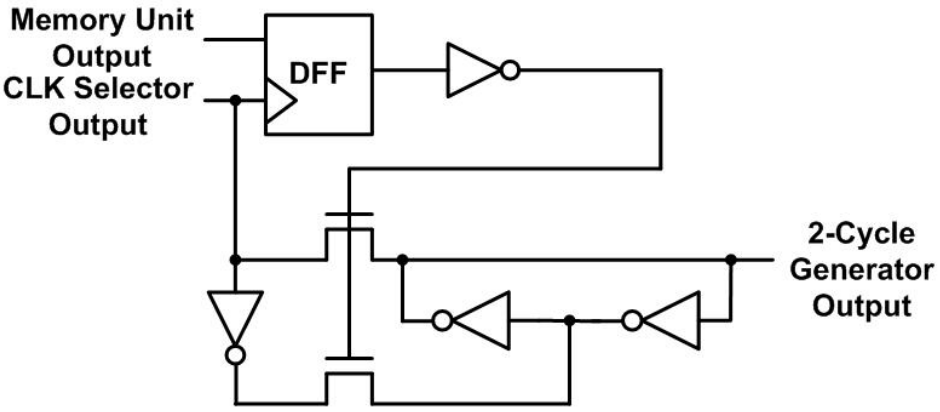


Fig. 5.6. Two-cycle generator block

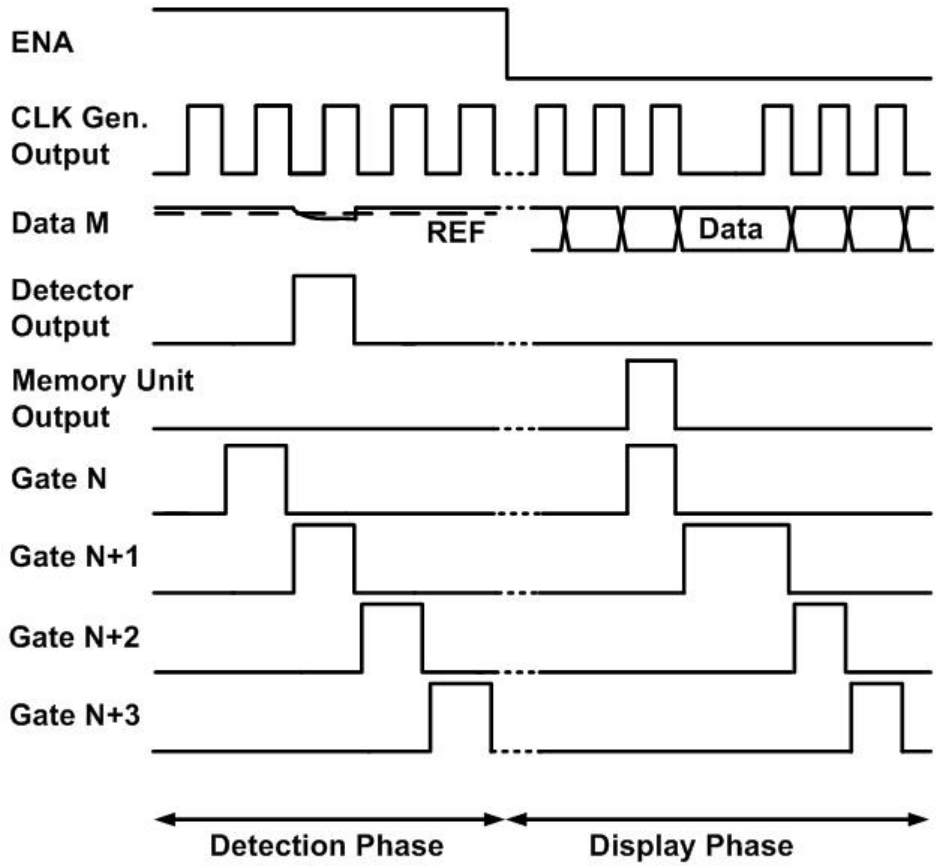


Fig. 5.7. Timing chart of proposed circuit

cycle operations. However, the frequency should be carefully selected for preventing increased failure of normal pixels due to a shorter charging time. After receiving the detector output signals in the detection phase, the four-bit binary counter generates four output signals which allow the CLK selector to select an appropriate clock for preventing unnecessary power consumption (e.g. CLK0 is selected as four output signals are low). The two-cycle generator, as illustrated in Figure 5.6, consists of one DFF, two access transistors and four inverters. In the display phase, the selected clock from the CLK selector will be processed with the output signals from memory unit in DFF to generate an output signal for enabling two-cycle operation. If the output of the memory unit is high, the DFF will generate a high signal to isolate the selected clock from the output by the access transistors. In the mean time, the output value of the previous cycle is held by the cross-coupled invertors leading to an extended clock. When the output of the memory unit is low, the selected clock from the CLK selector will become the output of the two-cycle generator without any modification. Figure 5.7 shows a timing diagram of a two-cycle operation for LCD panel that has a defective pixel in the $(N+1)^{th}$ row. In the detection phase, as the defective pixel is detected in the $(N+1)^{th}$ row, a pulse from the detector is generated in the $(N+1)^{th}$ clock cycle. In the display phase, a specific clock frequency is selected corresponding to the number of faulty rows obtained in the detection phase. The memory unit generates a pulse in the N^{th} clock cycle causing an extended clock signal to occur in the $(N+1)^{th}$ clock cycle, permitting doubled charging time for the $(N+1)^{th}$ row. In the $(N+2)^{th}$ row, normal clock period resumes.

5.4 Device Modeling and Panel Simulation

In this subsection, the supply voltage and yield for the proposed circuit architecture is compared with conventional design shown in Figure 5.2. For the sake of brevity and clarity, the focus of this simulation is limited to the GB induced variations. However, it should be noted that the proposed technique is also effective in

addressing the variations due to other process parameters. The Monte Carlo method was utilized to estimate the yield. The standard deviations of threshold voltage and mobility for the Monte Carlo simulation were acquired using the following models.

5.4.1 Device Modeling

In most crystallization processes of polycrystalline silicon, crystal grain grows in a random manner, thereby, introducing randomly distributed GBs. These GBs result in significant variation in electrical parameters between neighboring transistors. In this subsection, first, the device model of the interrelations between grain size and device characteristics is provided. Then, the standard deviations of threshold voltage and mobility are derived for use in subsequent Monte Carlo simulations. Assuming GBs are distributed in a Gaussian way,the Poisson area scatter distribution is employed to model the number of grains in a given area [97].

$$P(k) = [exp(-\lambda) \cdot \lambda^k]/k! \tag{5.1}$$

where k is the Poisson random variable, and $lambda$ is the mean. To correlate the average grain size with Poisson random variable, k is assumed to be the number of grains in the channel of the transistor. The average grain size, $L_{g,TFT}$, can be given by [12]

$$L_{g,TFT} = \sqrt{W \cdot L/k} \tag{5.2}$$

Based on the models established by Wang [12], which physically relates $L_{g,TFT}$ to TFT behavior, the variation range for threshold voltage and mobility is evaluated. Aside from body doping and gate oxide thickness, the threshold voltage of LTPS TFT is influenced by the defect states in GBs. The presence of defect states leads to the trapping of free charge carriers. To overcome the trapped charge effect, an extra voltage needs to be applied. The threshold voltage (V_{th}) model is then given by [12]

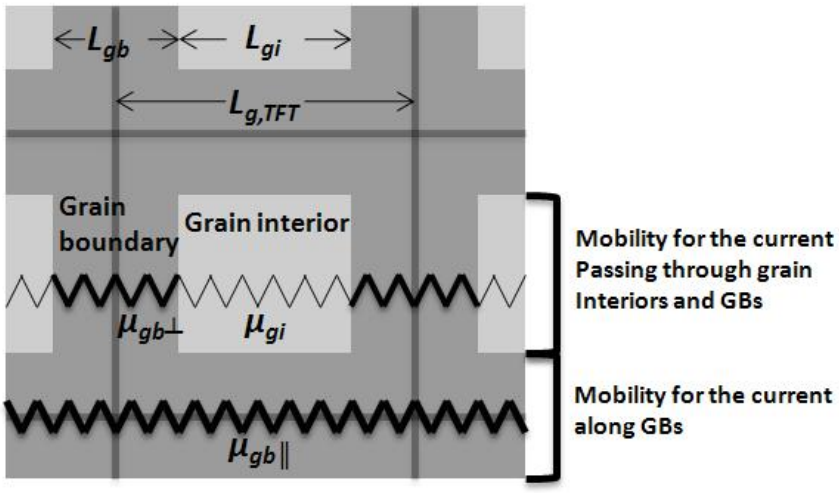


Fig. 5.8. Schematic of mobility model

$$V_{th} = V_{FB} + \left(1 - \left(\frac{\epsilon_{Si} E_{SC} L_{g,TFT}}{q N_{tr} L}\right)\right) \sqrt{\frac{8kTN_{tr}t_{ox}}{C_{ox}L_{g,TFT}} \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}}} \tag{5.3}$$

where V_{FB} is the flatband voltage ($-0.51V$), $L_{g,TFT}$ is the average grain size (800nm), N_{tr} is the monoenergetic trap density ($2 \times 10^{13}\ cm^2$), t_{ox} is the gate oxide thickness ($30nm$), and E_{SC} is the short-channel field parameter ($5.3MV/cm$). The flatband voltage, trap density and short-channel field parameters are set as suggested in [12]. The term in the bracket represents a semi-empirical short channel correction for some of the GBs charged by the drain in the channel. The term under the radical is for the trapped charge effect – free charges are depleted from the inversion layer by the trapped charges in GBs [98].

To model mobility, a TFT channel region is decomposed into grain interiors and GBs. The effective mobility of TFTs can be regarded as the weighted sum of the carrier mobility along the GBs and through grain interiors and GBs, as shown in Figure 5.8. The effective mobility (μ) thus follows [12]:

$$\mu = \left(\frac{l_{gb}}{L_{g,TFT}}\right) \mu_{gb,\parallel} + \left(1 - \left(\frac{l_{gb}}{L_{g,TFT}}\right)\right) \mu_g \tag{5.4}$$

The characteristic of μ_g is given by

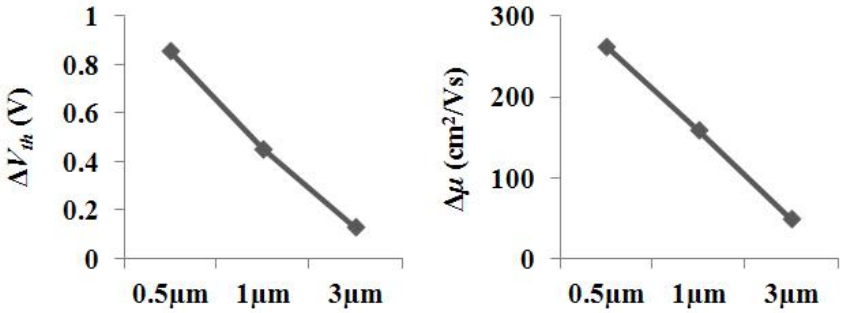


Fig. 5.9. Standard deviations of the threshold voltage and mobility at different technology nodes.

$$\mu_g = \mu_{gi} L_{eff} \left((N-1) \left(l_{gi} + \left(\frac{\mu_{gi}}{\mu_{gb,\perp}} \right) l_{gb} \right) + L_{g,TFT} \right)^{-1} \tag{5.5}$$

where l_{gb} is the effective GB width ($100nm$), μ_{gi} is the interior mobility ($300cm^2/Vs$), $\mu_{gb\perp}$ is the transverse boundary mobility ($30cm^2/Vs$) and $\mu_{gb\|}$ is the longitudinal boundary mobility ($3cm^2/Vs$) [12]. Trapped carriers at the GBs increase the scattering in the channel, and therefore, $\mu_{gi} \gg \mu_{gb\perp}$. $\mu_{gb\perp}$ represents the combination of both scattering when the carriers penetrate the GBs and the reduced trap density near the GBs. Compared to $\mu_{gb\perp}$, $\mu_{gb\|}$ is small since the high probability of scattering is observed when carriers travel along the GBs. One can see that the nominal effective mobility increases as the transistor size shrinks due to reduced number of GBs in the channel (eq. 5.4 and 5.5).

The calculated standard deviation of threshold voltage and mobility for different TFT sizes are plotted in Figure 5.9. Increased spread in threshold voltage and mobility is observed as device size decreases. This is due to the increased variation of average grain size when the size of device shrinks.

5.4.2 LCD Panel Simulation

In order to increase the computation efficiency of the Monte Carlo simulation, the complexity of the LCD panel circuit is simplified; one pixel model with 12 sets of

Table 5.1.
Characteristics of LTPS TFT-LCD panels

Panel size (inch)	3.9	0.85	0.4
Switch TFT (W/L)	$3/3\mu m$	$3/3\mu m$	$3/3\mu m$
Resolution (H/V)		640/480	
Gray level		256	
V_{th} of LC (V)		3.3	
Refresh rate (Hz)		60	

RC loading is applied in the simulation. Different sets of loading represent different locations of pixels in the display area. The characteristics of LCD panels evaluated in this simulation are shown in Table 1. For determining TFT characteristics, we have used the device simulator, TAURUS. The parameter extraction for the HSPICE RPI Poly-Si TFT model is done by using Aurora [88]. The parametric variations have been lumped into threshold voltage and mobility variations. The standard deviation of threshold voltage and mobility for the Monte Carlo simulation are modeled as mentioned in subsection IV. For the power estimation, an on-glass gate driver and multiplexer (MUX) are assumed, while the data driver is integrated externally. The gate driver with the calculated load is simulated in HSPICE for estimating power consumption. The power consumptions of MUX and Data driver are calculated using fCV^2 (f: Frequency, C: Capacitance, V: voltage swing). Simulations start with the nominal parameters and no variations for determining a solution that meets the specification. Thereafter, variations are included for determining suitable supply voltage that meets the yield constraint. The V_{dd}-V_{ss} obtained by $640 \times 480 \times 100$ (the total number of pixels in 100 LCD panels with VGA resolution) Monte Carlo simulations is shown in Figure 5.10. It can be observed that the required V_{dd}-V_{ss} increases as

the device size decreases. This is because V_{dd} and V_{ss} are mainly determined by the threshold voltage of liquid crystal (LC) and the transistor variations. Since smaller transistors have larger variations, as shown in Figure 5.9, higher supply voltage is needed for compensation. However, high supply voltage not only raises the power consumption but also aggravates the reliability of TFTs [21]. Due to the existence of GBs and poor heat dissipation of TFTs, hot carrier and self-heating can cause serious problems in TFT devices [21] [99]. When devices are subjected to high field, hot carriers, generated near the drain edge, are easily trapped at GBs or damage the gate oxide, thus degrading the leakage current and drivability of devices [99]. As the TFT turns on, the channel temperature is elevated by Joule heating. Deteriorated heat dissipation, due to glass substrate and high supply voltage, makes TFT device more vulnerable at high temperature. As a result, the density of midgap states in GBs increases and, hence, degrading the on-current, off-current and subthreshold swing of TFTs [21]. Consequently, the reduction of supply voltage is required for small-dimension TFTs. The proposed design, as shown in Figure 5.10, effectively reduces the required V_{dd}-V_{ss} compared to the conventional design in the same technology node. Furthermore, the advantage becomes more apparent as the transistor size shrinks. Hence, with reduced supply voltage, the proposed technique not only decreases the power consumption but, more importantly, provides relief from hot carrier and self-heating constraints for scaled-down devices.

In Figure 5.11, the simulated power consumption of the proposed and conventional design in different technology nodes are shown for comparison. It can be seen that, with shrinkage in device size, the power consumption reduces due to the decrease in switching and coupling capacitances. Figure 5.12 shows the power saving of the proposed design at different CLK frequencies for different technology nodes. As expected from Figure 5.10, the power saving is larger when the decrease in V_{dd}-V_{ss} is larger. However, it is worthy to note that the ratio of power saving in each technology node does not match with the difference of required V_{dd}-V_{ss}. This is due to the fact that the voltage swing of data driver is decided by the threshold voltage of LC rather

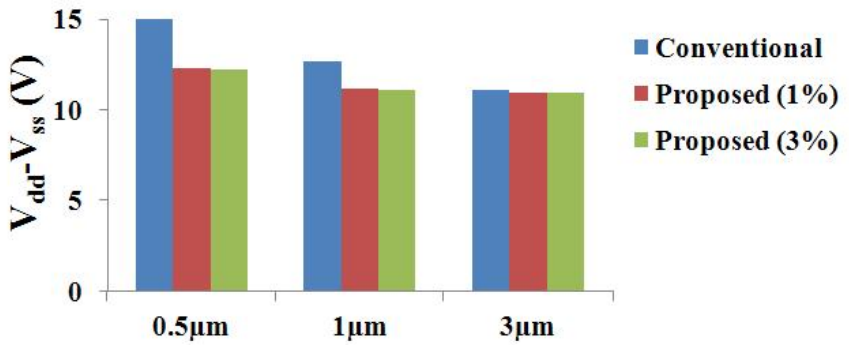


Fig. 5.10. The V_{dd}-V_{ss} of conventional and proposed methodology (1% and 3% increase of CLK frequency)

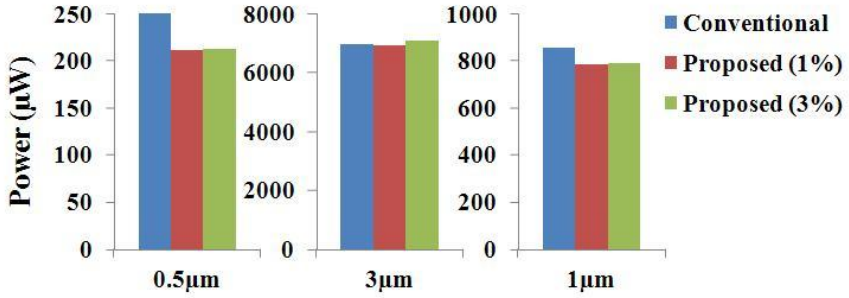


Fig. 5.11. Power consumption of conventional and the proposed methodology (1% and 3% increase of CLK frequency)

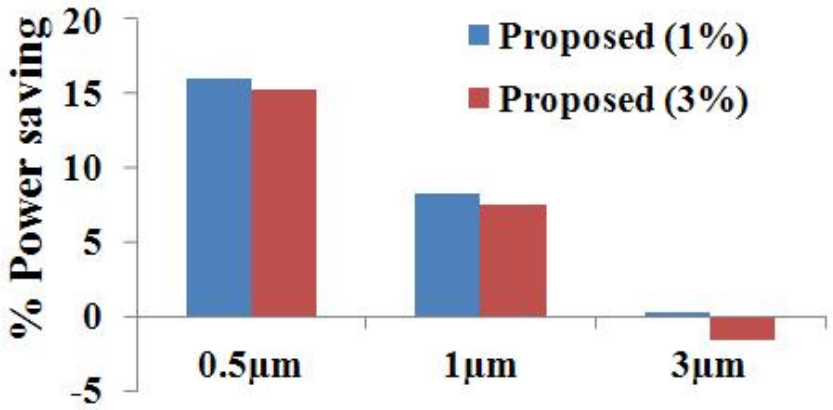


Fig. 5.12. Power saving of proposed methodology with 1% and 3% increase of CLK frequency at different technology nodes

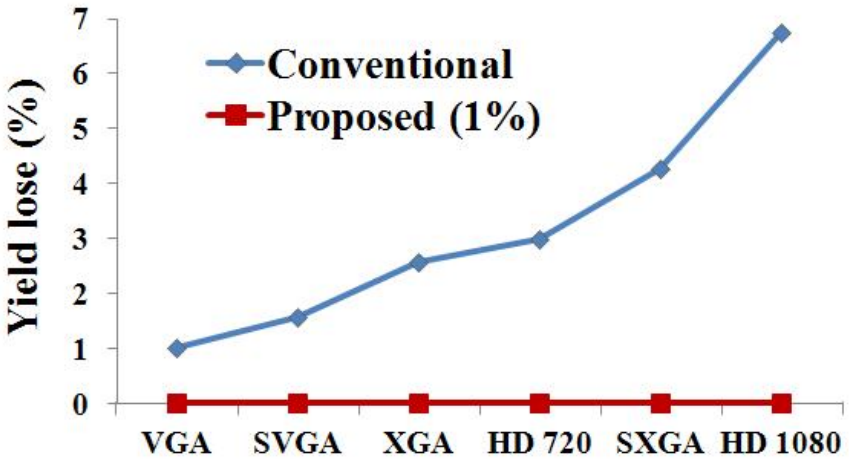


Fig. 5.13. Yield loss of conventional and proposed design with 1% increase of CLK frequency at different resolutions

than being dependent on the supply voltage. Although the simulation result shows small impact in the 3.9 inch panel ($3\mu m$ technology node), it should be noted that the device model used in this work considers only the GB-induced variations. Other important parameters, such as gate oxide thickness, are treated as constants in this model. As other parametric variations are taken into account, larger variations in threshold voltage and mobility can be observed in large sized transistor as shown in the measurement data [100]. Hence, the proposed methodology is expected to still have significant advantages in $3\mu m$ technology node as well. Moreover, as the resolution increases, yield loss due to the process variations becomes significant. Assuming the same probability of defective pixel (at fixed supply voltage), the increased yield loss in high-resolution display with conven- tional design can be seen in Figure 5.13. Compared to the conventional design with the same supply voltage, higher yield can be obtained at the expense of negligible power overhead. Note, the difference of yield losses between the conventional and proposed design is expected to be larger if other parametric variations are included.

In addition, many of the parameters and degradations that affect the voltage margin vary over time and temperature. It results in potential pixel defects to be hidden

in the testing stage while showing up when used by consumers. This undesirable issue keeps bothering manufacturers and consumers and cannot be prevented in conventional design. However, with the proposed circuit, the panel can update the number and location of defective pixels and, hence, achieve self-repair. This is because all the three phases are redone when panel is reset. Hence, better reliability is achieved. The area overhead of the proposed circuit is approximately 1% and hence negligible due to the relatively small number of transistors in the proposed circuit as compared to the number of transistors in pixel array. Furthermore, as the resolution or size of the display increases, the area overhead decreases.

5.5 Conclusions

In this section, a new adaptive design technique for variation tolerant and self-repair display panel is reported. It is shown that the proposed circuit can effectively minimize yield loss caused by process variations while using a decreased supply voltage. This will allow continued scaling of transistor for low power, high pixel density, and integration or to have high yield with very small power overhead. Consequently, we can choose to have lower power consumption for small sized panels in battery-operated electronics which have relatively less variations. Alternatively, we can achieve a higher yield for large panels which suffer from GB-induced variations, where power consumption may not be the most important criteria.

6. THE IMPACT OF HOT CARRIER INJECTION (HCI) ON VOLTAGE CONTROL OSCILLATOR LIFETIME PREDICTION

This section presents a comprehensive study of the impact of Hot Carrier Injection (HCI) on differential LC Voltage Controlled Oscillator (VCO) reliability tests. Although Negative Bias Temperature Instability (NBTI) has been recognized as major cause for reliability degradation of advanced circuits, HCI-induced degradation may become significant due to the accelerated aging of reliability tests leading to incorrect circuit lifetime prediction. To distinguish HCI effects, different stress voltages and frequencies are applied in Constant Voltage Stress (CVS) and Ramp Voltage Stress (RVS) tests. It is verified that the stress voltage and frequency dependence of time and voltage exponents in the reliability tests are due to the effect of HCI. Based on the observed results, a methodology is proposed to define proper stress conditions for accelerated circuit reliability tests for better lifetime prediction.

6.1 Introduction

Aggressive scaling of CMOS technology has provided a significant increase in performance and decrease in power of integrated circuits. However, due to the non-ideal scaling of supply voltage, the increased power density and electric field raise the reliability concerns of advanced circuits. To effectively evaluate the reliability of integrated circuits, elevated voltage (i.e. accelerated aging) is commonly applied in reliability tests, such as Constant Voltage Stress (CVS) and Ramp Voltage Stress (RVS) tests [23]- [24]. The acceleration technique has been commonly applied to predict the device degradation where solely one degradation effect is applied [23], [101]- [102]. However, unlike single device level degradation, circuit level reliability involves di-

verse degradation mechanisms, such as Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI), each with its own temperature, voltage and time dependences [103]- [104]. It is widely recognized that, in nominal operating voltages, NBTI is expected as the dominant degradation mechanism, while HCI can be neglected [105]- [107]. This can be attributed to the fact that HCI requires higher electric field to have "hot" electrons causing damages. Due to the large voltage acceleration factor of HCI [107]- [108], however, HCI-induced degradation is expected to be significant as the stress voltage is increased accordingly. The accelerated aging might shift the dominant degradation mechanism from NBTI to HCI leading to a pessimistic lifetime predictions due to incorrect parameters determined from reliability fits [109]. Therefore, a proper limitation for the accelerated aging is needed for minimizing HCI effects in reliability tests. In this section, a detailed study on the impact of HCI on CVS and RVS tests is presented [25]. By applying different stress conditions, the dependence of degradation slope on stress voltage is observed. Based on the experimental results, it is concluded that HCI-induced degradation is responsible for the change of time and voltage exponents in RVS and CVS tests. Further, a methodology for RVS and CVS tests is suggested to minimize the HCI effects and for better circuit lifetime prediction.

6.2 Experiments

The circuit studied is a basic component of analog circuits, differential LC Voltage Control Oscillator (VCO). The LC VCO is composed of an inductor, voltage-controlled capacitors (varactors), differential pair and frequency dividers, as illustrated in Fig. 6.1. The test circuits were fabricated on silicon-on-insulator (SOI) substrate utilizing a conventional CMOS process flow with gate length of 45nm. Note that, although the tested circuit is based on SOI technology, the conclusions obtained in this study should also apply to TFT-based circuits. In this work, circuit performance parameters, startup voltage (i.e. the minimum supply voltage for oscillation)

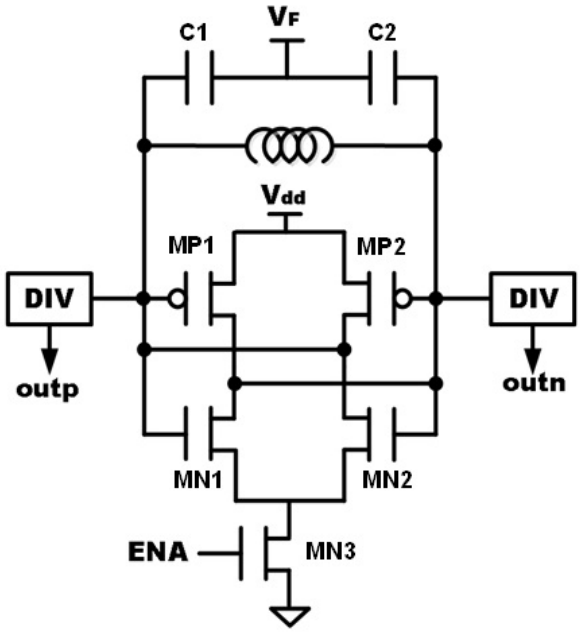


Fig. 6.1. Schematic of testing circuit, LC VCO. The circuit is implemented in 45nm SOI technology.

and operating frequency are selected as circuit aging monitors. The tests of CVS and RVS are based on a measure/stress/measure procedure as shown in Fig. 6.2. In both procedures, the stress was periodically interrupted to monitor startup voltage and operating frequency degradation. Note that both the reliability tests, CVS and RVS, were performed at elevated temperature (60°C).

6.3 Results and Discussions

Previous studies have shown that circuit level reliability degradation follows the same power dependence on time as single device level degradation [109]- [112]. Accordingly, for CVS tests, if dominated by BTI, the circuit performance degradation ($\Delta V_{startup}$ or Δf) is expected to follow the power-law with time and can be empirically expressed as

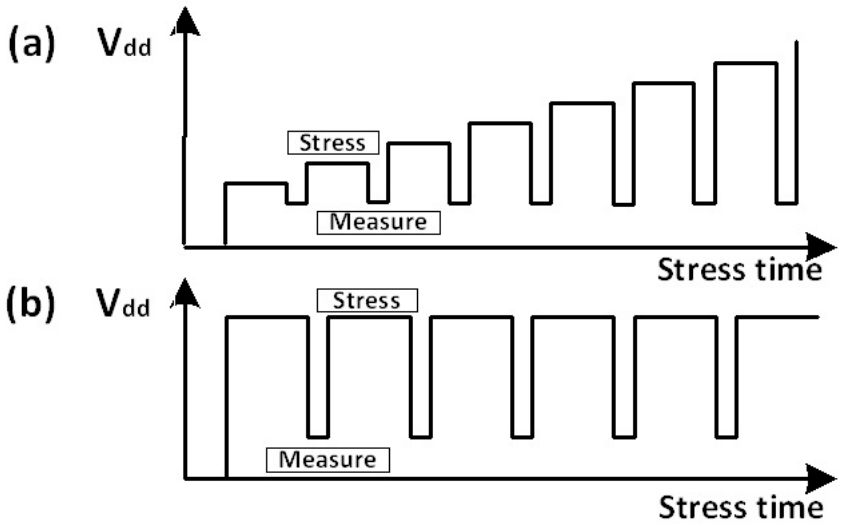


Fig. 6.2. Vdd-time traces for (a) RVS (ramped voltage stress) and (b) CVS (constant voltage stress) tests. Vdd is altered between stress and measurement. Operating frequency and startup voltage is measured to track the evolution of the performance degradation.

$$\Delta V_{startup} or \Delta f = A \cdot t^n \cdot V_{dd}^m \tag{6.1}$$

where A is a prefactor, n and m are time and voltage exponents,respectively. Also, for RVS test, the degradation can be expressed as [23]- [24]

$$\Delta V_{startup} or \Delta f = \frac{A}{RR^n \left(\frac{m+n}{n}\right)^n} {V_{RVSmax}}^{m+n} \tag{6.2}$$

where RR is the ramp rate which is defined as $\Delta V_{dd}/\Delta t$ [23]- [24],V_{RVSmax} is the maximum ramp voltage. Thus, the circuit performance degradation in RVS test is also expected to have power-law dependence on the maximum ramp voltage. To evaluate the circuit lifetime, the parameters [i.e. power-law time (n) and voltage (m) exponents and the prefactor (A)] in RVS and CVS tests are first extracted in accelerated aging conditions for better efficiency. Having the extracted parameters, the circuit lifetime under nominal voltage is then evaluated under the assumption of constant time and voltage exponents for different stress conditions. However, the data

in Fig. 6.3 show that both the startup voltage (Fig. 6.3a) and frequency degradations (Fig. 6.3b) show a break in slope dividing the degradation curve into high and low stress voltage regimes in RVS tests. Further, it can be observed that in the high voltage regime, the slope is higher than that in the low voltage regime. This indicates that the assumption of constant time and voltage exponents $(n + m)$ may not hold true. Based on previous experimental observations, HCI has higher time and voltage exponents than NBTI [107]- [108]. Hence, it can be speculated that the increase in time exponent in high voltage regime is related to HCI-induced degradation. The dominant degradation mechanism may shift from NBTI to HCI as the stress voltage increases.

Except for the value of time and voltage exponents, the other important difference between NBTI and HCI is the frequency dependence. Since the main source of hot carriers is from the drain current, HCI-induced degradation is expected to depend on frequency linearly. Conversely, a weak dependence of NBTI on frequency is experimentally observed in [113]- [114]. Accordingly, to further validate the domination of HCI in high voltage regime, VCOs with different operating frequencies were stressed. The measurements of Fig. 6.4a show that the startup voltage degradation in the low voltage regime has no frequency dependence suggesting negligible HCI impact and the dominance of NBTI. Meanwhile, in the high voltage regime, frequency dependence of degradation can be clearly observed. It is shown that the degradation increases with operating frequency. To examine this frequency dependence, degradation as a function of frequency at V_{stress}=2.6V is plotted in Fig. 6.4b. A clear linear dependence on frequency can be observed which is expected for HCI. Note that the degradation results in Fig. 6.4 also indicate the dependence of break point on operating frequency. Accordingly, it can be expected that the slope break in RVS tests will vary with stressed circuits and can be a good indicator of starting point of HCI dominance.

The impact of HCI stress can also be seen in CVS results. Fig. 6.5a shows the degradation trend of startup voltage with different stress voltages. The degradation

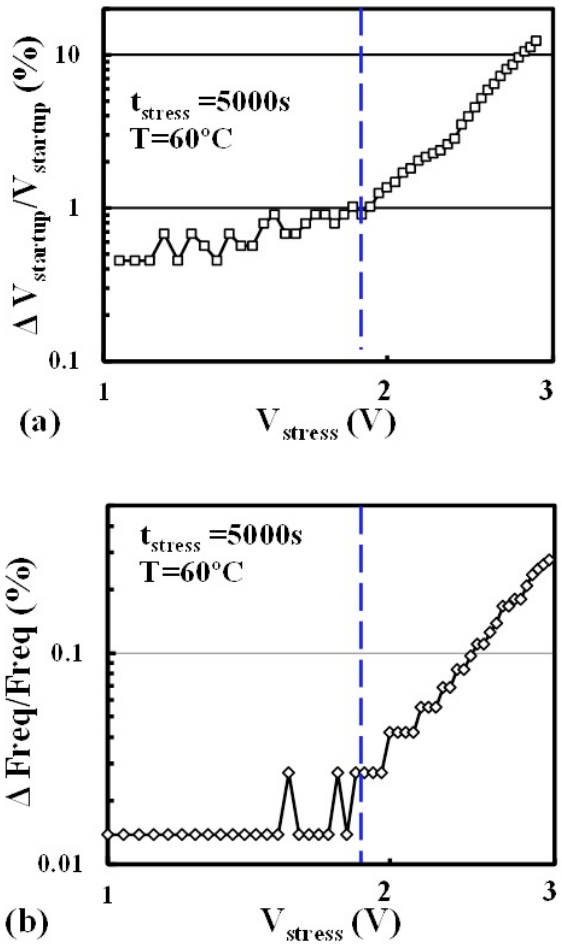


Fig. 6.3. Experimental results for (a) startup voltage degradation and (b) operating frequency degradation in RVS tests. A break in slope divides the degradation curve into high and low stress voltage regimes. The stress temperature is 60°C.

slope (i.e. time exponent n) increases with stress voltage which indicates the increase impact of HCI effects (n_{NBTI}=0.25, n_{HCI}=0.5 [108]). Furthermore, in Fig. 6.5b, one can observe that, for both startup voltage and operating frequency degradations, the time exponent n increases with the stress voltage. Note that the large n is due to the fact that measurements were done with interruption [115]. The impact of operation frequency on the time exponent is shown in Fig. 6.6. The frequency dependence of

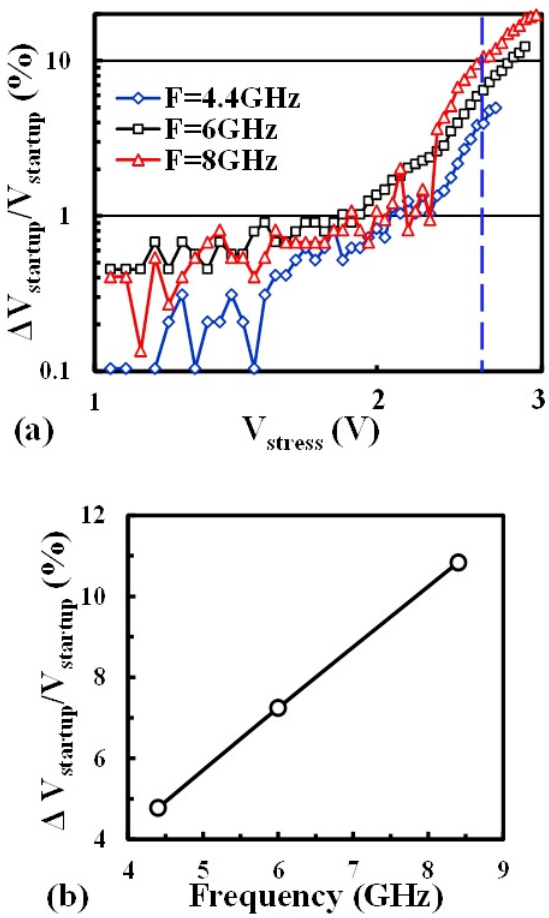


Fig. 6.4. (a) Startup voltage degradation with different operating frequency in RVS tests. Frequency dependence of degradation is shown in high voltage regime. (b) Linear dependence of startup voltage degradation on operating frequency at V_{stress}=2.6V.

the time exponent can be clearly observed which validates the non-negligible of HCI effect in CVS tests.

To further resolve the degradation contribution from HCI and NBTI, the circuit-level reliability simulation tool, RelXpert, which considers both HCI and NBTI effects is used [116]. By properly scaling the predicted degradation amplitude, the simulated degradation trend matches well with RVS experimental data, as shown in 6.7a. In 6.7b, the threshold voltage degradation of the pMOS in the differential pair (i.e. MP1 in 6.1) is decomposed into two factors, NBTI and HCI, by RelXpert. A comparison of

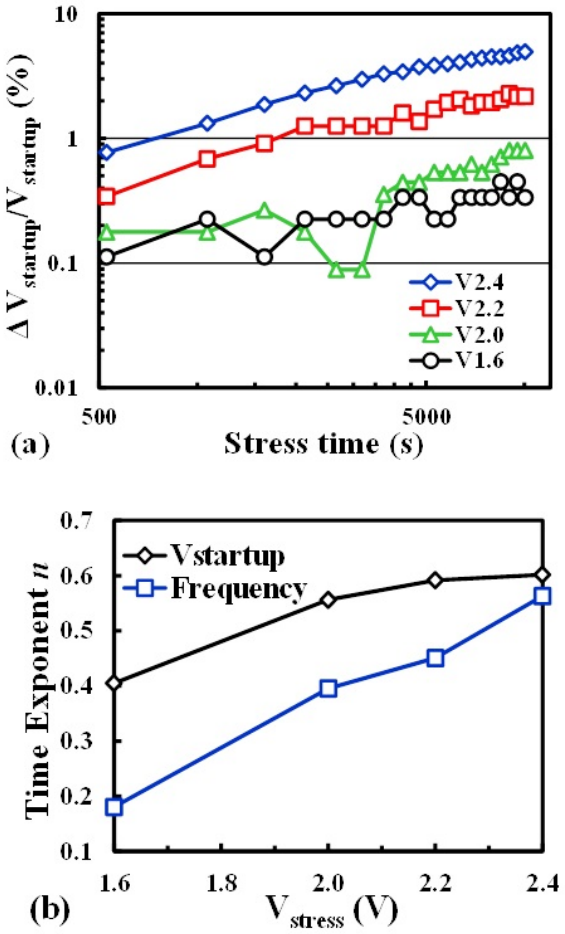


Fig. 6.5. (a) Degradation of startup voltage as function of time for different stress voltages in CVS tests. (b) Time exponent of startup voltage and frequency degradation as function of stress voltage in CVS tests.

these values clearly shows that the degradation due to NBTI is dominant below 2.0V and is surpassed by the HCI-induced degradation at 2.25V which again supports the assumption.

Consequently, it cannot be unconditionally assumed that the effect of HCI can be neglected in accelerated reliability tests. Although the reliability tests will be less efficient, the stress voltage needs to be properly limited for minimizing the impact of HCI. To that effect, we suggested that the break point observed in RVS tests, which

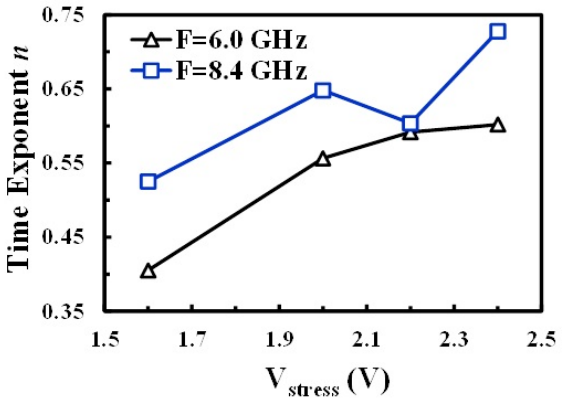


Fig. 6.6. Time exponent of startup voltage as function of stress voltage with different operating frequency in CVS tests.

distinguishes the dominant degradation mechanism and depends on stressed circuits, can be used as guidance for the maximum stress voltage in both RVS and CVS tests.

6.4 Conclusions

In this section, an experimental investigation of HCI impact on reliability tests is presented. We have shown that the stress voltage and frequency dependence of the time and voltage exponents in CVS and RVS tests are due to the impact of HCI. This observation validates that, with accelerated aging in reliability tests, HCI-induced degradation is significant which is contrary to nominal operating condition leading to erroneous reliability evaluation. Based on the experimental results, the break point observed in degradation curves of the RVS test can serve as a guideline to define the proper range of stress voltage in reliability tests for suppressing HCI effect and better lifetime prediction.

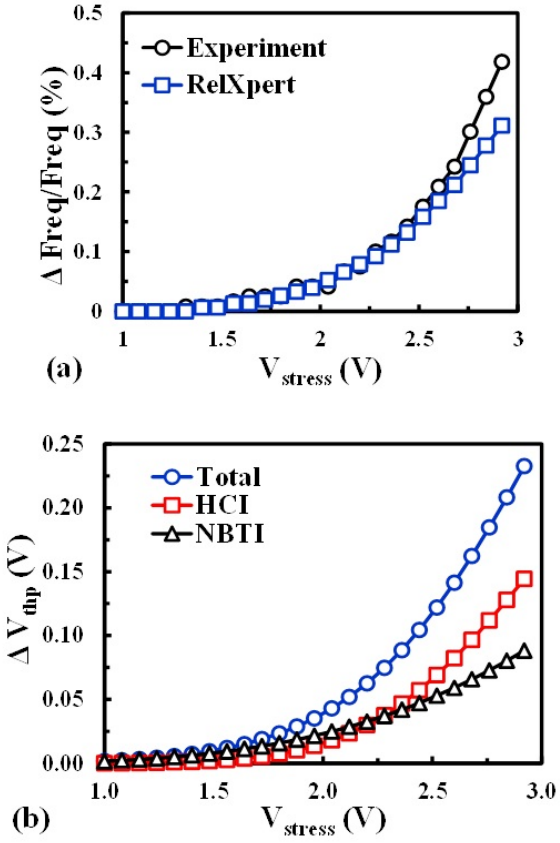


Fig. 6.7. (a) Comparison of frequency degradation from the simulation and the experimental data in RVS test. (b) Comparison of total threshold voltage degradation and HCIinduced and NBTI-induced threshold voltage degradations in the pMOS of differential pair from RelXpert results.

7. SUMMARY

Throughout the thesis, we presented new modeling and design optimization methodologies in different levels of hierarchy (device and circuit) for poly-Si TFT technology. We also proposed a new technique to reduce HCI impact on circuit-level reliability tests. At the device level, we demonstrated that GB-induced V_{th} variation can be properly modeled by simultaneously considering the impact of the number, the position and the orientation of GBs. The model is verified with experimental data and 3-D device simulator. We also show the effectiveness of the proposed model for different technology nodes and crystallization process. For the reliability of poly-Si TFT, we proposed a self-consistent electro-thermal model for self-heating enhanced NBTI. The model consists of a poly-Si TFT device model, NBTI model and thermal-diffusion model. Based on this framework, the significant impact of device geometry, substrate material and thickness on NBTI in poly-Si TFTs are shown. The work reflects on the main obstacles for future flexible electronics and validates the need for integration of thermal-diffusion model and NBTI model for precisely prediction of NBTI-induced degradation in poly-Si TFTs. Furthermore, from the circuit perspective, a pixel circuit for AMOLED display is proposed to address the threshold voltage and mobility variations and the supply voltage degradation. Monte Carlo based statistical analysis shows a smaller spread of drive current in the proposed pixel circuit as compared to that of prior pixel circuit. In addition, a self-repair and variation tolerant circuit is proposed for LCD and OLED display. We have shown that the proposed circuit can effectively minimize yield loss while using a lower supply voltage. Finally, for circuit-level reliability tests, we found that the break point observed in degradation curves of RVS tests can serve as a guideline to define the proper stress range for accelerated aging. With the proposed methodology, HCI effect in reliability tests can be suppressed leading to a better lifetime prediction. These works facilitate poly-Si

TFT technology for advanced circuits and make poly-Si TFT technology more attractive for new applications, such as flexible displays, biosensors, and smart clothing, as compared to conventional bulk Si technology.

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VITA

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