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Non-Silicon MOSFETs and Circuits with Atomic Layer Deposited Higher-k Dielectrics

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NON-SILICON MOSFETS AND CIRCUITS WITH ATOMIC LAYER
DEPOSITED HIGHER- κ DIELECTRICS

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Submitted to the Faculty

of

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Lin Dong

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West Lafayette, Indiana

To my beloved parents Qingchi Dong and Juxiang Cai, and my wife Man Wang.

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ABSTRACT

Dong, Lin Ph.D., Purdue University, December 2013. Non-Silicon MOSFETs and Circuits with Atomic Layer Deposited Higher- κ Dielectrics. Major Professor: Peide Ye.

The quest for technologies beyond 14 nm node complementary metal-oxide-semiconductor (CMOS) devices has now called for research on higher- κ gate dielectrics integration with high mobility channel materials such as III-V semiconductors and germanium. Ternary oxides, such as $\text{La}_{2-x}\text{Y}_x\text{O}_3$ and LaAlO_3 , have been considered as strong candidates due to their high dielectric constants and good thermal stability. Meanwhile, the unique abilities of delivering large area uniform thin film, excellent controlling of composition and thickness to an atomic level, which are keys to ultra-scaled devices, have made atomic layer deposition (ALD) technique an excellent choice. In this thesis, we systematically study the atomic layer epitaxy (ALE) process realized by ALD, ALE higher-k dielectric integration, GaAs nMOSFETs and pMOSFETs on (111)A substrates, and their related CMOS digital logic gate circuits as well as ring oscillators. A record high drain current of 376 mA/mm and a small SS of 74 mV/dec are obtained from planar GaAs nMOSFETs with 1 μ m gate length. $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}(111)\text{A}$ interfaces are systematically investigated in both material and electrical aspects. The work has expanded the near 50 years GaAs MOSFETs research to an unprecedented level. Following the GaAs work, Ge n- and p-MOSFETs with epitaxial interfaces are also fabricated and studied. Beyond the conventional semiconductors, the complex oxide channel material SrTiO_3 is also explored. Well-

behaved $\text{LaAlO}_3/\text{SrTiO}_3$ nMOSFETs with a conducting channel at insulating ALD amorphous LaAlO_3 - insulating crystalline SrTiO_3 interface are also demonstrated.

1. INTRODUCTION

1.1 CMOS scaling down and novel technologies

The Si CMOS has begun its journey of the seemingly endless scaling in pursuit of higher speed and less power consumption following the later proposed Moores Law by Gordon Moore ever since the first pointed-contacted transistor was invented back in 1947. In the past few decades, the number of transistors integrated in one single chip kept growing in an astonishing speed, which is caused by the continuous device size shrinking and non-stopping introduction of innovative technologies. The continuous device miniaturization (or device scaling down) leads to device performance and production improvement in all aspects: function, speed, power dissipation, reliability, cost and productivity. However, more and more challenges emerged while the scaling of the Silicon CMOS is finally approaching its fundamental limits. By looking at the International Technology Roadmap for Semiconductors (ITRS, <http://www.itrs.net/Links/2012ITRS/Home2012.htm>), some of the novel technologies to address the challenges are:

1. High carrier mobility substrates. Fig. 1.1 shows the novel technologies that will be potentially applied in the future device applications. III-V materials generally possess higher electron mobility (μ_e), lower effective mass (m^*), and smaller bandgap (E_g) than Si, while Ge has much higher hole mobility (μ_h) than Si as shown in Table Table 1.1. This makes III-V/Ge promising for high-speed low-power logic applications.

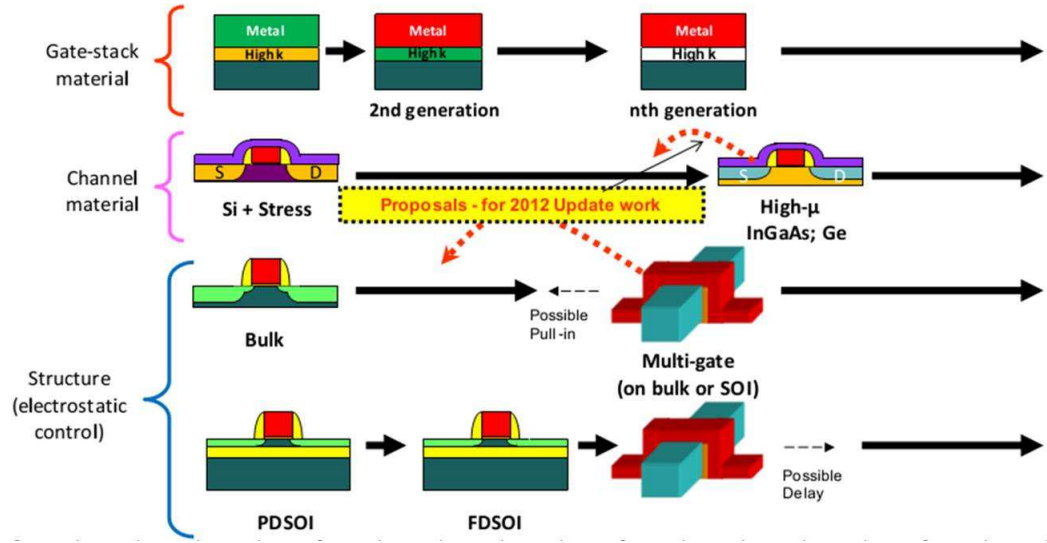


Fig. 1.1. 2011 ITRS equivalent scaling process technologies including high mobility channel materials, high- κ gate dielectrics and novel device structures.

Table 1.1

Carrier transport properties and energy bandgaps of semiconductor materials of interest under room temperature.

	Si	Ge	GaAs	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	InP	GaSb	InSb
μ_e ($\text{cm}^2/\text{V}\cdot\text{s}$)	≤ 1400	≤ 3900	≤ 8500	≤ 12000	≤ 5400	≤ 3000	$\leq 7.7 \cdot 10^4$
μ_h ($\text{cm}^2/\text{V}\cdot\text{s}$)	≤ 450	≤ 1900	≤ 400	≤ 300	≤ 300	≤ 850	≤ 1250
E_g (eV)	1.12	0.66	1.42	0.74	1.34	0.73	0.17

2. The integration of higher dielectric constant dielectrics. The dielectrics in the future should have proper κ value, thermodynamical stability and the ability of forming high quality oxide-semiconductor interfaces on high mobility substrates. SiO_2 gate dielectric oxide layer is reaching its physical limit (0.7 nm or 2 monolayers) with continuous scaling down. In order to reduce the gate

leakage current, high dielectric constant oxides are widely studied. With high- κ gate dielectric layer the equivalent oxide thickness (EOT) can be lower than the fundamental physical thickness limitation of SiO_2 while maintaining much higher physical thickness, as can be seen from the equation below:

$$EOT = \frac{\kappa_{\text{SiO}_2}}{\kappa_{\text{high}-\kappa}} t_{\text{high}-\kappa} + t_{\text{low}-\kappa IL} \quad (1.1)$$

where κ is the dielectric constant and t stands for the film thickness. Numerous dielectrics have been extensively investigated by researchers like binary oxides Al_2O_3 [1–3], HfO_2 [4, 5] and ZrO_2 [6, 7], however, some of them have relative low dielectric constant ($\kappa_{\text{Al}_2\text{O}_3} \sim 9$), and some suffer from low crystallization temperature ($T_{\text{crystallization}} < 500^\circ\text{C}$ for HfO_2 and ZrO_2), which make them unsuitable for future CMOS application.

3. Novel device structures. Multigate and gate-all-around structures are to be introduced on III-V/Ge technology similar to its Si counterpart to meet the requirement of channel electrostatic control at 14 nm technology node. The natural advantages of most III-V semiconductors like smaller bandgap, larger permittivity and smaller effective mass make them promising candidates to replace silicon for short channel devices. Some previous results have shown that the scaling of planar InGaAs MOSFETs has stopped below 150 nm due to severe short channel effects. [8, 9] Therefore the novel structures will be significant in the ultimate III-V technology. Evolution of InGaAs multi-gate device structures from bulk planar to fully gate-all-around structure greatly improved control of short channel effect over planar and thin-body devices.

1.2 High- κ dielectrics and Atomic Layer Deposition

The oxide with high- κ dielectric constants, such as LaAlO_3 , LaLuO_3 , LaYO_3 and so on, have been considered as strong candidates to replace SiO_2 , mainly due to their high dielectric constant, better thermodynamic stability than binary high- κ oxides and reasonable band offsets with semiconductors. Encouraging progresses have been made by different groups previously [10–12], showing a very promising future of complex oxide application in CMOS industry.

Atomic Layer Deposition (ALD) or Atomic Layer Epitaxy (ALE) is an ultrathin-film deposition technique based on sequences of self-limiting surface reactions, which enables thickness control on the atomic scale. Its unique advantages such as excellent conformality, accurate and simple thickness control and large area uniformity make ALD an indispensable technique tool in CMOS manufacture.

A ALD process is a gas phase deposition process employing sequential gas pulses containing chemical reagents called precursors. In most deposition processes two precursors are involved and alternating precursor sequences are sent into the reactor chamber. To better describe the ALD process, an example below illustrates the deposition of aluminum oxide (Al_2O_3 or alumina) on semiconductor surface with hydroxyl (-OH) termination. The ALD cycle starts with the injection of trimethylalumina (TMA, $\text{Al}(\text{CH}_3)_3$) precursor into the ALD reactor. The gas precursor carries out self-limiting chemical reactions at the target surface, in this case a hydroxylated surface. As described in the first three steps in fig. 1.2, the surface is saturated with $\text{O-Al}(\text{CH}_3)_2$ termination when reaction with TMA is complete. Following the first precursor pulse is a nitrogen (N_2) purge step designated to remove the remaining TMA and methane gas. After the purge step a second precursor, gas phase H_2O (water vapor), is sent into the reactor to continue the oxidation of aluminum atoms (Al) until the methyl termination is replaced completely by hydroxyl termination.

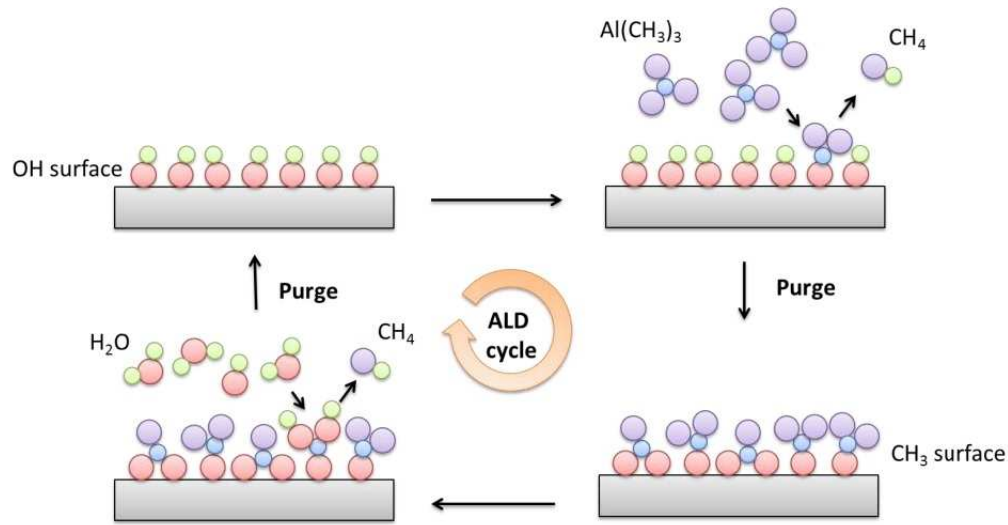


Fig. 1.2. Schematics of aluminum oxide deposition by ALD technique.

At the end of the cycle on the last step, the surface is covered by one mono-layer of aluminum oxide with the same hydroxylated surface as in the beginning of the ALD cycle. After another nitrogen purge, the cycle is then repeated again to deposit another oxide layer on the surface of the target sample. The number of ALD cycles usually gives an accurate estimate of the deposited mono-layers and hence the film thickness. There are several advantages of the ALD technique which make it the primary choice for depositing high-k gate oxide on semiconductor substrates. ALD films are highly conformal and pinhole free. Uniform films can be grown on steep trenches and various surface contours. Secondly, the number of ALD cycles reflects the number of mono-layers deposited, enabling precise control of film thickness down to a fraction of an angstrom. And since the mono-layers are chemically bonded to each other and the substrate, ALD films are very robust both electrically and mechanically. The ALD technique was introduced to the 45 nm CMOS technology since 2007 firstly by Intel. The success of ALD high-k oxide on silicon provides an encouraging baseline

for integrating high quality, high-k dielectric on III-V semiconductors and opens new possibilities for compound semiconductor device research.

1.3 Thesis outline

The thesis starts with the study of La-based higher- κ oxide on high mobility substrates with Atomic Layer Deposition (ALD) in chapter 2, most of the work are focused on the material and electrical characterizations of the $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}(111)\text{A}$ epitaxial interfaces, where x varies from 0 to 0.9. The density of traps at the epitaxial interface is extracted and compared using the room temperature conductance method, and thermal stability of the epitaxial $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}(111)\text{A}$ interface is systematically studied.

In chapter 3, epitaxial La-based higher- κ oxide integration in the GaAs enhancement-mode MOSFETs are carefully investigated with the experimental demonstration of GaAs(111)A n- and p-MOSFETs devices. Two types of La-base gate dielectrics, $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ and La_2O_3 epitaxial oxides are employed in the MOSFETs fabrication. GaAs CMOS circuits including inverters, NAND and NOR logic gates and five-stage ring oscillators are also demonstrated. The GaAs devices and circuits are systematically studied with the electrical characterization and analysis.

In chapter 4, Ge nMOSFETs and pMOSFETs with epitaxial $\text{La}_2\text{O}_3/\text{Ge}(111)$ interfaces are experimentally demonstrated. By the analysis of the electrical properties of the Ge devices, process fabrication optimizations are also discussed.

In chapter 5, Well-behaved $\text{LaAlO}_3/\text{SrTiO}_3$ nMOSFETs with a conducting channel at insulating ALD amorphous LaAlO_3 - insulating crystalline SrTiO_3 interface are demonstrated. Four types of interfaces are investigated by the comparison of SrTiO_3 transistors electrical properties. At last Metal-Insulator-Transition phenomenon is presented and corresponding mechanism is also discussed.

In the summary and outlook chapter, the entire research in this thesis are briefly summarized and some possible further works are discussed.

2. STUDY OF LA-BASED HIGHER- κ OXIDE ON HIGH MOBILITY SUBSTRATES WITH ATOMIC LAYER DEPOSITION

2.1 Introduction

High-mobility GaAs and InGaAs MOSFETs have shown promising performance compared to Si-based devices for high-speed complementary MOS (CMOS) logic applications. However, GaAs MOS devices suffer from Fermi-level pinning, which is mainly due to the high trap density of states at the oxide/GaAs interface [13, 14]. In this section, the deposited epitaxial layer of higher-k dielectric oxide La_2O_3 and $\text{La}_{2-x}\text{Y}_x\text{O}_3$, on GaAs(111)A, are systematically studied in both material and electrical aspects.

Usually, the dielectric oxide is either amorphous or polycrystalline, and therefore a high density of dangling bonds exists at the oxide/GaAs interface. These dangling bonds form interface states in the midgap [15], which trap carriers and produce a large frequency dispersion of capacitance and Fermi-level pinning. Growing an epitaxial oxide dielectric layer on GaAs to form the MOS devices with a heteroepitaxial structure is a good approach to reduce the density of the interface dangling bonds, since a perfect epitaxial interface is supposed to have no dangling bonds, and therefore the interface trap density of states D_{it} should be small. Also, contrary to polycrystalline oxides, a perfect epitaxial oxide should contain no grain boundaries [16], which preserves the desired features of the low leakage current and uniformity. However, growing epitaxial oxides on GaAs is rather challenging, since GaAs is neither chemically stable nor thermally stable: GaAs can be oxidized easily to form low quality

surface oxides that compromise the interface quality [17]; and GaAs starts to lose As over 400°C [18]. Hong et al [19,20]. have demonstrated a method of using in-situ electron beam evaporation to grow epitaxial $(\text{Ga,Gd})_2\text{O}_3$ or Gd_2O_3 layers on GaAs(100) with the epitaxial relationships $(110)\text{Gd}_2\text{O}_3//(\text{100})\text{GaAs}$, $[001]\text{Gd}_2\text{O}_3//[011]\text{GaAs}$, and $[-110]\text{Gd}_2\text{O}_3//[01-1]\text{GaAs}$. Their capacitance-voltage measurements do show a significant decrease in D_{it} [20], which suggests the importance of epitaxy in reducing interfacial defects [21]. However, the frequency dispersion of the capacitance was still fairly large [20], and the transistor characteristics of the inversion-mode MOSFETs made from $(\text{Ga,Gd})_2\text{O}_3/\text{GaAs}$ were not very impressive [22]. This may be due to the relatively large in-plane mismatch between Gd_2O_3 and GaAs (1.9 % and -3.9% in the $[011]$ and $[01-1]$ directions of GaAs, respectively). Getting MOSFETs even of this quality also requires that there is no air-break between growth of the GaAs and the oxide, so that complex multi-chamber MBE systems are necessary. Several follow-up structural analyses of $\text{Gd}_2\text{O}_3/\text{GaAs}(100)$ [23–25] revealed that perfect strained epitaxy only occurs in the first few layers. When the oxide film thickness exceeds 3 nm, the Gd_2O_3 film starts to relax by generating misfit dislocations, so that the film is no longer perfectly epitaxial [20]. Unfortunately, simply substituting Gd_2O_3 with other lanthanide sesquioxides cannot accommodate the mismatch simultaneously in two orthogonal in-plane directions, since the in-plane lattice spacing of Gd_2O_3 GaAs is greater than GaAs in one direction but smaller in the other. Very recently, epitaxial growth of cubic high-k oxide, LaLuO_3 , on GaAs(111)A has been achieved by an ex-situ atomic layer deposition (ALD) process in our group. The heteroepitaxy relationship was found to be $(111)\text{LaLuO}_3//(\text{111})\text{GaAs}$ ($\alpha\text{LaLuO}_3 \approx 2\alpha\text{GaAs}$) with a relaxed interface [26]. Since the (111) plane has a three-fold symmetry, the in-plane mismatch between oxide and GaAs can be simultaneously engineered with lanthanide sesquioxides that have appropriate cation sizes. Initial electrical characterizations

showed quite promising results, as the MOS capacitors made from epitaxial ALD LaLuO₃/GaAs showed an order of magnitude reduction in interface trap density ($D_{it} \sim 7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) compared with amorphous ALD Al₂O₃/GaAs ($8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$). But, still LaLuO₃ has a fairly large lattice mismatch with respect to GaAs (-3.8%), and another concern is that Lu is one of the rarest elements on earth, which would be problematic for large scale fabrication.

2.2 Atomic Layer Deposition experimental process and methods

La₂O₃ and La_{2-x}Y_xO₃ films were grown by ALD from precursors including lanthanum tris(N,N-diisopropylformamidinate), yttrium tris(N,N-diisopropylacetamidinate) and H₂O in a home-built tube reactor. The pure La₂O₃ films were deposited by alternately supplying the La precursor vapor and water at a deposition temperature of 385 °C, and the ternary La_{2-x}Y_xO₃ oxides were deposited by repeatedly growing one or multiple cycles of La₂O₃ followed by one or multiple cycles of Y₂O₃ at 300 °C. A schematic illustration of the Atomic Layer Epitaxy can be found in Fig. 2.1.

The exposures of the La and Y precursors were estimated to be 0.003 Torr s and the exposure of H₂O was 0.06 Torr s in each cycle. After each H₂O pulse, the chamber was purged under nitrogen flowing for 80 s to minimize the amount of water and/or hydroxyl groups trapped in the oxide films, as they considerably degrade the crystallinity and permittivity and cause large frequency dispersion. By controlling the cycle ratio of La₂O₃ and Y₂O₃, the elemental composition of the ternary oxide La_{2-x}Y_xO₃ (i.e. x) can be tuned. In this letter, two cycle ratios of (La:Y)_{cyc} = 1:3 and 3:1 were used, and their compositional ratios, which were determined by Rutherford backscattering spectroscopy, were (La:Y)_{comp} = 1.1:0.9 and 1.8:0.2, respectively. Before depositing La_{2-x}Y_xO₃ on the GaAs(111)A substrates, all the GaAs substrates were first dipped into a 3M HCl solution to remove the native oxide and then soaked in

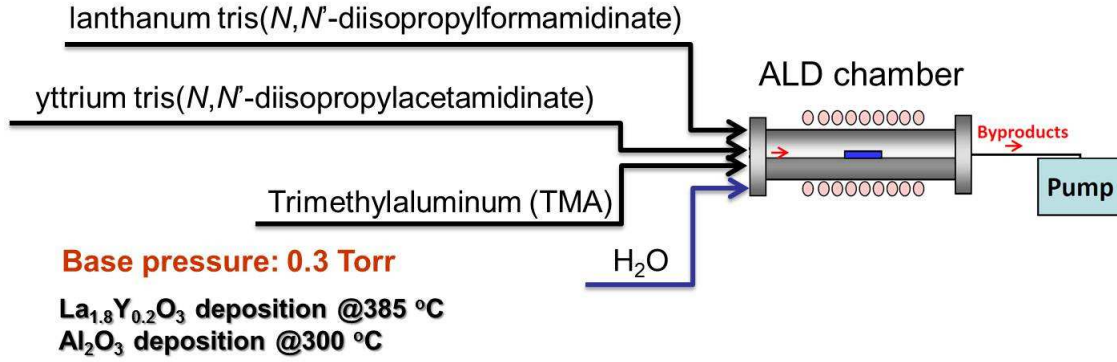


Fig. 2.1. Schematic illustration of the Atomic Layer Epitaxy process. The epitaxial La_{2-x}Y_xO₃ oxide film is deposited at 385 °C while the amorphous Al₂O₃ oxide encapsulation layer is grown at 300 °C. The relative long time purging during the process is the key to realize uniform and single crystalline oxide structure. The base pressure of the deposition is maintained at around 0.3 Torr.

a 10% (NH₄)₂S solution for 20 min for sulfur-passivation. Cross-sectional TEM images were taken with JEOL 2100. HRXRD spectra were taken by a Bruker D8 HRXRD with the incident beam Cu K1 being monochromated by a Ge (022) × 4 asymmetric monochromator. Due to the hygroscopic nature of La_{2-x}Y_xO₃, all the films for HRXRD analysis were capped by a 6 nm in-situ ALD Al₂O₃ layer before being taken out from the deposition chamber. For characterizing the electrical properties, n-type and p-type GaAs(111)A wafers with doping concentration of 5-7 × 10¹⁷ cm⁻³ were used as the substrates. To fabricate MOS capacitors, either 7.5 nm La_{2-x}Y_xO₃ (for x = 0.9 and 0.2) or 9 nm La₂O₃ was first deposited on the GaAs substrates, and then an in-situ ALD layer of 6.5 nm Al₂O₃ was deposited on top to prevent the hygroscopic La_{2-x}Y_xO₃ from being exposed to air. All the La_{2-x}Y_xO₃/GaAs capacitors were subjected to rapid thermal annealing (RTA) at 800 °C for 30 s in N₂ ambient. Capacitors with amorphous ALD Al₂O₃ as the dielectric material (Ni/8nm Al₂O₃/GaAs(111)A) were fabricated for comparison. The Al₂O₃/GaAs(111)A capacitors were subjected to

RTA at 600 °C for 30 s in N₂ ambient. Ni/Au circular electrodes for MOS capacitors were patterned by a lift-off process with a diameter of 150 μm . The capacitance-voltage/conductance-voltage measurements were carried out at room temperature by using an HP4284A precision LCR meter with frequency varying from 1kHz to 1MHz.

2.3 GaAs/oxide epitaxial atomic structures

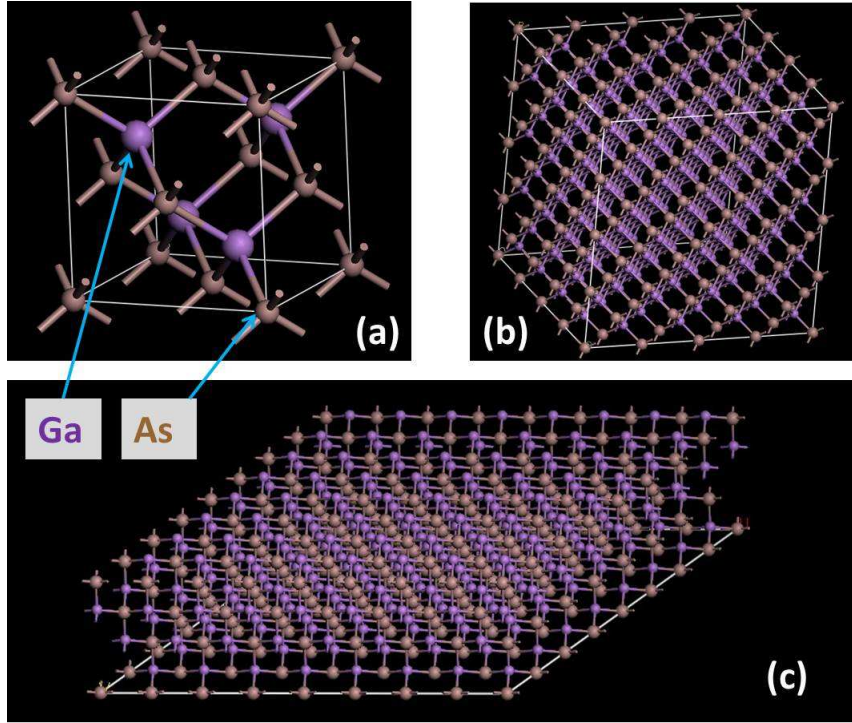


Fig. 2.2. (a) A typical GaAs zincblende lattice unit cell with (100) surface. The purple and brown balls represent Ga and As atoms, respectively (b) A GaAs super lattice with $4 \times 4 \times 4$ GaAs unit cell. (c) Illustration of GaAs(111)A surface with Ga termination.

The GaAs, as a typical III-V semiconductor, has a *zincblende* structure, as shown in Fig. 2.2 (a). It can be described as two interpenetrating fcc (Face-centered cubic) lattices, that is, a Ga fcc lattice is displaced along the one-quarter of the body diagonal direction relative to an As fcc lattice. In fact the *zincblende* structure is

essentially identical to the *diamond* structure (like Silicon), except that lattice sites are apportioned equally between Ga and As atoms. [27] The GaAs(111)A surface (Ga atom terminated surface) is exhibiting quite different properties with respect to the GaAs(100) surface. For example, the GaAs(111)A tends to be hydrophilic due to its Ga-As dipoles at the very top layer while the GaAs(100) surface favors hydrophobicity immediately after HCl wet etching. [28]

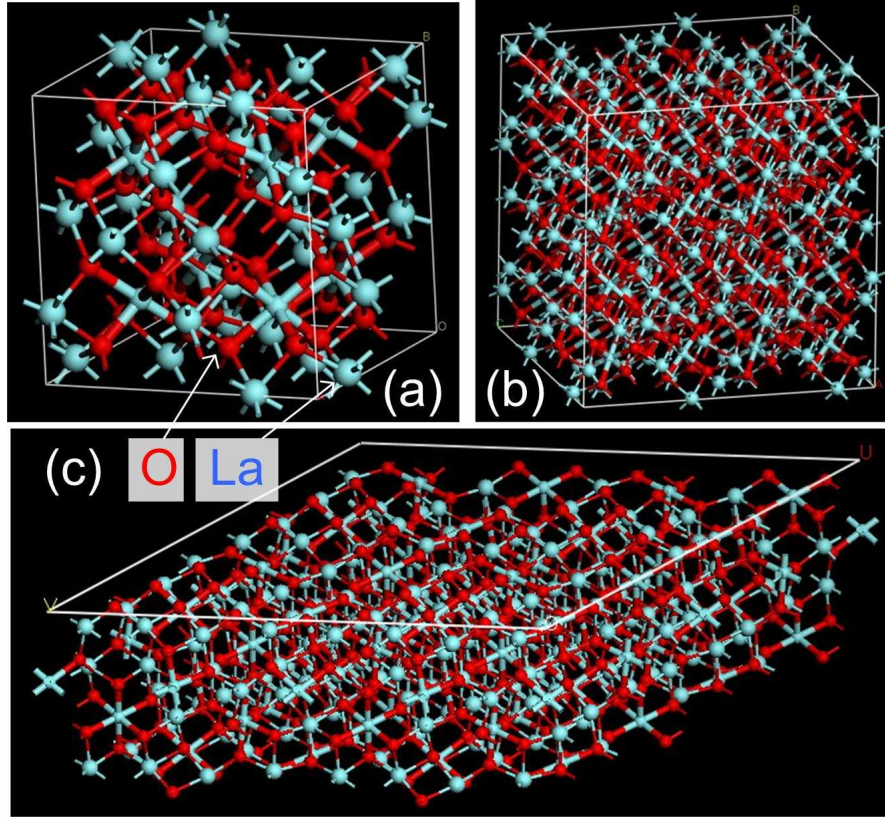


Fig. 2.3. (a) An atomic structural view of a La_2O_3 cubic cell. The light blue and red balls represent La and Oxygen atoms, respectively (b) A La_2O_3 super lattice with $2 \times 2 \times 2$ La_2O_3 unit cell. (c) Illustration of $\text{La}_2\text{O}_3(111)$ surface with Oxygen termination.

Similarly, we may construct the La_2O_3 super lattice with the single cubic La_2O_3 cell, as illustrated in Fig. 2.2. Here a $2 \times 2 \times 2$ La_2O_3 structure is employed for good lattice match with GaAs due to the lattice constant relationship of $\alpha\text{La}_2\text{O}_3 \approx 2\alpha\text{GaAs}$.

By cleaving the supper lattices along the (111) surface and proper aligning them together, the $\text{La}_2\text{O}_3/\text{GaAs}$ epitaxial interface structures are illustrated in Fig. 2.4. The hexagonal structure can be clearly observed through the (111) plane and atoms of upper La_2O_3 and GaAs in the lower level are well aligned, from the top view of the epitaxial interface structure in Fig. 2.4(c). The chemical bonds formed between oxygen and gallium atoms right at the interface are strong, and the well aligned epitaxial structure can effectively reduce dangling bond at the interface, leading to a robust and high quality GaAs- La_2O_3 interface.

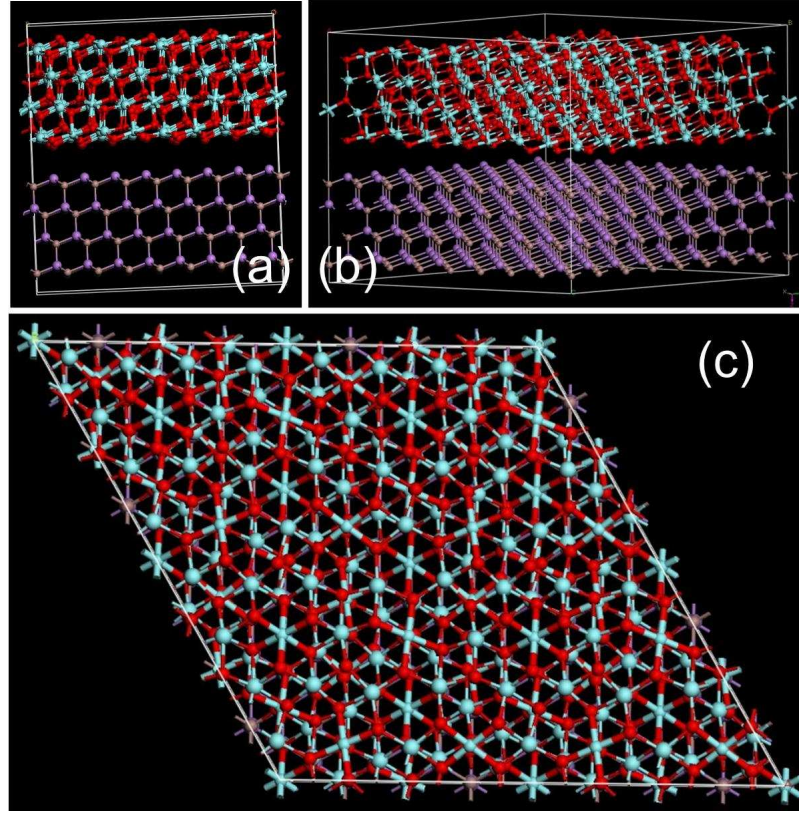


Fig. 2.4. (a) and (b) Atomic structural views of the epitaxial interface between La_2O_3 and GaAs. (c) A top view of the stacked atomic structure of epitaxial interface between La_2O_3 and GaAs, the hexagonal structures can be clearly observed.

2.4 Atomic Layer Epitaxial (ALE) interface material and electrical property study

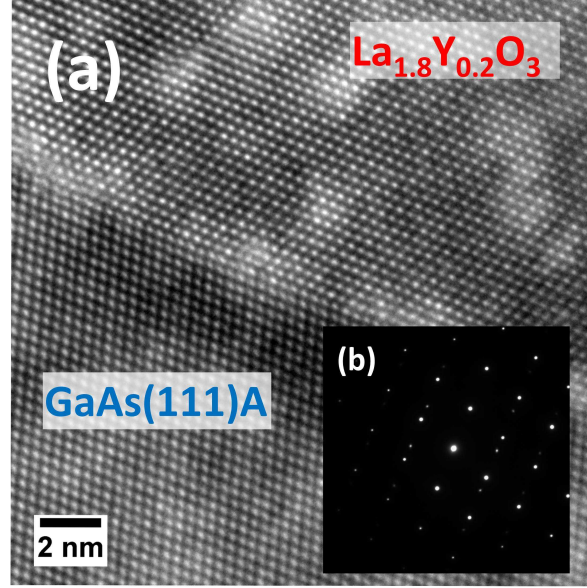


Fig. 2.5. (a) Cross-sectional TEM image of $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ interface, and (b) the corresponding electron diffraction pattern with the electron beam aligned along the $[011]$ direction of GaAs.

In this section, we report an ALD process for depositing another high-k oxide, $\text{La}_{2-x}\text{Y}_x\text{O}_3$, epitaxially on GaAs(111)A. The k value of $\text{La}_{2-x}\text{Y}_x\text{O}_3$ was reported as high as 27, and the terrestrial elemental abundance of Y is much higher than Lu in the Earth. The ternary oxide, $\text{La}_{2-x}\text{Y}_x\text{O}_3$, can be considered as a mixture of La_2O_3 and Y_2O_3 . The lattice constant of cubic La_2O_3 is very slightly larger than 2 times the GaAs lattice constant, while the lattice constant of cubic Y_2O_3 is $\sim 6\%$ smaller than that of La_2O_3 . Therefore, we can adjust the lattice constant of the ternary compound, $\text{La}_{2-x}\text{Y}_x\text{O}_3$, to study the effect of mismatch by varying the ratio of La and Y. As an ALD process grows films in a layer-by-layer manner, the compositional ratio of these two cations can be tuned by varying the cycle ratio of growing

La_2O_3 and Y_2O_3 . A high-resolution X-ray structural analysis indicates a high-quality heteroepitaxy of $\text{La}_{2-x}\text{Y}_x\text{O}_3$ on GaAs(111)A, and electrical measurements on MOS capacitors show a promisingly small frequency dispersion of capacitance and a low $D_{it} \sim 2 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ in the GaAs bandgap close to the conduction band edge. In addition, our process tolerates an air-break between growth of the GaAs and ALD of the epitaxial oxide. ALD is known to produce uniform films over large areas with good reproducibility [29], so we believe that this process is very promising for large scale manufacturing.

$\text{La}_{2-x}\text{Y}_x\text{O}_3$ films were grown by ALD from precursors including lanthanum tris(N,N-diisopropylformamidinate), yttrium tris(N,N-diisopropylacetamidinate) and H_2O in a home-built tube reactor. In particular, pure La_2O_3 or pure Y_2O_3 films can be made by using the corresponding single metal precursor source. When films were deposited on amorphous SiN_x substrates, the as-deposited pure La_2O_3 and pure Y_2O_3 films were polycrystalline in their cubic phases, respectively. But alloying these two oxides did not form a polycrystalline film on amorphous SiN_x , on which the $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$ film was almost amorphous. However, when $\text{La}_{2-x}\text{Y}_x\text{O}_3$ films were grown on GaAs (111)A, the as-deposited films, including La_2O_3 , $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$, and $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$, were all well crystallized and, in fact, they were highly epitaxial due to induction by the substrates. Cross-sectional transmission electron microscopy (TEM) of $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}$ interfaces indicates a cube-on-cube epitaxy with a twin boundary relation at the interface, and the interface is flat and sharp. A representative TEM image of a $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ sample is shown in Fig. 2.5(a). The twin boundary relation at the oxide/GaAs was also confirmed by the selective area electron diffraction pattern as shown in Fig. 2.5(b), where the two sets of diffraction patterns belonging to cubic-phase $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ and GaAs are well aligned vertically. Especially, the diffraction spot of GaAs (111) overlaps with the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ (222) spot, suggesting that the

cubic lattice constant of $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ is very close to twice that of GaAs. However, TEM does not have enough resolution to determine precisely the small difference between their lattice constants. Therefore, high-resolution X-ray diffraction (HRXRD) was used to investigate the detailed epitaxial structure.

Coupled $2\theta - \omega$ HRXRD scans were performed for the oxide/GaAs(111)A samples. The peaks from the GaAs substrate were used as the internal references, and the oxide/GaAs lattice mismatch, which is defined as $(\alpha_{\text{oxide}} - 2\alpha_{\text{GaAs}})/2\alpha_{\text{GaAs}}$, was calculated from the relative shift of the oxide peak with respect to the GaAs peak, assuming a fully relaxed heteroepitaxy relation at the interface.¹¹ For the $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3/\text{GaAs}$ sample, the coupled $2\theta - \omega$ scan clearly shows both peaks of the GaAs(111) and $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3(222)$ reflections, as shown in Fig. 2.6(a). The corresponding ω rocking curves of GaAs(111) and $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3(222)$ reflections have a similar shape with the same full width at half maximum of $\sim 32^\circ$. This indicates a high quality heteroepitaxy of $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3/\text{GaAs}$ over a large area (several mm^2). The 2θ angle of the $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3(222)$ peak was found to be 0.958° greater than that of the GaAs(111) peak, which corresponds to a lattice mismatch of -3.32% for $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$ with respect to GaAs. For the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}$ sample, the $2\theta - \omega$ scan (Fig. 2.6(b)) shows that the peaks of GaAs(111) and $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3(222)$ are much closer, indicating $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ has a smaller lattice mismatch to GaAs. Thus, we performed a $2\theta - \Delta\omega$ reciprocal space mapping (RSM) on this sample, and the RSM contour is plotted in the inset of Fig. 2.6(b), where the contour levels are chosen to highlight the peaks. The 2θ angle of the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3(222)$ peak was found to shift by $+0.18^\circ$ from the GaAs(111) peak, indicating a lattice mismatch of -0.64% for $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ with respect to GaAs. As for the $\text{La}_2\text{O}_3/\text{GaAs}$ sample, the peaks of GaAs(111) and $\text{La}_2\text{O}_3(222)$ in the $2\theta - \omega$ scan were found to be entirely overlapping with each other, as shown in Fig. 2.7. Therefore, we performed another $2\theta - \omega$ scan

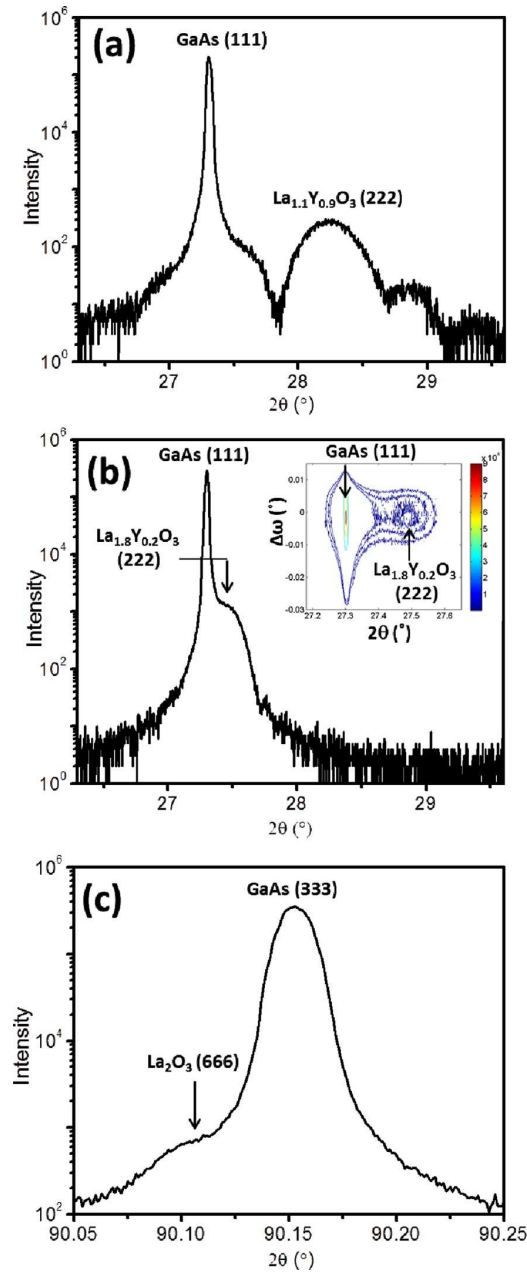


Fig. 2.6. HRXRD couples 2θ - ω scans of (a) $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$, (b) $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$, and (c) La_2O_3 on GaAs(111)A. The scans of (a) and (b) were performed around the GaAs(111) reflection, and the scan of (c) was performed around the GaAs(333) reflection. The inset of (b) shows the 2θ - $\Delta\omega$ reciprocal space map around the GaAs(111) peak for the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}$ sample.

around the GaAs(333) reflection to determine the mismatch with greater sensitivity. As shown in Fig. 2.6(c), the 2θ angle of the $\text{La}_2\text{O}_3(222)$ peak was only 0.046° smaller than that of the GaAs(333) peak, suggesting a much smaller lattice mismatch of only $+0.04\%$ for La_2O_3 with respect to GaAs.

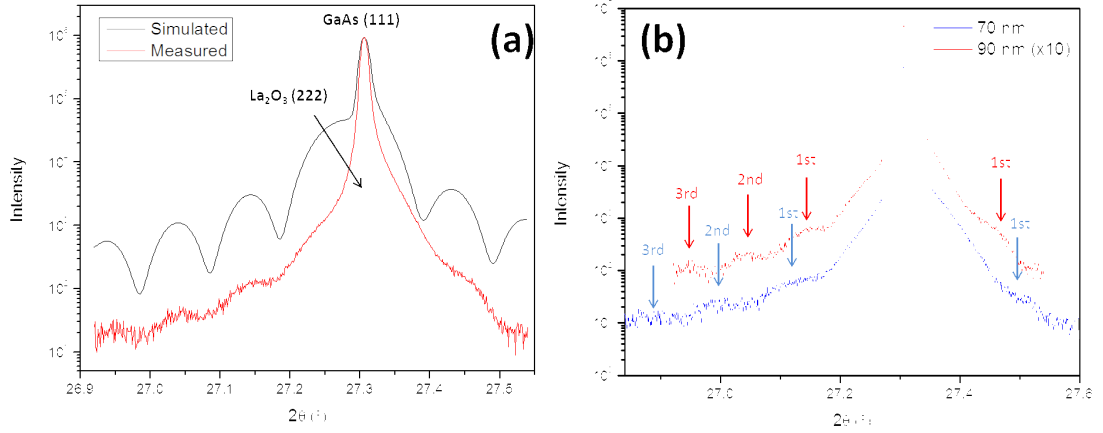


Fig. 2.7. (a) HRXRD coupled $2\theta - \omega$ scan of a 90 nm La_2O_3 film grown on GaAs(111)A, compared with a simulated diffraction curve from LEPTOS (Bruker). (Lattice mismatch used in simulation was $+0.037\%$ for $\text{La}_2\text{O}_3/\text{GaAs}$.) The good matching of the Laue oscillations indicates that the main peak of $\text{La}_2\text{O}_3(222)$ is indeed overlapping with GaAs (111). (b) By the comparing the $2\theta - \omega$ curves measured on two $\text{La}_2\text{O}_3/\text{GaAs}$ samples with different thickness (70 nm and 90 nm), we noticed that all of the side-band peaks shifted, suggesting that these side-band peaks all belong to the thickness fringes (Laue oscillations) of the $\text{La}_2\text{O}_3(222)$ main peak. This again indicates that the $\text{La}_2\text{O}_3(222)$ main peak is overlapping with GaAs (111) peak.

In summary of the above structural analysis, both of the TEM and HRXRD results suggested a high-quality heteroepitaxy relation of $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}(111)\text{A}$ ($x = 0, 0.2$ and 0.9) with smaller lattice mismatch for higher La-content oxide. The measured lattice mismatch approximately follows Vegards law Fig. 2.8.

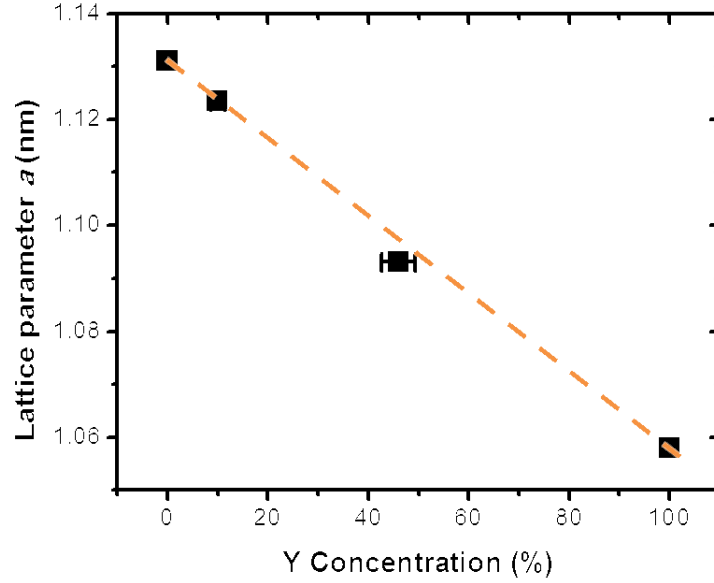


Fig. 2.8. Vegards law plot of the lattice parameters of $\text{La}_{2-x}\text{Y}_x\text{O}_3$. The Y concentration was determined by Rutherford backscattering spectroscopy. The obtained lattice constants of La_2O_3 and Y_2O_3 are comparable with the reference values.

In addition, we also found that pure Y_2O_3 on GaAs(111)A is also epitaxial. Therefore we believe that epitaxy can be achieved for mixed $\text{La}_{2-x}\text{Y}_x\text{O}_3$ oxides with any La:Y ratio. This epitaxial relation is quite similar to the $\text{LaLuO}_3/\text{GaAs}(111)\text{A}$ case.

Since epitaxial $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}$ structures are expected to provide a better interface quality with a lower interface trap density for electrical devices, we fabricated the corresponding $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}$ MOS capacitors to examine the electrical properties. Both p-type and n-type MOS capacitors of $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}(111)\text{A}$ ($x = 0, 0.2$ and 0.9) were fabricated and characterized by capacitance-voltage (C-V) and conductance-voltage (G-V) methods [2]. Due to the hygroscopic nature of $\text{La}_{2-x}\text{Y}_x\text{O}_3$, an in-situ ALD capping layer of 6.5 nm Al_2O_3 was deposited right after the deposition of $\text{La}_{2-x}\text{Y}_x\text{O}_3$ on GaAs(111)A. Capacitors with only amorphous ALD Al_2O_3 as the

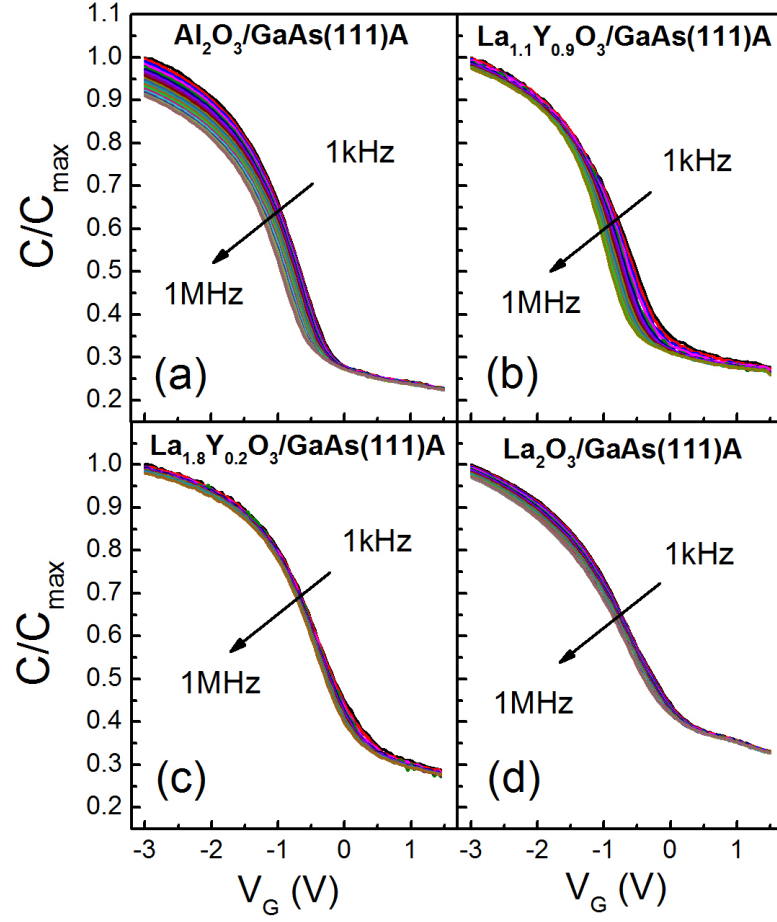


Fig. 2.9. C-V characteristics of p-type GaAs MOS capacitors with stacks of (a) Ni/8nm Al_2O_3 /GaAs(111)A, (b) Ni/6.5 nm Al_2O_3 /3/7.5 nm $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$ /GaAs(111)A, (c) Ni/6.5 nm Al_2O_3 /7.5 nm $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ /GaAs(111)A, and (d) Ni/6.5 nm Al_2O_3 /9 nm La_2O_3 /GaAs(111)A, respectively.

dielectric material (Al_2O_3 /GaAs(111)A) were also fabricated for comparison. The C-V response was measured at room temperature with the frequency of the small AC signal ranging from 1 kHz to 1 MHz. Fig. 2.9 and Fig. 2.10 shows the normalized C-V curves measured on these capacitors. A general trend for the frequency dispersion is that the capacitors with amorphous Al_2O_3 dielectric show the largest frequency dispersions compared with the capacitors with epitaxial $\text{La}_{2-x}\text{Y}_x\text{O}_3$ dielectric, and,

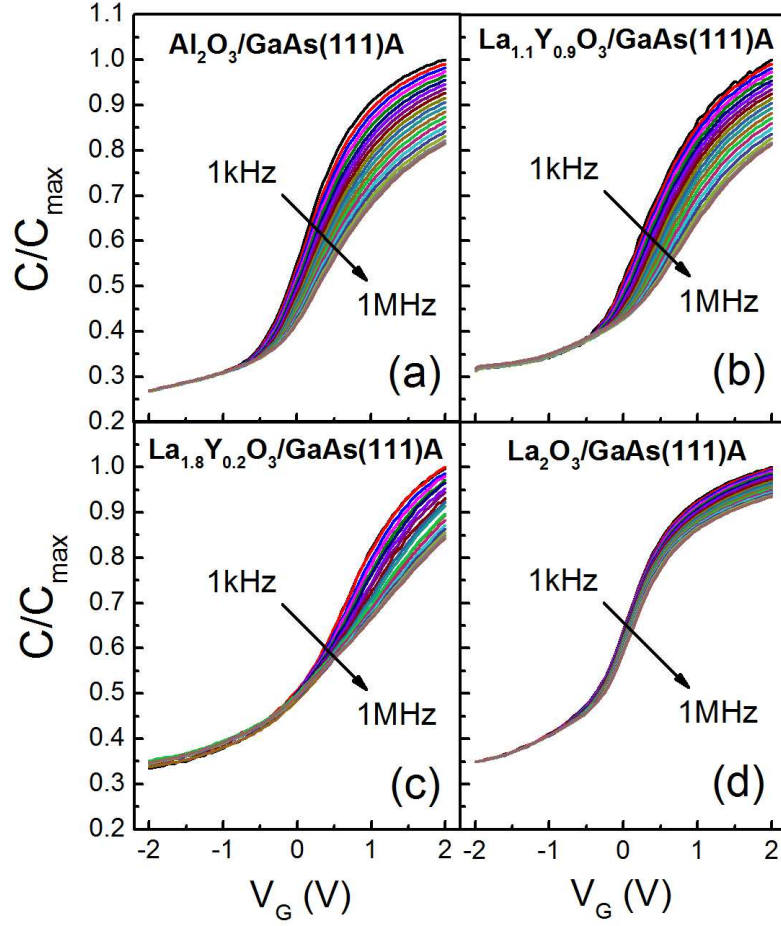


Fig. 2.10. C-V characteristics of n-type GaAs MOS capacitors with stacks of (a) Ni/8nm Al_2O_3 /GaAs(111)A, (b) Ni/6.5 nm Al_2O_3 /7.5 nm $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$ /GaAs(111)A, (c) Ni/6.5 nm Al_2O_3 /7.5 nm $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ /GaAs(111)A, and (d) Ni/6.5 nm Al_2O_3 /9 nm La_2O_3 /GaAs(111)A, respectively.

among these $\text{La}_{2-x}\text{Y}_x\text{O}_3$ capacitors, those with smaller lattice-mismatch $\text{La}_{2-x}\text{Y}_x\text{O}_3$ (higher La content) show smaller frequency dispersion. For p-type GaAs MOS capacitors, the frequency dispersion in the accumulation region ($\Delta C/C_{\text{max}}$) is reduced from 7.6% to 2.4% by replacing the amorphous Al_2O_3 with epitaxial $\text{La}_{2-x}\text{Y}_x\text{O}_3$ as the dielectric (2.5%, 1.9% and 1.7% for $x = 0.9, 0.2$ and 0 , respectively), and with a better lattice-matched oxide, La_2O_3 , the dispersion in the depletion region ($V_G = 0$) is further

reduced. A similar trend was also observed for the n-type GaAs MOS capacitors: Al_2O_3 shows the largest frequency dispersion of 19.0% in the accumulation region, and $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$, $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$, and La_2O_3 show decreasing frequency dispersions of 18.6%, 15.6%, and 9.9%, respectively.

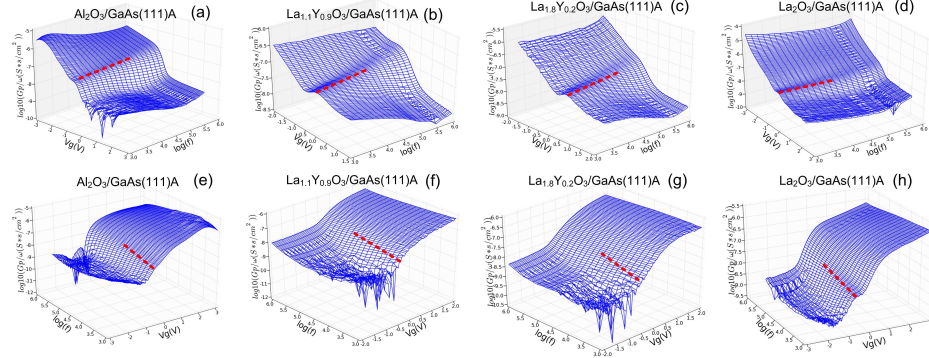


Fig. 2.11. Frequency-dependent conductance-voltage (G_p/ω vs V_g/f) plots measured on p-type and n-type (a, e) $\text{Al}_2\text{O}_3/\text{GaAs}$, (b, f) $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3/\text{GaAs}$, (c, g) $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}$, and (d, h) $\text{La}_2\text{O}_3/\text{GaAs}$ MOS capacitors.

We also measured the D_{it} by the conductance-voltage method. The distribution of D_{it} within the GaAs band gap is plotted in Fig. 2.12. Consistent with the C-V results, the interface of the amorphous $\text{Al}_2\text{O}_3/\text{GaAs}$ showed much larger interface trap density compared to the epitaxial $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}$ cases. Among these epitaxial $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}$ cases, the $\text{La}_2\text{O}_3/\text{GaAs}$ capacitor with a lattice-almost-matched interface showed the smallest D_{it} on the order of $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, and in particular, the interface trap density in the upper half of the band gap is below $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ in the whole region measured. Notice that typically the D_{it} close to the conduction band edge is quite high for other oxides on GaAs, and those traps severely pin the Fermi level. The traps hinder the Fermi level from moving away from the center of the bandgap up to the conduction band edge, preventing the realization of high-performance inversion-mode GaAs MOSFETs. With a lattice-matched La_2O_3

dielectric layer, a very good interface with low trap density was achieved. The decreasing trend of D_{it} with smaller lattice mismatch indicates the importance of matching the lattice constant of oxide with GaAs. In addition, the k values of $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3$, $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$, and La_2O_3 were estimated from the capacitance to be 20, 22, and 16, respectively. The above excellent electrical results show that the epitaxial $\text{La}_{2-x}\text{Y}_x\text{O}_3$ is a very promising gate dielectric candidate material for future high-performance GaAs MOS devices [30].

2.5 Summary

To Conclude, in this chapter, we demonstrated an ex-situ ALD process of growing epitaxial $\text{La}_{2-x}\text{Y}_x\text{O}_3$ on GaAs(111)A. High-quality epitaxy of $\text{La}_{2-x}\text{Y}_x\text{O}_3/\text{GaAs}(111)\text{A}$ was achieved for $x = 0$ (i.e. pure La_2O_3), 0.2 and 0.9. GaAs MOS capacitors made from this epitaxial structure showed very good interface quality with small frequency dispersion and low interface trap densities. In particular, the $\text{La}_2\text{O}_3/\text{GaAs}$ interface, which has a lattice mismatch of only 0.04%, showed very low D_{it} in the GaAs bandgap of below $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ near the conduction band edge. The $\text{La}_2\text{O}_3/\text{GaAs}$ capacitors also showed the lowest frequency dispersion of any dielectric on GaAs. This is the first achievement of such low trap densities for oxides on GaAs. We believe that these new results will expand the nearly 50-year research on the oxide/GaAs interface to an unprecedented level.

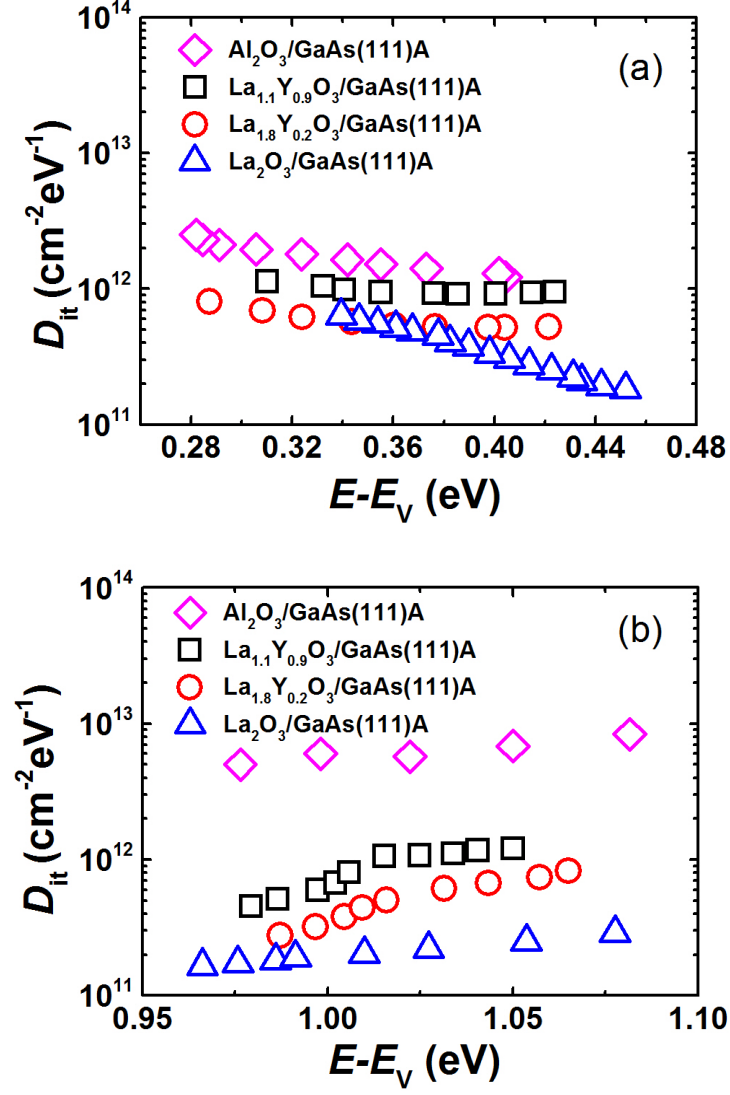


Fig. 2.12. D_{it} distribution in GaAs band gap obtained on both (a) p-type and (b) n-type MOS capacitors with $\text{Al}_2\text{O}_3/\text{GaAs}(111)\text{A}$, $\text{La}_{1.1}\text{Y}_{0.9}\text{O}_3/\text{GaAs}(111)\text{A}$, $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ and $\text{La}_2\text{O}_3/\text{GaAs}(111)\text{A}$ as the interfaces, respectively.

3. DEMONSTRATION OF HIGH PERFORMANCE GAAS CMOS DEVICES AND CIRCUITS ENABLED BY LA-BASED HIGHER- κ EPITAXIAL DIELECTRICS

3.1 GaAs(111)A MOSFETs nMOSFETs and pMOSFETs with $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs(111)A}$ epitaxial interface

3.1.1 Introduction

As we have discussed in the introduction, along with the device scaling and performance improving continues, silicon CMOS technology is approaching its fundamental physical limits. Meanwhile, III-V semiconductors have gained more and more attention, as they are promising candidates for replacing silicon owing to their high electron mobility and high saturation velocity [14].

GaAs inversion-mode MOSFET is a historically difficult problem since its first publication in 1965 [31]. In order to achieve a thermodynamically stable dielectric on GaAs with a low interface trap density [32], tremendous efforts have been made by different passivation techniques [33–36]. We previously demonstrated superior device performance of GaAs(111)A over GaAs(100) surface [37]. A higher mobility on InGaAs(111)A surface was also reported [38]. In this chapter, using atomic layer epitaxy (ALE) for the first time [26], we demonstrated high performance GaAs inversion-mode NMOSFETs with a single crystalline semiconductor-single crystalline oxide interface. The maximum drain current reaches 326 mA/mm for 0.5 μm gate length device with a low subthreshold swing (SS) of 97mV/dec. Systematic study of C-V and G-V characteristics confirms that this novel epitaxy has excellent quality of

interface, and it is thermally stable for the fabrication process of the inversion-mode GaAs NMOSFETs.

3.1.2 $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ Epitaxial Structure Study

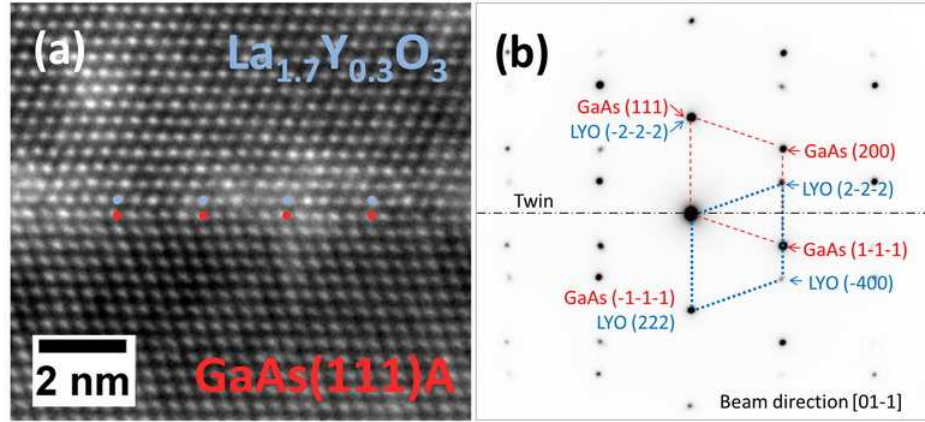


Fig. 3.1. (a) High-resolution cross-section TEM picture of a $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ epitaxial interface. A flat and sharp interface (denoted by red and blue dots) can be observed. (b) The electron diffraction pattern taken from the same cross-sectional TEM sample along the (110) zone axis.

High-resolution cross-section TEM picture taken from the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ single crystalline-single crystalline epitaxial interface is shown in Fig. 3.1. It can be observed that a clear and sharp semiconductor-oxide interface is formed, indicating a well lattice-matched epitaxial structure. The figure on the left of Fig. 3.1 is the electron diffraction pattern taken from the same TEM sample along the (110) zone

axis. The diffraction pattern clearly shows the crystalline structure of the cubic phase $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ oxide on top of the GaAs(111)A substrate.

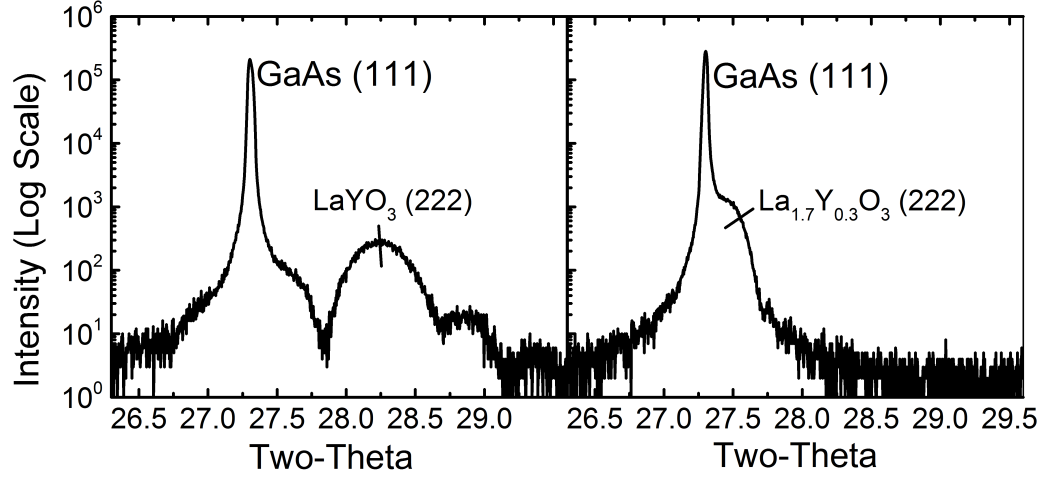


Fig. 3.2. High-resolution X-ray omega-two theta coupled scan for (a) LaYO_3 and (b) $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ on GaAs(111)A. The partial overlap of GaAs(111) and $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ (222) peaks indicates they are lattice-matched better than GaAs (111) and LaYO_3 .

The epitaxy structure is further confirmed by High resolution X-Ray Diffraction results shown in Fig. 3.2, The coupled $2\theta - \omega$ scans performed on the samples with 40 nm $\text{La}_x\text{Y}_y\text{O}_3$ on GaAs(111)A (Fig. 3.2) suggest that the lattice mismatches of $\text{La}_x\text{Y}_y\text{O}_3$ on GaAs(111)A are -3.32% and -0.67% for LaYO_3 and $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$, respectively, if relaxed epitaxy is assumed.

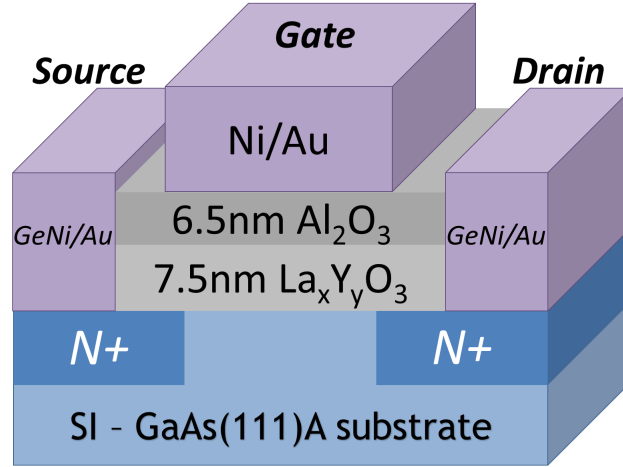


Fig. 3.3. Schematic view of an inversion-mode NMOSFET on a semi-insulating GaAs(111)A substrate with ALE $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ as gate dielectric.

3.1.3 Epitaxial $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs(111)A}$ interface enabled high performance GaAs nMOSFETs study

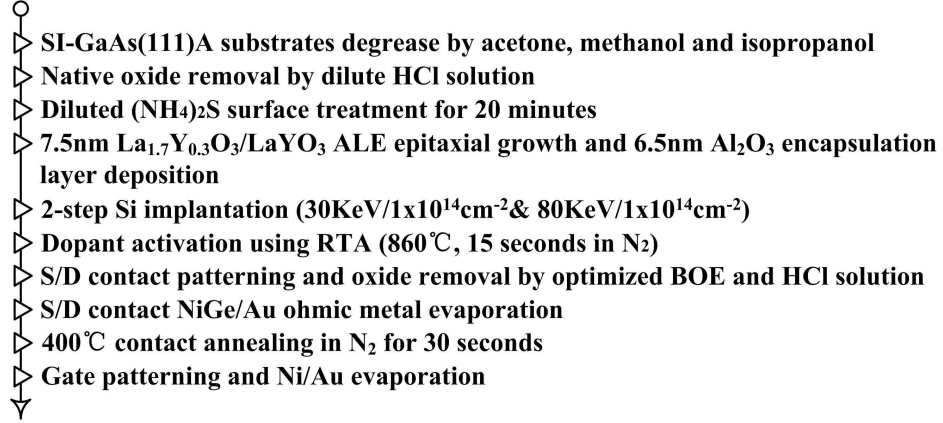
GaAs(111)A Inversion Mode NMOSFETs Device Structure and Fabrication

Figure 3.3 shows the schematic view of a GaAs(111)A NMOSFET fabricated in this work. The device fabrication started with semi-insulating (SI) GaAs(111)A substrates. The samples were degreased by acetone, methanol and isopropanol sequentially, then diluted hydrochloride acid ($\text{HCl} : \text{H}_2\text{O} = 1 : 3$) was used to etch away the surface native oxide, which is well known to cause high density of states at the semiconductor-oxide interface. After etching, the samples were dipped in $(\text{NH}_4)_2\text{S}$ solution (10% $(\text{NH}_4)_2\text{S}$) for 20 minutes so that the surface dangling bonds can be passivated, and they were quickly transferred into ALD chamber within 2 minutes. The deposition involves precursors including lanthanum tris(N,N -diisopropylformamidinate),

yttrium tris(N,N-diisopropyl-acetamidinate) and H_2O at $300^\circ C$. Uniform epitaxial layers were grown by the employment of long purging times (40s~80s).

Table 3.1

Process sequence for the fabrication of GaAs(111)A NMOSFETs. 7.5nm $LaYO_3$ or $La_{1.8}Y_{0.2}O_3$ was epitaxially grown by ALE, forming a single crystalline oxide-single crystalline semiconductor interface, whose electrical quality could be further improved by a high temperature annealing.



We studied the epitaxial high-k gate dielectric $La_xY_yO_3$ with two atomic ratios here, $x:y = 1:1$ and $x:y = 1.8:0.2$. Al_2O_3 6.5nm thick was deposited as a capping layer to prevent any reaction between $LaYO_3$ and air, the Al_2O_3 growth was completed using trimethylaluminum and water as Al and O precursors also at $300^\circ C$. With photolithography, the samples were patterned and sent out for ion-implantation. In order to reduce contact resistance, optimized 2-step Si ion-implantation ($1 \times 10^{14} cm^{-2}$ at 30keV and $1 \times 10^{14} cm^{-2}$ at 80keV) was performed. Dopant activation was done in a Minipulse RTA system, samples were annealed for 15 secs at $860^\circ C$ in N_2 ambient. Source and drain areas were then patterned by photolithography and GeNi/Au was evaporated as contact metal to form Ohmic contact. A contact annealing at $420^\circ C$ in N_2 for 30 seconds process was followed. Finally gate region was patterned, Ni/Au

evaporation was done in a CHA metal evaporation system following by a lift-off process. The complete process flow is also depicted in Table 3.1.

GaAs(111)A nMOSFET Devices characterization

A well behaved output characteristic of a $0.5\mu\text{m}$ -gate-length inversion-mode GaAs(111)A NMOSFET with $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{Al}_2\text{O}_3$ gate dielectric is demonstrated in Fig. 3.8, exhibiting a maximum drain current of 326 mA/mm with $V_{DS} = 2\text{V}$ and $V_{GS} = 5\text{V}$. The device on-current drivability is better than the GaAs(100) devices with silicon interfacial layer passivation [39], silane + ammonia surface passivation [40] and $\text{Gd}_2\text{O}_3(\text{Ga}_2\text{O}_3)$ oxide passivation [41] due to the lattice matching epitaxial interface.

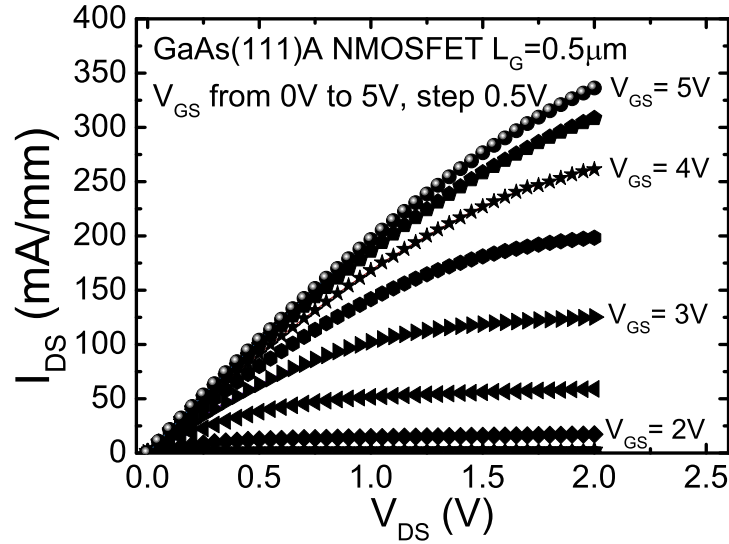


Fig. 3.4. Output characteristic ($I_{DS} \sim V_{DS}$) for a $L_G=0.5\mu\text{m}$ GaAs(111)A NMOSFET with $\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ as gate dielectric.

The transfer characteristics and gate leakage current from the same GaAs(111)A NMOSFET are plotted in Fig. 3.5. A SS of $\sim 97\text{mV/dec}$ is obtained with an $\text{EOT} \sim 4.5\text{ nm}$ at $V_{DS} = 50\text{mV}$, indicating a low mid-gap interface trap density. The on-off ratio

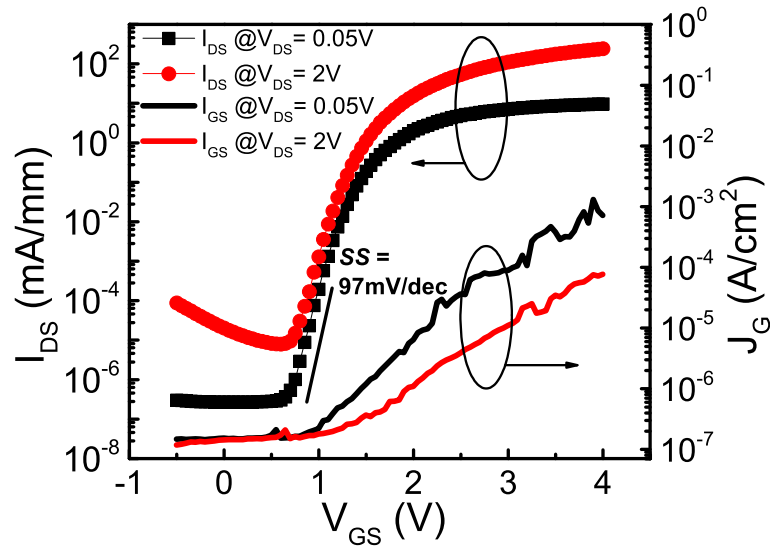


Fig. 3.5. Transfer characteristic ($I_{DS} \sim V_{GS}$) and gate leakage current density (J_G) for the same device of Fig. 3.4.

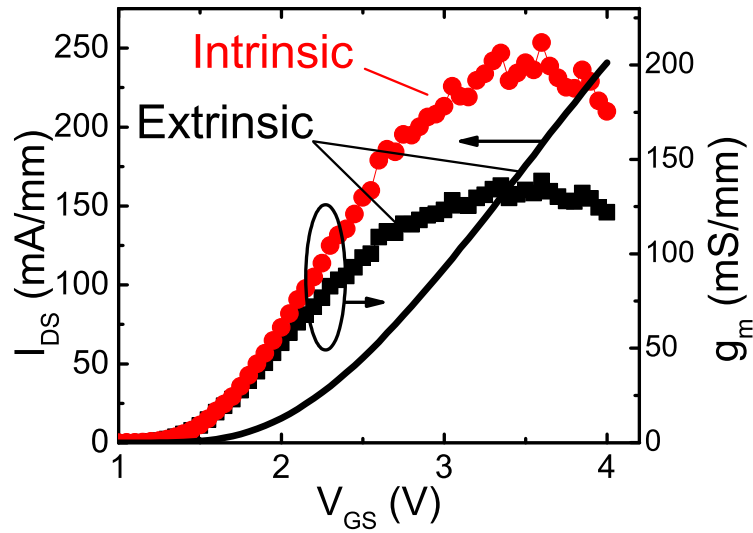


Fig. 3.6. Transfer characteristic, extrinsic and intrinsic transconductance (G_m) versus V_{GS} for the same device of Fig. 3.4.

is as high as 10^7 owing to the high on-current and low reverse junction leakage. The gate leakage current starts to increase when gate bias is larger than 1V because the high temperature annealing employed in the fabrication process (860°C for 15 seconds in N_2) resulted in the partial crystallization of the 6.5nm Al_2O_3 capping layer on top, however, the leakage current density at high V_{GS} bias ($\sim 10^{-3}$ A/cm²) is much smaller than the requirements in the ITRS roadmap. The extrinsic peak G_m is about 140 mS/mm, and the intrinsic G_m is about 210 mS/mm after correction with the series resistance obtained from Fig. 3.7. The R_{SD} extracted from Channel resistance (R_{CH}) versus gate length (L_G) under different gate biases (V_{GS}) in the linear region ($V_{DS}=10$ mV) on GaAs(111)A NMOSFETs with different L_G . The relative large R_{SD} (2.5Ω·mm) can be further improved by optimization of ion implantation and Source/Drain metal engineering. The ΔL comes from the over exposure error induced in photolithography process and dopant diffusion into channel area after high temperature activation. Linear scaling is obtained as expected.

The effective mobility depicted in Fig. 3.8 is extracted from a 20μm gate length device, the mobility at high inversion carrier density is about twice of that from GaAs(111)A NMOSFET with Al_2O_3 gate dielectric [37]. The peak electron effective mobility is not as high as that of devices with Si or silane + ammonia passivation at low inversion carrier density region, one possible reason is that the coulomb scattering induced by lattice defects. The split C-V curve in Fig. 3.9 exhibits very small frequency dispersion ($\Delta C/C_{max} \sim 7\%$), indicating low interface trap density even in the upper band gap.

The inset figure in Fig. 3.9 shows the measurement setup for split-CV. The source and drain areas are connected together with ground, the inversion carriers (electrons in NMOSFET) can be provided under channel region through contact part. With higher gate bias, the Fermi level in under the channel region will rise into upper

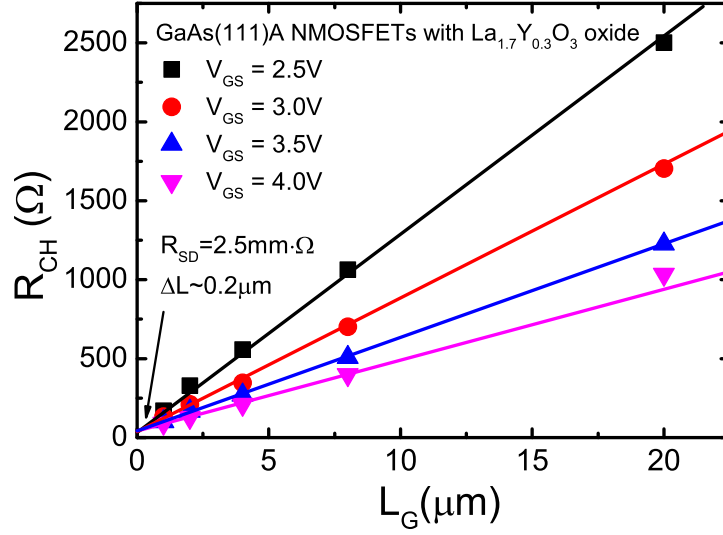


Fig. 3.7. Channel resistance (R_{CH}) versus gate length (L_G) under different gate biases (V_{GS}) in the linear region ($V_{DS}=10\text{mV}$) on GaAs(111)A NMOSFETs with different L_G . Linear scaling is obtained as expected.

band gap and approaching Conduction Band Edge (CBE), the high trap density will significantly affect the small AC signal of capacitance voltage measurement and the C-V curve will show frequency dispersion due to the carrier trapping-detrapping in the trap energy levels. However, in the epitaxial oxide on semiconductor system the D_{it} is greatly suppressed thanks to the lattice matching crystalline structure and the improvement of high temperature annealing process. Thus the frequency dispersion is much smaller comparing to most passivation techniques.

Scaling Behavior of GaAs(111)A nMOSFETs

Fig. 3.10 is the comparison of scaling characteristics of I_{DS} versus different gate lengths for GaAs NMOSFET devices with two different gate oxide stacks. The ION are taken from GaAs(111)A NMOSFETs at $V_{GS} = 4\text{V}$ and $V_{DS} = 2\text{V}$. It

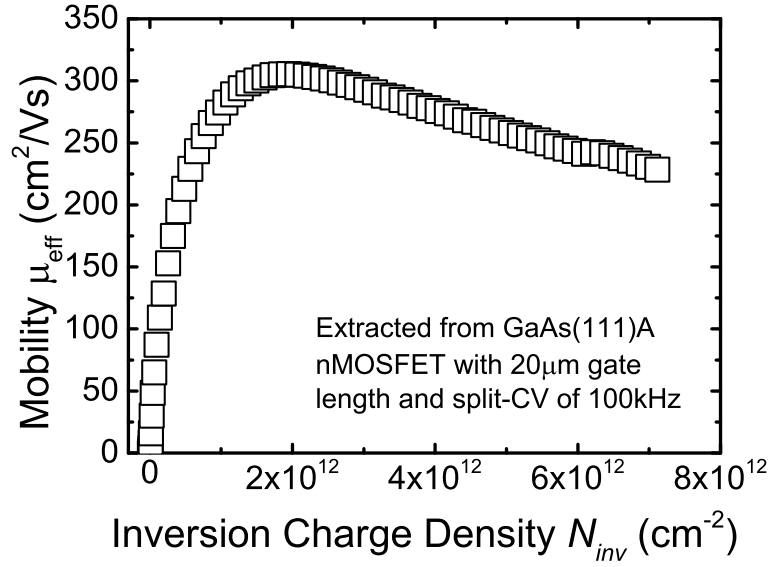


Fig. 3.8. Effective electron mobility extracted from a $L_G=20\mu\text{m}$ GaAs(111)A NMOSFET with $\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ as gate dielectric.

is clear that for devices with all the gate lengths the on-currents of NMOSFETs with $\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ gate stack are much higher ($10^1 \sim 10^2$) than that of devices with $\text{Al}_2\text{O}_3/\text{LaYO}_3$ gate stack, showing the advantage of better lattice matched $\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ interface.

The subthreshold swing (or called subthreshold slope) SS is shown in Fig. 3.10. The red dashed line is denoting the 100mV/dec for eye reference. For all the devices of different gate lengths the SS are around 97mV/dec, indicating an excellent semiconductor-oxide interface. SS is a good method for estimation of mid gap D_{it} . Ignoring the short channel effect, the SS usually can be expressed as

$$SS = 60\text{mV/decade} \cdot \left(1 + \frac{C_{it}}{C_{ox}}\right) \quad (3.1)$$

where $C_{it} = qD_{it}$ is the interface trap capacitance and C_{ox} is the oxide capacitance. The mid gap D_{it} from GaAs(111)A NMOSFETs is around $3 \times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$, which

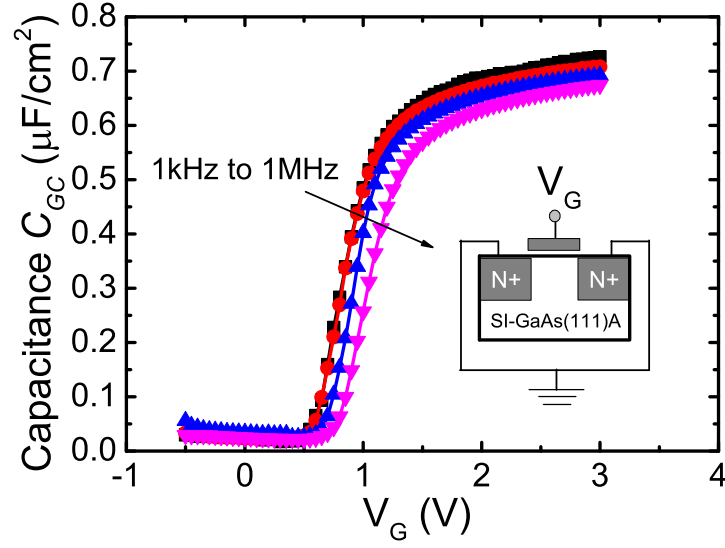


Fig. 3.9. Split C-V characteristics of a GaAs (111)A NMOSFET with $\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ as gate dielectric, showing very small frequency dispersion, indicating a good interface quality. Inset: measurement configuration.

is much lower than the GaAs(111)A device with Al_2O_3 gate dielectric. Further device scaling into the submicron regime may give better device performance with novel device structures.

3.1.4 Epitaxial $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ interface enabled high performance GaAs pMOSFETs

GaAs(111)A Inversion Mode pMOSFETs Device Structure and Fabrication

Similar to the nMOSFETs fabrication process described in the previous section, the device fabrication also starts from GaAs semi-insulating substrates with GaAs(111)A surface. The substrates were first degreased by acetone, methanol and

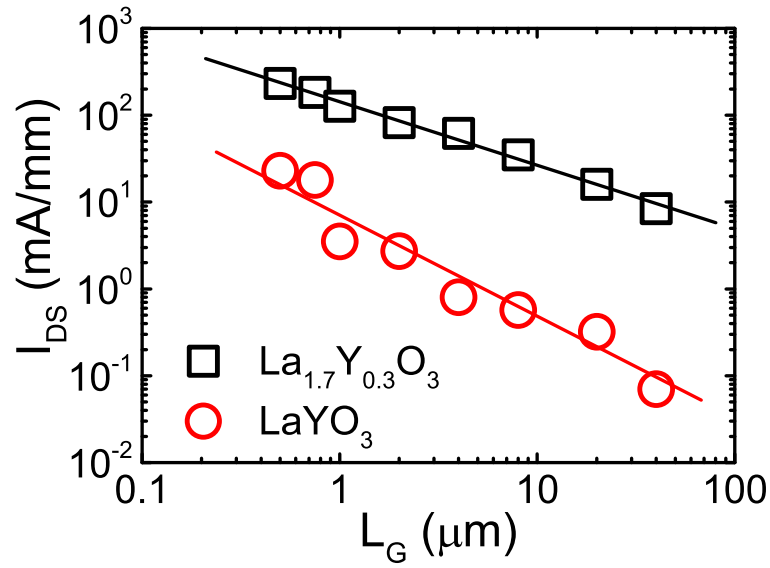


Fig. 3.10. Scaling characteristics of I_{DS} versus different gate lengths L_G for GaAs(111)A NMOSFETs with two different gate oxides.

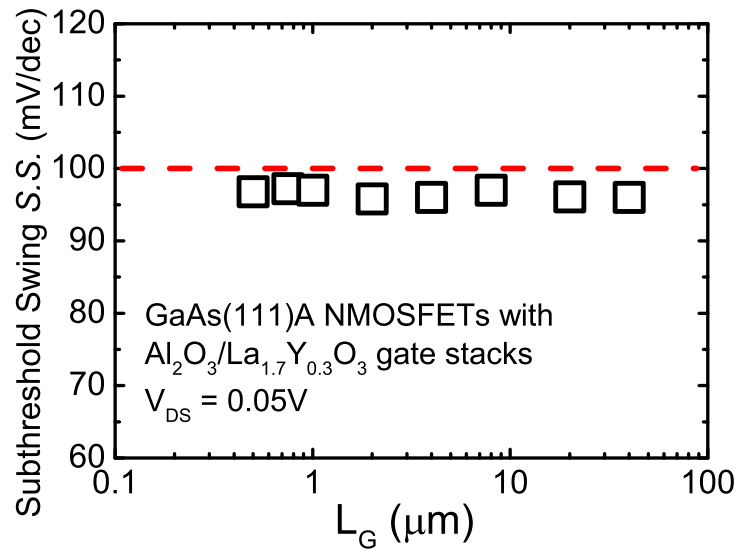


Fig. 3.11. Scaling metrics of subthreshold swing (SS) versus different gate lengths L_G for GaAs(111)A NMOSFETs with $\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ gate dielectric.

isopropanol, then dipped in diluted HCl for 30 seconds and soaked in 10% $(\text{NH}_4)_2\text{S}$ solution for 20 minutes for sulfur passivation. Right after the passivation, the samples were quickly transferred into atomic layer deposition (ALD) chamber, 7.5nm $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ and 6.5nm Al_2O_3 were sequentially deposited on the GaAs(111)A surface, and a $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}$ epitaxial interface is formed. The purpose of the Al_2O_3 top layer is to prevent $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ reacting with water in the air. The source/drain regions were patterned and implanted with a zinc dose of $5 \times 10^{14} \text{ cm}^{-2}$ and an energy of 60 keV, and ion activation was achieved by annealing at 800C for 30 seconds in nitrogen in a rapid thermal process (RTP) system. The GaAs/ $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ interface quality is greatly improved by the relative high temperature treatment, which at the same time caused dopant diffusion from source/drain into the device channel area. The oxide stacks at source and drain area were etched away by diluted BOE and HCl solution, and Pt/Ti/Pt/Au were electron beam evaporated for S/D ohmic contact. Finally Ni/Au was evaporated for gate electrode. A Keithley 4200 was used for the GaAs pMOSFETs electrical characterization and an HP4284A precision LCR meter was used for split-CV measurement at room temperature.

The cross-sectional view of a GaAs pMOSFET fabricated in this work is shown in Fig. 3.12, and the inset is a HRTEM image taken from the interface of $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ after high temperature annealing. A clear sharp, flat and epitaxial interface can be observed from the TEM image. The $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ formed cubic phase on top of GaAs(111)A surface and the epitaxial structure is formed and confirmed by both TEM and X-ray Diffraction (XRD) analysis, and detail interface studies can be found in [9]. The Capacitance-Voltage study of the epitaxial MOS structure shows that higher temperature thermal treatment is helpful to improve interface quality and reduce interface trap density. The Dit for the 800°C annealed samples is extracted to be around $5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ in the band gap position of $E = E_v + 0.4 \text{ eV}$, using

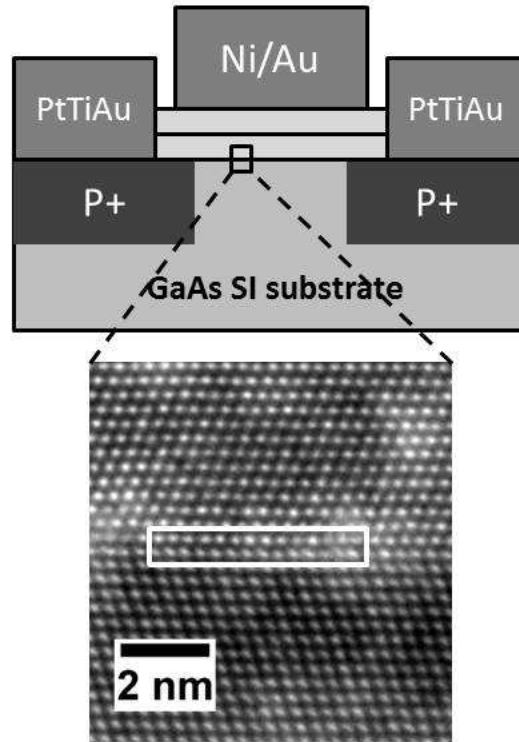


Fig. 3.12. (a) The cross sectional view of a GaAs(111)A pMOS-FET. (b) High-resolution TEM image of the single epitaxial GaAs(111)A/La_{1.8}Y_{0.2}O₃ interface after 860°C RTA annealing. The white box is denoting the flat interface for eye reference.

conductance method at room temperature. Therefore, in order to achieve better semiconductor-oxide interface quality, an optimized annealing of 800°C was employed in the pMOSFETs fabrication.

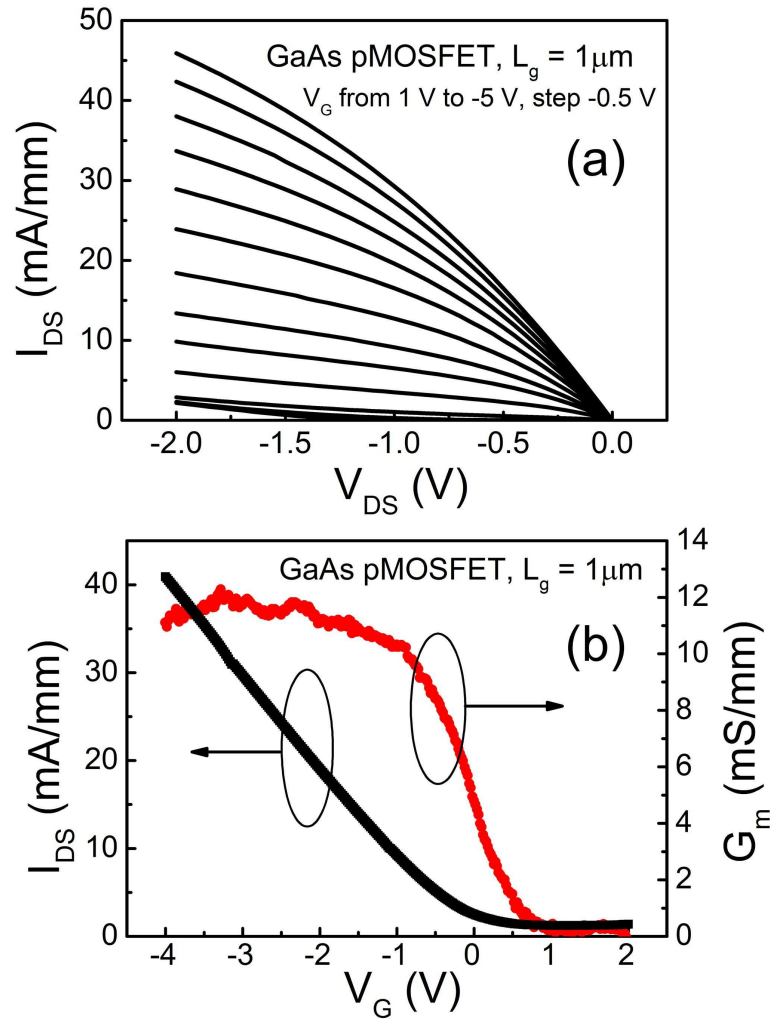


Fig. 3.13. (a) Current-voltage (I-V) characteristic and (b) extrinsic transconductance (G_m) and drain current versus gate bias of a 1μm-gate-length GaAs pMOSFET with ALE $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ gate oxide. This device shows a maximum drain current of 46 mA/mm and a peak extrinsic transconductance of 12 mS/mm.

GaAs pMOSFETs devices characterization and analysis

Fig. 3.13(a) shows the measured DC output characteristics of a GaAs pMOSFET with 1μm gate length fabricated in this work. At a gate bias of -5V and a drain bias of -2V, the maximum drain current is 46 mA/mm, which is among the highest

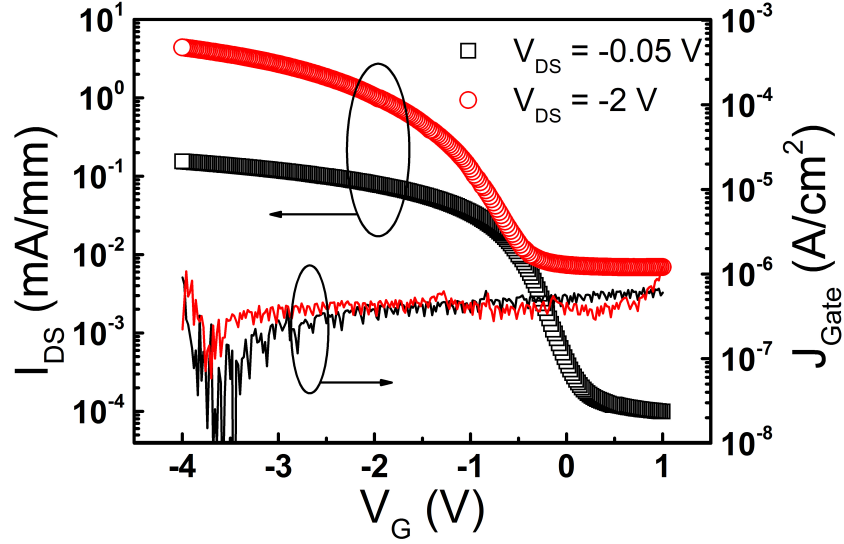


Fig. 3.14. Transfer characteristics and gate leakage current density of a 8 μ m-gate-length GaAs pMOSFET fabricated in this work.

III-V pMOSFETs reported so far. The current drivability has been greatly improved over the GaAs pMOSFET with amorphous Al₂O₃ gate dielectric (two orders of magnitude higher I_D). We attribute this to the high quality, low D_{it} interface epitaxial La_{1.8}Y_{0.2}O₃/GaAs(111)A interface, which is crucial in enhancement mode MOSFETs realization. The linear output characteristics as well as the transconductance as a function of gate voltage of the same device are plotted in Fig. 3.13(b). This device has a threshold voltage of -0.16V, which is suitable for the requirements of the future short channel CMOS applications with low driving voltage. As a result of the unoptimized process, relative large contact resistance of around 2.2 $\Omega \cdot \text{mm}$ is obtained, by the method of transmission line model. The extrinsic peak transconductance is about 12 mS/mm, which is comparable to the GaSb pMOSFETs with amorphous Al₂O₃ dielectrics of 4 nm EOT. The transconductance can be further improved by reducing the equivalent oxide thickness (4.5nm in this work) and optimizing the Ohmic contact

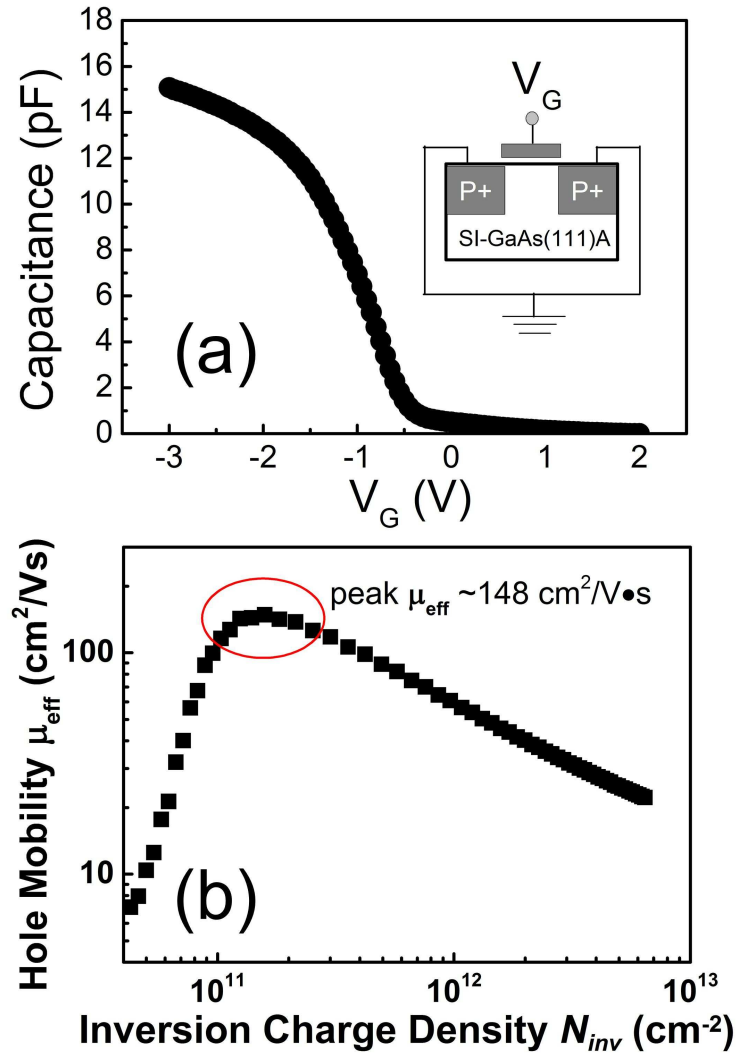


Fig. 3.15. (a) Split C-V characteristics and measurement setup of a $L_g = 8\mu\text{m}$ GaAs(111)A pMOSFET fabricated in this work (b) effective hole mobility extracted from the same GaAs(111)A pMOSFET as in (a), using the split CV results.

at S/D area. The transfer characteristics along with the gate leakage current density of an $8\mu\text{m}$ gate length GaAs pMOSFET are shown in Fig. 3.14. The gate leakage current density stays below 10^{-6} A/cm² for all measured gate biases, indicating excellent dielectric thermal stability even after high temperature annealing. At a high drain

bias of 2 V, the current I_{ON}/I_{OFF} of this device is over 2400. The subthreshold slope obtained is around 280 mV/dec. We ascribe the relative small current on/off ratio to the dopant fast diffusion from the source and drain into channel area because of the high temperature annealing process (800°C 30s). The high off-state current become more severe when the gate length is lower than $2\mu\text{m}$, which is in consistent with the above explanation. We previously reported the charge neutral level shifting towards the conduction band on the GaAs(111)A surface, which is favorable for nMOSFETs realization. However, the epitaxial structure greatly reduced the density of traps at the interface and thus enabled an unpinned GaAs surface, which is of vital importance for enhancement-mode MOSFETs. Split-CV characteristic of 10 kHz along with the capacitance measurement setup are shown in Fig. 3.15(a). The hole effective mobility is calculated and plotted in Fig. 3.15(b). The hole effective mobility

$$\mu_{eff} = \frac{g_d L}{W Q_n} \quad (3.2)$$

where g_d is the drain conductance, L and W are the channel length and width of the device, Q_n is the mobile channel inversion charge density, which can be obtained by integration of the split C-V curve. The peak hole mobility of $148 \text{ cm}^2/\text{V}\cdot\text{s}$ is achieved. Although the pMOSFETs are still constrained by the GaAs hole mobility by its nature, the high quality epitaxial interface make the GaAs pMOSFET very promising in future CMOS applications.

3.1.5 $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ MOS Capacitance-Voltage Study

In order to investigate the mechanism lying behind the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ system, Different $\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ capacitors were also fabricated and annealed at different temperatures for systematic interface studies.

MOS Capacitors Fabrication

The MOS capacitors fabrication began with p-type GaAs(111)A substrates of doping $5-7 \times 10^{17} \text{cm}^{-3}$ and n-type GaAs(111)A substrates of doping $6-9 \times 10^{17} \text{cm}^{-3}$, same surface pretreatment including surface degrease, HCl etching and sulfur passivation were performed sequentially before Atomic Layer Deposition oxides. The same oxide stacks 7.5nm $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{LaYO}_3$ and 6.5nm Al_2O_3 were deposited on the sulfur passivated surface at 300°C , while the Al_2O_3 topping layer serves as encapsulation layer preventing the reaction between $\text{La}_x\text{Y}_y\text{O}_3$ and air. The samples were then annealed in a Jipelec RTA system at different temperatures; the splits include as-deposited, 600°C for 30 seconds, 700°C for 30 seconds and 800°C for 30 seconds. The annealing ambient was nitrogen. Top-top capacitance structures were employed in the capacitor fabrication since only one metallization is needed, which simplified the process. Ni/Au was evaporated as top metal layer, followed by a lift-off process.

Capacitance-Voltage Comparison Analysis

Table 3.2 summarized the The capacitance frequency dispersion, flat band voltage and its shift from 5kHz to 1MHz of p-type capacitors at different annealing conditions with two oxide layers. The frequency dispersion in the capacitance accumulation region ($\Delta C/C_{\text{max}}$) indicates the density of traps where the Fermi level is reaching the valence band edge. The capacitors with $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ and $\text{LaYO}_3/\text{GaAs}(111)\text{A}$ exhibit similar dispersion and trend after different annealing conditions. The $\text{LaYO}_3/\text{GaAs}(111)\text{A}$ capacitors dispersion dropped from 4.7% to 1% after 800°C annealing while the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ capacitors dispersion dropped from 5% to 1.8%. The interface quality improvement also can be observed from the ΔV_{fb} from 5kHz to 1MHz, which shows the same tendency with the fre-

Table 3.2

Comparison of C-V curve frequency dispersion, ΔV_{fb} from 5kHz to 1MHz and V_{fb} of p-type Ni/Al₂O₃/La_{1.8}Y_{0.2}O₃/GaAs(111)A and p-type Ni/Al₂O₃/LaYO₃/GaAs(111)A capacitors under different annealing conditions. The reduction of frequency dispersion suggests that the interface quality is improved by high temperature annealing.

	Al₂O₃/LaYO₃				Al₂O₃/La_{1.7}Y_{0.3}O₃			
Annealing condition (30s in N ₂)	As-depo	600°C	700°C	800°C	As-depo	600°C	700°C	800°C
Frequency dispersion (%) ($\Delta C/C_{max}$)	4.7	2.6	2.9	1	5	2.1	2.1	1.8
ΔV_{fb} (mV) (from 5kHz to 1MHz)	420	320	240	95	300	220	190	103
V_{fb} (V)	-0.9	-0.7	-0.5	-0.4	-1.2	-1.2	-0.8	-0.3

quency dispersion. One noteworthy point is that although the high thermal budget can lead to improvement of interface, it will also induce the C-V flat band shift positively. This shift can be attributed to the negative charged oxygen vacancies residing in the La_xY_yO₃ oxide were reduced during the RTA process.

The Equivalent Oxide Thickness (EOT) versus annealing condition on Al₂O₃-/La_xY_yO₃/GaAs(111)A capacitors are plotted in Fig. 3.16. The EOT were calculated from the accumulation capacitance of C-V curve. The EOT decreased slightly after higher temperature annealing due to the following two reasons:

1. The oxide film densification resulted from high temperature annealing. The oxide stacks became thinner and thus the physical thickness is less.
2. Higher dielectric constant is achieved because of the crystalline structure is improved with high thermal budget.

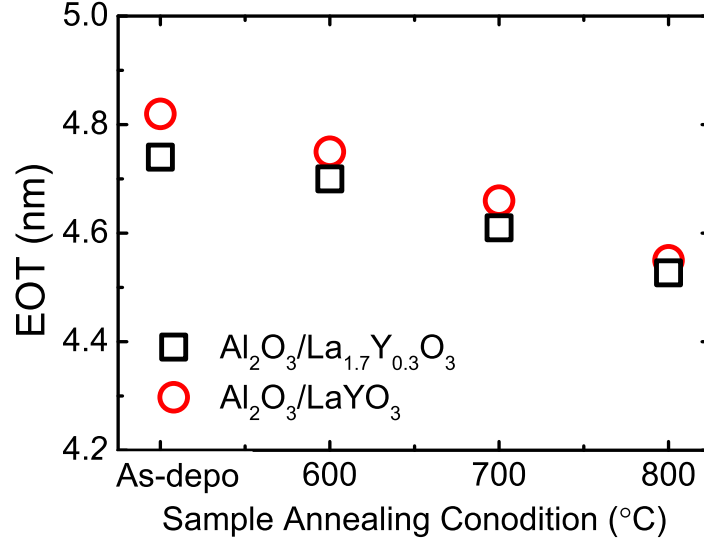


Fig. 3.16. EOT as a function of annealing condition on $\text{Al}_2\text{O}_3/\text{La}_x\text{Y}_y\text{O}_3/\text{GaAs}(111)\text{A}$ systems. Samples are annealed at 600°C , 700°C and 800°C for 30 seconds in N_2 , respectively.

The $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ oxide has higher dielectric constant which contributes to the smaller EOT than LaYO_3 oxide at all annealing conditions. The physical oxide thicknesses in this work ($\sim 7.5\text{nm}$ $\text{La}_x\text{Y}_y\text{O}_3$ and $\sim 6.5\text{nm}$ Al_2O_3) were confirmed by Atomic Force Microscopy (AFM) measurement, performed on the samples etched by diluted BOE and HCl solution. The higher dielectric constant make $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ more promising in the application of next generation MOSFETs in terms of scaling down, let alone much better interface electrical properties. Device integration with EOT as small as $1.0\text{-}1.2\text{nm}$ is achievable by reducing $\text{La}_x\text{Y}_y\text{O}_3$ and Al_2O_3 thickness [42].

Fig. 3.17 and 3.18 show the C-V characteristics of n-type and p-type $\text{Ni}/\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ capacitors after different annealing temperatures. The frequencies are from 1kHz to 1MHz . Notice the slightly larger accumulation capacitances are due to the densification effect we discussed earlier. Besides smaller frequency dispersion can be clearly observed from the annealed p-type capacitor samples, while

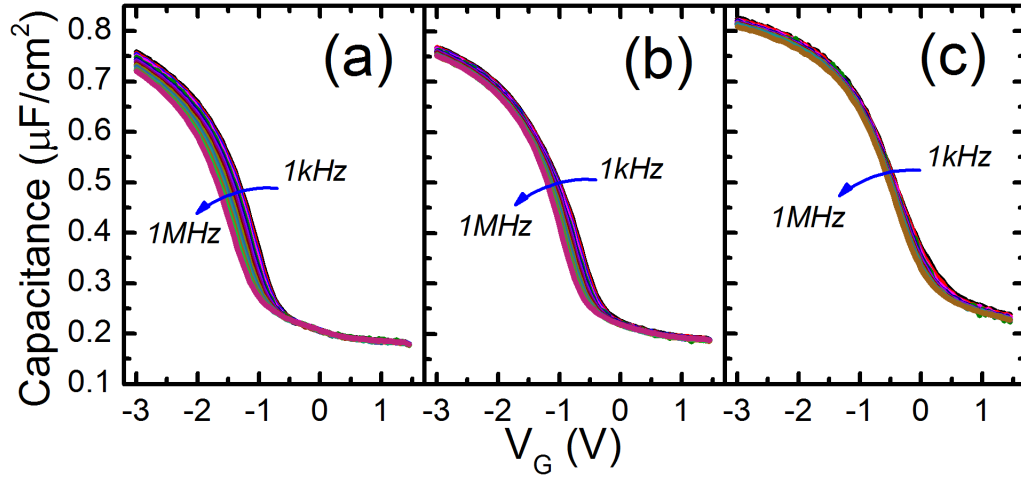


Fig. 3.17. Capacitance-Voltage characteristics of p-type Ni/Al₂O₃/La_{1.8}Y_{0.2}O₃/GaAs(111)A capacitors measured from 1kHz to 1MHz at different annealing conditions (a) As-deposited (b) 600°C annealed and (c) 800°C annealed in N₂ for 30seconds.

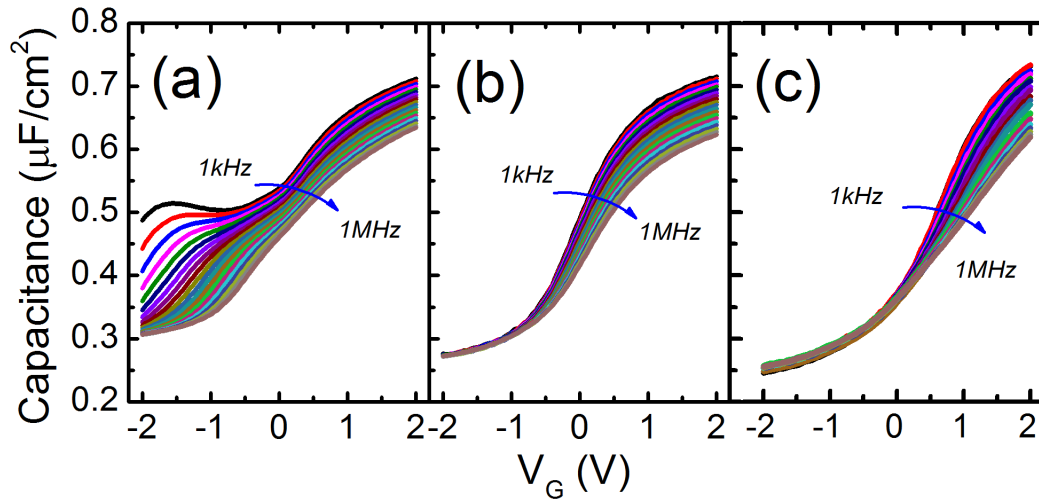


Fig. 3.18. Capacitance-Voltage characteristics of n-type Ni/Al₂O₃/La_{1.8}Y_{0.2}O₃/GaAs(111)A capacitors measured from 1kHz to 1MHz at different annealing conditions (a) As-deposited (b) 600°C annealed and (c) 800°C annealed in N₂ for 30seconds.

for n-type C-V the C-V bump caused by the mid-gap D_{it} is significantly reduced by high temperature annealing. However, the frequency dispersion remains around the same level; this may be due to the trap densities close to the conduction band edge are not suppressed effectively. The C-V results taken at 100 kHz and conductance spectroscopy of samples with two different interfaces annealed at 800°C are compared in Fig. 3.19. The capacitances are normalized to C/C_{max} for a fair comparison. The smaller capacitance in the inversion region of the capacitor $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ is attributed to the larger capacitance in the accumulation region. We can see that the transition of the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ C-V curve from accumulation to weak inversion is faster than that of $\text{LaYO}_3/\text{GaAs}(111)\text{A}$ C-V, which means the typical stretched out curve caused by higher D_{it} existing in the $\text{LaYO}_3/\text{GaAs}(111)\text{A}$ interface.

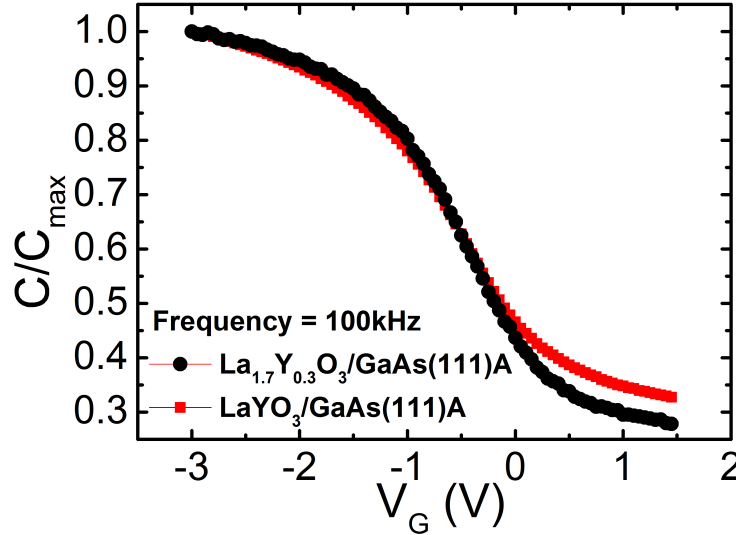


Fig. 3.19. A comparison of p-type 100 kHz C-V characteristics of $\text{Ni}/\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ and $\text{Ni}/\text{Al}_2\text{O}_3/\text{LaYO}_3/\text{GaAs}(111)\text{A}$ annealed at 800°C. A more stretched-out behavior is observed from the $\text{LaYO}_3/\text{GaAs}(111)\text{A}$ interface.

C-V Study with Conductance Methods

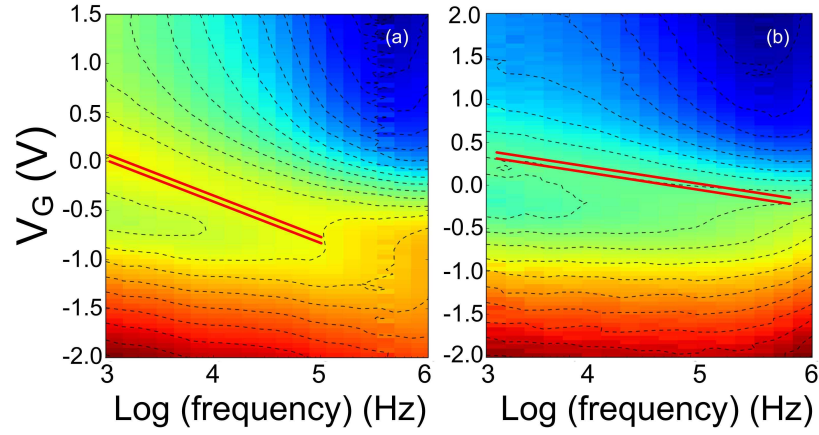


Fig. 3.20. Conductance spectroscopy in the plane of V_G versus frequency from p-type C-V of (a) Ni/Al₂O₃/LaYO₃/GaAs(111)A capacitors and (b) Ni/Al₂O₃/La_{1.8}Y_{0.2}O₃/GaAs(111)A capacitors. Both samples were annealed at 800°C in N₂ for 30 seconds. The Fermi level traces are denoted by the double red lines.

Fig. 3.20 compares the conductance spectroscopy of samples with two different interfaces annealed at 800°C. Using conductance method, Fermi level moving efficiency can be compared by the equation [43]:

$$f = \frac{\sigma v_t N}{2\pi \exp(\Delta E/kT)} \quad (3.3)$$

Where ΔE ($E_c - E_t$ or $E_t - E_v$) is the difference between the energy level of the trap state and the majority carrier band edge, σ is the trap state interaction cross section, v_t is the thermal velocity of the carrier and N is the density of state of the majority carrier band. The measurement frequency f is equal to $1/2\pi\tau$, where τ is the characteristic trapping time who describes the time needed for a free charge to be captured or trapped by a trapping state at energy level E_t . A typical frequency range for CV measurement goes from 1kHz to 1MHz which corresponds to 0.28 eV

- 0.47 eV above the valence band for holes and 1.01 eV - 1.19 eV above the valence band for electrons in GaAs at room temperature, as illustrated in Fig. 3.21.

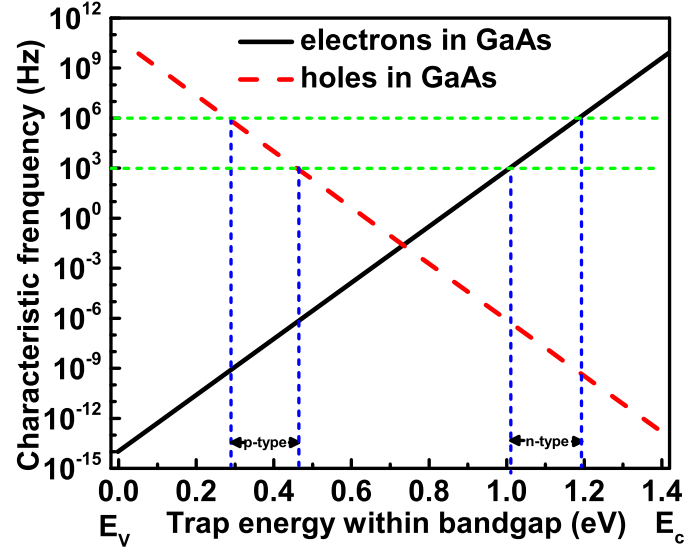


Fig. 3.21. Charge trapping characteristics for GaAs at room temperature (300K).

Therefore, it can be calculated from Fig. 3.20 that For the capacitor of $\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$, the Fermi level moves more than 0.2 eV in the GaAs bandgap within ~ 0.5 V gate bias, and the modulation efficiency is about twice that of $\text{Al}_2\text{O}_3/\text{LaYO}_3/\text{GaAs}(111)\text{A}$ capacitor. The much higher Fermi level moving efficiency [44] of $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ interface than $\text{LaYO}_3/\text{GaAs}(111)\text{A}$ suggests that much smaller density of traps (D_{it}) is achieved in former structure since more gate induced charges are effectively responsible for Fermi level moving instead of filling interface traps.

The D_{it} extracted from conductance method is plotted in Fig. 3.22 and Fig. 3.23. High temperature annealing effectively suppressed the D_{it} (from $3 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ down to $5 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$) at the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ interface while it is less

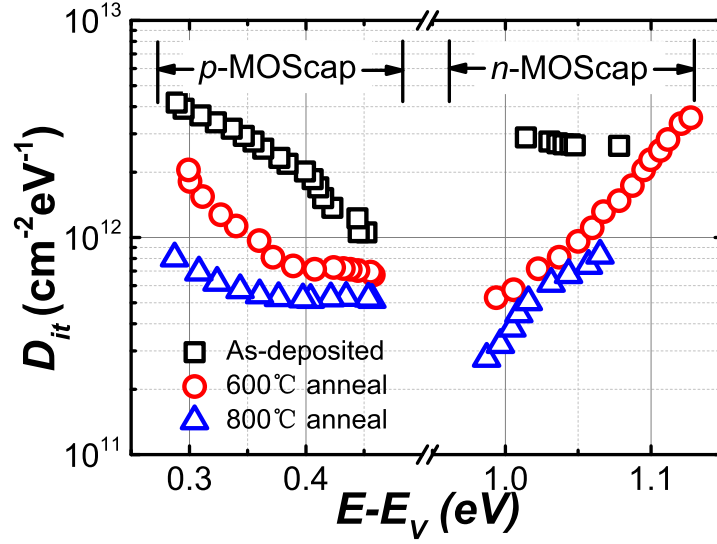


Fig. 3.22. D_{it} distribution in GaAs band gap obtained on p-type and n-type capacitors with $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ interface. The values are calculated by the conductance method at room temperature. A better interface is shown than the D_{it} in Fig. 3.23.

effective for the $\text{LaYO}_3/\text{GaAs}(111)\text{A}$ interface due to the lattice mismatch induced defects.

3.1.6 Summary

In this section, high performance inversion-mode GaAs(111)A NMOSFETs with ALE $\text{La}_x\text{Y}_y\text{O}_3$ as gate dielectric are experimentally demonstrated and characterized. The maximum drain current reaches 326 mA/mm for 0.5 μm gate length device with a low subthreshold swing (SS) of 97mV/dec. High temperature dopant activation annealing further improved interface quality, which enabled GaAs high performance inversion mode NMOSFETs. The low D_{it} crystalline interface is promising for III-V MOSFET applications thanks to its low density of traps and good thermostability.

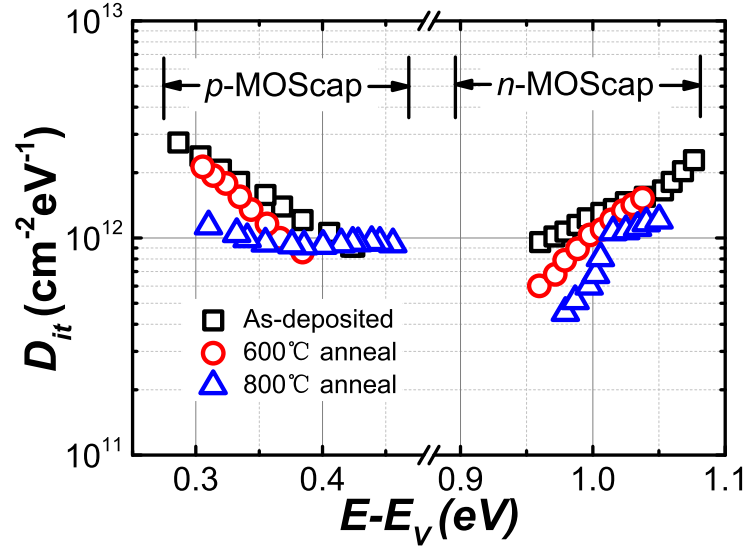


Fig. 3.23. D_{it} distribution in GaAs band gap obtained on p-type and n-type capacitors with $\text{LaYO}_3/\text{GaAs}(111)\text{A}$ interfaces. The values are calculated by the conductance method at room temperature.

3.2 Epitaxial $\text{La}_2\text{O}_3/\text{GaAs}$ (111)A interface enabled high performance GaAs CMOS devices

3.2.1 Introduction

The electrical results of GaAs MOSFETs with $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ interface in the last section showed great potential of the application of GaAs devices. The low density of traps in the GaAs bandgap solved the Fermi level pinning problem which make high performance inversion-type MOSFETs possible. However, there are still some questions worth exploring:

1. The lattice matching of the La-based oxide and the GaAs substrate below is of great importance. While the lattice mismatch of the $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ with respect to the GaAs is 0.64%, will the device performance and interface quality be further

enhanced if a better lattice matching single crystalline oxide film is applied as the gate dielectrics?

2. Is it possible to deposit a thin film that we would be able to control the film crystallinity, ultra thin thickness and chemistry property at the same time to meet our need?
3. What about the scaling ability of this single crystal oxide film? The scalability of the oxide thickness will be a key feature in the future device application due to the ever-shrinking device sizes.

In order to address these questions, a systematic study of the La-based oxides deposited with Atomic Layer Deposition on GaAs(111)A substrates, along with high performance GaAs devices and basic digital circuits experimental demonstration, are presented in this part.

In the last section we presented the demonstration of high performance GaAs nMOSFETs and pMOSFETs with $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ epitaxial dielectrics. The lattice matching of the single crystalline oxide film and the GaAs(111)A interface provides enormous potential for future device applications, since the number of dangling bonds at the interface will be greatly reduced because of the well matched lattice structure. According to the previous section we can see that with the incorporation of different concentration of Y or other elements, we are able to tune the lattice constant of the La-based single crystalline oxide (see Fig. 2.8). In this chapter, we demonstrate, for the first time, high-performance GaAs devices (nMOSFETs and pMOSFETs) that are integrated into CMOS circuits (inverters, NAND and NOR logic gates, and five-stage ring oscillators). These devices were enabled by the high-quality interface of single-crystalline La_2O_3 grown on GaAs(111)A by atomic layer epitaxy. The lattice

mismatch between La_2O_3 and GaAs is just 0.04%, which make devices with even better performance possible.

3.2.2 GaAs CMOS devices and circuits fabrication process

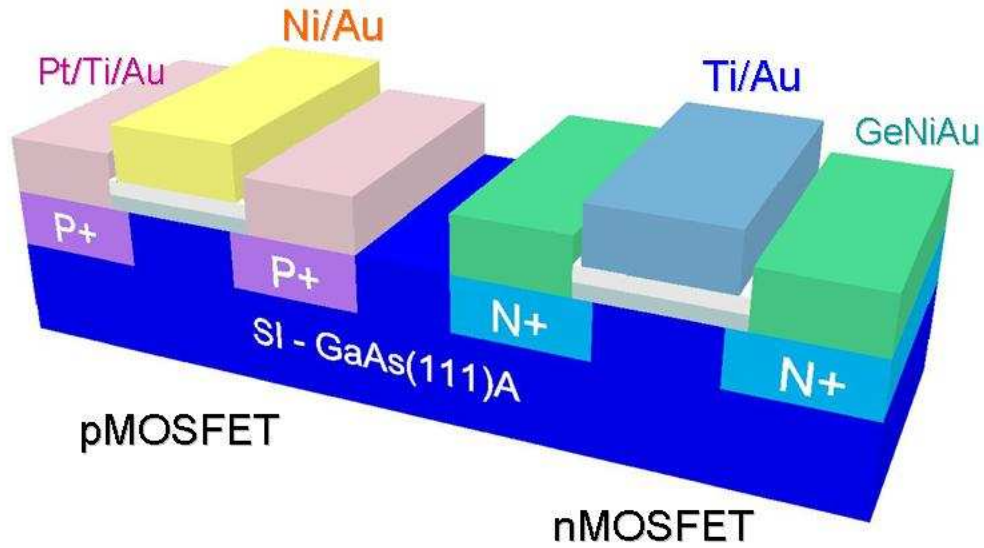


Fig. 3.24. Schematic view of a GaAs pMOSFET and an nMOSFET in the GaAs CMOS integrated circuits fabricated here. GeNiAu alloy is employed as S/D Ohmic contact metal for nMOSFETs and PtTi alloy is employed for pMOSFETs..

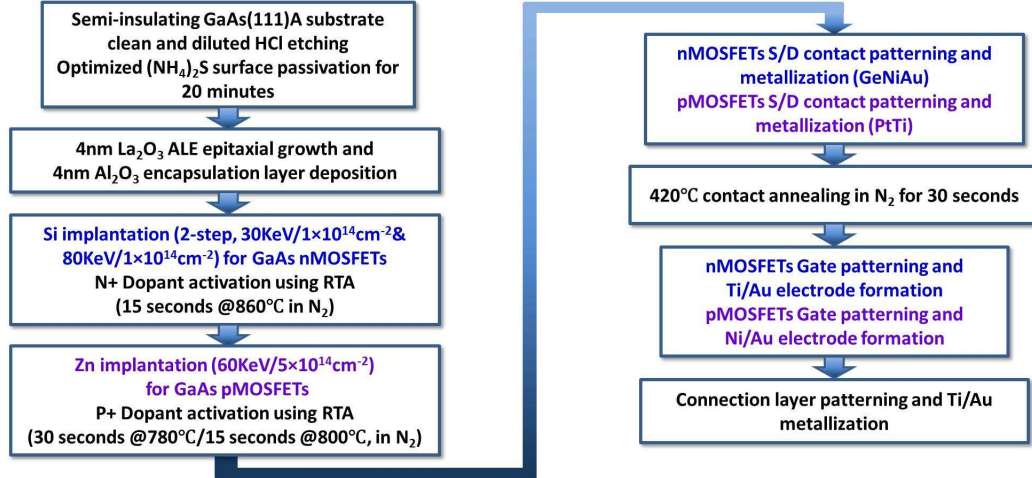
Fig. 3.24 shows the schematic view of nMOSFET and pMOSFET fabricated in this work on a common semi-insulating GaAs (111)A substrate with a common

ALE high-k dielectric. The detailed process flow is depicted in Table 3.3. The GaAs CMOS circuits fabrication began with semi-insulating GaAs substrates with (111)A surface (Ga-terminated). The substrates were sequentially first cleaned by acetone, methanol and isopropanol for degrease purpose, then diluted HCl solution (1:3) was employed to strip the native oxide on top of GaAs surfaces. After the oxide removal, the substrates were soaked in 10% ammonia sulfide ((NH₄)₂S) solution for surface sulfur passivation. The sulfur passivation is an important step in process since it can effectively protect the surface from re-oxidation caused by the exposure with air, for a relative short time though. The substrates were loaded into ALD chamber quickly after the sulfur passivation, then 4nm La₂O₃ and 4nm Al₂O₃ were deposited on the GaAs(111)A surface. The epitaxial La₂O₃ thin films employed here were deposited from the precursors lanthanum tris(N,N-diisopropylformamidinate) and H₂O at 385°C, while the amorphous Al₂O₃ oxide capping layer was deposited with precursors of trimethylaluminum (TMA) and H₂O at 300°C. Uniform epitaxial layers were grown by the employment of long purging times (40s~80s). The purpose of Al₂O₃ capping layer is to prevent the reaction between La₂O₃ and air.

After the film deposition, S/D active regions for nMOSFETs were defined by photolithography and a two-step ion implantation with a Si dose of $1 \times 10^{14} \text{ cm}^{-2}$ at 30 keV and $1 \times 10^{14} \text{ cm}^{-2}$ at 80 keV was performed to create N+ areas. N+ implantation activation was achieved by rapid thermal anneal (RTA) at 860 °C for 15 seconds in N₂ ambient. Then the S/D area were again defined by photolithography and an ion implantation of Zn with a dose of $5 \times 10^{14} \text{ cm}^{-2}$ at 60 keV was performed to form P+ regions, followed by another ion activation annealing at 780 °C for 30 seconds or 800 °C for 15 seconds, in nitrogen ambient and in an RTA system. The source and drain areas of GaAs nMOSFETs were then formed by photolithography and AuGe/Ni/Au metal stacks were evaporated to form ohmic contacts with N+ re-

Table 3.3

Process sequence for the fabrication of GaAs (111)A CMOS circuits. The epitaxial interface is formed by ALE 4nm single crystalline La_2O_3 , followed by 4nm ALD amorphous Al_2O_3 as an encapsulation layer. Si and Zn were used for N+ region and P+ region ion implantation, respectively..



gions, and for P+ regions the alloy metal of PtTi was chosen to form Ohmic contact. After lift-off processes, the samples were annealed by RTA at 420 °C for 30 seconds in N_2 . The gate electrodes for GaAs nMOSFETs was formed by e-beam evaporation of Ti/Au and for GaAs pMOSFETs was formed by Ni/Au deposition. At this point, the fabrication of both nMOSFETs and pMOSFETs are completed. For the CMOS circuits fabrication, a connection metal layer of Ti/Au was done by e-beam evaporation after photolithography, followed by a lift-off process.

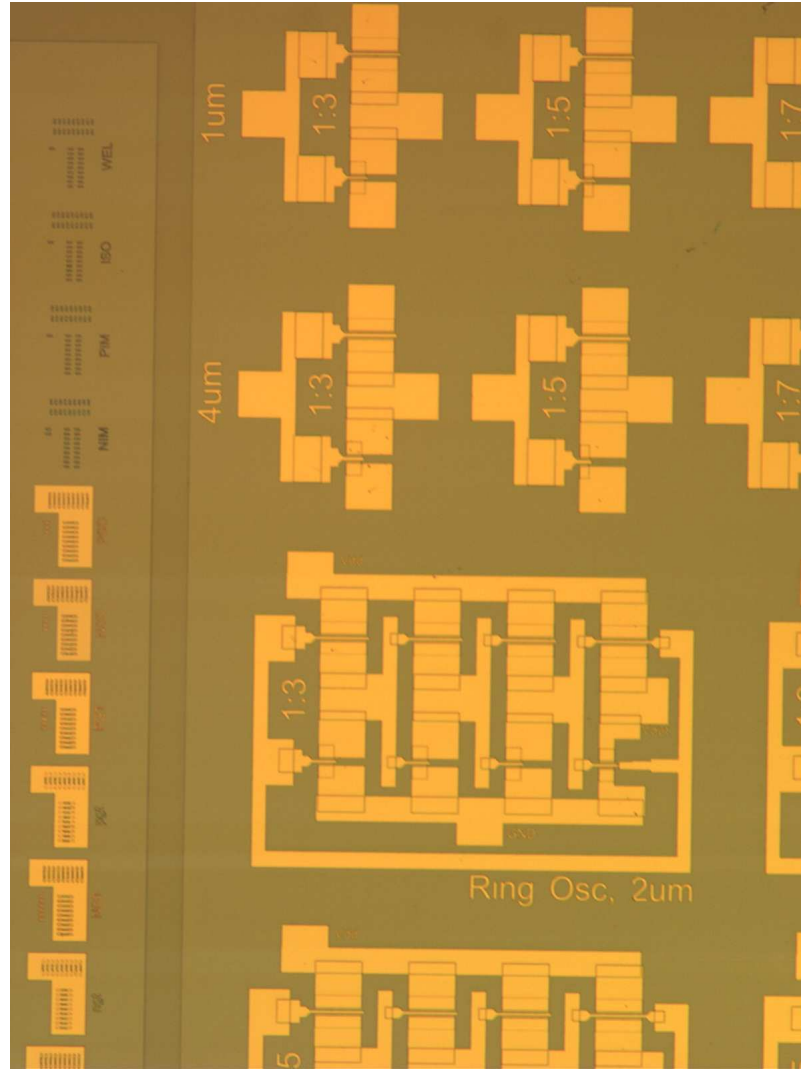


Fig. 3.25. A birds view of the sample with fabricated GaAs CMOS devices and circuits. The alignment marks are on the left part of the picture, which was used for alignment during the photolithography process for each layer. GaAs CMOS inverters are on the top right of the picture, and 1- μm -gate-length and 4- μm -gate-length pMOSFETs and nMOSFETs devices with different gate width ratios can be observed. Ring oscillators are at the bottom right part, and a complete 3-stage ring GaAs CMOS oscillator, with devices gate length of 2 μm and gate width ratio of 1:3 (nMOSFETs to pMOSFETs), is shown.

3.2.3 Electrical characterizations and analysis of GaAs CMOS devices

The fabricated GaAs MOSFETs in the integrated circuits have a nominal gate length varying from 1 μm to 8 μm , and the gate width ratios of nMOSFETs to pMOS-

FETs in GaAs CMOS inverters vary from 1:3 to 1:10. An optical micrograph view of the sample of with fabricated devices can be seen in Fig. 3.25.

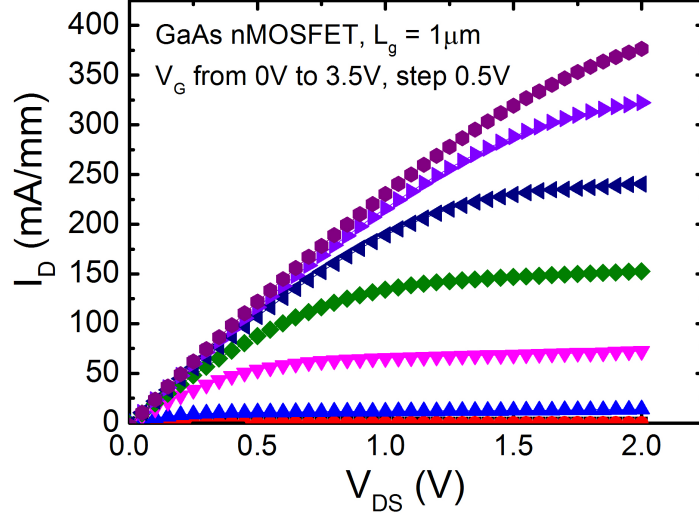


Fig. 3.26. Output characteristics ($I_{DS} \sim V_{DS}$) for a $L_G = 1\mu m$ GaAs(111)A nMOSFET with GaAs/La₂O₃ epitaxial interface. The maximum drain current can reach ~ 376 mA/mm with a gate bias of 3.5 V and a drain bias of 2 V.

For the purpose of a systematic study, we first look at the electrical performance of GaAs(111)A nMOSFETs and pMOSFETs independently. A well-behaved output characteristic of a $1\mu m$ -gate-length inversion enhancement-mode GaAs(111)A nMOSFET with La₂O₃/Al₂O₃ is plotted in Fig. 3.26, exhibiting a maximum drain current of 376 mA/mm with $V_{DS} = 2V$ and $V_{GS} = 3.5V$, and the on-state driving current is comparable to that of the previous InGaAs devices. The transfer characteristics from the same nMOSFET are plotted in Fig. 3.27. A small SS of ~ 74 mV/dec is obtained with an EOT of $\sim 3nm$, indicating a very low mid-gap interface trap density (D_{it}) of $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. The subthreshold slope obtained from the GaAs nMOSFETs in this work is the smallest of all the III-V planar MOSFETs to date, to the author's best knowledge for now. Most III-V MOSFETs suffers from relative large subthresh-

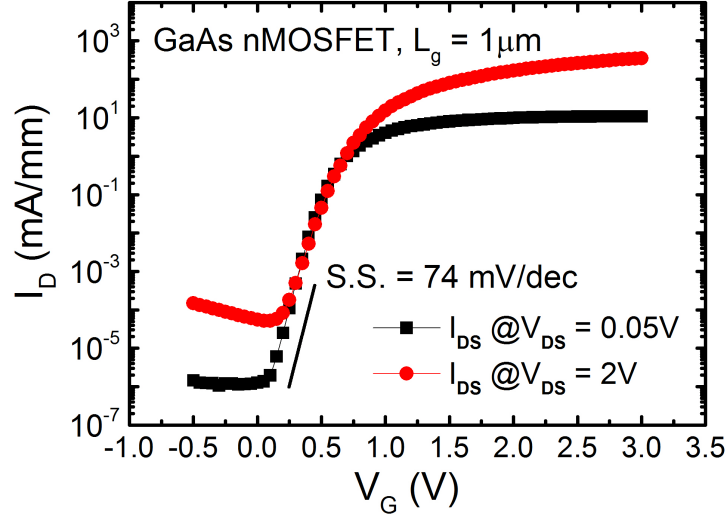


Fig. 3.27. Transfer characteristics ($I_{DS} \sim V_{GS}$) for the same device shown in Fig. 3.26. A low subthreshold (SS) of 74 mV/dec is obtained from the transfer curve measured with $V_{DS} = 0.05$ V. The current on/off ratio is $\sim 10^7$, showing the advantage of relative wide band gap of GaAs comparing to the narrower band gap semiconductors like InGaAs.

old slope due to the high density of traps at the oxide-semiconductor interface, which is critical for inversion layer formation. Besides the high current drivability and fast switching speed, the current ON/OFF ratio of the GaAs nMOSFETs is $\sim 10^7$, and this can be ascribed to the relative large band gap (~ 1.42 eV) for GaAs, comparing to narrower band gap semiconductors like InGaAs and InAs. The semi-insulating substrates, not available in silicon, contributes to the excellent off-state properties and is also necessary to reduce cross talk between high speed signal lines in dense GaAs circuits [45].

Fig. 3.28 shows the linear transfer characteristics as well as the extrinsic transconductance of a $1\mu\text{m}$ -gate-length GaAs enhancement-mode nMOSFET. The peak transconductance obtained from the curve with $V_{DS} = 2\text{V}$ is around 190 mS/mm. The effective

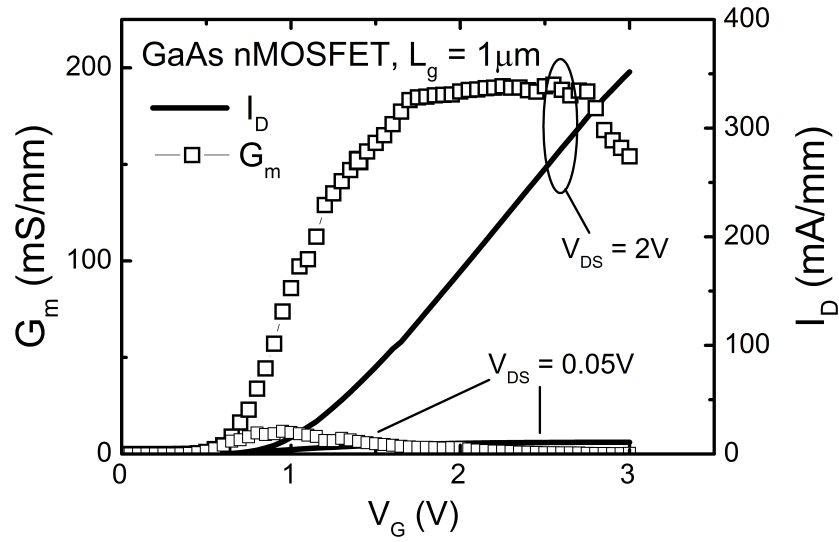


Fig. 3.28. Linear transfer characteristics and extrinsic transconductance (g_m) versus V_{GS} for the same device of Fig. 3.26.

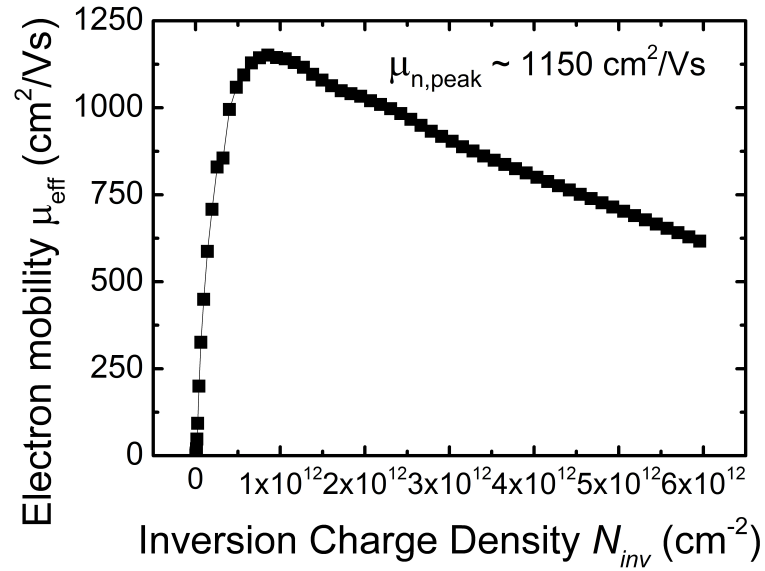


Fig. 3.29. Effective electron mobility extracted from a $L_G = 8 \mu\text{m}$ GaAs(111)A nMOSFET with GaAs/ La_2O_3 epitaxial interface. The peak mobility reaches $1150 \text{ cm}^2/\text{V}\cdot\text{s}$.

electron mobility is depicted in Fig. 3.29. The peak electron mobility is about $1150 \text{ cm}^2/\text{V}\cdot\text{s}$, which is much higher than the GaAs nMOSFETs with $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ epitaxial dielectric we presented in the previous section, showing an excellent interface quality enhancement due to better crystalline lattice matching.

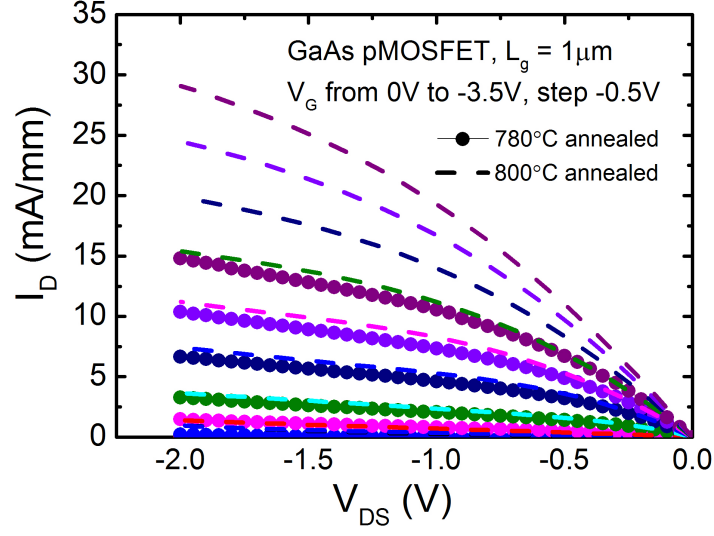


Fig. 3.30. Output characteristics ($I_{DS} \sim V_{DS}$) for $L_G = 1 \mu\text{m}$ GaAs(111)A pMOSFETs with GaAs/ La_2O_3 epitaxial interface annealed with P+ ion activation at 780°C for 30s and 800°C for 15s. The maximum drain current is $\sim 30 \text{ mA/mm}$ with a gate bias of -3.5 V and a drain bias of -2 V from the pMOSFET device with 800°C annealing.

The output and transfer characteristics of a $1 \mu\text{m}$ -gate-length enhancement-mode GaAs(111)A pMOSFETs with 780°C and 800°C ion activation annealing are plotted and compared in Fig. 3.30 and Fig. 3.31, respectively. The maximum drain current obtained is $\sim 30 \text{ mA/mm}$ for the GaAs pMOSFET annealed at 800°C and $\sim 15 \text{ mA/mm}$ for the pMOSFET annealed at 780°C . Higher annealing temperature leads to larger drain current but also decreased the current ON/OFF ratio of GaAs pMOSFETs (10^4) comparing to nMOSFETs (10^7), and this can be ascribed to the fast

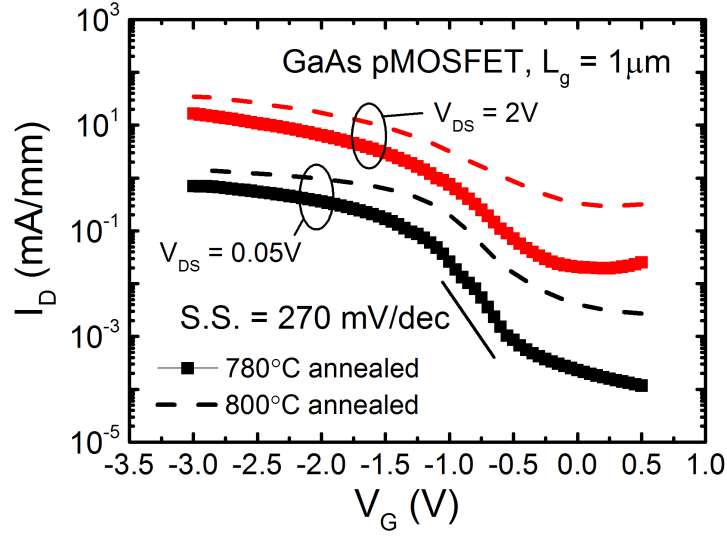


Fig. 3.31. Transfer characteristics ($I_{DS} \sim V_{GS}$) for the same devices shown in Fig. 3.30. A subthreshold (SS) of 270 mV/dec is obtained from the transfer curve measured with $V_{DS} = 0.05$ V, for the GaAs pMOSFET with 780 °C ion activation annealing.

Zn dopant diffusion in GaAs under high-temperature conditions. Consequently, a better SS of ~ 270 mV/dec for the device annealed at 780°C is observed, compared with the devices annealed at higher temperature. Apparently the off-state current of the GaAs pMOSFETs are greatly compromised by the high thermal budget induced by the annealing process, therefore the ion activation of the S/D regions needs to be further optimized in the future to accommodate to ultra-scaled devices with low stand-by power consumption.

The linear transfer characteristics, along with the extrinsic transconductance of the 1 μm -gate-length enhancement-mode GaAs(111)A pMOSFETs are shown in Fig. 3.32. Similarly, with the help of split-CV method we can also plot the effective hole mobility of GaAs pMOSFETs in Fig. 3.33. The peak hole mobility is about 180 $\text{cm}^2/\text{V}\cdot\text{s}$, which is obtained at low N_{inv} region. The relative low hole mobility

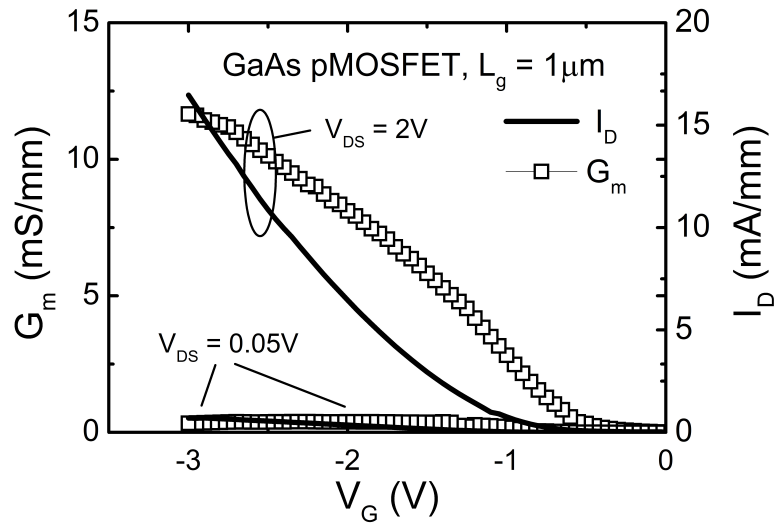


Fig. 3.32. Linear transfer characteristics and extrinsic transconductance (g_m) versus V_{GS} for the same device annealed at 780°C for 30s of Fig. 3.30.

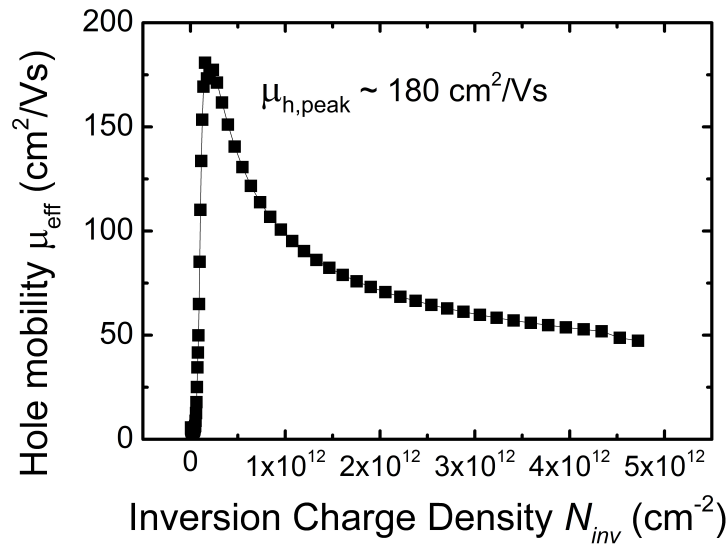


Fig. 3.33. Effective electron mobility extracted from a $L_G = 8 \mu\text{m}$ GaAs(111)A pMOSFET with GaAs/ La_2O_3 epitaxial interface. The peak mobility reaches $180 \text{ cm}^2/\text{V}\cdot\text{s}$.

is mainly throttled by the intrinsic electrical property of GaAs, which has the hole mobility below $400 \text{ cm}^2/\text{V}\cdot\text{s}$.

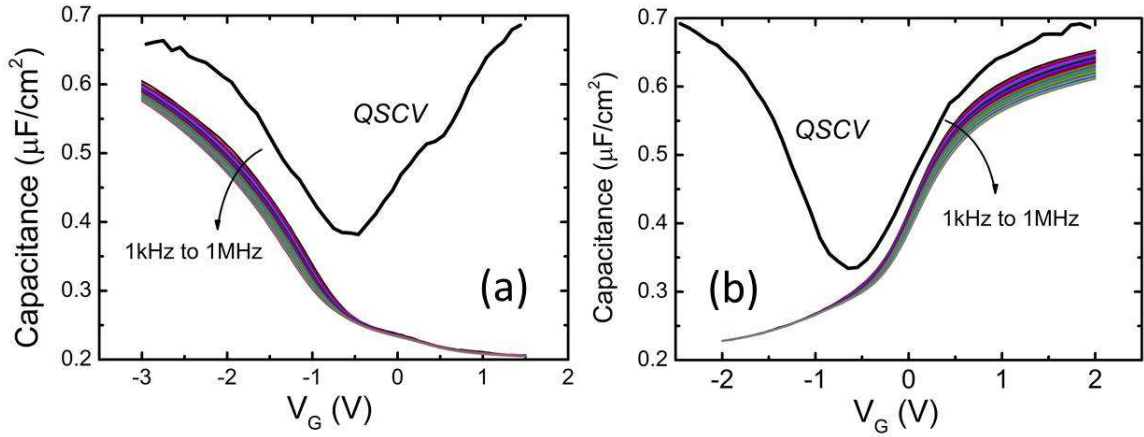


Fig. 3.34. Quasistatic and high-frequency Capacitance-Voltage characteristics measured from both p-type and n-type capacitors with $\text{La}_2\text{O}_3/\text{GaAs}$ epitaxial interface.

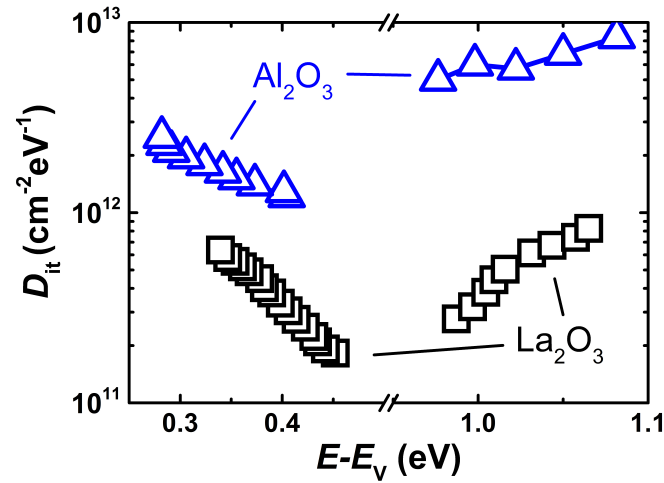


Fig. 3.35. Comparison of D_{it} distribution of amorphous $\text{Al}_2\text{O}_3/\text{GaAs}(111)\text{A}$ and epi-taxial $\text{La}_2\text{O}_3/\text{GaAs}(111)\text{A}$ interfaces in the GaAs band-gap. The values were determined by the conductance method.

Both p-type and n-type high frequency and quasi-static CV characteristics are plotted in Fig. 3.34. The high frequencies CV taken from 1 kHz to 1 MHz show small frequency dispersion at accumulation regions. Surface potentials were determined from the quasi-static CV characteristics using Berglunds equation. The surface potential is 0.94 eV at a gate bias of 1.5 V calculated from p-type CV, while from the n-type CV the surface potential is determined to be 1.06 eV at a gate bias of -2 V. Both the calculated surface potentials are much larger than half of the GaAs band gap (~ 0.71 eV), suggesting that the Fermi level is not pinned at the GaAs mid gap. The room temperature conductance method was employed to determine D_{it} [2], which is greatly reduced compared to the amorphous $\text{Al}_2\text{O}_3/\text{GaAs}(111)\text{A}$ system, as shown in Fig. 3.35.

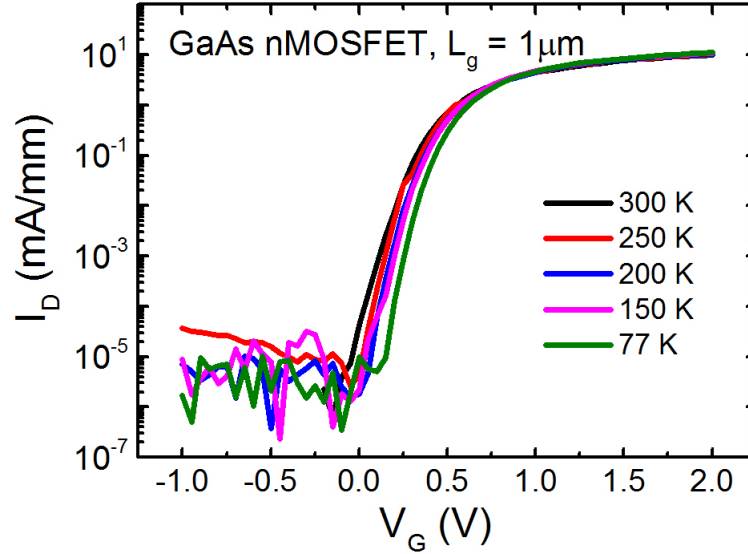


Fig. 3.36. Measured temperature dependent transfer characteristics of a 1 μm -gate-length GaAs nMOSFET with $\text{La}_2\text{O}_3/\text{GaAs}(111)\text{A}$ interface. The drain bias applied is 0.05 V.

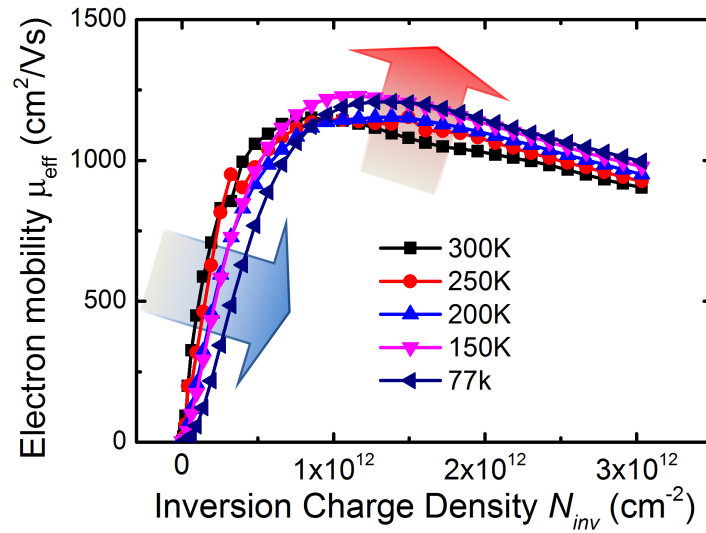


Fig. 3.37. Effective electron mobility versus inversion charge density is plotted in the 77K to 300K temperature range. The mobility increased at low temperature due to less phonon scattering.

The temperature-dependent transfer characteristics of a 1 μm -gate-length GaAs nMOSFET with $\text{La}_2\text{O}_3/\text{GaAs}(111)\text{A}$ interface and corresponding electron effective mobility is shown in Fig. 3.36 and Fig. 3.37. The slight increase of the mobility in moderate N_{inv} is due to less phonon scattering while the decreasing mobility at low N_{inv} suggests strong influence of Coulomb scattering at lower temperature.

3.3 First GaAs CMOS digital circuits demonstration

From the early Silicon technology, people realized that low stand-by power dissipation could be achieved by the digital circuits built with p- and n-channel MOSFETs on the same chip connected in series. This type of circuits is named complementary MOS transistor (CMOS) circuits. The basic building block of the CMOS digital circuits is an inverter, whose output is the inverse of its input. Arbitrary complicated logic circuits can be realized by the suitable connection of numerous inverters.

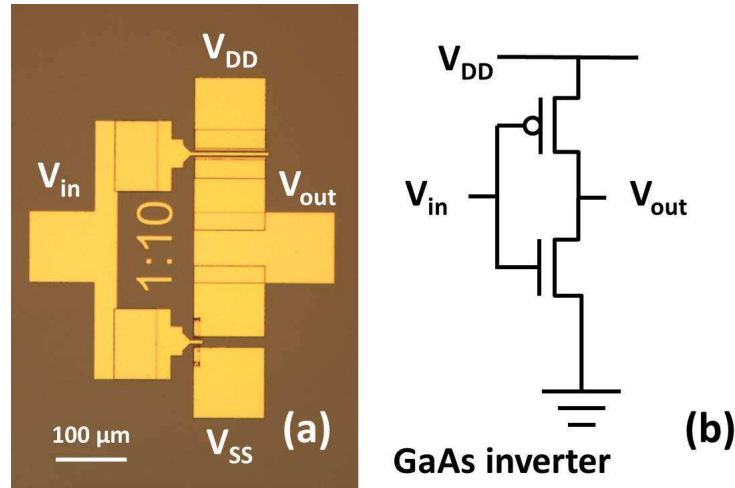


Fig. 3.38. (a) Optical micrograph of a GaAs CMOS inverter. The devices gate width ratio of nMOSFET to pMOSFET in this inverter is 1:10. (b) Circuit schematic of a CMOS inverter.

Fig. 3.38 shows the optical micrograph and schematic of a GaAs CMOS inverter fabricated in this work. The inverter has a width ratio of nMOSFET to pMOSFET 1:10. The threshold voltage of the GaAs nMOSFET is determined to be $\sim 0.7\text{V}$ and pMOSFET is determined to be $\sim -0.9\text{ V}$, using the method of linear extrapolation of the transfer curve at low V_{DS} bias. The inverter voltage transfer characteristics are plotted in Fig. 3.39, measured at different supply voltages ($V_{DD} = 2\text{V}$, 2.5V and 3V). This transfer characteristics is often employed for the evaluation of the quality of an logic inverter. The GaAs inverter functions as follows (take power supply V_{DD} of 2.5 V for example): when the input voltage V_{in} is 2.5 V (logic state "1"), the nMOSFET below is at on-state due to the $V_{GS,nFET} = 2.5\text{ V}$, which means the channel of nMOSFET is much more conductive than the pMOSFET. As a result, the output voltage V_{out} is pulled down to around 0.1 V (logic state "0"). When the input voltage V_{in} is 0 V (logic state "0"), the pMOSFET above is at on-state due to the $V_{GS,pFET} = -2.5\text{ V}$, while the nMOSFET is at off-state ($V_{GS,pFET} = 0\text{ V}$). At

this time channel of pMOSFET is much more conductive than the nMOSFET, and therefore the output voltage V_{out} is close to 2.5 V (logic state "1"). The corresponding inverter gain determined by the slope of the inverter transfer characteristics is shown in Fig. 3.40, and a gain of ~ 12 is obtained with $V_{DD} = 3$ V. The higher inverter gain obtained with larger drain bias is ascribed to the higher current drivability of the GaAs MOSFETs.

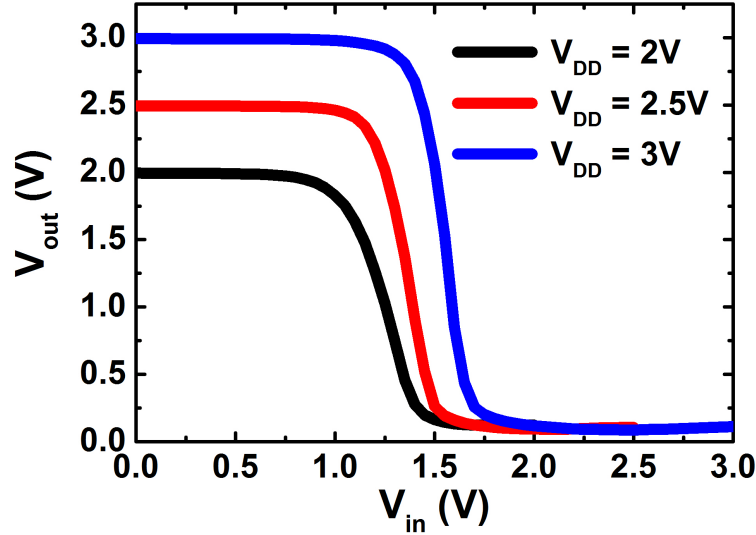


Fig. 3.39. Transfer characteristics of a GaAs CMOS inverter, measured with different supply voltages $V_{DD} = 2V$, 2.5V and 3V.

The GaAs CMOS logic circuit operation is further demonstrated by NAND and NOR logic gates. NAND gate stands for Negated AND or NOT AND in digital circuits. The NAND logic gate produces an output that is false ("0") only if all its inputs are true ("1") (see table). Fig. 3.41 shows the optical micrographs and schematic illustrations of the NAND logic gate, and we can see the NAND gate consists of two pMOSFETs connected in parallel and two nMOSFETs connected in series. The measured corresponding NAND logic gate voltage outputs is plotted in

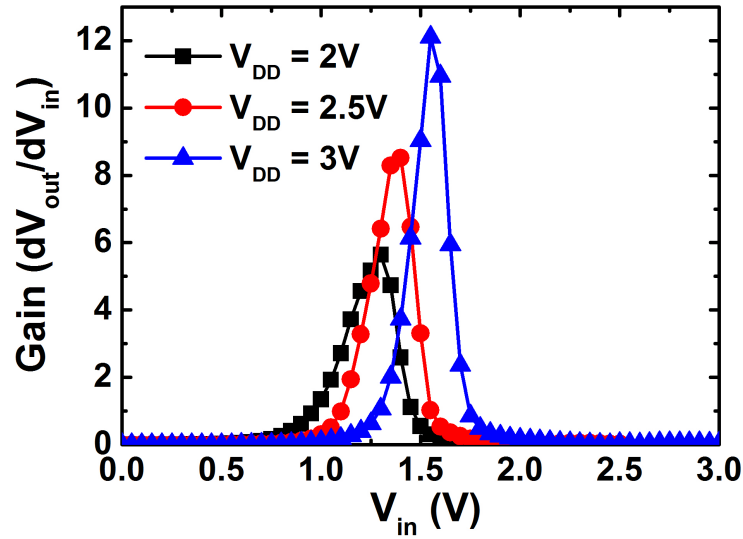


Fig. 3.40. GaAs CMOS inverter gain (dV_{out}/dV_{in}) as a function of input voltage. A gain of ~ 12 is achieved with $V_{DD} = 3V$.

Fig. 3.42, and four combinations of input states 1 1, 0 1, 1 0 and 0 0 and corresponding output states are marked.

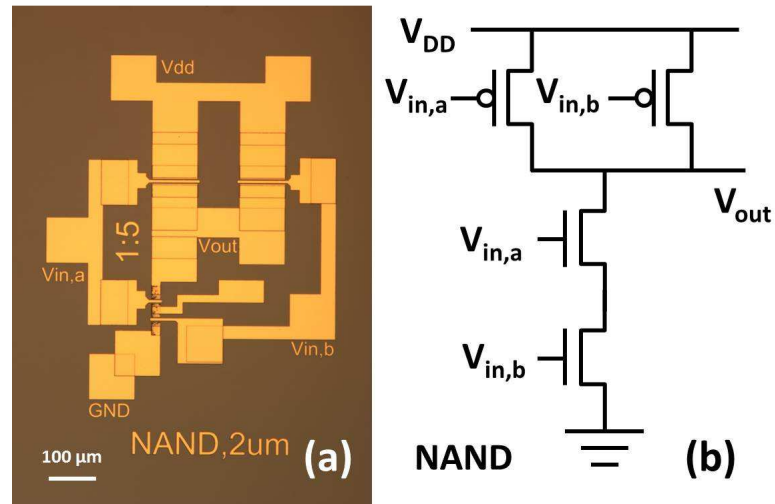


Fig. 3.41. (a) Optical micrograph of a GaAs CMOS NAND logic gate. The devices gate width ratio of nMOSFET to pMOSFET in this inverter is 1:5. (b) Circuit schematic of a CMOS NAND gate.

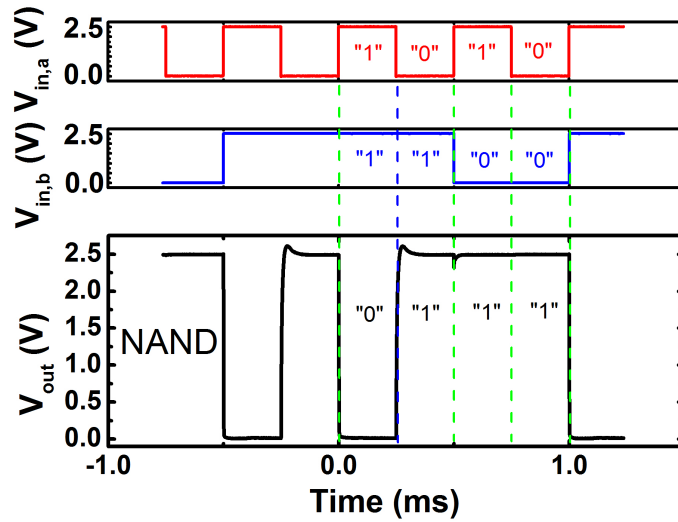


Fig. 3.42. Input V_{in} and output voltage V_{out} of the GaAs CMOS NAND logic gate in Fig. 15. Four combinations of input states 1 1, 0 1, 1 0 and 0 0 and corresponding output states are marked.

The GaAs CMOS NOR logic gates are also fabricated and demonstrated. NOR is the result of the negation of the OR operator, and it consists of two pMOSFETs connected in series mode and two nMOSFETs in parallel mode, as illustrated in Fig. 3.43.A HIGH output ("1") results if both the inputs to the gate are LOW ("0"); if one or both input is HIGH ("1"), a LOW output ("0") results. The measured corresponding NOR logic gate voltage outputs is plotted in Fig. 3.44, and four combinations of input states 1 1, 0 1, 1 0 and 0 0 and corresponding output states are highlighted.

The supply voltage V_{DD} used in all the logic gates is 2.5V, and for both input and output voltages the logic 1 is corresponding to 2.5V while the logic 0 is corresponding to 0V (GND). With the well behaved GaAs CMOS inverters, five-stage ring oscillators are also demonstrated. As shown in Fig. 3.45, a five stage ring oscillator was built by connecting five inverter stages in a close loop chain with an extra inverter stage

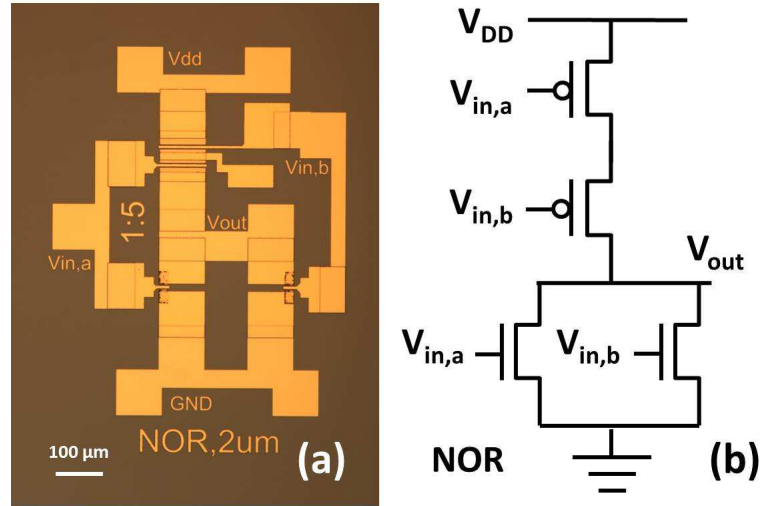


Fig. 3.43. (a) Optical micrograph of a GaAs CMOS NOR logic gate. The devices gate width ratio of nMOSFET to pMOSFET in this inverter is 1:5. (b) Circuit schematic of a CMOS NOR gate.

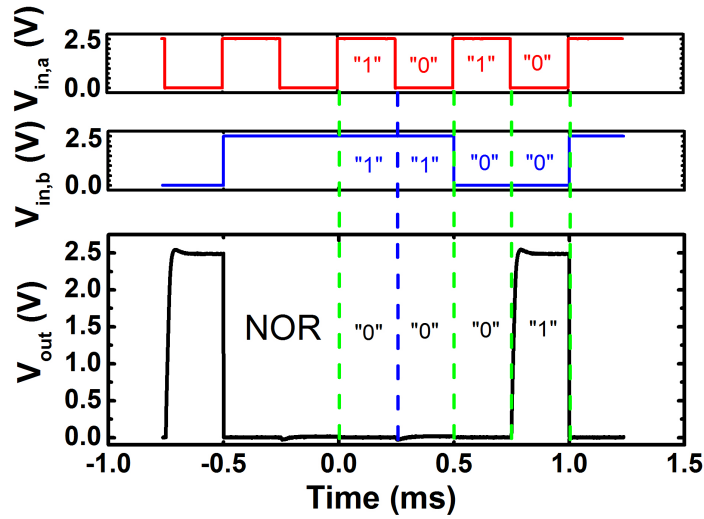


Fig. 3.44. Input V_{in} and output voltage V_{out} of the GaAs CMOS NOR logic gate in Fig. 15. Four combinations of input states 1 1, 0 1, 1 0 and 0 0 and corresponding output states are marked.

for the output signal measurement, which was connected to a digital oscilloscope or a spectrum analyzer.

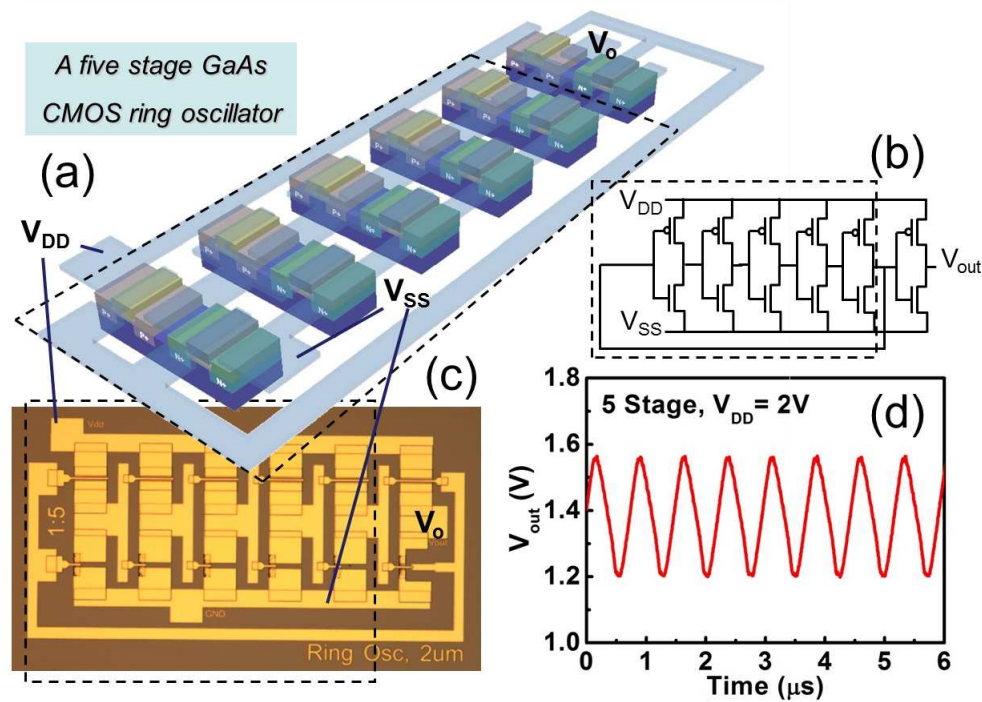


Fig. 3.45. (a) Schematic illustration, (b) circuit schematic, (c) optical micrograph and (d) output characteristics of a GaAs CMOS five-stage ring oscillator. The dash line denotes the five stage inverters in the ring oscillator.

Fig. 3.45(a) is a 3D schematic view of the 5-stage ring oscillator while Fig. 3.45(b) and (c) are the schematic illustration of a 5-stage CMOS ring oscillator and a optical micrograph taken from the fabricated sample, respectively. As shown in Fig. Fig. 3.45(d), at $V_{DD} = 2V$, the fundamental oscillation frequency is at 1.1 MHz, which is consistent with the output signal in its frequency power spectrum as shown in Fig. 3.46. The fundamental resonance frequency increases from 0.35 MHz at $V_{DD} = 1V$ to 3.87 MHz at $V_{DD} = 2.75V$. Also, the signal peak increases from 50 dBm to -20 dBm as V_{DD} increased from 1V to 2.75V. Both the frequency performance

and the power performance increased as the drain current of the transistors increases. At $V_{DD}=2.75\text{V}$, the corresponding propagation delay of each stage can be calculated using $\tau = 1/(2nf) = 25.8 \text{ ns}$, where n is the number of stages and f is the fundamental oscillation frequency.

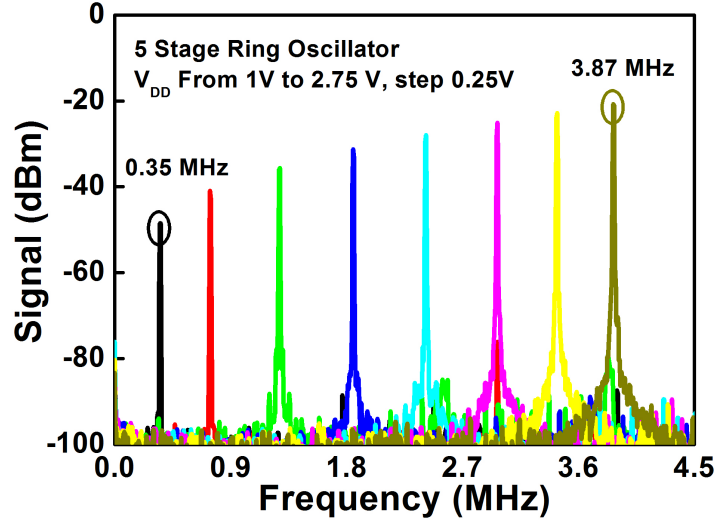


Fig. 3.46. Measured output power spectrum of a five-stage GaAs CMOS ring oscillator. The fundamental oscillation frequency increases from 0.35 MHz to 3.87 MHz as V_{DD} increases from 1 V to 2.75 V.

3.4 Summary

Conclusion: By realizing a high-quality epitaxial $\text{La}_2\text{O}_3/\text{GaAs}(111)\text{A}$ interface, we demonstrate GaAs CMOS devices and integrated circuits including nMOSFETs, pMOSFETs, CMOS inverters, NAND and NOR logic gates and a five-stage ring oscillator. As an exercise of III-V CMOS circuits on a common substrate with a common gate dielectric, it provides a route to realize ultimate high-mobility CMOS on Si if long-time expected breakthroughs of III-V epi-growth on Si occur.

4. GE MOSFETS WITH EPITAXIAL $\text{La}_2\text{O}_3/\text{Ge}(111)$ INTERFACES

4.1 Introduction

Germanium, which was originally used as transistor fabrication, is of great interest as a channel material for future technology nodes, owing to its bulk electron and hole mobilities that are approximately two and four times higher than those of Si, respectively. The small hole conductivity effective mass and hence can achieve higher inversion hole mobility. Also, the high density of states of Ge allows for it to support channel charge in its higher mobility valleys even with strong quantization attributed either to the spatial quantum confinement or to the high electric field. This makes Ge an attractive channel material for future high-performance MOSFETs. However, the replacement of Si channel by Ge in these devices requires alternative high κ gate dielectrics that can form a thermodynamically interface with Germanium itself.

Although enormous efforts have been put in the Ge MOSFETs study, The main hurdle of the Ge application is the lack of a robust gate dielectric oxide. Different surface passivation techniques like insertion of a thin SiO_2 /amorphous Si layer [46,47], and various gate oxides such as ZrO_2 [48], LaLuO_3 [49] and HfO_2 [50] have been used. The best gate oxide which can form a good oxide-semiconductor interface with low density of traps to date is GeO_2 [51–54], which is the native oxide of Ge. However, the GeO_2 suffers from low dielectric constant which would greatly compromise the gate oxide film thickness scaling in future high-speed low-power consumption digital logic devices. Therefore, the search of a thermodynamically stable high- κ dielectric is significant for the future Ge application.

An epitaxial interface, Ge(111)/LaYO₃ was previously discovered and reported by our group. The relative higher dielectric constant of La-based oxide (16 ~ 20) and excellent thermal stability proved in previous chapters of GaAs MOSFETs make it great candidate to serve as gate dielectric on Ge.

In this chapter, we present the demonstration of Ge pMOSFETs and nMOSFETs with the integration of epitaxial La₂O₃/Ge(111) interface, which is realized by Atomic Layer Deposition. The Ge MOSFETs show decent drive current and moderate sub-threshold slopes, which suggest the good quality of the epitaxial interface.

4.2 Ge pMOSFETs and nMOSFETs with La₂O₃/Ge(111) epitaxial interfaces

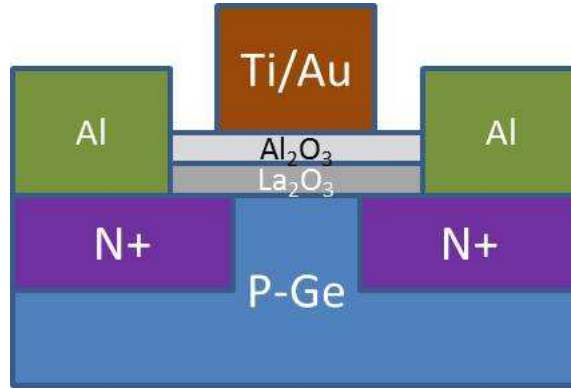


Fig. 4.1. (a) Cross-sectional TEM image of La₂O₃/Ge(111)A epitaxial interface, and (b) the corresponding electron diffraction pattern taken from the same sample as shown in (a).

Fig. 4.1. shows the cross sectional view of the Ge nMOSFETs fabricated in this work. The Ge nMOSFETs started from the Ge(111) p-type substrates (Ga doped) with resistivity of 0.005-0.04 $\Omega\cdot\text{cm}$. The substrates were first degreased with acetone, methanol and isopropanol, then the Ge native oxides were stripped with cyclic clean (repeatedly diluted HF dip and DI water rinse). 6 nm La₂O₃ and 6 nm

Al_2O_3 encapsulation layer were sequentially deposited on the Ge surface, and the detail of the ALD process can be found in previous chapters. The epitaxial interface can be achieved with the La_2O_3 layer formation, as shown in Fig. 4.2. The picture shows 10 nm single crystalline La_2O_3 formed on the Ge(111) substrate, and the inset is the electron diffraction pattern taken from the same sample, indicating the epitaxial structure between the substrate and the oxide film above.

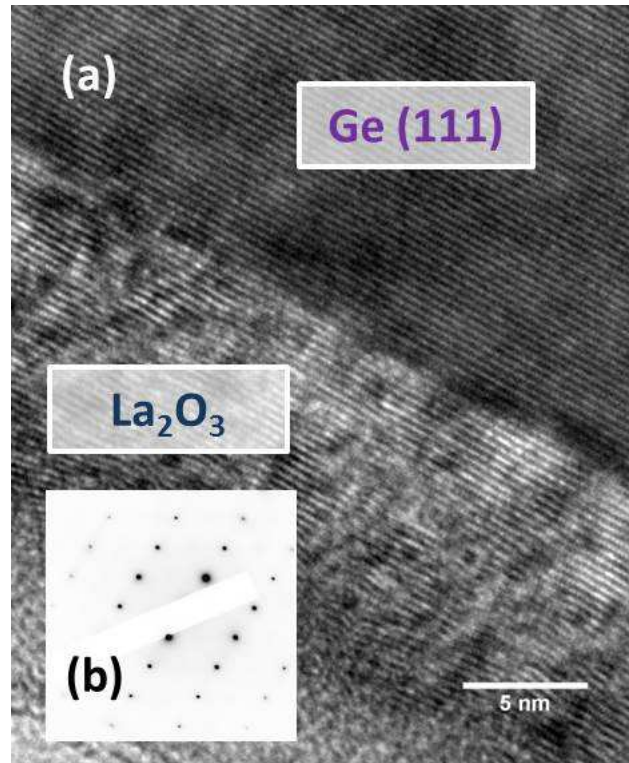


Fig. 4.2. (a) Cross-sectional TEM image of $\text{La}_2\text{O}_3/\text{Ge}(111)$ A epitaxial interface, and (b) the corresponding electron diffraction pattern taken from the same sample as shown in (a).

After the gate dielectric film deposition, source and drain area were defined by photolithography and Phosphorous ion implantation with a dose of $5 \times 10^{15} \text{ cm}^{-2}$ at 30 keV. Then ion activation annealing at 590 °C for 30 seconds in N_2 ambient was performed. The S/D regions were again defined by photolithography and the

oxide stacks above these regions were removed by diluted BOE solution (1:5) and HCl solution. Ohmic contact was formed by the e-beam evaporation of Al, followed by a lift-off process. The device fabrication was finally completed by the formation of Ti/Au gate electrode.

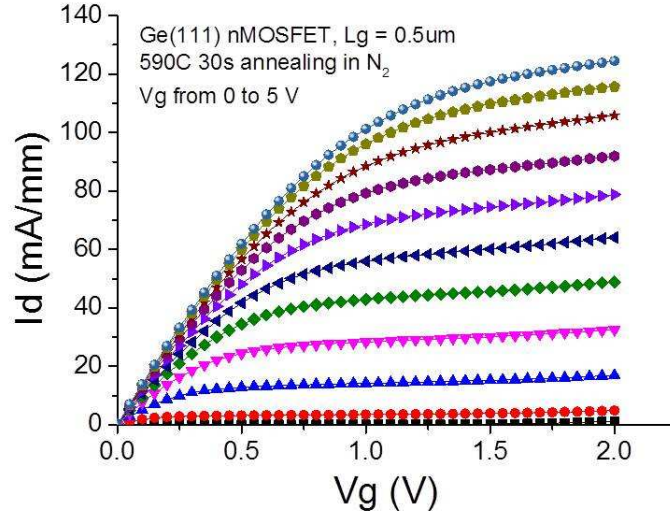


Fig. 4.3. Output characteristics ($I_{DS} \sim V_{DS}$) for a $L_G = 0.5\mu\text{m}$ Ge(111) nMOSFET with Ge/La₂O₃ epitaxial interface. The maximum drain current is around ~ 124 mA/mm with a gate bias of 5 V and a drain bias of 2 V.

The output characteristics of a $L_G = 0.5\mu\text{m}$ Ge(111) nMOSFET with Ge/La₂O₃ epitaxial interface is shown in Fig. 4.3. A high drain current of 124 mA/mm is obtained at a gate bias of 5 V. The transfer characteristics of the corresponding nMOSFET is plotted in Fig. 4.4. Due to the un-optimized fabrication process the drain current is much larger than the source current because of the junction leakage when gate voltage is less than 0 V. And the drain current increased with negative gate bias, which is ascribed to the gate induced drain leakage. The junction performance can be further investigated by the junction current measurement, as shown in Fig. 4.5.

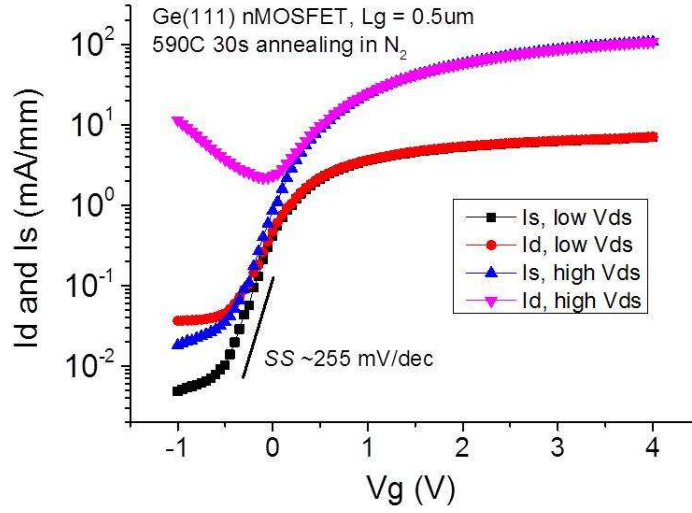


Fig. 4.4. Transfer characteristics (I_D and $I_S \sim V_{GS}$) for the same device shown in Fig. 4.3. A subthreshold (SS) of 255 mV/dec is obtained from the transfer curve $I_S \sim V_G$ measured with $V_{DS} = 0.05$ V. The difference between drain current and source current is due to the junction leakage induced by unoptimized fabrication process.

The current ratio of the N+/P diode is $\sim 10^3$, which needs to be further improved by careful ion-implantation and activation process.

The contact resistance and the sheet resistance of the ion implanted area can be determined by the transmission line method (TLM) structure, which is composed of $100\mu\text{m} \times 100\mu\text{m}$ squares with $5 \sim 80\mu\text{m}$ distance apart. The TLM measurement is plotted in Fig. 4.6. The contact resistance of the S/D part is $0.57 \Omega \cdot \text{mm}$ and the sheet resistance of the N+ area is extracted $65.7 \Omega/\square$.

Similar to the Ge nMOSFET fabrication, the Ge pMOSFET fabrication started from n-type Ge(111) substrate (Sb-doped) with resistivity of $0.05\text{-}0.5 \Omega \cdot \text{cm}$. The substrates were cleaned and the same 6 nm La_2O_3 and 6 nm Al_2O_3 oxide stacks as Ge nMOSFETs were deposited as gate dielectrics while a $\text{La}_2\text{O}_3/\text{Ge}(111)$ epitaxial interface is formed. Source and drain areas were then defined by photolithography and

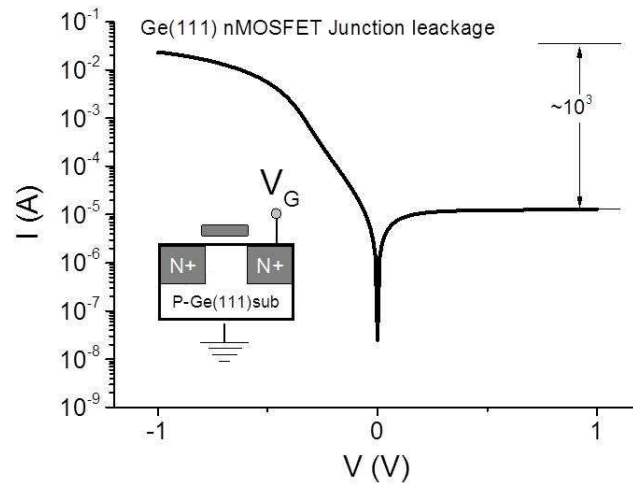


Fig. 4.5. I-V characteristics of the Ge N^+ -P junctions formed by phosphorous ion implantation and activation annealing at 590 °C for 30 seconds. Relative high junction leakage current and low current ratio $\sim 10^3$ is obtained due to the un-optimized fabrication process.

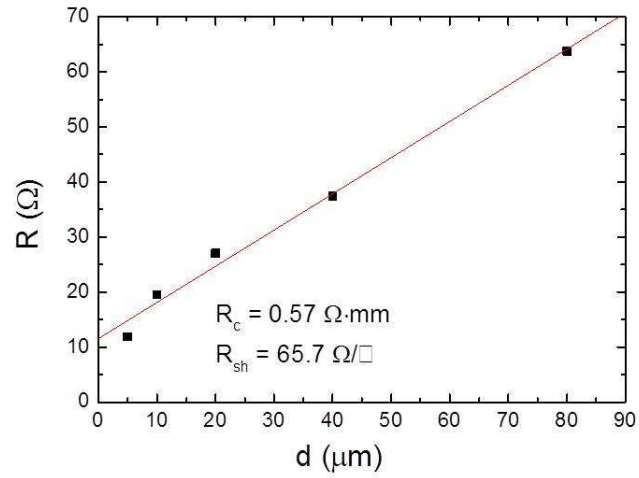


Fig. 4.6. The contact resistance R_c of the Ge nMOSFETs and sheet resistance of the implanted areas (N^+) extraction with the transmission line methods (TLM).

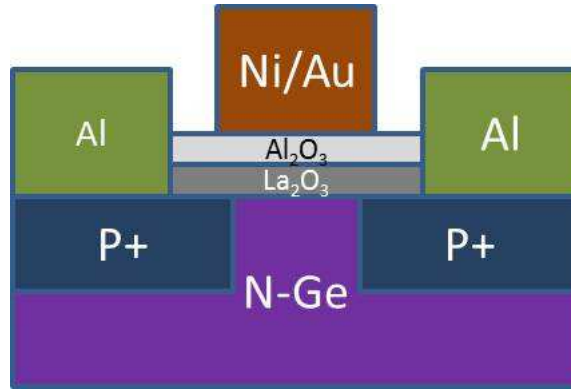


Fig. 4.7. Schematic view of an Ge(111) inversion-mode pMOSFET with ALE La_2O_3 as gate dielectric.

BF_2 ion implantation with a dose of $1 \times 10^{15} \text{ cm}^{-2}$ at 10 keV. Then ion activation was performed by a two-step annealing process in a rapid thermal process (RTP) system at 350°C for 30 minutes and then at 550°C for 30 seconds in N_2 . Same as the nMOSFETs process, the S/D metal Ohmic contacts were formed by e-beam evaporation of Al and Ni/Au is adopted as the gate electrode. The finished Ge pMOSFET's cross-sectional view is depicted in Fig. 4.7.

The $I_D - V_D$ output characteristics of a $L_G = 0.5\mu\text{m}$ Ge(111) pMOSFET with Ge/ La_2O_3 epitaxial interface is shown in Fig. 4.8. The maximum drain current is around 63 mA/mm at $V_G = -5 \text{ V}$. The corresponding transfer characteristics is plotted in Fig. 4.9. The dopants were effectively activated by the annealing of 350°C for 30 minutes and the P+/N diode junction quality was greatly improved due to the 550°C annealing, as shown in Fig. 4.10. The current ratio is $\sim 10^4$, from the two terminal DC measurement results of the P+/N diode. Comparing to the Ge nMOSFETs, the current I_D on/off ratio of Ge pMOSFETs is $\sim 10^3$ while for source current I_S is $\sim 10^5$. A threshold slope of 195 mV/dec is achieved, indicating good interface quality of the epitaxial $\text{La}_2\text{O}_3/\text{Ge}(111)$ structure.

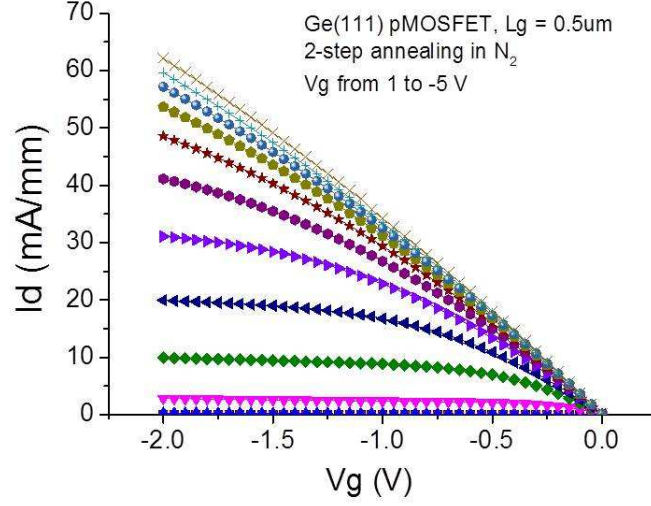


Fig. 4.8. Output characteristics ($I_{DS} \sim V_{DS}$) for a $L_G = 0.5\mu\text{m}$ Ge(111) pMOSFET with Ge/ La_2O_3 epitaxial interface. The maximum drain current is around $\sim 124\text{ mA/mm}$ with a gate bias of 5 V and a drain bias of 2 V.

The split-CV characteristics were measured from a $L_G = 8\mu\text{m}$ Ge(111) pMOSFET (see Fig. 4.11), and the 1 kHz - 1 MHz CV shows small frequency dispersion, which suggests low D_{it} near the valence band edge. With the help of split-CV the effective hole mobility can be determined, as shown in Fig. 4.12. The peak hole mobility is $270\text{ cm}^2/\text{V}\cdot\text{s}$, obtained at low inversion charge region ($N_{inv} \sim 1 \times 10^{12}\text{ cm}^{-2}$).

4.3 Summary

In conclusion, we have demonstrated high performance Ge nMOSFETs and pMOSFETs with integration of higher- κ La_2O_3 gate dielectrics. The maximum drain current of the nMOSFET is $\sim 124\text{ mA/mm}$ and for the pMOSFET is $\sim 64\text{ mA/mm}$. Relative small subthreshold slopes SS of 195 mV/dec is obtained from pMOSFETs and 255 mV/dec from nMOSFETs, benefit from the high quality $\text{La}_2\text{O}_3/\text{Ge}(111)$ interface. The measured split-CV characteristics from a $8\mu\text{m}$ -gate-length Ge pMOSFET shows

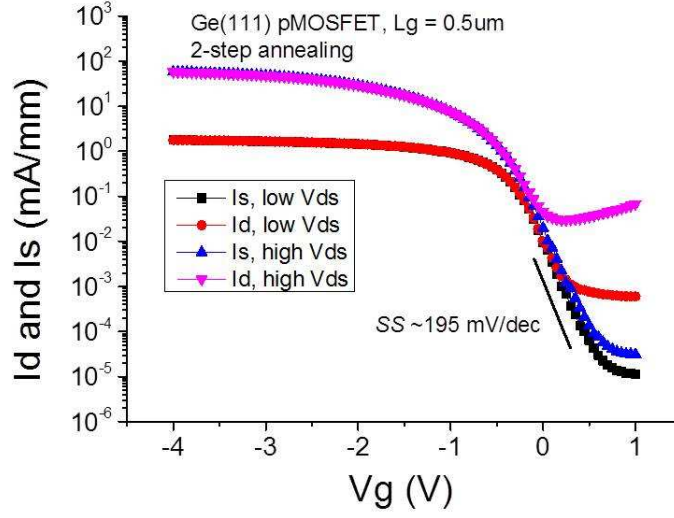


Fig. 4.9. Transfer characteristics (I_D and $I_S \sim V_{GS}$) for the same device shown in Fig. 4.3. A subthreshold (SS) of 255 mV/dec is obtained from the transfer curve $I_S \sim V_G$ measured with $V_{DS} = 0.05$ V. The difference between drain current and source current is due to the junction leakage induced by unoptimized fabrication process.

small frequency dispersion and the peak effective hole mobility is extracted to be about $270 \text{ cm}^2/\text{V}\cdot\text{s}$. While the epitaxial interface appears to be promising in future Ge high-speed low-power device applications, more work needs to be done on the process optimization to further device performance enhancement.

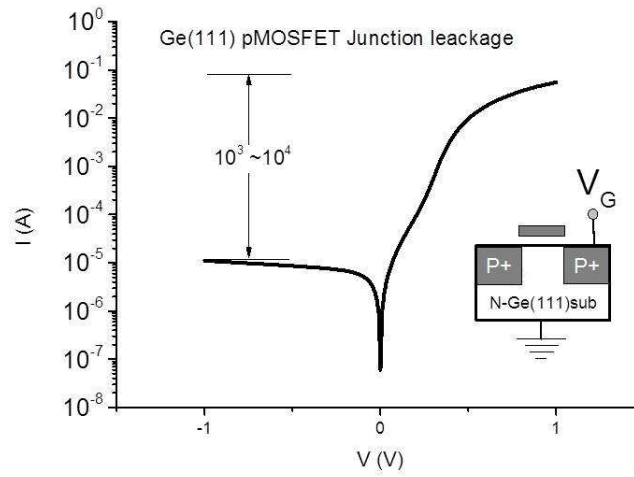


Fig. 4.10. Rectifying characteristics of the Ge P^+ -N junctions formed by phosphorous ion implantation and two-step annealing process. Better junction performance is obtained comparing to the N^+ -P junctions.

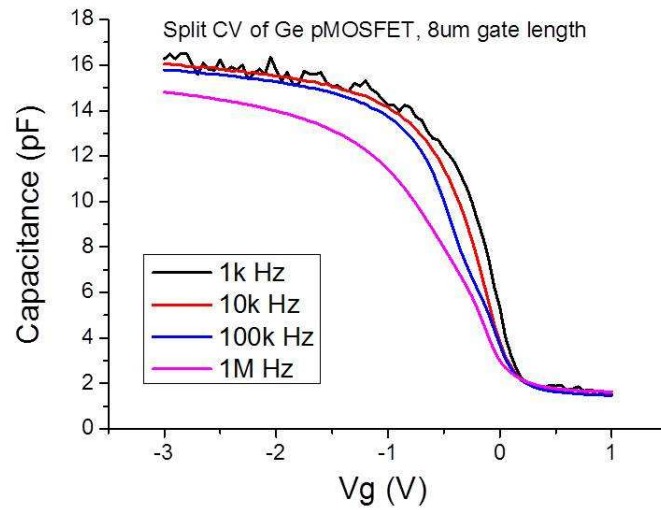


Fig. 4.11. Split-CV characteristics measure from a $L_G = 8\mu\text{m}$ Ge(111) pMOSFET with Ge/ La_2O_3 epitaxial interface. Small frequency can be observed from the 1 kHz to 1 MHz CV characteristics, indicating low density of traps at the Ge/ La_2O_3 interface.

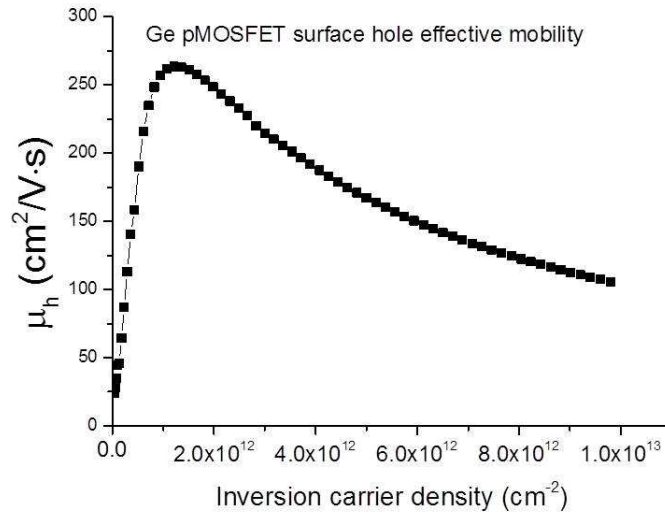


Fig. 4.12. Effective electron mobility extracted from a $L_G = 8\mu\text{m}$ Ge(111) pMOSFET with Ge/La₂O₃ epitaxial interface. The peak hole mobility is $\sim 270 \text{ cm}^2/\text{V}\cdot\text{s}$, obtained at low inversion charge region ($N_{inv} \sim 1 \times 10^{12} \text{ cm}^{-2}$)

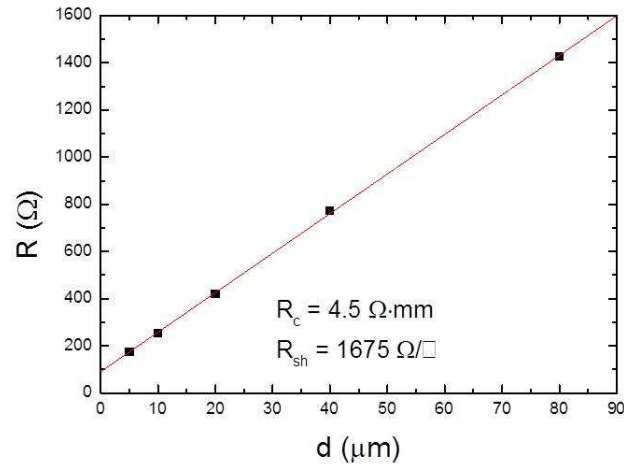


Fig. 4.13. The contact resistance R_c of the Ge pMOSFETs and sheet resistance of the implanted areas (P+) extraction with the transmission line methods (TLM).

5. SRTiO₃ MOSFETS WITH ALD LAAlO₃ GATE DIELECTRICS

5.1 Introduction

The class of transition metal oxide compounds exhibit a broad range of functional properties, such as high dielectric permittivity, piezoelectricity and ferroelectricity, superconductivity, spin polarized current, colossal magnetoresistance and ferromagnetism. Almost all these phenomenology result from strongly correlated electronic behavior and turned out to be very sensitive to external parameters such as electric and magnetic fields, internal or external pressure and so on. Polarity discontinuities at the interfaces between two different crystalline materials or called hetero-interfaces are believed to be the key to lead to nontrivial effects.

In 2004, Ohtomo and Hwang reported a high-mobility electron gas could be formed at the crystalline LaAlO₃/SrTiO₃ hetero-interface (as shown in Fig. 5.1) with the materials grown at ultra-high vacuum and by pulsed laser deposition technique (PLD). [55, 56] For very long time, it is widely believed that the oxide-oxide interface needs to be atomically engineered by hetero-epitaxial growth in order to achieve a conducting channel. Later, some research group reported that conducting channel can be achieved on SrTiO₃ with some PLD amorphous dielectrics formed under high temperature and high vacuum conditions. [57–60] In this chapter, we for the first time demonstrate that the conducting channel can also be formed at insulating amorphous LaAlO₃/insulating crystalline SrTiO₃ (100) interface by low temperature (300°C) and low vacuum (0.35Torr) atomic-layer-deposition technique. Well-behaved LaAlO₃/SrTiO₃ all oxide field-effect transistors (FETs) are realized with gate dielec-

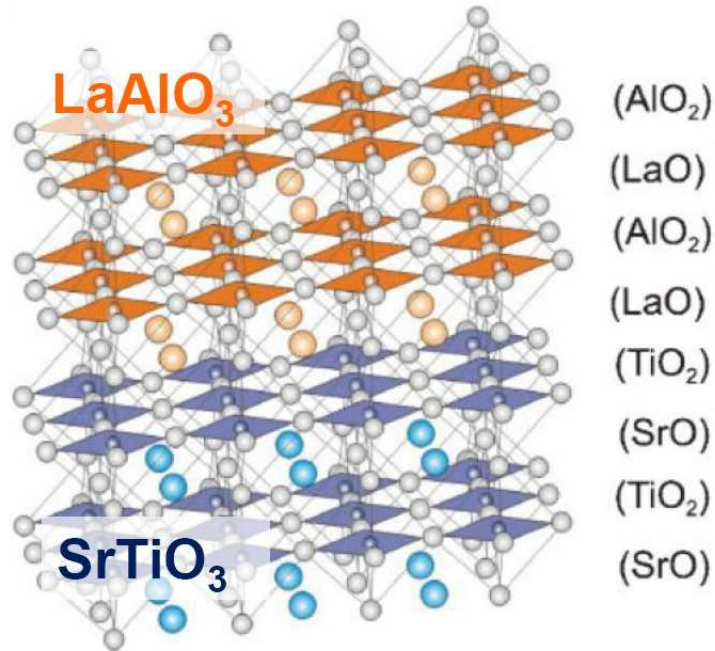


Fig. 5.1. Schematic view of crystalline LaAlO₃ oxide on Ti-terminated SrTiO₃ substrate. The 2 dimensional electron gas forms at the interface of the two oxide layers [55,56].

tric stacks of La-first cycle or Al-first cycle LaAlO₃, and LaAlO₃ with nanometer thin La₂O₃ or Al₂O₃ interfacial layer [61]. The impact of different interfaces (with AlO/LaO as the initial deposition cycle and with ultrathin Al₂O₃/La₂O₃ interfacial layer) are systematically studied. High resolution transmission electron microscopy (HRTEM) and temperature dependent MOSFET characterization are used to systematically study the LaAlO₃/SrTiO₃ interface.

5.2 Atomic Impact on LaAlO₃/SrTiO₃ NMOSFETs Interface: Initial Reaction Study

In order to better investigate the LaAlO₃/SrTiO₃ interface, two different initial reactions were employed in this experiment, including AlO as the first reaction cycle

and LaO as the first reaction cycle. SrTiO₃ NMOSFETs are fabricated and characterized.

5.2.1 SrTiO₃ Device Structure and Fabrication Process flow

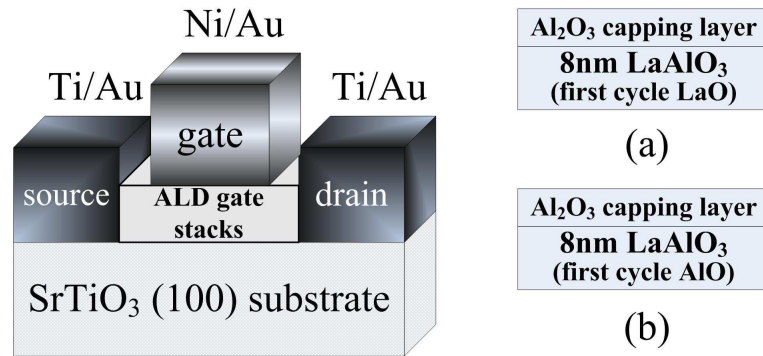
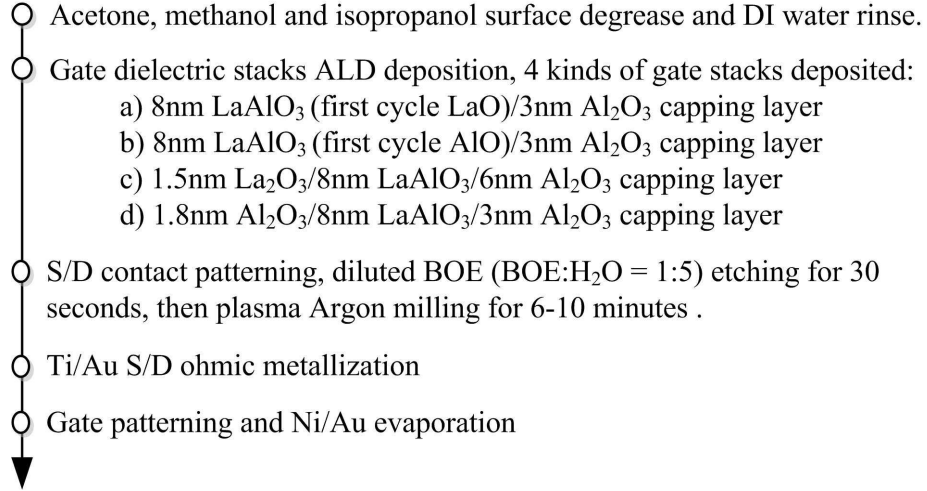


Fig. 5.2. Schematic view of an accumulation-mode NMOSFET on Ti-terminated SrTiO₃ substrate with 2 types of ALD LaAlO₃ gate stacks.

Fig. 5.2 and Table 5.1 show the schematic cross section of an accumulation-mode LaAlO₃/SrTiO₃ MOSFET and the device fabrication flow. Simple surface degrease using acetone, methanol and isopropanol was performed on 2-inch SrTiO₃ substrate. After DI water rinse, wafers were transferred via room ambient into ALD reaction chamber for gate stack deposition. For a systematical interface study, 2 kinds of high-k gate dielectric stacks were grown on insulating Ti-terminated SrTiO₃ substrates, which are La-first cycle 8 nm LaAlO₃ and Al-first cycle 8 nm LaAlO₃. Reactions of $\text{La}[\text{N}(\text{SiMe}_3)_2]_3 + \text{H}_2\text{O}$ and $\text{TMA} + \text{H}_2\text{O}$ at 300°C were employed for the dielectric deposition. La-first cycle/Al-first cycle refers to using $\text{La}[\text{N}(\text{SiMe}_3)_2]_3/\text{TMA}$ as the first pulse into the reaction chamber during the ALD process. After the gate dielectric layer, a layer of Al₂O₃ was immediately deposited as an encapsulation layer on top to prevent water adsorption of LaAlO₃ film. [62] After S/D pattern by photolithography,

Table 5.1

Process flow for SrTiO₃ NMOSFETs with ALD high-k dielectric. 2 types of LaAlO₃ gate stacks were employed. Plasma argon milling removes LaAlO₃ at S/D regions and also generates O vacancies on SrTiO₃ surface to ensure Ti/Au Ohmic contacts to the conducting channel.



diluted BOE solution (BOE : H₂O = 5 : 1) was used to first remove the Al₂O₃ capping layer and followed by an Argon milling in Plasma Technology RIE 80 for 6-10 minutes. During the milling process, over etch was a necessity to create shallow trench on SrTiO₃ surface where oxygen vacancies were generated and acted as donors to help to achieve good ohmic contacts on SrTiO₃ surface at the source and drain regions. Ti/Au was deposited as S/D metal by e-beam evaporation and a lift-off process was followed. Finally, the gate electrode was made by e-beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 3.5 μ m to 42.75 μ m and gate width of 100 μ m.

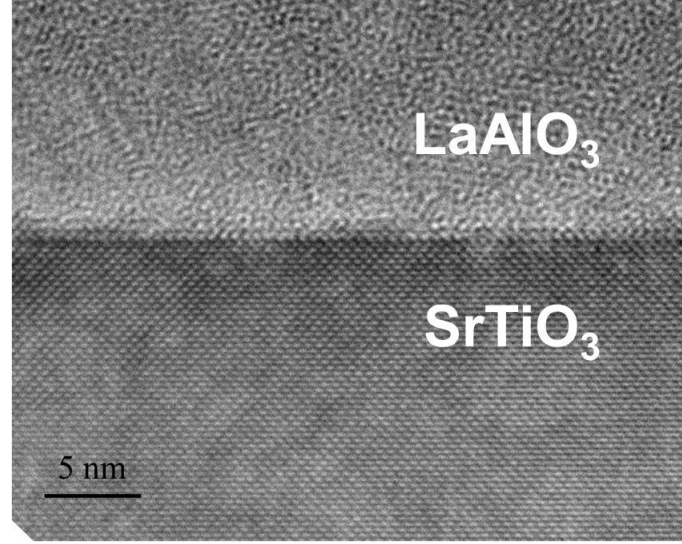


Fig. 5.3. Cross-section High Resolution Transmission Electron Microscopy (HRTEM) image of ALD $\text{LaAlO}_3/\text{SrTiO}_3$ interface. A sharp and clean interface is obtained between the top Atomic Layer Deposited (ALD) amorphous LaAlO_3 layer and the bottom single crystalline $\text{SrTiO}_3(100)$ substrate.

5.2.2 Device Characterization

The HRTEM image in Fig. 5.3 shows an amorphous layer of LaAlO_3 and a very abrupt $\text{LaAlO}_3/\text{SrTiO}_3$ interface. A Keithley 4200 was used for MOSFETs output characteristics at room temperature.

Well-behaved I-V characteristics of a $6.75\mu\text{m}$ -gate-length accumulation-mode SrTiO_3 NMOSFET with ALD high-k dielectric of La-first and Al-first LaAlO_3 is demonstrated in Fig. 5.4 and Fig. 5.5, with maximum drain current of 8.5 mA/mm and gate leakage less than 10^{-6} A/cm^2 . Fig. 5.6 and Fig. 5.7 illustrate the transfer characteristics of these $\text{LaAlO}_3/\text{SrTiO}_3$ NMOSFETs discussed above, both showing the on-off ratio (I_{on}/I_{off}) of ~ 1000 which is much smaller than that reported in [57]. This low I_{on}/I_{off} ratio is not due to the intrinsic property of this novel material system. It is because of the lack of device isolation in the current device fabrication process.

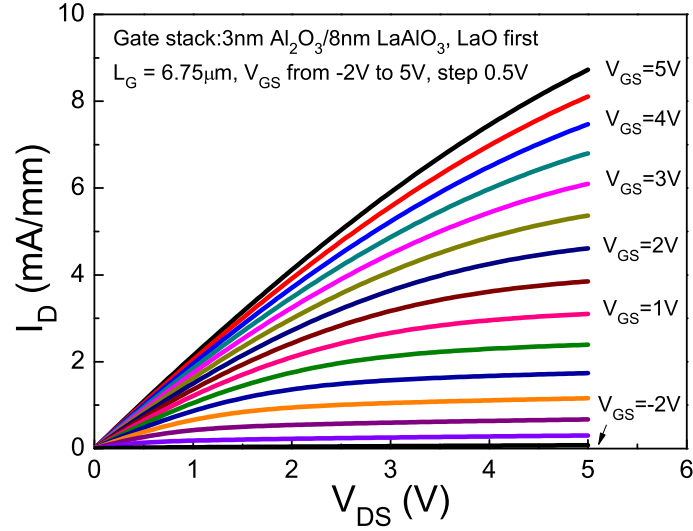


Fig. 5.4. The output characteristics of a SrTiO₃ MOSFET with La-first cycle LaAlO₃ as gate dielectric. The gate length of the device is 6.75 μm .

The NMOSFETs with AlO as first deposition reaction have slightly less drive current (6mA/mm versus 8mA/mm at $V_{GS} = 5\text{V}$ and $V_{DS} = 2\text{V}$) and higher I_{on}/I_{off} ratio, possibly due to the La atoms diffusion at the interface.

In order to study the importance of atomic structures at the interfaces, total resistance in mobility region vs. different gate length at different gate bias on La-first and Al-first devices are plotted in Fig. 5.8 and Fig. 5.9, respectively. It can be seen that sheet resistance for La-first interface at zero bias is 140 k Ω /sq. while 280 k Ω /sq. for Al-first interface. This observation might be correlated with the discovery reported in [55, 56, 63, 64], where the 2DEG formation is closely related with La involved interface structures.

The extrinsic peak transconductance G_m at $V_{DS}=5\text{V}$ is 2.1 mS/mm and an intrinsic value of 2.8 mS/mm can be obtained after subtracting the contact resistance R_{SD} . The less resistive channel at La-first LaAlO₃/SrTiO₃ interface than Al-first

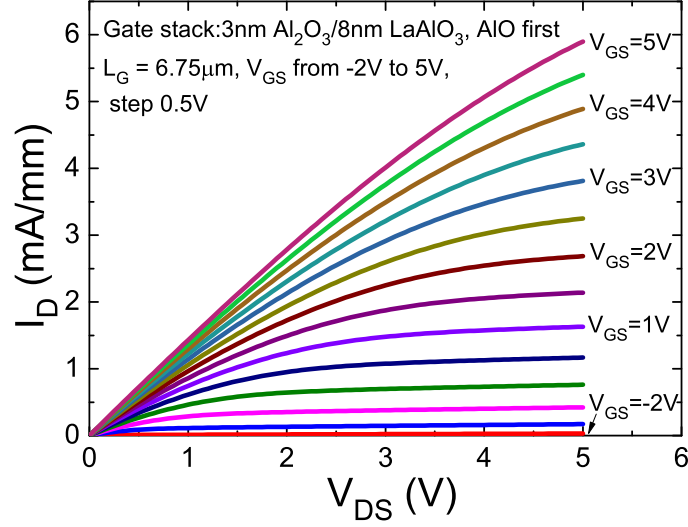


Fig. 5.5. The output characteristics of a SrTiO_3 MOSFET with Al-first cycle LaAlO_3 as gate dielectric. The gate length of the device is $6.75\mu\text{m}$.

$\text{LaAlO}_3/\text{SrTiO}_3$ interface is also supported by Fig. 5.10, where the field-effect mobility of La-first interface (with peak mobility of $\sim 3.9\text{ cm}^2/\text{Vs}$) is higher than that of Al-first interface (with peak mobility of $\sim 3.3\text{ cm}^2/\text{Vs}$).

5.3 Interfacial Layer Effect Study on SrTiO_3 NMOSFETs

5.3.1 Device structure and fabrication

Fig. 5.11 show the schematic cross section of an accumulation-mode $\text{LaAlO}_3/\text{SrTiO}_3$ MOSFET. The process flow is similar to that of Simple surface degrease using acetone, methanol and isopropanol was performed on 2-inch SrTiO_3 substrate. After DI water rinse, wafers were transferred via room ambient into ALD reaction chamber for gate stack deposition. Two gate stacks, 8 nm LaAlO_3 with 1.5 nm La_2O_3 interfacial layer, and LaAlO_3 with 1.8 nm Al_2O_3 interfacial layer were deposited on the

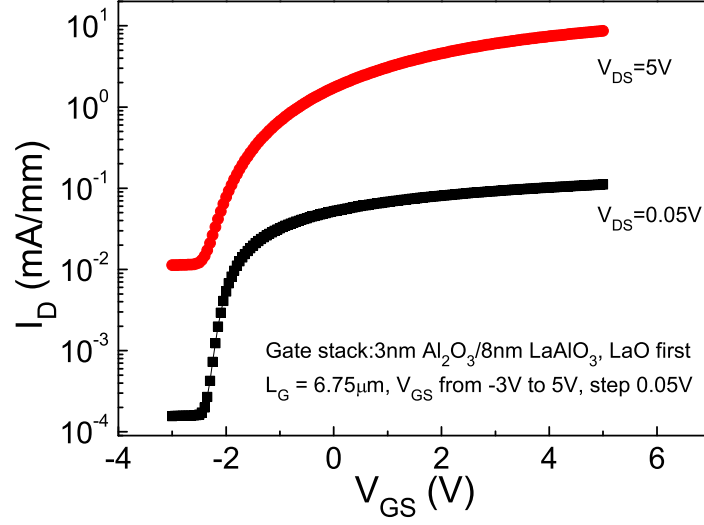


Fig. 5.6. The transfer characteristics of a SrTiO₃ MOSFET with La-first cycle LaAlO₃ as gate dielectric. The gate length of the device is 6.75 μm .

SrTiO₃ substrates. After the gate dielectric stacks, a layer of Al₂O₃ was immediately deposited as an encapsulation layer on top. After S/D pattern by photolithography, diluted BOE solution (BOE : H₂O \sim 5:1) was used to first remove the Al₂O₃ capping layer and followed by an Argon milling in Plasma Technology RIE 80 for 10 minutes. Ti/Au was deposited as S/D metal by e-beam evaporation and a lift-off process was followed. Finally, the gate electrode was made by e-beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 3.5 μm to 42.75 μm and gate width of 100 μm . A Keithley 4200 was used for MOSFETs output characteristics at room temperature, and a Janis 22C/350C Cryodyne Refrigerator system along with a Keithley 2612A SYSTEM source meter were used for low temperature measurement.

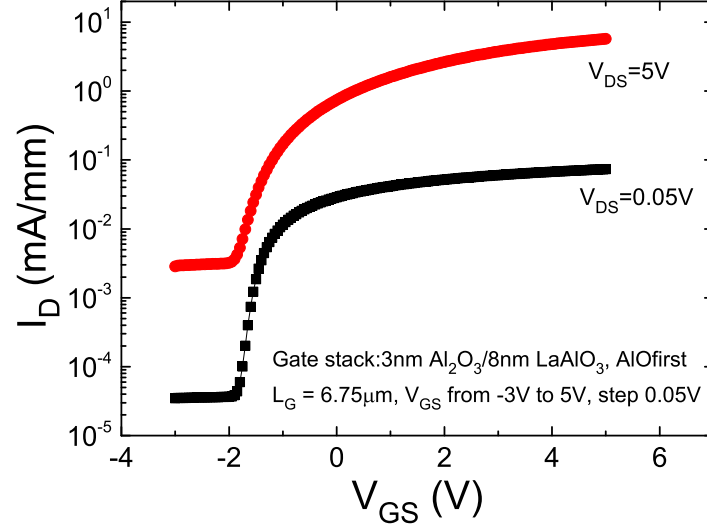


Fig. 5.7. The transfer characteristics of a SrTiO₃ MOSFET with Al-first cycle LaAlO₃ as gate dielectric. The gate length of the device is 6.75 μm .

5.3.2 Device Characterization: A Temperature Dependence Study

In order to further verify the importance of atomic structures at the interfaces, we deliberately designed two gate stack structures with 1.5 nm La₂O₃ and 1.8 nm Al₂O₃ as the interfacial layer between 8nm LaAlO₃ and SrTiO₃ substrates. Similarly, well behaved I-V characteristics are also obtained on these devices. As shown in Fig. 5.12, a 3.75 μm -gate-length device with 1.5 nm La₂O₃ interfacial layer has a drain current of 10 mA/mm.

Fig. 5.13 and Fig. 5.14 show the similar approach to probe the sheet resistance of different interfacial layers with 320 k Ω /sq. for La₂O₃ while 800 k Ω /sq. for Al₂O₃. The result reconfirms the importance of the atomic structure of La-Ti on SrTiO₃ surface to achieve higher conducting channel.

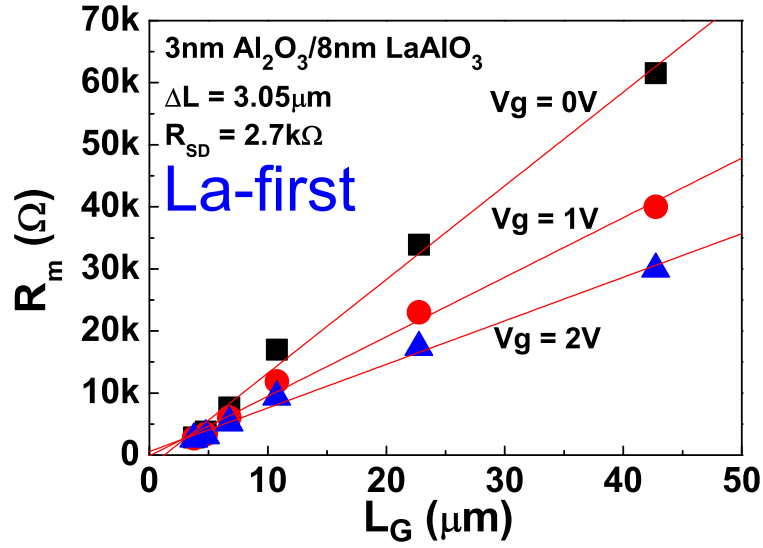


Fig. 5.8. Channel resistance (R_m) versus designed gate length (L_G) under different gate bias in the linear region on La-first SrTiO₃ MOSFETs. The S/D series resistance (R_{SD}) and effective gate length can be obtained at the cross point. La-first interface shows a sheet resistance of $\sim 140 \text{ k}\Omega/\text{sq.}$ at zero bias.

Fig. 5.15 shows the maximum drain current vs. different gate length on the two types of MOSFETs with a reasonable scaling behavior. More pronounced difference in terms of field-effect mobility can be observed in Fig. 5.16. As mentioned above, La-Ti atomic structure plays a key role to form a better conducting channel at LaAlO₃/SrTiO₃ interface, thus explaining the more obvious difference in terms of mobility than the case between La-first and Al-first as shown in Fig. 5.10. With different gate lengths, field effect mobility $\mu_{FE} \sim 4 \text{ cm}^2/\text{Vs}$ can be obtained on the devices with 1.5 nm La₂O₃ interfacial layer, while $\sim 2.5 \text{ cm}^2/\text{Vs}$ with 1.8 nm Al₂O₃ interfacial layer. All the data are peak values of field-effect mobility extracted from different gate-length device transfer characteristics in linear region.

Fig. 5.17 shows the maximum drain current (I_{DSS}) and on-off ration (I_{on}/I_{off}) vs. measured temperature from 300K down to 10K. The increase of maximum drain

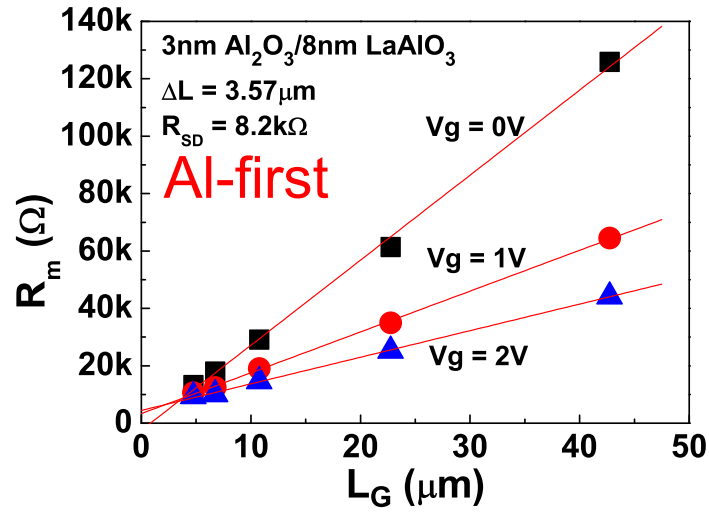


Fig. 5.9. Channel resistance (R_m) versus designed gate length (L_G) under different gate bias in the linear region on Al-first SrTiO₃ MOS-FETs. The S/D series resistance (R_{SD}) and effective gate length can be obtained at the cross point. La-first interface shows a sheet resistance of $\sim 280 \text{ k}\Omega/\text{sq.}$ at zero bias.

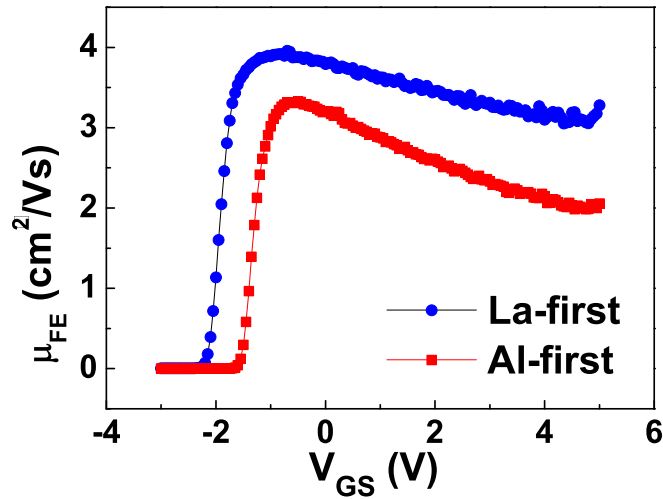


Fig. 5.10. Comparison of field-effect mobility of La-first and Al-first LaAlO₃/SrTiO₃ MOS-FETs, showing La-first interface has higher mobility than Al-first interface.

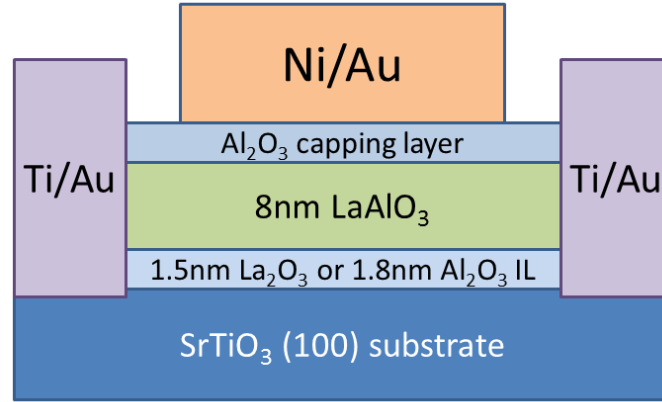


Fig. 5.11. Schematic view of an accumulation-mode NMOSFET on Ti-terminated SrTiO₃ substrate with two different interfacial layers (1.5nm La₂O₃ or 1.8nm Al₂O₃).

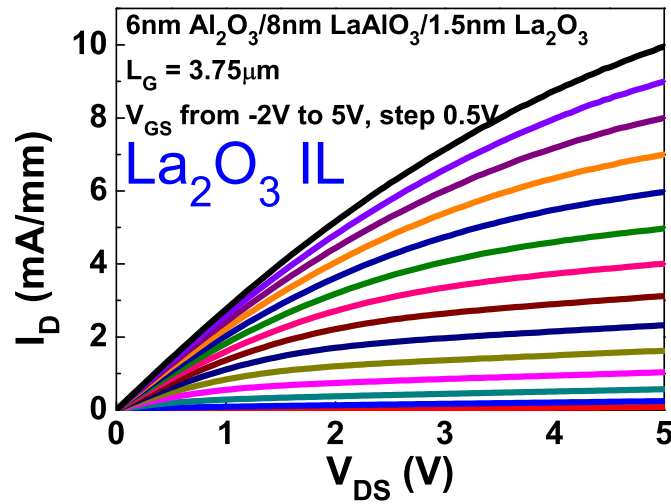


Fig. 5.12. The output characteristics of a SrTiO₃ MOSFET with 1.5 nm La₂O₃ as interfacial layer. The gate length of the device is 3.75 μm .

current is expected, because electron-phonon scattering should be suppressed with decrease of temperature thus increase the mobility. [65] The dramatic increase of I_{on}/I_{off} ratio from 10^3 to 10^7 provides an insight into the possible origin of the elec-

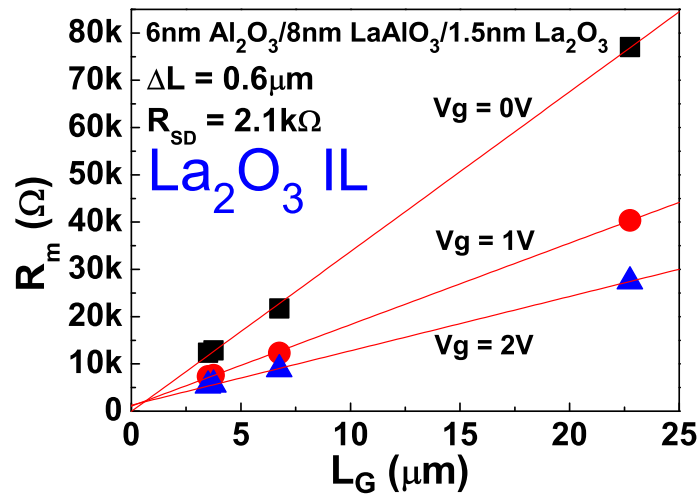


Fig. 5.13. R_m versus L_G under different gate bias in the linear region on SrTi₃ MOSFETs with La₂O₃ as interfacial layer. La₂O₃ interface shows a sheet resistance of $\sim 320\text{ k}\Omega/\text{sq.}$ at zero bias.

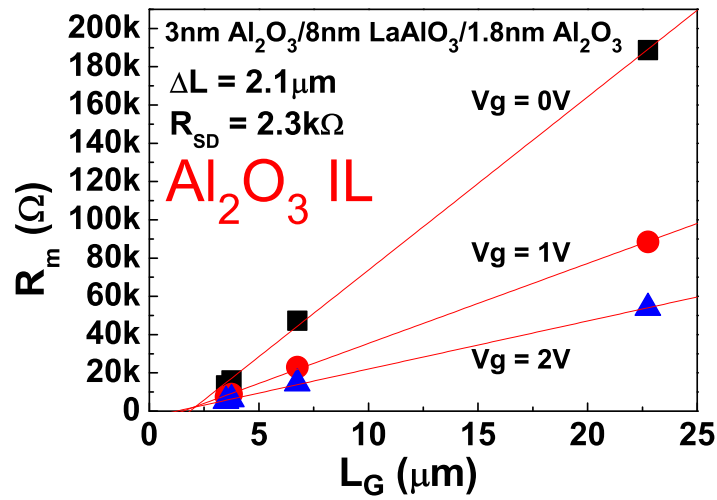


Fig. 5.14. R_m versus L_G under different gate bias in the linear region on SrTiO₃ MOSFETs with Al₂O₃ as interfacial layer. Al₂O₃ interface shows a sheet resistance of $\sim 800\text{ k}\Omega/\text{sq.}$ at zero bias.

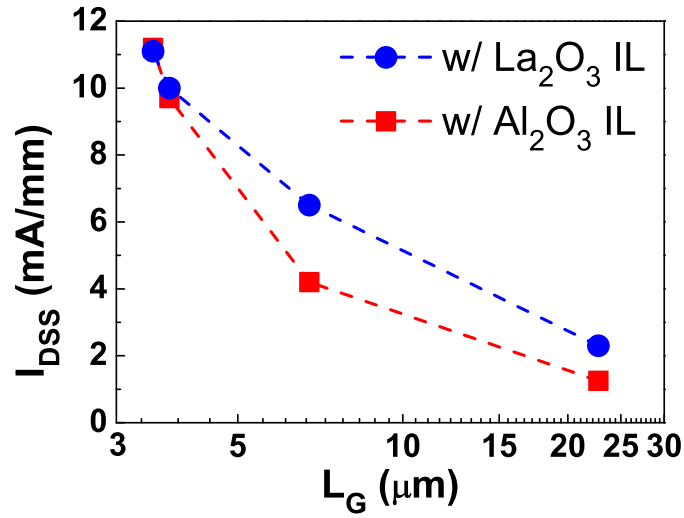


Fig. 5.15. Summary of the maximum drain current (I_{DSS}) at $V_{GS}=5\text{V}$ vs L_G on SrTiO_3 MOSFETs with La_2O_3 and Al_2O_3 as interfacial layers. La_2O_3 devices have larger I_{DSS} at the same gate length.

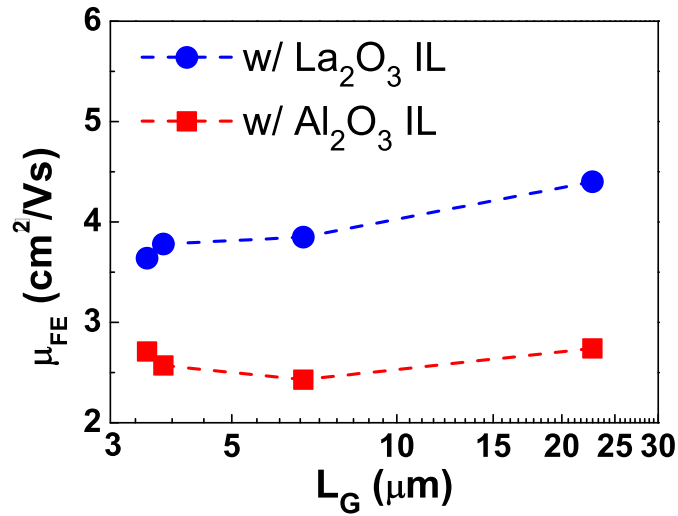


Fig. 5.16. Summary of field-effect mobility (μ_{FE}) at $V_{GS}=5\text{V}$ vs L_G on SrTiO_3 MOSFETs with La_2O_3 and Al_2O_3 as interfacial layers. La_2O_3 devices have larger μ_{FE} at the same gate length.

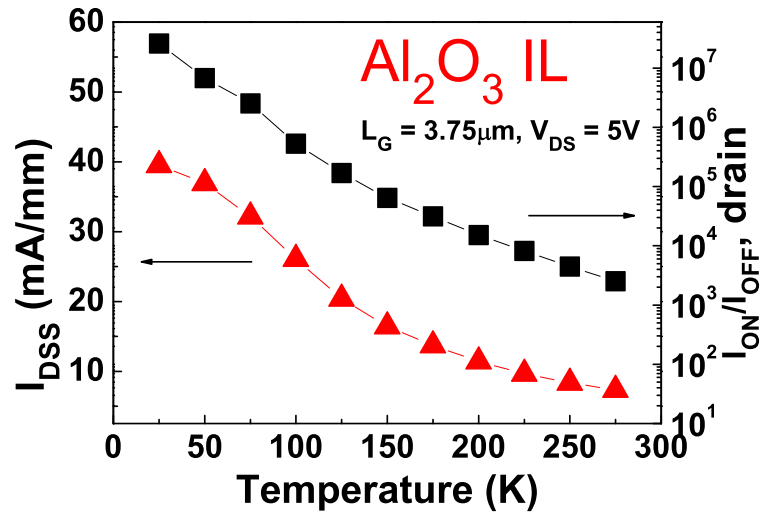


Fig. 5.17. I_{DSS} and I_{on}/I_{off} (drain current) vs. temperature for a SrTiO_3 MOSFET with a gate length of $3.75 \mu\text{m}$ and Al_2O_3 as an interfacial layer.

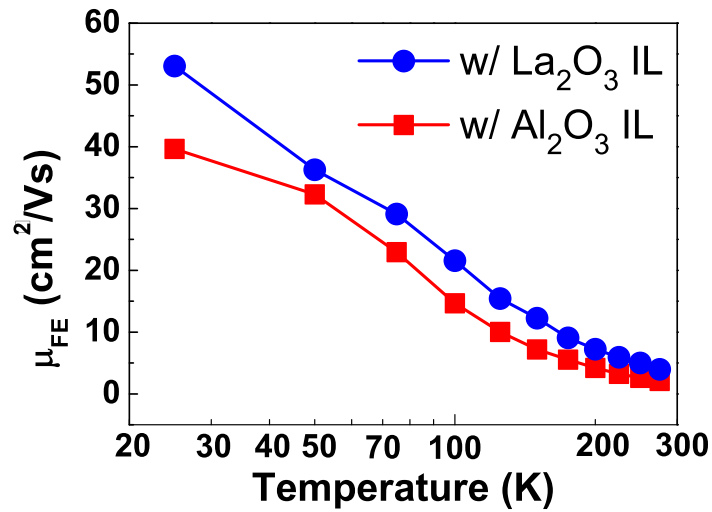


Fig. 5.18. Temperature dependent μ_{FE} at $V_{GS}=5\text{V}$ on SrTiO_3 MOSFETs with La_2O_3 and Al_2O_3 as interfacial layers and at $L_G = 3.75 \mu\text{m}$. La_2O_3 devices have larger μ_{FE} at the same gate length.

tron carriers at the $\text{LaAlO}_3/\text{SrTiO}_3$ interface. I_{off} is dominated by the fringe current between source/drain beyond gate controlled area due to the lack of device isolation. The 4 orders of magnitude decrement indicates that the intrinsic carriers are frozen out at low temperatures. The majority carriers in the channel are originated from electrostatic doping or field-effect. The intrinsic carriers at zero bias could be caused by a combination of the crystal-field effect, pseudo-Jahn-Teller distortion, and interface chemistry. Another possibility is from charge transfer from wider bandgap oxide into the adjacent narrower gap SrTiO_3 layer. [66] This charge transfer, similar to modulation-doping in III-V semiconductors, could be significantly suppressed at low temperature. The field-effect mobility vs. temperature for devices with La_2O_3 and Al_2O_3 interfacial layers are plotted in Fig. 5.18.

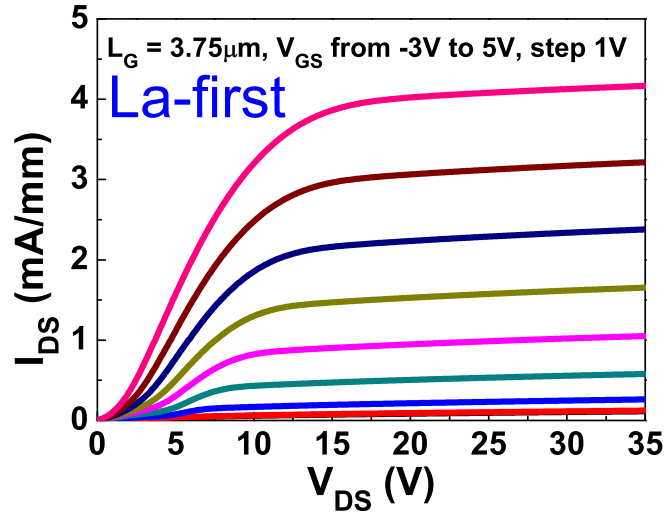


Fig. 5.19. High-voltage I-V output characteristics of a representative device among these SrTiO_3 MOSFETs. The device can be operated in tens of voltages as drain voltage due to the wide bandgap of SrTiO_3 .

High voltage output performance is characterized (seen in Fig. 5.19) to demonstrate the potential of this novel material system for all-oxide FETs with applications in transparent power amplifier/switch area due to its wide bandgap (3.2eV for



Fig. 5.20. SrTiO_3 single crystalline film was grown on 300 mm Si substrate by MBE as shown in the picture. The length of the ruler in the picture is 12 inch. The shining SrTiO_3 surface reflects the part of MBE system in which the film was grown.

SrTiO_3). A picture of epitaxial single crystalline SrTiO_3 film on 300mm Si wafer is also shown in Fig. 5.20, which demonstrates great potential to integrate the all-oxide FET technology into Si process platform with the availability of ALD technology on 300mm Si process.

5.4 Metal-Insulator-Transition at LaAlO_3 - SrTiO_3 interface

5.4.1 Introduction

It is widely believed that conducting oxide/oxide interface needs to be atomically engineered oxide heteroepitaxy in order to achieve conducting channels. Most of this phenomenology results from strongly correlated electronic behavior and turned out to be very sensitive to external electric and magnetic fields. Polarity discontinuities

at the interfaces between two different crystalline materials or called hetero-interfaces are believed to be the key to lead to non-trivial effects.

After the first demonstration that the conducting channel could be formed at amorphous LaAlO_3 /crystalline SrTiO_3 interface by simply atomic-layer-deposition (ALD) of LaAlO_3 as shown in previous sections, we report the observation of metal-insulator transition (MIT) of the conducting ALD LaAlO_3 / SrTiO_3 interfaces with the data focused on the gate stack with ultrathin (1.8nm) Al_2O_3 interfacial layer.

5.4.2 Metal-Insulator-Transition Observation at LaAlO_3 / SrTiO_3 Interface

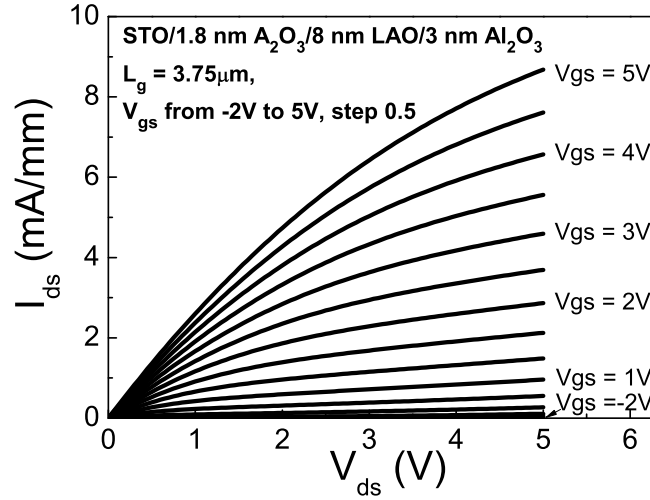


Fig. 5.21. Well-behaved I_{DS} - V_{DS} characteristics of a $3.75\mu\text{m}$ gate length $\text{LaAlO}_3/\text{SrTiO}_3$ FET with dielectric gate stacks including 1.8nm Al_2O_3 interfacial layer.

From the output characteristic (Fig. 5.21) of a FET formed on 8nm LaAlO_3 /1.8nm Al_2O_3 / SrTiO_3 interface with gate length of $3.75\mu\text{m}$. At $V_{DS}=5\text{V}$ and $V_{GS}=5\text{V}$, the drain current is $\sim 9\text{ mA/mm}$. The estimated room-temperature field-mobility is 4-5

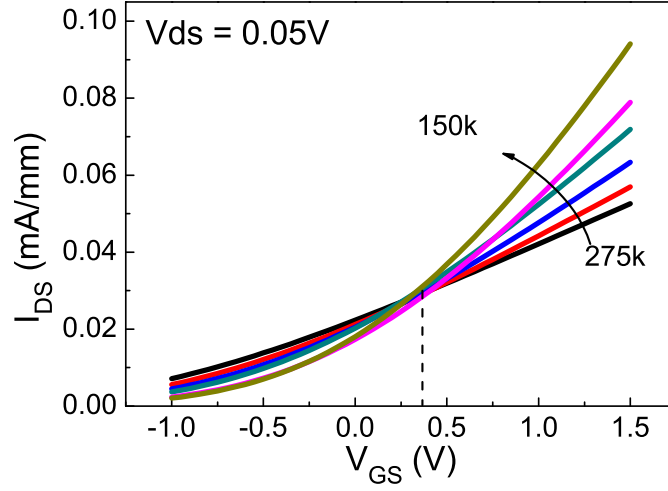


Fig. 5.22. Temperature dependent I_{DS} - V_{GS} measurement at $V_{DS}=5V$ of the same device in Fig. 5.21. A clear crossover is observed at $V_{GS}\sim 0.2V$ at $V_{DS}=5V$ and $V_{GS}\sim 0.5V$ at $V_{DS}=0.05V$.

cm^2/Vs similar to the value reported in [55] where the oxide interface is epitaxially grown. Another interesting point is that ALD LaAlO_3 stack not only provides the hetero-oxide-interface to induce the conducting channel, it also serves as high-k gate dielectric for top metal gate to electro-statically control the channel. The channel current is plotted in Figure 5.22 as a function of the gate bias for temperatures between 275K and 150K, in 25K step. All curves roughly cross at a single point, at a gate bias of about 0.2V for $V_{DS}=5V$ and 0.5V for $V_{DS}=0.05V$. This gate bias value corresponds to a crossover from an insulating state ($d\sigma/dT < 0$) to a metallic state ($d\sigma/dT > 0$).

Figure 5.23 shows the temperature dependence of the sheet resistance of the device for various gate bias values. Insulating behavior is seen below the critical gate voltage of 0.5V, switching to metallic conductance at higher bias. The sheet resistance at the critical voltage is almost temperature independent. This shows that an apparent MIT is induced by the field-effect in SrTiO_3 . The characteristic resistance is $2\text{M}\Omega/\text{sq.}$ as

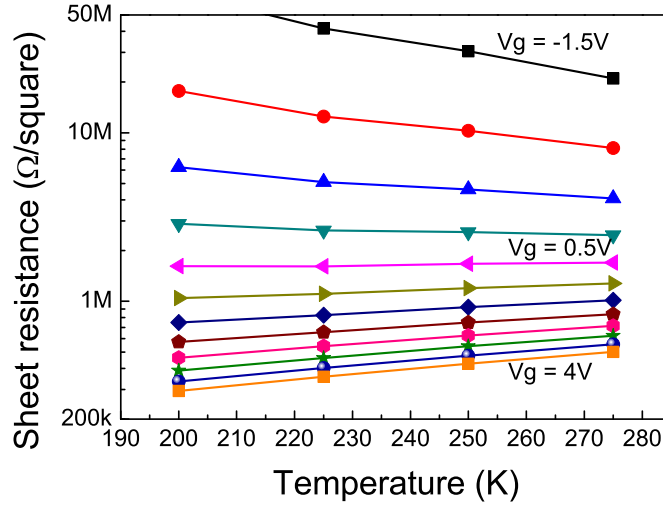


Fig. 5.23. Temperature dependence of the channel resistance as a function of gate bias. Insulating ($V_{GS} < 0.5V$) and metallic state ($V_{GS} > 0.5V$) behavior are seen. The sheet resistance is nearly temperature independent at the critical bias.

reported in Ref. [67] much higher than the quantum resistance ($\sim h/e^2$) obtained on Si MOSFETs [68].

5.4.3 Mechanism Investigation of Metal-Insulator-Transition

A schematic energy band diagram is employed here to help with the understanding of Metal-Insulator-Transition phenomenon (Fig. 5.24). SrTiO_3 can be regarded as an n-type semiconductor with the Fermi level pinned slightly below the conduction band bottom. We assume an existence of in-gap states in SrTiO_3 , which provides an explanation for conductivity in an otherwise insulating phase. Such in-gap states were recently characterized by photoinduced absorption measurements in single-crystal SrTiO_3 [69]. We assume that the mobility edge of SrTiO_3 coincides with the conduction band bottom. When a gate voltage is applied, the induced carriers are trapped in

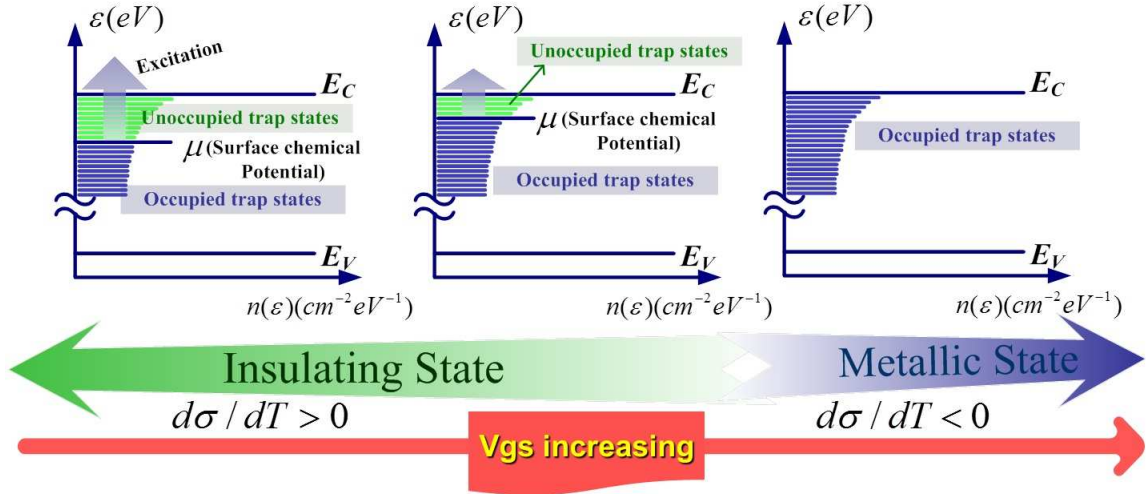


Fig. 5.24. In gap states filling model of the Metal-Insulator-Transition phenomenon. The system experiences the transition from insulating state with unoccupied states reside in the SrTiO_3 band gap to metallic state, where the in gap states are filled with field effect induced carriers.

vacant in-gap states and the chemical potential moves closer to the conduction band edge (Insulating state). In the SrTiO_3 MOSFET in this work, at a gate bias of $\sim 0.5\text{V}$, the chemical potential of SrTiO_3 crossed over the mobility edge into the conduction band (Metallic state). The critical gate voltage was independent of temperature and was only determined by the energy difference between the initial Fermi level and the mobility edge.

For the conduction in the insulating phase, with the help of Arrhenius plots (Fig. 5.25) of the drain currents, we are able to plot the carrier activation energy as a function of gate bias. The type of temperature dependence has been shown to be caused predominantly by a thermal excitation of carriers from shallow trap states in the channel. The activation energy E_a is suppressed as the gate bias is increased because the shallow states in the gap are gradually populated by field effect induced carriers.

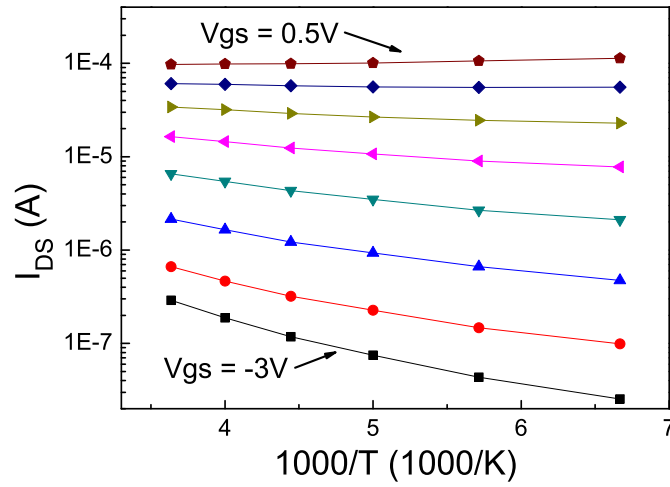


Fig. 5.25. Arrhenius plots of the drain current of the SrTiO_3 MOSFET for various V_{GS} .

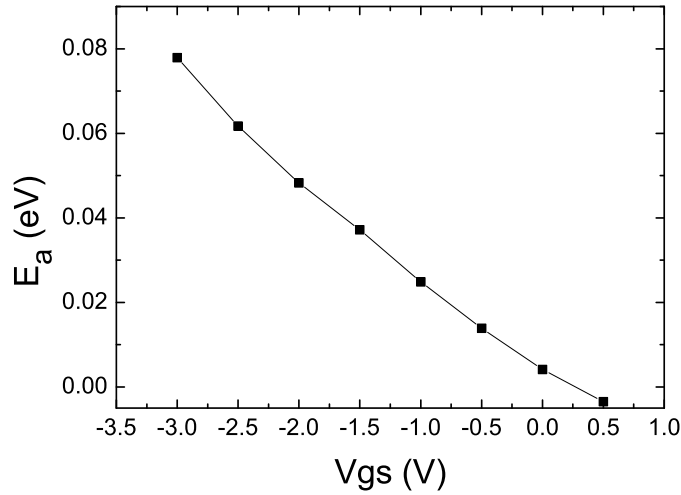


Fig. 5.26. Carrier activation energy vs gate bias in the insulating state. The activation energy was reduced by the gate field effect induced carriers in the channel area.

One parameter scaling analysis [68] for the sheet resistance in the temperature range from 275K to 150K is performed and plotted in Figure 5.26. Density or gate

bias dependent T_0 falls sharply for both insulating and metallic sides as the gate bias approaches to the critical gate voltage. As shown in Figure 5.27, all sheet resistance plots collapse into two curves: an insulating branch for carrier density below the critical value and a metallic branch for density above the critical value. Nevertheless, such conducting channel formed at an amorphous/crystalline oxide interface is a big surprise. Much more studies are needed to understand the physics and potential device applications for this novel all oxide electronic material.

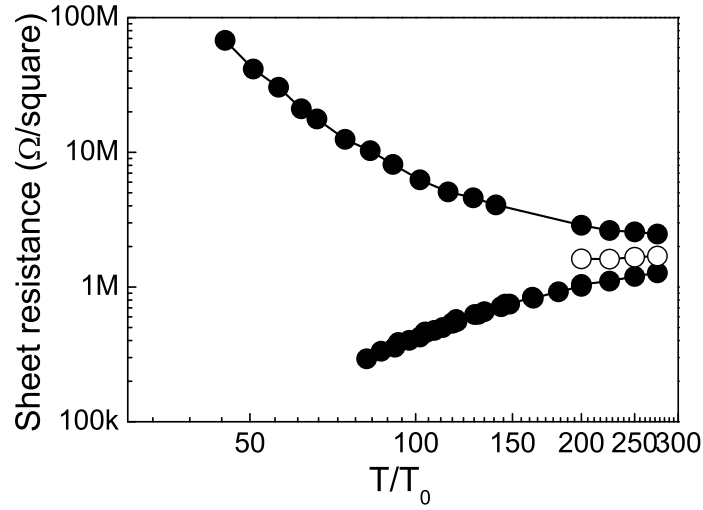


Fig. 5.27. Scaling behavior of the sheet resistance for the device, with T_0 chosen to yield scaling with temperature.

5.5 Summary and Conclusion

We have found a conducting channel at insulating ALD amorphous LaAlO_3 /insulating crystalline SrTiO_3 interface and demonstrated well-performed $\text{LaAlO}_3/\text{SrTiO}_3$ N-channel MOSFETs. The maximum drain current can exceed 10 mA/mm for a $3.75\mu\text{m}$ -gate-length device with La_2O_3 interfacial layer at $V_{GS} = 5\text{V}$. Four different gate dielectric stacks are designed to investigate the role of atomic structures

at the interfaces for the channel conductivity, showing La-Ti interface is preferable for a better conducting channel. Metal-Insulator-Transition was observed from the device temperature dependent transfer characteristics, an in-gap state theory was used to explain the MIT phenomenon at the amorphous LaAlO_3 /crystalline SrTiO_3 interface. With the availability of MBE SrTiO_3 and ALD LaAlO_3 on 300 mm Si substrates, these all-oxide field-effect transistors have the path for integration onto the state-of-the-art Si technology platform.

6. SUMMARY AND OUTLOOK

In summary, in this thesis for the first time, using atomic layer epitaxy (ALE) realized by ALD, with a single crystalline semiconductor-single crystalline oxide interface, high performance GaAs inversion-mode nMOSFETs, pMOSFETs, CMOS inverters, NAND and NOR logic gates and 5-stage ring oscillators are demonstrated. The maximum drain current of 376 mA/mm for a 1 μ m-gate-length device with a low subthreshold swing (SS) of 74mV/dec are achieved for the devices with La₂O₃/GaAs(111)A epitaxial interfaces. The single-crystalline La_{2-*x*}Y_{*x*}O₃/single-crystalline GaAs(111)A interface are systematically studied with High-resolution Transmission Electron Microscopy (HRTEM), X-ray Diffraction (XRD) and Capacitance-Voltage analysis. This high quality interface is very promising in future CMOS application. Ge pMOSFETs and nMOSFETs with La-based epitaxial gate dielectrics are also demonstrated, and the results show great potential of the epitaxial interface in future Ge digital logic applications. The complex oxide study also expanded to complex oxide material SrTiO₃, conducting channel is found at the interface of insulating ALD amorphous LaAlO₃/insulating crystalline SrTiO₃ interface, and well-behaved LaAlO₃/SrTiO₃ all oxide field-effect transistors (FETs) are demonstrated with different gate dielectric stacks. The interface was closely studied by manipulating the ALD initial reaction cycles and insertion of different interfacial layers, and results show that La-Ti interface is preferable for a better conducting channel.

In particular, the high quality epitaxial ALD complex oxide layer on GaAs(111)A substrate give rise to great opportunities of future high mobility MOSFETs applications. Along the line of the promising interface delivered by ALD, much more

interesting work could be done on the further exploration of next generation's device gate dielectrics. Firstly a detail study of the La-based higher- κ oxide is necessary for the interface chemistry study, which will lead to an in-depth understanding of the epitaxial formation and structure. Secondly the epitaxial oxide can be applied to more III-V semiconductor materials like InP and GaSb, who also have high carrier mobility and are of great interest in the future device fabrication. In addition, The integration of epitaxial interfaces in the devices with novel structures like FINFETs and GAA (Gate All Around) FETs, along with the ultra scaling oxide material and electrical properties, also need to be investigated.

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VITA

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