# Digitally-Assisted RF IC Design Techniques for Reliable Performance 

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For the degree of Doctor of Philosophy

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Head of the Graduate Program
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# DIGITALLY-ASSISTED RF IC DESIGN TECHNIQUES FOR RELIABLE PERFORMANCE 

A Dissertation<br>Submitted to the Faculty<br>of<br>Purdue University<br>by<br>Jang Joon Lee<br>In Partial Fulfillment of the Requirements for the Degree<br>of<br>Doctor of Philosophy

December 2013

Purdue University
West Lafayette, Indiana

For my dear parents, my beloved wife, Somyung, and my loving son, Jiho

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## SYMBOLS

| $\omega$ | Angular frequency |
| :--- | :--- |
| $I_{b}$ | Bias current |
| $V_{b}$ | Bias voltage |
| $C$ | Capacitor |
| $I_{D}$ | Drain current |
| $V_{D S}$ | Drain-to-source voltage |
| $C_{g d}$ | Gate-to-drain capacitance |
| $C_{g s}$ | Gate-to-source capacitance |
| $V_{G S}$ | Gate-to-source voltage |
| $L$ | Inductor |
| $Z_{i n}$ | Input impedance |
| $r_{o}$ | Output resistance |
| $\phi$ | Phase |
| $I_{r e f}$ | Reference current |
| $R$ | Resistor |
| $V_{t h}$ | Threshold voltage |
| $g_{m}$ | Transconductance |
| $f_{t}$ | Transit frequency |
| $A_{v}$ | Voltage gain |

## ABBREVIATIONS

| ADC | Analog-to-Digital Converter |
| :---: | :---: |
| BB | Baseband |
| CMOS | Complementary Metal Oxide Semiconductor |
| DLL | Delay-Locked Loop |
| DAC | Digital-to-Analog Converter |
| DSP | Digital Signal Processing |
| ED | Envelope Detector |
| EVM | Error Vector Magnitude |
| FF | Fast-Fast |
| FFT | Fast Fourier Transform |
| FPGA | Field-Programmable Gate Array |
| FS | Fast-Slow |
| HG | High-Gain |
| HL | High-Linearity |
| HL(HA) | High-Linearity(High-Attenuation) |
| HL(LA) | High-Linearity(Low-Attenuation) |
| IC | Integrated Circuit |
| IF | Intermediate Frequency |
| IIP3 | Input-referred 3rd-order Intercept Point |
| I/Q | In-phase/Quadrature-phase |
| LNA | Low-Noise Amplifier |
| LO | Local Oscillator |
| LPF | Low-Pass Filter |
| LSB | Least Significant Bit |


| MIMO | Multiple-Input Multiple-Output |
| :---: | :---: |
| MSB | Most Significant Bit |
| NF | Noise Figure |
| OP-AMP | Operational Amplifier |
| PSK | Phase-Shift Keying |
| PA | Power Amplifier |
| PVT | Process Voltage Temperature |
| P1dB | 1dB-compression Point |
| QAF | Quadrature All-pass Filter |
| QAM | Quadrature Amplitude Modulation |
| RF | Radio Frequency |
| RMS | Root Mean Square |
| RX | Receive |
| SF | Slow-Fast |
| SNR | Signal-to-Noise Ratio |
| SOC | System on Chip |
| SOI | Silicon on Insulator |
| SS | Slow-Slow |
| SPI | Serial Peripheral Interface |
| VDD | Supply Voltage |
| TDC | Pulsewidth (Time)-to-Digital Converter |
| TSPC | True Single-Phase Clocked |
| TT | Typical-Typical |
| TX | Transmit |
| VCO | Voltage-Controlled Oscillator |
| VGA | Variable-Gain Amplifier |
| XOR | Exclusive OR |


#### Abstract

Lee, Jang Joon Ph.D., Purdue University, December 2013. Digitally-Assisted RF IC Design Techniques for Reliable Performance. Major Professor: Byunghoo Jung.


Semiconductor industries have competitively scaled down CMOS devices to attain benefits of low cost, high performance, and high integration density in digital integrated circuits. On the other hand, deep scaled technologies inextricably accompany a large process variation, supply voltage scaling, and reduction in breakdown voltages of transistors. When it comes to RF/analog IC design, CMOS scaling adversely affects its reliability due to large performance variation and limited linearity. For addressing the issues related to variations and linearity, this research proposes the following digitally-assisted RF circuit design techniques: self-calibration system for RF phase shifters and wide dynamic range LNAs.

Due to PVT variations in scaled technologies, RF phase shifter design becomes more challenging with device scaling. In the proposed self-calibration topology, we devised a novel phase sensing method and a pulsewidth-to-digital converter. The feedback controller is also designed in digital domain, which is robust to PVT variations. These unique techniques enable a sensing/control loop tolerant to PVT variations. The self-calibration loop was applied to a 7 to 13 GHz phase shifter. With the calibration, the estimated phase error is less than 2 degrees.

To overcome the linearity issue in scaled technologies, a digitally-controlled dualmode LNA design is presented. A narrowband ( 5.1 GHz ) and a wideband ( 0.8 to 6 GHz ) LNA can be toggled between high-gain and high-linearity modes by digital control bits according to the input signal power. A compact design, which provides negligible performance degradation by additional circuitry, is achieved by sharing most of the components between the two operation modes. The narrowband and the
wideband LNA achieves an input-referred P 1 dB of -1.8 dBm and +4.2 dBm , respectively.

## 1. INTRODUCTION

### 1.1 Motivation

### 1.1.1 The advent of digitally-assisted RF circuits

Semiconductor industries have competitively scaled down CMOS devices to attain benefits of low cost, high performance, and high integration density in digital integrated circuits. Fig. 1.1 shows how rapidly the advancement of CMOS scaling has been progressed in the past two decades [1-3]. Commercial wireless SoCs in the 28 nm technology node are prevailing in market, and it is also reported that 14 nm chipsets have been demonstrated. With CMOS scaling, RF and analog circuits have also exploited the advantage of high speed and low noise properties provided by device scaling. Unfortunately, deep scaled technologies accompany negative effects on RF and analog circuit design, which turn down the merits of technology advancement.


Fig. 1.1. Trend of CMOS technology scaling.

More prominent random-dopant fluctuations, line edge/width roughness, and gate dielectric variations result in large process variations [4,5]. Supply voltage scaling and reduction in breakdown voltages of transistors limit linearity performance [6, 7]. In addition, RF and analog circuit design suffers from low output impedance, mismatch, gate leakage, and low voltage headroom $[8,9]$. Such problems are more influential in nanoscale CMOS technologies below the 90 nm node.

Despite the issues of RF and analog circuit design in deep scaled technologies, RF and analog circuits have to be integrated with digital baseband and processors in the same process to maximize the benefits afforded by device scaling. In order to overcome the issues, digital circuits are employed to maintain or improve the performance of RF and analog circuits, so called digitally-assisted RF/analog circuit design. Digital circuits are initially adopted for analog circuits [10-13] and gradually expanded for RF circuits [14-17]. Digital circuits are mainly utilized for calibration to guarantee reliable performance or for mode control to enhance dynamic range of RF and analog circuits. For addressing the issues related to variations and linearity, this research proposes the following digitally-assisted RF circuit design techniques: self-calibration system for RF phase shifters and wide dynamic range LNAs.

### 1.1.2 Self-calibration system for RF phase shifters

Phase shifter is an essential building block in a phased-array system because phase shifters enable directional beam-forming and electronic beam-steering in a phased array. In a phased-array system, phase shifting can be performed in RF, LO, or IF ( BB ) domain. Among them, RF domain phase shifting has the following advantages [18-21]. Since transmitted RF signal in a phased-array has a high pattern directivity, it can reject interferers and hence, it can provide superior linearity. As a result, phase shifting in RF domain would relax linearity requirements of the receiver. In addition, while phase shifting in LO or IF (BB) requires multiple frequency conversion components (i.e. mixers and LO distribution) or multiple IF (BB) stages, respectively,
phase shifting in RF can share those stages. Therefore, it could eventually achieve lower power and lesser complexity. However, RF phase shifter design becomes more challenging along with scaled technologies. As devices are scaled down, phase shifters are more sensitive to PVT variations. Consequently, small performance deviation at high frequencies would introduce significant phase error. Such PVT variations are drawbacks of phase shifting in RF domain. Phase and amplitude errors in a phase shifter cause sidelobe growth and directivity reduction as illustrated in Fig. 1.2 and hence, $\mathrm{Tx} / \mathrm{Rx}$ signal power and SNR would be reduced. As a result, multiple Rx paths require higher gain, lower noise, lower distortion, and PAs in Tx demand higher output power and higher linearity. Amplitude error would be easily compensated by a VGA, but phase calibration is much difficult at high frequencies. For $\sim 10 \mathrm{GHz}$ phase shifters, a phase needs to be sensed in sub-pico-second level.


Fig. 1.2. Sidelobe growth and directivity reduction in a phased array.

There have been calibration schemes for a phased-array system [22-27]. A conventional post-calibration method are presented in [22]. The receiver front-end array calibrates each path by measuring the output of test input signals. For measuring and analyzing the output signals, external equipments are used. Another post-calibration example are shown in $[23,24]$, which relies on external test equipments for phase sensing and control. An on-line calibration for RF phase shifters are introduced in [25]; however, it requires a reference signal with well-defined phase and amplitude. In ad-
dition, the variations of the analog circuits in the feedback loop have not been taken into account. A self-calibration method is presented in [26], but it also needs external test equipments for sensing and complex DSP for control. Moreover, this method can be applicable only to an LO phase shifting system. Such previous calibration methods employ external test equipments or external signal source for calibration, and PVT variations of the calibration circuits have not been properly addressed. Furthermore, due to the difficulty in sensing a phase difference at high frequencies, on-line selfcalibration for RF phase shifters has not been reported. So far, there has been no on-line self-calibration system for RF phase shifters in its true sense.


Fig. 1.3. Conceptual diagram of the proposed system.

In this work, we propose on-line self-calibration scheme for RF phase shifters using a novel phase amplification and a new pulsewidth-to-digital converter. The proposed self-calibration system enables 1) PVT-tolerant sensing and control loop 2) on-chip calibration 3) lesser complexity and 4) wide bandwidth ( 7 to 13 GHz ) with the calibration. Therefore, we can achieve a guaranteed performance of a RF phase shifter despite process variability of scaled technologies. Fig. 1.3 shows a conceptual diagram of a phased array with the proposed self-calibration. The self-calibration procedure is as following:

1) A phase difference between a phase shifter and a reference is amplified and


Fig. 1.4. Application of the prototype IC in a phased array. (a) In a receiver and (b) In a transmitter.
sensed and then, the amplified phase difference is represented by a pulsewidth of the output signal.
2) The pulsewidth is converted to an 8-bit digital code, which is proportional to the pulsewidth (i.e. phase difference) in low-frequency digital domain. Early adoption of digital processing enables the feedback loop robust to PVT variations.
3) This 8-bit digital code is compared with a preset 8-bit digital code (i.e. desired phase shift) and, based on this comparison, the phase shifter is calibrated.

Fig. 1.4(a) and (b) show the scope and application of the prototype IC in a receiver and a transmitter in a phased-array system, respectively. In the prototype IC, two phase shifters and the self-calibration system were implemented. One phase shifter is for phase shift and the other one is for phase reference.

### 1.1.3 Wide dynamic range LNA design

Gain, bandwidth, NF, power, area, impedance matching, supply voltage, and linearity are design parameters considered in LNA design. Unfortunately the optimization of individual design parameters does not go hand in hand, mandating tradeoffs among them. One of the most difficult challenges for LNA design in modern CMOS technologies is achieving high linearity. Device scaling in CMOS technologies has provided a significant improvement in the transit frequency $\left(f_{T}\right)$ of transistors, enabling LNA design with improved performances except the linearity [28]. The scaling in supply and breakdown voltages also adversely affects the linearity of CMOS LNAs [6, 29]. To mitigate the linearity issue, two design approaches have been applied for LNA design in general. The one emphasizes the tradeoff among the design parameters, and tries to improve the linearity at the minimal cost of other design parameters [30-35]. The effectiveness of this approach is limited to relatively small input power levels, and the front-end with this kind of LNAs can be saturated with large input signals.


Fig. 1.5. Conceptual diagrams of high-gain (HG) and high-linearity (HL) operations. (a) Receiver block diagram for the proposed LNAs and (b) Input power versus output power characteristic.

The other debinds the LNA design metrics to address the linearity issue [36-47]. In this approach, when the input signal is weak, the receiver performance mainly relies on the noise and gain performances and the effect of linearity is minimal. When the input signal is strong, it is the other way around. Based on the design metric debinding approach, the proposed LNA operation is divided into two modes: highgain and high-linearity modes as shown in Fig. 1.5. The high-gain mode focuses on noise and gain performances, but minimally considers linearity. The high-linearity mode focuses on input intercept points (IIP3) and P1dB, but pays less attention to noise and gain performances. The two operation modes are controlled in a digital
manner. With the design metric debinding approach, we tried to overcome the issues of this type of LNAs, which will be discussed below.

Such dual-mode design can be easily implemented by using two LNAs supporting high-gain and high-linearity modes respectively, in parallel, and by enabling one of the two according to the input power level. However, in addition to the obvious area penalty, this bulky design consisting of two independent LNAs suffers from increased parasitic, degrading its performance at high frequencies. For this reason, a reconfigurable design that shares most of the components among the multiple operation modes is preferred. However, sharing components poses challenges because of the strong correlation between the design parameters. The design examples in [42] and [43] provide multiple gains focusing on low-frequency ( $<1 \mathrm{GHz}$ ) applications. The designs presented in [40] and [47] provide multiple gain modes for narrowband (5.75 GHz ) and wideband ( 0.1 to 6 GHz ) applications, respectively, but need relatively high power dissipation. Additionally, good input impedance matching for large input signals is lacking in the existing multi-/dual-mode LNA designs. Good input impedance matching for large input signals is important since the reflected signal could be strong enough to cause interference in nearby devices and be reflected again back to itself degrading signal quality [48]. Another important design consideration that has not been fully explored in the existing designs is the forgiveness for errors in the modetransition point estimation. Since the transition among different gain modes relies on the measured signal power in many cases, there must be enough overlap in terms of the receiver performance between the adjacent gain modes to compensate for errors in power sensing.

In this work, we present a dual-mode (positive-gain and attenuation modes) design approach that provides a low-power and wide dynamic range operation while effectively addressing the input impedance matching issue for large and small signals alike and the forgiveness for power sensing errors. The design approach is applied to a narrowband LNA working at 5.1 GHz and a wideband LNA working from 0.8 to 6 GHz. The narrowband LNA is based on the inductively source degenerated topology
and the wideband one is based on the resistive feedback topology presented in [49]. The reconfigurable design, sharing most of the components between the two operation modes, also achieves negligible performance degradation at high frequencies.

### 1.2 Outline of Dissertation

This dissertation is organized in the following manner. Chapter 1 provides the motivation and brief overview of the research presented in this dissertation. Chapter 2 focuses on the design of the self-calibration system for RF phase shifters. Chapter 2 starts with the design of a main phase shifter, which is calibrated by the proposed system, in Chapter 2.1. The proposed phase sensing method including a novel phase amplification technique is presented in detail in Chapter 2.2. Then, in Chapter 2.3, the design and performance of the proposed PVT-tolerant pulsewidth-to-digital converter is described. Chapter 2.4 introduces a decision algorithm and circuit implementation, which is essential to properly sense a right phase shift. In Chapter 2.5 , the overall system architecture and performance including a digital controller is discussed. Chapter 3 presents the design of the proposed wide dynamic range LNAs. Chapter 3.1 introduces previous multi-/dual-mode LNA designs. The 5.1 GHz narrowband LNA and the 0.8 to 6 GHz wideband LNA designs are discussed in detail in Chapter 3.2 and 3.3, respectively. The experimental results of the narrowband and the wideband LNAs are shown in Chapter 3.4. Finally, Chapter 4 summarizes and concludes the dissertation.

## 2. SELF-CALIBRATION SYSTEM FOR RF PHASE SHIFTERS

### 2.1 Main Phase Shifter Design

Before discussion of the proposed self-calibration loop, the main RF phase shifter design in the proposed system is presented. There have been several phase shifting methods in RF domain: switched-delay line [50], loaded-line [51], reflection-type [52, 53], high-pass/low-pass [54-56], by-pass/low-pass [19, 57,58], and I/Q-vector-sum [23, 26, 59-61]. Among those techniques, as shown in Fig. 2.1, I/Q-vector-sum phase shifter generates a desired phase shift by using weighted sum of I and Q signals. The phase shift $(\theta)$ and amplitude $(R)$ of the phase shifter can be expressed by,

$$
\begin{align*}
& \theta=\tan ^{-1}\left(\frac{Q_{0}}{I_{0}}\right)  \tag{2.1}\\
& R=\sqrt{I_{0}^{2}+Q_{0}^{2}} \tag{2.2}
\end{align*}
$$



Fig. 2.1. Sum of weighted I and Q signals to generate a phase shift.

I/Q-vector-sum type is also an active design approach and it is widely used with the merits of small area, decent gain, and fine digital control [59]. Fig. 2.2(b) shows the schematic of the I/Q-vector-sum phase shifter, which is adopted in the proposed
system. The strength of I and Q signals are controlled by current DACs, which are named as DI and DQ in Fig. 2.2(b). In addition, the quadrant of a phase shift, from $0^{\circ}$ to $360^{\circ}$, is determined by the switches of SW1 to SW4. They control the positive or the negative path of I and Q signals.


Fig. 2.2. Main phase shifter. (a) Quadrature all-pass filter and (b) IQ-vector-sum RF phase shifter.

However, this type of phase shifter requires I and Q signals. To obtain $\mathrm{I} / \mathrm{Q}$ signals from an input differential signal, a quadrature-all-pass filter (QAF) is often used [59-61]. The schematic of a QAF is shown in Fig. 2.2(a). A QAF is reported to provide wideband property; however, since it consists of $L$ and $C$, it is inherently frequency-dependent. In addition, a QAF shows relatively large phase and amplitude
variation between I and Q signals, because a QAF is affected by capacitive loading and also suffers from process variation of the passive components of $\mathrm{R}, \mathrm{L}$, and C . According to [59], with $\mathrm{L}( \pm 5 \%), \mathrm{C}( \pm 5 \%), \mathrm{R}( \pm 10 \%)$ variations and $\pm 3 \sigma$ statistical variation, phase error of $\pm 15^{\circ}$ and amplitude mismatch of $1.2 \pm 0.3 \mathrm{~dB}$ are reported in 8 to 18 GHz . Here, it should be noted that performance metrics of a phase shifter are RMS phase error $\left(\theta_{\Delta, R M S}\right)$ and RMS amplitude (gain) error $\left(A_{\Delta, R M S}\right)$, and those are defined as [59],

$$
\begin{equation*}
\theta_{\Delta, R M S}(d e g)=\sqrt{\frac{1}{N-1} \times \sum_{i=2}^{N}\left|\theta_{\Delta i}\right|^{2}} \tag{2.3}
\end{equation*}
$$

where $N$ is number of phase shifts and $\theta_{\Delta i}$ is the $i$-th phase error from the ideal $i$-th phase shift.

$$
\begin{equation*}
A_{\Delta, R M S}(d B)=\sqrt{\frac{1}{N} \times \sum_{i=1}^{N}\left|A_{\Delta i}\right|^{2}} \tag{2.4}
\end{equation*}
$$

where $A_{\Delta i}=A_{i}-A_{\text {ave }}$. The $A_{i}$ is the $i$-th insertion gain and $A_{\text {ave }}$ is the average insertion gain. The maximum phase error and amplitude error are also often used. The maximum phase error and amplitude error are defined as the maximum values of $\theta_{\Delta i}$ and $A_{\Delta i}$, respectively. The 4-bit I/Q-vector-sum phase shifter in [59] shows the RMS phase error of $3^{\circ}$ to $7^{\circ}$ from 7 to 13 GHz in single chip measurement under one ambient condition.


Fig. 2.3. Modified QAF schematic.

In the proposed self-calibrated phased-array, we adopted the conventional QAF and 4-bit IQ-vector-sum phase shifter as main phase shifters. Since the QAF in Fig.

Table 2.1
Component values of the modified QAF

|  | R1 | L | C | R2 |
| :---: | :---: | :---: | :---: | :---: |
| Value | $12.5 \Omega$ | 0.78 nH | 240 fF | $106 \Omega$ |



Fig. 2.4. Simulation results of the modified QAF. (a) I and Q amplitude, (b) I and Q phase, and (c) S11.
2.2(a) provides input impedance matching to differential $50 \Omega$ [59], we modified the QAF as in Fig. 2.3 to match differential $100 \Omega$ for test purpose. In addition, our target frequency is 7 to 13 GHz and the corresponding component values of the QAF

(a)

(b)

Fig. 2.5. Binary 8-bit current-steering DAC. (a) Schematic and (b) Layout $(140 \mu m \times 85 \mu m)$.
are listed in Table 2.1. Fig. 2.4 shows the performance of the modified QAF. From 7 to 13 GHz , the I/Q phase error and the amplitude error of the QAF are $4^{\circ}$ and 1.9 dB , respectively. Hence, these errors should be properly compensated in the phase shifter design by adjusting the strength of I and Q signals. However, this compensation is typically performed for one process corner and one ambient condition. Considering process and temperature variations, the errors would be even worse and the phase shifter performance would not be guaranteed. As shown in Fig. 2.4(c), the S11 of the QAF is below -11.4 dB over the target frequency.

Table 2.2
Phase shift vs. digital code of DI and DQ current DACs (0: GND, 1: VDD)

| Phase shift $\left({ }^{\circ}\right)$ | SW1 | SW2 | SW3 | SW4 | DI | DQ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 1 | 0 | 0 | 0 | 11110000 | 00000000 |
| 22.5 | 1 | 0 | 1 | 0 | 11100000 | 00110000 |
| 45 | 1 | 0 | 1 | 0 | 10010000 | 01100000 |
| 67.5 | 1 | 0 | 1 | 0 | 01000000 | 10010000 |
| 90 | 0 | 0 | 1 | 0 | 00000000 | 10010000 |
| 112.5 | 0 | 1 | 1 | 0 | 01000000 | 10010000 |
| 135 | 0 | 1 | 1 | 0 | 10010000 | 01100000 |
| 157.5 | 0 | 1 | 1 | 0 | 11100000 | 00110000 |
| 180 | 0 | 1 | 0 | 0 | 11110000 | 00000000 |
| 202.5 | 0 | 1 | 0 | 1 | 11100000 | 00110000 |
| 225 | 0 | 1 | 0 | 1 | 10010000 | 01100000 |
| 247.5 | 0 | 1 | 0 | 1 | 01000000 | 10010000 |
| 270 | 0 | 0 | 0 | 1 | 00000000 | 10010000 |
| 292.5 | 1 | 0 | 0 | 1 | 01000000 | 10010000 |
| 315 | 1 | 0 | 0 | 1 | 10010000 | 01100000 |
| 337.5 | 1 | 0 | 0 | 1 | 11100000 | 00110000 |



Fig. 2.6. Bias generator schematic ( $\operatorname{Iref}=7.5 \mu \mathrm{~A})$ for the main phase shifter.

In order to control the strength of I and Q signals, binary 8-bit current-steering DAC is designed and used. The unit resolution current is $7.5 \mu \mathrm{~A}$ and it is generated by bias generator shown in Fig. 2.6. The external resistor for the bias generator is $61.5 \mathrm{k} \Omega$ to supply $7.5 \mu \mathrm{~A}$. The self-calibration block will use a separate bias generator. The 8-bit current DAC layout is shown in Fig. 2.6(b). In the layout, common-centroid technique and dummy cells are used for device and current matching.

Table 2.2 shows the setting of SW1~SW4 and DI \& DQ for each phase shift. Since we use 4 -bit phase shifters, the phase resolution is $22.5^{\circ}$. The 8 -bit digital codes for DI and DQ are compensated values according to the QAF performance as seen in Fig. 2.4 for TT process corner and $27^{\circ} \mathrm{C}$. Fig. 2.7 shows the simulated performance of the 4 -bit phase shifter. The phase shift and gain are depicted in Fig. 2.7(a) and (b), respectively. As shown in Fig. 2.7(c) and (d), the maximum phase error is $6^{\circ}$ and the maximum gain error is 1 dB from 7 to 13 GHz . In addition, Fig. 2.8 is Monte Carlo simulation results with the phase shift setting for $292.5^{\circ}$ and it shows the largest phase error of $-7^{\circ}$ to $10^{\circ}$.


Fig. 2.7. Performance of the main phase shifter. (a) Phase shift, (b) Gain, (c) Phase error, and (d) Gain error.


Fig. 2.8. Monte Carlo simulation with the phase shift setting for $292.5^{\circ}$.

### 2.2 Proposed Phase Sensing Method

### 2.2.1 Novel phase amplification technique

The fundamental issue of the self-calibration scheme for RF phase shifters is how to sense phase difference at high frequencies. Our target frequency is 7 to 13 GHz , and the difficulty lies in that a phase has to be gauged in sub-pico-second range of time. For example, the phase of $1^{\circ}$ at 10 GHz is equivalent to 0.277 ps in time and it is difficult to accurately sense such a small time as it is. In this work, we propose a simple and accurate method for time-difference amplification and sensing. As shown in Fig. 2.9, when two frequency different signals are applied to an adder and the adder output is gone through an envelope detector, the phase $(\phi)$ at the envelope detector output is amplified by $\omega_{1} / \Delta \omega$ where $\Delta \omega=\left|\omega_{1}-\omega_{2}\right|$. In addition, the adder can be easily implemented in current domain.


Fig. 2.9. Proposed phase amplification technique.


Fig. 2.10. Proposed phase amplification technique applied to a phaseshifted path and a reference path in a phased array.

(a)

(b)

Fig. 2.11. Example of proposed phase amplification method. (a) Summation of two 10 GHz signals and 10.01 GHz signal and (b) Transient simulation.

Since a phased-array system has phase shifters and a reference phase, this proposed phase amplification method can easily applied to sense a relative phase difference as illustrated in Fig. 2.10. A signal of $\omega_{2}$, which is a close frequency to $\omega_{1}$, is summed to phase-shifted signal and reference signal, respectively. Then, the two summed signals go through the two envelope detectors. Now, we obtain two phase-amplified signals and compare the phase difference as being amplified. Fig. 2.11 shows an example of the phase amplification method. Two 10 GHz signals which have phase
of $45^{\circ}$ and $0^{\circ}$ are applied to two adders, respectively, and those signals are added by 10.01 GHz signal. After the summation, as seen in Fig. 2.11(b), the envelopes are 10 MHz signals, and the $45^{\circ}(12.5 \mathrm{ps})$ relative phase is amplified by 1000 times (i.e. 12.5 ns ). It should be mentioned that this phase amplification method works all for two sinusoids, one sinusoid and one square signal, and two square signals. In the proposed system, we use two square signals because, if two applied signals of the same frequency have different amplitude, we would have two different-amplitude envelopes after phase amplification. Hence, we have to be careful to find the points to be compared for the phase difference sensing in such a case. However, if we use rail-to-rail square wave, we do not need to worry about the amplitude difference between the two phase-amplified signals.

### 2.2.2 $f / 2+\Delta f$ signal generator



Fig. 2.12. Continuous linear delay with respect to time.

We devised the phase amplification method. In order to use the method, we need an additional signal which has a close frequency to the main signal. In addition, the calibration loop should have minimal overhead to the main phased array. In reality, it is not feasible to use two VCOs because there would be possible frequency pulling between two VCOs and we would also have a problem of locking of two VCOs. So


Fig. 2.13. Phase rotator schematic including the 8 -bit thermometercode current DACs (D1 to D4).


Fig. 2.14. Current source (D1 to D4) control signals for $f+10 \mathrm{MHz}$ generation.
we have an issue of how to generate $f+\Delta f$ signal. We look into a delay and as we can see the following equation,

$$
\begin{equation*}
\cos \left(\omega_{0} t+\alpha t\right) \tag{2.5}
\end{equation*}
$$

if we make a continuous linear delay with respect to time, we can obtain a frequency shift. Hence, in order to attain a 10 MHz -distant frequency signal, we can use a phase rotator producing a continuous linear delay as in Fig. 2.12. With I and Q signals, a phase rotator as shown in Fig. 2.13 can be used to generate such a delay. D1~D4 are 8-bit thermometer-code current DACs in the proposed system. For better device and current matching, thermometer-code type is employed rather than binary one. The current DACs are controlled by digital signals shown in Fig. 2.14 to produce a 10 MHz -distant signal.


Fig. 2.15. 5.01 GHz generation from 10 GHz . (a) Output of the phase rotator and (b) FFT of the phase rotator output.

For this phase rotator operation, we also need I and Q signals. Latch-based I/Q divider in Fig. 2.22 [62] is used to generate I and Q signals from the original differential signal. Since the original signal is divided by 2 , we have actually $f / 2+\Delta f$ signal instead of $f+\Delta f$. Fig. 2.15 shows the phase rotator output, generating 5.01 GHz from 10 GHz original signal. Initially, it takes approximately 80 ns to properly produce 5.01 GHz sginal. Spurs distant from the output signal by 40 MHz will be rejected by an ED and a LPF. Fig. 2.16 shows the delay of the 5.01 GHz output signal compared


Fig. 2.16. Continuous linear delay for the 5.01 GHz generation.
with the divided 5 GHz signal. As we can see, after the 80 ns initialization, the delay is continuously linear with respect to time and the delay changes 200ps in 100ns. The delay of 200 ps corresponds to $2 \pi$ phase shift at 5 GHz . Thus, the output signal is expressed as

$$
\begin{aligned}
\text { Output signal } & =\cos \left(2 \pi \times 5 G H z \times t+\frac{2 \pi}{100 n s} \times t\right) \\
& =\cos (2 \pi \times 5 G H z \times t+2 \pi \times 10 M H z \times t) \\
& =\cos (2 \pi \times 5.01 G H z \times t)
\end{aligned}
$$

and the 10 MHz -distant signal is obtained from the divided 5 GHz signal.

### 2.2.3 Overall architecture for phase shift sensing

Fig. 2.17 is an overall diagram for phase difference sensing with phase amplification including the main phase shifters. Due to poor performance of a frequency doubler, we use divide-by-2 for main phase shifters, too. For this purpose, TSPC divide-by-2 circuit [63] is employed and the TSPC schematic is shown in Fig. 2.23. These I/Q divider and TSPC divider are designed to operate up to 16 GHz under


Fig. 2.17. Block diagram for phase difference sensing with phase amplification.
all process corners and $65^{\circ} \mathrm{C}$ in post-layout simulation. Now, we compare the phase difference in $f / 2$ range. The two phase-amplified signals go through envelope detectors, low-pass filters, and self-reference comparators. The signals at the output of the self-reference comparators are 10 MHz digital signals, and the XOR senses the phase difference in 10 MHz range. Another important advantage of this sensing method is that any systematic offsets including PVT variations can be cancelled out if the layout of the two paths is symmetric and close enough. We used interdigitation, commoncentroid, and dummy cells for the layout of the two paths. The schematics of the building blocks are also shown in Fig. 2.23 to 2.26.

Fig. 2.18 to 2.20 show simulation results of the phase difference sensing, where $22.5^{\circ}, 225^{\circ}$, and $337.5^{\circ}$ phase differences at 10 GHz are sensed respectively. An upper figure is the XOR output and a lower one is the ED and LPF outputs. In this simulation, $\Delta f$ of 10 MHz was used and we can see that the phase difference can be sensed within $0.8^{\circ}$ error. In addition, we need to consider the variation of the I/Q divider. The maximum phase variation of $I$ and $Q$ signals from a latch-based $I / Q$


Fig. 2.18. $22.5^{\circ}$ phase difference sensing.


Fig. 2.19. $225^{\circ}$ phase difference sensing.
divider is $5^{\circ}$ [64]. Including the $5^{\circ}$ error, the phase difference was sensed within $1^{\circ}$


Fig. 2.20. $337.5^{\circ}$ phase difference sensing.


Fig. 2.21. Phase shift vs. pulsewidth (i.e. duty cycle) of the XOR output.


Fig. 2.22. I/Q divide-by-2 circuit schematic.


Fig. 2.23. TSPC schematic of divide-by-2 circuit for main phase shifter.


Fig. 2.24. Adder schematic.


Fig. 2.25. Envelope detector.


Fig. 2.26. Self-reference comparator.
error, too. It is because such a systematic offset can be cancelled out, as mentioned before.

The output, i.e. pulsewidth of the XOR output, will be converted to an 8-bit digital code by a pulsewidth-to-digital converter (TDC) for digital-domain processing, which will be discussed in Section 2.3. The diagram in Fig. 2.21 depicts the relationship between phase shift at RF and pulsewidth of XOR output (i.e. duty cycle of XOR output) in $\Delta f$ range. Since the main phase shifter is 4 -bit phase shifter, the phase resolution is $22.5^{\circ}$. Since the phase fine resolution for the calibration is determined by the binary 8 -bit current DACs in the main phase shifter, an 8-bit digital comparator will be used to compare the sensed 8-bit digital code (from the TDC) and the 8 -bit preset value (indicating a desired phase shift). The 8 -bit preset values are also shown in Fig. 2.21. Finally, Table 2.3 shows the power consumption for phase sensing with the power dissipation of the individual blocks. The total power

Table 2.3
Power consumption for phase sensing with 1V supply

|  | Current (mA) | number | Total current <br> $(\mathrm{mA})$ |
| :---: | :---: | :---: | :---: |
| Phase rotator and buffers | 2.5 | 1 | 2.5 |
| IQ divider and buffers | 4.8 | 1 | 4.8 |
| TSPC divider and buffers | 1.12 | 2 | 2.24 |
| Adder | 2 | 2 | 4 |
| Envelope detector | 0.08 | 2 | 0.16 |
| Self-reference comparator | 0.18 | 2 | 0.36 |
| Bias circuit | 0.4 | 1 | 0.4 |
| Total | 14.46 |  |  |

consumption is 14.46 mW for phase sensing. Since the building blocks are high-speed analog and digital circuits, it dissipates the most power in the self-calibration system.

### 2.3 Proposed Pulsewidth-to-Digtal Converter (TDC)

After the XOR, we have 20 MHz digital signal and its pulsewidth represents phase difference. The pulsewidth needs to be converted to an 8-bit digital code for digitaldomain processing, which makes the calibration loop robust to PVT variations. However, we have the following issues in pulsewidth-to-digital conversion:

1) How to overcome random noise? Hence, we need averaging.
2) How to overcome PVT variations in the digital conversion?
3) How to handle wide input dynamic range of almost $0^{\circ}$ to $360^{\circ}$ phase?

TDC design has a tradeoff between resolution and input dynamic range. A state-of-the-art wide-input-range TDC provides 0.1 ns resolution and 0 to 2 ns input range [65]. To achieve the maximum $2^{\circ}$ phase error with the calibration and $0^{\circ}$ to $360^{\circ}$ input
range, we require 0.2 ns resolution and 0 to 100 ns input range. In this work, from the dual-slope integrating ADC concept [66], an 8-bit dual-slope integrating pulsewidth-to-digital converter (TDC) is presented. Before discussion of the proposed TDC design, the next section will briefly discuss the dual-slope integrating ADC.

### 2.3.1 Conventional dual-slope integrating ADC

Fig. 2.27 shows a block diagram of the dual-slope integrating ADC and Fig. 2.28 illustrates the operating principle of a 3-bit dual-slope integrating ADC with two different inputs. After the reset sets the integrator input and output to be a common-mode voltage of the op-amp (Vcm), during the fixed integration period (T1 $=2^{\wedge}$ number of bits $\times T_{\text {clk }}$ ), the switch at the input of the integrator is connected to the input voltage $\left(V_{I N}\right)$ and the integrator output is charging. After T1, the switch is connected to the reference voltage $\left(V_{R E F}\right)$ and the integrator starts discharging with $V_{R E F}$. Hence, the discharging period, the slope is always constant regardless of an input. During this period, the counter operates. As soon as the integrator output goes below Vcm, the comparator sends a signal so that the counter stops its operation and the counter values is stored in the latch. As a result, the ADC output is proportional to the input voltage and the digital conversion has been done.


Fig. 2.27. Block diagram of conventional dual-slope integrating ADC [66].


Fig. 2.28. Operating principle with 2 different inputs [66].

Even though a dual-slope integrating ADC has relatively slow conversions, it provides high accuracy, high resolution, and low power. Moreover, the most important advantage of the dual-slope integrating ADC is to be robust to PVT variations. Since the same integrator and the same clock are used to produce both charging and discharging slopes, any non-idealities including PVT variations would be essentially cancelled out.

### 2.3.2 Proposed 8-bit dual-slope integrating TDC

The simplified diagram of the proposed 8-bit dual-slope integrating TDC is shown in Fig. 2.29. The diagram shows the core of the TDC and it does not include 8-bit counter, digital control, bias circuitry, buffers, etc. The Vcm of op-amp in the integrator is set to 500 mV , and VL and VH is 450 mV and 550 mV , respectively. The Vcm, VL, and VH are produced by a resistive divider which includes 40 series resistors. In the TDC design, the relative values of $(\mathrm{Vcm}-\mathrm{VL})$ and $(\mathrm{VH}-\mathrm{Vcm})$ are required to be the same rather than the absolute values of Vcm, VL, and VH. Hence, the resistive


Fig. 2.29. Simplified diagram excluding 8-bit counter, digital control, bias circuitry, buffers, etc.
divider is designed to provide a constant ratio regardless of PVT variations. Consequently, the constant up- and down-slopes are achieved. Fig. 2.30 also illustrates the TDC operating principle with an XOR output of $50 \%$ duty-cycle (i.e. $180^{\circ}$ phase shift). The conversion procedure of the TDC can be explained as following:

1) The reset signal sets the integrator input and output to be Vcm.
2) XORen enables the XOR output to be applied to SW1 during a fixed time period T1, which is 256 cycles with 10 MHz clock. Hence, the XOR output controls SW1 and it connects VL to the integrator only when the XOR output is high. Depending on the duty cycle of the XOR output, the integrator repeats integrating and stopping until the fixed T1.
3) After T 1 , CountEN is set to high and the integrator starts discharging with VH. During this period, the 8-bit counter operates.
4) As soon as the integrator output goes below Vcm, the comparator sends a signal to stop the counter operation. The final counter value is stored in the registers.


Fig. 2.30. Operating principle with $50 \%$ duty-cycle.

We can obtain an 8-bit digital output which is proportional to the duty cycle (i.e. pulsewidth). Then, a beacon signal informs the following stage of the availibility of the TDC output so that the following stage would catch it for the further processing
5) The TDC will wait for the next update of the XOR output during the programmed wait time.

In the TDC design, it should be noted that, during the first integration with XOR output, the integrator input can be a floating node when XOR output is low. Since the integrator is a continuous analog circuit, the integrator keeps integration if there is a tiny voltage difference between the input and Vcm. As a result, the integrator output could be slightly deviated from the expected value. To prevent the floating input, a prevent-floating circuit is added at the integrator input as shown in Fig. 2.29. Only when both enabled XOR output and CountEN are 0 , the integrator input
is fixed to Vcm. It can prevent undesired integration when the XOR output is low during the first integration.

The TDC operation can also be expressed in the following manner to clearly prove how the 8 -bit ouput of the counter is proportional to the duty cycle of the XOR output:

$$
\begin{aligned}
& T_{u p}=\text { time for up-slope } \\
& T_{\text {down }}=\text { time for down-slope } \\
& T_{c l k}=\text { period of clock } \\
& P=\text { duty cycle (in percentage of } T_{c l k} \text { ) }
\end{aligned}
$$

The peak of the waveform can be given by $\left(V_{i n} \times T_{u p}\right) / R C$ and it is also given by $\left(V_{\text {in }} \times T_{\text {down }}\right) / R C$. Therefore, $T_{u p}=T_{\text {down }}$. If we let the up-slope be fixed number of clock $(N)$ but the XOR output has $P$ duty cycle, then

$$
\begin{equation*}
T_{u p}=N \times P \times T_{c l k} \tag{2.6}
\end{equation*}
$$

We let the duty cycle of the down-slope be fixed, but the number of counts $(M)$ be variable. Then,

$$
\begin{equation*}
T_{\text {down }}=M \times T_{c l k} \tag{2.7}
\end{equation*}
$$

Since $T_{u p}=T_{d o w n}, N \times P \times T_{c l k}=M \times T_{c l k}$. Thus,

$$
\begin{equation*}
P=\frac{M}{N} \tag{2.8}
\end{equation*}
$$

which means that $P$ is proportional to $M$.

### 2.3.3 Performance and simulation results

The TDC is tested with $50 \%$ and $6.25 \%$ duty cycle of inputs with 5 process corners (TT, FF, FS, SF, SS). The TDC outputs are the same for each case. For the $50 \%$ and $6.25 \%$ duty cycle, the outputs are 10000001 and 00010001, respectively. Fig. 2.31 shows the simulation results with $50 \%$ duty cycle including integrator output, control signals, and 8-bit digital output of the TDC. TDC_done is the beacon signal


Fig. 2.31. TDC simulation results with $50 \%$ duty cycle: integrator output, control signals, and 8 -bit digital output of the TDC.
to inform the following stage that one-cycle of the TDC operation is complete. The Vcm of the integrator is set to 500 mV . Total power consumption is only $740 \mu \mathrm{~W}$ with 1V power supply as shown in Table 2.4 and it also summarizes the TDC performance. Fig. 2.32 shows the bias generator for the TDC and it also provides bias currents for all the calibration blocks. It supplies a reference current of $10 \mu \mathrm{~A}$ with $\mathrm{R}=8.8 \mathrm{k} \Omega$. The schematic also contains a start-up circuit.

In recapitulation, the proposed TDC has the following advantages and it enables a PVT-tolerant self-calibration system. The TDC design is also able to resolve the issues aforementioned.

- It can average out random noise during the 256 cycles.
- Since the rising slope and the falling slope is the same, it provides PVT-tolerant performance.
- It has the same benefits of dual-slope integrating ADC, which are high accuracy,


Fig. 2.32. Bias generator schematic ( $\operatorname{Iref}=10 \mu \mathrm{~A})$ for the calibration blocks.
high resolution, and low power consumption.

- It provides a wide input dynamic range of almost $0^{\circ}$ to $360^{\circ}$.
- Slow conversion helps the feedback loop stability.

Table 2.4
8-bit TDC performance summary

| Bit resolution $\left({ }^{\circ}\right)$ |  | 1.4 |
| :---: | :---: | :---: |
| Input range $\left({ }^{\circ}\right)$ |  | $0 \sim 360$ |
| Power <br> consumption <br> $(\mu \mathrm{W})$ | Integrator | 100 |
|  | Comparator | 80 |
|  | Analog buffers | 320 |
|  | Digital and bias circuits | 240 |
|  | Total | 740 |

### 2.4 Decision Algorithm and Circuit



Fig. 2.33. Issue due to using divide-by-2 for the main phase shifter.

We obtain an 8-bit digital output by the TDC, which has the phase shift information. But we have one more issue because the divide-by-2 circuits are used for the main phase shifters. As illustrated in Fig. 2.33, for one phase shift, we may have two possible XOR outputs depending on an initial condition of the TSPC divider. It is because we do not know at which rising edge the divider would start. Hence, we need to properly choose one of them.

As in Table 2.5, we need a 4-bit initial setting in order to set the desired phase shift. It also shows the 8 -bit preset value for each phase shift. The 4 -bit codes (S3,S2,S1,S0) for initial setting are decoded for initial SW1~SW4 setting and initial DI \& DQ current DACs' setting in Fig. 2.2(b). As we can see in Fig. 2.33 and 2.34, two possible XOR outputs are 2's compliment to each other. It is noted that the $S 3$ in 4-bit initial setting indicates upper half $(S 3=0)$ or lower half ( $\mathrm{S} 3=1$ ) plane.


Fig. 2.34. 2's complement relationship of two possible TDC outputs.


Fig. 2.35. Logic implementation of the decision circuit.

Table 2.5
4 -bit initial settings and 8 -bit preset values ( 0 : GND, 1 : VDD)

| Phase shift $\left(^{\circ}\right)$ | Initial setting 4-bit <br> $(\mathrm{S} 3, \mathrm{~S} 2, \mathrm{~S} 1, \mathrm{~S} 0)$ | 8-bit preset value |
| :---: | :---: | :---: |
| 0 | 0000 | 00000000 |
| 22.5 | 0001 | 00010000 |
| 45 | 0010 | 00100000 |
| 67.5 | 0011 | 00110000 |
| 90 | 0100 | 01000000 |
| 112.5 | 0101 | 01010000 |
| 135 | 0110 | 01100000 |
| 157.5 | 0111 | 01110000 |
| 180 | 1000 | 10000000 |
| 202.5 | 1001 | 10010000 |
| 225 | 1010 | 10100000 |
| 247.5 | 1011 | 10110000 |
| 270 | 1100 | 11000000 |
| 292.5 | 1101 | 11010000 |
| 315 | 1110 | 11100000 |
| 337.5 | 1111 | 11110000 |

Hence, we can compare the S3 and the MSB of TDC output to obtain a right 8bit code representing the phase shift. If two values are the same, the TDC output is correct. Otherwise, we have to take 2's complement of the TDC output. Based on this selection function, Fig. 2.35 shows the logic implementation of the decision circuit composed of only XORs and registers.


Fig. 2.36. Architecture of the self-calibration system including the main phase shifters (one for phase shift and the other one for reference).

### 2.5 Overall Architecture of Self-Calibration System

### 2.5.1 Control algorithm and implementation

As discussed in the previous section, the two phase-amplified signals produce a digital pulse at the XOR output. Then, the 8-bit TDC and decision circuit convert the pulsewidth to an 8-bit digital code. This digital code is compared with the 8bit preset code by the digital comparator. The output of the digital comparator controls the Up/Dn counter and hence, the 8 -bit DI or DQ current DAC of the main phase shifter. Fig. 2.36 shows the overall architecture of the self-calibration system including the main phase shifters. The calibration continues until a decision circuit


Fig. 2.37. Control algorithm. (a) Quadrant selection and DI/DQ control, (b) Control for the 1st and 3rd quadrants, and (c) Control for the 2 nd and 4 th quadrants.
output equals the preset code. Once the calibration ends, the right control codes for DI and DQ current DACs are stored in the registers until the next calibration. The self-calibration loop is powered off during normal operation.

As illustrated in Fig. 2.37, the control between DI and DQ is determined by the quadrant of target phase shift. If the target phase shift is on the 1st and the 3rd quadrants as in Fig. 2.37(b), DI is fixed and DQ is increased when the preset value is bigger than the measured value, and vice versa. If the target phase shift is on the 2nd and the 4th quadrant as in Fig. 2.37(c), DQ is fixed and DI is increased when the preset value is greater than the measured value, and vice versa. In cases of $90^{\circ}$ and $270^{\circ}$ phase shifts, the digital controller is designed to properly toggle the two adjacent quadrants until the decision circuit output matches the preset code. In addition, the digital controller was designed in Verilog and then, it was synthesized with ARM standard cells, which is IBM SOI12S0 HVT Process (45nm CMOS 12S0 Technology, High Vt). The Verilog scripts are shown in Appendix A. The digital control block was verified by ModelSim and AMS as shown in Fig. 2.38. The synthesized block also includes the decision circuit, the digital comparator, and the Up/Dn counter.


Fig. 2.38. Verification of the digital control block.

### 2.5.2 Layout and performance

The prototype of the self-calibration system and the phase shifters is designed in 45 nm SOI CMOS technology. Fig. 2.39 shows the whole chip layout and pin assignment, and the chip area is $2.1 \mathrm{~mm} \times 2.1 \mathrm{~mm}$ including the pads. The calibration loop shows somewhat area overhead; however, in reality, since sixteen 4-bit phase shifters are used in a 4-bit phased array, the area overhead of the calibration loop would be significantly reduced in an actual phased array system. In addition, since 1V supply voltage is used for the prototype, an active inductor could not be adopted due to a voltage headroom issue. This design is targeted for wide bandwidth and thus, high-Q inductors are not required. If a higher supply voltage is allowed, the use of active inductors for the adder and the $f / 2+\Delta f$ generator could reduce the area overhead even further. The power overhead of the calibration loop is 16.2 mA with 1V supply. Table 2.6 also shows its power breakdown. It is noted that this power overhead is not an issue because the calibration loop is turned off once the calibration


Fig. 2.39. Layout of the self-calibration system including the main phase shifters.
is complete. Considering the error from phase sensing and the quantization error from the TDC, the maximum phase error is estimated to be less than $2^{\circ}$.

### 2.5.3 Test setup

The test of the prototype can be performed either with internal digital control or with external FPGA control. As shown in Fig. 2.40, for using the internal control, synth_sel is set to VDD. Using SPI control with 1 kHz SPI clock, an initial setting

Table 2.6
Power breakdown of the self-calibration loop

|  | Power consumption (mW) |
| :---: | :---: |
| Phase sensing | 14.46 |
| TDC | 0.74 |
| Digital controller, buffers, bias | $\sim 1$ |
| Total | 16.2 |

needs to be done as following:

- S3,S2,S1,S0: 4-bit target phase shift setting
- Iext and Qext: Initial upper 4-bit for DI/DQ registers and hence, DI/DQ current DACs
- Preset: 8-bit preset code
- Programmable loop settling time: TDC wait time with a 24 -bit register; 16bit input will be loaded into upper 16 bits of the register; TDC wait time can be programmed from $25.6 \mu$ s to 1.67 s

Other external control and output signals are also as following:

- synth_sel: Multiplex between internal control and external FPGA control
- rst: Global digital reset
- load: Load initial DI and DQ values to DI/DQ registers from SPI registers
- count: Enable/disable calibration
- calib_comp: Output signal to inform the calibration complete

The calibration is controlled by the input signals of load and count designed in the following sequence:

1) load $=0$, count $=0$ : Through the SPI control, all initial values are loaded to the SPI registers.
2) load is set to $0 \rightarrow 1$ (count $=0$ ): The DI/DQ registers are loaded with external


Fig. 2.40. Test board setup.

Table 2.7
Truth table for load and count ( 0 : GND, 1: VDD)

| load | count | Operation |
| :---: | :---: | :---: |
| 0 | 0 | Do nothing; retain values |
| $0 \rightarrow 1$ | 0 | Load external values to DI/DQ registers |
| $1 \rightarrow 0$ | 0 | Load Up/Dn counter depending upon S2 value |
| 0 | $0 \rightarrow 1$ | Calibration loop starts |
| 1 | 1 | Prohibited |

initial values.
3) load is set to $1 \rightarrow 0$ (count $=0$ ): Based on S 2 indicating the quadrant (1st and

3rd, or 2nd and 4th), either DI or DQ value is loaded to the Up/Dn counter.
4) count is set to $0 \rightarrow 1(\operatorname{load}=0)$ : The calibration operation begins. [Note] count should be set to 1 after all values are settled with load $=1 \rightarrow 0$ (i.e. after a proper delay).
5) If count $=0($ load $=0)$, the calibration loop stops and the final calibrated DI or DQ values are retained in DI or DQ registers. Table 2.7 summarizes the function of load and count signals.

In addition, an external 160 MHz crystal oscillator is used to control the 8 -bit thermometer-code current DAC in the $f / 2+\Delta f$ generator, for the generation of $\Delta f=10 \mathrm{MHz}$ distant signal. A divide-by-16 circuit as shown in Fig. 2.41 is implemented to provide the TDC, decision circuit, digital comparator, and digital controller with 10 MHz system clock. When calibration is complete, the output signal of calib_comp will be changed from 0 to 1 .


Fig. 2.41. Block diagram of the divide-by-16 circuit.

### 2.6 Conclusion

In this work, we presented an on-line self-calibration system for RF phase shifters in a phased array. In the proposed system, we also developed a novel phase amplification for phase sensing and a new dual-slope integrating pulsewidth-to-digital converter (TDC) for a PVT-tolerant sensing/control loop. These unique techniques are applied to a 4-bit IQ-vector-sum phase shifter and the phase shifter can operate in 7 to 13 GHz with the phase error of less than $2^{\circ}$. This design methodology is the first on-line self-calibration for RF phase shifters, which is fully implemented on chip.

The proposed calibration system also provides lesser design complexity, and it does not require external equipments and complex DSP. Moreover, this calibration scheme can be applied to other types of RF phase shifters.

## 3. WIDE DYNAMIC RANGE LNA DESIGN

### 3.1 Previous Multi-/Dual-Mode LNA Designs

The existing works on multi-/dual-mode LNAs can be roughly categorized into seven approaches: (1) two independent gain paths [36,37], (2) variable transconductance $\left(g_{m}\right)$ [38,39], (3) variable load impedance [40,41], (4) pre-attenuation [42-45], (5) current steering [43], (6) current splitting [42,46], and (7) multiplexing gain paths [47]. The design with two independent signal paths in Fig. 3.1(a) is easy to implement, but wastes die area. It could also suffer from the increased parasitic and the signal loss in a mode selection switch. The variable $g_{m}$ approach in Fig. 3.1(b) can provide a wide gain tuning range. However, since an input impedance is a strong function of $g_{m}$ in most LNA design, providing a consistent input matching quality over a wide gain tuning range is challenging. Furthermore, typically there is no linear relation between $g_{m}$ and linearity, which prohibits an effective implementation of a dual-mode design with high-gain and high-linearity modes. The variable load approach in Fig. 3.1(c) could also provide a wide gain tuning range, but it provides a negligible linearity tuning range because of its fixed input biasing condition. The resistive or capacitive pre-attenuation approach in Fig. 3.1(d) allows handling of large input signals, but it needs to be combined with a high-gain mode LNA for implementing a dual-mode operation. The current steering and splitting approaches in Fig. 3.1(e) and $3.1(\mathrm{f})$, respectively, could provide consistent input matching because of the fixed $g_{m}$ of the input transistor, but they would not provide a wide linearity tuning range due to the fixed $g_{m}$. The multiplexing approach in Fig. 3.1(g) is attractive because its by-pass and high-gain paths can be used for high-linearity and high-gain mode operations, respectively. However, the use of a high-frequency multiplexer increases


Fig. 3.1. Prior multi-/dual-mode LNA designs. (a) Two independent gain paths, (b) Variable $g_{m}$, (c) Variable load impedance, (d) Resistive and capacitive pre-attenuation, (e) Current steering, (f) Current splitting, and (g) Multiplexing gain paths.
design complexity and input matching for large input signals still needs to be properly addressed.

As discussed, the existing approaches demand area overhead, waste in power, or increase in design complexity. Besides the area, power, and complexity issues, input matching for large input signals and forgiveness for the errors in mode-transition point estimation need to be properly addressed for a successful implementation of a dual-mode LNA that can toggle between high-gain and high-linearity modes.

### 3.2 Narrowband Dual-Mode LNA



Fig. 3.2. Proposed narrowband LNA schematic.

Since fine gain tuning can be efficiently achieved using a variable gain amplifier placed after a mixer, we focus on improving dynamic range for the proposed dualmode approach. One of the best ways to improve the upper bound of the input power range is using a passive divider that reduces the signal amplitude to below the dynamic range limit of the following stage. For the narrowband design, we combine the inductively source degenerated topology [67] with a capacitive divider as shown

Table 3.1
Component parameters of the narrowband LNA

| Transistor | Dimension | Component | Value |
| :---: | :---: | :---: | :---: |
| M1 | $204 \mu \mathrm{~m} / 0.13 \mu \mathrm{~m}$ | $L_{G}$ | 2.12 nH |
| M2 | $51 \mu \mathrm{~m} / 0.13 \mu \mathrm{~m}$ | $L_{L}$ | 2.67 nH |
| M3 | $51 \mu \mathrm{~m} / 0.13 \mu \mathrm{~m}$ | $L_{S}$ | 0.63 nH |
| M4 | $102 \mu \mathrm{~m} / 0.13 \mu \mathrm{~m}$ | $C 1$ | 26.2 fF |
| M5 | $102 \mu \mathrm{~m} / 0.13 \mu \mathrm{~m}$ | $C 2$ | 2.26 pF |

in Fig. 3.2. Device dimensions and component values are shown in Table 3.1. The capacitive divider $(C 1$ and $C 2)$ is placed between the gate inductor $\left(L_{G}\right)$ and the gate of the input transistor (M1) to minimize its impact on the input matching and NF during high-gain mode operation. For the high-gain mode, Vcont is set to 0 V to turn off M3 and M5. Vcontb is the inverted signal of Vcont. Therefore, the circuit works as a typical inductively source degenerated LNA while the effect of the capacitive divider is minimal because of its small effective capacitance value ( $<26.2 \mathrm{fF}$ in the proposed design). The sizes of $L_{G}$ and $L_{S}$ are adjusted to partially compensate for the effect of $C 1$ and $C 2$. The additional capacitive divider degrades the S21, S11, and NF of high-gain mode only by $0.1 \mathrm{~dB}, 1.6 \mathrm{~dB}$ and 0.04 dB , respectively, at 5.1 GHz. M6 works as a buffer in source follower configuration, driving external $50-\Omega$ test equipments.

For high-linearity mode, Vcont is set to VDD (1.2 V). The input stage consisting of $L_{G}, L_{S}$, M1, and M3 does not provide signal amplification anymore, but provides the desired narrowband input impedance matching that reflects out-of-band signals. The input signal is attenuated by the capacitive divider, and the cascoded common source stage (M4 and M5) operates as a transconductor, delivering the attenuated signal to the output load. The size of M3 is matched to that of M2, so the DC current through M1, and hence $g_{m}$ of M1, are consistent for the two operation modes. This
allows reliable narrowband input impedance matching for the two modes since the input impedance is approximately $g_{m 1} L_{S} / C_{g s 1}$, where $g_{m 1}$ and $C_{g s 1}$ are the transconductance and the gate-to-source capacitance of M1, respectively. In fact, since the LC-tank load ( $L_{L}$ and $C_{L}$ ) affects the small-signal input impedance in both the real and the imaginary parts, through $C_{g d}$ of M1, the high-linearity mode with zero load impedance at the drain of M3 can provide better small-signal input matching as shown in Fig. 3.3.

Fig. 3.3 also shows the input impedance ( S 11 ) variation at 5.1 GHz with increasing input signal power. For the wide dynamic range up to 0 dBm , the inductively source degeneration topology maintains the good input matching in both high-gain and high-linearity modes. When input power increases over -10 dBm , the real input impedance decreases as shown in Fig. 3.3(a). In this topology, the input impedance is approximately equal to [67]

$$
\begin{equation*}
Z_{i n} \approx s\left(L_{s}+L_{g}\right)+\frac{1}{s C_{g s}}+\frac{g_{m} L_{s}}{C_{g s}} \tag{3.1}
\end{equation*}
$$

Thus the real impedance is created by the $g_{m}$ of the input transistor. However, it cannot be considered to be constant over a large voltage swing and is a function of a time-varying gate-to-source voltage by the input signal. The effective $g_{m}$ for large signals is obtained as the RMS value of instant $g_{m}[68,69]$. As an input signal increases, non-linear behaviors of the transistor such as subthreshold and triode operations decrease the increment of the drain current with respect to the gate-to-source voltage and it causes the reduction of the effective $g_{m}$ and the real impedance. As depicted in Fig. 3.3(b), with increasing input power, the input matching starts to degrade at around -15 to -10 dBm of input power for both modes. For high-linearity mode, S11 is less than -10 dB up to 1.2 dBm of input power.

The size of M4 (M5) was selected for the best linearity of the common source stage during high-linearity mode operation. From simulation, a width of $102 \mu \mathrm{~m}$ provides the highest IIP3 under the given gate bias voltage.


Fig. 3.3. Simulated input matching vs. input power of the narrowband LNA at 5.1 GHz (HG: high-gain, HL: high-linearity).

### 3.3 Wideband Dual-Mode LNA

Wideband LNAs are finding more applications in multi-band and multi-standard systems. Thus, an LNA for multi-bands and multi-standards needs to provide a wide dynamic range as well as a wideband input matching, gain, and NF. The dual-
mode design approach is applied to a resistive feedback based wideband LNA. Fig. 3.4 shows two versions of the proposed wideband LNA: cascode design and single transistor design. The cascode design is more suitable for a high supply voltage. When a low supply voltage is required for a scaled technology, the IIP3 of the cascode design can be worsened in high-gain mode because of the $g_{d s}$ non-linearity of M2 in Fig. 3.4(a). In order to design in 45 nm SOI CMOS technology which recommends the maximum supply voltage of 1.1 V , the single transistor design in Fig. 3.4(b) was adopted and implemented. Table 3.2 summarizes the device dimensions. For high-gain mode operation, Vcont, H_Atn, L_Atn, and Iref are set to $0 \mathrm{~V}, 0 \mathrm{~V}, 0 \mathrm{~V}$, and $130 \mu \mathrm{~A}$, respectively. Vcontb is the inverted signal of Vcont. M1 and M2 work as a transconductor with a resistive load. The output impedances of M1 and M2 form the load impedance. The resistive feedback using $R_{F}$ provides a wideband input matching.

For high-linearity and low-attenuation (HL(LA)) operation, Vcont, L_Atn, H_Atn, and Iref are set to $\mathrm{VDD}(1.1 \mathrm{~V}), \mathrm{VDD}, 0 \mathrm{~V}$, and 0 A , respectively, turning off M1, M 2 , M4 and turning on M3. In high-linearity mode, $R_{F}$ and M3 work as a voltage divider. Because $R_{F}$ and the on-resistance of M3 are set to be much bigger than the source impedance ( $50 \Omega$ ), the $R_{M}$ and M5 combination, connected in shunt to the signal path, provides a wideband input matching. The on-resistance of M5 can be adjusted to $50 \Omega$ to provide the desired wideband input matching without using $R_{M}$, but the drain-body junction can enter forward bias region with large input signals. For this reason, $R_{M}$ is added and set to $20 \Omega$ to prevent the forward biasing condition with large input signals. $R_{M}$ also improves the input matching by partially shielding the junction capacitance of M5. When even higher attenuation is required, M4 can be turned on by setting H_Atn to VDD for high-linearity and high-attenuation (HL(HA)) operation. The passive voltage division allows a low-power in high-linearity mode, and a highly linear operation producing almost negligible third-order intermodulation until the input signal amplitude reaches the threshold voltages ( $V_{t h 1}$ and $V_{t h 2}$ ) of M1 and M2. For input signals with amplitudes larger than $V_{t h 1}$ or $\left|V_{t h 2}\right|$, M1 or


Fig. 3.4. Proposed wideband LNA schematic. (a) Cascode design (concept) and (b) Single transistor design (implemented).

M2 works as a class-C amplifier, producing intermodulation and degrading linearity. Mb6 is added to prevent this undesirable class-C amplification. Since Mb6 is off

Table 3.2
Component parameters of the wideband LNA

| Transistor | Dimension | Component | Value |
| :---: | :---: | :---: | :---: |
| M1 | $38.8 \mu \mathrm{~m} / 56 \mathrm{~nm}$ | $R_{F}$ | $515 \Omega$ |
| M2 | $48 \mu \mathrm{~m} / 56 \mathrm{~nm}$ | $R_{M}$ | $20 \Omega$ |
| M3 | $2 \mu \mathrm{~m} / 56 \mathrm{~nm}$ | $C_{F}$ | 0.8 pF |
| M4 | $10 \mu \mathrm{~m} / 56 \mathrm{~nm}$ | $C 1$ | 1 pF |
| M5 | $9 \mu \mathrm{~m} / 56 \mathrm{~nm}$ | $C 2$ | 1 pF |

during the high-linearity mode operation, no branch current is available for the classC amplification of M1 and M2. The effect of the parasitic of $R_{M}$, M3, M4, and M5 on high-gain mode operation is almost negligible from 0.8 to 6 GHz . Simulation shows that the parasitic degrades the $\mathrm{S} 21, \mathrm{~S} 11$, and NF of high-gain mode only by 0.1 dB , 0.15 dB , and 0.02 dB , respectively, at 6 GHz .

Fig. 3.5 shows the simulated S 11 at 2 GHz in the face of different input power levels. The S11 from 0.8 to 6 GHz with varying input power levels also exhibits a similar result. For small input signals, the high-linearity mode shows much better S11 because of its simple matching using a shunt resistive network. The small signal input impedance $\left(Z_{i n}\right)$ of the LNA in high-gain mode is approximately

$$
\begin{equation*}
Z_{i n} \approx \frac{R_{F}+R_{L}}{1+A_{v}} \| \frac{1}{s C_{g s}} \tag{3.2}
\end{equation*}
$$

where $A_{v}$ is the voltage gain, $R_{F}$ is the feedback resistance, $R_{L}$ is the load resistance, and $C_{g s}$ is the total gate-source capacitance of the input transistors. In this design, $R_{L} \approx r_{o 1} \| r_{o 2}$, where $r_{o 1}$ and $r_{o 2}$ are the output resistances of M1 and M2, respectively. Equation (3.2) shows that $Z_{i n}$ is a complex function of the input transistor size, voltage gain, load resistance, and feedback resistance, compared with the highlinearity case. With increasing input signal power, the input impedance starts to deviate from its small-signal value because $A_{v}$ starts to saturate and the effective $C_{g s}$ across the input voltage swing range starts to deviate from the small signal $C_{g s}$. The


Fig. 3.5. Simulated input matching vs. input power of the wideband LNA at 2 GHz .
simulated S 11 becomes worse than -10 dB at above -13 dBm of input power. For highlinearity mode, the input matching deteriorates with increasing input power because of the voltage dependent on-resistance of M5. We note that the effective gate-source capacitances of M1 and M2 are not sensitive to the input signal amplitude because
the current through the branch is zero. The S 11 becomes worse than -10 dB at above 7.5 dBm of input power, which is 20.5 dB larger than that of high-gain mode.

### 3.4 Experimental Results

### 3.4.1 Narrowband dual-mode LNA



Fig. 3.6. Chip microphotograph of the narrowband LNA.

The narrowband LNA was implemented in $0.13 \mu \mathrm{~m}$ CMOS technology, and Fig. 7 shows a chip microphotograph. The LNA core area is $550 \times 880 \mu m^{2}$ and the total area including test pads is $815 \times 1015 \mu \mathrm{~m}^{2}$. The LNA draws 3.2 mA and 4.9 mA from a 1.2 V voltage supply in high-gain and high-linearity modes, respectively. Fig. 3.7 shows the measured and simulated S 21 and S 11 with -40 dBm of input power. For high-gain mode, the measured S 21 and S 11 at 5.1 GHz are 15.4 dB and -7.6 dB , respectively. The corresponding numbers for high-linearity mode are -9 dB and -20 dB , respectively. As expected, the high-linearity mode shows a narrowband input matching characteristic. Fig. 3.8 shows the measured S 11 at 5.1 GHz in the face of


Fig. 3.7. Measured and simulated S-parameters of the narrowband LNA with -40 dBm input. (a) S21 and (b) S11.
different input power levels. Compared with the simulation results shown in Fig. 4, the measurement results show a slight offset, mostly because of the errors introduced in parasitic extraction, but show a good agreement in the trend over the input power range. The measured S 11 for high-linearity mode stays below -10 dB up to 5 dBm of input power. The measured NF is 2.9 dB and 25.7 dB at 5.1 GHz for the two modes, respectively, as shown in Fig. 3.9. IIP3 measurements used a two-tone signal with


Fig. 3.8. Measured S11 vs. input power of the narrowband LNA at 5.1 GHz.


Fig. 3.9. Measured and simulated noise figure of the narrowband LNA.
5.1 GHz and 5.105 GHz components, and, as shown in Fig. 3.10, the measured IIP3 are -7.3 dBm for high-gain mode, and +5.6 dBm for high-linearity mode. Fig. 3.11 shows the measured input-referred $\mathrm{P} 1 \mathrm{~dB} ;-18.3 \mathrm{dBm}$ and -1.8 dBm in high-gain and high-linearity modes, respectively.

Table 3.3 shows comparison with published multiple-mode or highly-linear LNAs for narrowband applications. The proposed narrowband LNA achieves a low NF in

Table 3.3
Narrowband LNA performance summary and comparison

|  |  | Frequency $(\mathrm{GHz})$ | Gain (dB) | $\begin{aligned} & \mathrm{S} 11 \\ & (\mathrm{~dB}) \end{aligned}$ | $\begin{gathered} \mathrm{NF} \\ (\mathrm{~dB}) \end{gathered}$ | P1dB (dBm) | $\begin{gathered} \text { IIP3 } \\ (\mathrm{dBm}) \end{gathered}$ | $\begin{aligned} & \text { Power } \\ & (\mathrm{mW})^{1} \end{aligned}$ | Supply <br> (V) | CMOS <br> Tech. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| This work | HG | 5.1 | 15.4 | -7.6 | 2.9 | -18.3 | -7.3 | 3.8 | 1.2 | $0.13 \mu \mathrm{~m}$ |
|  | HL |  | -9 | -20 | 25.7 | -1.8 | 5.6 | 5.9 |  |  |
| [40] | HG | 5.65~5.85 | 21.4 | $<-7$ | 4.4 | n/a | -18.5 | 16.2 | 1.8 | $0.18 \mu \mathrm{~m}$ |
|  | HL |  | 10.8 |  | 6.2 | n/a | -6.5 |  |  |  |
| $[41]^{2}$ | HG | $2.0 \sim 3.5$ | 23.8~26.2 | <-10 | 2.6~2.96 | -18 | -8 | 10.08 | 1.8 | $0.18 \mu \mathrm{~m}$ |
|  | HL |  | 10.2~12.5 | <-7.5 | 6.7~8.58 | -10 | n/a | 10.8 |  |  |
| $[43]^{2}$ | HG | $0.47 \sim 0.87$ | 16 | <-11 | 4.3 | n/a | -1.5 | 22 | 1.8 | $0.18 \mu \mathrm{~m}$ |
|  | HL |  | -17 |  | 35 | n/a | 27 |  |  |  |
| [31] |  | 2.5 | 12 | -16 | 3.5 | -5 | 5 | 19.8 | 1.8 | 32 nm |
| [32] |  | 2.1 | 5.2 | -14 | 3.0 | n/a | 10.5 | 12.6 | 1.2 | $0.13 \mu \mathrm{~m}$ |
| [33] |  | 2.2 | 8.4 | -13 | 1.92 | n/a | -2.55 | 16.2 | 1.8 | $0.35 \mu \mathrm{~m}$ |

1: Power consumption of output buffer for testing is excluded
2: Medium gain level not shown


Fig. 3.10. Measured IIP3 of the narrowband LNA. (a) High-gain mode and (b) High-linearity mode.
high-gain mode and high P1dB and IIP3 in high-linearity mode while consuming low power.


Fig. 3.11. Measured input-referred P1dB of the narrowband LNA.


Fig. 3.12. Chip microphotograph of the wideband LNA.

### 3.4.2 Wideband dual-mode LNA

The wideband LNA was implemented in 45 nm digital SOI CMOS technology, and Fig. 3.12 shows a chip microphotograph. Its area excluding test pads and decoupling capacitors is only $150 \times 100 \mu \mathrm{~m}^{2}$. The LNA core including the bias circuitry draws 5.6 mA from a 1.1 V voltage supply in high-gain mode, and does not consume power in high-linearity mode. Fig. 3.13(a) shows the measured and simulated S21. The


Fig. 3.13. Measured (solid lines) and simulated (dashed lines) Sparameters of the wideband LNA with -30 dBm input. (a) S21 and (b) S11.
measured S21 in high-gain mode ranges from 9.4 to 7.0 dB over the target frequency range ( 0.8 to 6 GHz ). Fig. 3.13(b) shows the measured and simulated S11 with -30 dBm of input power. As expected, it shows a wideband input matching characteristic. Fig. 3.14 shows the S 11 versus input power curves measured at 2 GHz . The S11 starts to increase at around -15 dBm for high-gain mode and at around -10 dBm for


Fig. 3.14. Measured S11 vs. input power of the wideband LNA at 2 GHz .


Fig. 3.15. Measured (solid lines) and simulated (dashed lines) noise figure of the wideband LNA.
high-linearity modes, which agree well with the simulation results shown in Fig. 3.5. The measured S11 for high-linearity modes stay below -10 dB up to 8 dBm of input power. As seen in Fig. 3.15, the measured NF ranges from 3.0 to 3.6 dB over the target frequency range in high-gain mode. Since the gain is negative in high-linearity modes, the attenuation factor directly adds to the NF which ranges from 22.7 to 26.3


Fig. 3.16. Measured input-referred P1dB of the wideband LNA.


Fig. 3.17. Measured P1dB and IIP3 vs. frequency of the wideband LNA.
dB in high-linearity and low-attenuation (HL(LA)) mode, and ranges from 32.4 to 39.3 dB in high-linearity and high-attenuation (HL(HA)) mode.

The input-referred P 1 dB is measured at 1 GHz as shown in Fig. 3.16. The P1dB for HG, HL(LA), and HL(HA) modes are $-14.0 \mathrm{dBm},+2.7 \mathrm{dBm}$, and +4.2 dBm , respectively. It suggests that the operation mode can be switched from HG to HL(LA) when the input signal power gets close to -14.0 dBm . Because the mode-

| $\begin{array}{lll} \text { EVM: } & 0.44 \% \text { RMS } \\ & 1.62 \% \quad \text { Peak @ sym } 9 \end{array}$ |  |  |  |
| :---: | :---: | :---: | :---: |
| $\begin{array}{ll}\text { Mag Err: } & \begin{array}{l}0.29 \% \\ \\ 1.31 \%\end{array} \quad \text { RMS } \\ & 0.3 \text { @ sym } 0\end{array}$ | $\begin{array}{r} 975 \\ \mathrm{~m} \end{array}$ |  |  |
| Phase Err: 0.3 deg RMS <br>  1.28 deg Peak @ sym 14 |  |  |  |
| Rho: 0.5212 |  |  |  |
| Length: 162 symbols |  |  |  |
| Freq Err: 1.101 kHz |  |  |  |
| Origin Offset: -54.92 dB | $\begin{array}{r} -975 \\ \mathrm{~m} \end{array}$ |  |  |
| Scale: $8.021 \mathrm{mV} /$ Unit |  |  | 1.454 |

(a)

(b)

(c)

(d)

Fig. 3.18. EVM measurement results of the wideband LNA. (a) HG, input power $=-40 \mathrm{dBm}$, (b) HG, input power $=-5 \mathrm{dBm}$, (c) HL(LA), input power $=-5 \mathrm{dBm}$, and (d) Input power vs. EVM.
transition relies on signal power sensing, and because power sensing inevitably incurs errors, the acceptable mode-transition power range needs to be wide enough to forgive the errors in the transition point estimation based on power sensing. This issue will be further discussed based on EVM measurements.

A $50-\mathrm{MHz}$ spaced two-tone signal is used for the IIP3 measurements, and the measured IIP3 ranges from -5.0 to -2.4 dBm over the target frequency band in highgain mode as shown in Fig. 3.17. In high-linearity modes, the circuit works as a passive divider, and no third-order intermodulation signal bigger than the noise floor $(-90 \mathrm{dBm})$ of the test equipment was observed with the input power up to 8 dBm . Due to this, we could not measure IIP3 for high-linearity modes. We stopped the measurement at 8 dBm of input power because the peak voltage across the input transistor at 8 dBm is higher than the operating voltage limit $\left(1.15 \mathrm{~V}\right.$ at $\left.105^{\circ} \mathrm{C}\right)$ posed by hot-carrier effects of the technology.

To demonstrate the forgiveness for the mode-transition point estimation error, we conducted EVM measurements, shown in Fig. 3.18. An Agilent E4433B signal generator produced 16-QAM modulated signals at 1 GHz and a Tektronix RSA3408A spectrum analyzer was used as a demodulator. A typical upper bound of EVM for a 16-QAM receiver for a bit error rate compliance of $5 \times 10^{-4}$ is $12 \%$ [73]. For enough margin and for a quantitative example, we use a conservative number, $5 \%$, for the LNA. As can be seen in Fig. 3.18(d), with increasing input power, the EVM of highgain mode starts to deteriorate at around -20 dBm , and its EVM becomes bigger than $5 \%$ at above -13.5 dBm which is close to the P1dB of high-gain mode. Based on the $5 \%$ EVM criteria, the LNA operation mode can change from HG to HL(LA) anywhere between -40 dBm and -13.5 dBm of the input power, which provides a 26.5 dB transition window. For the same reason, the LNA operation mode can change from $\mathrm{HL}(\mathrm{LA})$ to $\mathrm{HL}(\mathrm{HA})$ anywhere between -28 dBm and -2 dBm of the input power, providing a 26 dB transition window. The wide mode-transition windows would allow reliable mode-transitions based on a measured signal power using a crude power sensing. Also, the EVM for $\mathrm{HL}(\mathrm{HA})$ mode stays below $5 \%$ up to 8 dBm of

Table 3.4
Wideband LNA performance summary and comparison

|  |  | Frequency <br> (GHz) | Gain (dB) | $\begin{aligned} & \mathrm{S} 11 \\ & (\mathrm{~dB}) \end{aligned}$ | $\begin{gathered} \mathrm{NF} \\ (\mathrm{~dB}) \end{gathered}$ | P1dB (dBm) | IIP3 (dBm) | Power $(\mathrm{mW})^{1}$ | Supply <br> (V) | CMOS <br> Tech. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| This work | HG | $0.8 \sim 6$ | $9.4 \sim 7.0$ | $<-10$ | $3.0 \sim 3.6$ | -14.0 | $>-5$ | 6.2 | 1.1 | 45 nm |
|  | HL(LA) |  | -19.9~-19.3 | $<-19.8$ | $22.7 \sim 26.3$ | 2.7 | $>8^{2}$ | 0 |  |  |
|  | HL(HA) |  | -33.0~-32.4 | $<-23.4$ | $32.4 \sim 39.3$ | 4.2 |  |  |  |  |
| $[47] \mathrm{LB}^{3,4}$ | HG | 0.5,1.0,2.0 | 23,22.5,21.5 | <-15 | 4,2.8,2.7 | $\mathrm{n} / \mathrm{a}$ | $\mathrm{n} / \mathrm{a}$ | $29 \sim 31^{5}$ | 1.2 | 90 nm |
|  | HL |  | $0 \sim 5$ | $\mathrm{n} / \mathrm{a}$ | $\mathrm{n} / \mathrm{a}$ | -3.3,-2.5,-2.9 | 8.6,7,9.4 | $12 \sim 14^{6}$ |  |  |
| [47] $\mathrm{HB}^{3,4}$ | HG | 3.0,4.5,6.0 | 14.5,14.2,12 | $<-9.6$ | 2.8,2.7,3.9 | $\mathrm{n} / \mathrm{a}$ | $\mathrm{n} / \mathrm{a}$ | $30.2 \sim 32.2^{5}$ |  |  |
|  | HL |  | $0 \sim 5$ | $\mathrm{n} / \mathrm{a}$ | $\mathrm{n} / \mathrm{a}$ | -5,-3,-2.4 | 10.5,7.5,7.8 | $12 \sim 14^{6}$ |  |  |
| [70] |  | $0.2 \sim 5.2$ | $4 \sim 6.6{ }^{7}$ | <-10 | <3.5 | $\mathrm{n} / \mathrm{a}$ | $>0$ | 14 | 1.2 | 65 nm |
| [71] |  | $0.5 \sim 7$ | $12 \sim 15$ | $<-7.5$ | $2.3 \sim 2.9$ | $\mathrm{n} / \mathrm{a}$ | $-2.3{ }^{8}$ | 12 | 1.8 | 90 nm |
|  |  | $-8.8{ }^{9}$ |  |  |  |  |  |  |  |  |
| [72] |  |  | $3 \sim 8$ | $10.8 \sim 16.4$ | $<-10$ | $2.9 \sim 4.66$ | $\mathrm{n} / \mathrm{a}$ | -4.3~-2.2 | 3.9 | 1.8 | $0.18 \mu \mathrm{~m}$ |

1: Power consumption of output buffer for testing is excluded
2: 3rd-order intermodulation was not measured until the maximum applied input power of 8 dBm
3: Medium gain level not shown
4: LB and HB is a low-band and a high-band LNA, respectively
5: Power consumption of LNA and multiplexer
6: Power consumption of multiplexer
7: Single input to differential output
8: At $0.5 \mathrm{GHz}, 9$ : At 5.8 GHz
input power, which is bigger than the measured $\mathrm{P} 1 \mathrm{~dB}(4.2 \mathrm{dBm})$. This demonstrates that the upper bound of input dynamic range of the proposed topology, ignoring in-band interferers, is essentially determined by the maximum operating voltage of the technology limited by hot-carrier effects. Based on the $5 \%$ EVM criteria, the lower bound of input dynamic range is -69 dBm , which can be further improved by enhancing the baseband signal processing gain. Due to the limitation in the operating frequency of the available test equipment, similar measurements could not be performed at higher frequencies.

Table 3.4 compares the proposed wideband LNA with published multiple-mode or highly-linear LNAs for wideband applications up to higher than 5 GHz . The proposed design provides a low NF while consuming low power in high-gain mode, and provides a high power handling capacity and negligible intermodulation while consuming no power in high-linearity mode.

### 3.5 Conclusion

We presented a narrowband and a wideband LNA using a dual-mode design approach that provides wide dynamic range and low power consumption. The two modes, high-gain and high-linearity, can be digitally selected, and share components, minimizing the inter-loading between the two modes and alleviating the performance degradation at high frequencies caused by parasitic. The proposed designs provide good input impedance matching for small and large signals alike, and improve the power handling capacity by passive attenuation, which produces almost negligible intermodulation. In the narrowband design, the additional circuitry for signal attenuation was effectively integrated into the inductively source degenerated topology with a negligible effect on high-gain mode operation while achieving high P1dB and IIP3 in high-linearity mode. For the wideband design, the P1dB and EVM measurement results demonstrate that the upper bound of the input dynamic range is limited by the maximum voltage across transistors, which is determined by hot-carrier ef-
fects, not by the nonlinear transconductance of the input transistor. The comparison with existing works demonstrates the effectiveness of the proposed dual-mode design approach for achieving low power and wide dynamic range. Also, the measured wide mode control window ( $>26 \mathrm{~dB}$ ) of the wideband LNA shows the feasibility of a reliable mode control using a crude power sensing.

## 4. SUMMARY AND CONCLUSION

The semiconductor industry in the field of wireless communications has grown rapidly and the advancement of CMOS technology has been a major momentum in the development. While CMOS scaling has brought low cost, high performance, and high integration density, it also accompanies large variability to PVT variations and limited linearity on RF and analog circuit design. To achieve reliable performance of RF circuits in deeply-scaled technologies, wireless communication systems include a lot of calibration and mode-selection circuitries, which are adopted a digital-friendly manner. As proposed are design techniques to overcome such issues in phase shifters and LNAs with a digitally-assisted method, the self-calibration system for RF phase shifters and the wide dynamic range LNAs were presented.

With the proposed self-calibration system, the 7 to 13 GHz phase shifter achieves the phase error of less than $2^{\circ}$. In this work, several unique design methodologies are developed, which are phase amplification technique, signal generation by phase rotator, PVT-tolerant pulsewidth-to-digital converter, and digital controller with lesser complexity. The proposed phase amplification is a powerful technique in measuring phase or time difference with high accuracy, especially for high-frequency circuits. This technique can be applied to many other applications such as DLL, PSK modulator, and I/Q calibration. The 8-bit dual-slope integrating TDC provides many benefits comparing previous TDC designs. It offers robustness to PVT variation, high accuracy, low power, built-in averaging function, high resolution, and wide input dynamic range. The devised algorithm and digital controller can be also shared with other calibration circuitries in a system and hence, it can be used for local and global calibration.

To enhance the power handling capacity of LNAs, an LNA can be designed to support multiple modes. However, the parasitic effect by added circuits would limit
the high-frequency performance of an LNA. The presented narrowband (5.1GHz) and wideband ( 0.8 to 6 GHz ) LNAs effectively share the circuit components between highgain and high-linearity modes, and thereby, the inter-loading between the two modes is minimized. As a result, their high-frequency performance is negligibly degraded in high-gain mode achieving low power consumption. In addition, this research fully explores the following issues, which have not been properly addressed: input impedance matching with large input signals and tolerance to input power sensing error. The S11 of the narrowband LNA is less than -10 dB up to 5 dBm of input power in highlinearity mode, and the S 11 of the wideband LNA stays below -10 dB up to 8 dBm of input power in high-linearity mode. In addition, with the EVM test, the wideband LNA shows the wide mode-control window of more than 26 dB , and this enables reliable mode control even with power sensing error. Finally, the narrowband and the wideband LNA achieves the input-referred P 1 dB of -1.8 dBm and +4.2 dBm , respectively.

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APPENDIX

## A. VERILOG SCRIPTS

1. Synthesis_top: Top module synthesized with ARM standard cells
```
module Synthesis_top (I_synth, Q_synth, SW_synth, XOR_en_synth,
    count_en_synth, clk, rst, SPI_clk, SPI_data, SPI_load,
    TDC_done, count, load, tdc, loop_hault_synth, calib_comp);
    input count;
    input SPI_data;
    input SPI_load;
    input clk;
    input [7:0] tdc;
    input rst;
    input TDC_done;
    input SPI_clk;
    input load;
    output [4:1] SW_synth;
    output count_en_synth;
    output [7:0] I_synth;
    output XOR_en_synth;
    output [7:0] Q_synth;
    output loop_hault_synth;
    output calib_comp;
    wire [3:0] I_ext,Q_ext;
    wire [3:2] S_ext;
    wire [7:0] Preset;
    wire [23:0] loop_set;
    wire loop_hault_synth_w;
SPI_top U1(
    clk(clk),
    clk_SPI(SPI_clk),
    data(SPI_data),
    load(SPI_load),
    I(I_ext),
    Q(Q_ext),
    Preset(Preset),
```

```
    S(S_ext),
    loop_set(loop_set)
    );
Control_block U2(
    rst(rst),
    DI(I_synth),
    DQ(Q_synth),
    I_ext(I_ext),
    Q_ext(Q_ext),
    preset(Preset),
    tdc(tdc),
    load(load),
    clk(clk),
    count(count),
    s(S_ext),
    sw(SW_synth),
    TDC_done(TDC_done),
    calib_comp(calib_comp)
    );
TDC_control U3(
    XOR_en(XOR_en_synth),
    clk(clk),
    TDC_done(TDC_done),
    count_en(count_en_synth),
    rst(loop_hault_synth_w)
    );
TDC_wait U4(
    clk(clk),
    count_done(TDC_done),
    rst(rst),
    wait_cycle(loop_set),
    wait_out(loop_hault_synth_w)
    );
```

assign loop_hault_synth=loop_hault_synth_w;
endmodule
2. SPI_top
// The 8-MSB-bits are data and 3-LSB-bits are control
// Data is moved everywhere at rising edge of clock and load

```
|// control = 000 : Do Nothing
// control = 001 : MSB }->\mathrm{ LSB = [4-bit I, 4-bit Q]
// control = 010: MSB }-> LSB=[8-bit Preset]
// control = 011 : MSB -> LSB = [2-bit S, XXXXXX]
// control = 100 : MSB }->\mathrm{ LSSB = [23:16] of wait counter
// control = 101 : MSB }->\mathrm{ LSB = [15:8] of wait counter
// control = 110 : Do Nothing
// control = 111 : Do Nothing
// SPI module must not have any reset pin for reg
module SPI_top (clk, clk_SPI, data, load, I, Q, Preset, S,
    loop_set);
    input clk, clk_SPI, data, load;
    output reg [7:0] Preset;
    output reg [23:0] loop_set;
    output reg [3:0] I,Q;
    output reg [3:2] S;
    reg [10:0] SPI_reg;
    reg load_r, clk_SPI_r;
always @ (posedge clk)
begin
    if (load && !load_r)
    begin
        case(SPI_reg[2:0])
        3'b001: begin
            I[3:0]<= SPI_reg[10:7];
            Q[3:0]<= SPI_reg[6:3];
        end
        3'b010 : begin
            Preset[7:0] <= SPI_reg[10:3];
        end
        3'b011:begin
            S[3:2]<= SPI_reg[10:9];
        end
        3'b100:begin
            loop_set[23:16]<= SPI_reg[10:3];
```

```
            end
        3'b101:begin
                loop_set[15:8]<= SPI_reg[10:3];
                loop_set[7:0]<= 8'b0;
        end
        default:begin
        end
        endcase
    end
end
always@(posedge clk)
begin
    if (clk_SPI && !clk_SPI_r)
    begin
        SPI_reg[10:0]}<={\mathrm{ SPI_reg [9:0], data };
    end
end
always @ (posedge clk)
begin
    clk_SPI_r <= clk_SPI;
    load_r <= load;
end
endmodule
```


## 3. Control_block

```
module Control_block (rst, DI, DQ, I_ext, Q_ext, preset, tdc,
```

    load, clk, count, s, sw, TDC_done, calib_comp);
        input [3:0] I_ext, Q_ext;
        input [3:2] s;
        input [7:0] preset, tdc;
        input rst,load, count, clk, TDC_done;
    output [7:0] DI, DQ;
    output reg [4:1] sw;
    output reg calib_comp;
    reg [7:0] DI_reg, DQ_reg, tdc_reg, counter;
    ```
    reg [8:0] counterreg;
    reg TDC_update;
// Loading I and Q to 8-bit registers
always @ (posedge clk or posedge rst)
begin
    if (rst)
    begin
        counterreg[8:0] <= 9'b0;
        DI_reg[7:0] <= 8'b0;
        DQ_reg[7:0] <= 8'b0;
        TDC_update <= 1'b1;
        calib_comp <= 1'b0;
    end
    else
    begin
        if (!load && !count) // Load=0, Count=0;
        begin
            if (s [2])
                begin
                    counterreg[8] <= 1'b0;
                    counterreg[7:4] <= DI_reg[7:4];
                    counterreg[3:0] <= 4'b0;
                end
                else
                begin
                    counterreg[8] <= 1'b0;
                    counterreg[7:4]<= DQ_reg[7:4];
                    counterreg[3:0]<= 4'b0
            end
            end
            else if (load && !count) // Load=1, Count=0;
            begin
                DI_reg[7:4]<= I_ext[3:0];
                DI_reg[3:0] <= 4'b0;
                DQ_reg[7:4] <= Q_ext[3:0];
                DQ_reg[3:0] <= 4'b0;
                TDC_update <= 1'b0;
            end
            else if (!load && count && TDC_update && TDC_done) //
    Load=0, Count=1;
            begin
                if (s[2])
                    DI_reg <= counter;
```

```
        else
            DQ_reg <= counter;
        // Comparator
        if (tdc_reg < preset) // M<PS
        begin
            counterreg <= counterreg + 1'b1;
            calib_comp <= 1'b0;
        end
        else if (tdc_reg > preset) // M> PS
        begin
            counterreg <= counterreg - 1'b1;
            calib_comp <= 1'b0;
        end
        else calib_comp <= 1'b1; // M = PS
        TDC_update <= 1'b0; // TDC flag Low
        end
        else if (!TDC_done)
        begin
            TDC_update <= 1'b1;
        end
    end
end
// Counter logic for 90deg and 270deg
always @ (posedge clk or posedge rst)
begin
    if (rst)
    begin
        counter[7:0] <= 8'b0;
    end
    else
    begin
        if (counterreg[8])
            counter [7:0] <= ~ counterreg [7:0];
        else
            counter[7:0] <= counterreg [7:0];
    end
end
// Switches
always @ (posedge clk or posedge rst)
begin
```

```
    if (rst)
    begin
        sw[4:1]<= 4'b0;
    end
    else
    begin
        sw[2]<=s[3]^ s[2]^ counterreg[8];
        sw[1]<=(~(s[3])^s[2] ^ counterreg[8]);
        sw[3]<=(~s[3]);
        sw[4]<=s[3];
    end
end
// TDC logic
always @ (posedge clk or posedge rst)
begin
    if (rst)
    begin
        tdc_reg[7:0]<= 8'b0;
    end
    else
    begin
        if (s[3] ^ tdc[7])
            tdc_reg <= (~tdc) + 1'b1;
        else
            tdc_reg <= tdc;
    end
end
assign DI = DI_reg; assign DQ = DQ_reg;
endmodule
```

    4. TDC_control
    module TDC_control (XOR_en, clk, TDC_done, count_en, rst);
input clk, TDC_done, rst;
output reg count_en, XOR_en;
reg [7:0] count_reg;
always @ (posedge rst, posedge clk)
begin
if (rst)

```
    begin
    XOR_en <= 1'b1;
    count_en <= 1'b0;
    count_reg <= 8'b0;
    end
    else if (TDC_done)
    begin
        XOR_en <= 1'b1;
        count_en <= 1'b0;
        count_reg <= 8'b0;
    end
    else
    begin
        if(count_reg = 8'd255)
        begin
            XOR_en <= 1'b0;
            count_en <= 1'b1;
            count_reg <= 8'b0;
        end
        else
        begin
            count_reg <= count_reg + 1'b1;
    end
    end
end
endmodule
```

5. TDC_wait
module TDC_wait (clk, count_done, rst, wait_cycle, wait_out);
input clk, rst, count_done;
input [23:0] wait_cycle;
output reg wait_out;
reg count;
$\operatorname{reg}[23: 0]$ ctr_reg;
always @ (posedge clk or posedge rst)
begin
if (rst)
begin
ctr_reg $<=24^{\prime}$ b0;
count $<=1$ 'b1;
wait_out $<=1$ 'b1;
```
    end
    else
    begin
        if (ctr_reg= wait_cycle)
        begin
            wait_out <= 1'b0;
            ctr_reg <= 24'b0;
            count <= 1'b0;
        end
            else if (count=1'b1)
            begin
                    ctr_reg <= ctr_reg + 1'b1;
            wait_out < = 1'b1;
        end
        else
        begin
            if (count_done)
            count <= 1'b1;
        end
    end
end
endmodule
```

VITA

## VITA

Jang Joon Lee received his B.S. degree in electrical engineering from Korea University, Seoul, Korea, in 2004, and his M.S. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, in 2006. From 2006 to 2013, he worked to pursue his Ph.D. degree in electrical and computer engineering at Purdue University under the guidance of Prof. Byunghoo Jung. During summer and fall of 2008, he was an RF IC design intern at Qualcomm, San Diego, CA, where he designed an active TX leakage canceller for SAW-less advanced wireless receiver. In fall of 2009 and spring of 2010, he was a teaching assistant for the course of Electronic Devices and Design Laboratory, and he instructed two classes each semester. During the rest of the period, he was a research assistant at School of Electrical and Computer Engineering. His research interests include the design of RF and analog integrated circuits and the development of self-healing/calibration circuits for deeply-scaled technologies.

