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Developing Compact Models for Passive Devices on IBM 45nm CMOS SOI Technology

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ABSTRACT

The standard IBM 45 nm technology is widely adopted for industrial and academic purpose by integrates circuit designers. Original models provided by foundry are not accurate, which might cause inaccuracy in circuit simulations. Equivalent circuit models, using RLC elements to simulate electrical component, will effectively deliver their electrical performance. This study consists of four steps to construct these models. First, Cadence Virtuoso, the commercial circuit design software was used to run simulations and extract data for different device parameters. Second, analyzing tools, like Microsoft Excel or Matlab, are used to analyze the extracted data. Then, equations are written for each parameter. Finally, these models are implemented in the device descriptive language, Verilog-A and test circuits will be constructed to demonstrate the accuracy of the models. The accurate passive component models from this study will contribute to accelerating the circuit designing process and improving the accuracy of circuit simulations.

KEYWORDS

IBM, Simulation, Verilog-A, Circuit design

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