Void Detection in Dielectric Films Using a Floating Network of Substrate-Embedded Electrodes

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A sensor is developed for simple, in situ characterization of dielectric thermal interface materials (TIMs) at bond line thicknesses less than 100 μm. The working principle is based on the detection of regions of contrasting electric permittivity. An array of long, parallel electrodes is flush-mounted into each opposing substrate face of a narrow gap interface, and exposed to the gap formed between the two surfaces. Electrodes are oriented such that their lengthwise dimension in one substrate runs perpendicular to those in the other. A capacitance measurement taken between opposing electrodes is used to characterize the interface region in the vicinity of their crossing point (junction). The electric field associated with each electrode junction is numerically simulated and analyzed. Criteria are developed for the design of electrode junction geometries that localize the electric fields. The capacitances between floating-ground electrodes in the electrode sensor configuration employed give rise to a nontrivial network of interacting capacitances which strongly influence the measured response at any junction. A generalized solution for analyzing the floating network response is presented. The technique is used to experimentally detect thermal grease spots of 0.2 mm to 1.8 mm diameter within a 25 μm interface gap. It is necessary to use the generalized solution to the capacitance network developed in this work to properly delineate regions of contrasting permittivity in the interface gap region using capacitance measurements. [DOI: 10.1115/1.4028075]

Keywords: thermal interface, capacitance, impedance, thermal grease, TIM, nondestructive, tomography

1 Introduction

Within the thermal management architecture of modern electronic systems exist numerous component interfaces between chip, heat spreader, and heat sink layers, which often contribute a significant portion of the overall package thermal resistance. The medium used in these gaps must provide minimal thermal resistance uniformly across the entire interface for reliable performance. Dielectric TIMs are often employed in order to allow direct contact of the TIM with devices without risk of electrical interference, avoiding the need for intermediate passivation layers. Common problems encountered with TIMs include voiding, cracking, and pump-out during thermal cycling. The performance characterization of these materials is crucial to their optimized use in electronics applications. Many challenges confronted in the thermal management of modern electronics systems are discussed in Garimella et al. [1].

Various nonintrusive means have been used to characterize the quality of TIM layers, such as acoustic microscopy [2,3] and X-ray methods [3]. An infrared microscopy technique to characterize a TIM layer through a silicon wafer was demonstrated by Hu et al. [4]. Thermography techniques [5,6] may be used to characterize the transient thermal response of an interface, and thus infer the existence and location of voids. High-resolution methods, such as scanning electron microscopy [3], have also been applied to TIM layers. Although the above techniques provide microscale or nanoscale resolution, the necessary equipment, sample preparation, and expertise required for these methods may be prohibitive in many industrial applications.

For applications where millimeter-scale defect detection is sufficient, a TIM layer characterization methodology that compromises spatial resolution in return for ease of implementation is highly desirable. Islam et al. [7] conducted an experimental investigation showing that void fractions of 30% or higher may occur during thermal cycling of many common TIMs; nonintrusive millimeter-scale TIM void detection would be valuable in such cases. The technique developed in the present work is amenable to implementation in rapid in situ measurements during TIM compression and thermal cycling, creating a time-dependent map of the TIM layer.

A method for characterizing dielectric interfaces by means of a set of discrete capacitance measurements made over the interface area is proposed here. This map of capacitances is obtained using two sets of orthogonal electrode arrays embedded flush in the substrate on either side of the TIM layer. The electrode arrays form a rectangular grid of electrode junctions for capacitance measurement. The sensor creates a two-dimensional map of the interface based upon a series of individual measurements between pairs of opposing electrodes across the interface gap. In this work, the media filling the interface region is considered to have a binary distribution, where the dielectric constants of each phase (TIM and void) are known a priori. Void regions that are too small to bridge the interfacial gap are unlikely to be detected by the method. The problem formulation and boundary conditions for the current approach are fundamentally different from three-dimensional capacitance tomography where phases are reconstructed based on combinatorial actuation of multiple electrodes around the periphery.

The proposed sensor is instead similar to the wire-mesh concept first introduced by Prasser et al. [8], which utilized the electrical

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resistance at each crossing point of perpendicular wires to identify the local phase in a cross section of two-phase flow. Da Silva et al. [9] extended the technique to purely dielectric flows using the capacitance measured at each crossing point. In their wire mesh sensor, the wire electrodes were 0.12 mm in diameter, and spaced at a pitch of 3.12 mm. Wire mesh sensors can produce images of bubbles in real time through signal measurement at a higher frequency than the timescale of flow dynamics [9–11]. They have also proven useful for characterization of trickling flows in packed beds [12,13]. Comparisons to capacitance tomography applied to the cross section of 6.7 and 10 cm pipes [13,14] have demonstrated an advantage in spatial resolution with the wire mesh, for which the resolution corresponds to the electrode pitch. Paranjape et al. [15] demonstrated that bulk impedance could be used to characterize the void fraction of two-phase flow within a 0.78 mm square microchannel. With respect to thermal interfaces, capacitance has been used with a spectroscopy technique utilizing a single electrode to detect flaws in an insulating layer [16,17]. In this paper, the perpendicular-array wire mesh sensor concept is adapted for characterization of a dielectric TIM layer. This capacitance mapping technique presents a new method of in situ characterization to aid in void detection and the understanding of time-dependent TIM behavior.

2 Description of Sensing Approach

The proposed sensing device operates with a thermal interface surrounded by two nonconductive substrates. One of the substrates contains N long parallel electrodes that are polished flush with the surface facing the TIM. The second substrate contains M electrodes that are identical to the first set, but rotated such that the electrode arrays are turned at right angles to each other as shown in Fig. 1. The gap between the substrates is thus bounded on each side by a series of electrodes, with the electrode surfaces directly exposed to the TIM. The crossing points of pairs of perpendicular electrodes are hereafter referred to as junctions.

In this study, the configuration in Fig. 1 is investigated for the case where two materials of different dielectric constant fill the interface region. If the design conditions in this study are met, the capacitance measurement obtained by actuating any junction provides information about the junction region (i.e., of the region of the interface material contributing to the measured capacitance at that electrode junction). By measuring the capacitance at all junctions sequentially, the relative distribution of dielectric materials may be mapped, providing a means for void detection in real interfaces.

3 Single Junction Analysis

The behavior of the electric field at any given junction must be understood in order to characterize the behavior of the system. Electric field characteristics at the junction are investigated through numerical simulation. In the absence of physical charges within the gap, the field is governed by the simplified form of Gauss's Law,

$$\nabla \cdot E = 0 \tag{1}$$

where the electric field is given by

$$E = -\nabla\varphi \tag{2}$$

Thus, the distribution of electric potential is governed by the Laplace equation for electric potential

$$\Delta\varphi = 0 \tag{3}$$

The domain of interest consists of the volume defined by the height of the interface gap H, and length of electrodes in both directions L, as shown in Fig. 2. The underside of the top electrode and the top surface of the bottom electrode are illustrated as two-dimensional surfaces on the boundary of the domain.

The boundary conditions used in the simulation are shown in Fig. 2. The electrode surfaces are held at a constant voltage, while a zero flux condition is imposed on the surrounding boundaries. The volume is discretized with regularly spaced nodes throughout. Due to the extreme aspect ratio of the domain, the resolution of cells in the z direction dictates the mesh size required for grid independence. A grid-independence study indicated that six cells along the z direction are sufficient to resolve the voltage gradient through the gap. Meshes of between 25,000 and 600,000 cells were used for a one-quarter symmetry section of the domain. A sample case is illustrated in top view in Fig. 3. The surface of the top electrode in this one-quarter domain is shaded and corresponds to the contour plot of the electric field in Fig. 4.

After calculating the distribution of electric potential, the capacitance of the junction is calculated as an integral over the area of the top electrode as

$$C = \frac{\varepsilon}{V_1 - V_2} \iint \frac{\partial\varphi}{\partial z} dA \tag{4}$$

The electric field and capacitance per unit length are shown for the example geometry in Fig. 4. The capacitance is concentrated near the junction. The length of the localized region of the electric field, p_{min}, is defined as the length along the electrode wherein a chosen threshold of the total capacitance is obtained (see Fig. 3). In Fig. 4, a chosen threshold of 95% is indicated, signifying that 95% of capacitance (area under the curve) occurs to the left of this point.

A nondimensional characterization of an electrode pair may be used to correlate the capacitance value obtained from the geometry illustrated in Fig. 2 for any case. The distribution of capacitance over the electrode is a function of the total electrode length

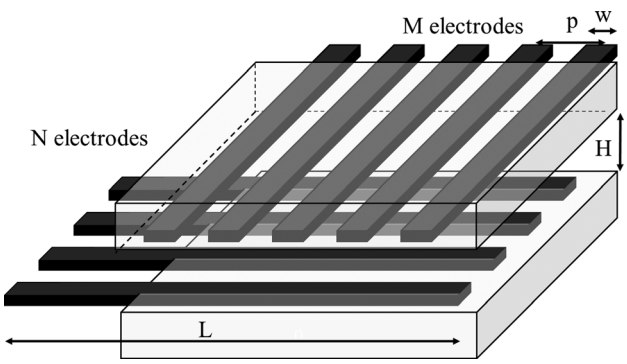

Fig. 1 Schematic diagram of proposed device configuration for characterization of dielectric interfaces

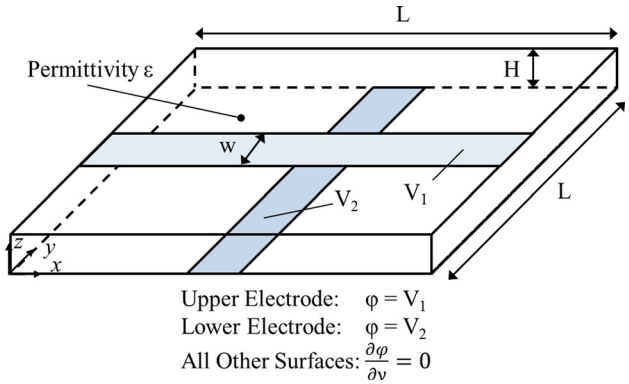

Fig. 2 Domain of interest for a single electrode pair, composed of the gap region between two substrates

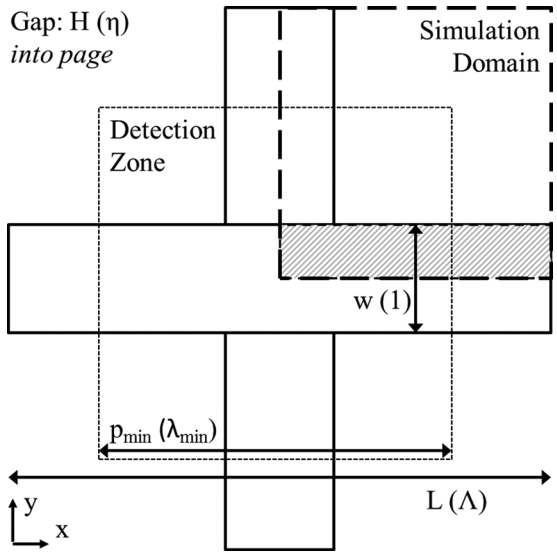

Fig. 3 Top view of domain of interest for sample case ($L = 5$ mm; $H = 0.25$ mm; $w = 1$ mm; $p_{min} = 3.37$ mm). The shaded region of the top electrode surface corresponds to the contour plot in Fig. 4.

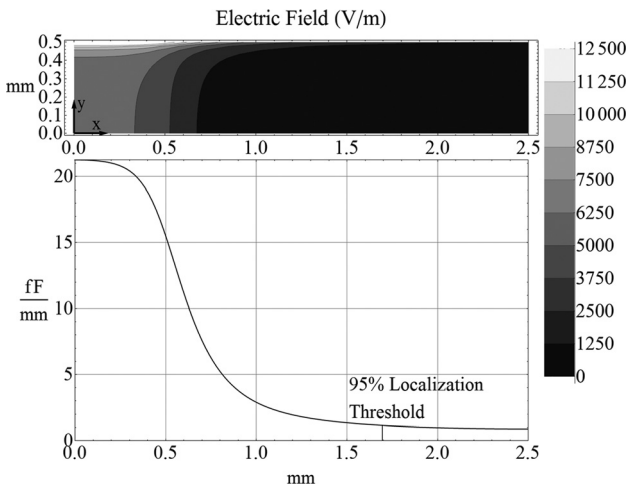

Fig. 4 Top: contour plot of electric field on the lower surface of the top electrode. The one-quarter domain is shown corresponding to the shaded region in Fig. 3. Bottom: dependence of capacitance along the electrode length.

L, the gap size H, the electrode width w, and the dielectric constant ε. Using the electrode width as the length scale, the dimensionless capacitance is given by

$$\frac{C}{\varepsilon w} = f(\eta, \Lambda) \tag{5}$$

where η and Λ stand for the dimensionless gap H/w, and the dimensionless electrode length L/w, respectively. As part of the investigation of electrode behavior for this study, simulations for various values of η and Λ were carried out to characterize the design space of the gap and electrode geometry. Figure 5 shows the results for various geometries. For cases where the dimensionless gap width η, is greater than 0.1, the capacitance of the electrode pair is substantially greater than for an ideal parallel-plate capacitor of area $w \times w$. This indicates that regions of the electrode surfaces beyond the immediate vicinity of the junction have significant influence on the electric field in the interface gap, and contribute substantially to the overall capacitance.

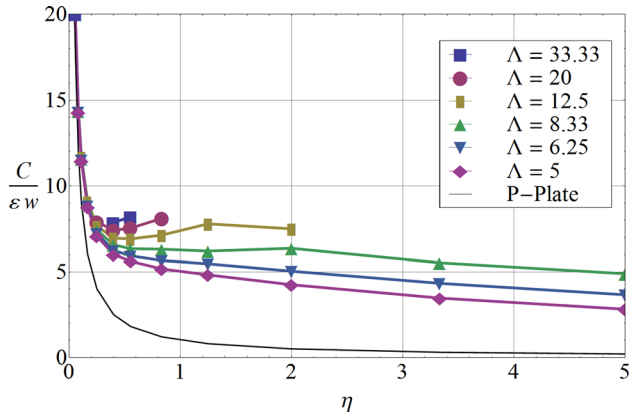

Fig. 5 Plot of dimensionless capacitance versus normalized gap thickness η for several values of normalized electrode length Λ. The behavior of an ideal parallel-plate capacitor of area $w \times w$ is shown for comparison.

For practical applications, electrode configurations with closely spaced junctions are desired so that the sensor exhibits near-uniform sensitivity across the entire interface; however, the sensor is most useful for creating a map of the material distribution if each junction exhibits dependence on only one isolated region of the interface gap, with no overlap with corresponding regions from adjacent junctions. For this reason, junctions should be spaced to allow for independence of electric fields to a desired (threshold) extent; this requirement is referred to as the *localization criterion*. The capacitive response of a junction corresponds to the interfacial dielectric material(s) present in the $p_{min} \times p_{min}$ region centered at the junction, termed the *detection zone,* as shown in Fig. 3. The localization criterion may be satisfied through design of the electrode pitch p to be large enough to prevent the detection zones of adjacent junctions from overlapping. Hence, p_{min} defines not only the detection zone, but the minimum electrode pitch allowed by the criterion.

The detection zone length, or minimum electrode pitch p_{min}, is normalized against the electrode width w, and the normalized quantity is denoted λ_{min}. As with overall capacitance, λ_{min} must be a function of gap size η and electrode length Λ. Although the minimum physical limit of λ is unity, corresponding to an electrode pitch being equal to the electrode width, a stricter limitation is imposed by the localization criterion. Figure 6 shows the dimensionless minimum electrode pitch allowed by a 95% localization criterion predicted by the simulation as a function of gap

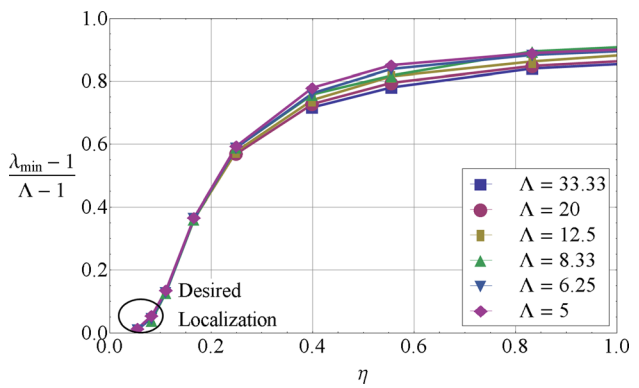

Fig. 6 Minimum pitch for parallel electrodes normalized such that a value of 0 corresponds to an electrode pitch equal to the electrode width, and a value of 1 correspond to an electrode pitch equal to the electrode length. The results are shown for several values of electrode length Λ as a function of gap thickness.

size. The minimum pitch allowed by the criterion approaches the electrode width for narrow gaps ($\eta \ll 1$). For $0.2 < \eta < 1$, the detection zone encompasses nearly the entire electrode ($\lambda_{min} \to \Lambda$). For such a system, the localization criterion only allows a single junction to represent the entire $L \times L$ area of the interface, leading to poor resolution.

In order to design a system where many junctions may be accommodated over an interface while satisfying the localization criterion, the electrode width must be large compared to the interfacial gap that must be characterized. Only when this condition is met can the minimum electrode pitch be reduced to a reasonable fraction of the electrode length. The number of junctions that may be placed across the length of an electrode must satisfy

$$M \leq \Lambda_n/\lambda_n, \quad N \leq \Lambda_m/\lambda_m \tag{6}$$

where the subscripts n and m are used to refer to the first substrate with N electrodes and the second substrate with M electrodes, respectively (see Fig. 1). With an $N \times M$ array of electrode junctions, the interfacial region may then be characterized by capacitance readings taken from each pair of electrodes.

In contrast to wire mesh sensors, where the intrusive electrodes are kept very narrow (0.12 mm) with their spacing being large in relation (3.12 mm) [9], the rectangular, surface-mounted electrodes in the sensor design proposed here should be comparatively wide and spaced as closely as the localization criterion allows. By this means, the large active surface area of the electrodes will allow for greater sensitivity by creating a larger nominal capacitance, against which variations produced by even small voids may be detected. This design advantage is not possible for wire meshes inserted into fluid flows, because the physical intrusiveness of large electrodes would disrupt the flow.

4 Capacitance Network Model

4.1 Problem Formulation. This work considers capacitance measurements between two electrodes on opposite substrates (i.e., active electrodes), where no grounding is used for all other electrodes (i.e., inactive electrodes). Thus, the capacitance measured at any junction is indicative of the junction capacitance plus any additional capacitance contributions from neighboring regions throughout the floating system. This approach is in contrast to the active reduction of crosstalk for the wire mesh sensors in Ref. [9].

When inactive electrodes are allowed to float, significant interactions occur between the capacitances at all electrode junctions as well as those between parallel electrodes. Thus, all capacitances present in the system contribute to the measured capacitance of any given electrode pair at a junction. Understanding the behavior of the network of capacitors created by the circuit is necessary to match experimentally obtained measurements with theory, and ultimately, to produce a robust system where anomalies in the dielectric distribution may be identified and void regions detected.

Consider the basic system of two pairs of parallel electrodes shown in Fig. 7. Peripheral capacitance pathways, besides the one at the actuated junction, result in an effective network of capacitors, of which only the overall effective capacitance may be directly measured. The solid arrow indicates the region of the desired capacitance value, while the other arrows represent peripheral capacitances created by the electrode configuration. These include capacitances between parallel electrodes (Cn_i and Cm_j) and junction capacitances other than the active junction (C_{ij} where $i \neq h$ and $j \neq k$). Two simplifying assumptions are made in this type of model: (1) only capacitances between proximate electrodes are considered, but some capacitance exists between a given electrode and every other electrode in the system; (2) the sidewall capacitances (Cn_i, Cm_j) and junction capacitances (C_{ij}) are modeled as independent. For modeling purposes, these approximations capture first-order effects.

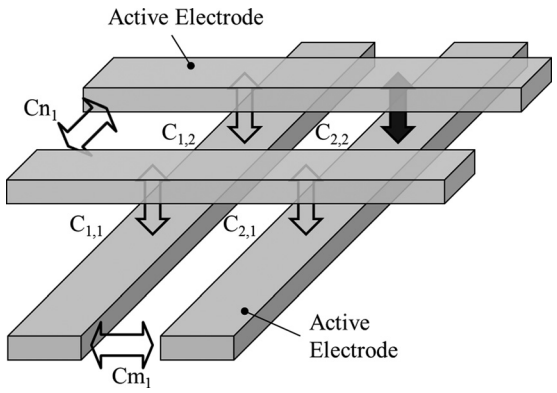

Fig. 7 Schematic diagram of a two-by-two system of electrodes. The desired capacitance measurement junction is shown as a solid black arrow.

The components illustrated in Fig. 7 all contribute to the measured capacitance between the active electrodes, and together, constitute a large network. This network is illustrated in Fig. 8 for a 5×5 junction array, and described in generalized terms for an $M \times N$ system. No groupings of either parallel or serial capacitors can be identified which would simplify the system.

Solution of this circuit requires the use of Kirchoff's conservation laws, where the capacitors contribute imaginary impedances to the circuit. Voltage conservation through each pathway from V_1 to V_2 provides MN equations describing the circuit

$$V_1 - V_2 = \sum \left(j\omega C_{ij}\right)^{-1} \tag{7}$$

Conservation of current is used at each of $N+M$ nodes to complete the mathematical description of the circuit

$$\sum I_{in} - I_{out} = 0 \tag{8}$$

The resulting system of coupled $MN+N+M$ equations must be solved simultaneously to obtain the imaginary currents through each capacitor.

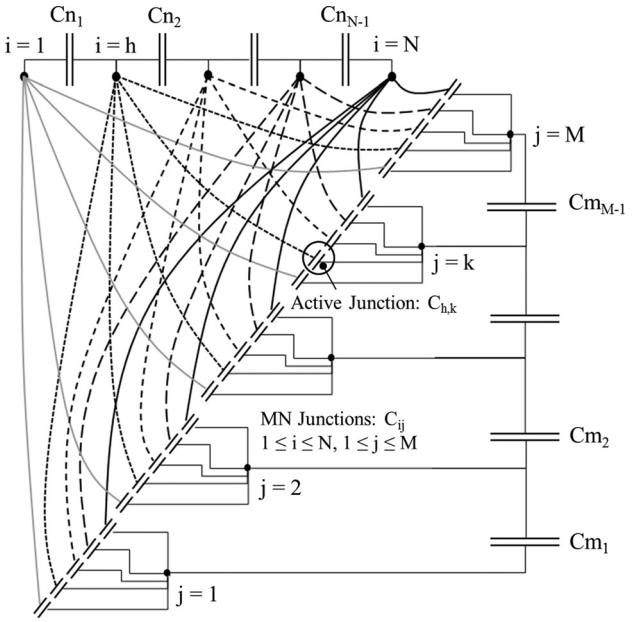

Fig. 8 Circuit network created by an $M \times N$ array of electrodes. For the case shown, $M = N = 5$, $h = 2$, and $k = 4$.

4.2 Network Model. A generalized solution method for the coefficient matrix describing the linear system of equations for any given N, M, h, and k, for the actuated electrode pair, h–k is presented here.

First, the system matrix **A** is defined as a square $MN+M+N$ matrix (see Fig. 9), where the first MN columns represent coefficients of the unknown imaginary currents $I_{i,j}$ through the junction capacitors C_{ij}. The j index is nested within i index. The next $N-1$ columns represent coefficients of the unknown imaginary currents In_i, through the side capacitors Cn_i. The next $M-1$ columns represent coefficients of the currents Im_j, through the side capacitors Cm_j. The final two columns hold coefficients of the unknown inlet and outlet currents $I_{\mathrm{sys,in}}$ and $I_{\mathrm{sys,out}}$. The first MN rows of the matrix correspond to the voltage loops that begin at V_1 and end at V_2, traveling through capacitor C_{ij}, as described by Eq. (7). The indexing is performed as for the columns, forming diagonal matrix **D**. The next N rows are used to perform the current balances at all side nodes 1–N, and the final M rows are used to perform the current balances at the j nodes, 1–M, as described by Eq. (8). The system matrix is conveniently shown as consisting of the six submatrices **D**, **P**, **Q**, **R**, **S**, and **T** in Fig. 9.

A brief description of each submatrix is presented here. The diagonal matrix **D** contains coefficients describing the imaginary impedance at every junction. The matrices **P** and **Q** contain entries representing the impedance resulting from the capacitance existing between parallel electrodes on the n side and m side, respectively. The $M+N$ electrodes in the system are modeled as current nodes (all points i and j in Fig. 8), for which ingoing and outgoing currents must sum to zero. The matrix **R** contains a series of positive and negative coefficients of magnitude one, which represent the contributions of the imaginary currents passing through the junctions C_{ij} pertaining to these $M+N$ constraints for current conservation. The matrix **S** completes the constraints for current conservation with a series of positive and negative coefficients of magnitude one, which represent the contributions of currents passing through the side capacitances Cn_i and Cm_j. The matrix **T** contains only two nonzero entries: 1 for the incoming current $I_{\mathrm{sys,in}}$, and 1 for the outgoing current $I_{\mathrm{sys,out}}$. All nonzero entries of the submatrices may be determined by the following equations:

$$\mathrm{D}_{(i-1)M+j,(i-1)M+j} = \left(j\omega C_{ij}\right)^{-1} \tag{9}$$

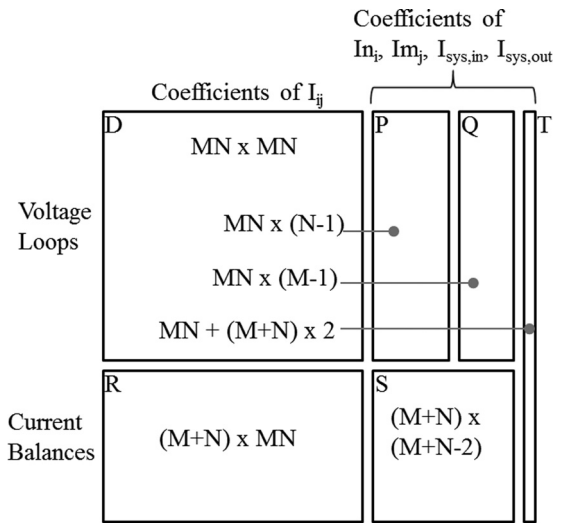

Fig. 9 Layout of the square matrix, A, of dimension *MN+M+N*, describing the circuit network. The system is shown as a compilation of six submatrices.

$$\mathrm{P}_{i,j} = \begin{cases} (j\omega Cn_i)^{-1} & 1 \le i \le Mj \quad \text{for} \quad 1 \le j < h \\ (j\omega Cn_j)^{-1} & Mj < i \le MN \quad \text{for} \quad h \le j < N \end{cases} \tag{10}$$

$$\mathrm{Q}_{i+aM,j} = \begin{cases} (j\omega Cm_j)^{-1} & i \le j < k \ \text{ for } \ 1 \le i < k \\ (j\omega Cm_j)^{-1} & k \le j < i \ \text{ for } \ k < i \le N \end{cases} \quad a = 0,1,2,\ldots N-1 \tag{11}$$

$$\mathrm{R}_{N+j,iM+j} = -1 \quad 1 \le j \le M \quad \text{and} \quad 0 \le i < N \tag{12}$$

$$\mathrm{R}_{i,j} = -1 \quad M(i-1) < j \le Mi \quad \text{for} \quad 1 \le i \le N \tag{13}$$

$$\mathrm{S}_{i,i} = \begin{cases} 1 & 1 \le i < h \\ -1 & h \le i < N \end{cases} \tag{14}$$

$$\mathrm{S}_{i,i-1} = \begin{cases} -1 & 2 \le i \le h \\ 1 & h < i < k+N \\ -1 & N+k \le i < N+M \end{cases} \tag{15}$$

$$\mathrm{S}_{i,i-2} = \begin{cases} -1 & N+2 \le i \le k+N \\ 1 & N+k < i \le N+M \end{cases} \tag{16}$$

$$\mathrm{T}_{NM+h,1} = 1 \tag{17}$$

$$\mathrm{T}_{NM+N+k,2} = 1 \tag{18}$$

The complete $MN+N+M$ square matrix **A** describing the network is formed from grouping the matrices in the manner shown in Fig. 9, which may be written explicitly as

$$\mathbf{A} = \left((\mathbf{D}|\mathbf{P}|\mathbf{Q})^{\mathrm{T}} | (\mathbf{R}|\mathbf{S})^{\mathrm{T}} \right)^{\mathrm{T}} \Big| \mathbf{T} \tag{19}$$

Complete description of the system also requires an $MN+N+M$ column vector **B**, which contains the potential difference for the first MN entries. Vector **B** completes the voltage loop equations represented in the first MN rows of **A**

$$\mathrm{B}_i = \begin{cases} V_1 - V_2 & 1 \le i \le MN \\ 0 & MN < i \le MN+M+N \end{cases} \tag{20}$$

The solution to the system is a vector **U** containing all imaginary currents in the network

$$\mathbf{U} = \mathbf{A}^{-1}\mathbf{B} \tag{21}$$

Letting **I** represent an $M \times N$ matrix of the currents passing through each junction, the values of **U** are related to **I** according to

$$\mathrm{I}_{i,j} = \mathrm{U}_{(i-1)M+j} \tag{22}$$

The imaginary currents in **I** provide one measure of comparison of the contribution of each junction to the overall capacitance of the system. As may be seen in Fig. 8, only at the active junction is the voltage loop characterized by a single capacitance from node h to node k. For all other pathways between the active nodes, the current path from node h to node k passes through multiple serial capacitances, which has the effect of reducing imaginary current. Thus, for a nominal array where all junction capacitances are equal, the current in the active junction will be greater than in the surrounding junctions. When the side capacitances Cn_i and Cm_j are small, the current through the nonactive junction pathways is reduced, and the overall capacitance measurement becomes more representative of the capacitance at the active junction.

The overall network capacitance is the value that may be compared against experimental measurements. Solving for the network capacitance requires the overall system input current. This current is contained in the penultimate entry of **U**. As a solution check, the final entry of **U**, $I_{\mathrm{sys,out}}$, must be equal to $I_{\mathrm{sys,in}}$ in magnitude but opposite in sign

$$I_{\text{sys,in}} = \text{U}_{MN+M+N-1} \tag{23}$$

The overall capacitance of the network, as measured through junction h–k, may now be calculated as

$$C = \text{Ceq}_{h,k} = \frac{I_{\text{sys,in}}}{(V_1 - V_2)j\omega} \tag{24}$$

The equivalent capacitance predicted by the network model may be directly compared with the experimental value obtained by actuating the junction h–k. In order to produce a map of theoretical capacitance readings comprising **Ceq**, Eqs. (9)–(24) must be computed for every permutation of h–k in the array.

4.3 Reverse Network Solution. To detect anomalies in the dielectric distribution in the interface gap, an experimentally obtained capacitance map of network capacitances, **Cx**, must be used to reconstruct the map of actual junction capacitances, **C**, where **Ceq** is approximated as **Cx** in the model. This requires solving the network model in reverse. A reverse solution cannot be explicitly calculated junction-by-junction as done for the for ward solution. Thus, recovering the capacitance map **C** requires solving $(MN) \times (MN + M + N)$ simultaneous unknown imaginary currents. Instead of finding an explicit, generalized solution to this problem, it is solved via an unconstrained optimization routine that utilizes the search direction update recommended by Fletcher [18], commonly known as the Broyden–Fletcher–Goldfarb–Shanno (BFGS) method.

The optimization routine searches for the set of MN junction capacitances (in matrix **C**) that minimizes the sum of squared errors between the calculated network solution (matrix **Ceq**) and the experimentally obtained capacitance map (matrix **Cx**). Due to the approximations inherent in the model, the mathematical inverse of the network model exhibits a pattern of nonphysical errors in the recovered **C** map. If the interfacial gap thickness is known a priori, then these effects may be accounted for through introduction of appropriate bounds in the optimization routine. When such bounds are used, the reverse network model is referred to as the constrained reverse network model. The bounding technique is illustrated with experimental data in Sec. 6.

5 Test Unit and Calibration

An experimental test unit was fabricated for validation of the proposed sensor system using two arrays of five copper electrodes each, imbedded in transparent acrylic substrates. Figure 10 shows the test piece. Plastic spacers (not shown) fit between the blocks to create defined spacing values of 25, 51, 102, 256, and 508 μm (corresponding to 1, 2, 4, 10 and 20 mil, respectively). The thickness of the electrodes (resulting in sidewall area depicted in Fig. 7) is 850 μm, while their width is 640 μm. The simulation reveals that for this particular test unit: (1) The maximum allowable gap thickness for 95% electric field localization while maintaining independent detection zones is 79 μm and (2) for an interfacial gap of 25 μm, a 95% criterion places the detection zone at exactly the 640×640 μm electrode junction area.

The capacitance at each junction is measured with a commercial capacitance sensor (Analog Devices AD7746), at an excitation frequency of 32 kHz. The Evaluation Board software package associated with the AD7746 is employed for data acquisition. The manufacturer specification for absolute uncertainty of capacitance measurements is ± 4 fF [19].

The capacitance sensor utilizes manual probe contacts that are connected sequentially to each h–k electrode pair of the test cell. Fifty consecutive readings are taken, with RMS variation of 0.1 fF. Gap size variability associated with disassembly and reassembly of the test unit is the dominant source of uncertainty, and ranges from ± 2 μm for the 25 μm gap to ± 10 μm for the 508 μm gap. The sidewall capacitances (entries of **Cm** and **Cn**) are obtained experimentally with the same sensor. Test unit parameters are listed in Table 1. Data obtained for the center junction and a corner junction with an empty interface gap filled with air are

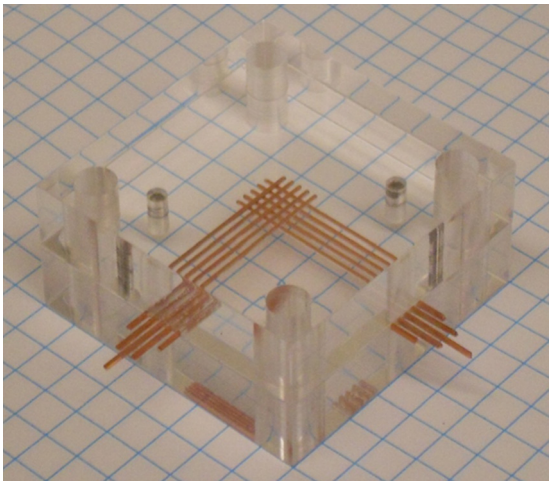

Fig. 10 Experimental test unit with an $M = N = 5$ electrode array. The two acrylic substrates are shown placed flush together.

Table 1 Parameters of the experimental test unit.

	Actual	Dimensionless
Electrode width	$w = 0.64$ mm	—
Electrode pitch	$p = 1.55$ mm	$\lambda = 2.38$
Electrode length	$L = 30.5$ mm	$\Lambda = 50$
Parallel electrode capacitance on side N	$\mathbf{Cn} = \begin{Bmatrix} 1489 \\ 1602 \\ 1573 \\ 1556 \end{Bmatrix} fF$	$\mathbf{Cn}/\varepsilon w = \begin{Bmatrix} 263 \\ 283 \\ 278 \\ 275 \end{Bmatrix}$
Parallel electrode capacitance on side M	$\mathbf{Cm} = \begin{Bmatrix} 1406 \\ 1464 \\ 1516 \\ 1564 \end{Bmatrix} fF$	$\mathbf{Cm}/\varepsilon w = \begin{Bmatrix} 248 \\ 258 \\ 268 \\ 276 \end{Bmatrix}$
Threshold gap for localization	$H_{\max} = 79$ μm	$\eta_{\max} = 0.123$
Permittivity of interface	$\varepsilon = 8.854 \times 10^{-12}$ F/m	$\varepsilon_r = 1.00$
Single junction capacitance (simulation estimate)	153 fF	$\mathbf{Cm}/\varepsilon w = 27$
Detection zone at $H = 25$ μm	640×640 μm	$p_{\min}/w \times p_{\min}/w = 1 \times 1$

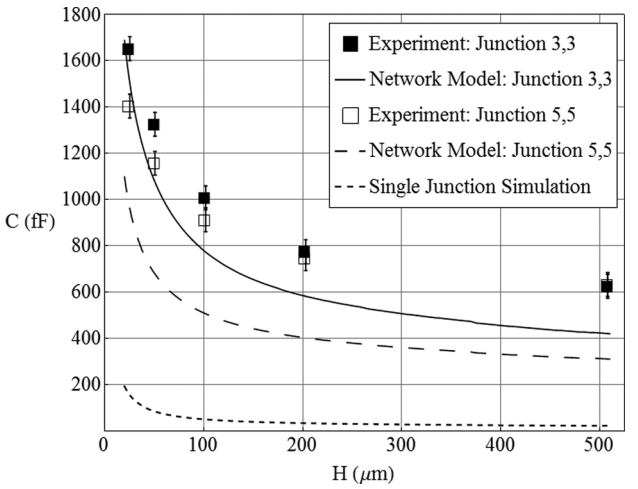

Fig. 11 Comparison of experimental capacitance measurements with predictions from a representative junction simulation and the network model as a function of gap size H

shown in Fig. 11. The performance of the sensor with an empty air gap interface is used as a baseline case for comparison with the grease spot experiments in Sec. 6, as well as for model validation. A theoretical single junction capacitance, simulated in a domain corresponding to $p = 1.55$ mm in each direction, is used to estimate a theoretical baseline value of 153 fF for C_{ij} to create the network model curve. The theoretical capacitance of an isolated junction is also shown to illustrate the disparity between a single junction capacitance and the floating network capacitance.

The map of readings predicted by the network model using the theoretical baseline for a 25 micron gap is shown in Fig. 12(*a*). The network model captures the magnitude and trends of the experimental measurements (Fig. 12(*b*)). The model underpredicts the network

(a) Network Model: Baseline 153 fF				
938	1111	1152	1112	944
1114	1368	1431	1369	1122
1158	1435	1504	1436	1167
1122	1381	1444	1382	1131
954	1135	1177	1135	960
(b) Experiment				
1386	1544	1553	1541	1428
1457	1631	1638	1622	1493
1507	1691	1697	1683	1551
1491	1665	1672	1663	1538
1374	1518	1525	1525	1435
(c) Error				
-32%	-28%	-26%	-28%	-34%
-24%	-16%	-13%	-16%	-25%
-23%	-15%	-11%	-15%	-25%
-25%	-17%	-14%	-17%	-26%
-31%	-25%	-23%	-26%	-33%

Fig. 12 Theoretical and experimental results for an empty air gap, H = 25 μm, in fF: (*a*) network model results, (*b*) experimental results, and (*c*) model error

(a) Theoretical Baseline				
153	153	153	153	153
153	153	153	153	153
153	153	153	153	153
153	153	153	153	153
153	153	153	153	153
(b) Calibrated Baseline				
345	272	252	262	377
218	173	158	165	216
239	191	170	177	257
240	181	167	180	237
329	244	220	235	388
(c) Error				
-56%	-44%	-39%	-42%	-59%
-30%	-12%	-3%	-7%	-29%
-36%	-20%	-10%	-14%	-40%
-36%	-15%	-8%	-15%	-35%
-53%	-37%	-30%	-35%	-61%

Fig. 13 Baseline estimate for empty air gap, H = 25 μm in fF: (*a*) single junction simulation, (*b*) reverse network model calculation on experimental data providing the calibrated baseline, and (*c*) model error

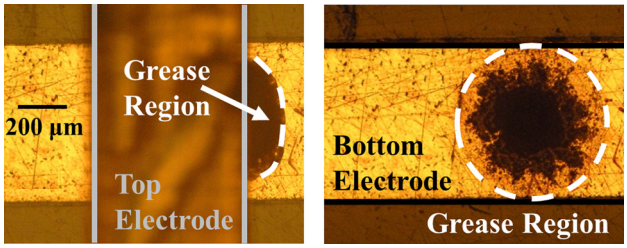

Fig. 14 Photograph of the grease spot for case 2 between the horizontal electrode underneath and vertical electrode above (left) and with top substrate removed (right)

capacitance by 10–30%, and overestimates the variation between the center junction and perimeter junctions. It is noted that the uncertainty in gap size alone is expected to contribute to an error of 3–5%. The majority of the error observed is attributed to the two simplifying assumptions of the model discussed Sec. 4.1.

As previously mentioned, the theoretical baseline capacitance of each junction, shown in Fig. 13(*a*), is 153 fF. However, the baseline capacitance values calculated by applying the reverse network model to the experimental measurements (Fig. 13(*b*)) have a nonuniform distribution. The discrepancy observed between baseline maps (Fig. 13(*c*)) is analogous to the discrepancy in network maps (Fig. 12(*c*)). In order to mitigate model error, it is recommended that a baseline map of the individual junction capacitances be obtained by experimental calibration using an empty gap. This compensates for second-order effects not accounted for in the network model and avoids the need for simulation to characterize a typical baseline electrode junction.

6 Thermal Grease Detection With Reverse Network Model

The test unit is used for identifying the location of small spots of thermal grease (Laird Tgrease 1500) with a manufacturer-reported dielectric constant of 5.9 [20], in an otherwise empty 25 μm-thick air–gap interface. The analysis approach presented for this experiment is easily extended to the detection of small voids in a grease-filled interface. Use of dielectric grease spots allows easier control in practice for introducing anomalous dielectric regions artificially into the gap, relative to creation of voids in a grease-filled gap.

The grease spot is applied to one sensor substrate and pressed against an opposing substrate. After the map of readings is taken, the top substrate is carefully separated to expose and observe the grease spot location under a microscope. Microscopic features visible on the surface of the electrode on the bottom substrate before and after separation of the substrates are used to calculate the position of the electrode on the top substrate relative to the grease region. A circle is fitted to the pixel coordinates of the grease spot perimeter; the expected resolution of the sensor does not warrant more refined spatial characterization of the grease spot. Figure 14 illustrates the top view of an electrode junction with a grease spot shown before (left) and after (right) the top substrate is removed. During substrate separation, grease retracts from the original perimeter, but residue defining the original perimeter of the region is still distinguishable.

Six cases are used to illustrate the capabilities of the sensor. Cases 1–4 include a grease spot of decreasing size roughly centered at the middle junction. Case 5 considers a grease spot centered between two junctions, and case 6 consists of two grease spots at different junctions. The locations of each circular grease region as obtained from microscopic imaging are illustrated graphically in Fig. 15.

To illustrate the data reduction, intermediate stages of analysis are shown for case 1 in Fig. 16, beginning with the raw capacitance measurements (Fig. 16(*a*)). The reverse network solution (Fig. 16(*b*)) indicates that capacitances for the highlighted junctions are lower than the baseline value with no grease (Fig. 13(*b*)). However, for a given gap size, capacitance can only increase due to the introduction of grease. Although gap size uncertainty could account for some of this effect, consistent recurrence of this pattern, particularly at the four junctions adjacent to an affected junction, identifies it as a nonphysical distortion of the reverse solution due to the approximations inherent in the network model.

Instead of simply reassigning these highlighted junctions their baseline values, model sensitivity can be enhanced by constraining the

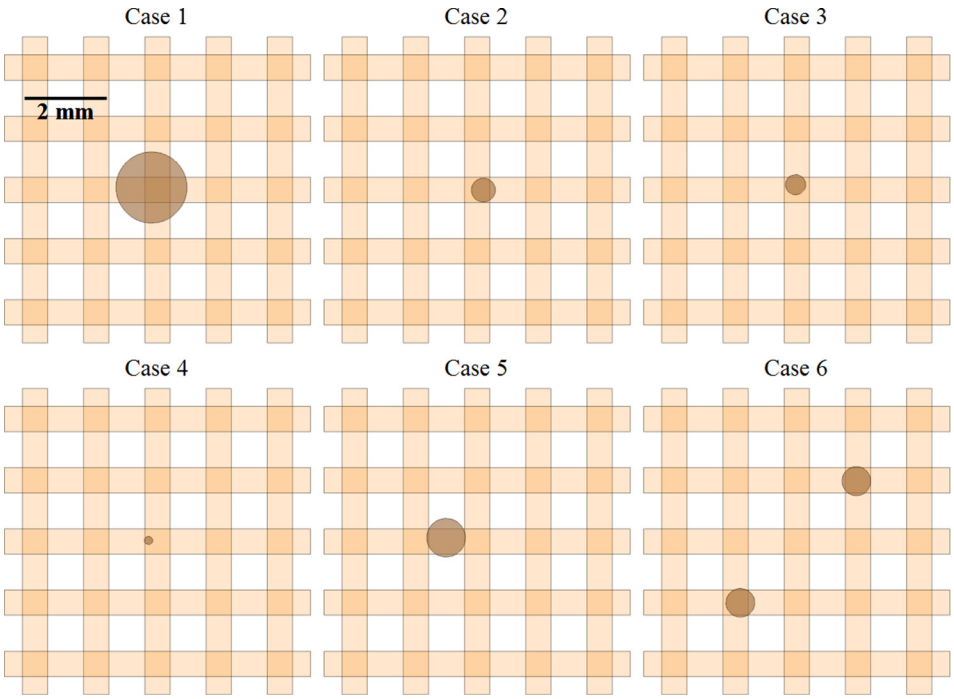

Fig. 15 Graphic illustration of grease spots used in the experiment, drawn to scale

(a) Measured Values				
1387	1549	1667	1545	1430
1466	1657	1836	1647	1505
1625	1900	2433	1890	1679
1494	1679	1864	1681	1550
1374	1520	1650	1532	1441
(b) Reverse Network Model				
338	274	270	263	369
217	198	79	187	219
266	100	1029	87	280
240	203	59	200	247
322	231	266	229	381
(c) Constrained Reverse Network Model				
345	272	252	262	377
218	173	158	165	216
239	191	865	177	257
240	181	167	180	237
329	244	220	235	388

Fig. 16 Data analysis steps for Case 1 showing capacitance in fF: (*a*) experimentally measured values, (*b*) junction capacitance map obtained by solving the reverse network model using measured values (junction values lower than the baseline values in (*b*) are highlighted in yellow), and (*c*) junction capacitance map using the constrained reverse network model. The darkened cell indicates that the junction detection zone contains grease.

optimization routine with the baseline values as lower bounds. The BFGS algorithm for unconstrained optimization may still be employed when the optimization variables are defined as $x_{i,j}$ according to

$$C_{i,j} = (C_{i,j})_{\text{base}} + 2^{x_{i,j}} \tag{25}$$

where $(C_{i,j})_{\text{base}}$ indicates the baseline value for the junction. In this way, the optimization variables may range without bound while the value of $C_{i,j}$ is bounded at the baseline value. This implementation of an unconstrained optimization algorithm is simpler than traditional alternative methods of constrained optimization. When optimization is constrained, the solution for the map of junction capacitances is no longer the mathematical inverse of the network model, but does provide improved physical insight. Fig. 16(*c*) shows the results of the constrained reverse network model for case 1.

The impact of the grease on the dielectric distribution is visualized by subtracting the baseline map of capacitance junctions (Fig. 13(*b*)) from the calculated map of capacitance (Fig. 16(*c*)) for each case. Analysis on all six cases yields the maps of capacitance change shown in Fig. 17.

The smallest grease region centered under an electrode (200 μm diameter, case 4) is clearly detected above the background variation. The results indicate that submillimeter sensitivity may be achieved with this technique. In all cases where the grease spots are centered at electrode crossing points (cases 1–4, 6), the affected junctions contrast starkly against the background variation. For the case where the grease region is centered between junctions (case 5), the nearby detection zones are barely affected. The grease spot in case 5 is the second largest of the cases considered and emphasizes that electrode spacing should be as small as the localization criterion allows in order to properly tessellate detection zones over the region and minimize the detectable anomaly size. Case 6 illustrates that the model correctly isolates multiple anomalies within the interface gap.

A critical aspect of the sensor is the establishment of a proper threshold for identifying capacitance changes above those expected from random variation. The background variation for this set of experiments ranged from 0 to 15 fF; however, this "noise" is not distributed randomly throughout all cases. The variability observed in the cases is primarily attributed to uncertainty in gap size between the baseline case (no grease) and each experimental case. If the gap size of the test case were slightly smaller than that of the baseline, the processed measurement would exhibit a capacitance increase for all cells, such as in case 5. If the substrate planes were slightly off parallel, tilting may manifest in numerical values such as those seen in case 4, where the interface gap likely narrows from left to right. If the gap size of the particular case were slightly larger than that of the baseline, the constrained reverse model would drive background cells toward their minimum allowed values, giving the appearance of little or no background variation, as seen in cases 1 and 2.

7 Conclusion

A simple method for detecting regions of contrasting permittivity in a thin dielectric interface is proposed using orthogonal arrays of imbedded parallel electrodes. Fundamental design criteria for the use of the method are discussed in order to ensure that each capacitance measurement is the result of an electric field that is localized to the junction region of interest. Neighboring capacitances in the electrode system prevent sensor characterization using the measured capacitance from a single electrode pair. The network created by the arrays of electrodes is analyzed and a generalized solution method for the linear system presented. The solution to this system has been shown to be in reasonable agreement with experimental measurements. A method for solving the model in reverse has been outlined, and its utility demonstrated for processing capacitance measurements used to identify regions of dielectric contrast in the interface gap. The current apparatus is useful for identifying dielectric anomalies as small as 200 μm in a 25 μm thick thermal grease bondline. The technique offers an inexpensive and practical alternative to more elaborate methods commonly used for thermal interface characterization.

Case 1					Case 2					Case 3				
0	0	1	0	0	0	0	1	0	0	7	0	1	0	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	695	0	1	0	0	331	0	1	4	0	298	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1	0	0	5	0	1	0	0
Case 4					Case 5					Case 6				
0	0	2	12	9	3	7	1	8	5	0	0	1	0	0
4	2	6	8	10	7	9	6	14	11	4	0	0	588	0
0	0	75	2	14	5	24	42	1	14	0	0	0	0	1
8	2	1	5	15	3	12	1	6	14	0	554	0	0	13
0	9	8	11	14	2	6	8	8	8	0	0	1	12	3

Fig. 17 Capacitance change for the six different grease-spot cases shown in Figure 15 inside a 25 um gap, in fF. Junctions affected by the presence of grease in their detection zones are darkened.

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Nomenclature

$\mathbf{A}$ = square matrix ($NM+N+M$)
$\mathbf{B}$ = vector ($NM+N+M$)
C = capacitance
$\mathbf{C}$ = matrix ($N \times M$) of junction capacitances
$\mathbf{Ceq}$ = matrix ($N \times M$) of predicted network capacitances
$\mathbf{Cm}$ = vector ($M-1$) of parallel electrode capacitances
$\mathbf{Cn}$ = vector ($N-1$) of parallel electrode capacitances
$\mathbf{Cx}$ = matrix ($N \times M$) of experimentally observed capacitances
$\mathbf{D}$ = diagonal matrix ($MN \times MN$)
E = electric field
H = interface gap height
I = imaginary electric current
$\mathbf{I}$ = matrix ($N \times M$) of junction currents
$\mathbf{Im}$ = vector ($M-1$) of parallel electrode currents
$\mathbf{In}$ = vector ($N-1$) of parallel electrode currents
j = imaginary unit $\sqrt{-1}$
L = electrode length
M = number of electrodes on second substrate
N = number of electrodes on first substrate
p = electrode center to center pitch
$\mathbf{P}$ = system submatrix ($MN \times N-1$)
$\mathbf{Q}$ = system submatrix ($MN \times M-1$)
$\mathbf{R}$ = system submatrix ($M+N \times MN$)
$\mathbf{S}$ = system submatrix ($M+N \times M+N-2$)
$\mathbf{T}$ = system submatrix ($MN+M+N \times 2$)
$\mathbf{U}$ = vector ($MN+M+N$)
V_1 = top electrode potential
V_2 = bottom electrode potential
w = electrode width
$\mathbf{x}$ = matrix of design optimization variables

Greek Symbols

ε = permittivity
ε_r = relative permittivity ($\varepsilon/\varepsilon_0$)
ε_0 = permittivity of free space (8.854×10^{-12} F/m)
η = dimensionless gap size (H/w)
λ = dimensionless electrode pitch (p/w)
Λ = dimensionless electrode length (L/w)
ν = unit surface normal vector
φ = electric potential
ω = signal angular frequency

Subscripts

base = baseline value
h = active electrode of first substrate
i = index parameter
in = current direction entering network
j = index parameter
k = active electrode of second substrate
m = substrate containing M electrodes
max = maximum allowed by localization criterion
min = minimum required by localization criterion
n = substrate containing N electrodes
out = current direction exiting network
sys = capacitance network system

Individual matrix and vector entries are written with the matrix or vector name in nonbold type with identifying subscripts. For example, $Ceq_{i,j}$ indicates the i,j component of ***Ceq****.*

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