Society of Engineering Science 51st Annual Technical Meeting

1–3 October 2014

Purdue University, West Lafayette, Indiana, USA

High density semiconducting nanotube arrays for high-performance electronics

Cao, Qing, qcao@us.ibm.com, IBM T.J. Watson Research Center

ABSTRACT

Single-walled carbon nanotubes are poised to replace silicon in high-performance microprocessor chips and are expected to offer a significant improvement in energy-delay product. However, one key challenge of realizing such a technology is to produce semiconducting nanotube arrays with both minuscule and uniform inter-tube pitch to provide sufficient packing density, power output, and performance homogeneity for each transistor. Here, we will review our latest progress on assembling pre-sorted high purity semiconducting nanotubes into densely packed arrays. In an example, double-layered arrays with full surface coverage and a tube density >500 tubes/μm are assembled with Langmuir–Schaefer method. The nanotube pitch is self-limited by the tube diameter plus Van der Waals separation. In another example, submonolayered arrays with both tight and consistent pitch as small as 21 ± 6 nm are assembled using the fringing field formed between surface microelectrodes and the substrate. Effective screening of the fringing field by the deposition of nanotubes limits the pitch and prevents the formation of multilayer structures in a self-limited fashion as revealed by detailed experimental and theoretical studies. Field-effect transistors based on such arrays demonstrate exceptional performances, setting new benchmarks for nanotube devices.