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Impact of Buffer Charge on the Reliability of Carbon Doped AlGaN/GaN-on-Si HEMTs

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***Abstract*— Charge trapping and transport in the carbon doped GaN buffer of an AlGaN/GaN-on-Si high electron mobility transistor (HEMT) have been investigated. Back-gating and dynamic R_{ON} experiments show that a high vertical leakage current results in significant long-term negative charge trapping in the buffer leading to current collapse under standard device operating conditions. Controlling current-collapse requires control of not only the layer structures and its doping, but also the precise balance of leakage in each layer.**

***Keywords*-Field effect transistors, HEMTs, microwave transistors, power transistors, current collapse, dynamic R_{ON}**

I. INTRODUCTION

High Electron Mobility Transistors (HEMTs) based on the GaN/AlGaN materials system are the primary semiconductor devices for RF power applications [1]. Of late, these devices have also been fabricated for power switching applications as a result of the basic material advantages of high breakdown voltage, high mobility, high 2DEG density and excellent thermal conductivity [2] – [7]. The underlying physics for these devices are generally understood, but some effects like current collapse (CC) (the recoverable temporary reduction in drain current after the application of a high voltage) and buffer breakdown have not been explained fully and can cause major restrictions to device performance [8, 9], particularly in power devices. CC can be induced by surface states, which can be very effectively controlled by the use of field plates [10]. But CC arising due to charge trapping in the semi-insulating buffer is still a concern. HEMTs require the use of a semi-insulating buffer to suppress leakage and punch-through which can have a profound effect on device performance. Buffer-related CC was initially explained as being due to hot-carrier injection into the buffer followed by trapping in deep levels. These deep levels are a necessary requirement for device operation since they suppress buffer leakage and short-channel effects [11]. RF devices frequently make use of Fe doping to render the GaN insulating [12] – [14], but for the higher voltages required for many power switching applications, it has been found that carbon doping delivers higher breakdown voltage and lower off-state leakage [15, 16]. Unfortunately, it has also been found that using carbon can often result in significant current-collapse [10, 15]. It is clear that CC in these devices mostly results from charge storage in deep levels in the buffer, with the difference in CC between Fe and C doping reported to be the result of their relative energy levels, respectively pinning the Fermi level in the upper and lower halves of the bandgap [17] – [22]. Monitoring the substrate bias dependence of the 2DEG current, and its dispersion as the ramp-rate and temperature are varied, allowed a model for the transport within each layer within the buffer to be constructed [18] – [20]. The structures investigated in this work generally consist of a AlN nucleation layer grown on a p-type Si substrate, followed by a superlattice or graded AlGaN layer to compensate the lattice mismatch between the substrate and the GaN. Termed as the accommodating layer, or strain relief layer (SRL), it is an insulating layer to prevent vertical leakage in the devices. Above the SRL is the carbon doped GaN (GaN:C) and the unintentionally doped GaN layer forming the channel region.

This work presents CC and substrate-bias results on a range of devices with different SRL structures. It shows that a high leakage current results in significant long-term negative charge trapping in the buffer which leads to a reduction of 2DEG current, high dynamic on-resistance and serious current instabilities under field polarities corresponding to those of normal device operations, making it unsuitable for power applications.

II. EXPERIMENTAL DETAILS

Two-finger HEMTs were processed on GaN-on-Si wafers using TiAlNiAu based contacts. Three flavors of SRL were fabricated. Table I shows the device description with associated parameters such as sheet resistance of the 2DEG, Hall mobility and 2DEG density. All epitaxial layer structures contain 800nm of intentionally carbon doped GaN buffer with a 250nm undoped channel region grown on various thicknesses of graded AlGaN:C SRL. The graded AlGaN layer, starting as pure AlN at the substrate inter-face transforming to pure GaN at the GaN:C interface, was chosen to not introduce any hetero-interface between GaN:C and substrate that might lead to accumulation of free charges and/or hinder vertical charge flow similar to [20]. Two experiments were undertaken: a drain transient measurement to measure dynamic R_{ON} and substrate bias ramp to characterize buffer charging and vertical leakage.

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TABLE I: DEVICE DESCRIPTION WITH ASSOCIATED PARAMETERS

Device Type	SRL Type & Thickness	Threshold Voltage (V)	Sheet Resistance (Ω/cm^2)	Hall Mobility (cm^2/Vs)	2DEG Density ($/cm^2$)
A	AlGaN (C & Si co-doped) 1.7 μm	−4.5 V	381	1891	$8.7x10^{12}$
B	AlGaN (C & Si co-doped) 2.5 μm	− 4.3 V	375	1909	$8.7x10^{12}$
C	AlGaN (C & Si co-doped) 3.8 μm	− 5 V	335	2032	$9.1x10^{12}$

For the dynamic R_{ON}, the HEMTs tested had a gate-drain spacing of 12μm. All the devices tested had a gate and source field plate each 1μm long. They were biased in the off-state with V_{GS} = −7V and V_{DS} = 100V for a time period of 1000s before pulsing to the on-state with V_{GS} = 0V, V_{DS} = 1V. This corresponds to a "worst case" V_{DS} for dynamic R_{ON} measurement [23, 24]. The on-state current, I_{DON}, was then recorded for 1000s allowing the device to return towards equilibrium. The complementary substrate bias ramp works as follows. The change in conductivity of the 2DEG in the HEMT as substrate-bias was applied to the silicon wafer was used to monitor changes in the vertical electric field in the buffer below the 2DEG. Changes in the channel conductivity can then be used to quantify bulk charge storage and trapping assuming 1D conduction. However variation of the gap size between ohmic contacts was found to influence the measurements, indicating strong contact related effects meaning that lateral transport also had to be considered [18]. Only negative substrate bias, V_{SUB}, is considered here since this corresponds to the polarity experienced under the drain in a transistor under OFF state conditions.

III. RESULTS & DISCUSSION

Fig. 1 shows the dynamic R_{ON} measurements of the three device types following 1000s off-state stress at room temperature. Device A shows the smallest change in the on-state resistance (up to 10%) after 1000 seconds of OFF stress recovering to within 4% of the original value after 1000 seconds. Device B shows up to 30% increase in R_{ON} recovering to within 15% of the original value after 1000 seconds. Device C shows the worst behaviour (ΔR_{ON} up to 55%) and recovers to ~10% of the original value after 1000 seconds of on-time. It is interesting to note that none of the devices show complete recovery even after 1000 seconds of ON-state measurements. Since it is challenging to distinguish between surface and bulk induced CC, complementary substrate ramp measurements were undertaken to determine the trapping mechanism. This approach has the major advantage that any effect on the channel conductivity cannot be associated with surface effects, and the applied vertical electric field is normally assumed to be roughly uniform between source and drain. Fig. 2 shows the normalized 2DEG conductivity and the vertical leakage through the structure with respect to the substrate voltage for ungated devices (TLM structures) with varying gaps. Changes in substrate bias applied to the silicon resulted in a change in the electric field below the 2DEG and hence a change in 2DEG channel charge and I_D. As the device is ramped from 0V to −100V, the initial

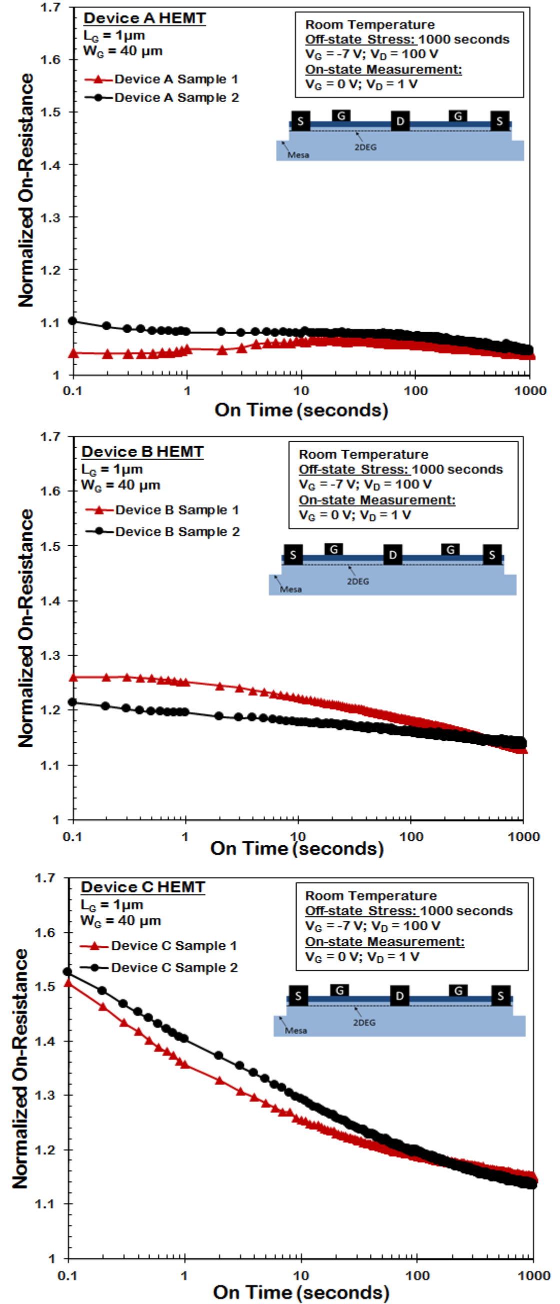

Fig. 1: On resistance after switching from off-state (V_{GS} =−7V, V_{DS} = 100V) to on-state (V_{GS} = 0, V_{DS}= 1V) on three types of devices (2 samples per device type) at room temperature. The measurements are normalized to the drain current before stress.

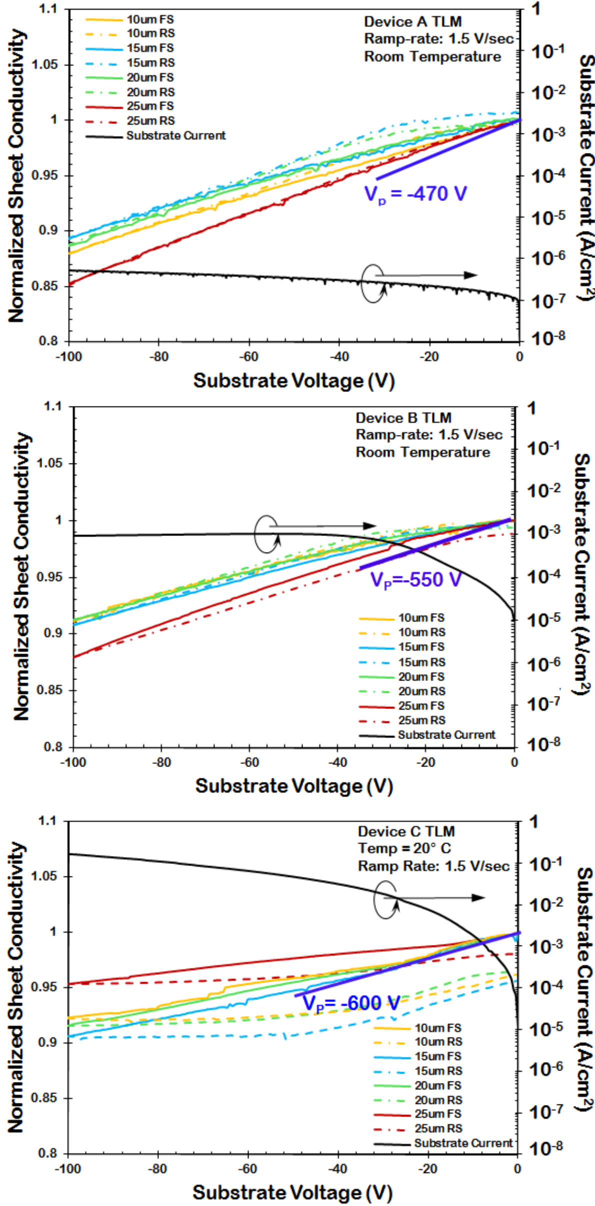

Fig. 2: (Left axis) Sheet conductivity for TLMs with varying separation between the ohmic contacts during a ramp of the substrate bias from 0 to –100V and back. (Right axis) Representative vertical substrate current (similar for all TLM gaps) during a ramp of the substrate from 0 to –100V. The experiments were carried out at room temperature at a ramp-rate of 1.5 V/sec. The sheet conductivity measurements are normalized to the drain current at V_{SUB} = 0V. (FS: Forward Sweep = 0 to –100V; RS: Reverse Sweep = –100 to 0V)

slope indicates capacitive coupling between substrate and channel (the channel current drops linearly with the voltage as indicated by the blue solid lines in fig. 2 for pure capacitive coupling together with corresponding pinch off voltage, V_P; see Appendix for the method to calculate capacitive coupling). If layers start to conduct and charging occurs, the sheet conductivity vs. V_{SUB} relation can begin to deviate from linear. Conducting layers are represented by resistors in the equivalent circuit model shown in Fig. 3. The change of doping polarity between the UID GaN and GaN:C layer is

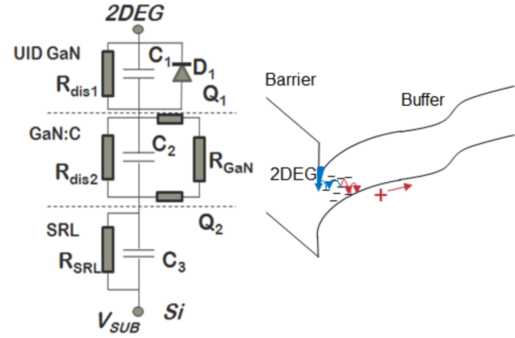

Fig. 3: 1D lumped-element representation of the device structure and the band-to-band tunneling in the UID GaN layer. The bands are lifted on the substrate side. In the C-doped region the bands are flattened. More voltage is therefore dropped across the UID GaN channel and the graded AlGaN layer.

represented by a n-p junction. As the voltage is increased, a decrease in the back-gate transconductance is observed for all device types indicating that the voltage drop across the channel region is changing slower than expected for an insulating buffer, and assuming that 1D transport applies, it would suggest that positive charge storage is occurring in the buffer which stays after the device is ramped back to 0 V resulting in slightly higher 2DEG current (as is observed in Device A). Given the sign of the field, that positive charge must have come from the 2DEG despite the fact that carbon doping results in a p-type buffer with a very low density of holes isolated from the 2DEG by a reverse biased depletion region. GaN on Si is a highly defective material with typically $>10^9/cm^2$ threading dislocations, and consequently GaN p-n diodes are normally leaky. Defect related leakage in such diodes is strongly non-Ohmic and linked to multistep trap-assisted-tunneling, probably associated with threading screw and mixed dislocations [25], [26]. The schematic showing how holes can be injected into the buffer under reverse V_{SUB}, as required to explain the V_{SUB} transients is shown in Fig. 3. However, we observe a weak dependence on the TLM gap suggesting deviations from this 1D vertical behavior. This has previously been observed locally within the device and was associated with enhanced leakage under contact regions resulting in lateral current flow within the GaN:C layer [18]. The mechanism is shown in Fig 4a.

Device B, shows intermediate behavior between A and C. In Device C, there is a very high leakage current which if distributed uniformly across the structure would mean that capacitive effects would be insignificant compared to the resistive paths. Such a high current is possible when the p-type silicon substrate goes into deep depletion and any electrons reaching the top of the silicon substrate would face no barrier to penetrate into the stack. The high substrate current at low fields indicate electron injection into the GaN:C layer from the substrate. These electrons possibly occupy deep trap states in the buffer region, effectively screening out the voltage on the substrate and remain after the back bias, causing the 2DEG current reduction. In Device C, the electron injection from the substrate overcompensates the UID leakage, which is underpinned by the high vertical leakage. Devices B and C

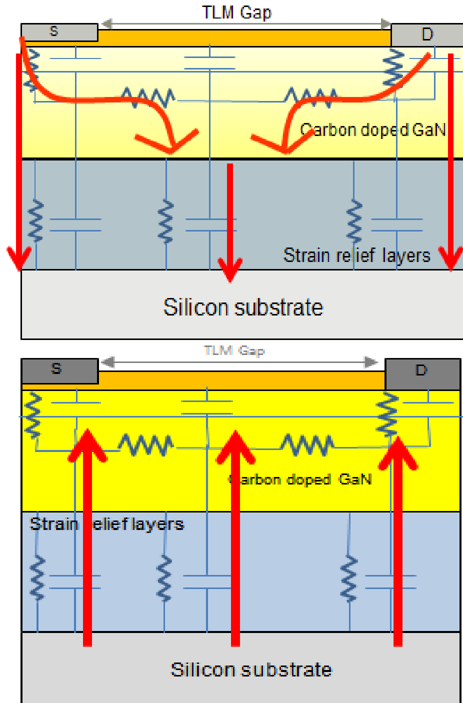

Fig 4: Proposed model of charge redistribution in the GaN:C layer leading to stored negative charge in the buffer. The figure on top indicates the mechanism at play in Devices A and B. The low substrate leakage at low fields lead to positive charge being stored in the buffer. Leaky contacts pin the GaN:C potential to the S/D potential under those contacts and generate the gap dependence. Only at very high fields, the entire structure becomes leaky. The figure at bottom indicates the mechanism in Device C, where the substrate goes into deep depletion injecting electrons into the buffer. This negative charge results in significant current collapse in the DUT.

which show a higher SRL conductivity (vertical substrate current) compared to UID leakage at low fields show higher R_{ON} dispersion. As noted above Device A shows positive charge storage in the buffer and has the least dispersion in its on-resistance. On the contrary, Devices B and C show negative charge trapping in the buffer, and show significant dispersion in their on-state resistances. The beneficial positive charge from the UID in Devices A and B, lead to neutralization of the negative charge in the buffer leading to lower R_{ON} dispersion in these devices compared to Device C. Fig. 4 shows the proposed model to explain the substrate-biasing results in Fig. 2. The TLM gap dependence showed two opposing trends. In Devices A and B, the 25 µm TLM gap showed almost no hysteresis indicating close to capacitive coupling behavior between the 2DEG and the Si and little trapping in the buffer (although Device B showed some charge trapping even for the largest TLM gap), whereas for smaller gaps hysteresis was observed implying that trapping was occurring. The simplest explanation is that there is a reverse leakage path between the buffer and the 2DEG under the contacts in Devices A & B. The TiAlNiAu based contacts create a rough interface, thereby increasing the likelihood of creating a strong coupling with the GaN:C layer allowing the injection of holes into the weakly p-type GaN:C layer. In contrast, Device C shows a complete reversal of trend and can possibly be explained by negative charge injection through the SRL into the GaN:C layer.

The negative charge storage after negative back bias implies high dynamic on-resistance and serious current instabilities under field polarities corresponding to those of a device with grounded substrate and positive voltage applied to the drain contact, making Device C unsuitable for power applications. This is evident from the results shown in Fig. 1. However as evident in Device A, positive charge tunneling into the GaN:C layer from the 2DEG is beneficial as it lowers dispersion in the on-resistance. As seen in Device C, deep depletion of the substrate at low fields results in negative charge injection into the GaN:C layer which stays even after the stress is removed leading to serious long-term trapping. Intentional incorporation of dislocations into the UID GaN to feed holes from the 2DEG into the GaN:C layer, which presumably establishes the vertical leakage path [18], could prevent the current collapse, but increasing the defect density is likely to come with other detrimental effects.

IV. Conclusion

Dynamic Ron behavior in GaN HEMTs can be dramatically different even in devices having nominally identical epitaxy. Dynamic R_{ON} measurements of devices under worst case stress conditions resulted in a significant increase in the resistance and serious current instabilities under on-state conditions, not completely recovering even after 1000s of ON-state measurements. Complementary back-gate measurements show deep depletion in the substrate can lead to electron injection into the buffer stack at low field conditions which stay after the back-bias, overcompensating the beneficial positive charge from the UID, leading to significant current collapse. Control of current-collapse thus requires control of not only the layer structure and its doping, but also the precise balance of leakage in each layer.

Appendix

Capacitive coupling calculation: Capacitive coupling can be calculated as follows

$$S(D) = \frac{\varepsilon W \mu V_D}{LD}$$

where $S(D)$ is the slope of the capacitive coupling line for a structure of thickness D, ε is the permittivity of GaN, W is the width of the structure, μ is the mobility of the 2DEG, V_D is the drain voltage and L is the distance between the ohmic contacts.

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