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Investigating the effect of $GaCl_3$ incorporation into the usual $CdCl_2$ treatment on CdTe-based solar cell device structures

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Abstract

The incorporation of $GaCl_3$ into the usual $CdCl_2$ post-deposition treatment solution of CdTe-based solar cells has been investigated. Both CdS and CdTe layers used in this work were prepared by electroplating technique and they are n-type in electrical conduction as observed from photoelectrochemical cell measurement technique. Before applying the chemical treatments to the device structures, the effect of $GaCl_3$ incorporation into the usual $CdCl_2$ treatment was first studied on the structural and optical properties of CdTe thin films. The results of the optical properties show that the bandgap of CdTe thin films treated with a mixture of $GaCl_3$+$CdCl_2$ is closer to that of bulk CdTe layers than the ones treated only with $CdCl_2$ solution. The structural properties also showed that CdTe thin films treated with $GaCl_3$+$CdCl_2$ is more crystalline than CdTe thin films treated only with $CdCl_2$ solution. The addition of $GaCl_3$ into the $CdCl_2$ solution have been seen to drastically enhance the solar-to-electric conversion efficiency of CdS/CdTe based solar cells. One of the effects of Ga incorporation into the usual $CdCl_2$ treatment was seen in the series resistance reduction which ultimately leads to enhancement in the observed short-circuit current density, fill factor and overall solar cell efficiency. For the glass/FTO/n-CdS/n-CdTe device structures, the cell efficiencies were observed in the range 1.9 - 2.1% after being treated with $CdCl_2$ solution only. When treated with $CdCl_2$+$GaCl_3$, the efficiency increased to 6.1 - 6.4%. Subsequent study on multi-junction graded bandgap solar cells using the $GaCl_3$+$CdCl_2$ chemical solution for the surface treatment of glass/FTO/n-ZnS/n-CdS/n-CdTe device structures results in solar cell efficiency >10%.

Keywords: $GaCl_3$+$CdCl_2$ solution, surface treatment, n-CdS/n-CdTe, solar cell efficiency.

1.0 Introduction

Cadmium Telluride (CdTe), a group II-VI binary compound semiconductor has been widely studied due to its unique and versatile optoelectronic properties. Different features possess by the CdTe thin films make it a suitable semiconductor material that can be applied in different research areas such as $X-$ and $\gamma-$ radiation detectors [1,2] and in photovoltaic devices [3,4]. Despite its numerous applications, the performance of CdTe devices can be limited due to tellurium precipitation during growth [5]. The presence of these Te precipitates is harmful to solar cell devices since these create defect levels which act as trap centres for photo-generated charge carriers. As explained by Fernández [5], it is difficult to totally eliminate these Te precipitates either by modifying the growth conditions or post growth treatment conditions. Researchers working in $X-$ and $\gamma-$ ray detectors have however devised some means of reducing the effect of these Te precipitates. Some of the techniques explored in reducing Te precipitates include Cl doping of CdTe thin films [6], thermal annealing in Cd vapour and use of Ga melt [7]. The experimental work reported by Sochinskii et al. [7] showed that the dissolution of Te precipitates in CdTe single crystals can be achieved by annealing in Ga melt. Since the midgap defects known as killer centres in CdTe thin films originate from Te-richness [8], finding a possible means of reducing these defects to the barest minimum would cause the efficiency of the CdTe-based solar cell device structures to further improve.

Some of the other present challenges involved in thin film solar cells fabrication have to do with improving all the solar cell parameters which are short-circuit current density (J_{sc}), open circuit voltage (V_{oc}) and fill factor (FF). Researchers working on solar cells and modules have applied $CdCl_2$ treatment to greatly improve the CdTe-based solar cells efficiency [9–11]. The application of $CdCl_2$ as chemical treatment to the top surface of CdTe thin films before annealing have been known to offer numerous advantages such as: improvement in the material crystallinity, formation of bigger grains and passivation of grain boundaries, lattice mismatch reduction between the CdS and CdTe hetero-partner, improvement of the alloying between CdS/CdTe interface, reduction of series resistance and removal of some unwanted sources of defects such as Te precipitates [9,11–13]. Therefore, since Ga which is a shallow donor in the Cd sites of CdTe thin films [5] has the potential of removing these Te precipitates and doping the material n-type; the incorporation of $GaCl_3$ into the universal $CdCl_2$ treatment has therefore been proposed in this work to be used as means of surface treatment to improve the efficiency of CdTe-based solar cells. This idea comes from the

knowledge exhibited by researchers working on $X-$ and $\gamma-$ ray detector systems. It is expected that the complementary efforts of the three ions namely Ga^{3+}, Cd^{2+} and Cl^{-} in the $GaCl_3$+$CdCl_2$ solution would be more effective to combat Te precipitates and improve material quality.

2.0 Experimental details and techniques

There are numerous methods of depositing CdS and CdTe layers. As mentioned by Basol [14], four techniques namely close-spaced sublimation, screen printing, chemical vapor deposition and electrodeposition have been successfully used to produce high efficiency CdTe-based solar cells. Electrodeposition technique with two electrode set-up has been used in this work to carry out the films deposition because it is a less expensive technique which does not require costly equipment [14]. The ED technique provides a medium for the electrolyte to be self-purified during growth [15] and it allows continuous deposition of the thin films [16]. It offers a platform for CdS and CdTe to grow as columns (that is, as nano and micro grains normal to the FTO substrate). The surfaces of FTO substrate are generally spiky and the application of DC voltage to the FTO substrate during electroplating produces high electric fields at these FTO spiky surfaces. Nucleation of materials occurs at these spiky points during ED because of the electric field present at the spikes. Due to the nature of most materials to grow best on their own surface, CdS and CdTe thin films grow perpendicular to the FTO surface while gradually increasing in diameter laterally [17]. This technique also allows the growth of n- and p-type semiconductor materials like CdTe simply by changing the growth parameters such as growth voltage and composition of the salts in the electrolytic bath [18,19].

The chemicals used were purchased from Sigma Aldrich. Since conducting substrates are required in electroplating, glass/fluorine-doped tin oxide (FTO) substrates having sheet resistance of 7 Ω/□ were used for this work. The glass/FTO substrates were cut into the required dimension and cleaned using soap solution in an ultrasonic bath for ~15 minutes. After completing the ultrasonic cleaning, the substrates were rinsed in de-ionised water. The final cleaning was done by rinsing with methanol and washing in de-ionised water before being used as the working electrode in the electrodeposition set-up. The ultrasonically cleaned glass/FTO substrates were tied to a graphite rod using polytetrafluoroethylene film to function as the cathode commonly known as working electrode in a cathodic electrodeposition process while the anode is a high purity graphite rod.

The CdS electrolyte was prepared using 0.3 M $CdCl_2$ (99.995% purity) and 0.03 M $(NH_4)_2S_2O_3$ (99% purity) in 400 ml of de-ionised water. The CdS layers used in this work were grown to a thickness of ~150 nm at an optimised cathodic potential of 1200 mV. The pH and temperature of the electrolytic bath were maintained at 2.50±0.02 and 80^{o}C respectively at the start of deposition. Similar work related to the growth and characterisation of CdS thin films using $CdCl_2$ and ammonium thiosulphate precursors has been published in details by Abdul-Manaf et al. [20].

The CdTe electrolyte was prepared using 1 M $CdSO_4$ (99.999% purity) and 2 ml of dissolved TeO_2 (99.995% purity) in 800 ml of de-ionised water. It was ensured that the Te content in the electrolyte containing 1 M $CdSO_4$ was kept low due to the Te ability to deposit at low cathodic potential and faster than Cd. The CdTe layers used in this work were grown at an optimised cathodic potential of 1400 mV. The pH and temperature of the electrolytic bath were maintained at 2.00±0.02 and 80^{o}C respectively at the start of deposition. Full details of the growth and characterisation of CdTe thin films using $CdSO_4$ precursor has been published by Diso et al. [21].

The CdTe layers grown at optimised cathodic potential of 1400 mV is n-type in electrical conduction. n-CdTe is used in this work due to its numerous advantages over p-CdTe. The resistivity of p-CdTe has been reported to be higher than those of n-CdTe [22]. The experimental work carried out by the corresponding author of this work on the resistivity of as-deposited p- and n-CdTe thin films at room temperature also showed that p-CdTe thin films have higher resistivity of 8.64×10^5 Ω.cm while n-CdTe thin films have lesser resistivity of 2.11×10^4 Ω.cm [23]. For semiconductor materials to possess higher mobility, they must have reduced resistivity according to the mathematical relationship $\left(\mu = 1/nq\rho\right)$ assuming the concentration of charge carrier is uniform. Due to the reduced resistivity in n-CdTe, the mobility of charge carriers in n-CdTe are generally higher than those of p-CdTe; this makes the electrons and holes generated after photon absorption to be quickly transported to the external circuits where they are collected for useful current generation [24]. Yang et al. [22] also reported higher resistivity and lower mobility for p-CdTe layers grown at potential of perfect stoichiometry (PPS). The authors observed a type conversion from p-CdTe to n-CdTe after annealing the PPS grown p-CdTe layer at 350^{o}C. For the converted n-CdTe layers, the authors reported higher electron mobility and reduced resistivity when compared to the p-CdTe.

The majority charge carriers in n-CdTe are electrons while the majority charge carriers in p-CdTe are holes; due to the higher mobility of electrons than holes [25], the level of R&G within the device structure having n-CdTe as the main absorber material is reduced and this can lead to enhancement in the output J_{sc} since most of the generated charge carriers are effectively separated and transported to external circuits before recombining with one another. The higher mobility values observed in n-CdTe may also be explained in terms of the effective mass of the charge carriers since the effective mass of hole is heavier than that of electrons in CdTe [26]. As explained by Sze and Ng, mobility increases with decrease in effective mass. The minimal value of effective mass in n-CdTe impact high thermal velocity to the charge carriers and this makes them to be less deflected by Coulomb scattering [27].

Another important difference between n-type CdTe and p-type CdTe can be seen in the location of their depletion region when these CdTe layers with different conductivity types are incorporated into solar cell device with the structure glass/FTO/CdS/CdTe/metal contact. Figs. 1a and 1b show the likely positions where depletion region can be formed when p-CdTe and n-CdTe are respectively used as absorber layer to n-CdS window layer. The depletion region occurs within the band bending region and it is also the area where the electric field is being built. The strength of electric field in this region determines how the photo-generated charge carriers would be separated and transported to the external circuits.

The device type formed from glass/FTO/n-CdS/p-CdTe/Au is known as the p-n junction device. The depletion region for this type of device is formed at the interface between the n-CdS and p-CdTe as illustrated in Fig. 1a. The device type formed from glass/FTO/n-CdS/n-CdTe/Au is known as Schottky barrier device. This type of device structure consists of interface from n-n heterojunction (HJ) and large Schottky barrier. The n-n HJ is formed between n-CdS and n-CdTe while the large Schottky barrier is formed between the n-CdTe and metal contact. The depletion region for this type of device is formed at the junction between the metal contact and the semiconductor. In most cases, the depletion region can extend from the n-CdTe into the n-CdS layer if the device structure is almost fully depleted as illustrated in Fig. 1b. The device structure glass/FTO/n-CdS/n-CdTe/Au can also be referred to as n-n+Schottky barrier (n-n+SB).

By comparing Fig. 1a with Fig. 1b, it could be seen that the probability of obtaining an almost fully depleted device is higher in n-n+SB than p-n device structure. A device which is almost fully depleted will experience low level of electron and hole recombination within the

device structure after the generation of the photo-generated charge carriers. For instance, the striking of a photon of adequate energy on the depletion area of the device structure generates electron and hole pairs. In both Figs. 1a and 1b, the electron moves towards the FTO electrical contact while the hole moves towards the Au electrical contact. This movement is facilitated as a result of the built-in electric field within the device structure. The region of the semiconductor material in the device structure where band bending does not take place is known as the neural region [28] and this region is known to contribute to the resistance of the bulk of the semiconductor material which make up the device structure. Thus the larger the neutral region, the more would be the resistance that the photo-generated charge carriers have to overcome for them to be successfully transported to the external circuits [29]. This resistance is likely to be more in the p-n junction device illustrated in Fig. 1a due to the presence of neutral region on both sides of the depletion region. If the photo-generated charge carriers are not able to overcome this resistance before getting to the external circuits, the chances of both generated electrons and holes recombining within the bulk of the material before getting to the external circuits would be high. This recombination can therefore lead to a reduced J_{sc} value in a p-n junction device.

In Fig. 1b, the neutral region only exists on one side of the depletion region (this side is to the left as illustrated in Fig. 1b. Either the device is fully depleted or not in n-n+SB device structure, the chances of electrons and holes recombining within the device structure is minimised. This is because holes are easily transported to the Au contact since there is no neutral region which can obstruct its movement. With the quick transportation of holes to the external circuit, the electrons are not able to easily recombine with holes after their generation. For an almost fully depleted device structure, the distance in which the photo-generated electrons would travel through would be small before getting to the external circuit. This means that for n-n+SB device structure, the resistance offered to the electron flow is small and this can make the electron to be transported with little or no obstruction to the FTO contact while the holes are quickly moved to the Au contact. This process thus leads to collection of more charge carriers at the output of device structure shown in Fig. 1b. With the collection of these charge carriers, the output J_{sc} of the n-n+SB can therefore be enhanced. This possibly explains one of the reasons why high J_{sc} values are observed in the n-n+SB device structures [24]. This same explanation can equally be applied to n-n-n+SB device fabricated from multi-junction graded bandgap solar cells with the structure glass/FTO/n-ZnS/n-CdS/n-CdTe/Au.

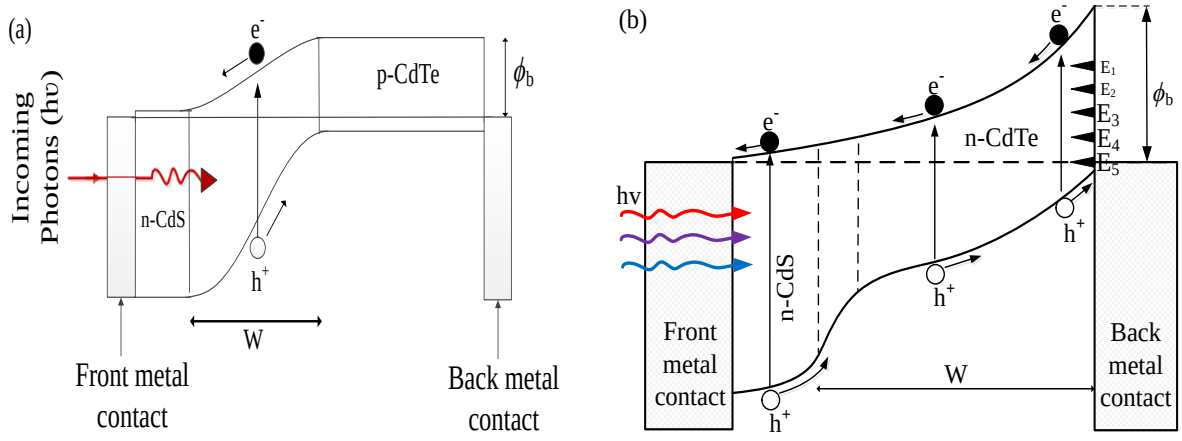

Fig. 1. Energy band diagram illustrating the position of depletion width formation in a typical (a) p-n junction solar cell based on n-CdS and p-CdTe and (b) n-CdS and n-CdTe (n-n) hetero-junction device structure with a large Schottky barrier at the metal back contact.

The optical properties of the semiconductor materials used in this work were explored using Carry 50 scan UV–Visible spectrophotometer (Varian Australia Pty. Ltd.). The structural properties were also investigated by using Philips PW 3710 X'pert Pro diffractometer (Philips Analytical, Almelo, The Netherlands) with Cu-K_α monochromator of wavelength, λ = 0.154 nm in the range of $2\theta=(20–70)^o$. The X-ray generator tension and current used were 40 kV and 40 mA respectively. A fully automated I-V system comprising of Keithley 2401 source meter with embedded power supply unit and solar simulators were used to assess the current-voltage (I-V) characteristics of the developed solar cells under AM1.5 illumination conditions.

2.1 Preparation of $GaCl_3$ and $CdCl_2$ solution for surface treatment before annealing

The initial $GaCl_3$ aqueous solution was prepared by using gallium (III) sulphate as Ga precursor and concentrated hydrochloric acid (HCl) acid as Cl precursor. 0.18 M of $Ga_2(SO_4)_3$ was prepared by adding ~1.06 g of $Ga_2(SO_4)_3$ into 35 ml of de-ionised water to produce an aqueous solution. 2.5 ml of concentrated HCl acid was later added to the prepared $Ga_2(SO_4)_3$ solution to initiate a reaction leading to gallium chloride ($GaCl_3$). Ga has the unique feature of reacting slowly with HCl acid to produce gallium chloride required for this treatment.

Saturated $CdCl_2$ aqueous solution was prepared by adding 0.15 M of $CdCl_2$ to 35 ml of de-ionised water. The $GaCl_3$ and $CdCl_2$ mixture were put together in 100 ml beaker and it was continuously stirred to obtain homogeneity before being used as surface treatment to CdTe thin films. Drops of the mixed solution were then applied to the top surface of the device structure with the aid of laboratory pipette and the solution was uniformly spread on the CdTe thin film surface. The device structure was allowed to dry in air before annealing inside a temperature controlled furnace. The initial device structures were subjected to different annealing conditions.

2.2 Chemical etchants used for device processing

After annealing in air, the device structures were allowed to cool down before chemically etching the top surface. The chemical etchants used are acidic etchants and alkaline etchants. Etching is usually carried out to remove any form of surface impurities on the layer; by so doing, a cleaner surface with reduced defects is being ensured. Surface contaminations such as oxides formed on the CdTe top surface during heat-treatment in air can be removed during etching process[30].

These two etchants can help in modifying the CdTe surface stoichiometry before metal contact evaporation. For instance, acidic etchants attack Cd preferentially and leave the CdTe thin films with a Te-rich surface while the alkaline etchants attack Te preferentially and leave a Cd-rich surface [31]. The acidic etchant was prepared by dissolving 1 g of potassium di-chromate ($K_2Cr_2O_7$) in 20 ml of deionised water; this was followed by the addition of 1 ml of concentrated H_2SO_4 acid into the prepared solution. The alkaline etchant was prepared by dissolving 0.5 g of NaOH and 0.5 g of $Na_2S_2O_3$ in 50 ml of de-ionised water. The alkaline etchant solution was heated up to a temperature of ~60^oC before being used. The device structures were dipped inside the acidic etchant solution for ~5 seconds after which they were removed and rinsed in de-ionised water before being transferred to the alkaline solution for etching. The alkaline etchant duration was ~120 seconds.

After performing the alkaline etching, the device structures were rinsed again in de-ionised water, dried with nitrogen gas before being transferred to the vacuum coating system for back contact metallisation. It is essential to quickly transfer the etched layers into the vacuum coating system to prevent the surface from oxidising. Oxidation of the top surface can be at times useful since it creates an insulating (I) layer between the metal and semiconductor [32]. If the created I layer is very thin, it can act as a de-coupler between the metal and

semiconductor and this tends to increase the band bending at the interface [33]. However, if the created insulating layer is very thick, it introduces additional series resistance to the solar cell device structures, decreases the short-circuit current density and causes a deterioration of the solar cell conversion efficiency [27]. The final stage of the solar cell device fabrication before device assessment is the deposition of Au back contact. The metal coatings were done using Edwards Auto 306 vacuum metalliser at a chamber pressure of 10^{-7} mbar. The diameter and thickness of the Au contacts are 2 mm and ~100 nm respectively. The solar cell active area is ~0.031 cm^2.

2.3 What happens when the top surface of CdTe layers are treated with Ga

As explained by Basol [14], the likely intrinsic defects in CdTe thin films are cadmium interstitials (Cd^i), cadmium vacancies (V_{Cd}), tellurium interstitials (Te^i) and tellurium vacancies (V_{Te}). Tellurium vacancies and cadmium interstitials act as donors while cadmium vacancies and tellurium interstitials act as acceptors. These donors and acceptors are all intrinsic in nature because they come mainly from the atoms that make up the semiconductor and not from external chemical elements introduced during growth, surface treatment or etching. Chu et al. [10] explained that triethylgallium (TEGa) can be used as an extrinsic dopant to change the electrical conductivity type of p-CdTe to n-type. The authors affirmed that one of the factors which determine the CdTe resistivity is the incorporation of Ga into Cd sites when TEGa is introduced as an extrinsic dopant into the MOCVD reaction chamber containing a mixture of dimethylcadmium and di-isopropyltellurium for CdTe formation. The explanation given by these authors showed the possibility of Ga occupying Cd sites. Similarly, Fernández [5] reiterated the possibility of Ga atoms to diffuse from Ga melt into the CdTe wafer during annealing of the wafers in Ga melt. Fernández [5] explained that when Ga diffuses into the CdTe wafer, the donor concentration is increased as a result of Ga atoms residing in Cd sites. Either Ga is used as a dopant or for treatment purpose to remove Te precipitates, Chu et al. [10] and Fernandez [5] both explained the possibility of Ga atoms being in Cd sites.

If the n-CdTe top surface is chemically treated with solutions containing trivalent atoms such as gallium (Ga), it is therefore possible for Ga being a trivalent atom to displace Cd in CdTe to form $Ga_{Cd}Te$. Two out of the three valence electrons in the Ga atoms are involved in forming covalent bonds with the six valence electrons of the neighbouring Te atoms. The remaining one negatively-charged electron which does not take part in bond formation

becomes free and available for conduction; this conduction electron is now donated to the crystal lattice in the conduction band. The Ga atom is therefore called a donor atom when it displaces Cd in its site due to its ability to give out a free electron for conduction. Fig. 2a shows the covalent bond formation that takes place between one Cd and Te valence atom while Fig. 2b illustrates the likely bond formation between the Ga and Te atoms after $GaCl_3$ surface treatment.

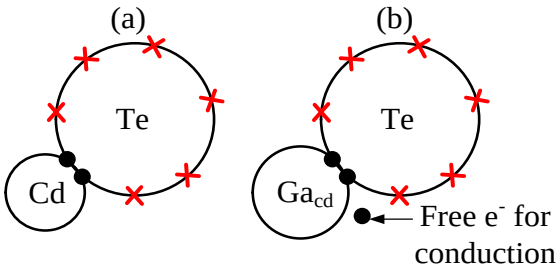

Fig. 2. Covalent bond formation between (a) Cd and Te atoms and (b) Ga occupying Cd sites and bonding with Te as a result of surface treatment.

3.0 Results and Discussion

3.1 Effect of different post deposition treatments on optical and structural properties of CdTe absorber layers

The effect of different treatment conditions have been studied on the optical and structural properties of CdTe thin films. For the optical study, the graph of absorbance square versus the photon energy is shown in Fig. 3 while the diagram in the inset of Fig. 3 shows the bar chart representation of how the bandgap changes with un-treated and treated CdTe thin films. Fig. 3 shows the optical absorption curves for as-grown CdTe thin films, CdTe films annealed in air without and with different chemical treatments. It can be seen that heat treatment affects the energy bandgap of the material. As reported by Dharmadasa et al. [17], energy bandgap is useful to design and develop PV devices to harvest photons effectively and achieve better performance.

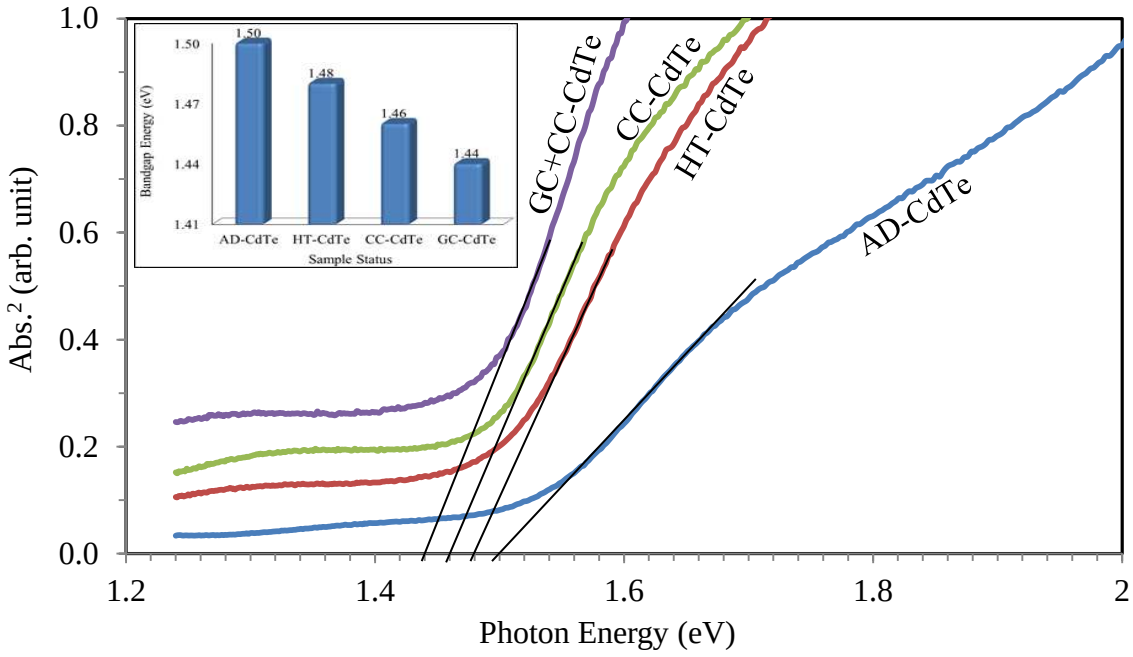

Fig. 3. Optical absorption analysis of as-deposited CdTe (AD-CdTe) thin films, heat-treated CdTe (HT-CdTe) thin films, CdTe layers annealed in the presence of $CdCl_2$ (CC-CdTe) solution only and in the presence of mixture of $GaCl_3$ and $CdCl_2$ (GC+CC-CdTe) solution.

Researchers have reported the energy bandgap of CdTe thin films to be in the range 1.44-1.50 eV [34,35]. This range of values has also been obtained in this experimental work. The estimated energy bandgap of the as-deposited CdTe material was ~1.50 eV and this value decreases to ~1.48 eV after annealing ordinarily in air with no chemical treatment. Annealing in the presence of $CdCl_2$ (CC) and mixture of $GaCl_3$+$CdCl_2$ (GC+CC) further reduces the bandgap to 1.46 and 1.44 eV respectively. As stated by Redwan et al. [36], the reduction in energy bandgap after annealing with or without $CdCl_2$ treatment is an indication of improvement of crystallinity in the thin film. Thus, the energy bandgap reduction observed in this work after annealing CdTe thin films with and without chemical treatments reveal that the crystallinity of the materials was enhanced after heat-treatment in air. The energy bandgap obtained in this work for CdTe layers annealed with a mixture of $GaCl_3$+$CdCl_2$ corresponds to the bandgap of bulk CdTe layers. By visually observing the spectra in Fig. 3, the optical absorption spectrum labelled GC+CC is the most absorbing spectrum and it has sharper absorption edges than the AD, HT and CC-CdTe thin films.

To further determine which of the CdTe post deposition treatment conditions give the highest absorption edge, the slope of each of the spectrum in Fig. 3 was determined. The result obtained from the absorption edge slope was plotted as a function of the four different post

deposition treatment conditions and the results are shown in Fig. 4. These post deposition treatment conditions will be referred to as sample status in this paper. In Fig. 4, the plot of energy bandgap versus sample status was also plotted on the same graph with absorption edge slope for comparison purpose and to deduce the relationship between absorption edge and energy bandgap (E_g).

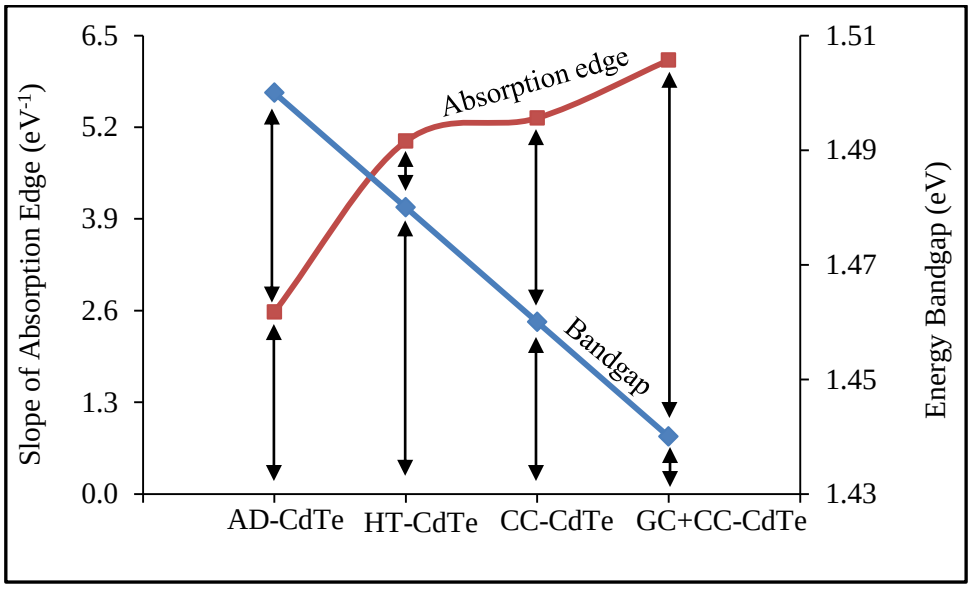

Fig. 4. Typical diagram illustrating the relationship between absorption edge slope and energy bandgap for AD-, HT-, CC- and GC+CC-CdTe thin films.

The result in Fig. 4 shows that GC+CC- treated CdTe films with the least E_g has the highest absorption edge slope while AD-CdTe films with the highest E_g has the least absorption edge slope. As seen from Fig. 4, the relationship between E_g and absorption edge slope is therefore an inverse type. As explained by Han et al. [37], semiconductor materials with sharper absorption edge will have lesser impurity energy levels and defects in the thin film. The explanation given by Han et al. [37] demonstrates the possibility of GC+CC-treated CdTe layers to have lesser defects. Another advantage of having a sharp absorption edge is that it allows more photons to be absorbed even when the CdTe thickness is of few microns [30]. This optical result therefore shows the possibility of having better solar cell efficiency if mixtures of $GaCl_3$ and $CdCl_2$ solutions are used in treating solar cell device structures. The larger bandgaps recorded in AD-CdTe thin films could arise as a result of quantum effects caused by smaller grains in the material [38,39] while the small slope of absorption edge can be due to presence of large defects in the as-deposited materials thus making them unsuitable for solar cells fabrication in its present form [37].

To investigate the structural properties of CdTe thin films, X-ray diffraction (XRD) and Raman analytical techniques were used. The XRD spectra of CdTe thin films grown on glass/FTO substrates are shown in Fig. 5. This study was carried out on AD-CdTe, CC-CdTe and GC+CC-CdTe. The as-deposited CdTe serves as the baseline to enable us distinguish the significant effects of chemically treating the top surface of the CdTe layers before annealing. The CC- and GC+CC- heat-treatments were carried out at 400^{o}C for 10 minutes in air. As seen in Fig. 5, the three CdTe spectra exhibit the prominent CdTe peak at 2θ within the range 23.92^{o} to 24.01^{o} along the (111) plane. The XRD peak along the (111) plane can therefore be referred to as the peak with most preferred orientation due to its highest intensity along this plane. The positions of angle 2θ and observed d-spacing values of the three CdTe spectra closely matches the reported values in the JCPDS reference file with code number 01-075-2086. CdTe with properties corresponding to this reference code have cubic crystal structure. Therefore the crystal phases of the AD-, CC-, and GC+CC-CdTe thin films are cubic.

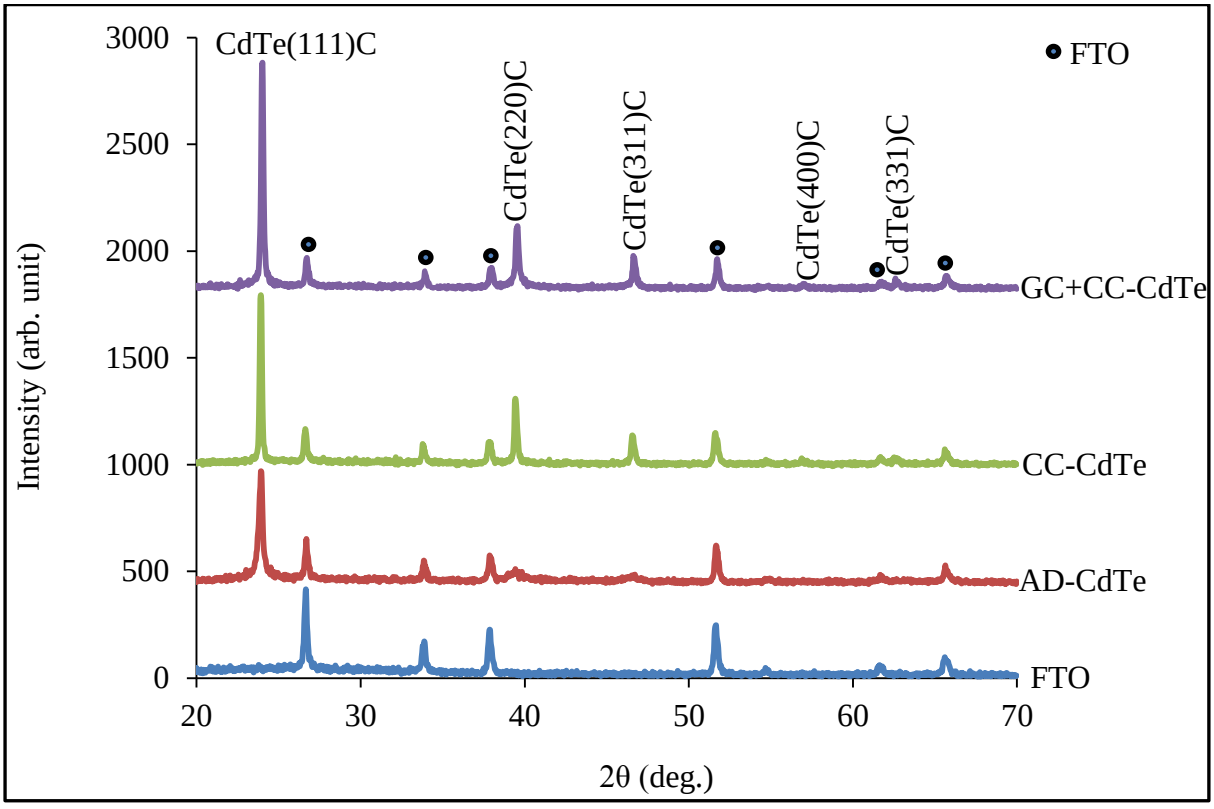

Fig. 5. Typical XRD spectra of as-deposited CdTe thin films, CdTe layers annealed in the presence of $CdCl_2$ solution only and in the presence of mixture of $GaCl_3$ and $CdCl_2$ solution.

The AD-CdTe thin films have three peaks at 2θ = 23.92^{o}, 39.43^{o}, 46.51^{o} along (111), (220) and (311) planes respectively. The XRD peaks along (220) and (311) planes are not so

significant as a result of its low peak intensity. However, all these peaks increased in intensity after annealing in the presence of chemical treatments. Tremendous improvements were seen in the (111), (220) and (311) peaks of CC-CdTe and GC+CC-CdTe after annealing with different chemical treatments. As illustrated in Fig. 5, CdTe thin films treated with a mixture of $GaCl_3$ and $CdCl_2$ have the highest peak intensity along (111) plane while as-deposited CdTe layers have the least peak intensity along the same plane. A plot of the (111), (220) and (311) peak intensities versus the sample status is shown in Fig. 6 to further demonstrate the significant contributions made by Ga addition into $CdCl_2$ solution. The high (111) peak intensity in GC+CC-CdTe is an indication of improved and higher crystallinity as compared to CC-CdTe and AD-CdTe thin films. It is a well-established fact in the literature that post deposition treatments using $CdCl_2$ solution improves the crystallinity of CdTe layers [17,36]. Our present investigation shows that the crystallinity of CdTe thin films can further be enhanced via a mixture of $GaCl_3$ and $CdCl_2$ treatment solution.

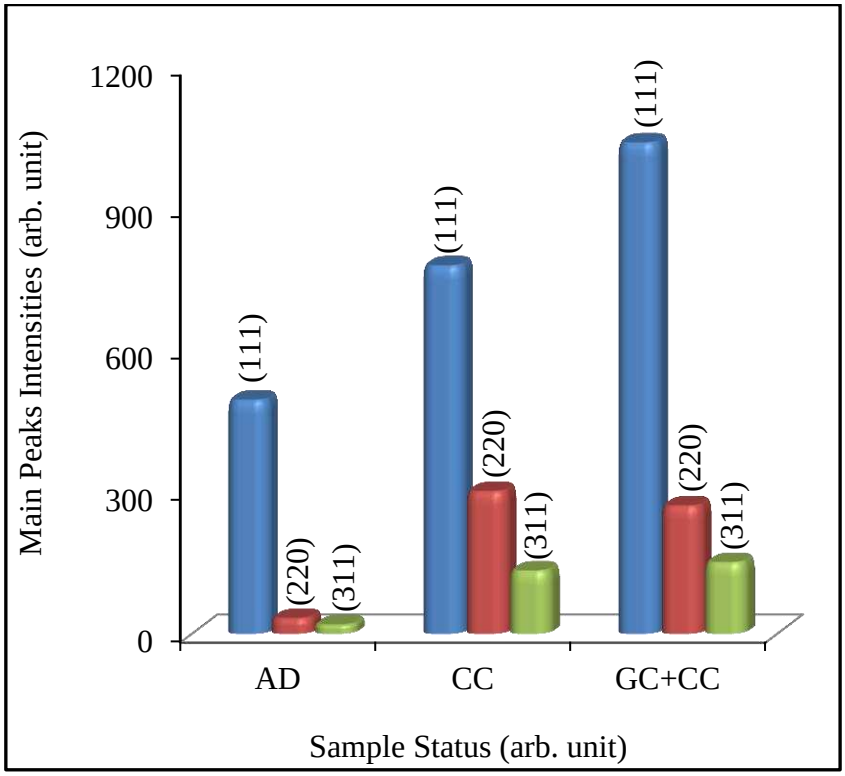

Fig. 6. Variation of three main peaks intensities versus different post growth conditions for CdTe thin films.

Two other weak peaks with cubic crystal structures absent in AD-CdTe were also observed along (400) and (331) planes of CC-CdTe and GC+CC-CdTe. The presence of these two peaks observed in CC-CdTe and GC+CC-CdTe demonstrate the crystallinity improvement

that accompanies annealing in the presence of chemical treatments. The XRD analyses of AD-, CC- and GC+CC-CdTe were carried out with respect to the (111) highly preferred orientation plane and the summary of results extracted from XRD measurements is shown in Table 1.

Table 1: Summary of XRD analyses of AD-, CC- and GC+CC-CdTe thin films along (111) preferred orientation plane.

Sample status	Position, 2θ (deg.)	d-spacing (Å)	FWHM (deg.)	Crystallite size (nm)	Peak intensity (arb. unit)	Crystal structure
AD_CdTe	23.92	3.72	0.1624	52.3	495	Cubic
CC_CdTe	23.92	3.72	0.1624	52.3	779	Cubic
GC+CC_CdTe	24.01	3.71	0.1299	65.4	1040	Cubic

The size of the crystallites (D) were estimated using the standard Scherrer's equation,

$$D = \frac{0.94\lambda}{\beta \mathrm{Cos}\theta} \quad (1)$$

where β is the full width at half maximum (FWHM) measured in radian, λ is the X-ray wavelength (0.154 nm) and θ is the Bragg's angle measured in degrees. The values of the crystallite sizes are also given in Table 1.

A sudden orientation change in CdTe thin films has recently been identified [17]. When heat-treated at 385 ± 5^{o}C, the grain boundaries melt and the randomisation of grains take place. At this point, intensity of (111) plane collapses and (220) and (311) peak intensities increase. However, further increase in temperature with $CdCl_2$ again increase (111) peak intensity; this trend has clearly been achieved in CC-CdTe samples. It is really interesting to observe further increase in (111) peaks for GC+CC-CdTe. This shows that CdTe layers improve much better in the presence of $GaCl_3$ and $CdCl_2$. Therefore, the device performance should improve with Ga addition.

The Raman results obtained for AD-, CC- and GC+CC-CdTe thin films are illustrated in Fig. 7. The peaks of the Raman spectra were observed at 123 cm^{-1}, 140 cm^{-1}, 165 cm^{-1}and 328 cm^{-1} Raman shift. The peaks at 123 cm^{-1} correspond to elemental Te vibrations while the two

phonon modes at 165 cm^{-1} and 328 cm^{-1} arise as a result of vibrations from CdTe thin films. The Raman peaks at 140 cm^{-1} signify mixed phases which comprises of E(Te) + TO(CdTe). This peak cannot be used as blueprint to notice the trend of changes in material crystallinity as a result of the overlap. Elemental Te peak at wave numbers 123 cm^{-1} is most prominent in the as-deposited CdTe sample. The presence of this peak shows the un-suitability of as-deposited CdTe semiconductor materials for device fabrication because of the defects being introduced by Te precipitates [8]. After chemically treating the CdTe layer with $CdCl_2$ and mixture of $GaCl_3$+$CdCl_2$, it was observed that the 123 E(Te) was almost totally eliminated. Also, there was an enhancement in the peak intensities of CdTe Raman peaks at wavenumbers corresponding to 165 $cm^{-1}$and 328 cm^{-1}. The drastic reduction of elemental Te peak at 123 cm^{-1} and enhancement of 1LO and 2LO CdTe modes at 165 cm^{-1} and 328 cm^{-1} respectively show one of the improvements brought about by CC- and GC+CC chemical treatments.

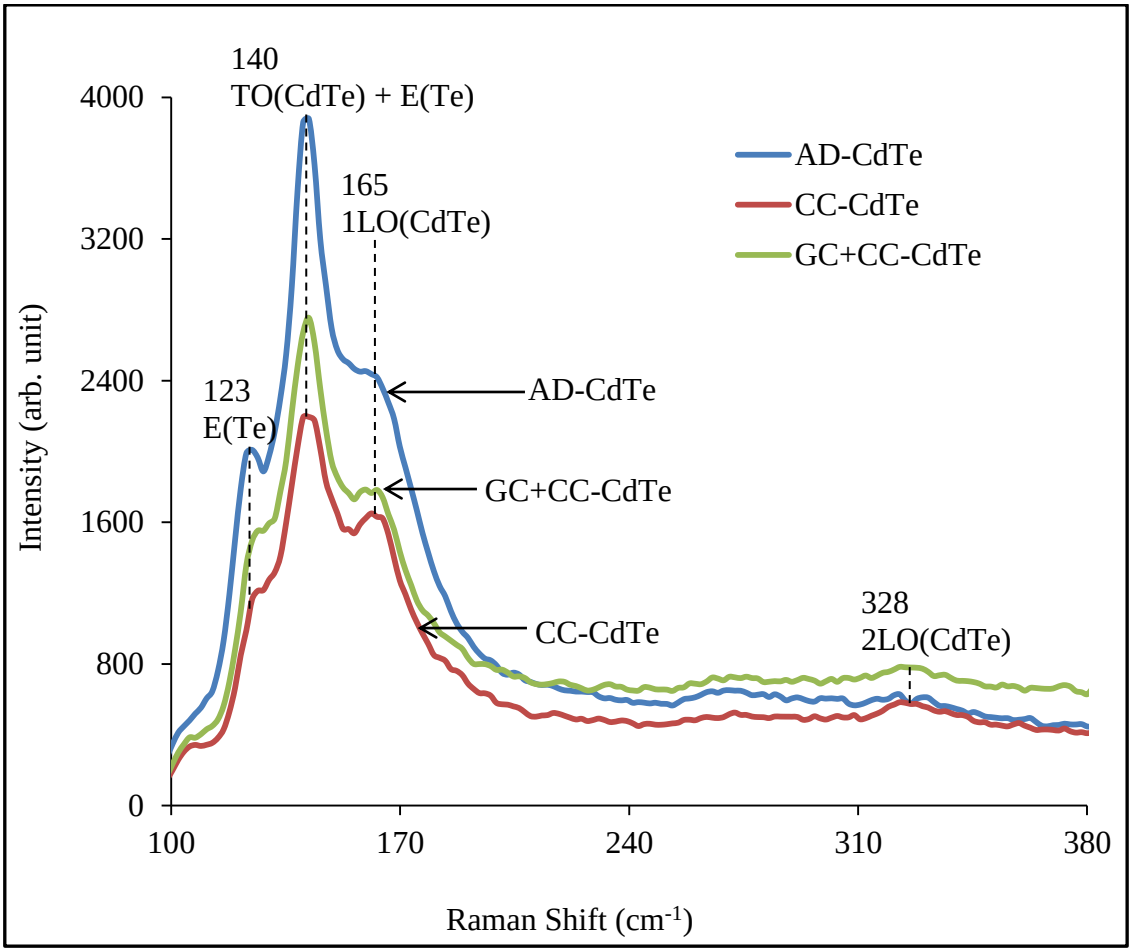

Fig. 7. Raman spectra obtained for AD-, CC- and GC+CC-CdTe layers. Note the reduction of elemental Te peak at 123 cm^{-1} and enhancement of 1LO CdTe peak at 165cm^{-1} after $CdCl_2$ and mixture of $GaCl_3$ + $CdCl_2$ surface treatment.

3.2 Assessment of glass/FTO/n-CdS/n-CdTe/Au solar cells

Table 2 shows the summary of I-V parameters obtained under AM1.5 illumination conditions for glass/FTO/n-CdS/n-CdTe/Au solar cells. For each experimental set, several cells were fabricated but for comparison purpose, the best cell was selected from the different post deposition treatment conditions for comparison purpose. The thickness of CdS and CdTe thin films used in this experiment are ~150 nm and 1.5 µm respectively. The annealing temperature and time for samples in Table 2 are 450^{o}C and 10 minutes in air. These initial solar cells were fabricated using three different heat-treatment conditions namely heat-treatment ordinarily in air (HT), annealing in the presence of $CdCl_2$ solution only (CC) and annealing in the presence of $GaCl_3$ solution only (GC).

Table 2: Solar cell parameters obtained from CdTe layers treated with different conditions.

Samples	Measured solar cell parameters					
Sample status	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	R_s (Ω)	R_{sh} (Ω)
HT	300	4.0	0.24	0.29	3185	2444
CC	300	17.5*	0.27	1.42	732	842
GC	300	3.1	0.35*	0.33	1911	10350

The efficiencies obtained from this initial work are generally very poor; however, it could be seen that each of the treatment used played a key role in improving some of the solar cell parameters. For instance, with reference to Table 2, it was observed that solar cells made from device structures treated with $GaCl_3$ only had the highest FF while the highest J_{sc} was observed in the device structures treated with $CdCl_2$ only. Overall, the lowest efficiency was observed in the solar cells fabricated from samples that were not subjected to any chemical treatment before annealing.

The series resistance and shunt resistance of each of these cells were also measured under AM1.5 illumination conditions. The HT-device structure was found to have the highest R_s. After $GaCl_3$ treatment, a reduction was observed in the R_s from 3185 Ω to 1911 Ω. The application of $CdCl_2$ reduces the R_s value from 3185 Ω to 732 Ω. The reduction of R_s value after $CdCl_2$ treatment in this work agrees with the explanation given by Rohatgi et al. [12] on

how $CdCl_2$ treatment brings about a reduction in R_s. The presence of low R_s in CC-device structure is one of the contributing factors which led to its J_{sc} improvement as compared to HT- and GC-device structures. The highest R_{sh} value was observed in GC-device structure; this value is more than four times and twelve times higher than the R_{sh} values observed in HT- and CC-device structures respectively. It is a well-known fact that low R_{sh} and high R_s values cause a significant reduction in FF. Therefore, the improvement in FF of CC-device structure as compared to the HT-device structure can be explained in terms of its lower R_s value while the much better FF observed in GC-device structure with respect to other treatments can be attributed mainly to increased R_{sh} value.

The result from this initial work led to the decision made in using a mixture of $GaCl_3$ and $CdCl_2$ solution for surface treatment in the subsequent experimental investigations reported in this paper. Based on the initial work, it is expected that the mixture of $GaCl_3$ and $CdCl_2$ solution would enhance all solar cell parameters. The J-V curves of the cells described in Table 2 are shown in Fig. 8.

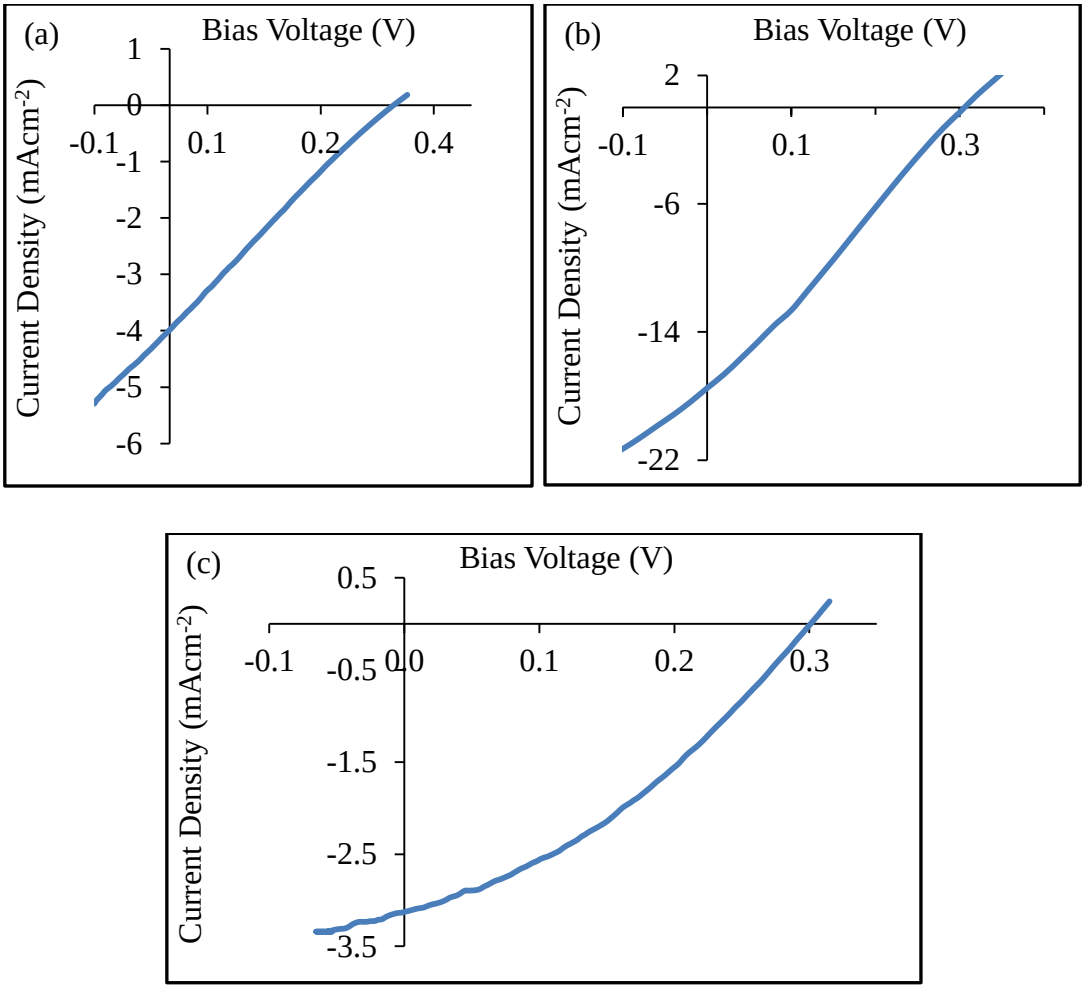

Fig. 8. Typical J-V curves obtained for solar cells fabricated from samples annealed (a) ordinarily in air, (b) with $CdCl_2$ treatment only and (c) with $GaCl_3$ treatment only.

3.3 Investigating the effect of $GaCl_3$ inclusion into the usual $CdCl_2$ treatment on glass/FTO/n-CdS/n-CdTe/Au device structures

The annealing temperature of 450^{o}C was discontinued for the n-n heterojunction device structure due to the reduced V_{oc} observed in the initial work. The experimental investigations carried out by Abdul [40] showed that 450^{o}C may not be suitable for device processing. The author's work showed that chemically treated device structures processed at high annealing temperature of 450^{o}C showed a huge reduction in V_{oc} and FF when compared to device structures processed at annealing temperature of 400^{o}C. The J_{sc} values obtained at 400^{o}C and 450^{o}C by the author for the different chemical treatments showed that the results are comparable with each other [40].

Table 3 shows the summary of I-V parameters obtained under AM1.5 illumination conditions for CdS/CdTe device structures annealed under different chemical treatment conditions. The

thickness of CdS and CdTe thin films used in this experiment are ~150 nm and 2.0 µm respectively. The chemical treatments employed here are: $CdCl_2$ only and mixture of $GaCl_3$+$CdCl_2$ (GC+CC). From each device structure, a typical cell has been selected for comparison purpose. The summary of the device parameters obtained for this set of device structures are illustrated in Table 3. The annealing temperature and time for samples in Table 3 are 400^{o}C and 15 minutes respectively.

Table 3: Summary of solar cell parameters fabricated from CdS/CdTe-based device structures annealed in the presence of $CdCl_2$ and $GaCl_3$+$CdCl_2$.

Samples	Measured solar cell parameters					
Sample status	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	R_s (Ω)	R_{sh} (Ω)
CC	600	14.5	0.24	2.1	2844	4363
GC+CC	600	33.5	0.32	6.4	386	3599

As expected, drastic improvements were seen in solar cells fabricated from device structures treated with Ga incorporation into $CdCl_2$ solution when compared to solar cells fabricated from device structures treated only with $CdCl_2$. These experimental results show that mixture of $GaCl_3$+$CdCl_2$ solution would be an effective means of treating CdTe top surface prior to metal evaporation. The reason for the improvement in device structures treated with chemical solutions containing Ga, Cd and Cl ions can be attributed to the ability of the trio to remove Te precipitates, reduce structural defects and doping effects [5]. Further experimentation on Ga inclusion is in progress.

Removal of Te precipitates can take place when CdTe thin films are deposited or when their surfaces are treated in a medium containing Cd or Cl ions [41,42]. As previously explained in section 1.0 and reported by Sochinskii et al. [7] and Fernandez [5], Te precipitates can also be successfully removed after annealing CdTe in Ga melt and Cd vapour media. Therefore, getting a solution containing Ga^{3+}, Cd^{2+} and Cl^- would be an effective means of removing Te precipitates. Te precipitates have been reported by researchers to be detrimental to CdTe-based solar cell performance [43,44].

As observed in the initial work discussed in section 3.2, a remarkable improvement was seen in the FF of device structures treated with $GaCl_3$ solution while $CdCl_2$ treatment drastically improves the J_{sc}. By combining the two chemical treatments together, a great improvement in

all solar cell parameters was observed in Table 3 when compared to the initial results stated in Table 2. As seen in Table 3, drastic improvements were observed in J_{sc} and FF of samples treated with chemical solutions containing Ga^{3+}, Cd^{2+} and Cl^{-}. This improvement can be mainly attributed to the complementary efforts of these three ions to effectively combat Te precipitates. As discussed in section 3.1, CdTe thin films which were chemically treated with mixture of $GaCl_3$+$CdCl_2$ produced bandgap which corresponds to the energy bandgap of bulk CdTe thin films, sharpest absorption edge and highest crystallinity when compared with CdTe thin films treated only with $CdCl_2$. The excellent collective features displayed by the $GaCl_3$+$CdCl_2$-treated CdTe layers thus enhance the transportation of mobile charge carriers across the device structure. This is therefore one of the likely reasons why solar cells fabricated from $GaCl_3$+$CdCl_2$-treated device structures with CdTe as an absorber layer showed improved solar cell parameters especially in the J_{sc} and FF. It could also be observed from Table 3 that the incorporation of Ga into $CdCl_2$ treatment solution has helped in further reducing the R_s as seen from sample GC+CC treated device structures. The J-V curves of the two cells stated in Table 3 are diagrammatically shown in Fig. 9.

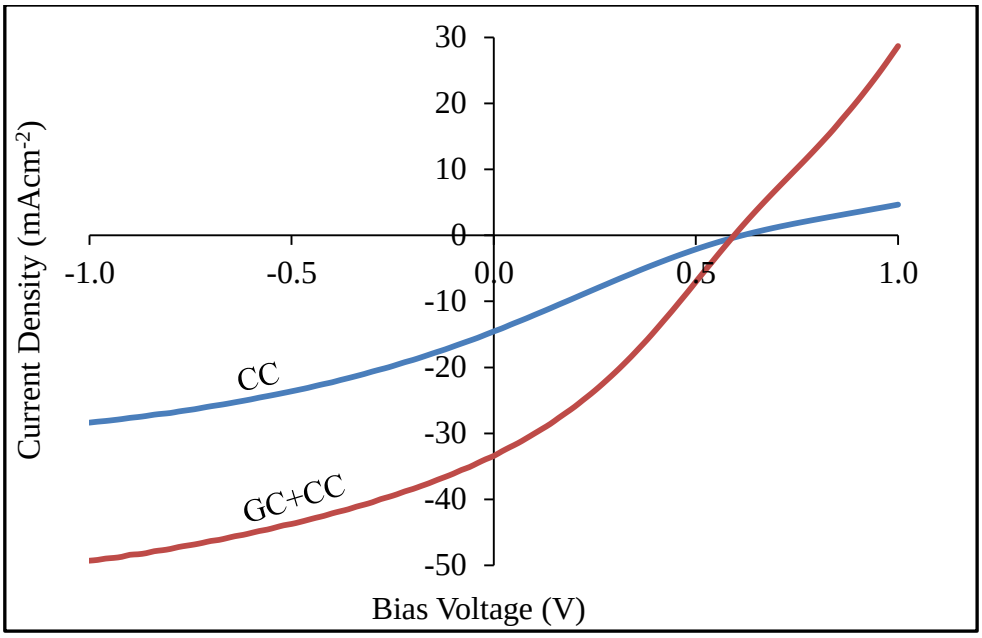

Fig. 9. Short-circuit current density versus voltage curves obtained for selected solar cells fabricated from samples annealed (a) with $CdCl_2$ treatment only and (b) with $GaCl_3$+$CdCl_2$ treatment.

3.4 Investigating the effect of $GaCl_3$ inclusion into the usual $CdCl_2$ treatment on glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structures

Similar experiments carried out in section 3.3 on glass/FTO/n-CdS/n-CdTe/Au device structure was repeated for multi-junction graded bandgap solar cells with the device structures glass/FTO/n-ZnS/n-CdS/n-CdTe/Au. These experiments were carried out as a result of the previous work reported by Echendu et al. [45] that multi-junction graded bandgap solar cells produced better efficiency than two-layer device structures fabricated from glass/FTO/n-CdS/n-CdTe/Au. The summary of device results obtained from multi-junction graded bandgap solar cells are illustrated in Table 4. Both CC- and GC+CC-treated samples have reduced R_s and increased R_{sh} value as compared to the previous results discussed in Table 3. This improvement can be mainly attributed to the presence of ZnS which acts as a buffer layer and also partake in the grading of the device structure. The effect of Ga incorporation into the $CdCl_2$ treatment could also be seen in the R_s reduction from 306 Ω to 185 Ω and R_{sh} slight increment from 7582 Ω to 7962 Ω. The lower R_s and high R_{sh} values obtained in GC+CC device structures all contribute to the efficiency improvement from ~6.7% for CC-treated device structures to ~10.2% for GC+CC-treated device structures. The J-V curves of the two cells are plotted on same graph for comparison purpose as shown in Fig. 10.

Table 4: Summary of multi-junction graded bandgap solar cell parameters obtained from device structures (glass/FTO/n-ZnS/n-CdS/n-CdTe/Au) annealed in the presence of $CdCl_2$ and $GaCl_3$+$CdCl_2$.

Samples	Measured solar cell parameters					
Sample status	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	R_s (Ω)	R_{sh} (Ω)
CC	620	28.5	0.38	6.7	306	7582
GC+CC	620	34.1	0.48	10.2	185	7962

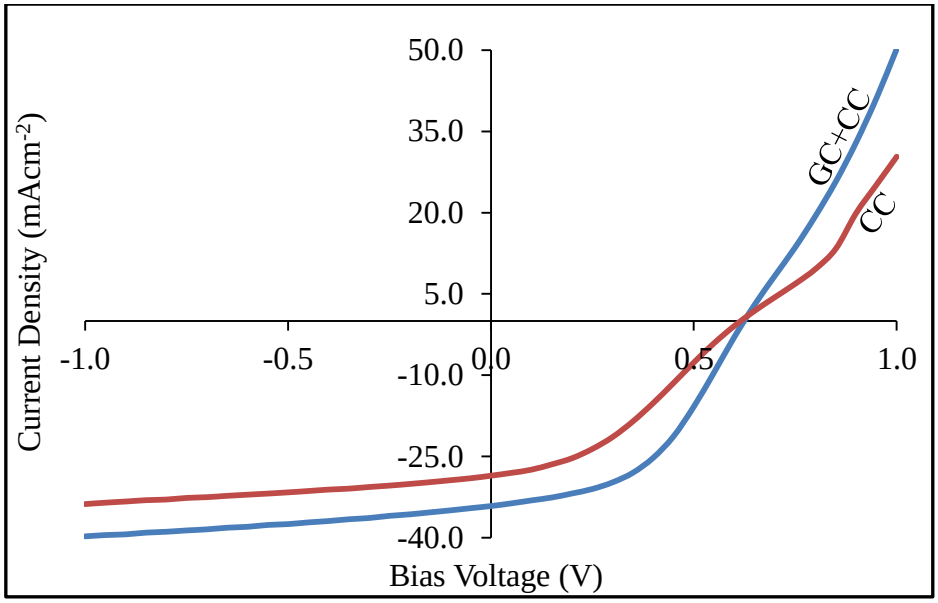

Fig. 10. Short-circuit current density versus voltage curves obtained for selected multi-junction solar cells fabricated from samples annealed (a) with $CdCl_2$ treatment only and (b) with $GaCl_3$+$CdCl_2$ treatment.

Conclusion

The positive effects of Ga incorporation into the usual $CdCl_2$ treatment have been demonstrated on the opto-electronic properties of CdTe-based device structures. The results presented in this work showed that CdTe thin films and solar cell device structures treated with mixture of $GaCl_3$+$CdCl_2$ exhibit better performance in terms of electronic device quality than CdTe-based device structures treated only with $CdCl_2$. The inclusion of Ga into $CdCl_2$ solution has been seen to aid the reduction of series resistance thus leading to enhancement in short circuit current density and fill-factor. This improvement in solar cell parameters demonstrate the ability of Ga^{3+}, Cd^{2+} and Cl^- in the $GaCl_3$+$CdCl_2$ solution to effectively reduce Te precipitates which contribute to the recombination and generation of photo-generated charge carriers in the device structure. It was noticed that the open-circuit voltage of solar cells annealed at 400^{o}C is almost twice that of solar cells annealed at 450^{o}C while the open-circuit voltage remains fairly the same for most of the measured solar cells under different chemical treatment conditions. Even though chemical treatments may also affect the open-circuit voltage, this result explains the possibility of open-circuit voltage to be strongly dependent on annealing temperature rather than the chemicals used for surface treatment.

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