Model Based Design and Auto Coding of an FPGA Based Satellite Control System
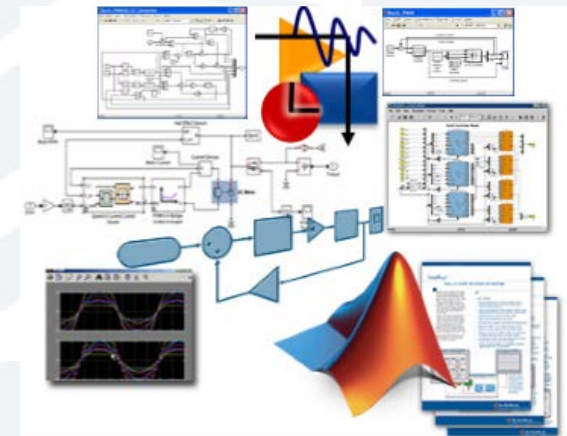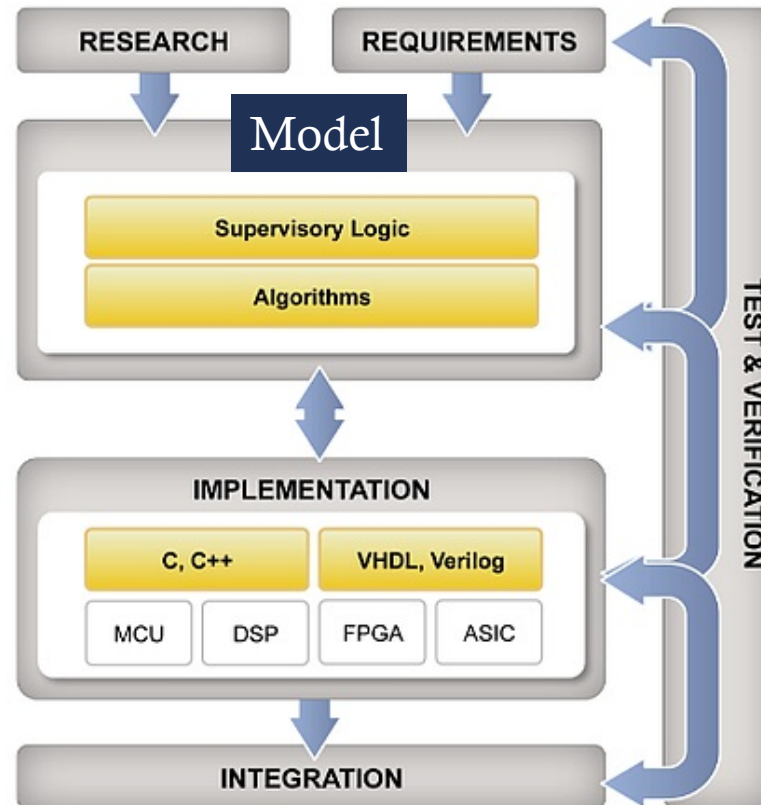
Jorden Luke

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What is Model Based Design?
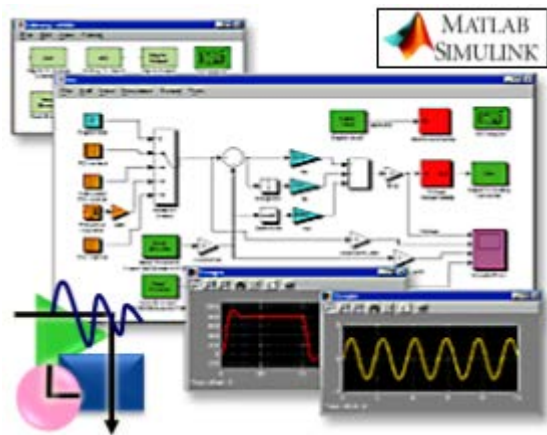
Traditional design process

1. An expert creates a high level computer simulation: Control system, commutation, etc.

2. Engage with a firmware developer/expert to code model to FPGA hardware.

3. Lots of back and forth between these two experts.

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FPGA Implementation

❧ Simulink is often used to model the spacecraft system

   ❧ Instrument control

   ❧ ADCS subsystem

❧ The programmer often creates diagrams of the FPGA functionality required

❧ Text entry of the system in a descriptive language like HDL

❧ Synthesis tools take HDL code and place on an FPGA

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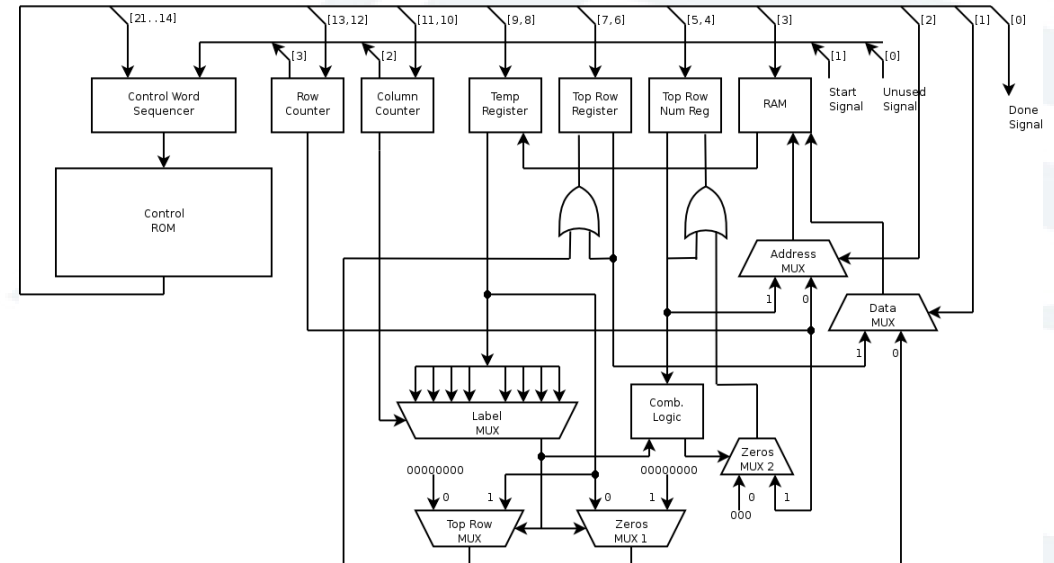
Model Direct Implementation

Model Based Auto coding

1. Expert creates a model.

2. Expert generates FPGA code from model.

3. Expert deploys code to hardware.

4. Expert confirms that model is working properly on hardware.

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Why FPGA for Small Sats?

൪ Ease of Parallel and real time
   processing.

൪ Low power.

൪ Radiation Tolerance.

൪ Advanced Computational
   Capabilities.

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Simulink/HDL Coder

℘ Simulink
- ℘ Block level design
- ℘ Arithmetic functions (filters, FFT's)

℘ State flow
- ℘ Logic flow (if then else)
- ℘ State Machines

℘ HDL Encoder
- ℘ Auto codes both to HDL
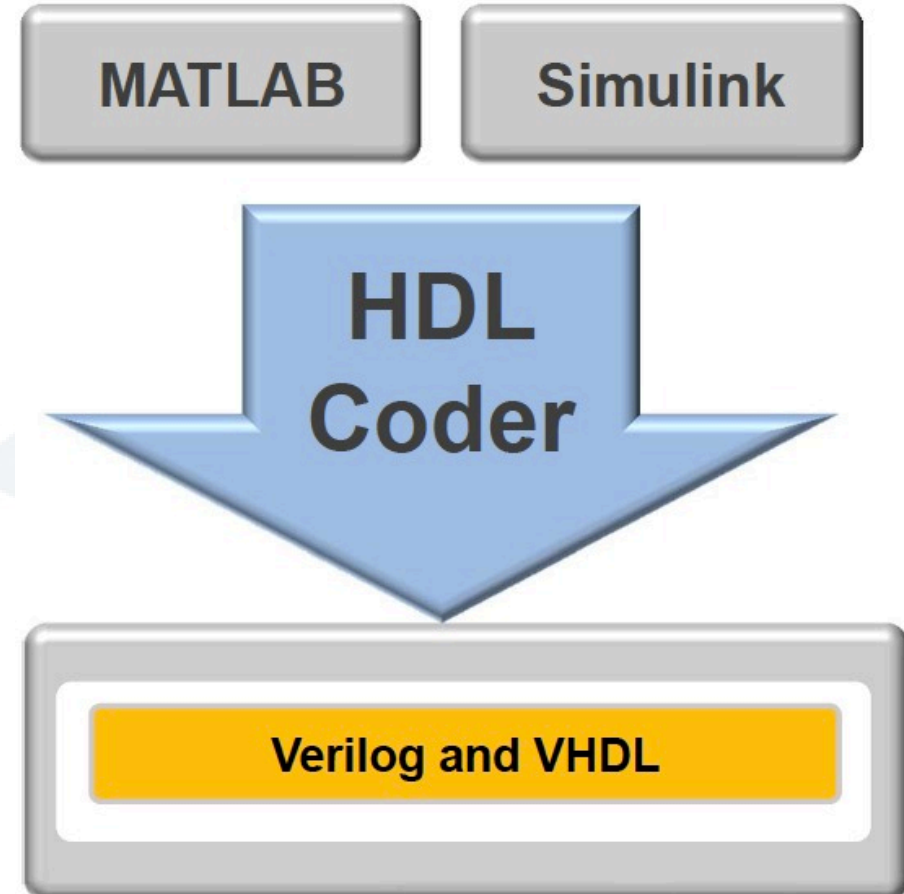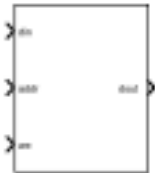
MATLAB   Simulink

HDL Coder

Verilog and VHDL

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HDL Coder Blocks
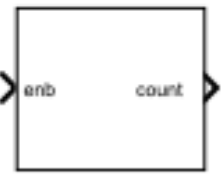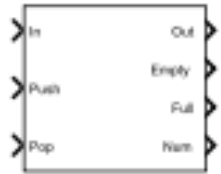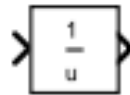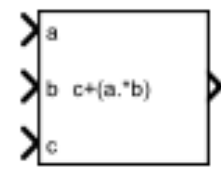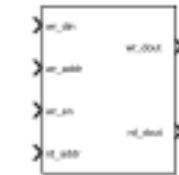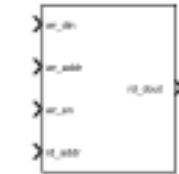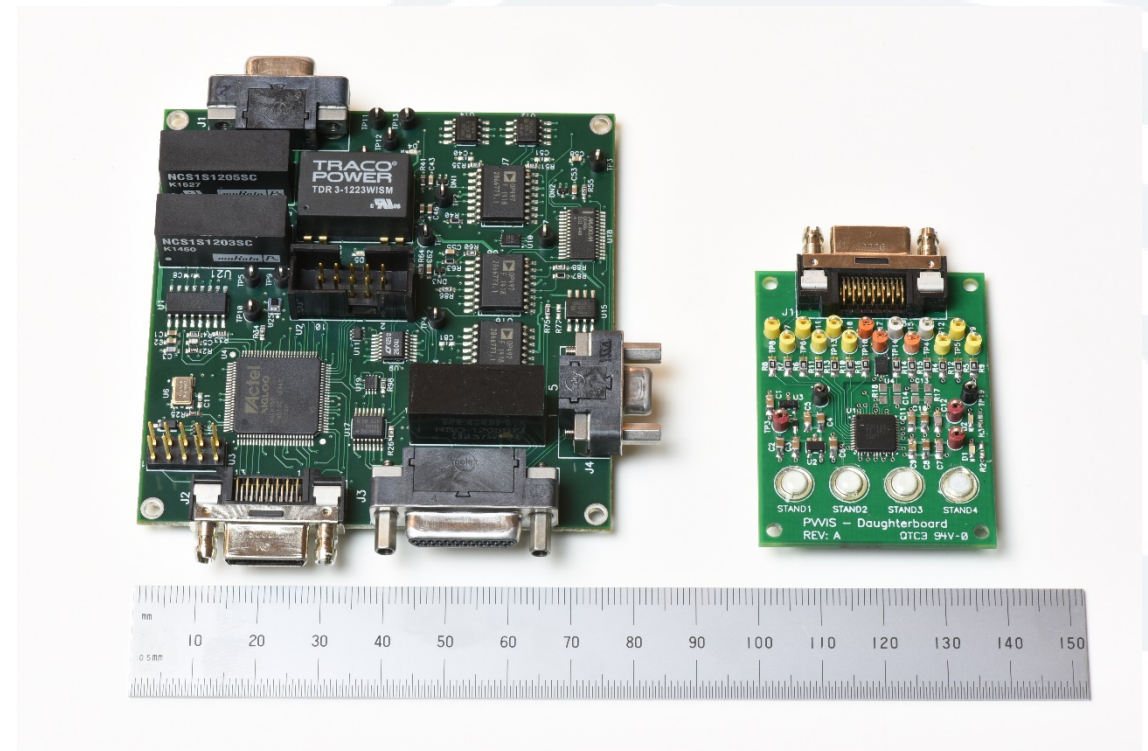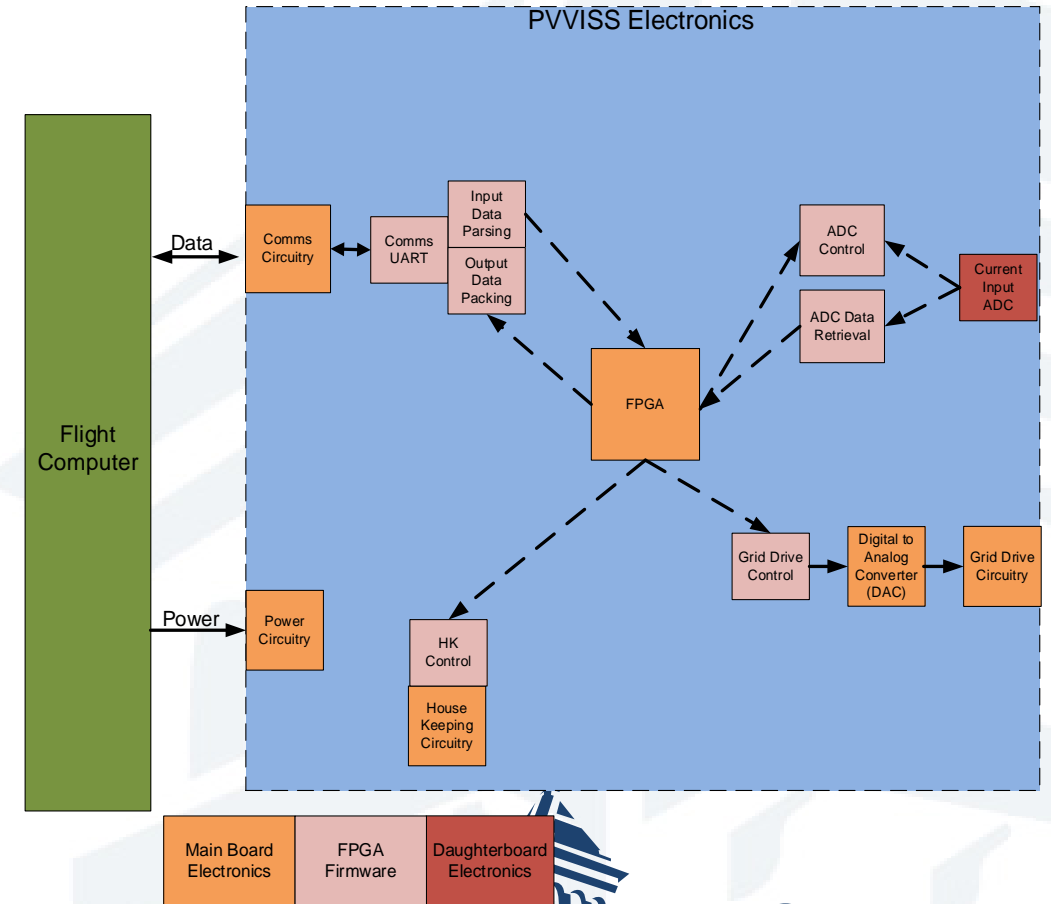
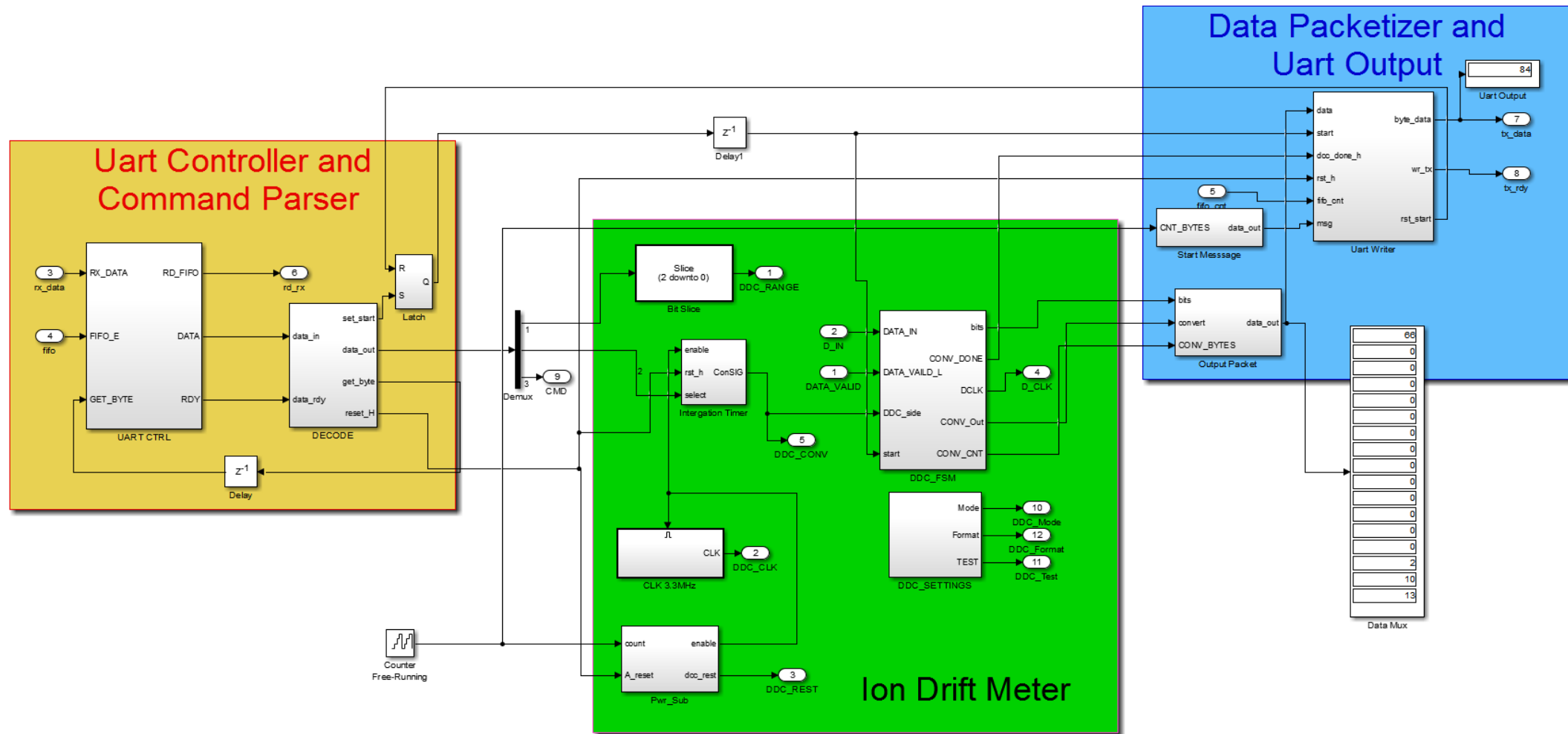# Where we are using this process
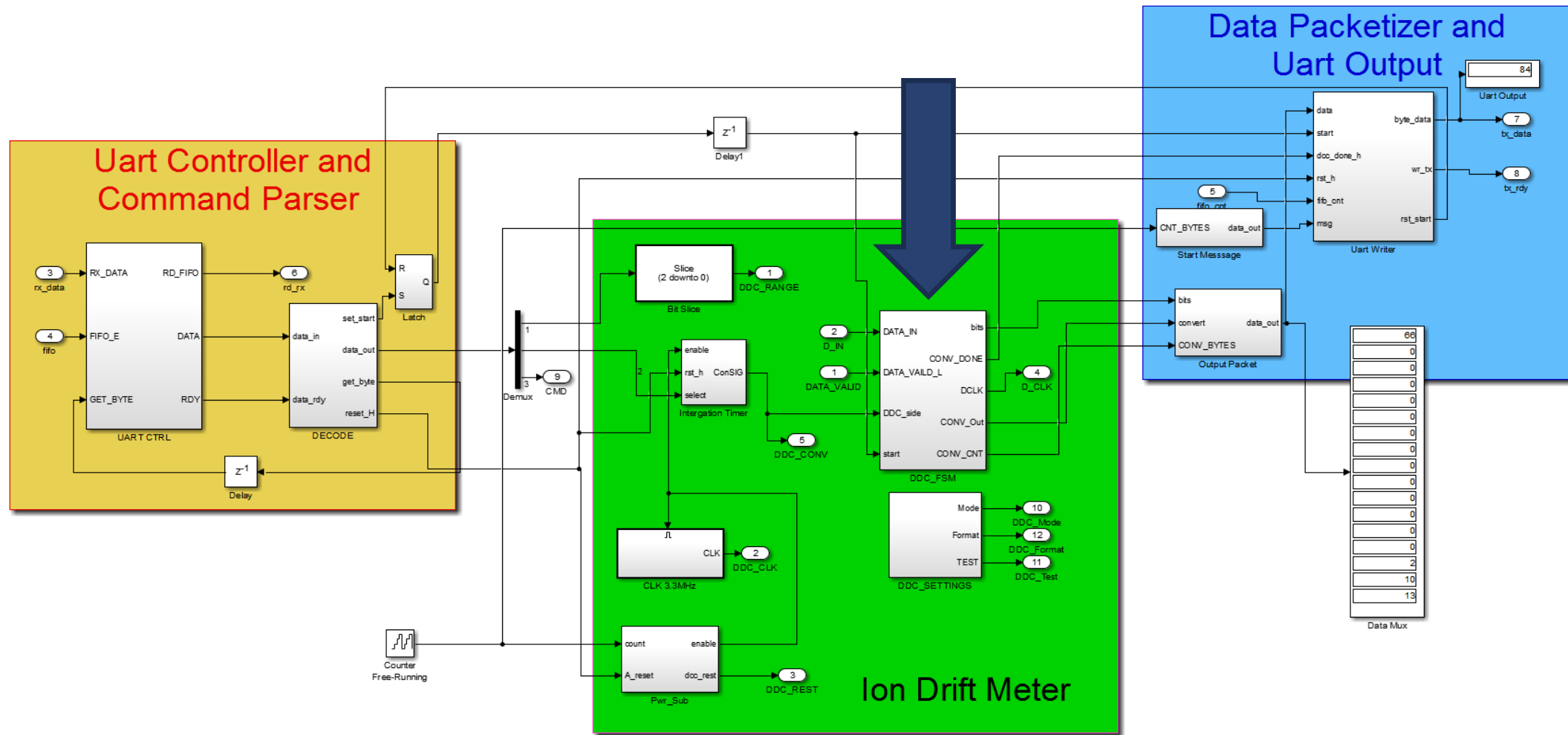
ADCS
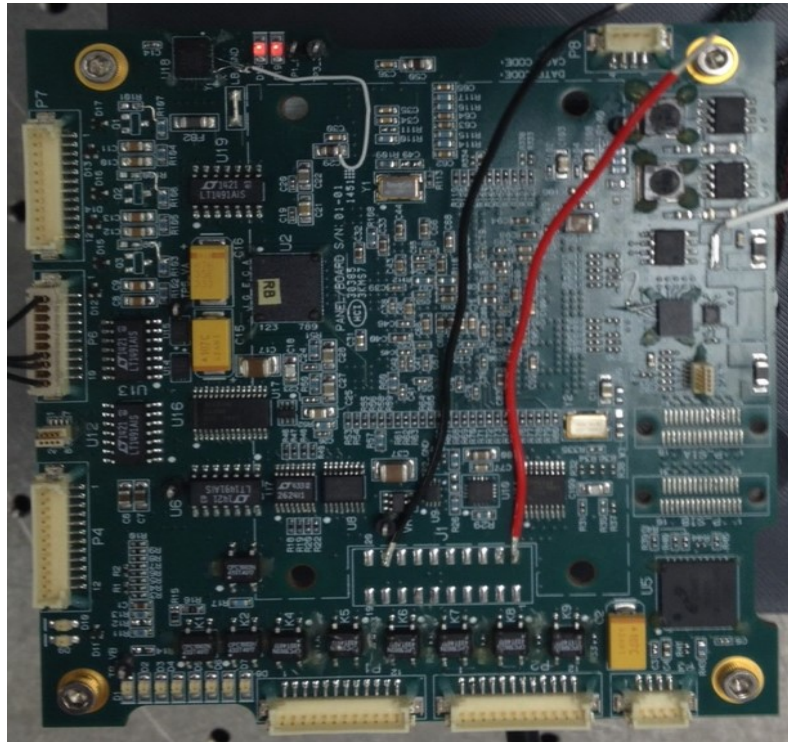
Ion Drift Meter

Ion Drift Meter Hardware

- FPGA Microsemi Igloo
  - Control Instrument
  - Packetizes Data

- Ion Drift Meter
  - Designed to measure currents down to femto amps
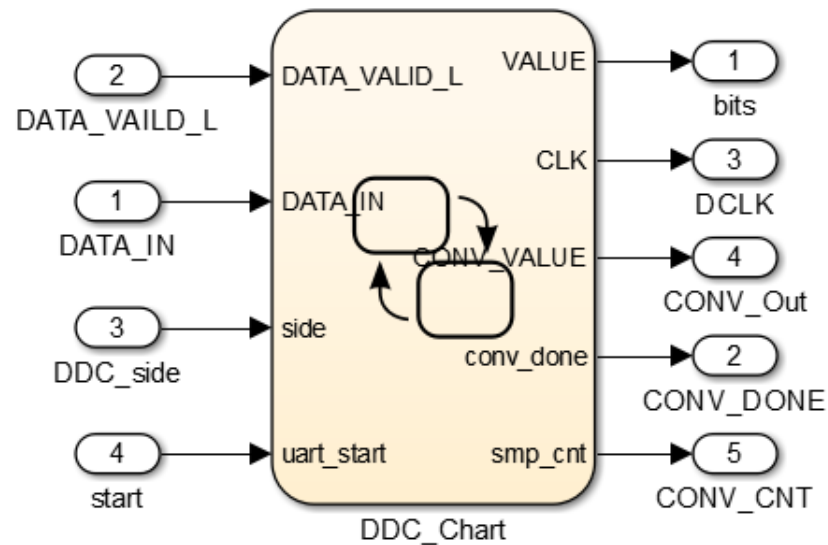

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The Drift Meter Simulink Model

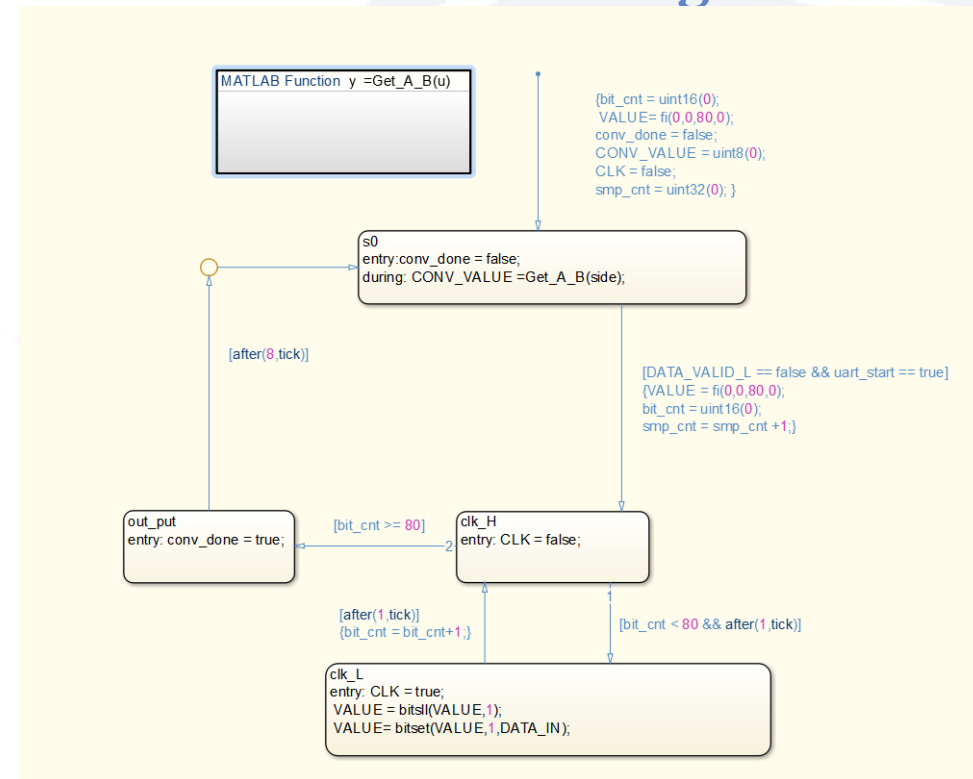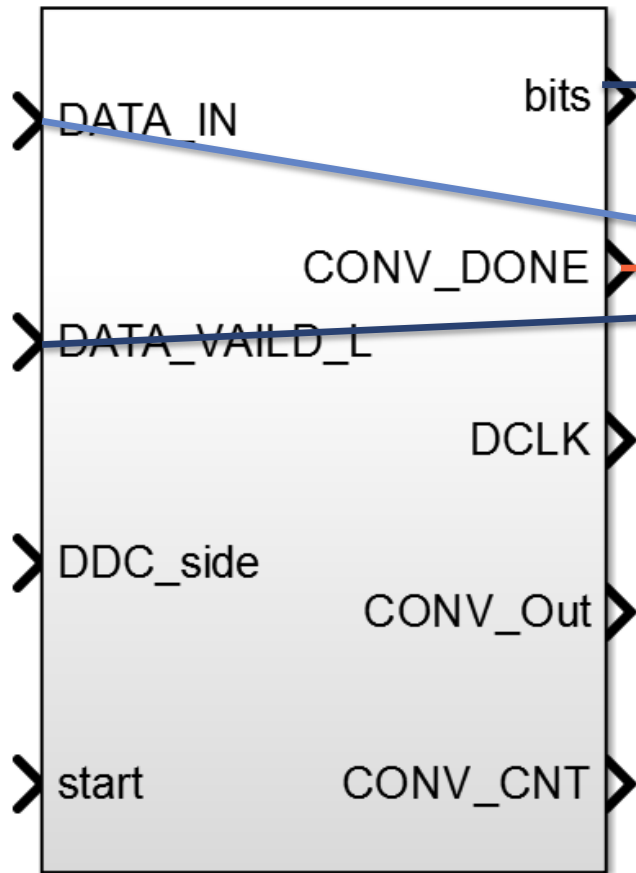# The Drift Meter Simulink Model

Inside Look at the DDC FSM

DDC Chart

State Flow Diagram

Generated Code Vs Model

Outputs From Scopes

Simulink Scope

Bit Scope

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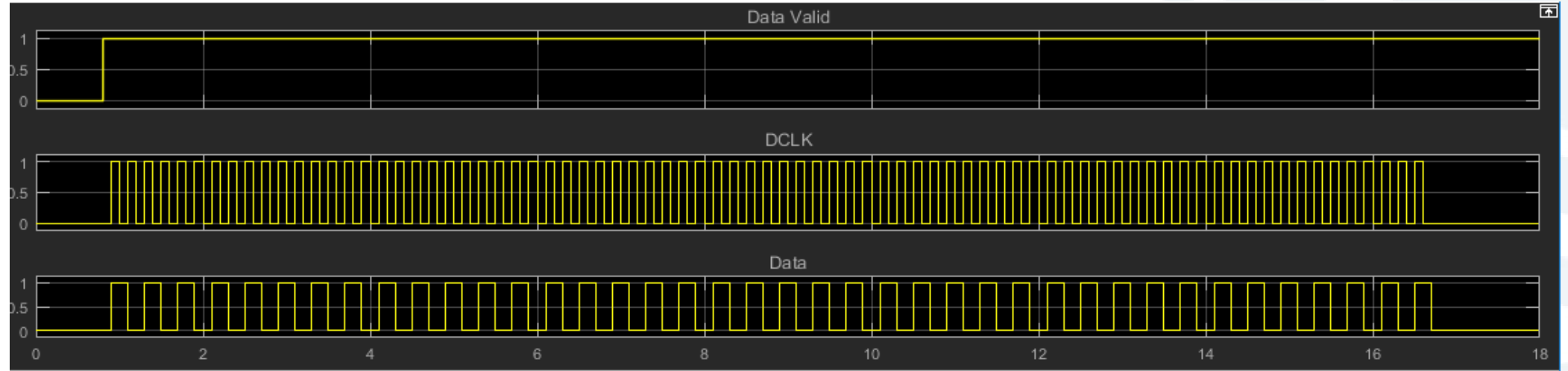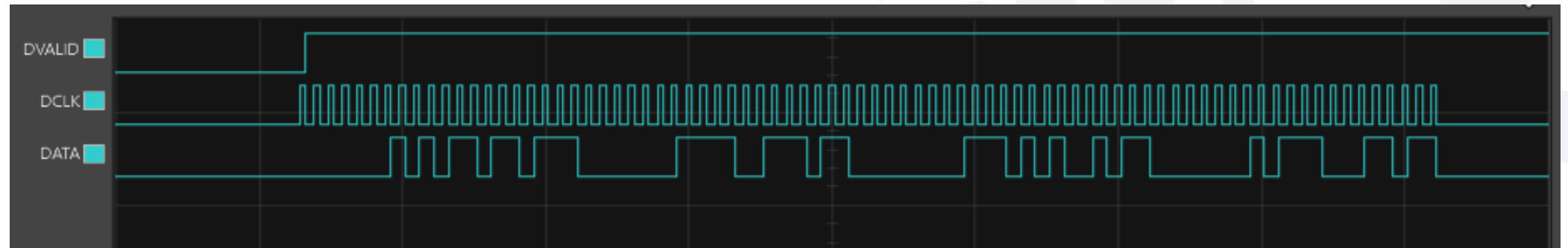
Synthesized Model
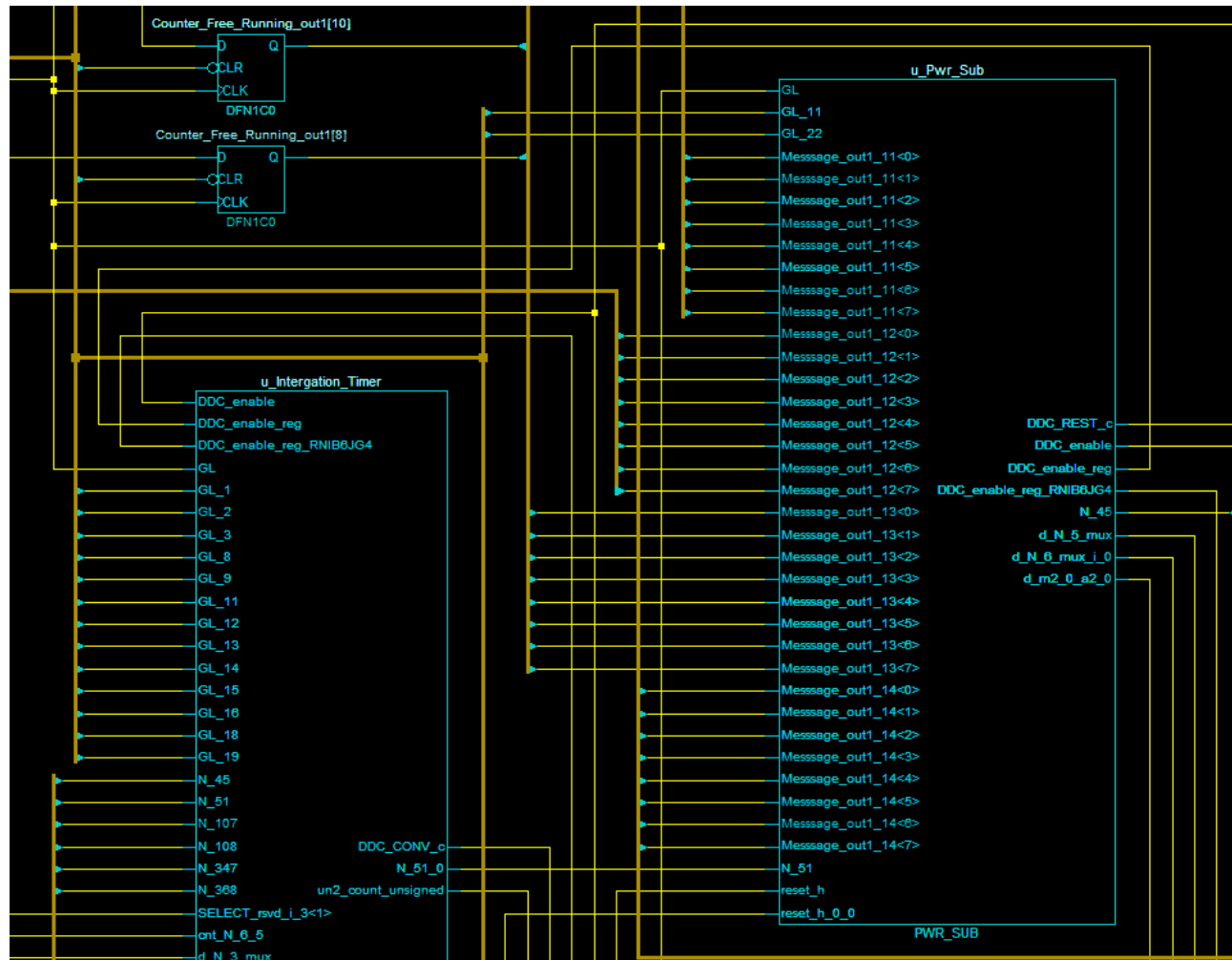
Results

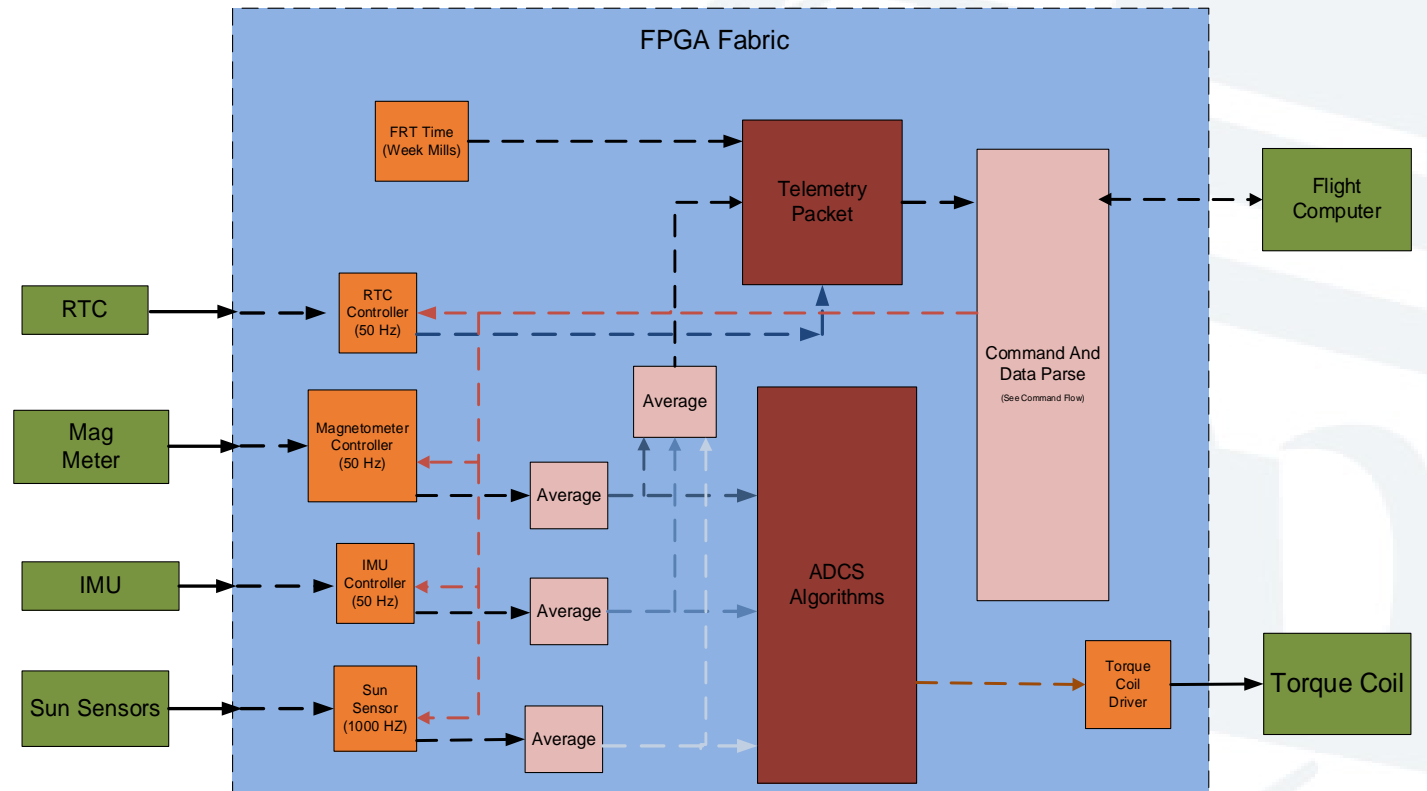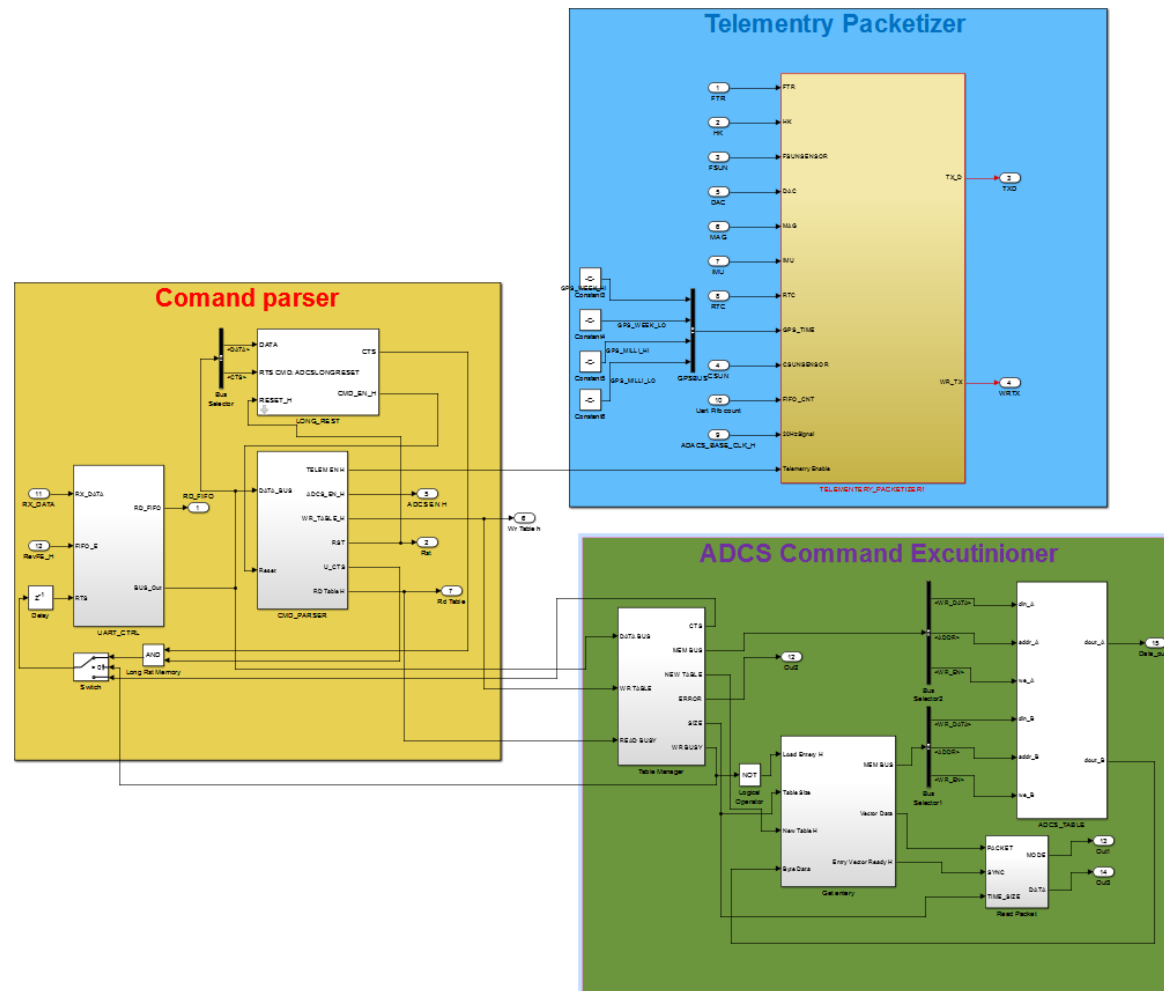℗ We were able to use Simulink and HDL coder to talk to low level hardware.

℗ We were able to use Simulink to quickly generate HDL code to packetize our data.

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ADCS

- Full simulation of Attitude Determination and Control System

- Full orbit simulation of ADCS

- Hardware in the loop

ADCS Model

Conclusions

ଔ A really good option for faster development

ଔ Produces well optimized HDL Code

ଔ Self Documenting

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Questions?