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CHREC
NSF Center for High-Performance Reconfigurable Computing

µ CHREC Space Processor (µCSP)

A Diminutive, Hybrid, Space Processor for Smart Modules and CubeSats

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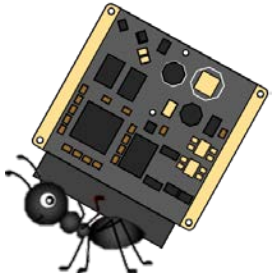

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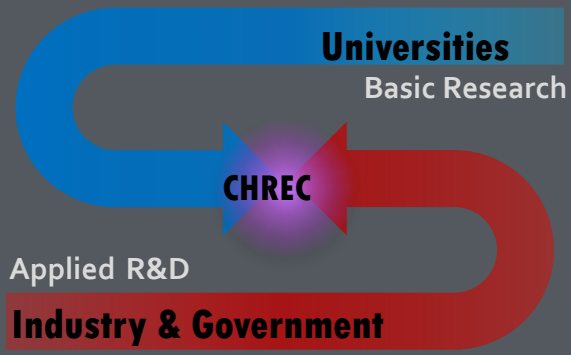
Outline

- Acknowledgements
- Brief Background and Challenges
- CSP “The Concept”
- µCSP
- Smart Modules
- Conclusions

CSP Acknowledgements

- CSP is a research project at CHREC
  - NSF Center for High-Performance Reconfigurable Computing (**CHREC**)
    - Founded in 2007
    - Comprises 3 university sites and **over 30 industry and government** partners
- CSP is a collaborative CHREC effort
  - Original partners:
    - University of Florida (lead), NASA Goddard, and Brigham Young University
  - Additional partners:
    - NASA Kennedy, Honeywell, Space Micro, Lockheed Martin SSC, NASA Johnson, NASA Ames, Xilinx, Space Sciences & Engineering and growing!

National Science Foundation
WHERE DISCOVERIES BEGIN



CHREC
Space Processor

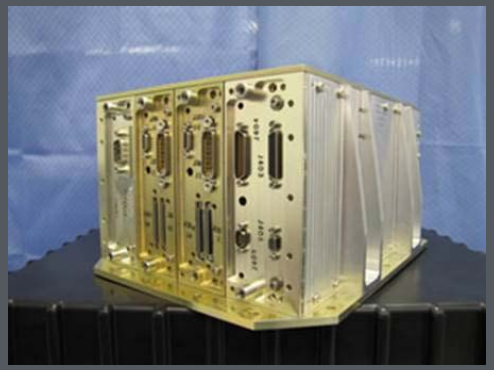
See **www.chrec.org** for more info

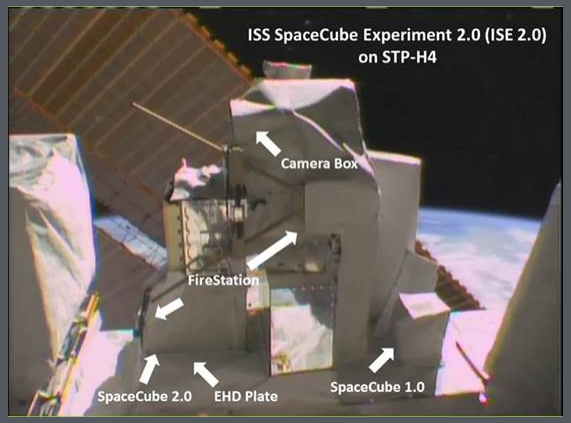
CHREC
NSF Center for High-Performance Reconfigurable Computing

Goddard Code 587

Science Data Processing Branch
Advanced Avionics and Architectures Group

- Overall Mission Objective:
  - "To enable a new class of future Goddard missions by developing technology for small spacecraft architectures, mission concepts, component subsystem hardware, and deployment methods."
  - Provide strong science rationale for using small spacecraft platforms & constellations





- Key Platforms
  - Scalable components for 3U, 6U, 12U, SmallSat
  - Success with SpaceCube v1, SpaceCube v1.5, SpaceCube v2, SpaceCube Mini and now CSPv1

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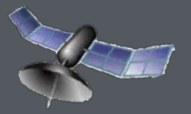
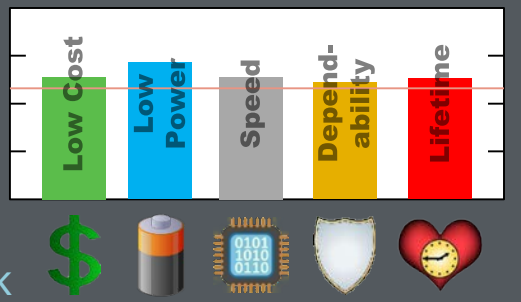
Challenges and Key Terms



- Challenges
  - Escalating high-speed computing demands for both sensor-data and autonomous processing
  - Restrained by limited bandwidth

- Requirements
  - Space environments have strict requirements and restrictions
  - Performance (throughput and real-time)
  - Size, Weight, Power, Cost (**SWaP-C**)& Reliability



- Key Terms
  - FPGA (Field-Programmable Gate Array)
    - Large amount of logic resources and specialized cores connected with configurable routing network
    - Massive algorithm parallelism for immense speedup
  - SoC (System on a Chip)
    - Integrated circuit that combines many processing technologies into single chip
    - Some applications are control-flow oriented and better suited for CPUs

XILINX®

CSP "The Concept"

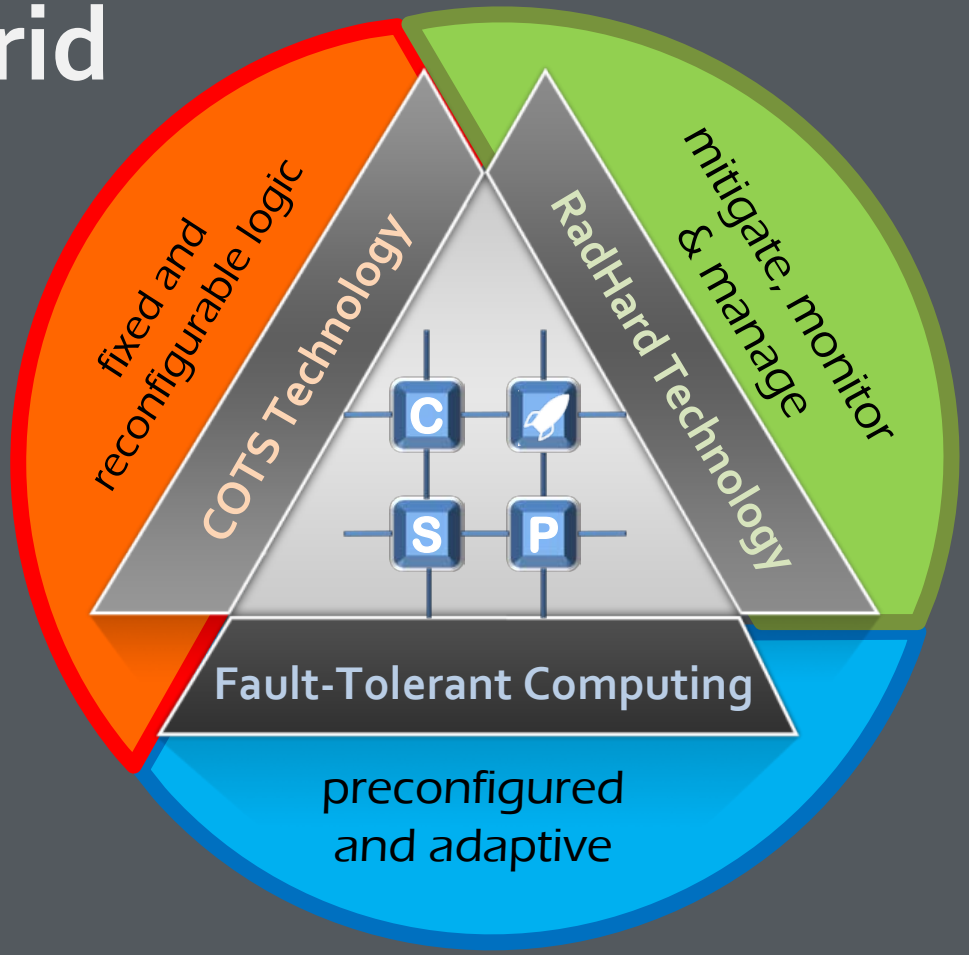
Multifaceted Hybrid

Space Computing

Hybrid processor
(multicore CPU [fixed] + FPGA subsystem [reconfig])

Hybrid system
(commercial + rad-hard)

Robust design
Novel mix of COTS, rad-hard, & FTC



CHREC Space Processor v1

Motivation

Create a scalable, high performance, lower power, reconfigurable, and high reliability development system to meet future mission needs

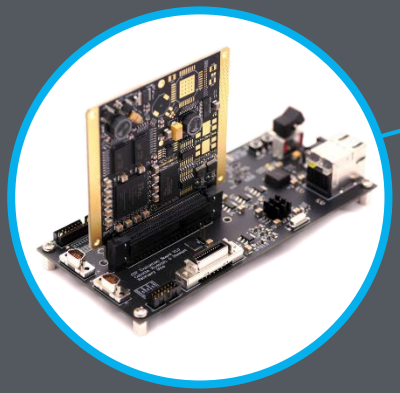
Overview

CHREC Space Processor v1 (CSPv1) is first design in family of CHREC-developed boards embodying CSP concept

- Unique selective population scheme supports assembly of Engineering Model (EM) or flight design
- Flexible app speedup with hybrid and reconfigurable architecture coupled with cost-effective prototyping

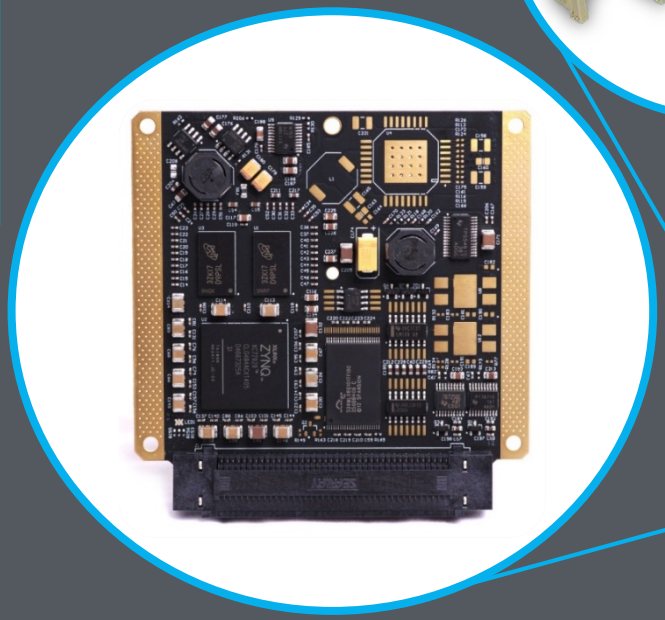
Keystone Principle

Commercial technology featured, for best in high performance and energy efficiency, but monitored by radiation-hardened devices, and augmented with fault-tolerant computing strategies



Evaluation Board

Example Flight Configuration



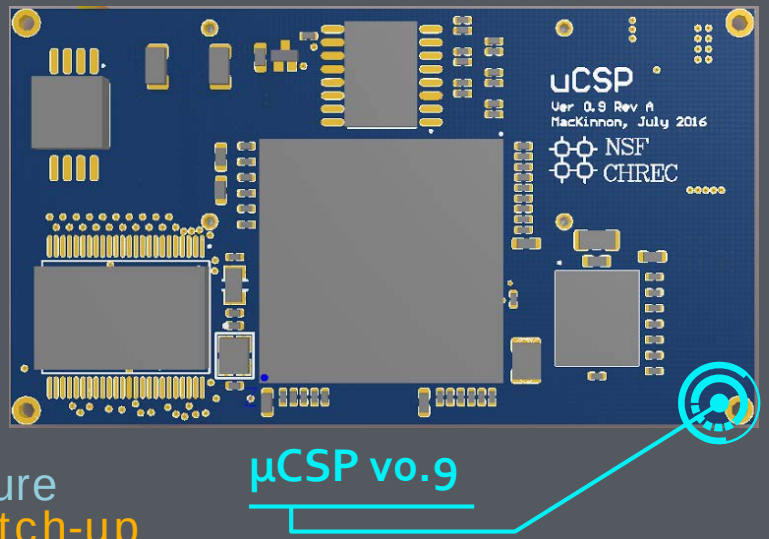
(CSPv1) CHREC Space Processor

sales@spacemicro.com

S: 1U CubeSat form factor (10x10 cm)
W:60 g P:1.6-2.9 W (Request Datasheet for more info)

µCSP Introduction

- **Motivations**
  - Create high-performance and reliable space-computing platform with lower SWaP-C than CSPv1
    - Several missions reported CSPv1 has too high power for mission needs during several proposals
    - Many commercial CubeSat kits feature microcontrollers with catastrophic latch-up
  - Develop scalable and flexible capabilities to provide "smart" functionality to additional modules



- **Goals**
  - Develop multifaceted mini hybrid computer featuring **SmartFusion2** SoC (ARM-M3 processor + FPGA) retains original CSP concept definition

Microsemi
Power Matters.
SmartFusion®2
SoC FPGA

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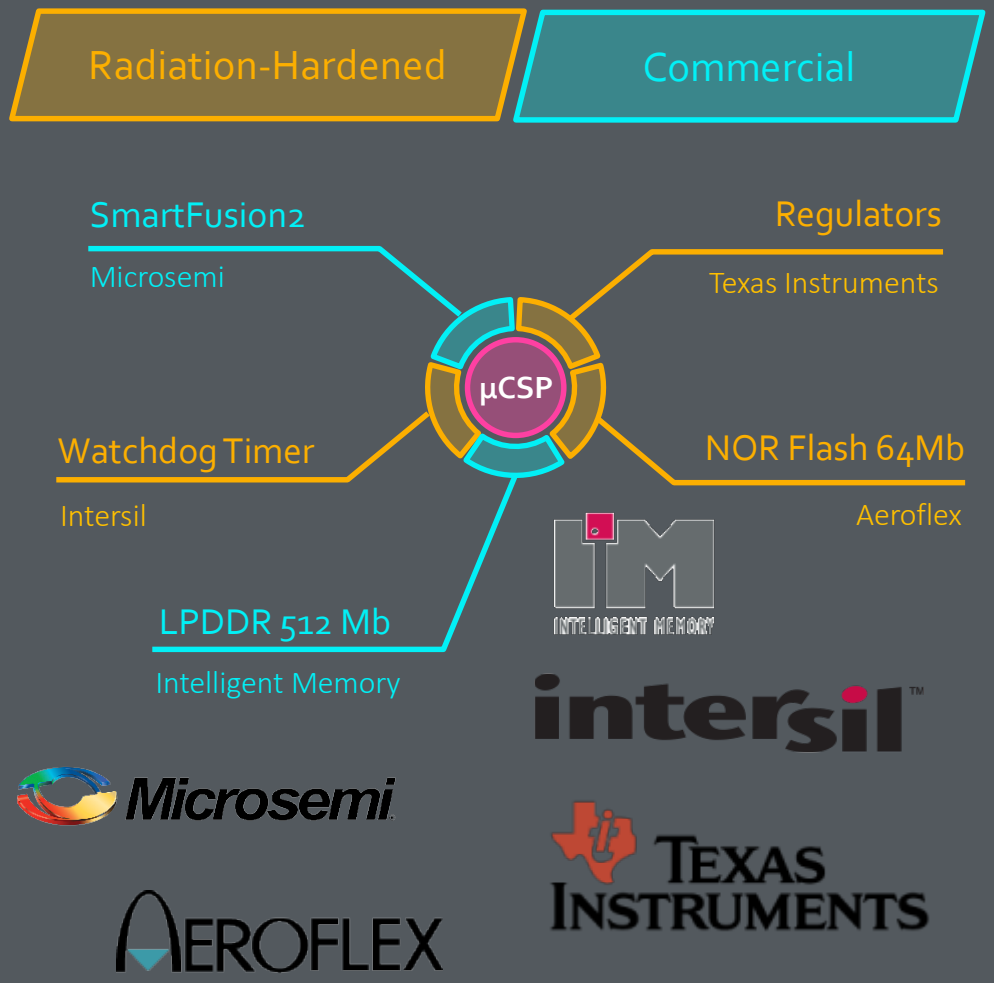
µCSP Details



Additional Info

Power: 50-100 mw (standby) .5 – 1W (nominal)
Temperature: -40°C to +85°C (Industrial)
IO: 30 differential pairs (also used as single-ended)
Interfaces: 1 CAN, 1 USB2.0, 100 Mb/s Ethernet PHY, 1 lane PCI-Express, JTAG, 2x (UART, I^2C, SPI)

SmartFusion2 Specifications

ARM Specifications	
Maximum Clock Frequency	166 MHz
Instruction Cache	8 KB
Embedded SRAM (eSRAM)	64 KB
Embedded Nonvolatile Memory (eNVM)	512 KB
FPGA Specification	
Logic Elements	86,184
Math Blocks	84
SRAM Blocks	2074

Smart Module Introduction

- Motivation
  - Currently, there are many missions that have **one-off**, one-time designs, with little to no reuse between missions
  - Universally many spacecraft will need same types of components on each mission
  - Need for network interfaces for **distributed space systems**
- Goals
  - **Develop framework** for designing series of hardware platforms that can be easily configured, integrated, and tested in preparation for new mission
  - Three Main Objectives
    - Provide "Smart" capability to each design slice
    - Achieve faster configuration and prototyping (**Plug-and-Play** designs)
    - Exploit reuse of designs through qualification
  - Focus on application and not on low-level implementation
  - Create inventory of designs that can be reused, to take designs from "**shelf-to-spacecraft**"

Wiring Advantages

- Another benefit of Smart Module is **reduction of extensive wiring**
- Smart modules place processing intelligence closer to sensors
- Unified communications system reduces bulk of wiring for power and communication interfaces
- Reduction of wiring has multitude of benefits:
  - Reduces weight of spacecraft, thereby reducing cost by extension
  - Decreases integration and test time involved with building, assembling, and testing wiring harness
  - Simplifies debugging and emulation of system; no longer have to be familiar with multiple interface standards

Example Smart Modules

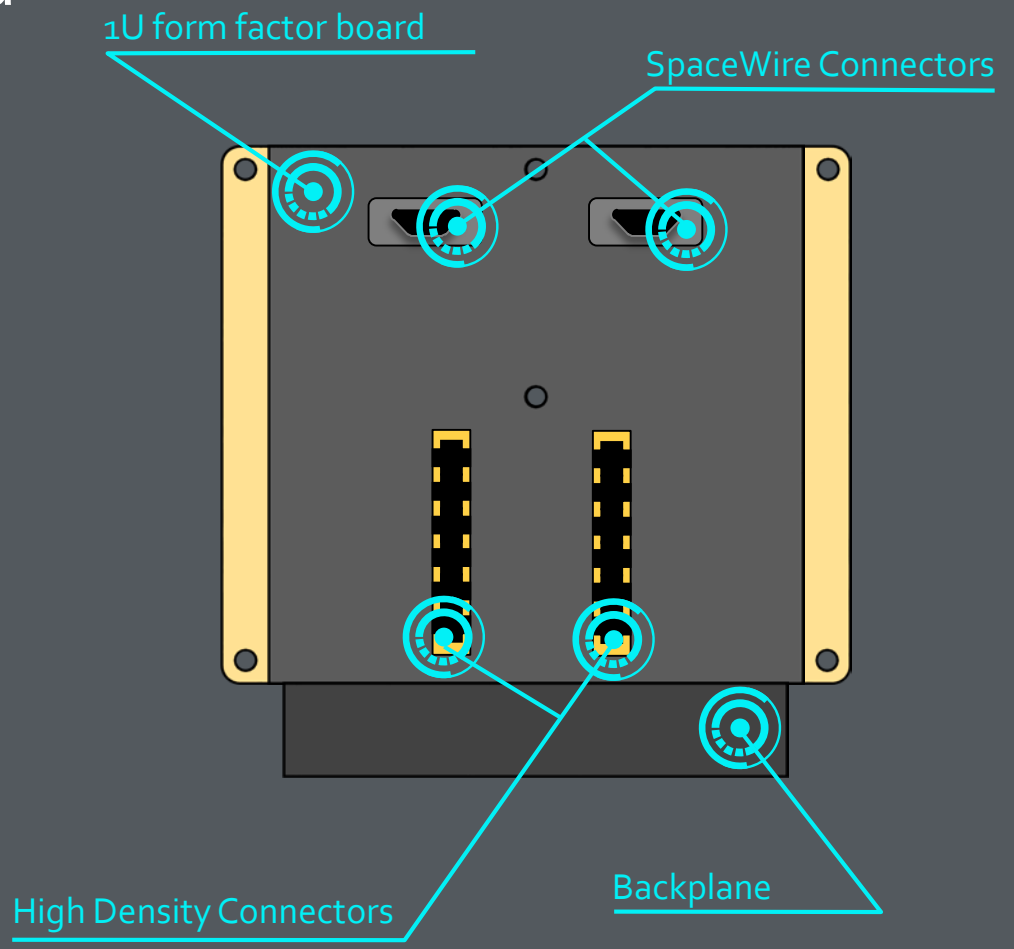
- Construct a series of hardware "cards" or "slices" that have desired functionality while following provided design template
- Make each smart module capable of computing and networking, however modest with µCSP "Brain"

Subsystem	Example Components
Power	Solar Cells Batteries Power Generator
Propulsion	Thruster Solar Sail
Communication	Transmitters Flight Terminal
Instruments	Optical Spectrometer Photometer Particle Detector
Attitude Determination and Control	Reaction Wheels Magnetorquer Control Moment Gyros Star Track Sun Sensors GPS Receiver and Antennas

Source: "Small Spacecraft Technology State of the Art" (NASA/TP–2014–216648/REV1)

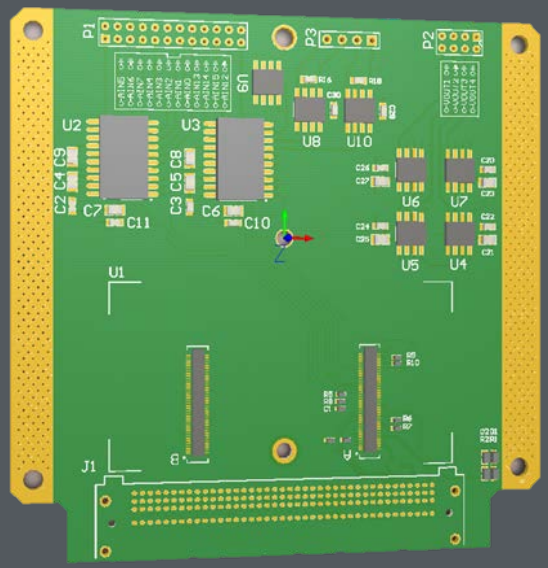
Example Template

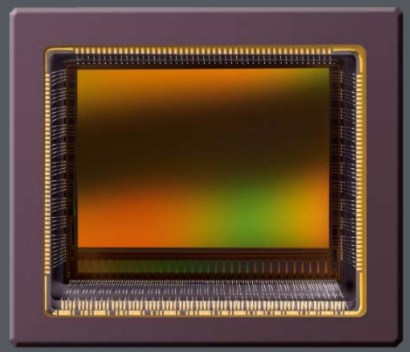
- 1U form factor board for CubeSat
- 2 high-density connectors
  - Mate µCSP to design
- Backplane
  - Provides power, ground, and bus communications
- Optional SpaceWire connectors (can go through backplane)



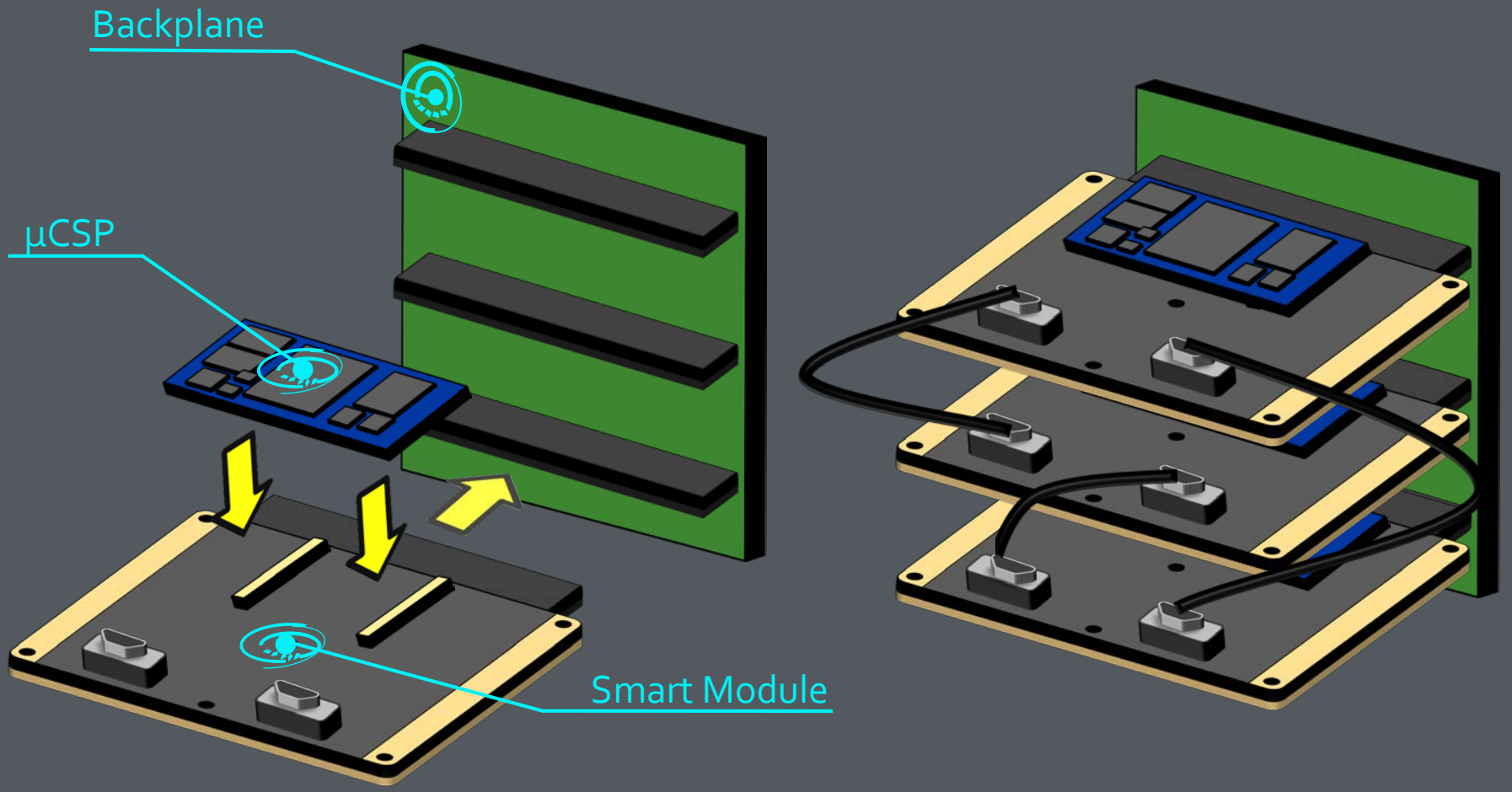
Smart Module Boards

- Several modules in development to showcase versatility of µCSP
- General Instrument Interface
  - Hi-speed ADC/DACs, RTC, Instrument amplifiers, JTAG programmer
- BLDC Driver and Torquer
  - Three motor drivers, H-bridges, Acc/gyro
  - Support as attitude control unit
- CMV4000 Imager
  - 4.2-megapixel 1” visual spectrum sensor
  - Pin-compatible NIR variant available
- Network-Attached Storage (NAS)
  - Support long-term data storage
  - Incorporates fast memory for buffering, in addition to large capacity non-volatile mem.





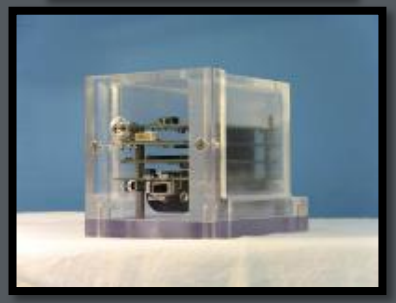
Full System Configuration



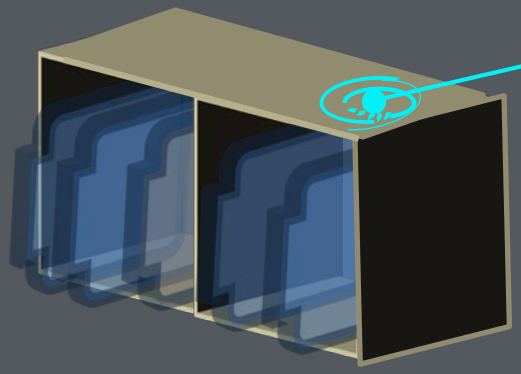
Disclaimer! Diagrams NOT to scale

Modular Integrated Stackable Layers

- Introduction
  - Original concept by NASA Johnson
- Goals
  - Design space environment capable instrumentation systems with flexible design
  - Developed to have reusable modules to meet different mission requirements
- Objectives
  - Small microcontroller applications
  - Not limited to one µController/Processor
  - Modular, Scalable, Reconfigurable
  - Industrial temperature environments
  - Low Earth Orbit environments



µCSP Illustrated Concept

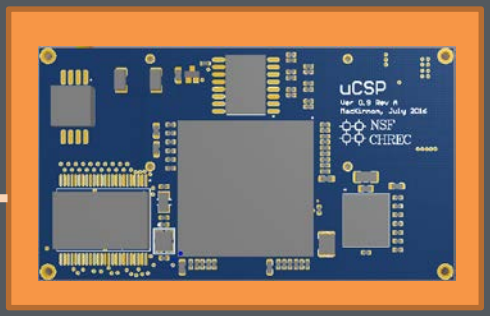


Design Library

Instrument Board

MISL

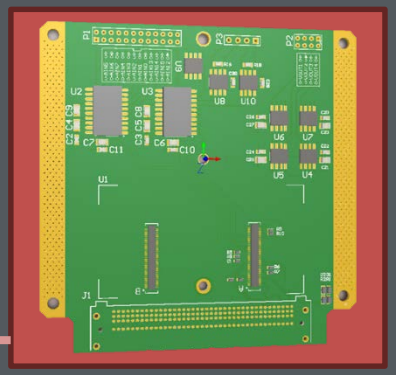
µCSP

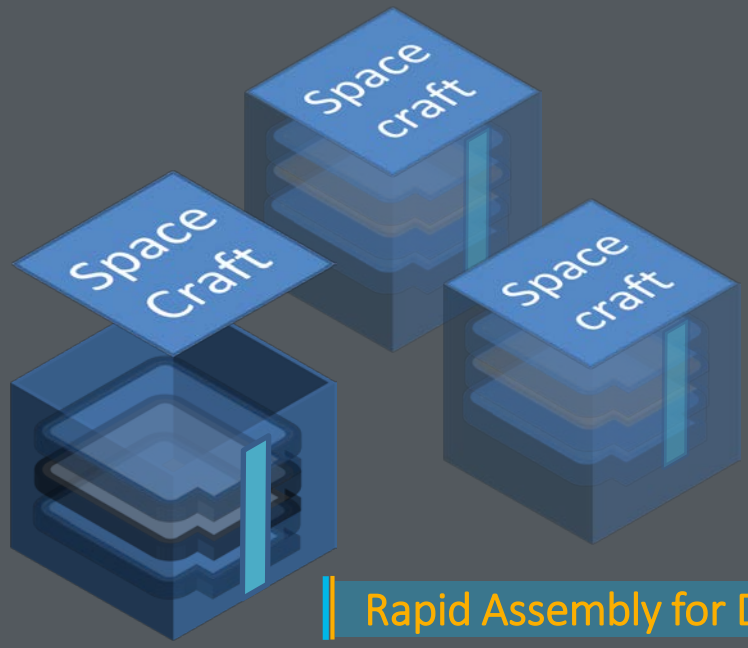


Instrument Board

CSP

µCSP





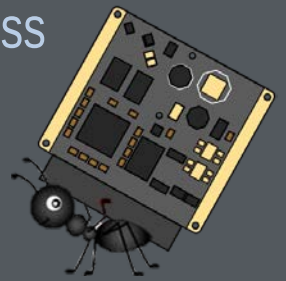
Rapid Assembly for Distributed Space Missions

What's Next?

- Engineering Models and Production
  - µCSP-EM available for CHREC members Q4 2016 along with evaluation board
  - Smart Modules available Q1 2017
- Future Mission Planning and Proposals
  - Making proposals for missions including µCSP targeting LEO in distributed system
- Radiation Testing
  - Planning heavy-ion radiation testing Q4 2016

Conclusions

- **Major challenges lie ahead**
  - Escalating app demands in harsh environments
  - Tightening constraints of platform, budget, process
  - ***Necessitates adeptly doing more with less***
- µCSP and Smart Modules for future missions
  - Focus upon verifying new µCSPv1 flight design
    - CSP "The Concept" (**multifaceted-hybrid** and **hardware-reconfigurable** design) in lower SWaP-C form factor
  - Establish Smart Module framework and library of "slices"
    - Provide easily configuration, integration, and testing
  - Push the bounds of possibility in space
    - Explore flexibility and scalability with distributed systems



Contact Information

- **Center Web Site**
  - www.chrec.org

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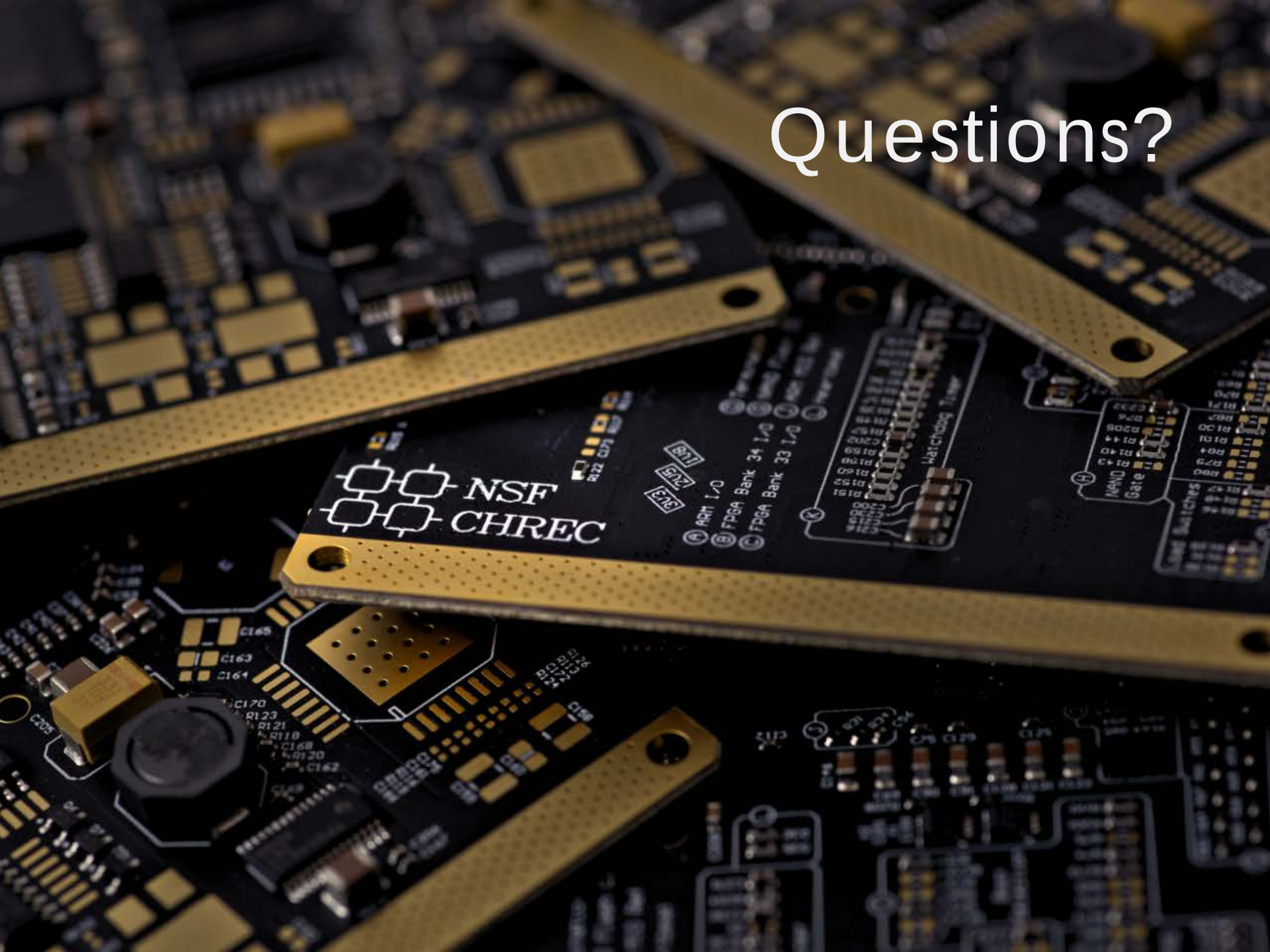
Questions?
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