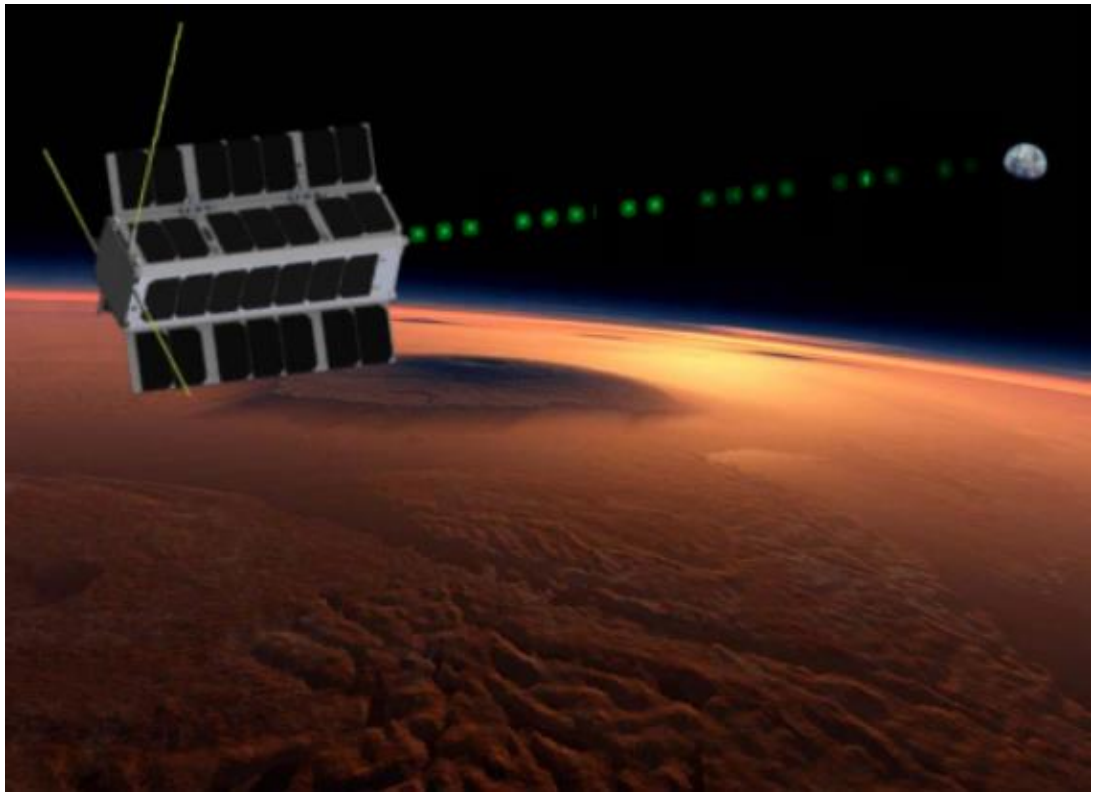
Deep Space Laser Communication Transmitter and High Precision Timing System for Small Satellites



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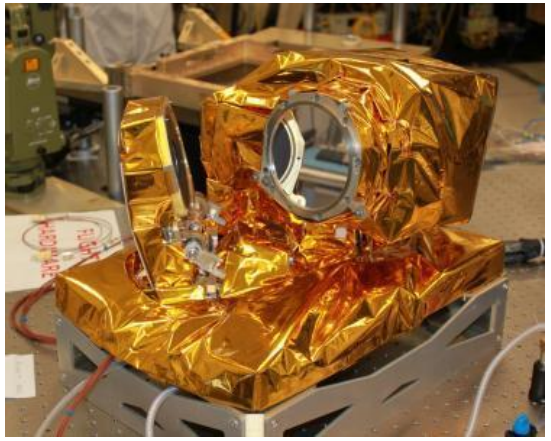
Motivation and Objectives

- Precision timing of optical pulse for communication:
  - Reduced spread at optical frequencies
    - Compact, lower power design
    - x10 to x100 data throughout at equivalent SWaP

- Advantage of pulsed modulation scheme:
  - Higher peek-power
    - Longer range
    - Resilient to disturbances and absorption
  - One way-ranging
  - Non-linear detection



	Deep Space Network	LADEE LLCD
Type	S-Band (~2 GHz)	1550 nm, (~200 THz)
Aperture	34 m	0.1 m
EIRP	8.3 GW	8.1 GW

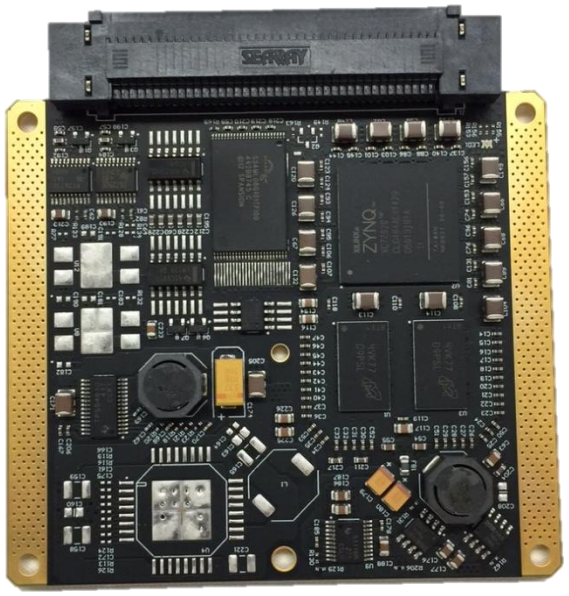
Don Boroson, MIT Lincoln Laboratory

Motivation and Objectives

Objective: Demonstrate small volume, low power optical communication.

- 2U, ~5W, ~100 Mbps (GEO) to ~5 Mbps (Lunar)
- Proof of Concept (TRL 1 to TRL 3)
- Focusing on downlink

LLST Modem on LADEE



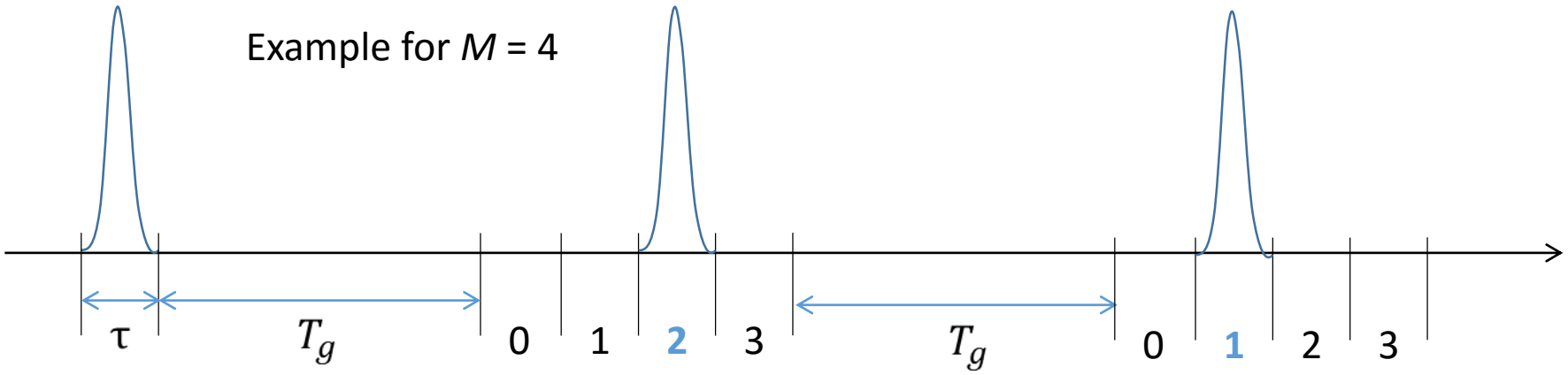
CubeSat Space Processor with FPGA
From Space Micro / CHREC

M-slot Pulse Position Modulation

- Time is divided into M slots of duration τ
- Guard time T_g begins after fixed interval $T_g + M\tau$
- Pulse rising edge in one of M slots, transmitting one of M possible symbols

$$D_{PPM} = \frac{data\ per\ pulse}{time\ per\ pulse} = \frac{\log_2 M}{M\tau + T_g}$$

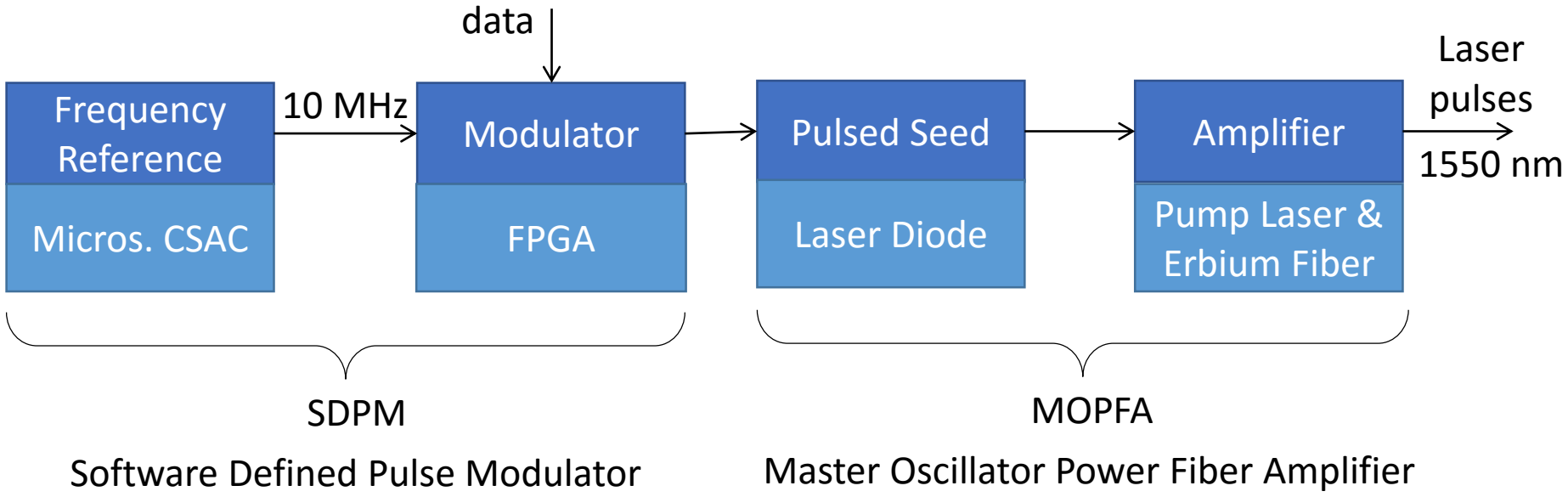
τ = slot width
T_g = guard time



Structure

Two subsystems:

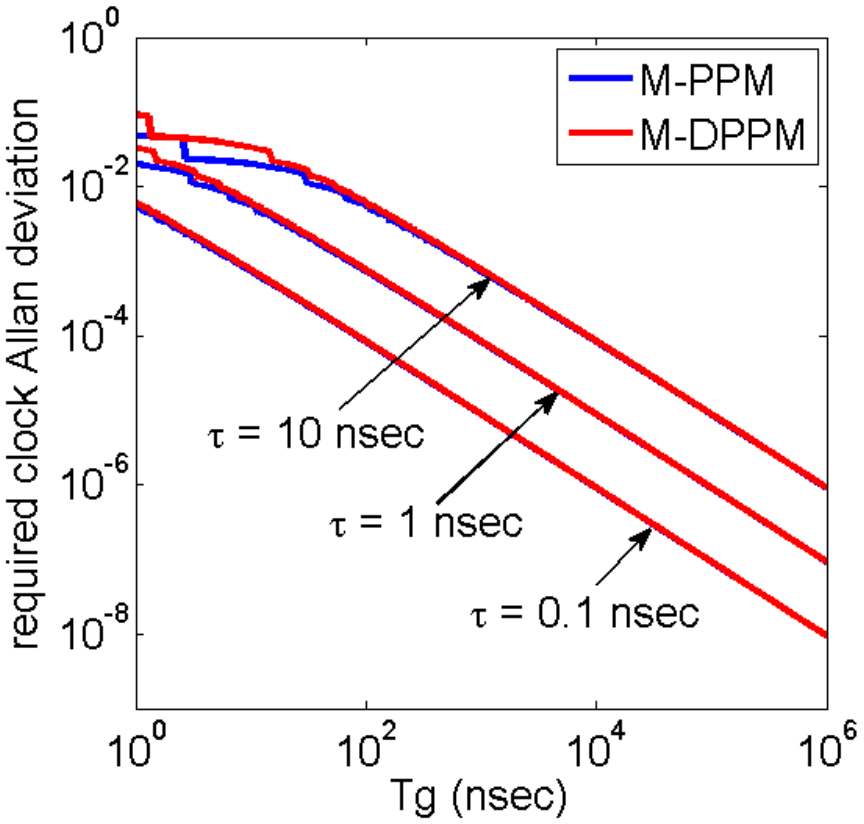
- Software Defined Pulse Modulator (SDPM)
  - Generate electric pulses according to the modulation scheme
- Master Oscillator Power Fiber Amplifier (MOPFA)
  - Transform electric pulses into amplified light pulses



Modulator Hardware: Clock

Characteristic	Chip Scale Atomic Clock (CSAC)
Standard	Cesium
Alan deviation	Measured 10^{-10} @1s in lab
Power	0.12 W
Mass	35 g
Size (LxWxH)	40.64 x 35.31 x 11.42 mm

CSAC in a CubeSat packaging

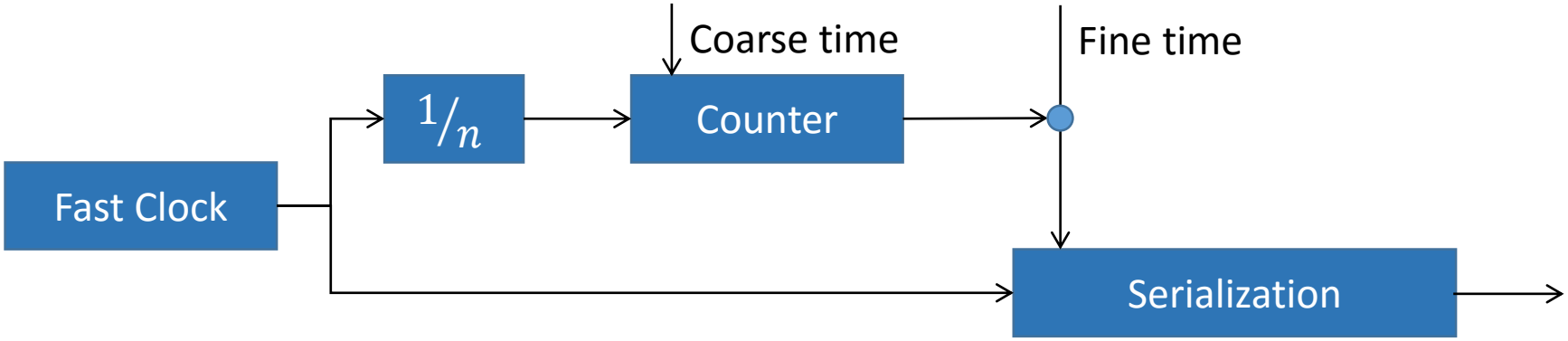


Modulator Hardware: FPGA

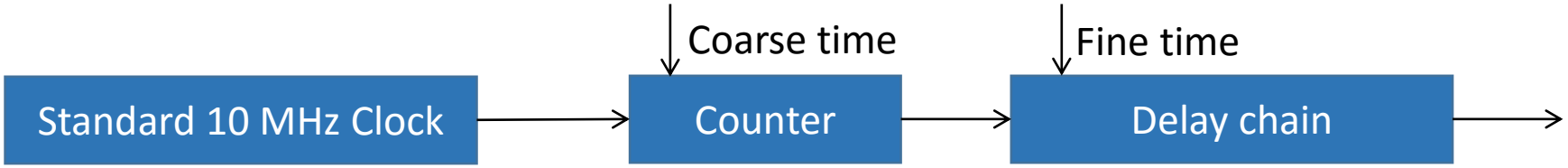
- Fully software-defined modulator, no other hardware
- Platform specific design
- Flash-based FPGA SmartFusion®2 RTG4™
  - Reprogrammable, allows for design exploration
  - Simple design: no configuration upset, no external programming
  - Rad-tolerant version with same IC process and structure

Modulator Architecture

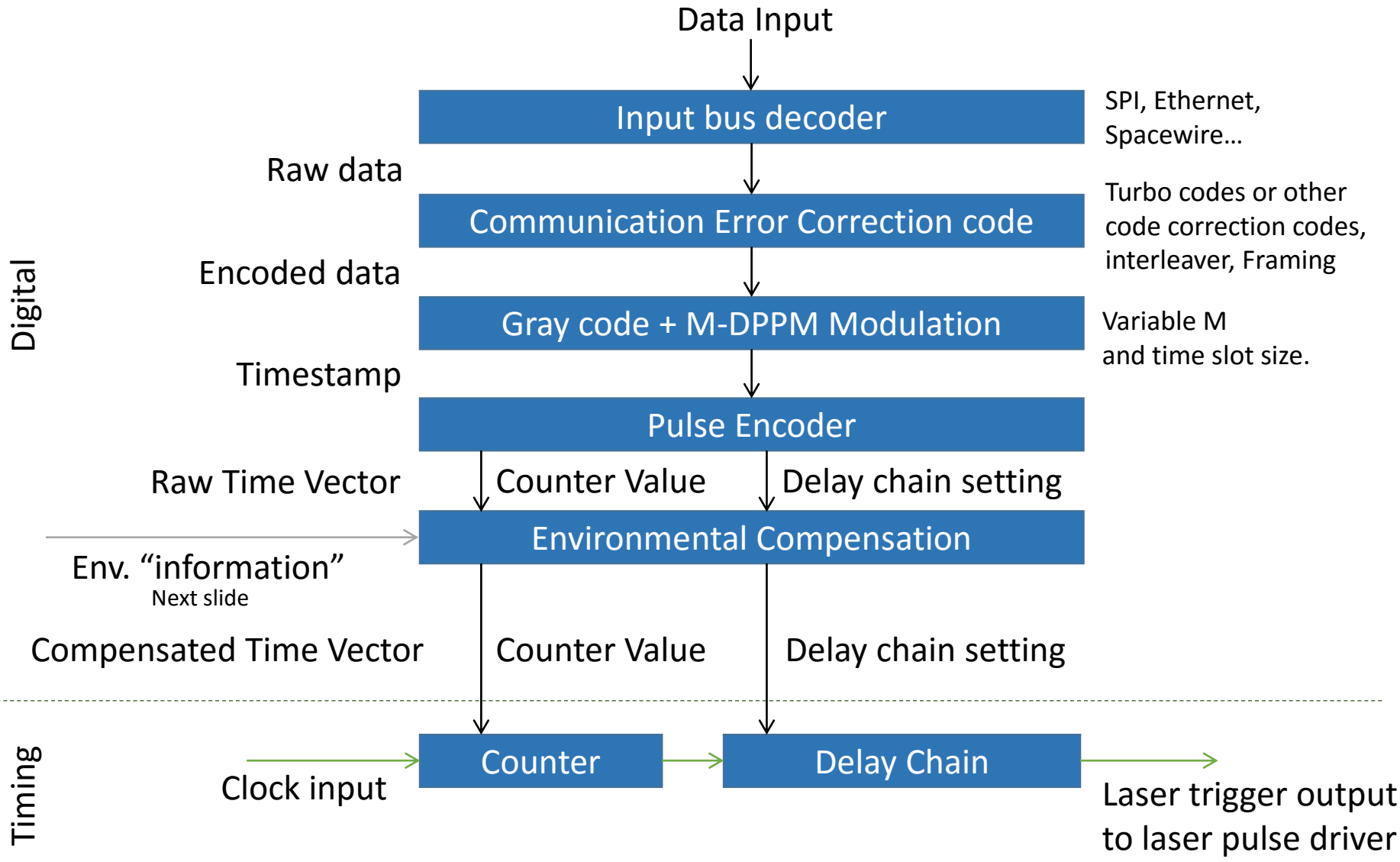
- Pulse picking with a fast slot clock
  - Low jitter (~1 ps), Limited resolution (~10 GHz → 100 ps)
  - High maximum pulse rate (= Clock frequency)



- Pulse skewing with delay chain
  - High jitter (~10 ps), High resolution (~1 ps)
  - Lower maximum pulse rate (delay chain overhead)

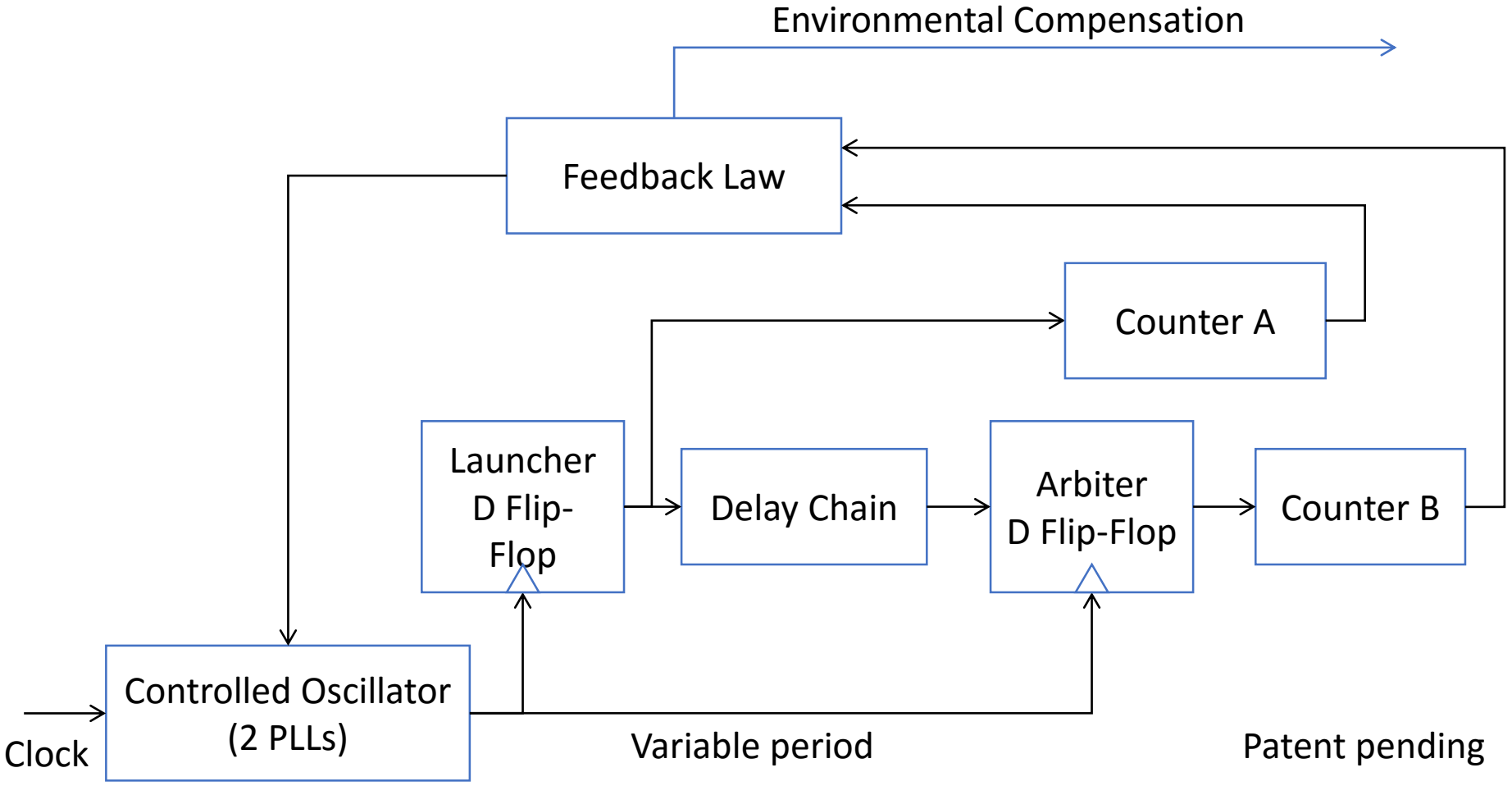


Modulator Data Flow

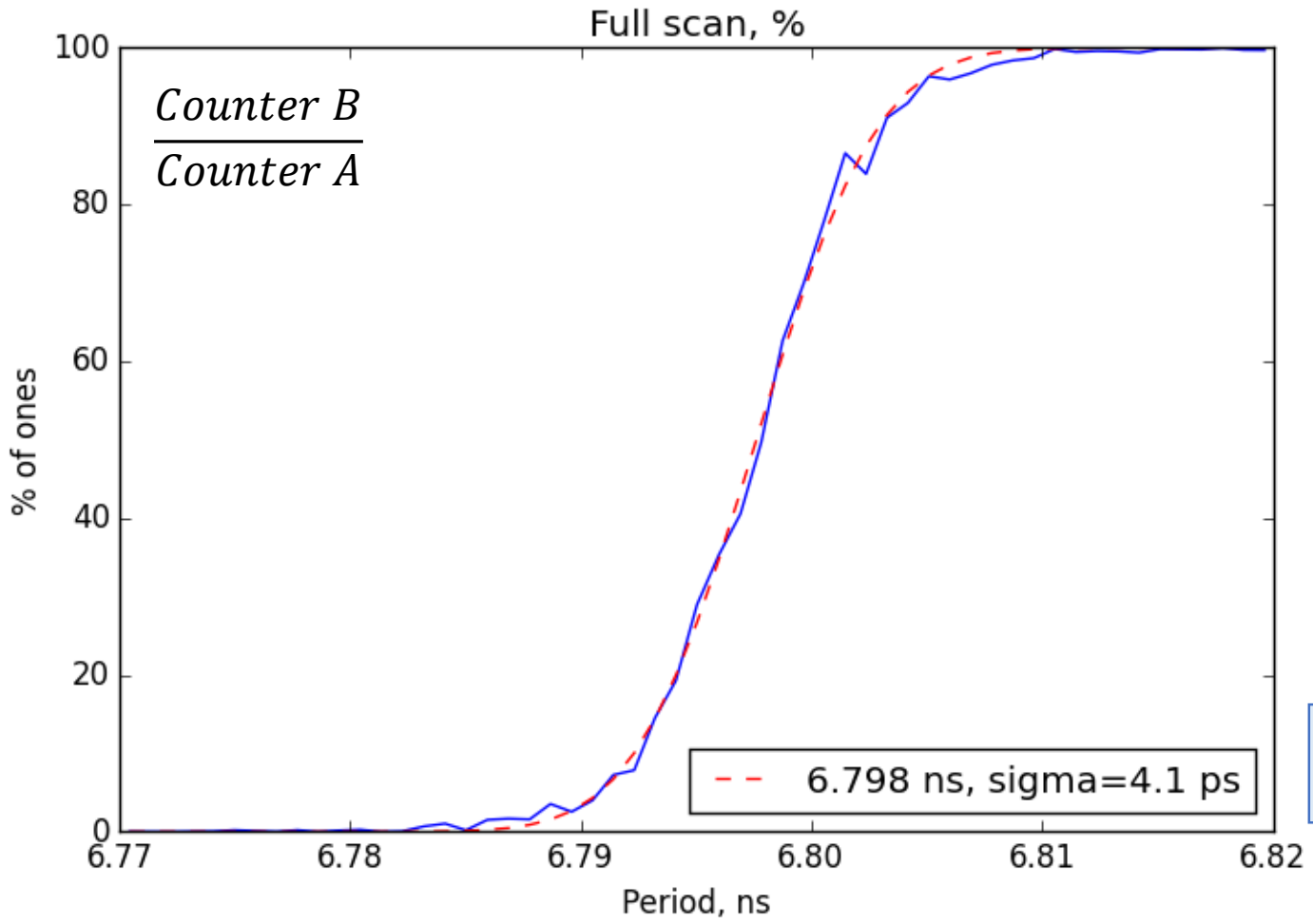


Environmental Compensation

- Temperature, voltage, radiation, aging → chain delay variations
- Delay Locked Loop (DLL) measures delay variations



DLL Results



Result from DLL circuit, $3x10^6$ binary samples at 150 MHz

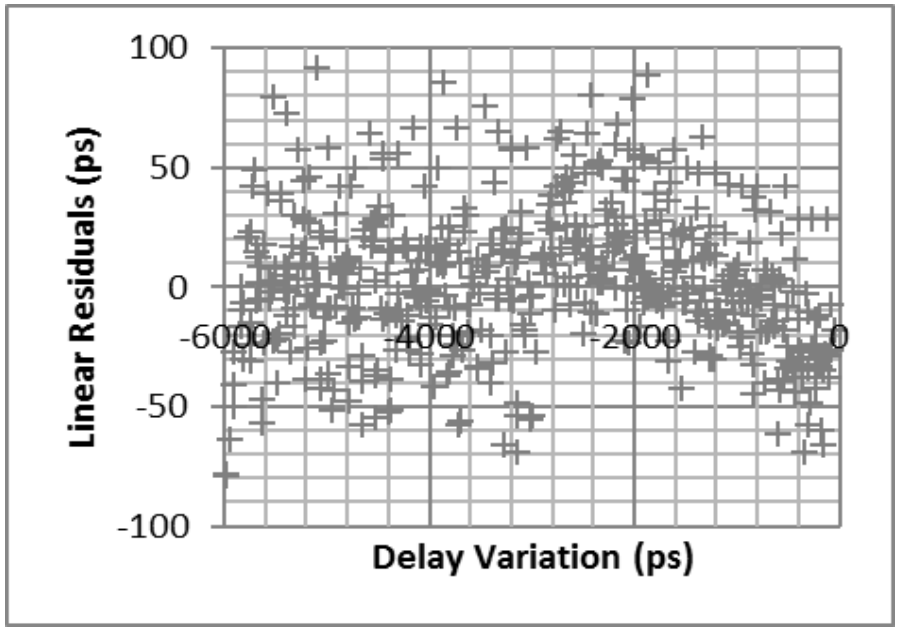
Can be tracked by a control system

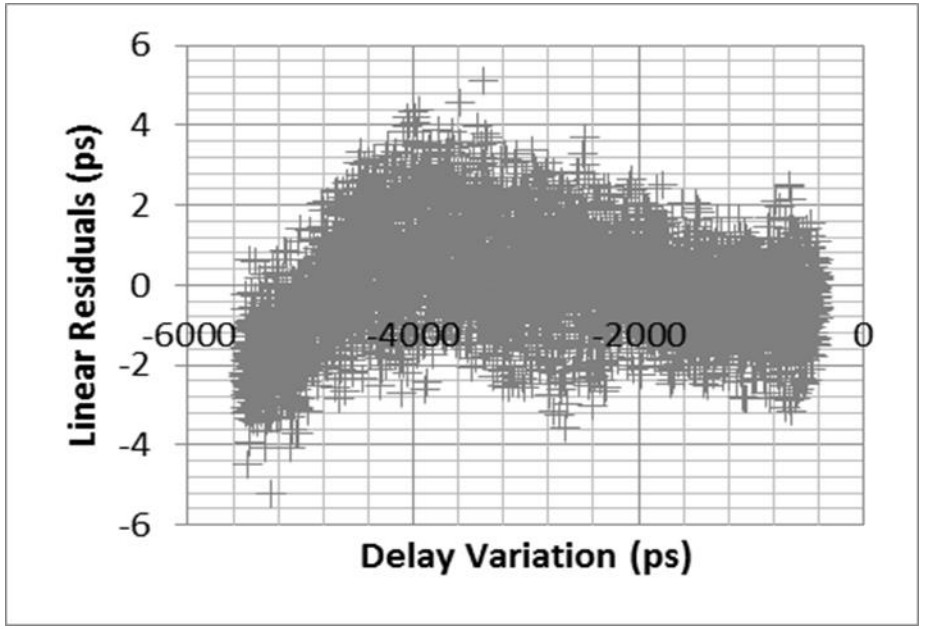
Consistent with < 100 ps slots width

- DLL oscillator: variable period resolution 1 ps typical, 2.3 ps max gap, range 4 to 24 ns

Timing with Two Chains

Residuals of linear fit to the measured delays





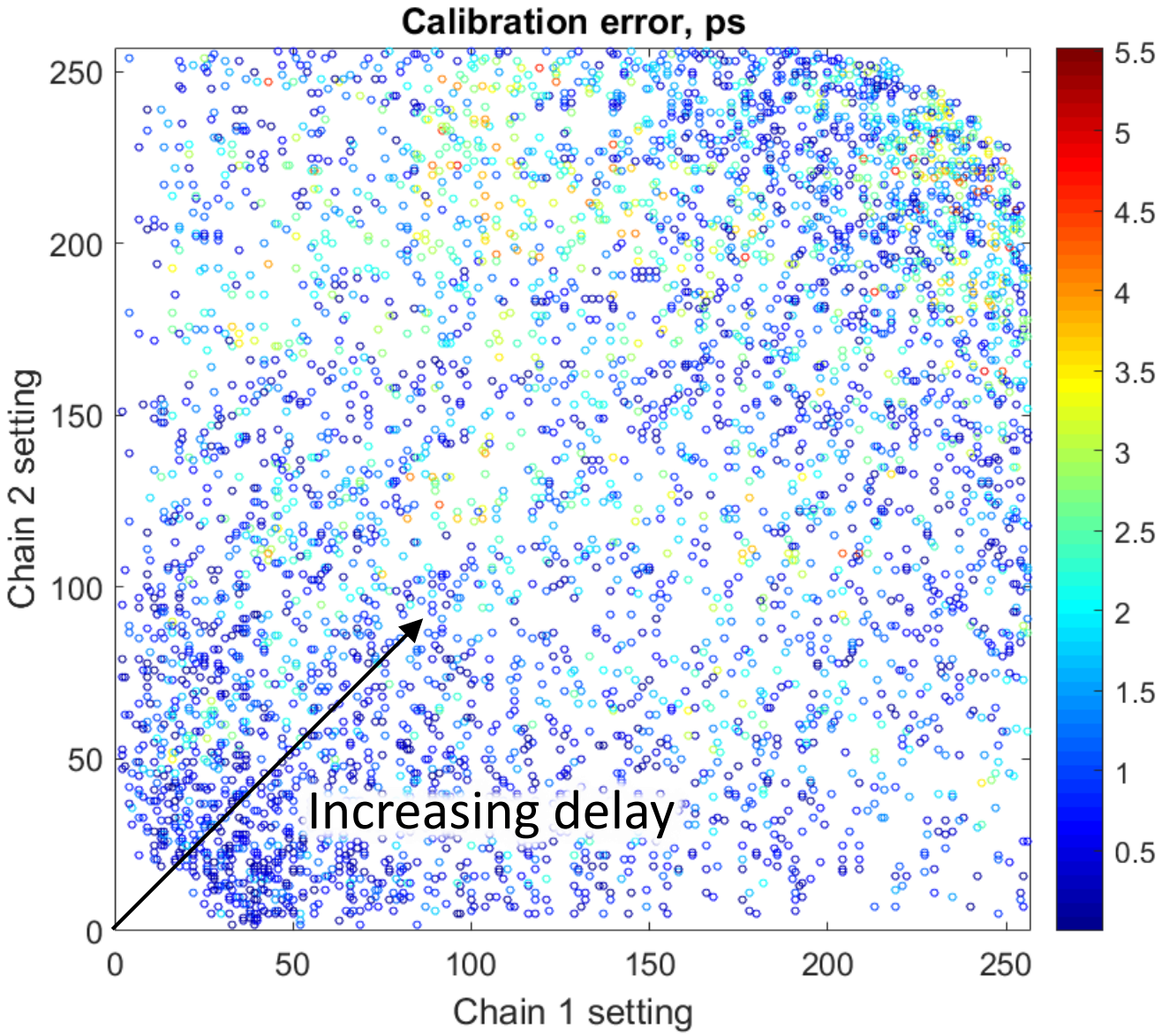
independent delay chains

- LSB: 12 ps
- Number of entries: 512
- Largest gap: >70 ps
- Max. nonlinearity: 97 ps
- Stdev of error: 39 ps

combinatorial chains

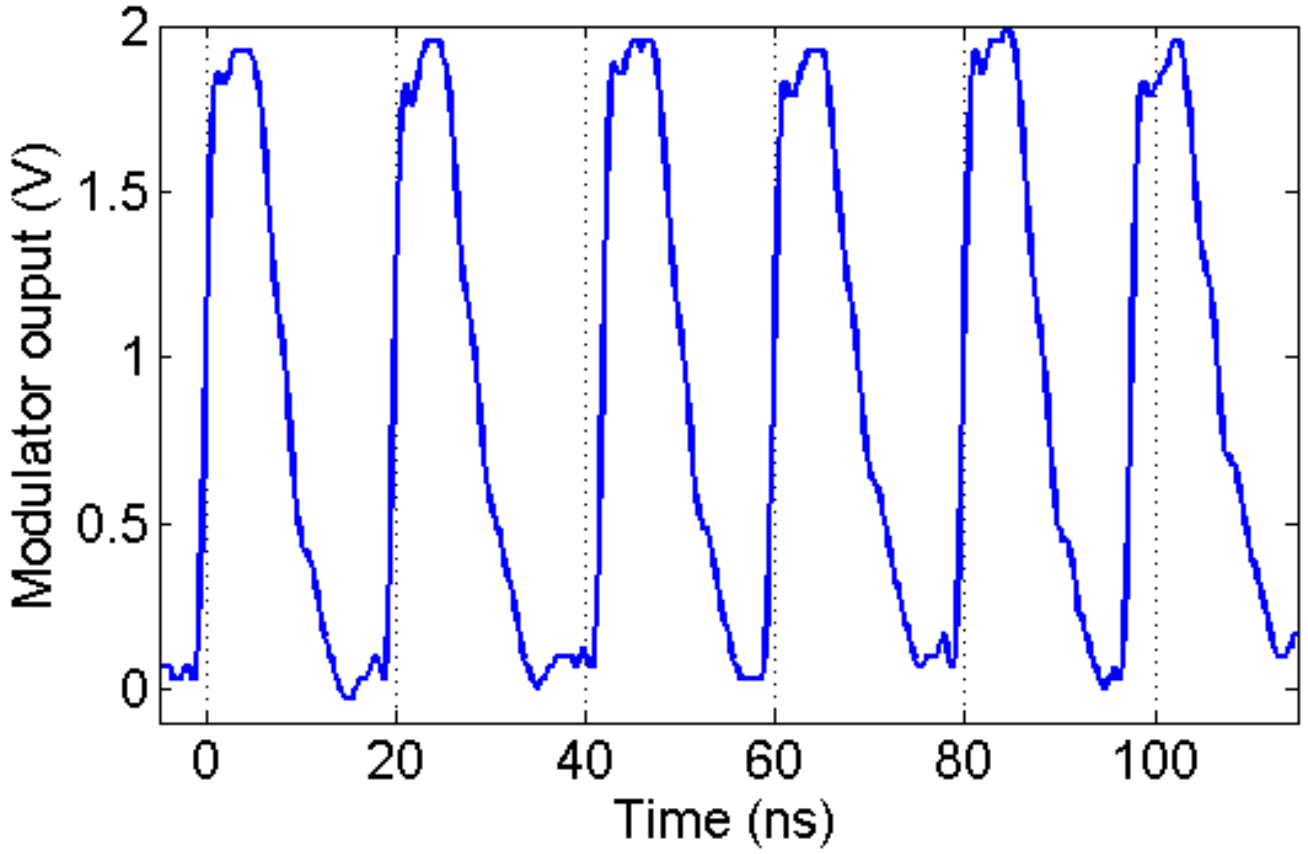
- LSB: 1 ps
- Number of entries: 5100
- Largest gap: 6.7 ps
- Max. nonlinearity: 5.5 ps
- Stdev of error: 1.4 ps

Errors on Two Chains



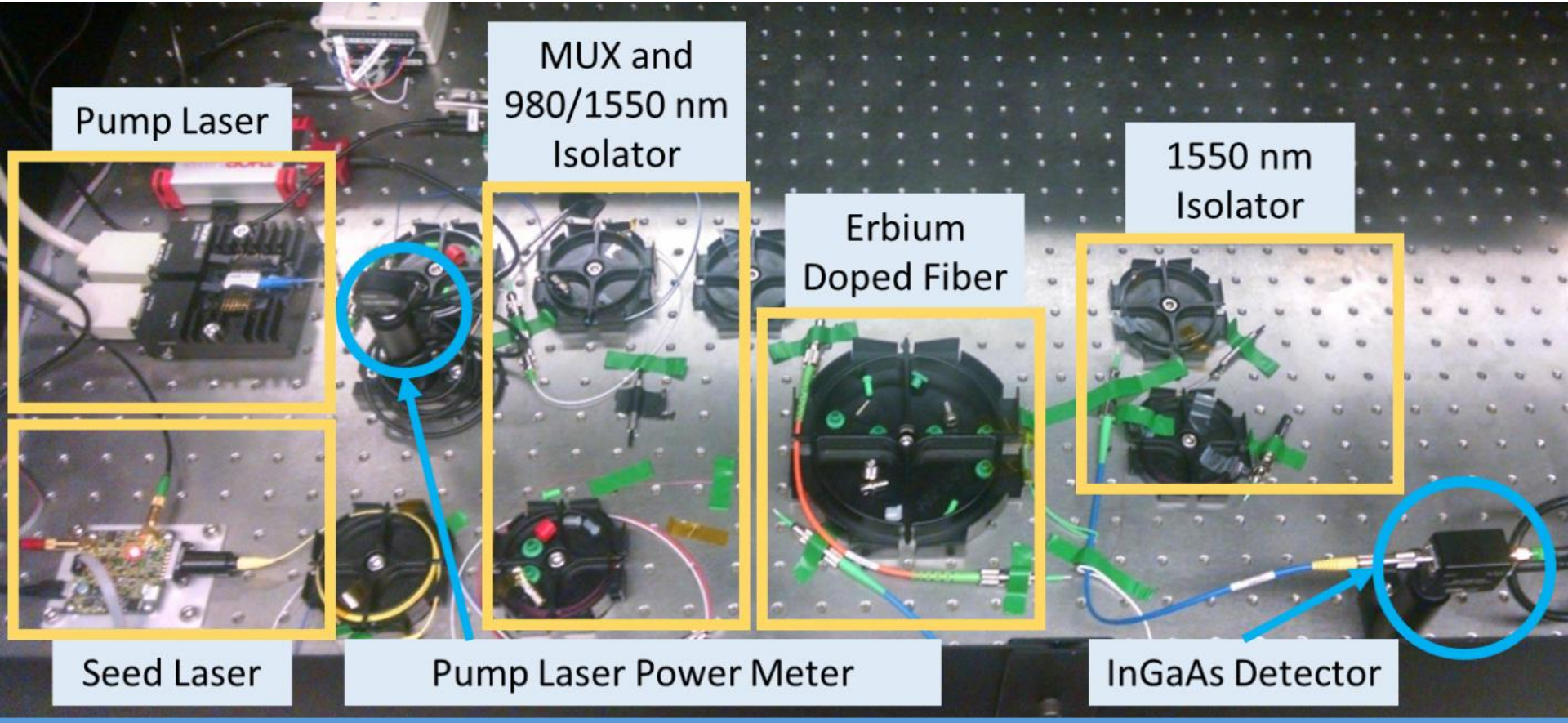
Premilinary Modulator Output

- Modulator programmed to generate delay sequence
  - 20 ns, 22 ns, 18 ns, 20 ns, 18 ns
- Measured jitter: 27 ps

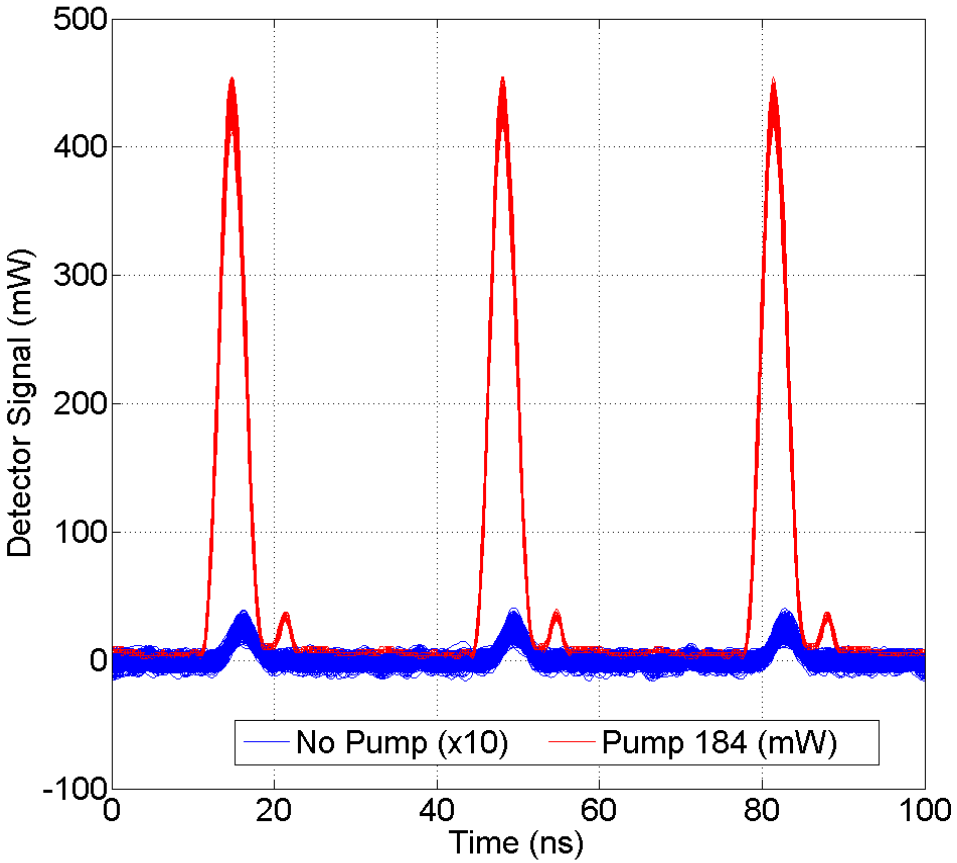


MOPFA Testbed

- Testbed designed to explore fiber laser & driver designs that can take advantage of the SDPM

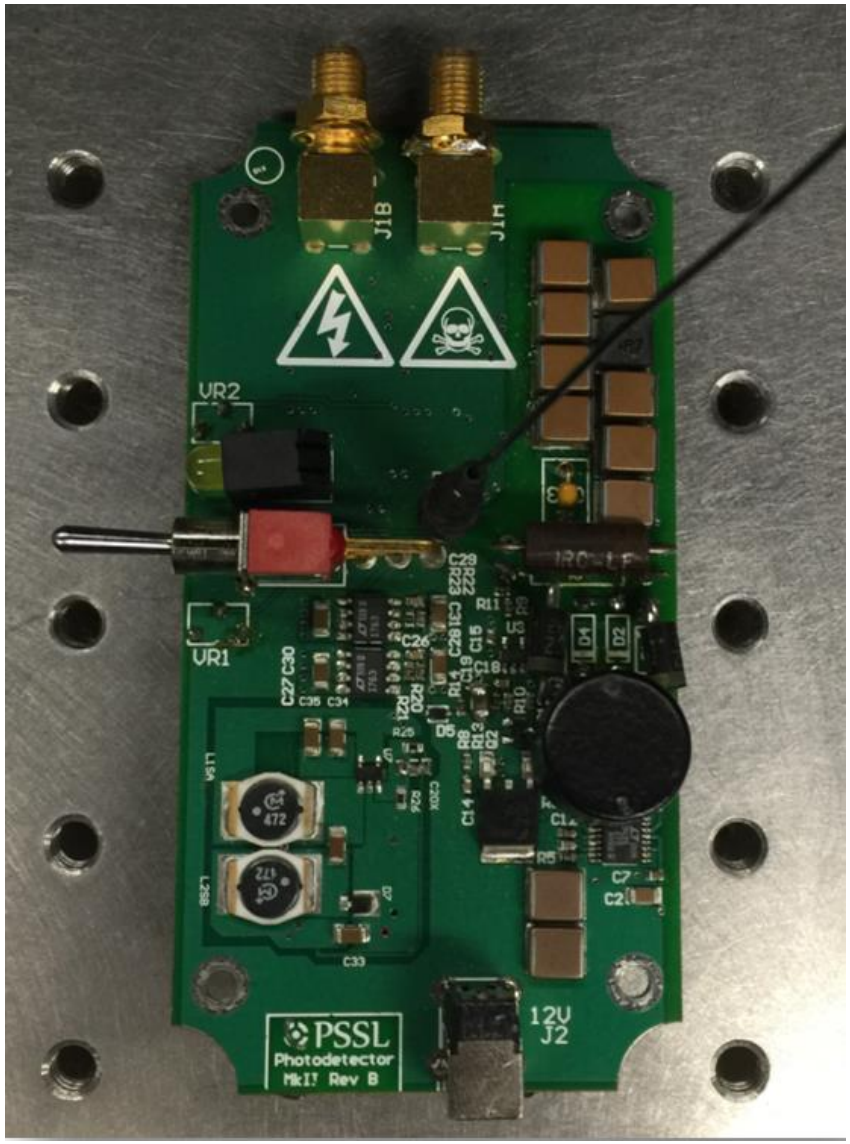


MOPFA Performance



- 50 mW, 1544 nm seed
- 500 mW, 976 nm pump
- Variable erbium fiber gains & lengths
- Connectors, mode-mismatches limit gain

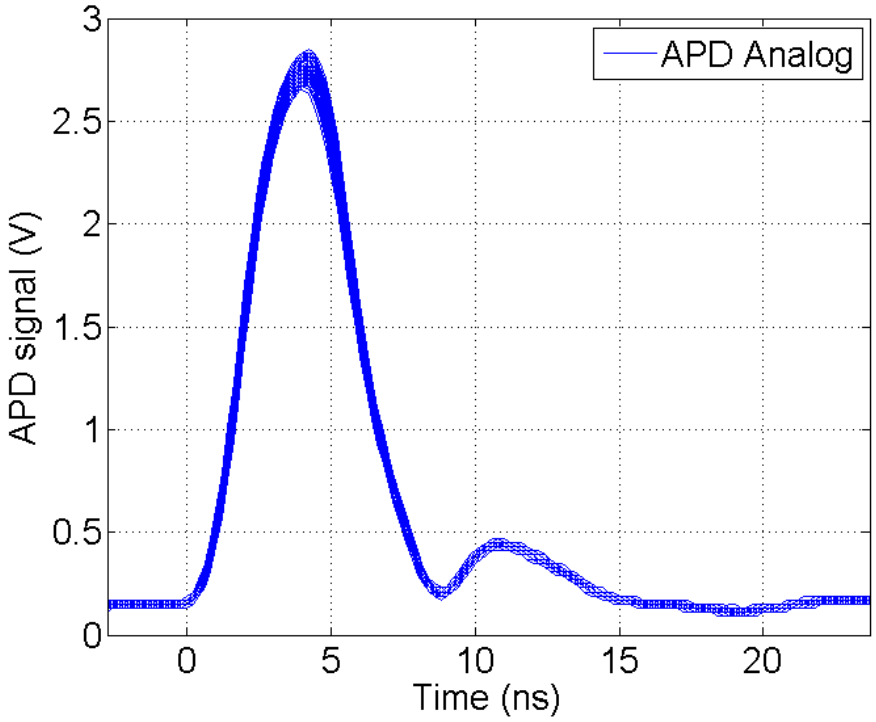
Custom APD Detector



- Custom APD unit designed & tested based on AFRL/NASA time-transfer CubeSat mission tech
  - Fiber-coupled, 80 µm, InGaAs APD
  - Temp controlled APD via TEC → stable breakdown voltage
  - Tunable high voltage reverse bias
  - Analog + digital outputs

Optical Pulses from Detector

1000 optical pulses generated by seed, measured by APD



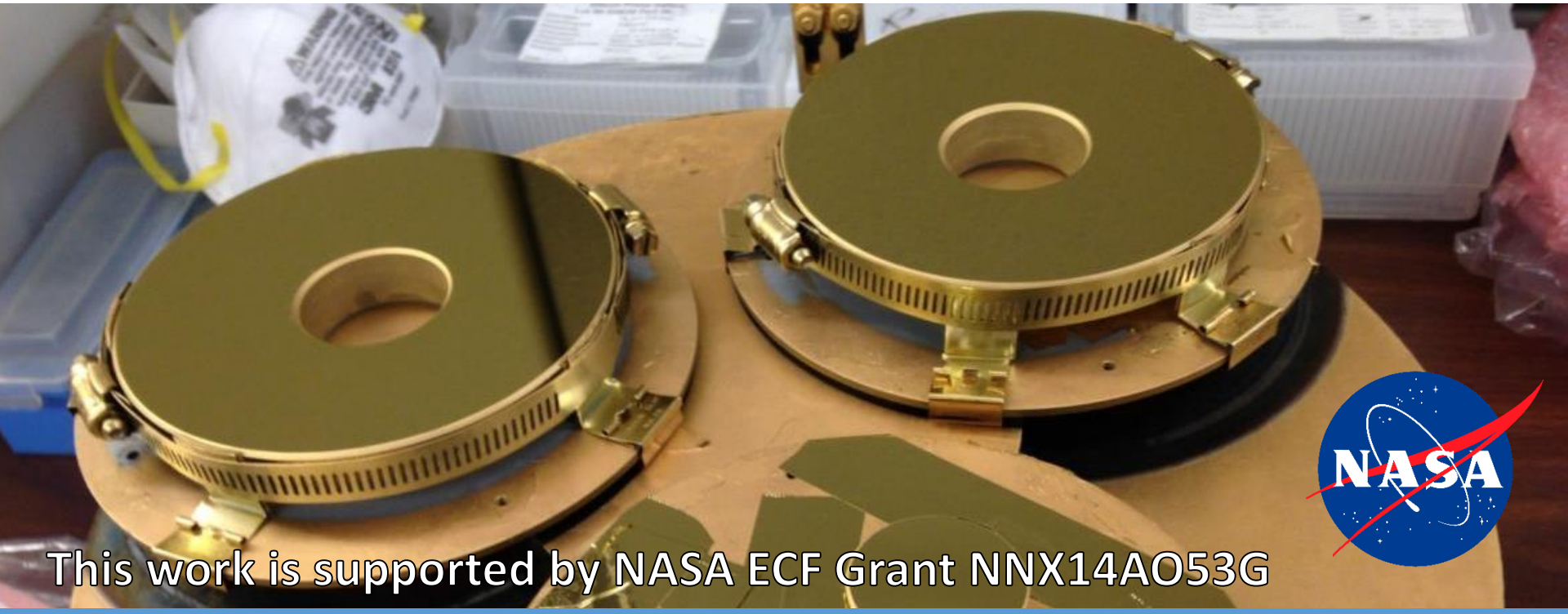
Measured jitter

- Modulator: 27 ps
- Pulse Driver: 52 ps
- Custom APD analog: 52 ps
- Custom APD digital: 47 ps
- Likely limited by seed laser driver

Conclusion

- Completed:
  - Automated modulator test bed
  - Delay chain design
  - Laser amplifier testbed
- Future work:
  - Fully embedded calibration
  - Packaging and SWaP reduction
  - Seed laser driver improvement
  - Demo on a CubeSat ~2018

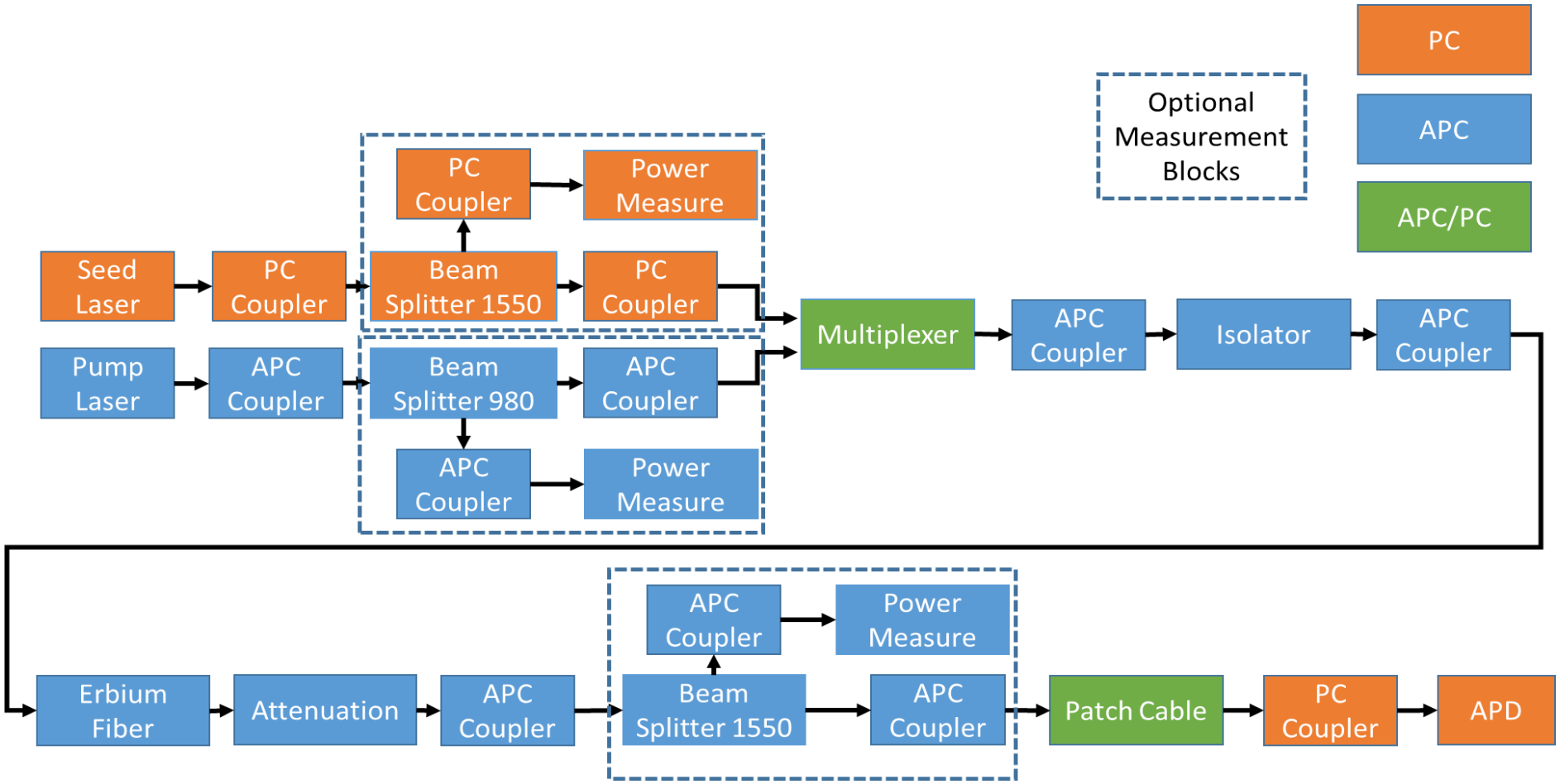
Gold-coated 5 inch primary, from NASA Glenn



This work is supported by NASA ECF Grant NNX14AO53G

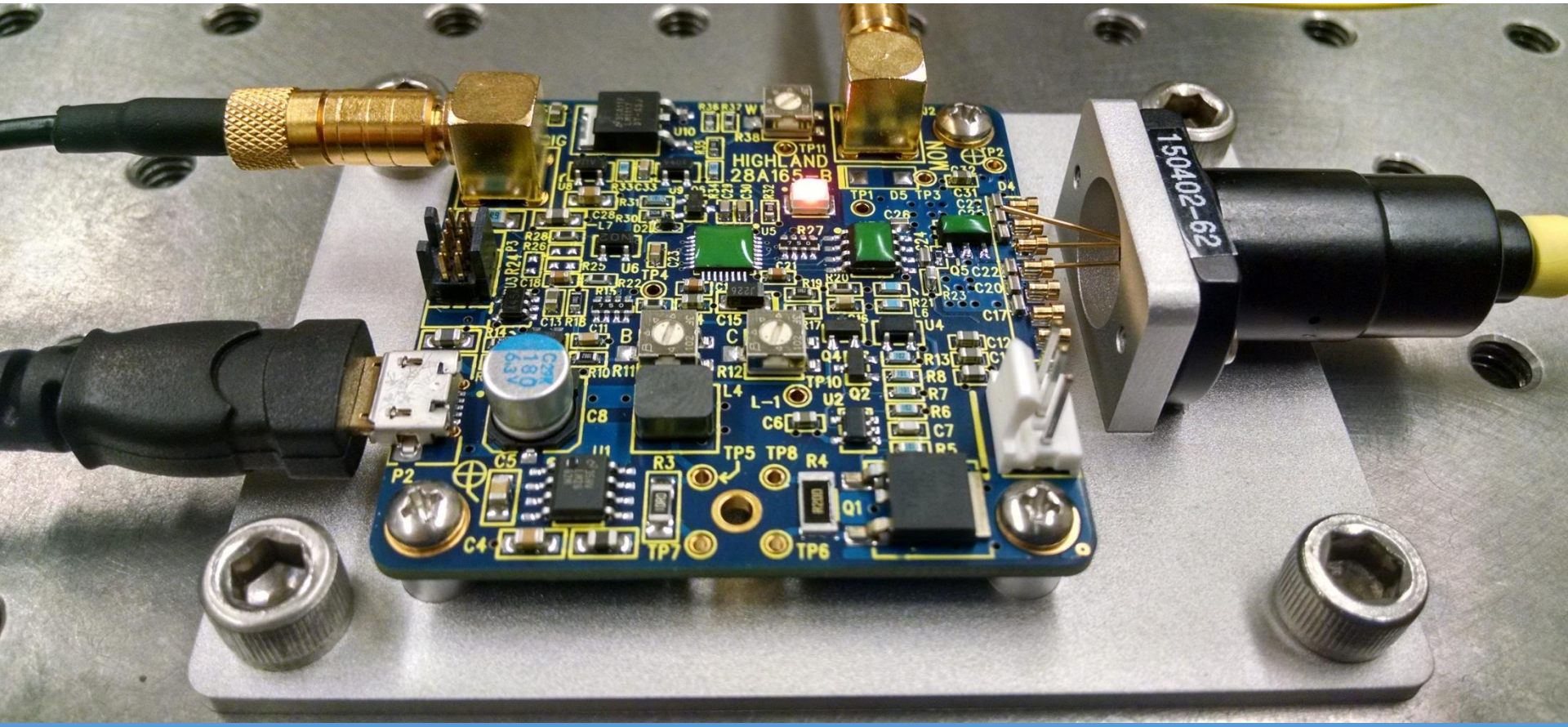
Backup Slides

MOPFA Testbed Design

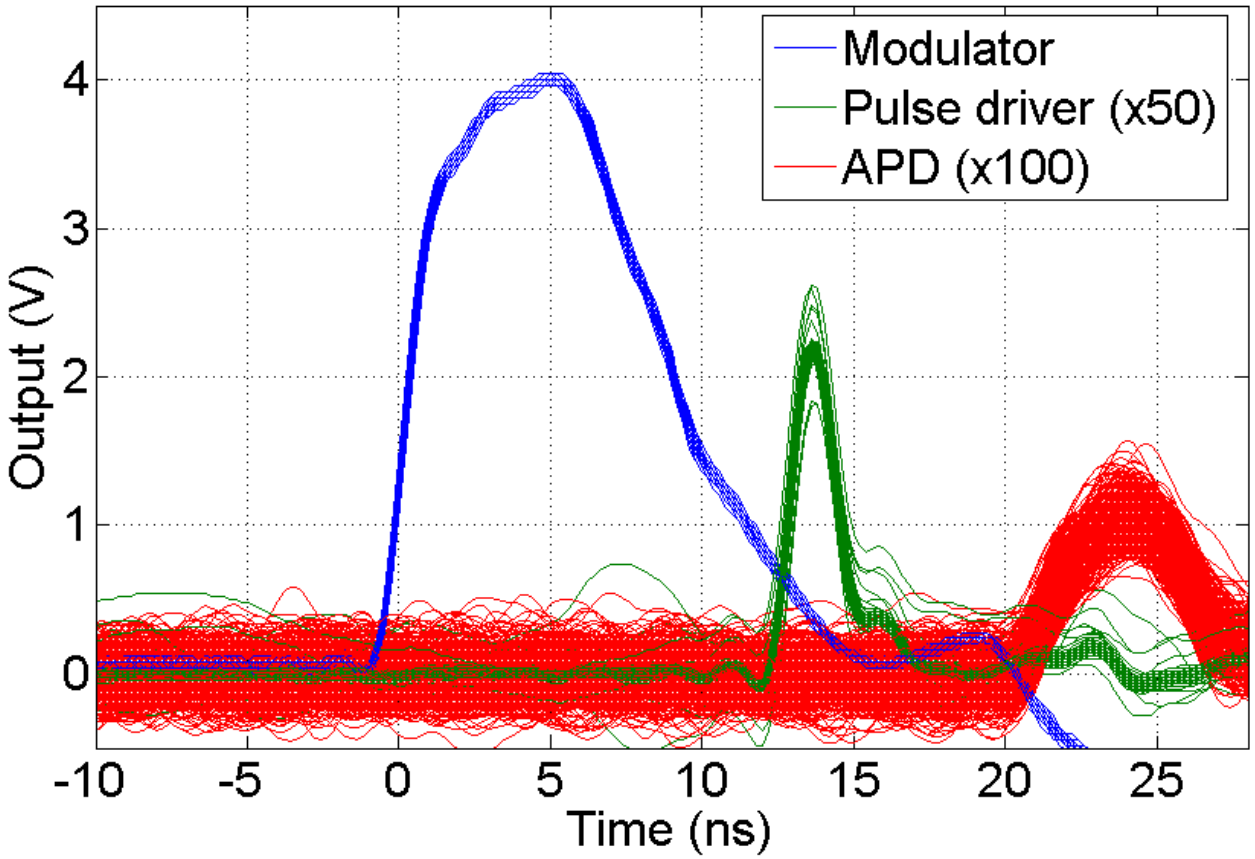


MOPFA Hardware: Seed Laser

- 1550 nm, 1 to 2 GHz laser diode
- Highland technologies 200 ps pulse driver



Premilinary Results



Component	Jitter (ps)
Modulator	27
Pulse Driver	52
APD	244

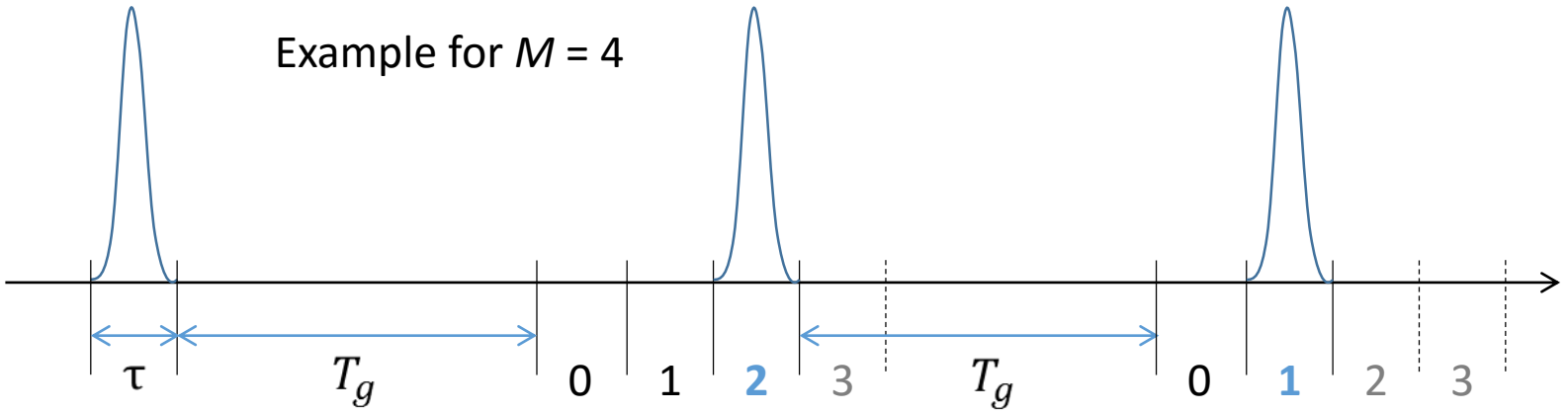
- Single ended, unterminated modulator signal
- Commercial APD BW limit (< 100 ps with custom design)

Differential Pulse Position Modulation

- The guard time starts immediately after the previous pulse
  - Increased data rate
  - Reduced noise immunity: 2 symbols lost when 1 pulse is missing
  - Increased ground segment complexity as 1st slot position is changing

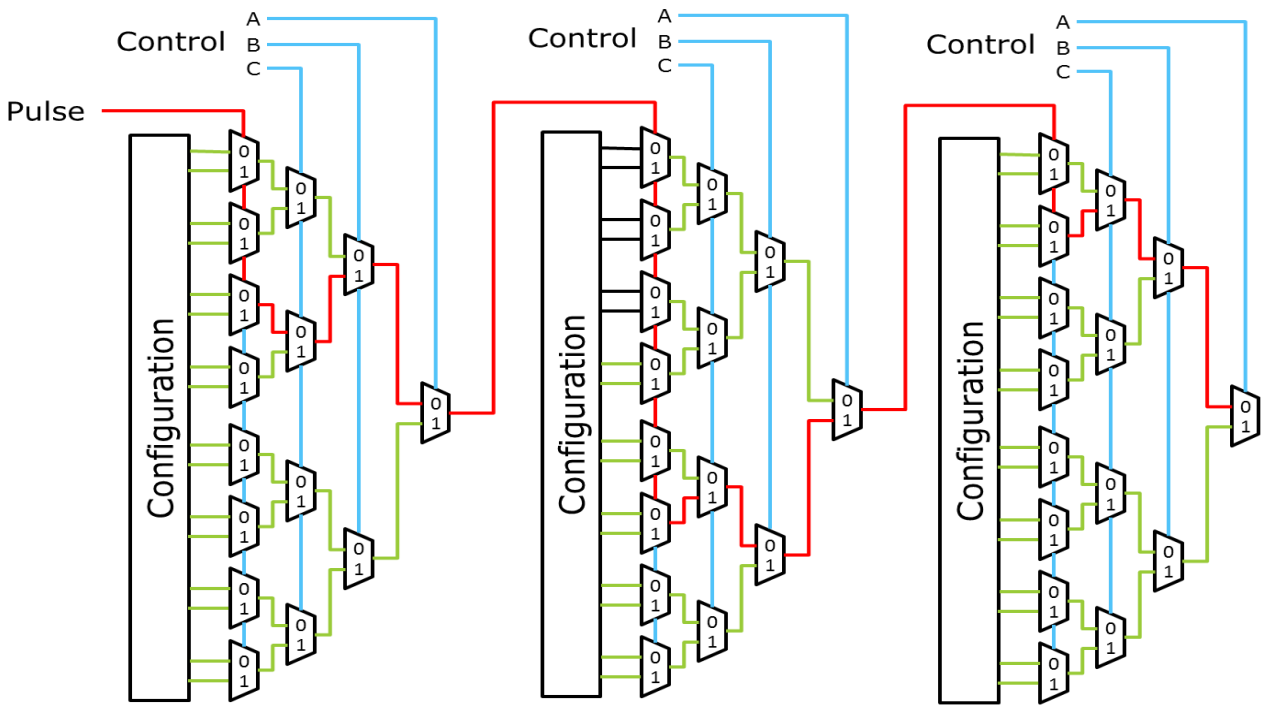
$$D_{PPM} = \frac{data\ per\ pulse}{average\ time\ per\ pulse} = \frac{\log_2 M}{(M+1)\tau/2 + T_g}$$

τ = slot width
T_g = guard time



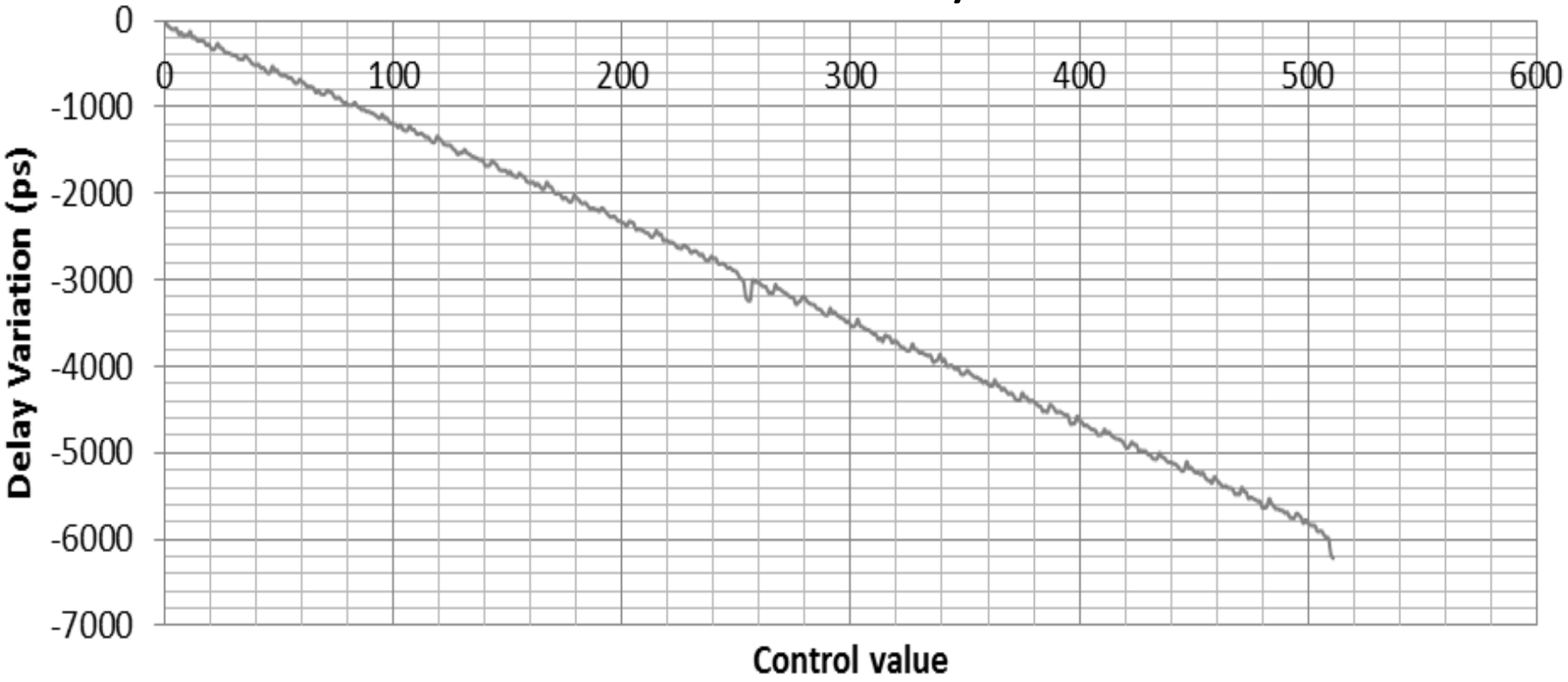
Delay Chain

- Coarse resolution: counter (5 ns)
- Fine resolution: delay chain (<10 ps)
- Methodology: Route electrical pulses through different elements of FPGA → different delays



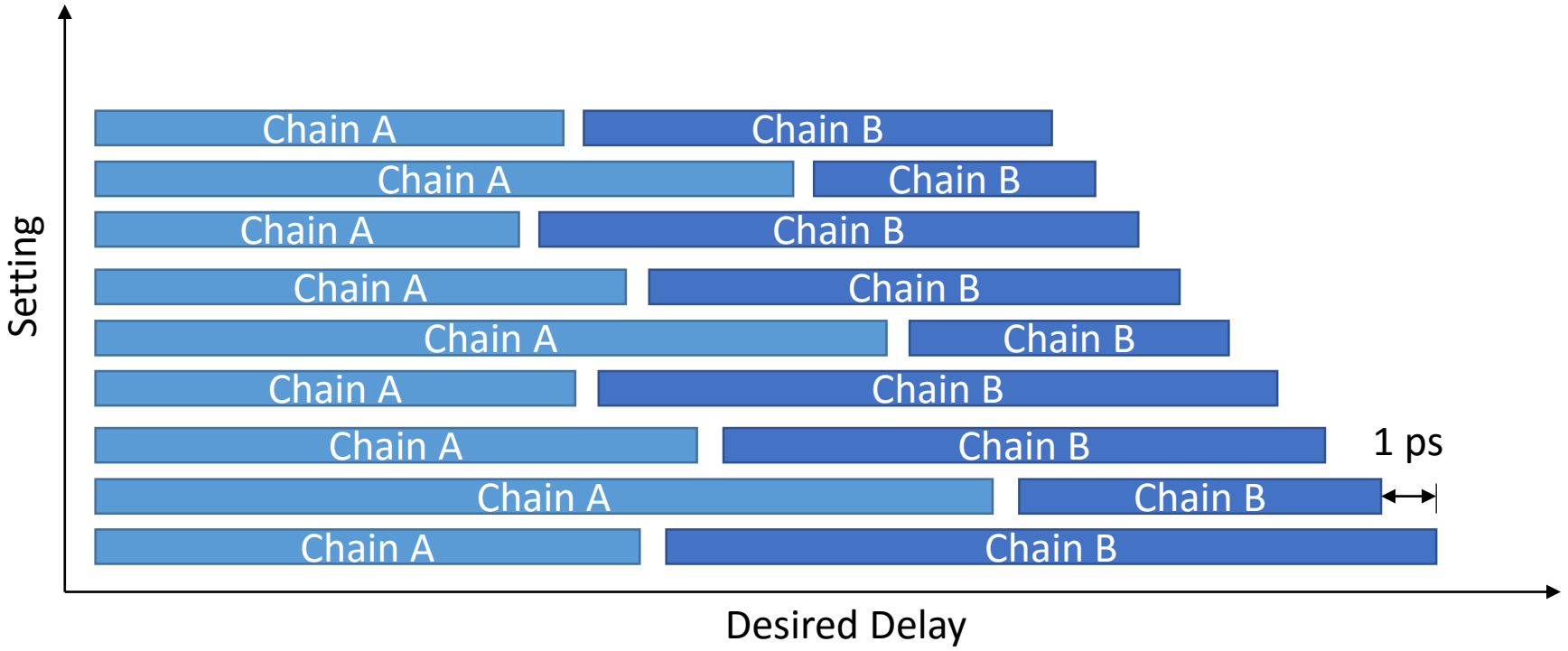
Delay Chain Performance

- Methodology: Route electrical pulses through different elements of FPGA → different delays



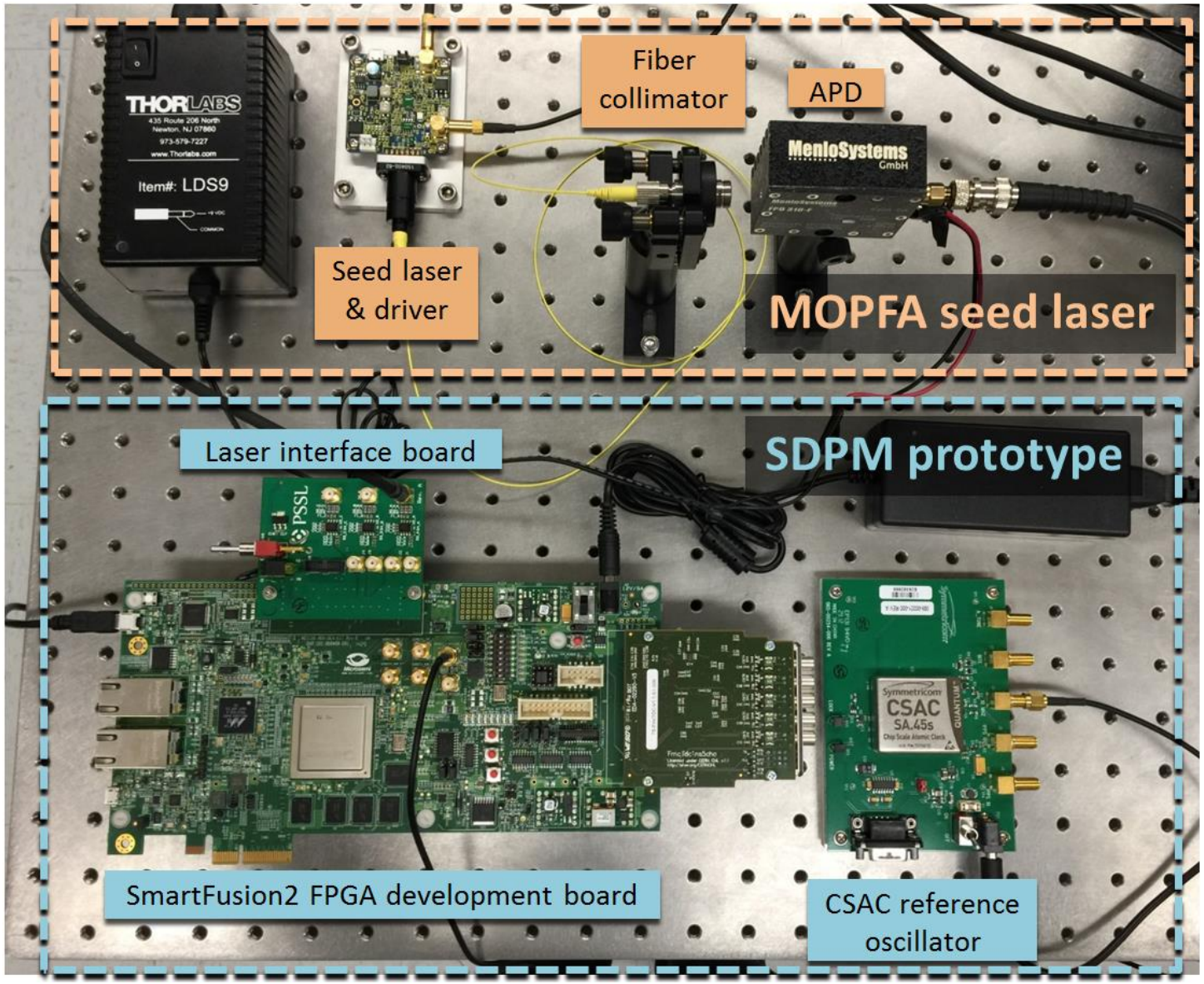
- Measured on die by DLL circuit
- 6 ns variable delay + **6 ns static delay**, **~3 ps jitter**, for 256 elements
- Typical 1 bit increment = 12 ps, **> 92 ps nonlinearities**

Balancing with 2 Delay Chains

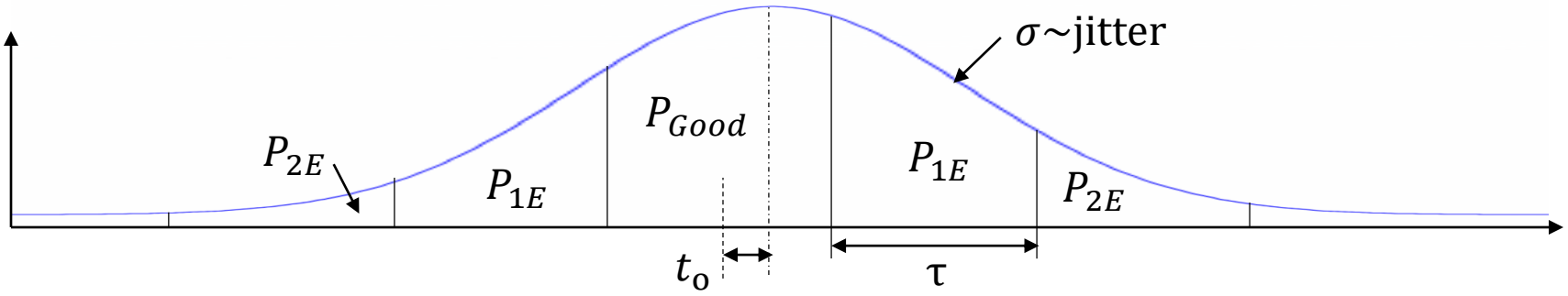


- Need at least 5 ns of delay variation : 2 chains required
- Result: 1 ps monotonic steps with selected delay chain pairs

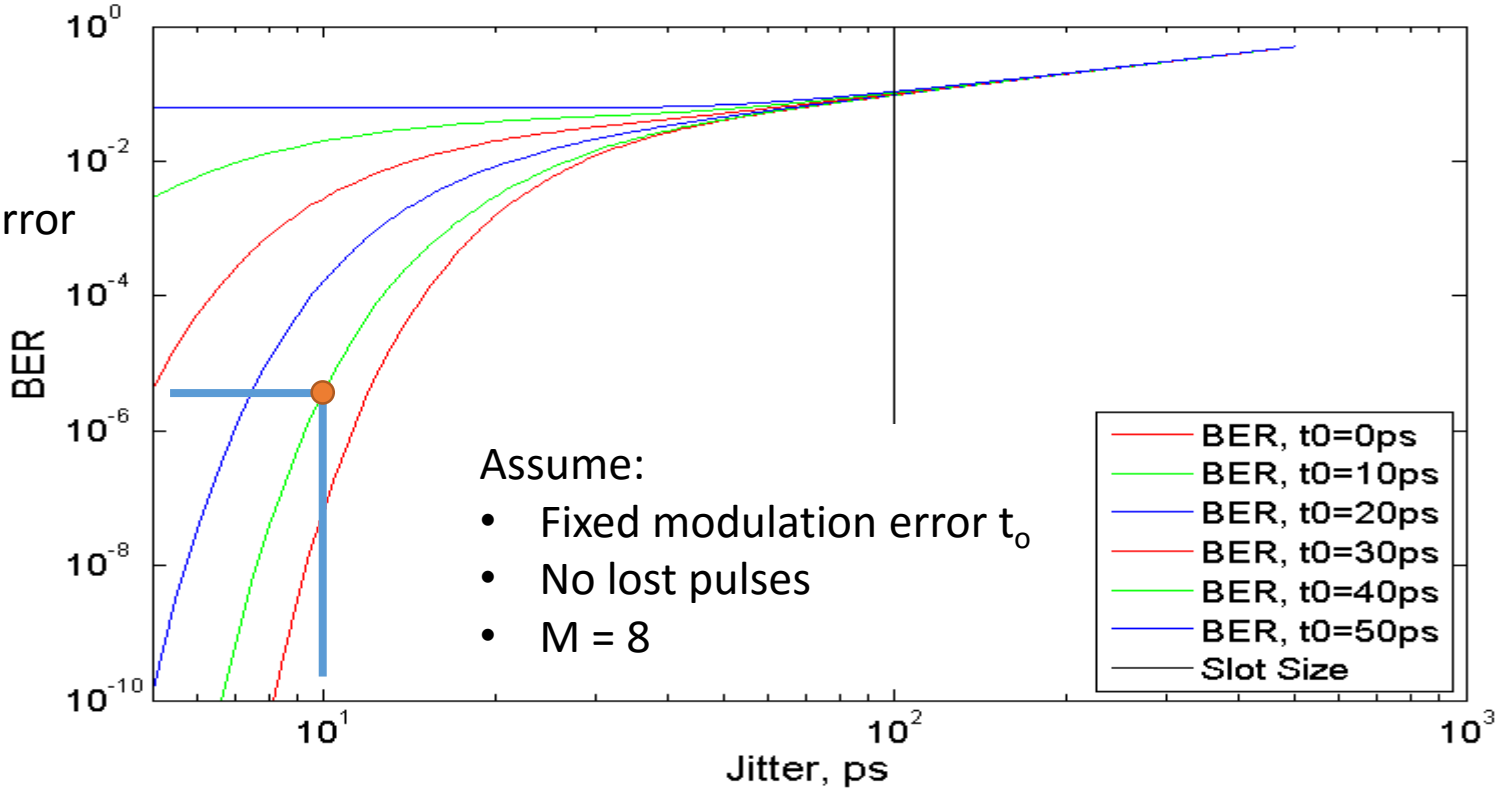
1st Prototype



Uncoded, Theoretical BER



10 ps systemic error
+ 10 ps jitter :
< 10^{-5} BER
without ECC

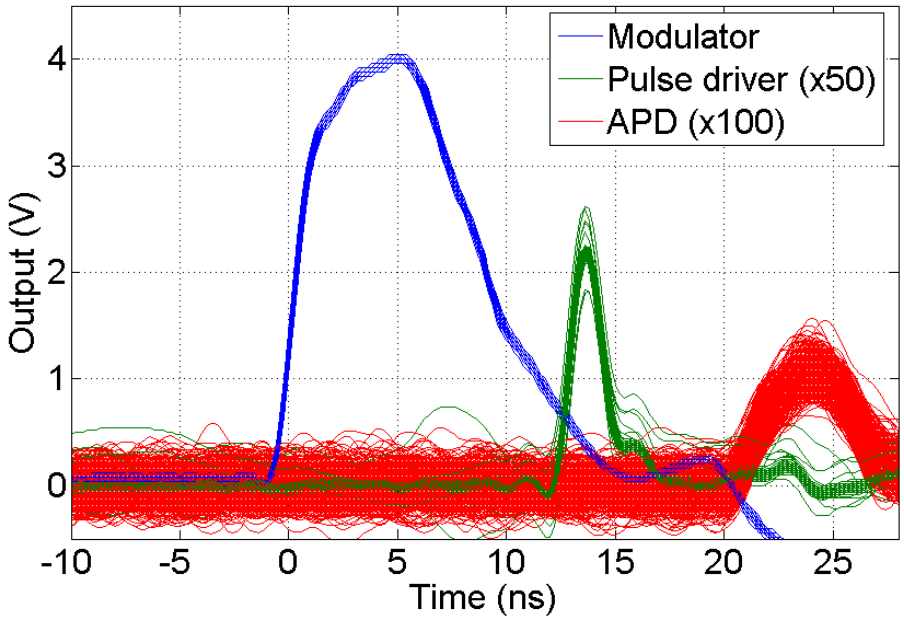


Optical Pulses from Detector

~100 optical pulses generated by seed, measured by APD

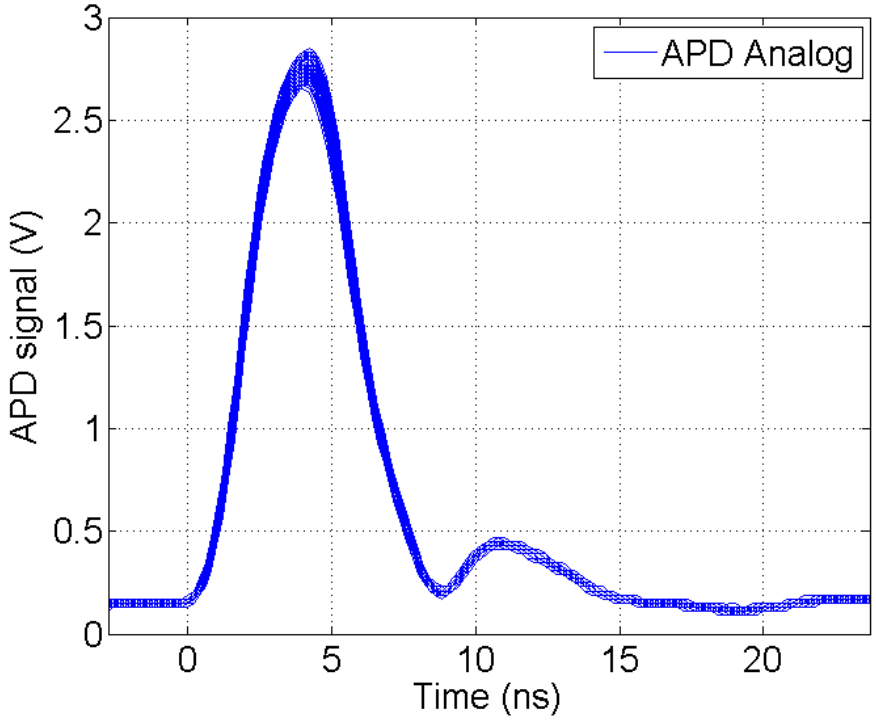
Previous results

- Modulator: 27 ps
- Pulse Driver: 52 ps
- Commercial APD: 244 ps



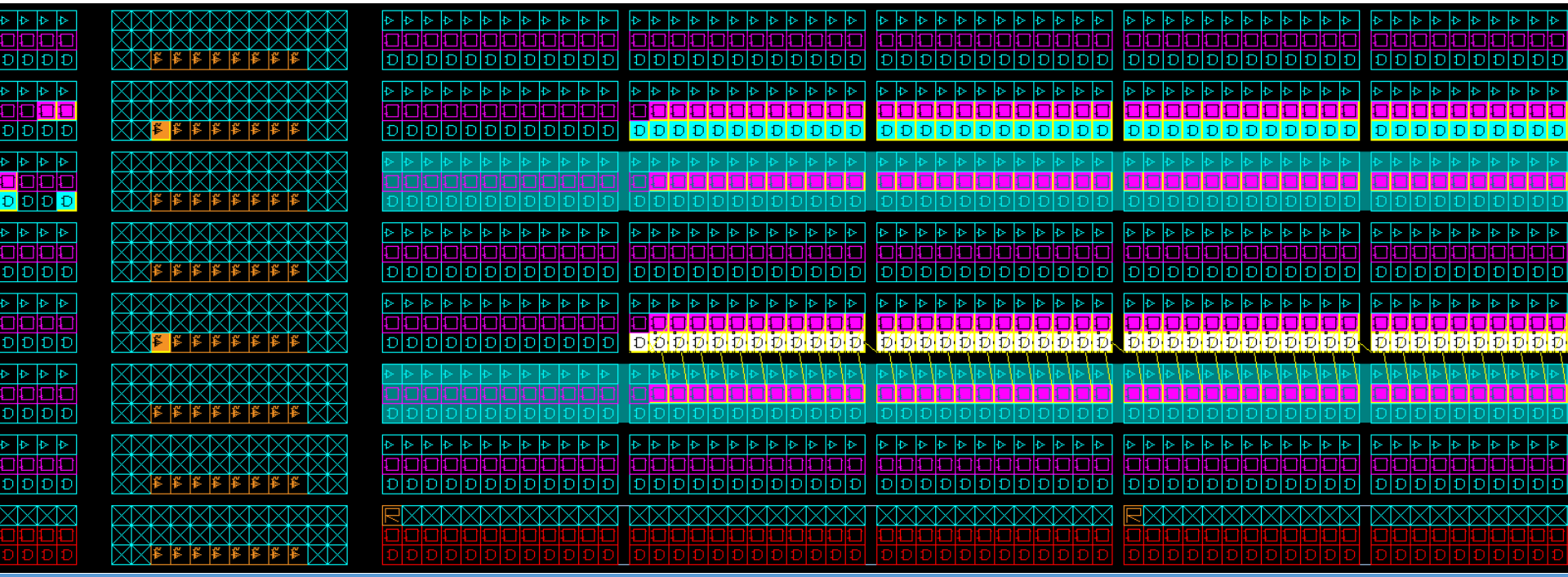
Custom APD

- Custom APD analog: 47 ps
- Custom APD digital: 52 ps
- Likely limited by seed laser driver

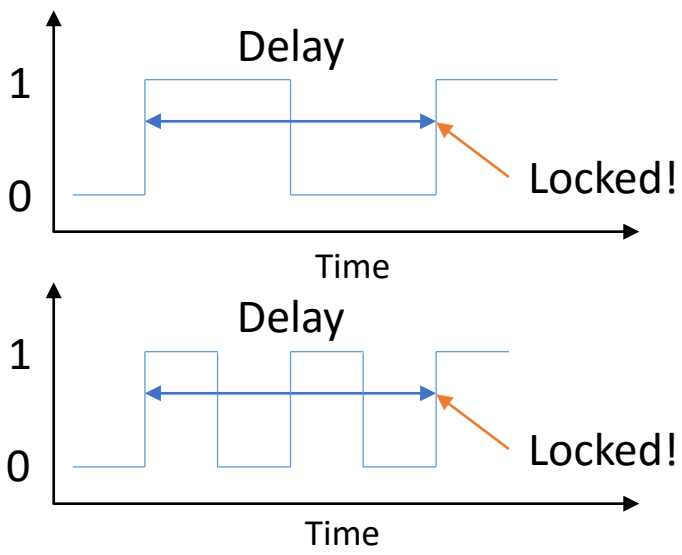


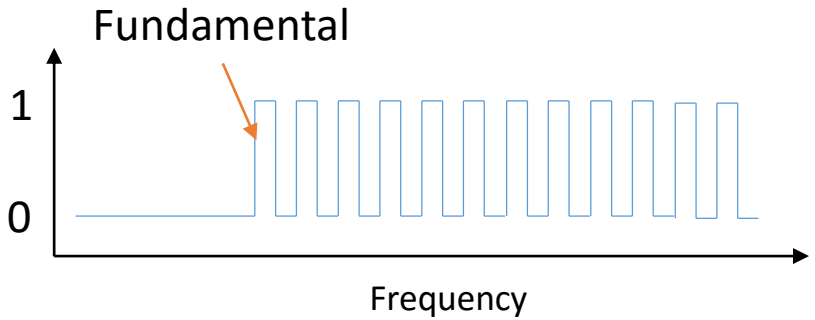
Chain realization

- Hardware described with general logic tile macro (ARI1) from Verilog library
- Automated VHDL generation, using python.
- Automated placement (.pdc) generation, using python
- Libero “SmartDesign” for interconnects.
- DLL piloted by python script on UART or modulator with time vector from UART

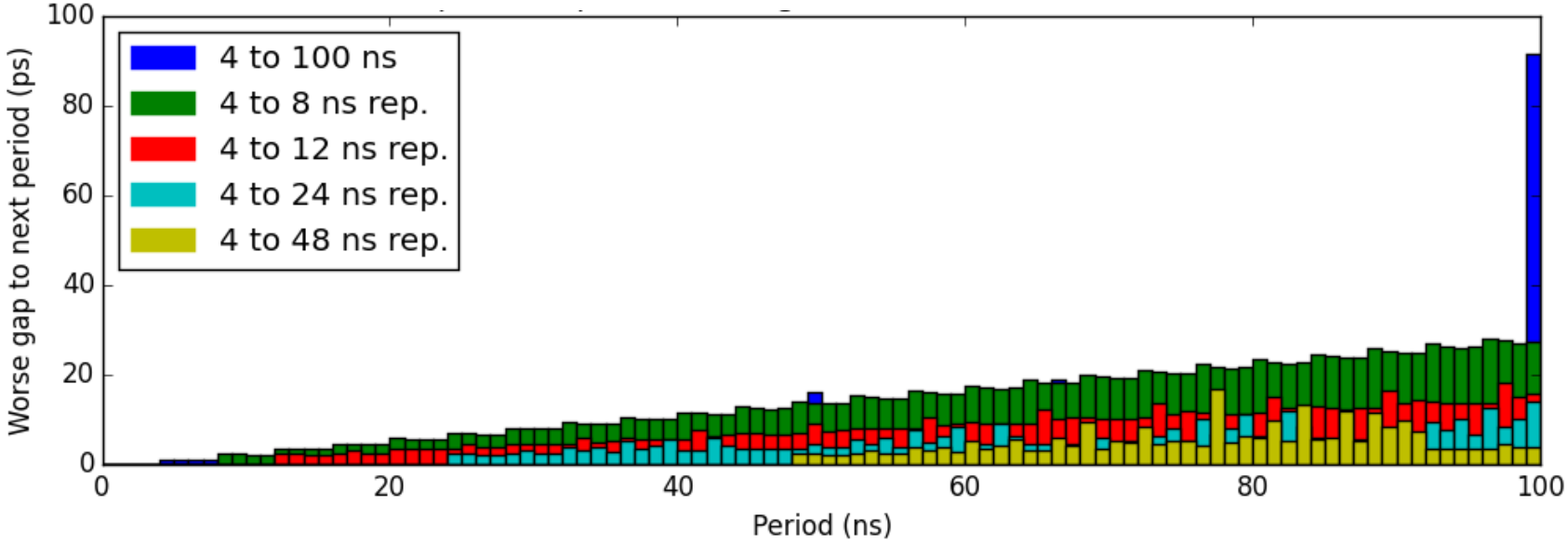


DLL “Digital Harmonics”



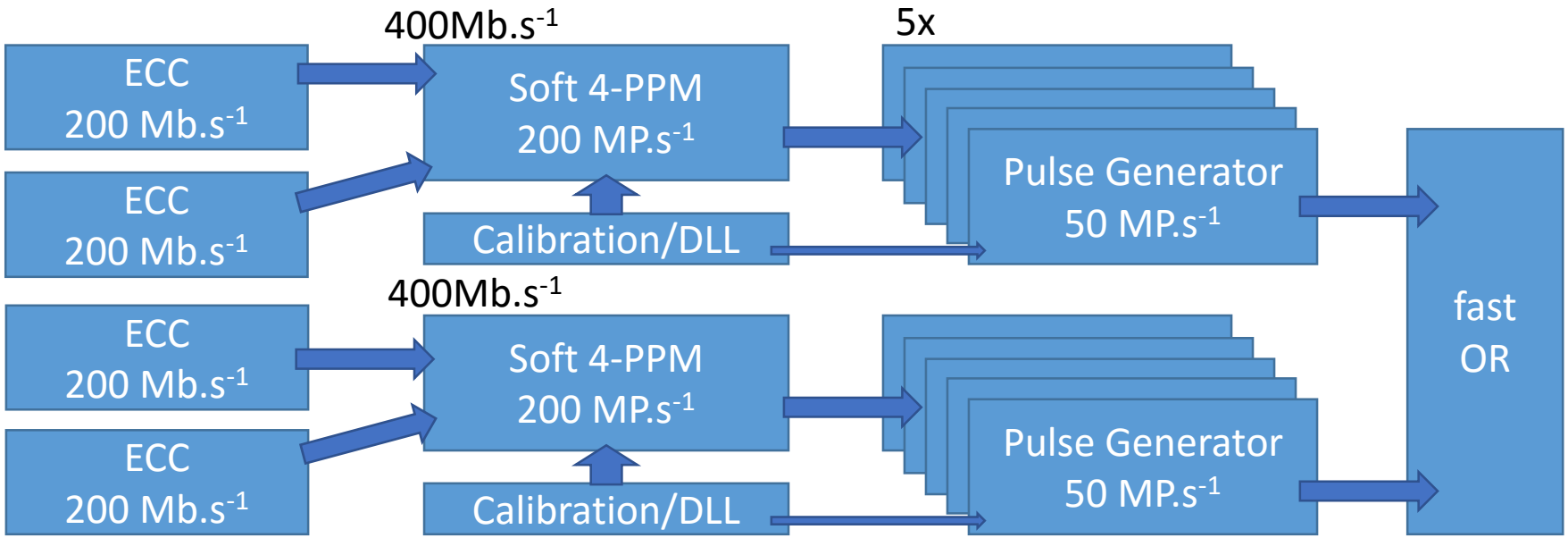


- If you can lock for F, then also for all $n \cdot F$
- The resolution is divided by n
- Find mode: $n = \frac{T_{n+1}}{T_n - T_{n+1}}$ (Tested)



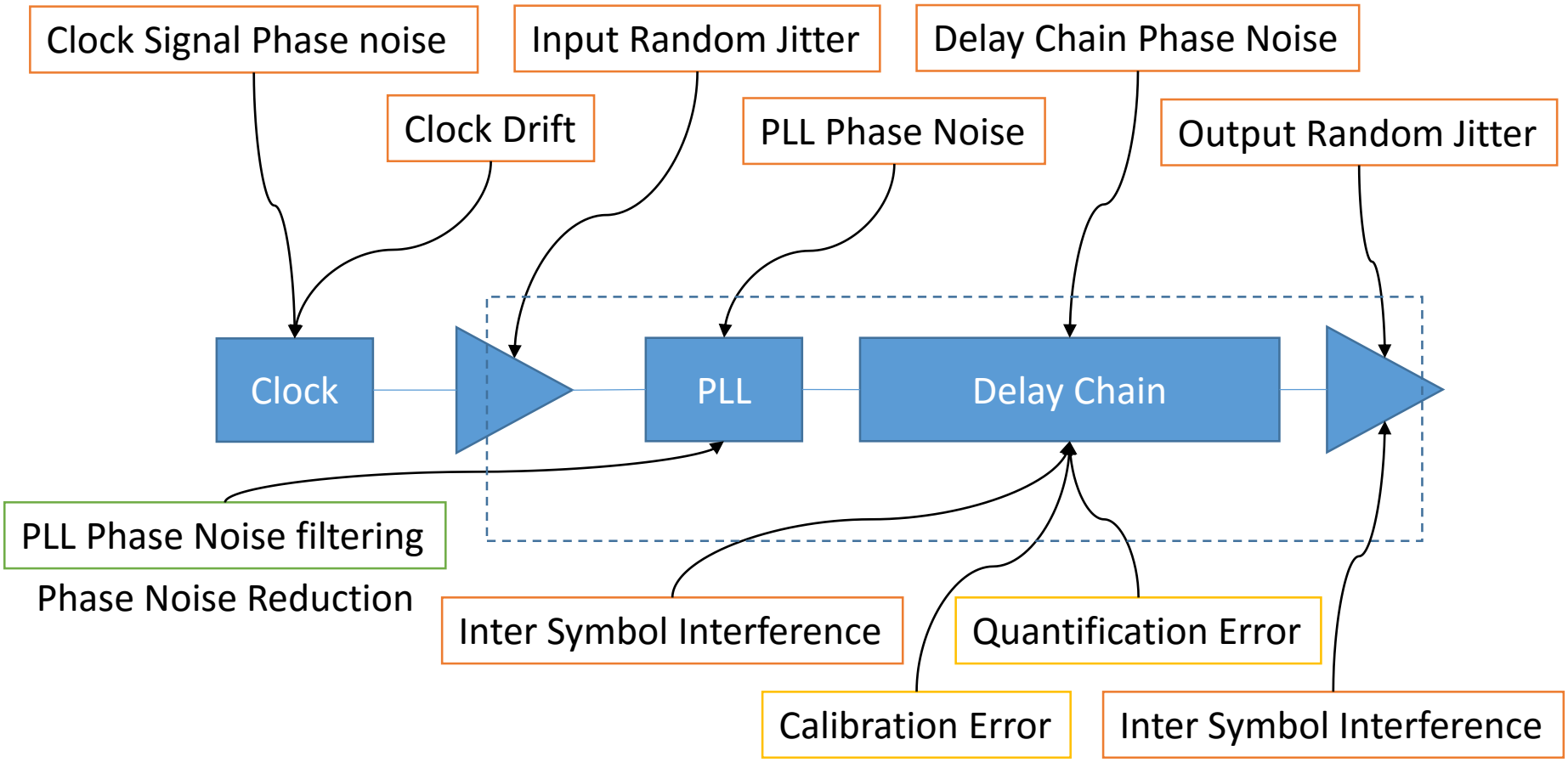
Modulator Scalability

- Pulse Generator are limited by the delay chain.
- We probably are limited at 50 Mpulses by second on smartfusion2.
- Can have several pulse generator for one timestamp FIFO, and several FIFO
- May need to switch to fixed-size code (like non-differential PPM) to put PPM encoder in parallel.
- If delay chain are always working on data, we will need extras for calibration.
- Crosstalk?



Modulator Error Sources

Random Sources (Gaussian)



Systematic Sources (not Gaussian)