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FPGA-based GPS Receiver for Nanosatellite Applications

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Background

This poster is about an FPGA-based GPS receiver design intended for CubeSat applications. CubeSats are a class of small Nanosatellites weighing approximately 1 kg to 3 kg in mass. Due to the small size and mass of the satellite, there is limited room and power available to the subsystems and payloads.

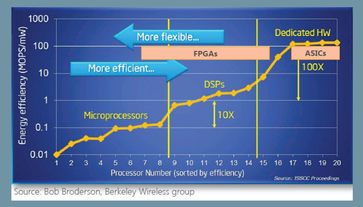
Implemented on a satellite, a GPS receiver can be used for time and location information, but by carefully examining the signal, it can also be used for atmospheric research or satellite attitude determination. The different GNSS systems are constantly evolving by being augmented with new signals. An FPGA is well suited for GPS / GNSS receiver applications as it combines the hardware performance of an ASIC and reconfigurability of software.

ASIC vs SDR vs FPGA

Commonly used in consumer GPS receiver are Application Specific Integrated Circuit (ASIC) chips. Commercial GPS ASICS have built in limitations on the operating altitude and velocity due to governmental regulations, preventing ASIC-based GPS receivers from being used in space applications.

Software Defined Radio (SDR) GPS receivers, as the name implies, utilize software to implement their processing. A SDR GPS receiver is one alternative to ASICs for use in space, as software can be changed and customized. However, a processor needs to operate at significantly higher clock speeds compared to an ASIC to achieve similar performance.

FPGAs are similar to ASIC, in that they use hardware to implement the processing logic. Unlike an ASIC, FPGAs consists of many reconfigurable logic elements and interconnections. Their reconfigurability allows for flexibility, similar to software, where different designs can be programmed onto a device.



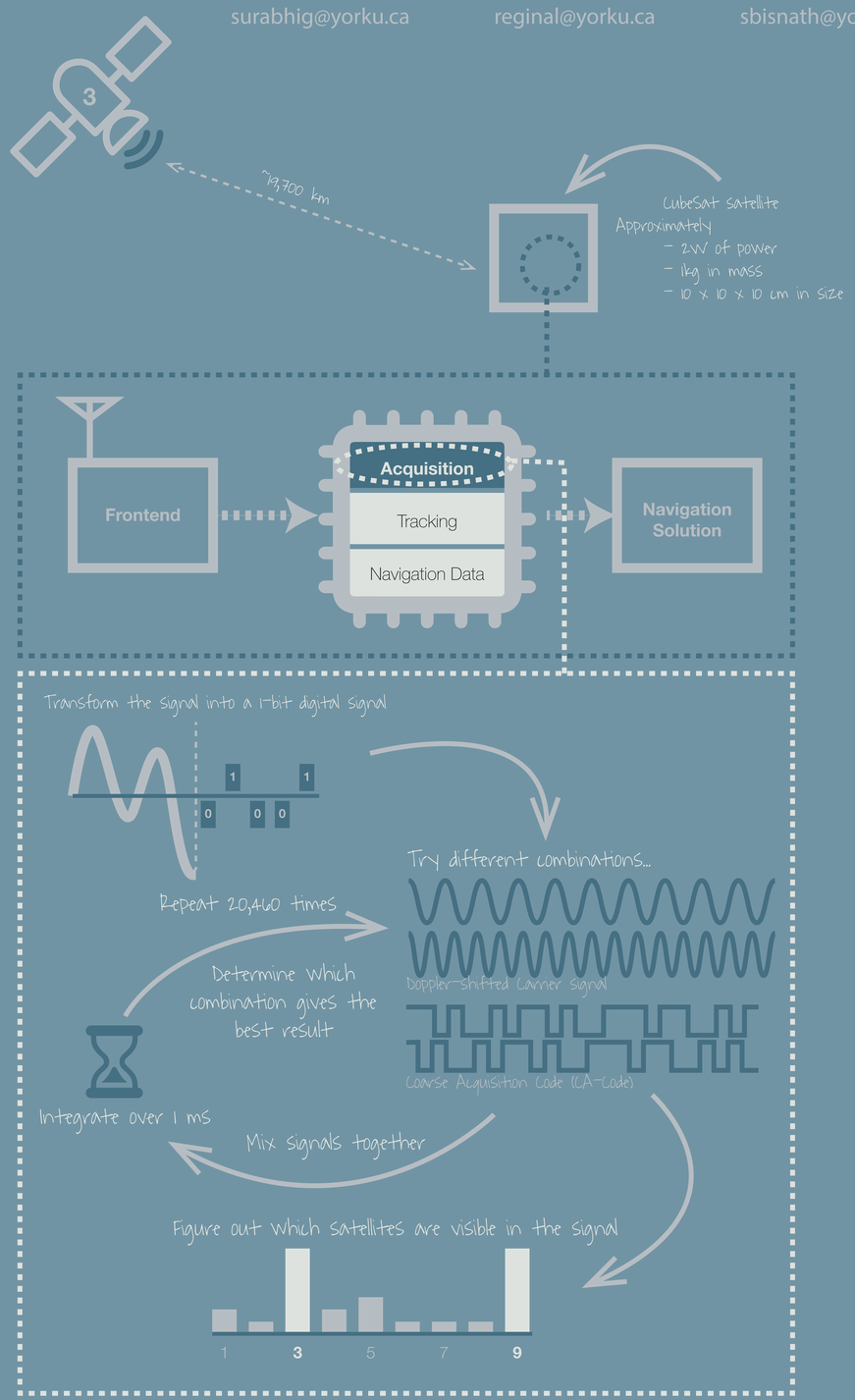
Source: Bob Broderson, Berkeley Wireless group

Time-Domain Serial Acquisition

Before a GPS receiver can determine its position, it needs to determine the satellites that are visible in the received signal, this process is called acquisition. During acquisition, two important parameters are determined, the Doppler-shifted carrier frequency and the phase of the Coarse-Acquisition (CA)-code belonging to the visible satellites.

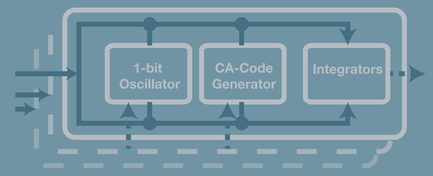
This particular design uses the serial-acquisition process, meaning it sequentially goes through each possible Doppler frequency and CA-code phase in the time-domain, to determine the combination that gives the correlation value.

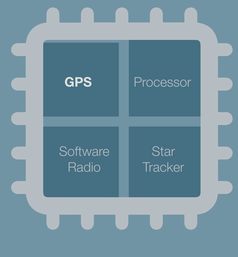
An alternative to serial-acquisition process is parallel-acquisition, where the processing is done in the frequency-domain via Fourier and inverse Fourier transforms. The transformations are performed using Fast Fourier Transforms on an FPGA, but they use a large portion of the available logic elements on an FPGA to accomplish this task. The serial-acquisition results in a slower acquisition time, but uses less logic elements, allowing for either a smaller FPGA to be used or additional designs to be implemented on an FPGA.



Implementation

The correlator module consists of a 1-bit NCO to generate the replica carrier signal and 32 acquisition channels. Each acquisition channel contains a CA-code generator, state machine and accumulators. The parameters of the carrier generator NCO and each acquisition channel, along with the integrator results are stored in a register file accessible by the processor. The code sequence for the CA-code generator of each channel is controlled through software, allowing for each acquisition channel to be assigned to look for different GPS satellites, or to correlate different phases of the CA-code for one GPS satellite.





Compared to Frequency-Domain Acquisition

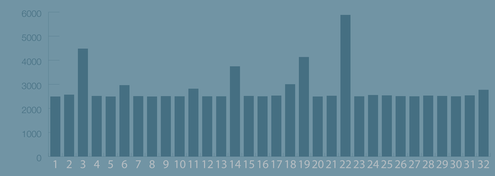
- 1-bit Oscillator design does not use any memory blocks
- 1-bit signal does not need multipliers for mixing signals
- Tracking channels can be used for acquisition
- Search parameters such as frequency range, step size, and the CA-code generators can be changed through software without re-compiling the hardware design
- Small baseline design can fit on an FPGA alongside other designs
- Scaleable, performance can be increased by:
  - Adding more acquisition units
  - Increasing clock speeds
  - Multiple sequential acquisitions

	Serial-Search channel	32 Channel Serial-Search	1024-point FFT IP Core
Logic Elements	407	14213	673*
Registers	139	4936	1508
Memory (M10K blocks)	0	0	6

Results

The design currently has 32 acquisition units and searches a frequency range of ±5000 Hz in 500 Hz increments. Using a 16.368 MHz clock took 42 seconds to acquire satellites from 1 ms of data

Using a 50 MHz clock, the same process took approximately 13 seconds - 3x performance increase



Conclusion

The GPS baseband receiver design discussed in this paper is a feasible design for CubeSats because of its small size, allowing it to be used on a single FPGA along side other designs. What makes the small size possible is the time-domain implementation, which does not use memory bits and utilizes a small amount of DSP units.

In future implementations, the design of the acquisition channels can be expanded to be used as tracking channels, allowing for the acquisition channel to be used for acquisition and later tracking without relying on separate hardware for each purpose.