ARC FAULT CIRCUIT INTERRUPTER DEVELOPMENT FOR RESIDENTIAL DC
ELECTRICITY

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                    Residential DC Electricity

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ABSTRACT

Arc Fault Circuit Interrupter Development for Residential DC Electricity

Cassidy Alan Aarstad

The following technical report describes the development and testing of an arc fault circuit interrupter (AFCI) for DC circuits operating primarily at 48 volts. We have identified an effective method for determining when arcing is occurring. Our method is primarily based on comparing the frequency spectrum of current flowing through the circuit during an arcing event to a known characteristic spectrum. Once an arc has been identified, our interrupter is capable of responding adequately to eliminate the arc. Hardware tests show the AFCI developed in this thesis responded, in all test cases, within 2 seconds of an arc fault occurrence. Commercialization and adoption of our interrupter will increase the safety of DC circuits operating at 80 volts or less.

Keywords: Arc Fault Circuit Interrupter, AFCI, DC, direct current, low voltage, frequency spectrum

ACKNOWLEDGMENTS

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EXECUTIVE SUMMARY

Introduction

The use of direct current (DC) electricity in California homes will likely increase in the future due to greater adoption of residential photovoltaics and increasing use of electric (and plug-in hybrid) vehicles. While less certain to occur, there are also a lot of benefits to powering entire homes on direct current. A "DC house" has direct benefits like reduced energy consumption due to fewer conversions from alternating current (AC) to DC, and secondary benefits like potential increase of photovoltaic panel and electrical vehicle sales due to higher overall system efficiencies and shorter payback times. Perhaps the home of the future will be a "hybrid", with some loads served by alternating current and others direct current.

An Arc Fault Circuit Interrupter (AFCI) is a special circuit breaker that detects and eliminates unintended electrical arcs, which can cause a fire. Electrical arcs, also known as arc faults, occur when current jumps from one conductor across an air gap to another conductor. The high temperatures generated by an electrical arc are a fire safety concern, regardless of whether AC or DC electricity is being used. The U.S. Consumer Product Safety Commission estimates roughly 18,000 residential fires are started each year due to electrical wiring, with some indication that one-third of those are specifically due to electrical arcing [1]. While these statistics relate to the standard AC electricity available in most residences, as the use of DC electricity increases, the risk of fire due to arcing of DC electricity also increases. Unfortunately, reliable detection of arc faults and determining the appropriate response is particularly difficult in DC circuits. Because DC does not pass through a zero-current state like AC, a DC arc is more likely to maintain itself.

The National Electric Code (NEC) and Underwriters Laboratories (UL) have recently developed requirements for AFCIs for photovoltaic systems with DC circuits operating at 80 volts or greater [8], [9]. Despite these adopted specifications, these AFCIs are still in development for many

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manufacturers and there is little consensus on the best approach. Virtually no research has occurred on protecting household DC circuits from arcing. These circuits are likely to be at voltages less than 80 volts, but still at a high enough voltage to cause significant fire risk if arcing were to occur.

Project Purpose

Our research program focused on developing an Arc Fault Circuit Interrupter for a DC-powered house. In the context of increasing the efficiency of California's electric power supply, safety is the primary objective of this research project. Arcing events in electrical circuits are a major fire risk, and AFCIs can significantly reduce this risk. Arc Fault Circuit Interrupters are currently in development for 80 volts or higher photovoltaic circuits, but we developed a prototype AFCI for DC household plug circuits operating at primarily 24-80 volts. This new application of the AFCI has its own unique challenges due to the diversity of loads that may be present in household plug circuits.

Project Results

Change to the frequency spectrum of the DC electricity was chosen as the marker of an arc occurring. Consequently, the frequency response due to a DC electrical arc was studied carefully. Each experiment varied the parameters of the components used to ensure likely variations were accounted for in the spectral response characterization. Series arcing and parallel load arcing were tested in this manner. The impedance and characteristics (passive and active) of the loads were varied as well as the models and manufacturers of each component and device used (power supply, current transformer, spectrum analyzer, cables, and contacts). The DC power supply

voltage was varied between the minimum voltage required to create an arc, and 80 volts. The contacts used in the Arcing Device were interchanged with various materials, contact shape, and size. Results showed that if an arc is occurring, it will create noise content at every frequency within the observed range (244 Hz-100 kHz), though the amplitude distribution may vary depending on components used.

To provide a robust system, a predictable shape in the frequency response during an arc is needed; having a predictable shape will allow a microprocessor to compare and map several sample points to an arcing "signature" and, upon a successful match, send a shutoff signal to a current controller. To accomplish a reliable and repeatable response despite differing system parameters and components, an analog gain and filter system was designed to achieve a specific response by forcing the arcing noise to a predefined shape.

A full-featured spectrum analyzer will not be available for use in a low-cost AFCI. Instead, a microprocessor from Microchip is used for analysis and logic. The on-chip analog-to-digital converter was used with a sampling rate of 250 kHz, satisfying Nyquist criterion up to 125 kHz. Once the entire design of the AFCI was finalized and tested, it was then implemented on a printed circuit board to demonstrate its low-cost reproducibility.

The UL standard for DC arc fault circuit interrupters requires a shutoff signal to be sent within 2 seconds of an arc occurring [9]. During testing, the AFCI design detailed in this report had a response time between 8 ms and 54 ms, which is well within the requirement. With that significant of a margin, several improvements can be made in the software to prevent false positive detections (nuisance trips) by utilizing averages across more sample sets, and performing more complex processing.

Project Benefits

A DC-powered (or partially DC-powered) home could become a component of a future, smart electrical network that increases the security, quality, reliability, and affordability of the electric power system. Safety is paramount with these systems, which is why we have developed here a low-cost Arc Fault Circuit Interrupter (AFCI) for residential direct current electricity. We believe the DC AFCI is a technology that will enable better energy efficiency, accelerate adoption of electric vehicles, enhance service reliability, and of course, increase safety.

CHAPTER 1:
Introduction

1.1 Residential Direct Current Electricity

For a multitude of reasons, the use of direct current (DC) electricity in California homes will increase in the future. These reasons include: greater adoption of residential photovoltaics (PV), increasing use of electric (and plug-in hybrid) vehicles, and more air conditioners/furnaces equipped with variable speed drives (which use DC internally). While less certain to occur, there are also a lot of benefits to powering entire homes on direct current [2], [3]. A "DC house" has direct benefits like reduced energy consumption due to fewer conversions from AC to DC [4], and secondary benefits like potential increase of PV and electrical vehicle sales due to higher overall system efficiencies and shorter payback times. Perhaps the home of the future will be a "hybrid", with some loads served by alternating current and others direct current. While at first glance, this may seem unlikely, this exact situation presently exists with telephone lines, Ethernet wiring, and normal electrical power all in one home.
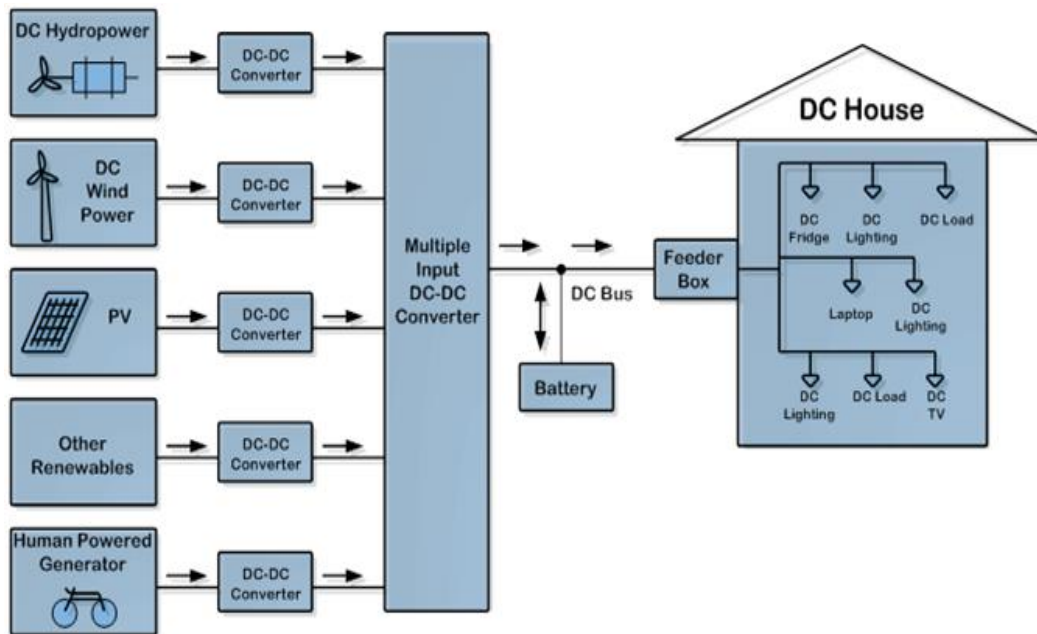
Figure 1-1: Cal Poly's DC House Project

[2], [5], and [6] have previously summarized the benefits and barriers to using DC microgrids in the United States. Rather than spend a lot of time recreating the "battle of the currents," we feel it is our responsibility as engineers to simply do our best to enhance quality of life at the lowest financial and environmental cost. We do not know what the future holds regarding DC residential microgrids, but we want to be sure that technology exists to make the use of DC electricity as safe as possible.

1.2 Arc Fault Circuit Interrupters

An Arc Fault Circuit Interrupter (AFCI) is a special circuit breaker that detects and eliminates unintended electrical arcs, which may cause a fire. The U.S. Consumer Product Safety Commission estimates roughly 18,000 residential fires are started each year due to electrical wiring, with some indication that one-third of those are specifically due to electrical arcing [7]. Arc faults are a fire-safety concern in both AC and DC residential wiring, but reliable detection of arc faults and determining the appropriate response is particularly difficult in DC circuits. In fact, the Electric Power Research Institute has referred to extinguishing arcs as the "achilles heel" of direct current [3]. Because DC does not pass through a zero-current state like AC, a DC arc is more likely to maintain itself. It is obviously important that DC arcs be reliably detected without false alarms by an AFCI. An additional complication is that the appropriate corrective action for series arcs can be the opposite of the action necessary for parallel arcs, depending where in a circuit the arcing is taking place.

The NEC and UL have recently developed requirements for AFCIs for PV systems with DC circuits operating at 80 V or greater [8], [9]. Despite these adopted specifications, these AFCIs are still in development for many manufacturers and there is little consensus on the best approach. Virtually no research has occurred on protecting household DC circuits from arcing. These circuits are likely to be at voltages less than 80 V, but still at a high enough voltage to cause significant fire risk if arcing were to occur.

1.3 Research Purpose

Our research program focused on developing an Arc Fault Circuit Interrupter (AFCI) for a DC-powered house. In the context of increasing the efficiency of California's electric power supply, safety is the primary objective of this research project. Arcing events in electrical circuits are a significant fire risk, and AFCIs can significantly reduce this risk. Arc Fault Circuit Interrupters are currently in development for 80 V or higher photovoltaic circuits, but we developed a prototype AFCI for DC household plug circuits operating at primarily 24-80 V. This new application of the AFCI has its own unique challenges due to the diversity of loads that may be present in household plug circuits.

We integrated AFCI abilities into our existing Smart DC Wall Plug. As described below, the Smart DC Wall Plug is an electrical outlet powered from a single DC voltage bus and can automatically sense the required DC load output voltage. This eliminates the need for each appliance to have its own DC-DC converter, but the use of a Smart DC Wall Plug presents a major challenge to detecting arc faults. Whenever you have DC-DC converters, certain types of arc faults could trick an AFCI into taking inappropriate control actions and worsen the problem. Our design can detect series, parallel, and ground arcs, which is more general than the series arc focus of NEC 690.11. We also ensured that our design successfully detects and responds to arcs for both true DC and rectified DC electricity.

At present, the AFCIs required in residential AC wiring cannot detect arcing downstream of any AC-DC converters. We were able to develop a system which is able to detect arcing downstream of a DC-DC converter, so we feel our system, if implemented, is safer than the current system required by most electrical codes in the U.S.

1.4 The Smart DC Wall Plug

A related previous research project of ours is the "Smart DC Wall Plug for DC House." This is an electrical outlet powered from a single DC voltage bus and can automatically sense the required

DC load output voltage [10]. One major challenge in a DC House is that existing DC electrical loads operate at different voltage levels from one DC bus voltage [11]. It will be costly and not practical to have a unique individual DC wall plug for each required DC load voltage. A more economical and practical approach would therefore be a common DC wall plug that will work for any DC load. The "Smart DC Wall Plug for DC House" that we have developed takes in one DC bus voltage and it outputs a suitable DC voltage required to operate any typical DC load.

1.5 Technical Approach

As we originally proposed, we have designed, built, and tested a prototype low-voltage AFCI for a DC House. The AFCI has been incorporated into the Smart Wall Plug, which was recently developed at Cal Poly State University [10]. The Smart Wall Plug provides a single converter solution for automatic detection of multilevel output voltages required by various DC loads.

Key design specifications are included in Table 1-1:

Table 1-1: Design Specifications for our DC Arc Fault Circuit Interrupter

Maximum Current = 12.5 amps
Maximum Voltage = 80 volts DC
Response Time = shutdown within 2 seconds
Capable of detecting arcs on both sides of Smart Wall Plug
Avoids nuisance tripping
Easily reset after a tripping event

Prior to the construction of the proposed AFCI, we characterized the frequency response of arc faults in conjunction with the DC house. Such characterizations were critical since wiring conditions may filter arc fault noise frequencies, causing the AFCI to fail to trip and extinguish the arc [12], [13]. Compared to grid-connected DC systems, the DC house poses unique challenges in protection system design primarily due to the use of mainly DC-DC converters (pure DC) instead of grid-connected rectifier (AC to DC), which has current-limiting capability

during faults [14]. The frequency characterization of arc faults was therefore performed on the multi-voltage DC outlet with its associated DC-DC converters to ensure that suitable sensing circuitry can be implemented in the AFCI design phase.

In addition, the characterization was done on both sides (input and output) of the DC outlet to see whether it was possible to detect both arc problems with one detector. Results from this characterization were useful in determining the best location to implement the proposed AFCI. A DC arc generator was used to initiate the DC arcs for the characterization by using a fixed and a movable electrode whose gap distances, shape, and material composition can be easily adjusted.

Upon completing the arc characterization phase, we began the design phase for the proposed AFCI. During the characterization phase and especially in the design and testing phase, we worked closely with industry collaborators who provided technical guidance, given their expertise in residential power system and protection as well as the integration of sensors and controllers into the AFCI system.

1.6 Final Introductory Thoughts

A DC-powered (or partially DC-powered) home could become a component of a future, smart electrical network that increases the security, quality, reliability, and affordability of the electric power system. Safety is paramount with these systems, which is why we have chosen to focus on arc fault circuit interruption for DC electricity. Consequently, we have developed an Arc Fault Circuit Interrupter (AFCI) for the DC house. We believe the DC AFCI is a technology that will enable better energy efficiency, accelerate adoption of electric vehicles, enhance service reliability, and of course, increase safety.

CHAPTER 2:
Background

IEEE defines an arc as "a continuous luminous discharge of electricity across an insulating medium, usually accompanied by the partial volatilization of the electrodes."

Section 210.12 of the National Electrical Code (NEC) describes an arc-fault circuit interrupter (AFCI) as "a device intended to provide protection from the effects of arc faults by recognizing characteristics unique to arcing and by functioning to de-energize the circuit when an arc fault is detected."

Information on DC arcing is currently not nearly as available, at least in the academic space, as AC arcing. However, many similarities exist and previous research into AC arcing can provide insight into DC arcing.

Arcing is often caused by degraded cable insulation, a frayed end of stranded wire, wire touching grounded conduits or tubing [15]. Loose electrical connections, wire cut by furniture or pierced by a nail also have the potential to cause electrical arcing [16].

The impedance path of an arc is typically high, limiting the current flow and therby preventing traditional overcurrent protective devices from opening. Despite a relatively lower current, the heat generated from an arc could be significant enough to become a fire hazard [15]. In AC systems, an arc is relatively short as it may extinguish when the current passes through the zero level of a normal sinusoidal cycle. However, DC systems do not have a zero current level crosses during normal operation. As a result, an arcing condition is more readily maintained in a DC system over a relatively large span of time [17].

Arcs in AC systems are often sputtering in nature as they'll extinguish then reignite each cycle as the voltage oscillates between 0V and a significantly high voltage [15]. In a DC system, a continuous arc can be expected.

Different arcing-faults exist – for example series arcing and line-to-ground arcing – that require different strategies to extinguish. A line-to-ground arc fault can be easily detected and extinguished using a GFCI with a fast response time, however using a GFCI requires a ground path to be present for this protection to be effective [15]. A possible protection scheme is to use only double-core cables with concentric grounded conductor shields that will force any arcing fault to be a line-to-ground fault and will be detected by a GFCI [16]. For this thesis, using special cable on all connections is not deemed practical in many circumstances and will not be considered solution in this thesis.

During an AC arc-fault some general characteristics have been determined [18]. Only a few characteristics can also be expected in a DC system:

- High-Frequency noise is seen in voltage and current waveforms

- The arc has a voltage drop across it; the arc has a nonzero impedance

- Arcing current is typically lower than nonarcing current in the same circuit

While the above points can be used for the detection of an arc, any intermittent connection, caused by a switch or otherwise, may cause an arc in a DC system [17]. As a result, purposeful switches, such as lightswitches, may cause very brief arcing that is not hazzardous; differentiating between purposeful arcing due to switches and hazzardess arc faults will need to be addressed.

PV systems are entirely DC systems and are therefore prone to sustained arcing. A series arc is most likely to occur in a PV system due to the large number or series connections in a solar array. PV systems are also typically exposed to thermal cycling and ultraviolet exposure, causing insulation degradation and electrical connection deterioration [17]. A significant portion of this thesis is dedicated to series arc detection and de-energization.

CHAPTER 3:
AFCI Design Requirements

3.1 Functional Requirements

Table 3-1 summarizes the specifications for the DC AFCI detailed in this thesis.

Table 3-1: Summary of DC AFCI Design Requirements

1.	Maximum Current = 12.5 amps
2.	Maximum Voltage = 80 volts DC
3.	Response Time = shutdown within 2 seconds
4.	Capable of detecting arcs on both sides of Smart Wall Plug
5.	Avoids nuisance tripping
6.	Easily reset after a tripping event

1. The maximum of 80 Volts DC was chosen as residential DC will likely be rated below 80 Volts DC. The DC House Prototype, for example, constructed at California Polytechnic State University San Luis Obispo is rated at 48 Volts DC

2. The DC house is also rated for 600 Watts. 12.5 amps is an appropriate and sufficient maximum rated current.

3. The arc interruption response time of the system requirement is taken from the UL standard for DC arc fault circuit interrupters. While an electrical arc is always a safety and fire hazard, interrupting the arc in under 2 seconds will significantly decrease its ability to cause irreparable damage. The AFCI designed in this thesis will allow for different relays to be used in the future should the power and voltage ratings change. Because different relays will have different response times, a strong effort will be made to minimize the response time of the detection circuitry to allow sufficient margin to accommodate slower relays if necessary.

4. Electrical arcing can happen at any point along power lines, both between the source and AFCI and between the AFCI and load. Being able to detect an arc regardless of location is necessary to further reduce safety concerns.

5. Nuisance tripping can cause inconvenience to the user. Unnessesary interruption of power can cause other safety issues (i.e. loss of lighting or plumbing) as well as loss of work, data, or information (i.e. unexpected computer shutdown). Nuesance tripping can incure financial loss and highten safety risks and therefore needs to be minimized.

6. After a tripping event, the system needs be easily reset to minimize some of the inconveniences detailed above caused by an interruption of electrical power.

3.2 Functional Decomposition

The level 0 block diagram depicted in Figure 3-1 highlights the main inputs and output of the entire system built in this thesis project.
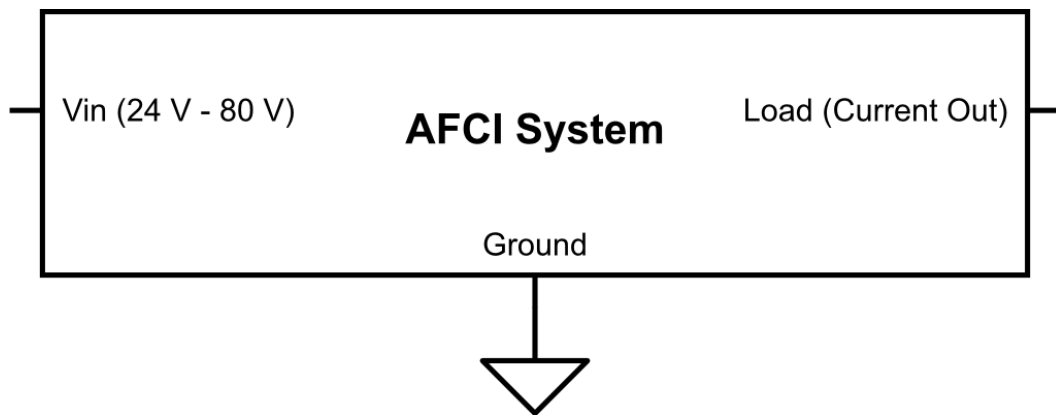
Figure 3-1: Level 0 Black Box Diagram

Table 3-2: AFCI Functionality Table with Inputs and Outputs

Module	AFCI
Inputs	Vin (24 V - 80 V) • Provides Voltage Power source for internal components of AFCI • A range from 24 V to 80 V DC is required Power Source (Current In) • Connects to the source that will be supplying the load with current • Maximum 12.5 A Ground • Provides voltage reference across circuitry
Outputs	Load (Current Out) • Connects to load • Supplies current to load • Maximum 12.5 A
Functionality	To take in current and pass current to the load while simultaneously monitoring the current for signs of electrical faults

The total AFCI system built in this thesis is composed of two main sections: The AFCI Analog Board which houses all analog filtering and the Smart DC Wall Plug which houses the MCU, output voltage control, and current control.
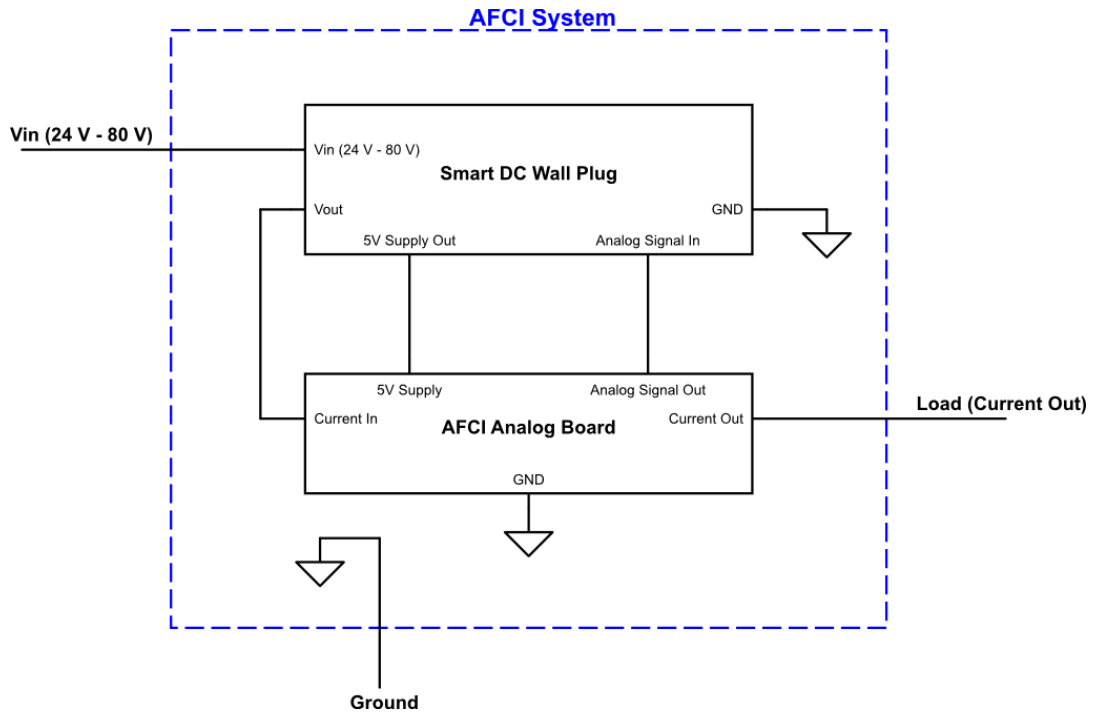
Figure 3-2: Level 1 Black Box Diagram

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The two Subsystems ("Smart DC Wall Plug" and "AFCI Analog Board") shown in Figure 3-2 will be built on two separate PCBs to enable easier troubleshooting during the final testing phase of this project. In future work, both subsystems should be on a single PCB to reduce noise.

The final configuration of the AFCI system is represented in Figure 3-3 and shows the necessary subsystems needed for each of the two PCB boards.
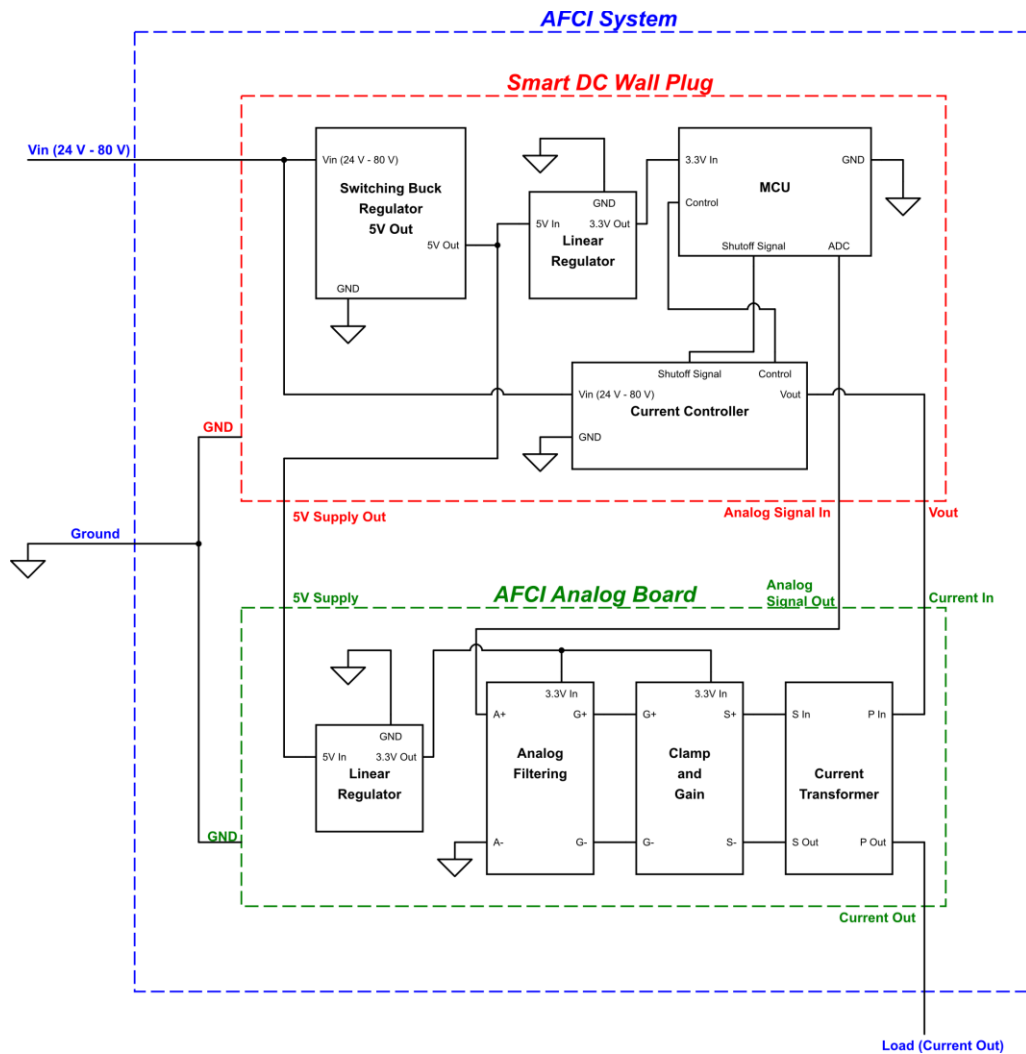
Figure 3-3: Level 2 Black Box Diagram[*]

*Not all connections and subsystems for the "Smart DC Wall Plug are shown. Only subsystems needed for AFCI are displayed.

CHAPTER 4:
Arc Generator Development

4.1 Background

From the outset, it was clear we would need a reliable and repeatable way to create an electrical arc while powering a circuit with a DC power supply. This "Arc Generator" or "Arcing Device" would need to satisfy the following requirements:

Table 4-1: Design Requirements for Arc Generator

A sustained electrical arc must be achieved at voltages of 80 volts or less
No substantial risk of electric shock to the operator should exist
The distance between electrodes needs to be adjustable between tests and possibly during a particular test
The electrode material needs to be easily replaceable
The device needs to be easy to use for the operator running each experiment

To fully achieve all of these requirements, we ended up using two different Arc Generators during our project.

4.2 Arc Generator 1: UL/EATON Design

Because the UL (Underwriter Laboratories) was one of the first organizations to focus on arcing in DC circuits, they have developed a recommended arc generator design to satisfy their UL 1699B requirements. Figure 27.1 of their 1699B document provides the following schematic:
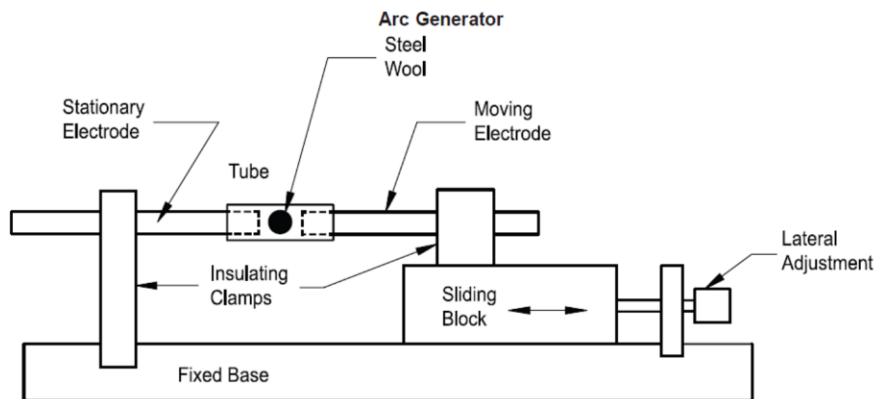
Figure 4-1: Arc Generator as Recommended by UL [9]

It appears that EATON may have assisted UL in the development of this generator, because we

were able to also obtain the following CAD file prepared by P. Rollman at EATON Corporation:
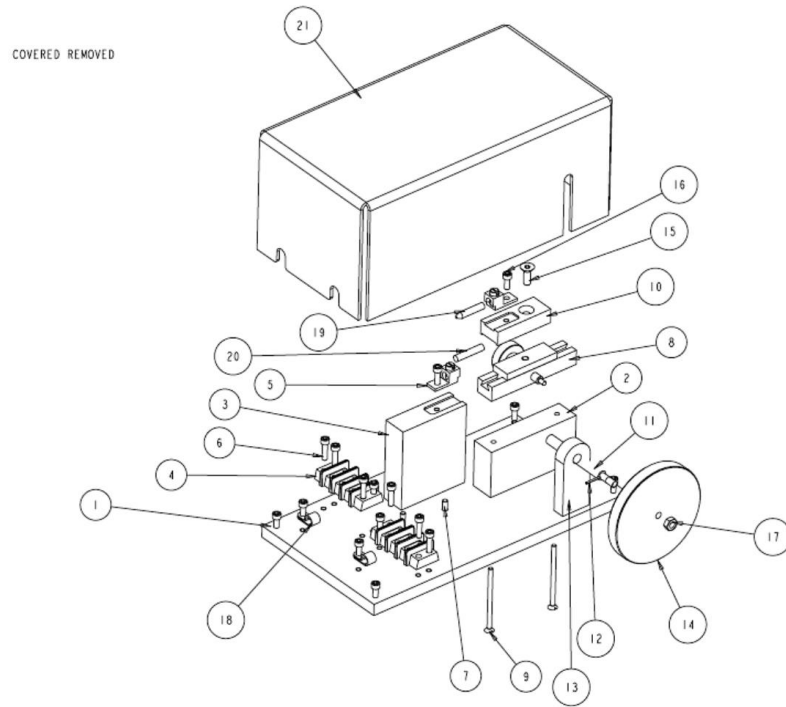
Figure 4-2: Additional Details of UL Arc Generator

Using these schematics and additional details from EATON Corporation, we built the following

Arc Generator apparatus:
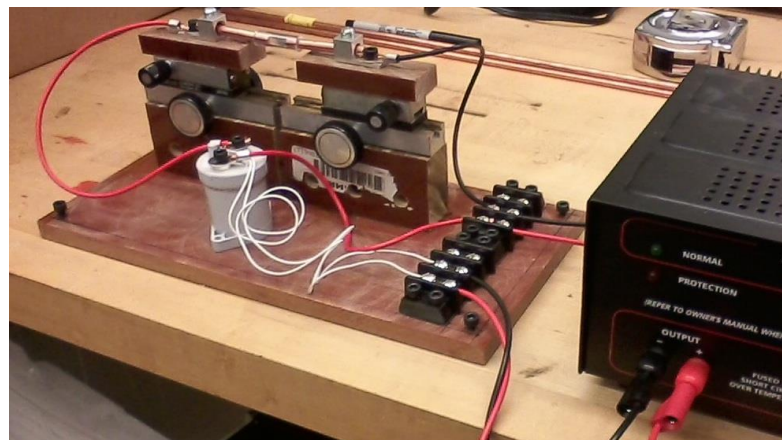
Figure 4-3: Our First Arc Generator Built to UL Specifications

Figure 4-4: UL Specifies Using Steel Wool to Help Initiate Arcing
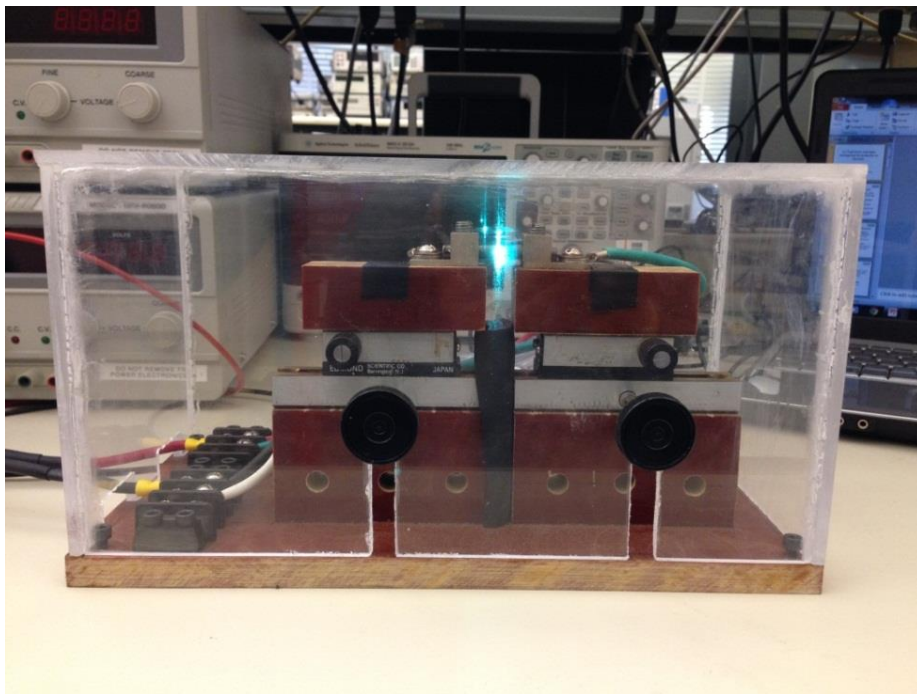
Figure 4-5: Our First Arc Generator with Sustained Arc Occurring

After using this apparatus for a while, it became clear that it primarily satisfied the first four requirements listed above, but was not as easy to use as it could be. In particular, initiating the arc with steel wool was not as repeatable as we would have liked. Nor was it very quick to re-set the experiment for another test run. So we redesigned the arc generator, putting greater emphasis on Ease of Use, and decreased the emphasis on Ease of Electrode Replacement.

4.3 Arc Generator 2: Knife Switch Design

By using a knife switch, it became much easier to initiate the arc. Essentially, the switch is closed to set up a current, and then the switch is opened slightly to cause an arc (see Figure 4-6). The pivot of the switch is kept tight enough that the gap between electrodes does not change significantly once the operator has removed their hand from the adjuster. If the gap is adjusted correctly by the operator, a sustained arc can be easily initiated and maintained with our second design.

This design is also not perfect in that we can no longer easily control the electrode shape and material, but through use of both of our Arc Generators, we have been able to perform all of the experiments that we felt were necessary.

Figure 4-6: Knife Switch Arc Generator Design

CHAPTER 5:
Arc Detection in DC Electricity

5.1 Arc Categorization

For this report, the type of electrical arc occurring falls under one of the four categories listed

below. Different strategies will be used to detect these different types of arcs. The solution to

extinguish an arc before possible damage differs depending on the type of arc detected.

5.1.1   Series Arcing

Series arcing is described as an electrical arc occurring within a closed circuit in series with

various loads and the power source. During series arcing, no current leaves the intended circuit.

All current leaving the positive terminal of the source is returned to the negative terminal. As a

result, a GFCI (ground-fault circuit interrupter) is not capable of detecting such an electrical fault.

Measuring the total amplitude of current out versus current returned is not a viable method for

detection. More complicated processing will be required to detect such an arc and is detailed in

this report. Figure 5-1 shows a basic series arc example.
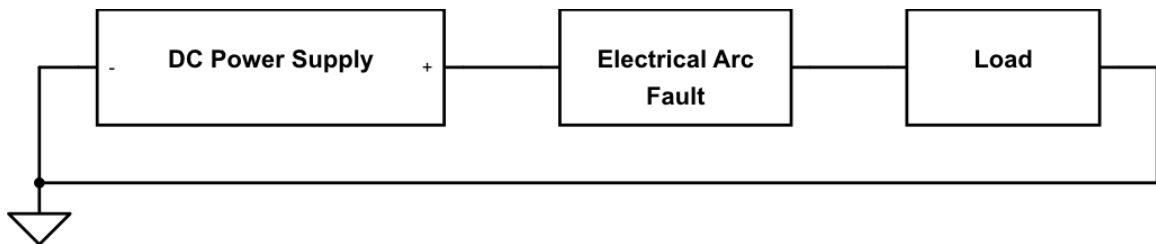
Figure 5-1: Basic Series Arc Example

5.1.2   Parallel Load Arcing (Series Arcing Variation)

Parallel load arcing is described as an electrical arc occurring across a load within a closed

circuit. This parallel combination of load and arc may or may not be in series with other loads.

During parallel load arcing, as in series arcing, no current leaves the intended circuit loop. All

current leaving the positive terminal of the source is returned to the negative terminal. The issues in detecting this type of arcing is identical to the issues presented by series arcing. Figure 5-2 shows a basic parallel load arc example.
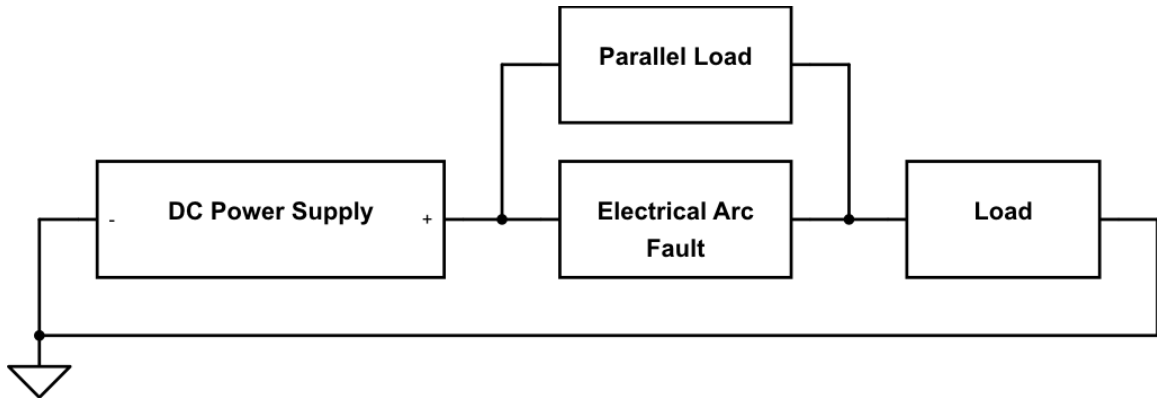
Figure 5-2: Basic Parallel Load Arcing (Contains Optional Series Load)

5.1.3 Parallel Conductor Arcing (Series Arcing Variation)

Parallel conductor arcing occurs when an additional current path outside the designed circuit loop becomes available, often because of poor electrical insulation or wire damage. In this case, the current leaving the source will not match the current returning to the source. This type of arc is easy to detect. Typical amplitude measurements of all string currents, in and out of the Smart DC Wall Plug, can be used to detect such an arc. If the current out of the plug does not match the current returning to the plug, an arc or other fault has occurred. Figure 5-3 shows a basic parallel conductor arc example.
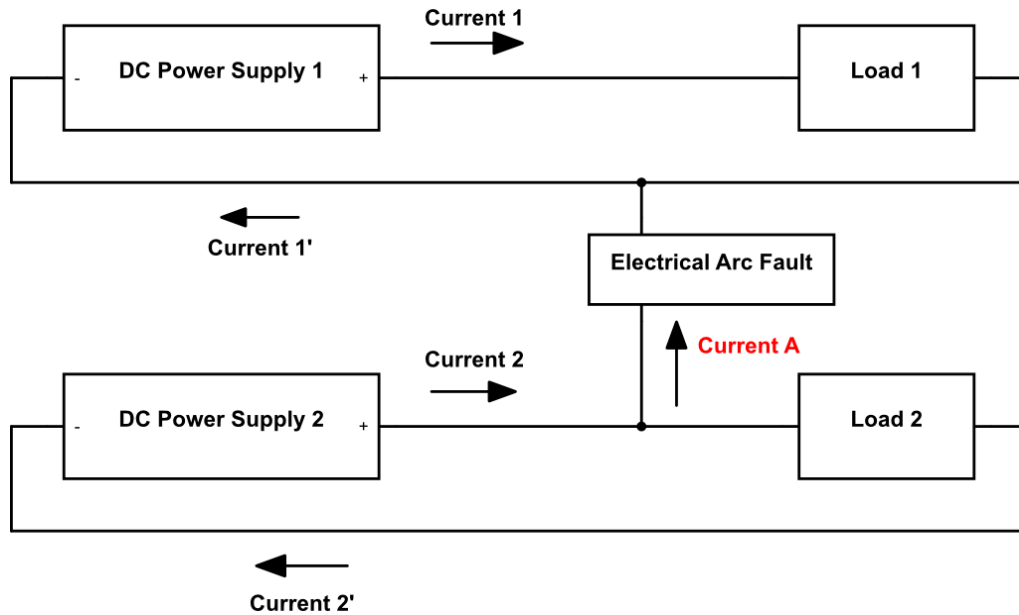
Figure 5-3: Basic Parallel Conductor Arcing Example

5.1.4   Ground Arcing

Similar to parallel conductor arcing, ground arcing occurs when an unintentional electrical path to ground outside the desired current loop becomes available. If a less resistive path to ground becomes available outside the desired loop, an arc to ground can occur. To detect this type of arcing, typical measurements monitoring the current flowing out and the current returning is used (just as in parallel conductor arcing.) A difference in the two measurements indicates a fault, which may be an arc or other ground fault.
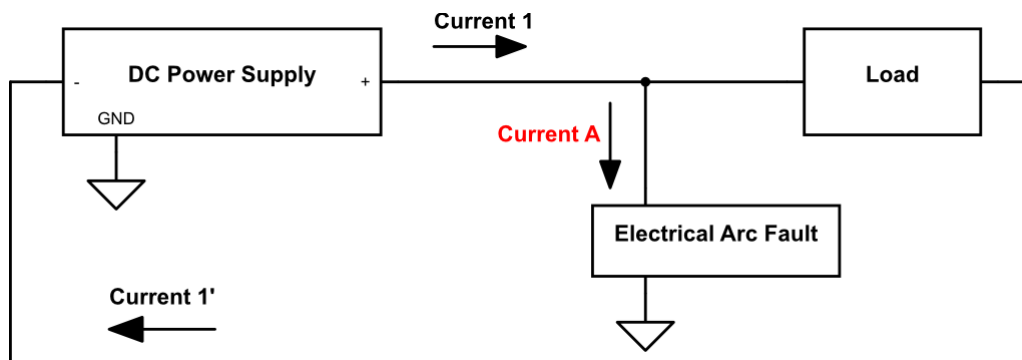
Figure 5-4: Basic Ground Arcing Example

<u>5.1.5 Summary of Categories</u>

Parallel conductor arcing and ground arcing are easy to detect with methods already available. To detect parallel conductor arcing and ground arcing, simple measurements of output current versus return current is all that is needed; a difference in the two measurements indicates a fault. Series arcing and parallel load arcing are more difficult to detect as all output current is returned to the source. Simple measurements of output and return current are not sufficient. As a result, the majority of research performed during this project was directed towards the characterization and detection of series arcing and parallel load arcing. The strategy used to detect series arcing and parallel load arcing will require monitoring the spectrum of current flowing through the affected circuit. As will be discussed later in this report, the strategy used to detect series arcing and parallel load arcing may also be used to help differentiate parallel conductor arcing and ground arcing from other non-arc related faults.

5.2 Characterization of Spectral Response

To characterize the spectral response of current from a DC power supply during series and parallel load arcing, a basic setup was used as shown in Figure 5-5. "Load 1" represents a parallel load while "Load 2" represents a series load. Each experiment varied the parameters of the components used to ensure possible variations were accounted for in the spectral response characterization. The impedance and characteristics (passive and active) of the loads were varied as well as the models and manufacturers of each component and device used (Power supply, Current Transformer, Spectrum Analyzer, cables and contacts). The DC Power Supply voltage was varied between the minimum voltage required to create an arc for that particular setup and 80 volts. The contacts used in the Arcing Device were interchanged with various materials, contact shape, and size. The specific equipment used during this research project is summarized in Table 5-1.
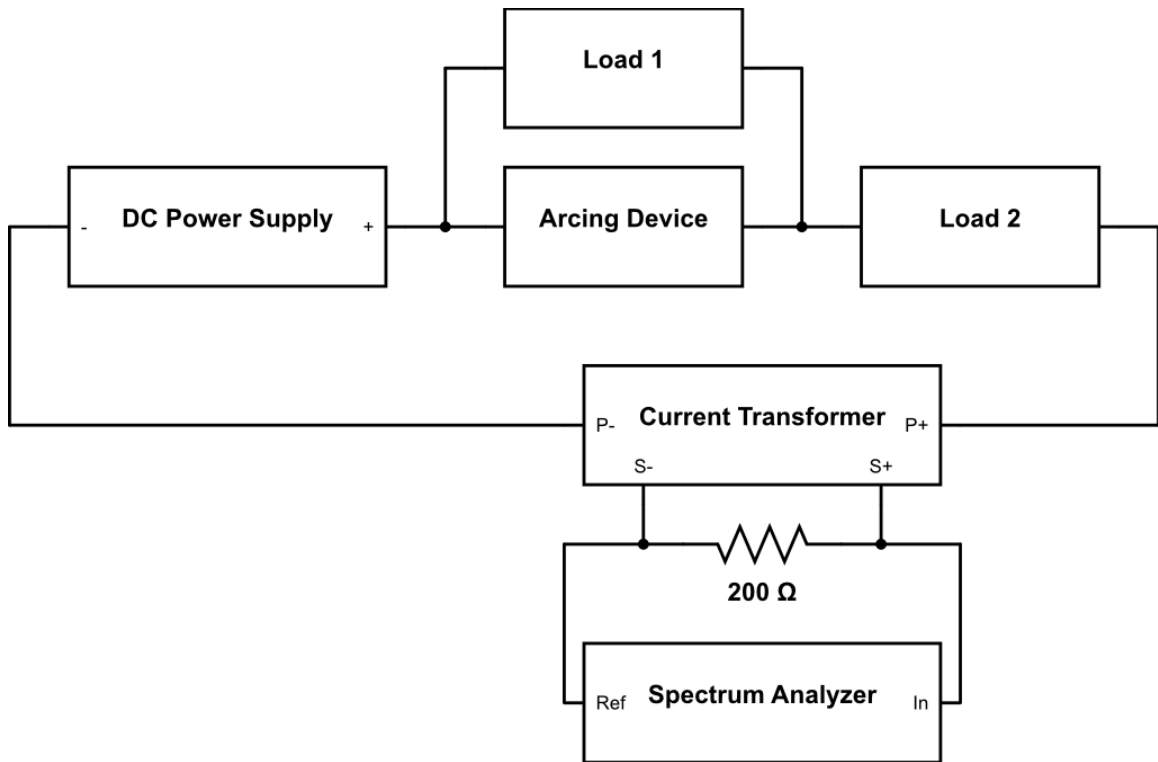
Figure 5-5: Testing Setup 1

Table 5-1: Parts List of Equipment Used During This Research Project

Clarostat MRG. Co., Inc Power Resistor Decade Box Model Number 240-C
BK Precision 8510 600 W Programmable DC Electronic Load
HP 6032A System Power Supply
Kikusui Electronic Load PLZ303W
GW Laboratory DC Power Supply GW Model: GPR-6060D
Agilent Infiniivision MSO-X-2012
Digilent Analog Discovery
Teledyne LeCroy HDO4104 High Definition Oscilloscope
Power Ten P83C-25040 Power Supply
TycoElectronics LEV100A4ANG Relay

An overlay of a few of the experiments performed is shown in Figure 5-6. A few individual experiment results, which are representative of all experiments performed, are available in APPENDIX A. Each color in Figure 5-6 represents a different experiment with different component values. The baseline provides a no arc condition to compare to. The baseline exhibits a flat response as the spectrum analyzer simply displays the noise-floor. Each experiment resulted in a different spectrum response. The spectrum of some experiments varied only slightly from the baseline, others more so. At times the response during an arc was nearly indistinguishable in shape from the baseline. Variance in the arcing frequency response poses a problem as the sources and loads used in the field are unpredictable and beyond the designer's control. A reliable and consistent spectrum is required if a microprocessor is to be programmed to recognize a "signature" arcing response.

Figure 5-6, and all further spectrum screenshots are, unless otherwise noted, observing the spectrum from 244 Hz to 100 kHz. The spectrum analyzer has available resolution settings to be adjusted when appropriate. The resolution settings used, unless otherwise noted, is set to provide the greatest resolution between 244 Hz and 100 kHz. The decision to monitor this specific range was not arbitrary. Any area of the frequency spectrum could have been monitored and analyzed for a possible pattern to develop an arcing characterization from (Ex. 1 MHz-2 MHz.) However,

the goal of this research is to develop a fully functional AFCI and keep costs of such a device to a minimum. Therefore, once data has been collected and a strategy developed, implementing a design that monitors 1 MHz-2 MHz will be significantly more expensive than one that monitors 244 Hz to 100 kHz. In addition, higher frequencies are often used for other processes such as communications, microprocessors, and DC-DC converters; keeping the AFCI design in the lower frequency range will help to avoid possible interference from such devices. Frequencies lower than 244 Hz take too long for a microprocessor to analyze and would not allow the completed design to extinguish an arc within 2 seconds.
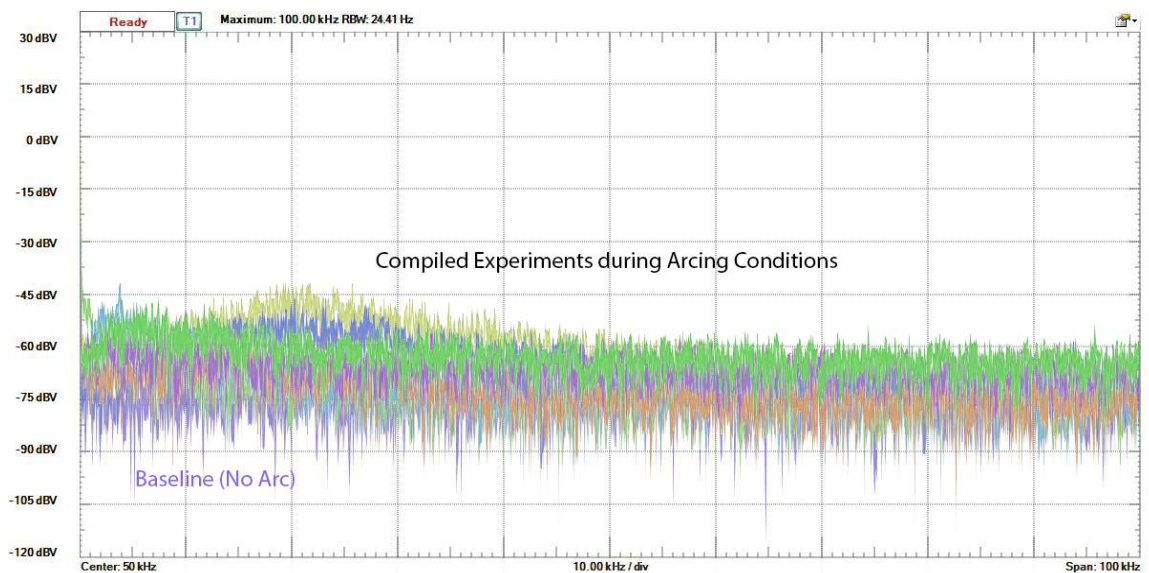
Figure 5-6: A Compilation of Spectra as Different Arcing Parameters Were Adjusted

As can be seen in Figure 5-6 and in APPENDIX A, some arcing responses appeared no different in shape or magnitude from the baseline conditions. Rather than using a current transformer, the spectrum analyzer was used to measure the voltage across an inline, purely-resistive load (As shown in Figure 5-7.) Via Ohm's law, by measuring the voltage signal across an inline resistive

load, the current through the circuit is indirectly measured. Testing Setup 5 was used to determine the possibility of information loss due to the small amplitude of current output by the current transformer. Loss of signal information was suspected to be a possible issue when stepping down the current. The primary-side of the current transformer has between 1 and 12.5 amps flowing through it. The current transformer has a 100:1 ratio resulting in the secondary-side only outputting a total 10 mA-125 mA. The total energy supplied by the secondary-side current is dispersed among every frequency produced; therefore, many individual frequencies often have too little energy to be detected by the spectrum analyzer. The signal produced from the current transformer is often too small to be detected in its raw form by the spectrum analyzer. This issue is due to the bit depth of digital spectrum analyzers. The spectrum analyzer used during this phase of the experiment has a noise floor of approximately -75 dB due to its 14 bit ADC. Any signals with amplitude too small to affect the least significant bit of the spectrum analyser's ADC will not appear in the measured spectrum. Therefore, some data may be unobtainable using the setup featured in Figure 5-5 as the signal produced by the arc and stepped down through the current transformer is on the same order of magnitude as the inherent noise of the spectrum analyzer.
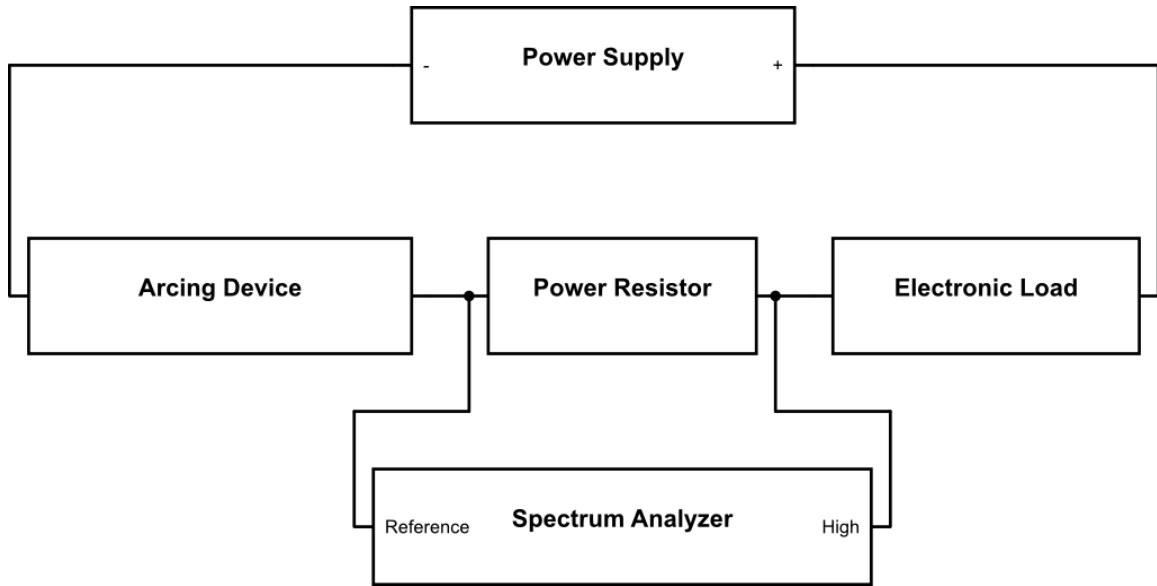
Figure 5-7: Testing Setup 5
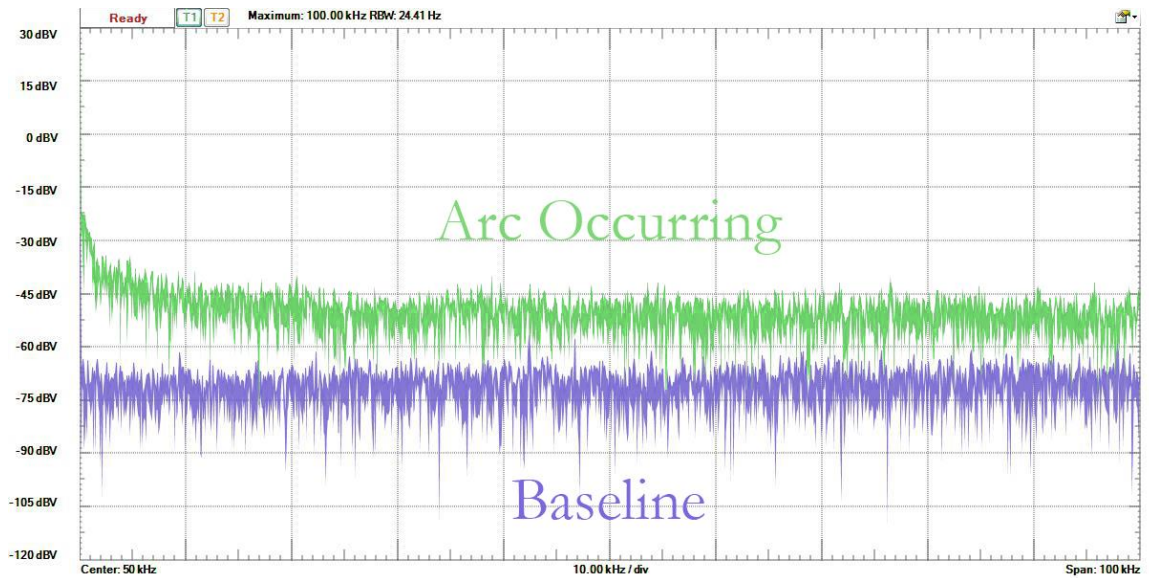
Figure 5-8: Arcing Test Using Inline Power Resistor for Spectrum Measurement

When compared to Figure 5-6, Figure 5-8 provides obvious evidence that loss of information was occurring due to limited resolution when using Testing Setup 1 shown in Figure 5-5. Figure 5-8 shows a definite difference of energy magnitude when an arc is occurring compared to the

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baseline; it is of interest to note that the overall distribution of energy across the frequency spectrum in the baseline and while an arc is occurring is very similar. More examples that utilize Testing Setup 5 are available in APPENDIX A.

During practical application, using an inline resistor to measure the spectrum causes unacceptable power waste; a current transformer is required. To solve this issue and allow the continued use of a current transformer, a low noise operational amplifier was used to gain the signal output from the current transformer before being fed into the spectrum analyzer.

Figure 5-9 shows the new testing setup using a gain stage on the signal before analysis. Figure 5-10 shows a compilation of experiments using Testing Setup 6 while varying component parameters as done for Figure 5-6. Individual examples using Testing Setup 6 are available in APPENDIX A.

Figure 5-9: Testing Setup 6 (Implements Gain)

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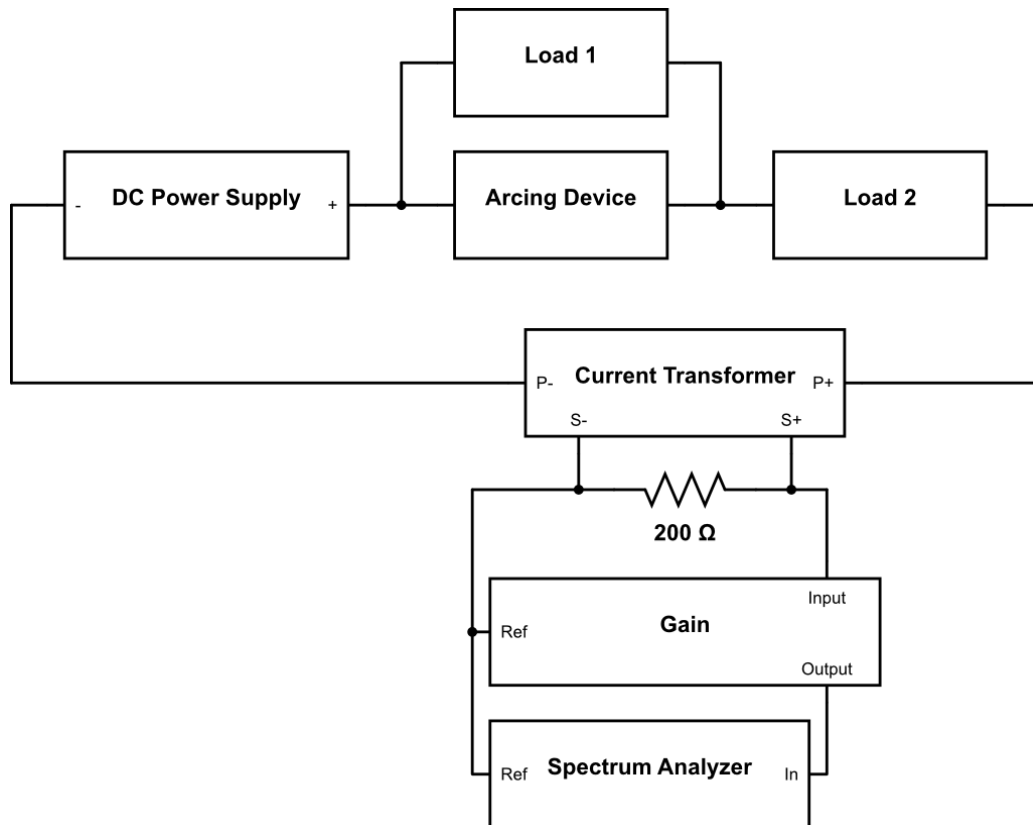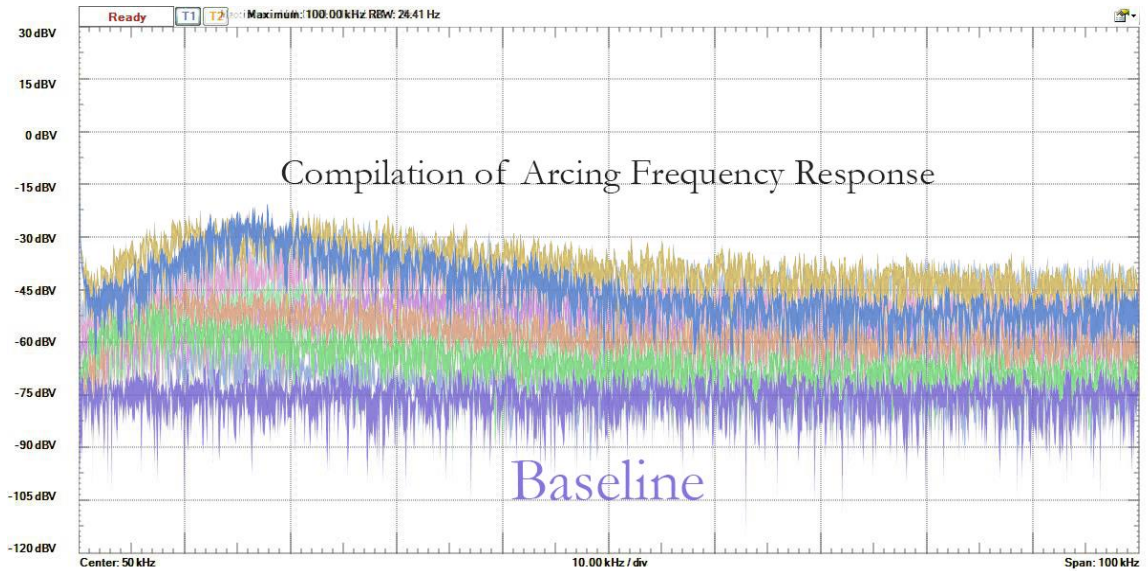
Figure 5-10: Compilation of Spectra as Different Arcing Parameters Were Adjusted

During an arcing event – as can be seen in Figure 5-10, Figure 5-6, as well as "Arc Test 1"

through "Arc Test 5" detailed in APPENDIX A – the spectrum appears to be noise distributed in

a different fashion for different component configurations. Some contain an overall shape that

differs from the flat baseline, and some that appear identical in shape to the baseline but with

greater total energy. The only consistent result from the experiments is: If an arc is occurring it

will create noise content throughout the observed frequency range (244 Hz-100 kHz), though the

amplitude distribution may vary depending on components used.

To test whether this behavior is isolated to the 244 Hz-100 kHz range, the spectrum analyzer's

range was extended to 1 MHz. Figure 5-11 shows a test (using Testing Setup 6 shown in Figure

5-9) with the spectrum analyzer set to monitor 244 Hz-100 kHz. Figure 5-12 shows the same

testing setup but with the analyzer set to monitor 2.441 kHz-1 MHz. To see the exact components

used in the arcing test to produce each plot, see APPENDIX B. It is of interest to note that the

overall shape of the spectrum during arcing in this specific test is nearly indistinguishable from

the baseline shape, though the displayed magnitudes are different.
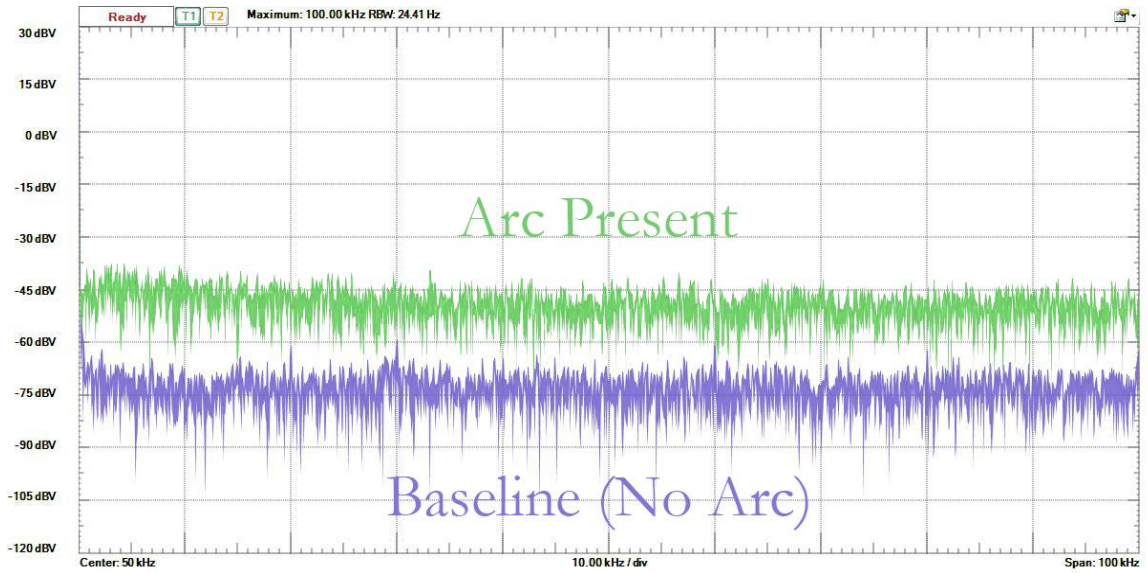
Figure 5-11: Arcing Test (244 Hz-100 kHz)
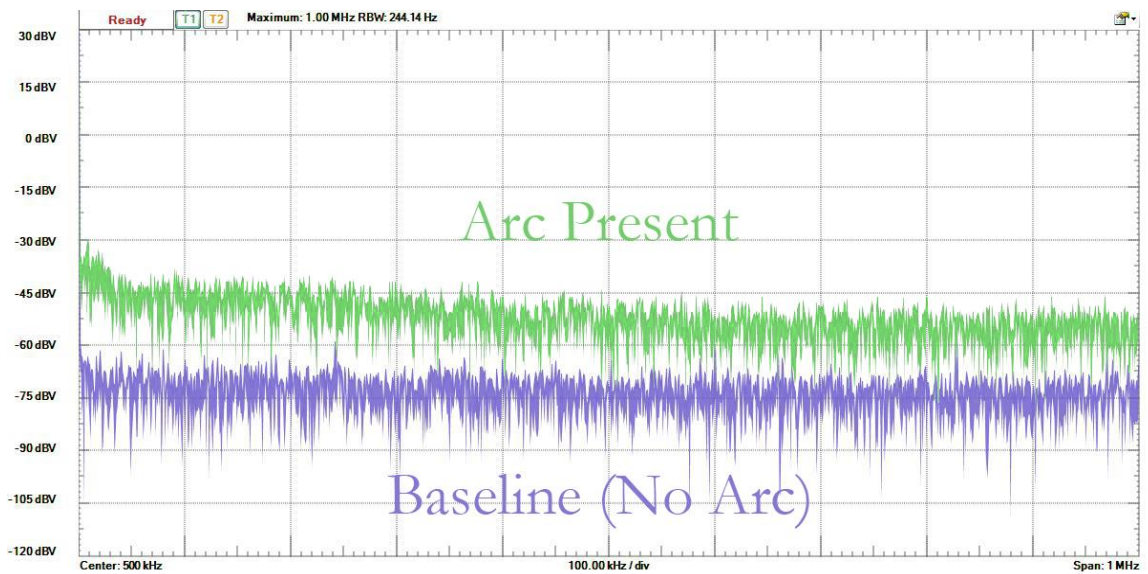
Figure 5-12: Arcing Test (2.44 kHz-1 MHz)

Figure 5-11 and Figure 5-12 show that the noise created from an arc is not just isolated to our target range, but extends well beyond 100 kHz.

5.3 Design, Simulation, and Post-Processing of Tests

As mentioned previously, the spectral response of current drawn through an electrical arc is not consistent across all component variables. Therefore, the shape of an arbitrarily chosen test case cannot be used as a model for detection as such a design would fail in nearly all other circumstances. As previously stated, some arc spectra appear identical in energy distribution to the baseline. A predictable frequency response that applies to all, or as many as possible, system configurations is needed to create a reliable AFCI.

A possible method of detection would involve measuring the magnitude of several arbitrarily chosen points on the spectral response and determining if they are higher in magnitude than a predefined baseline. This method is flawed as the noise floor (baseline) of each individual board may be different due to internal noise variations in the microprocessor and associated components. Therefore, defining a baseline value to be used for all manufactured AFCIs may cause faulty products if the noise floor of some boards happens to be higher than the predefined baseline. In the interest of future improvements that may utilize a different ADC than the one currently used, having a predefined baseline may require more work to edit the code used to analyze and detect an arc. In addition, if loads that use some form of periodic electrical switching (such as DC-DC converters) happens to have its switching frequency at one of the arbitrarily chosen points used for detection, a false positive detection will result. While efforts can be made to avoid most commonly used frequencies, proper operation can't be guaranteed under this design. Defining the baseline by analyzing the entire spectrum during startup is a possible workaround to the above-mentioned issues. However, if an electrical arc was occurring during startup the AFCI would fail to recognize its presence.

To provide a robust system, a predictable shape in the frequency response unique to an electrical arc is needed; having a predictable shape will allow a microprocessor to compare and map several sample points to an arcing "signature" spectrum and, upon a successful match, send a shutoff

signal to a current controller. The baseline must also be allowed to vary from board to board, with different loads and sources, and be universal with a variety of ADCs, without affecting the functionality of the AFCI.

To accomplish a reliable and repeatable response despite differing system parameters and components, an analog gain and filter system was used to achieve a specific response by forcing the arcing noise to a predefined shape.

As can be seen in Figure 5-6 and Figure 5-10, as well as APPENDIX A, most variation occurred in the frequency region below 30 kHz while the response above 30kHz was more consistent. Additionally, low frequency noise and harmonics may arise if a DC system is within an AC system. As a result, the decision was made to filter out frequency content below 30 kHz, thus avoiding potential noise issues from other causes, as well as providing a baseline that can be referenced regardless of whether an arc occurs at startup or not. In other words, the frequency range from 0 Hz to approximately 30 kHz is always forced to baseline via analog filtering, regardless of the presence of an arc or varying components. Frequencies between 30 kHz and 80 kHz are amplified, and frequencies greater than 80 kHz are progressively reduced in gain as the frequency increases until baseline is eventually reached at approximately 170 kHz. The frequency range between 30 kHz and 80 kHz provides enough bandwidth to analyze so that the AFCI, with proper coding and logic implementation, will not be deceived by electronic switching loads or sources.

Figure 5-13 shows the entire analog gain and filtering circuitry from the output of the current transformer to the output voltage signal fed directly into the ADC of the microprocessor. A clamping stage is implemented at the front of the chain to protect the initial OpAmp (Named STG1 in Figure 5-13) from potential voltage spikes at its non-inverting input. The Gain stage (as

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introduced in Figure 5-9) is made up of OpAmps STG1 and STG2. OpAmps STG3 through STG8 make up the filtering stage. OpAmp STG9 acts as a unity-gain buffer.

The filtering stage of the analog circuitry shown in Figure 5-13 is made up of five high-pass Sallen-Key topology active filters and one low-pass Sallen-Key active filter. Each filter's specific design configurations and response are shown in APPENDIX C. More complex filter topologies were an option and would allow gain and filtering to be implemented on the same OpAmp, thus reducing the amount of OpAmps used. However, using separate gain stages and 2nd order Sallen-Key filters create a system that is not highly sensitive to poor component tolerances. Typical consumer resistor tolerances are 5% and capacitor tolerances range from 10% to 15%. Better resistor and capacitor tolerances are available but the increase in costs would be prohibitive. The topologies used in this design prevent the possibility of significant tolerance stack-up. As a result, this design allows the use of cheaper, consumer grade resistors and capacitors without significant effect on the resulting signal. The additional costs associated with additional OpAmps are easily compensated by the reduction in price for resistors and capacitors.

Figure 5-14 shows a simulation of the frequency response of the entire circuit chain displayed in Figure 5-13. The simulation was performed in LTSpice. The schematic used in LTSpice as well as the Spice Netlist is available in APPENDIX D.
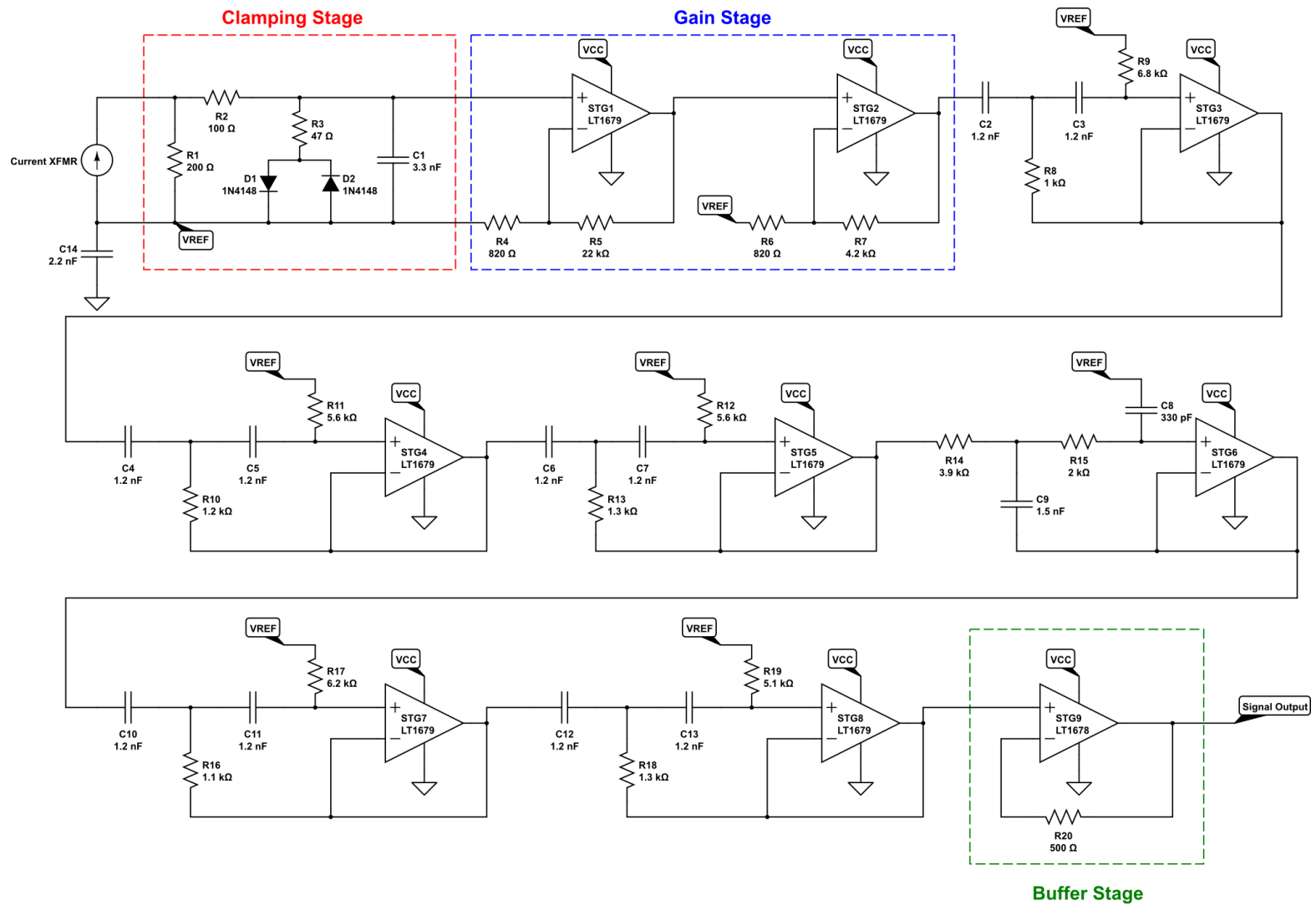
Figure 5-13: Analog Circuitry Schematic (Clamping Stage, Gain Stage, Filter Stage, Buffer Stage)

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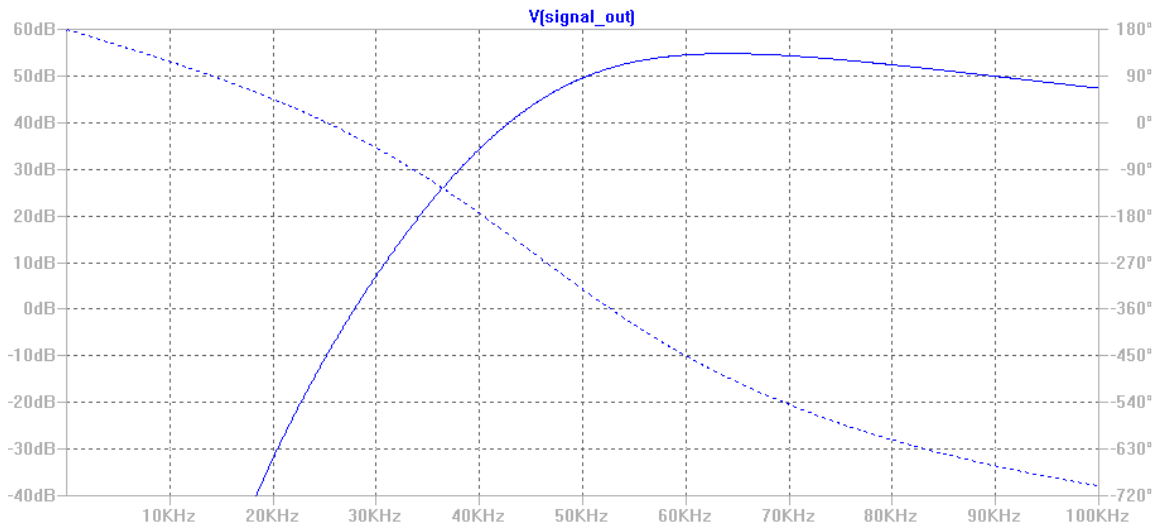
Figure 5-14: Frequency Response Simulation of Complete Analog Circuitry Shown in Figure 20

The simulation in Figure 5-14 shows the predicted response crossing 0 dB gain at slightly less than 30 kHz (approximately 27 kHz.) Any frequency content below 27 kHz is highly attenuated, easily driving 0 Hz-27 kHz down to the baseline of the spectrum analyzer. Frequencies above 27 kHz are gained, with a peak gain of approximately 55 dB (~562 volts/volt) at ~64 kHz. During arcing, the measured spectrum should fit the distribution shape shown in Figure 5-14 with the spectrum matching the baseline from 0 Hz-27 kHz.

Figure 5-15 provides a testing setup that utilizes the gain and filtering circuitry shown in Figure 5-13 to measure the frequency spectrum of current passing through a circuit affected by an electrical arc. Figure 5-16 shows a compilation of several arcing tests and iterations using the setup shown in Figure 5-15. Individual results are available in APPENDIX A. All tests using the complete processing circuit and Testing Setup 7 show very consistent spectrums during an arc regardless of components or parameters. Such consistency provides a predictable spectrum that can be used to detect an arc reliably while avoiding false positive detections.
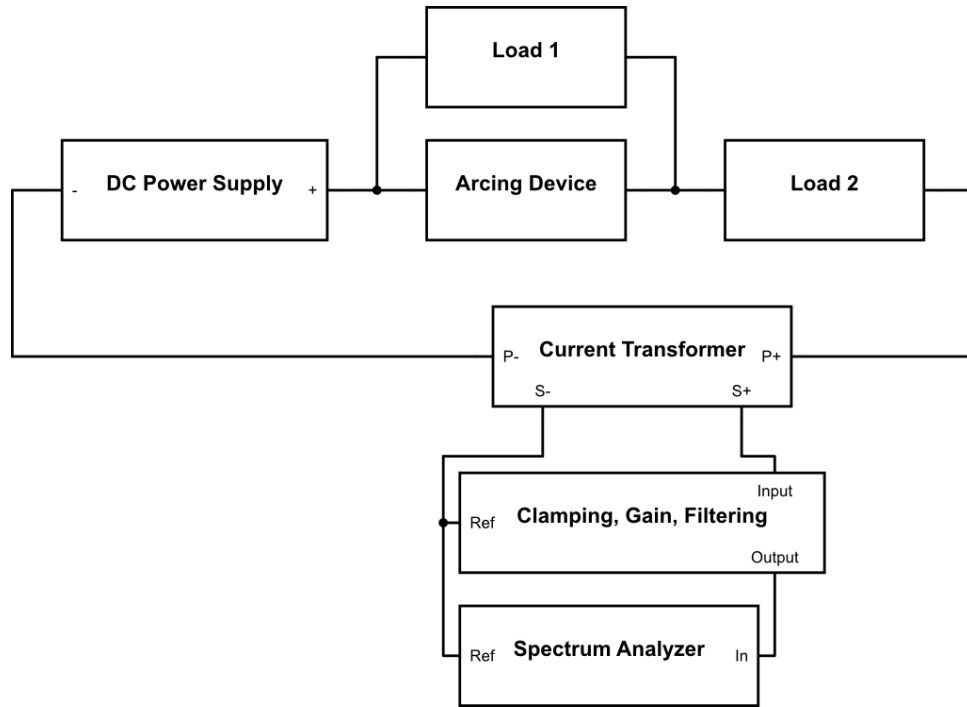
Figure 5-15: Testing Setup 7 (Utilizing Complete Clamping, Gain, and Filtering Circuit)
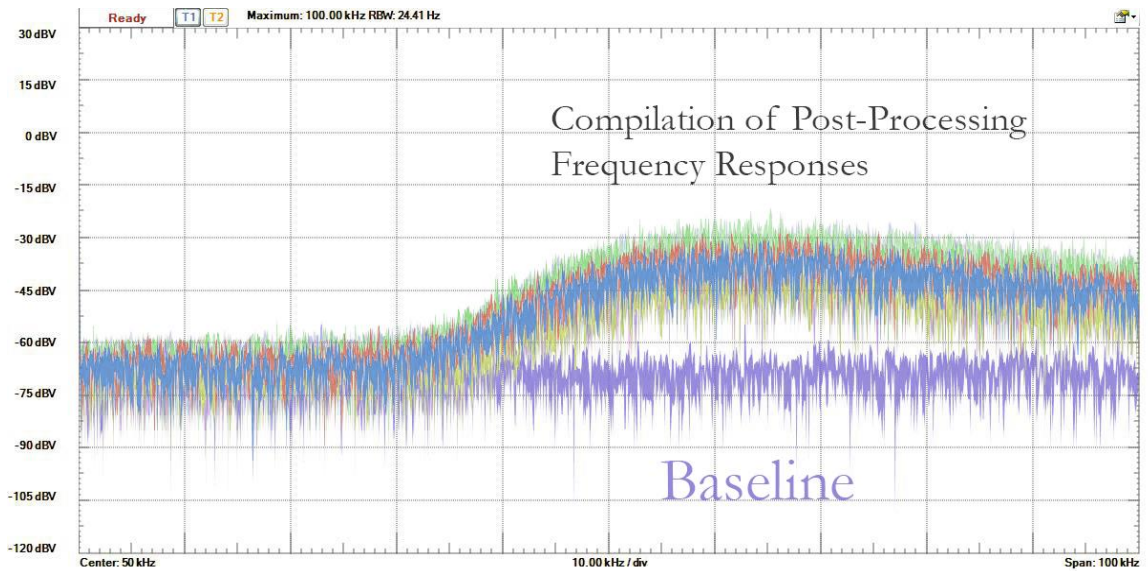
Figure 5-16: Compilation of Post-Processing Frequency Responses During Electrical Arc

The AFCI design was implemented on a printed circuit board (PCB). The populated AFCI PCB is shown in Figure 5-17. Figure 5-18 shows a completed schematic of the analog circuitry used for the AFCI as well as its pin-outs used to connect with the Smart DC Wall Plug. A switching regulator is used to step the power source (typically 48 V) to 5 V. Linear regulators are then used to step 5 V to 1.5 V and 3 V rails. Figure 5-19 shows the DipTrace schematic used to design and manufacture the PCB (same design as in Figure 5-18). During our tests, the AFCI board consumed between 10 mA-25 mA depending on whether an arc was occurring or not.
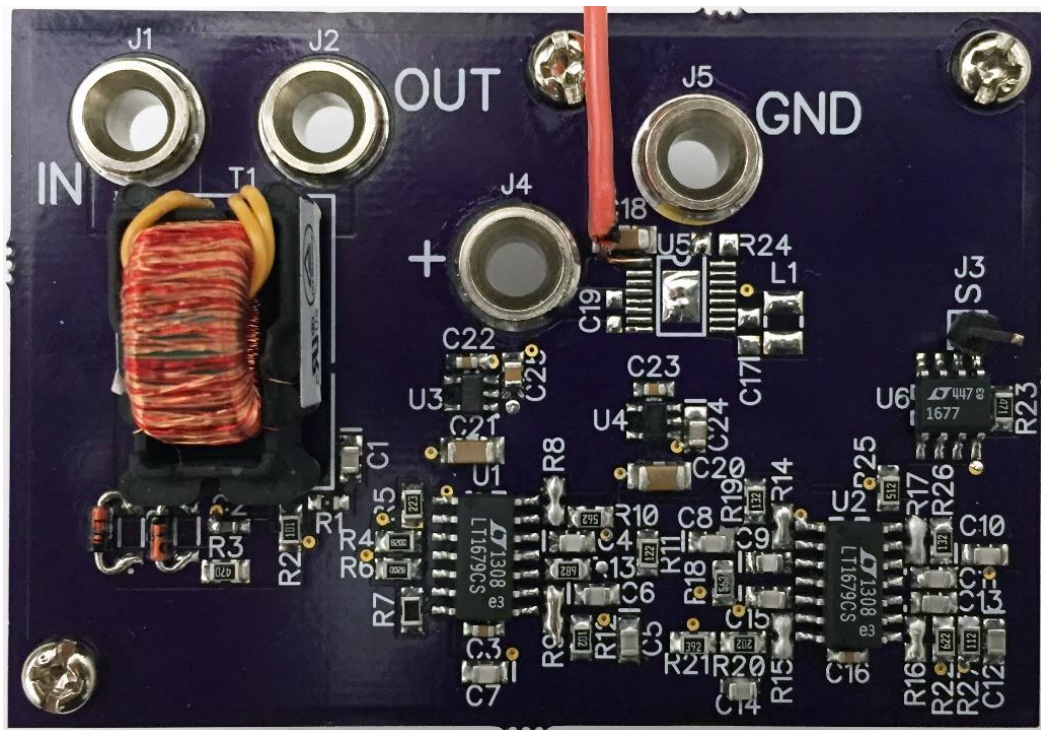
Figure 5-17: Populated AFCI Board
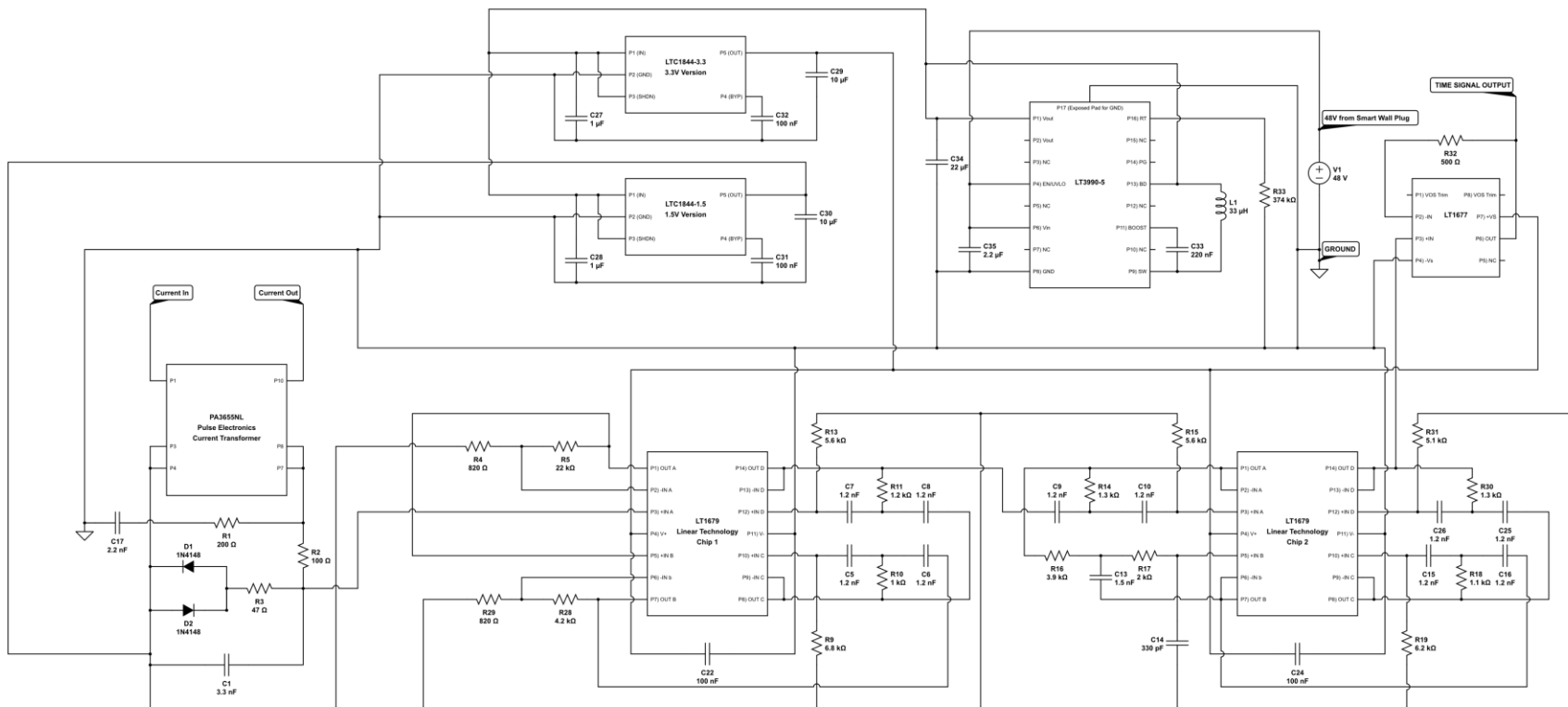
Figure 5-18: Full Schematic of AFCI Board Circuitry

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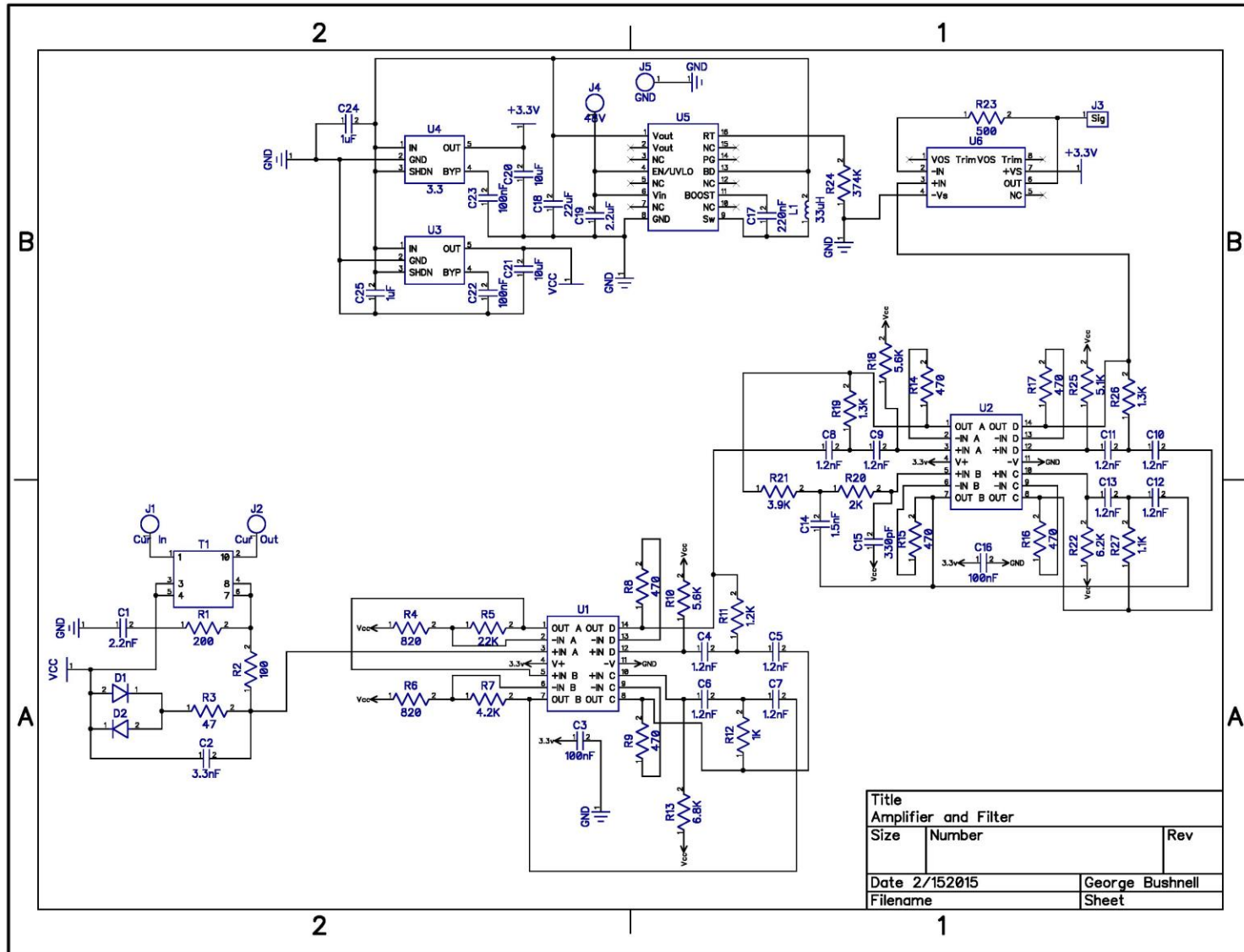
Figure 5-19: DipTrace Schematic of AFCI Analog Circuitry

CHAPTER 6:
AFCI Integration with the Smart Wall Plug

6.1 Current Status

A full-featured spectrum analyzer will not be available in the field. Instead, the microprocessor

available on the Smart Wall Plug is used for analysis and logic. The Smart Wall Plug was

upgraded (microprocessor and associated components) to support the integration of the AFCI.

This project utilized the dsPIC33EP512GM710 microprocessor from Microchip. The on-chip

ADC was used with a sampling rate of 250 kHz, satisfying Nyquist criterion up to 125 kHz. An

FFT function was performed on the incoming signal with an FFT block length of 256, providing

128 functional bins. The resulting resolution is 976.56 Hz/bin. Table 6-1 summarizes the

microprocessor's FFT setup.

$$FFT\ Resolution = \frac{Sampling\ Frequency}{FFT\ Block\ Length} = \frac{250000}{256} = 976.56\frac{Hz}{bin}$$

Table 6-1: Summarization of Microprocessor Setup Used

Microprocessor Model	Microchip dsPIC33EP512GM710
Microprocessor Clock	8 MHz
Sampling Frequency (F_S)	250 kHz
ADC	10 bit
ADC Resolution	1024
FFT Block Length	256
Functional Bins (Satisfy Nyquist Criterion)	128
Functional Range (Satisfy Nyquist Criterion)	976.56 Hz-125 kHz
FFT Resolution	976.56 Hz/bin

The FFT resolution of 976.6 Hz/bin is a fairly low resolution; however, in this case it works to

benefit the project's design. The low resolution allows for faster response times from the

microprocessor as less time is needed for calculations. In addition, as can be seen in Figure 5-16,

the frequency spectrum during an arc does not exhibit strong peaks, but rather a smoother curve.

The smooth curvature was inherent in the design. Analyzing fine peaks in this project is not required to detect the occurrence of an electrical arc.

The logic was coded and compiled using Microchip's MPLAB X IDE v2.30. The code calculates the Fourier transform of the time signal via an FFT function. The code takes the Fourier transform and compares it to a set of rules that, if all are satisfied, will indicate the presence of an arc. The rules are based on the theoretical and tested frequency responses during an arc (shown in Figure 5-14 and Figure 5-16) to create a list of conditions that will be true only when an arc is occurring. During an arc, certain frequency locations, which are stored in their respective "bins," will have more or less energy than others; which bins have a greater energy magnitude is predictable as such behavior was inherent in the filter design.

Creating more conditions that must be satisfied for arc detection help minimize false detections caused by interference from loads or sources with switching frequencies and other possible components. However, doing so will increase the response time when an actual arc is occurring as more sample sets will likely be needed before a set matching all conditions is obtained. The code also utilizes counters and delays to avoid tripping when a typical switch – such as a light switch, which may cause an electrical arc very briefly but still detected by the design detailed in this report – is used. Efforts were taken to optimize the rules and conditions to avoid false detections while ensuring the system is sensitive enough to recognize an arc quickly. This is an area that can be continuously improved with more testing to further balance response time with sensitivity. The entire FFT code used, along with inline code comments is available in APPENDIX E.

Figure 6-1 is the final testing setup that utilizes the complete clamping, gain, and filtering circuit for processing, and uses the microprocessor described in Table 6-1 for analysis.
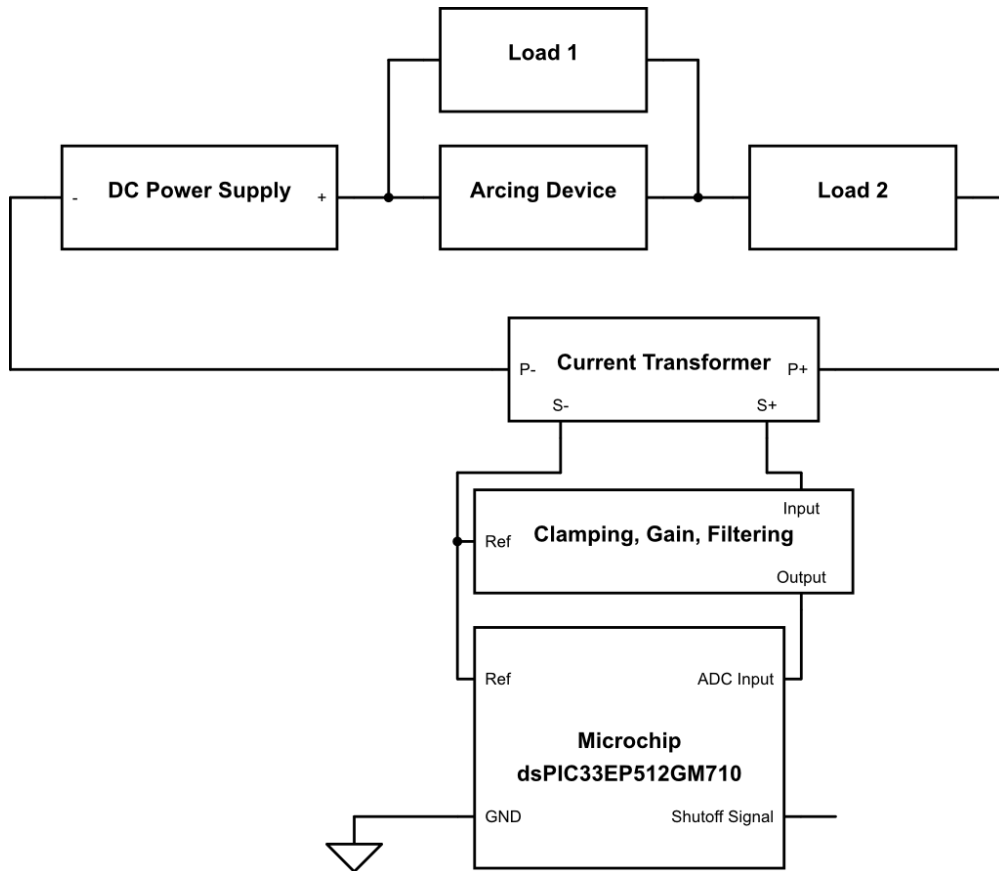
Figure 6-1: Testing Setup 8

Figure 6-2 shows an average of several (approximately 25) arc response tests performed for series

and parallel load arcs. Figure 6-2 displays the energy magnitude of bin 0 through bin 128,

providing a usable frequency range of 976.56 Hz-125 kHz. The highest average peak occurs at

FFT Bin 62, which corresponds to frequencies 59.57 kHz-60.55 kHz. FFT Bins 0-30 corresponds

to frequencies 0 Hz-29.3 kHz and has an average magnitude of approximately 0, as shown in

Figure 6-2. The data presented in Figure 6-2 closely matches the simulated response (Figure

5-14) and experimental data from a full featured spectrum analyzer (Figure 5-16.) A forced

baseline exists from 0 Hz-29.3 kHz and bins 31-100 provide enough bandwidth to perform

adequate analysis.

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The microprocessor correctly determined the presence, or absence, of an arc in every test case performed.
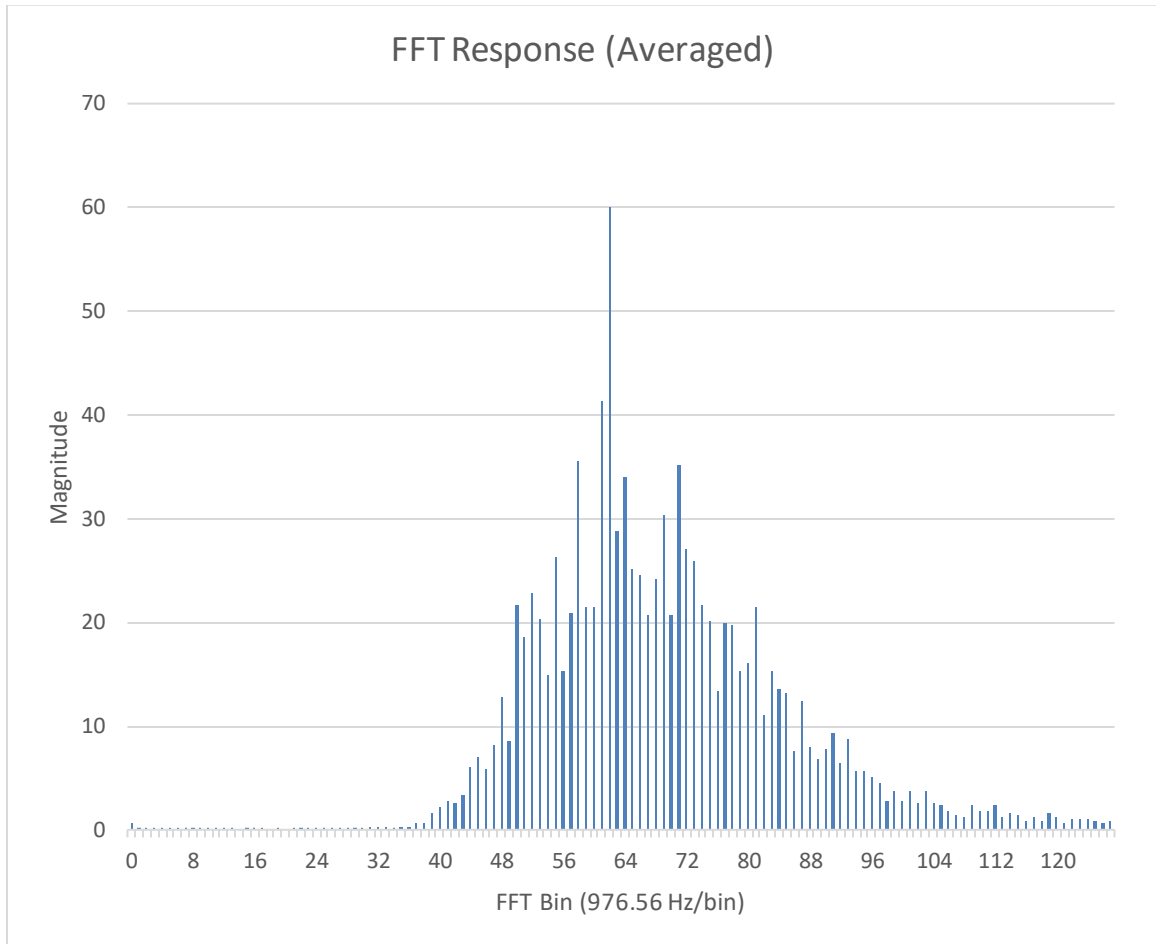
Figure 6-2: Averaged FFT Responses During Arc
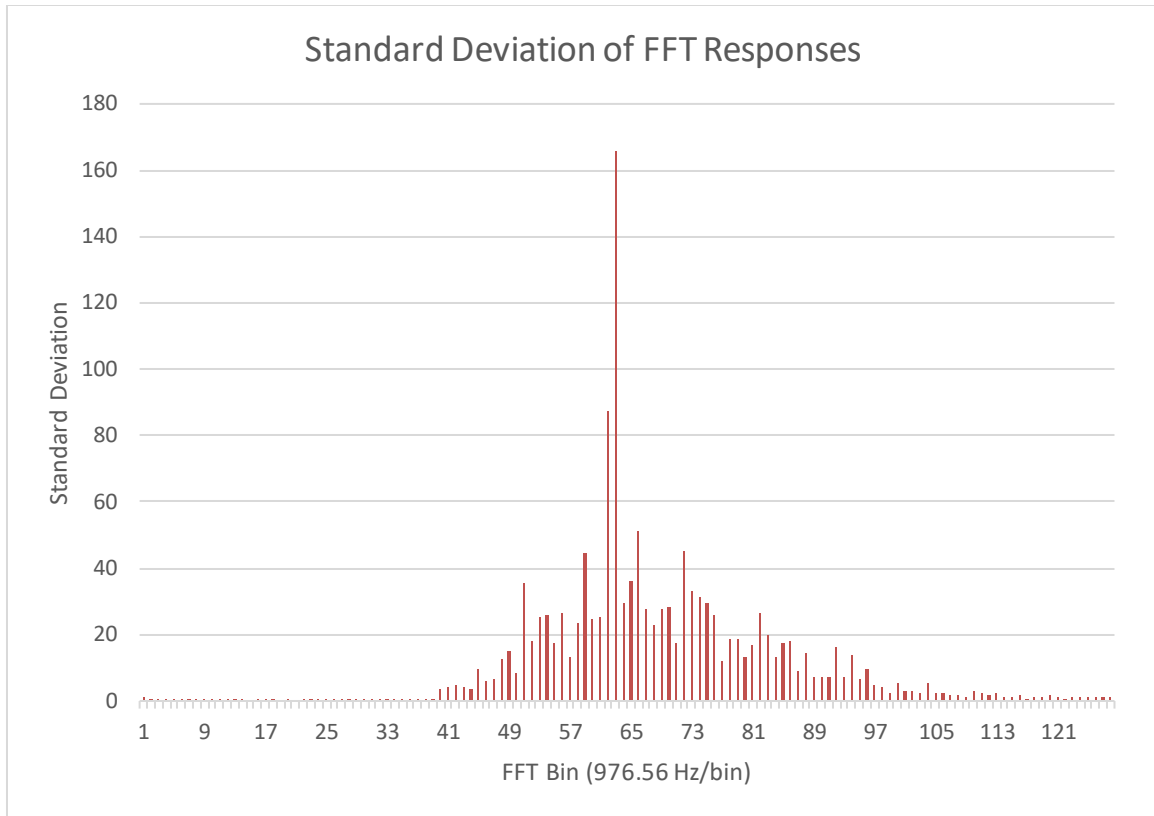
Figure 6-3: Standard Deviation of FFT Responses During Arc

Figure 6-3 shows the standard deviation of several (approximately 25) arcing tests performed for series and parallel load arcs. The standard deviation is considerably high. Outliers did occasionally appear in the tests that significantly increased the standard deviation of bin 62 and 63. It is important to note that the magnitude of energy in each bin is recorded for each test performed at a random moment during arcing. When arcing, the distribution of energy across the frequency spectrum varies randomly from sample set to sample set, even for the same testing setup. For example, the FFT Spectra shown in Figure 6-4 and Figure 6-5 were taken during the same arc occurrence, but at very slightly different moments in time (less than 1 second apart.)

Figure 6-4 and Figure 6-5 show how much the spectrum varies from sample set to sample set. Depending on the microprocessor used, and the clock speed the processor runs at, sample sets are generated anywhere from every 20 ms to every 1 ms. Due to the high rate at which sample sets are recorded, a high variance and high standard deviation is not cause for concern.
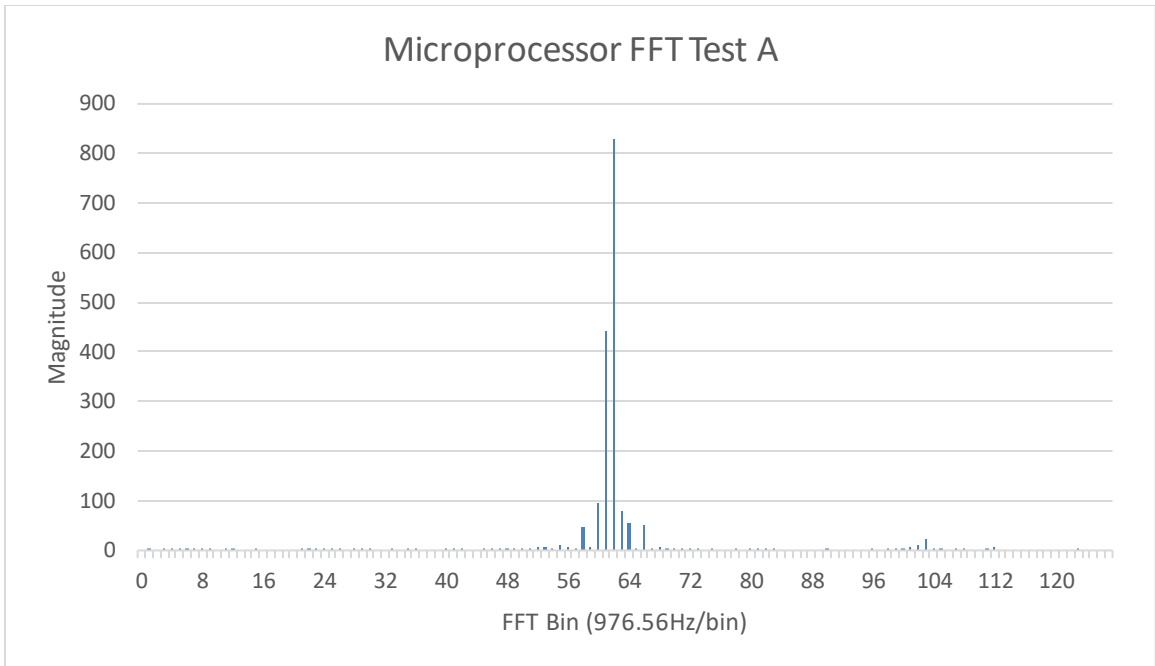
Figure 6-4: Microprocessor FFT Test A
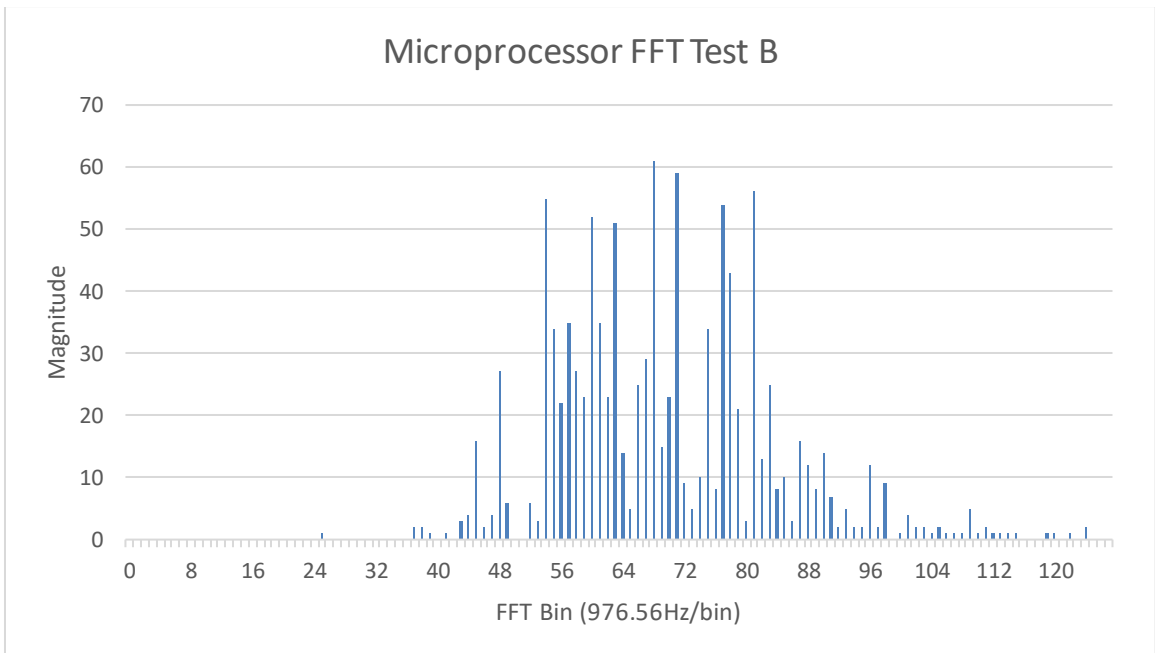
Figure 6-5: Microprocessor FFT Test B

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Design specifications required the response time of the AFCI to be under 2 seconds as recommended by UL 1699B [9]. During testing, the design detailed in this report had a response time between 8 ms and 54 ms, which is well within the UL 1699B standard. With that significant of a margin, several improvements can be made in the software coding to prevent false positives by utilizing averages across more sample sets, and performing more complex processing.

Figure 6-6 shows a test of the AFCI's response time. Channel 1 (yellow) is the time signal produced by the gain and filtering system. Channel 1 is the signal fed into the ADC of the microprocessor. Channel 2 (Pink) is the shutoff signal. A shutoff is triggered when the shutoff signal is high. Figure 6-6 shows a time delay of 18.302 ms. Figure 6-6, however, doesn't account for the propagation delay caused by the OpAmps used in the gain and filtering process.

Figure 6-7 shows the measurement (with Channel 1 (yellow)) of the voltage across an inline resistive load. During normal operation, the voltage across the resistor is constant and stable. The moment an arc occurs, the voltage will vary and exhibit noise. This test allows the OpAmps' propagation delays to be accounted for. The delay shown in Figure 6-7 is 19.82 ms which is nearly identical to Figure 6-6. The OpAmp's propagation delay does not contribute significantly to the overall delay time. Table 6-2 provides several tests showing the microprocessor's response time to the occurrence of a series or parallel load arc. The microprocessor correctly detected the presence, or absence, of an electrical arc in every test case performed.

The test results shown in Figure 6-6, Figure 6-7, and Table 6-2 were performed while using the code specified in APPENDIX E.
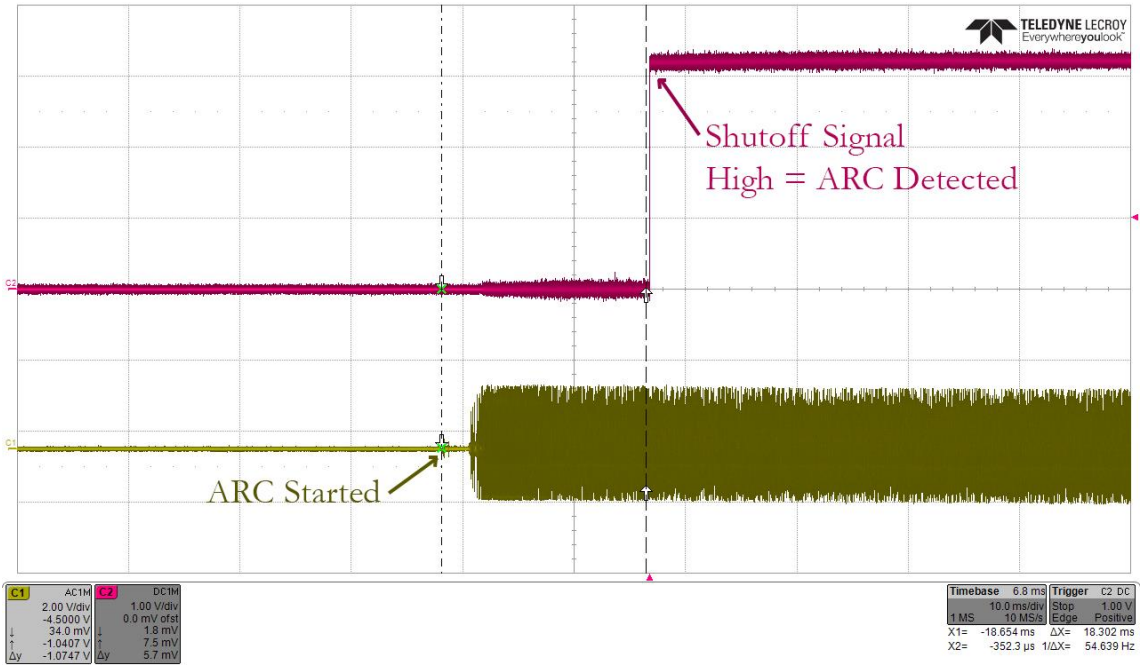
Figure 6-6: AFCI Response Time (Test 1)
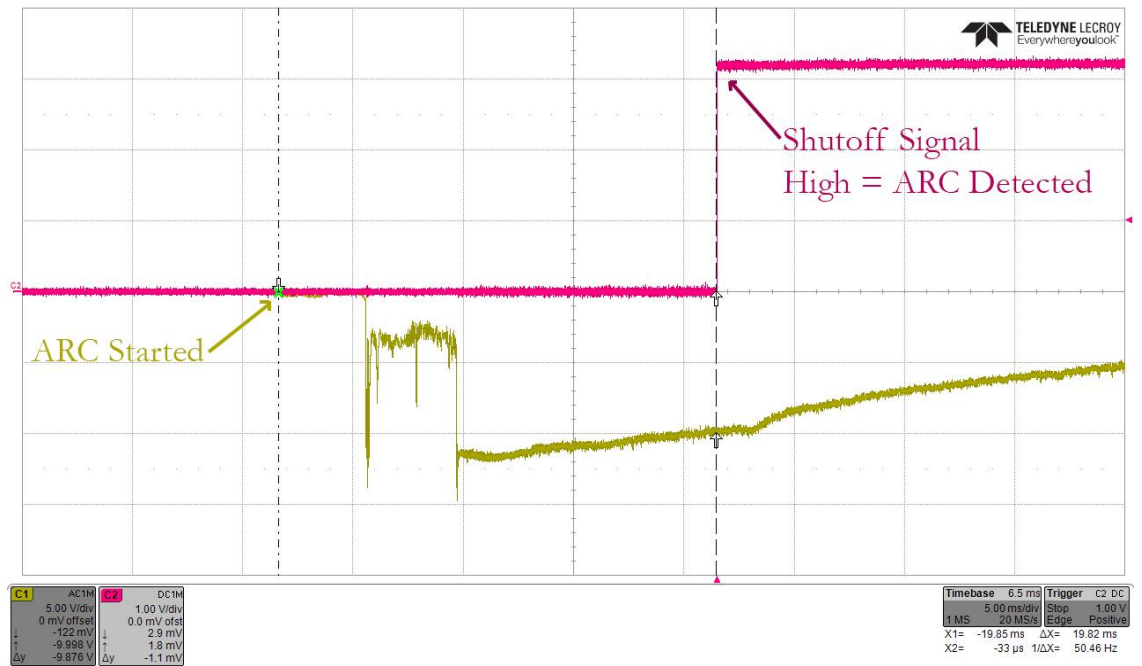
Figure 6-7: AFCI Response Time (Test 2)

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Table 6-2: Response Time Tests

		Setup			Response
Test #	Power Supply (Volts)	Channel 1 Measurement Method	Arcing Device	Load*	Delay in Detection (ms)
1	48	inline resistive load	Copper Contacts	PR = 9 Ω	**8.5**
2	48	inline resistive load	Copper Contacts	PR = 6 Ω	**8.0**
3	48	inline resistive load	Copper Contacts	PR = 18 Ω	**8.0**
4	48	inline resistive load	Aluminum Knife	PR = 9 Ω	**15.5**
5	36	inline resistive load	Aluminum Knife	PR = 9 Ω	**19.8**
6	48	Time signal Output of Buffer OpAmp	Aluminum Knife	PR = 9 Ω	**22.6**
7	48	Time signal Output of Buffer OpAmp	Aluminum Knife	PR = 9 Ω	**9.8**
8	60	Time signal Output of Buffer OpAmp	Aluminum Knife	EL = 9 Ω	**12.8**
9	80	Time signal Output of Buffer OpAmp	Aluminum Knife	PR = 9 Ω	**10.2**
10	36	Time signal Output of Buffer OpAmp	Aluminum Knife	PR = 9 Ω	**42.1**
11	36	Time signal Output of Buffer OpAmp	Copper Contacts	PR= 9 Ω	**54.2**
12	48	Time signal Output of Buffer OpAmp	Copper Contacts	PR = 9 Ω	**15.3**
13	48	Time signal Output of Buffer OpAmp	Copper Contacts	EL = 9 Ω	**13.5**
14	80	Time signal Output of Buffer OpAmp	Copper Contacts	PR = 9 Ω	**9.6**

*PR = Power Resistor; EL = Electronic Load

The upgraded Smart DC Wall Plug used for integration with the AFCI board is shown in Figure 6-8. The Smart DC Wall Plug houses the microprocessor as well as the current controller. The current controller, upon receipt of a high shutoff signal from the microprocessor, will shut down and prevent any current from flowing, and consequently extinguish a series or parallel load electrical arc.
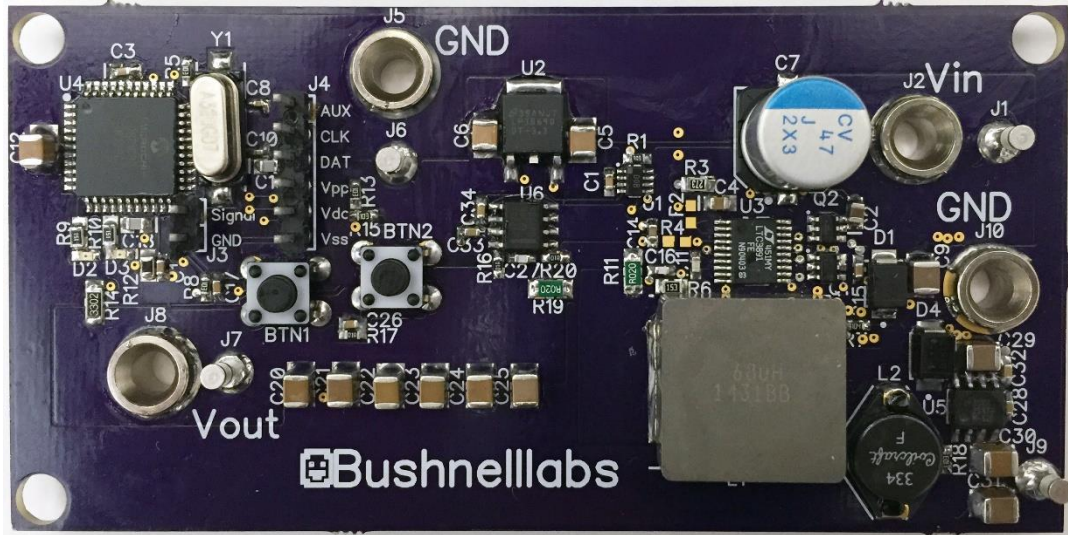
Figure 6-8: Populated Smart DC Wall Plug

If a series or parallel load arc occurs between the Smart DC Wall Plug and the load, the current controller will shut off and no current will be supplied, thereby extinguishing the arc.

A series or parallel load arc occurring between the Smart DC Wall Plug and the Power Supply works in the same manner. An arc, even upstream from the Smart DC Wall Plug, requires sufficient initial current to begin arcing. This can only happen if a load was initially drawing current. If an arc occurs in these circumstances, the current controller will still open the circuit, preventing any further current from being delivered to a load. The Smart DC Wall Plug, however, will still attempt to draw current to power itself. The current drawn by the Smart DC Wall Plug is in the low hundreds of milliamps max. A few hundred milliamp current is not sufficient enough to sustain an arc in these circumstances with the voltage levels used. Therefore, a series arc or parallel load arc occurring between the Smart DC Wall Plug and the power supply will be extinguished by the current controller opening the circuit.

Detection of arcing to ground and to parallel conductors is implemented as described in section 5.1 Arc Categorization. The amplitude of outgoing current is compared to the amplitude of returning current. If these two current amplitudes do not match, current must be leaving the intended circuit loop. To distinguish a ground arc or parallel conductor arc from a typical ground fault, both the spectrum and the amplitude comparison method is used. Even though the current through a ground arc or parallel conductor arc does not directly flow through the current transformer used on the AFCI board, the varying impedance of the arc will cause noise to appear in the remaining current flowing through the circuit, and thus through the transformer. (This phenomenon can be observed in APPENDIX A – "Arc Test 6" and "Arc Test 7".) If the real-time spectrum matches the "signature" arc spectrum, and the outgoing current and returning current do not match, then a ground or parallel conductor arc is occurring.

The method of extinguishing a ground or parallel conductor arc is precisely the opposite of the method used to extinguish a series and parallel load arc. To extinguish a ground or parallel conductor arc, shorting the positive and negative strings to ground is the best option. Opening the circuit, as done for series and parallel, may force more current through an arc rather than preventing any further current from contributing. Shorting the positive and negative strings to ground provides a path of least resistance to ground for all strings, thereby drawing current away from the electrical arc.

To short the positive and negative strings to ground, high current relays can be used. These high current relays are not currently built into the Smart DC Wall Plug. The logic, and control pins from the microprocessor are however available and capable of shutting down ground and parallel conductor arcs with the use of external relays. This method works for both sides of the Smart DC Wall Plug as every string is grounded.

Our setup had the negative, or neutral, power supply terminal referenced to ground, so only the

positive rail needs to be grounded during a parallel conductor or ground arc. Figure 6-9 shows an

example test setup used to shut off a ground arc. The relay used in testing had a 12 V coil, 100

amp continuous rating (Relay Model LEV100A4ANG by TycoElectronics.) By shorting the

power source, all available current passes through the relay, effectively extinguishing the

electrical arc. The detection and signal delay for this setup matches the response times for series

and parallel load arcs presented in Table 6-2 as the detection method is the same with the addition

of typical current monitoring. Further delay is produced by the response time of the relay used.

This particular relay has a max Operate Time of 25 ms and Release Time of 10 ms, effectively

doubling the delay of the response time for shutting down an arc. To protect the batteries, which

in this case act as the Power Source, the Smart Wall Plug allows the Relay to conduct for a very

short period of time (approximately 100 ms.) Additional testing will be required to determine the

most effective, and safest, duration of relay operation.
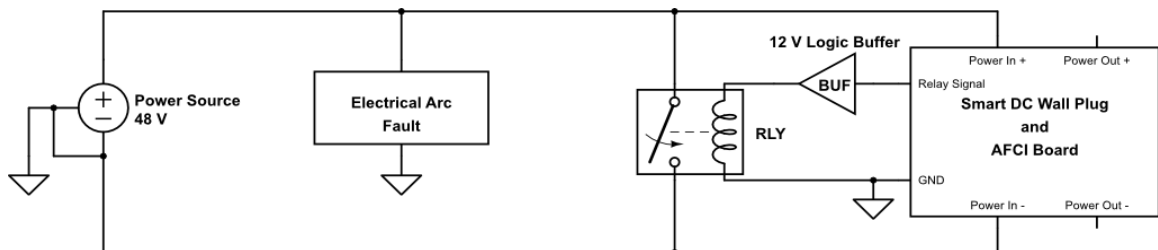
Figure 6-9: Ground Arc Test

Additional methods may be needed to protect the integrity of the batteries if arcing occurs too

often. A possible solution would be attaching a current limiter directly to the batteries as close to

the positive terminal as possible. This would limit the short circuit current to reasonable levels

and protect the batteries from a surge in current.

To summarize, the Smart Wall Plug, in conjunction with the AFCI Board, provides a complete system capable of detecting all forms of electrical arcing detailed in 5.1   Arc Categorization. The system can shut down an arc on either side of the Smart Wall Plug. Series and parallel load arcs can be extinguished with no additional components. Parallel conductor and ground arcs can be extinguished with the addition of an external relay.

The combination of both the Smart DC Wall Plug and AFCI Board, providing the final product, is shown in Figure 6-10.
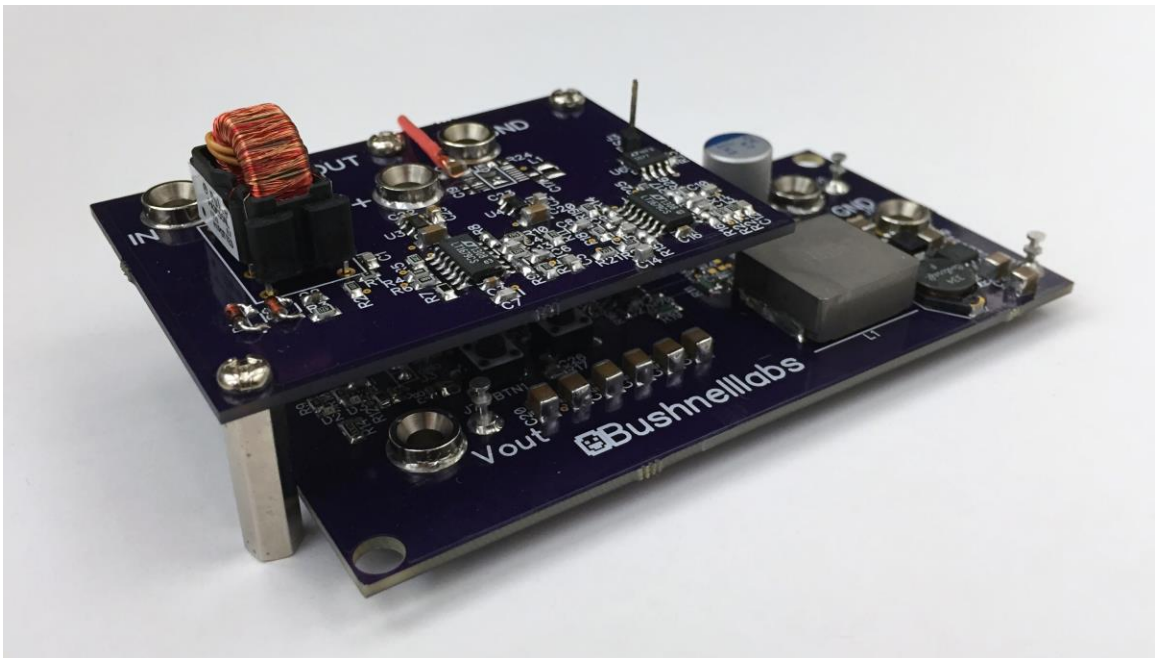
Figure 6-10: Final Product (Smart Wall Plug and AFCI Board)

6.2 Summary of Industry Collaborations

During all phases of this investigation, we worked closely with industry collaborators who provided technical guidance. Specifically, we sought out the advice of engineers at Texas Instruments and Linear Technology.

Arief Hernadi is an Application Engineer in the Power Product Division at Texas Instruments (TI), San Jose. Mr. Hernadi had the first-hand experience in the development of TI's solar application products. Given his knowledge of residential DC electricity, we consulted with Mr. Hernadi in a number of technical aspects of the project. In one case, Mr. Hernandi directed our attention to an evaluation board produced by TI called "RD-195 DC Arc Detection Reference Design Solution." This board was intended to assist non-TI developers in designing a reliable arc detection system for voltages between 80 and 1000 volts. This board does not have the ability to respond to a DC arc fault, but simply provides a signal when a high voltage arc is detected. Mr. Hernandi advised us on the algorithm and components needed for our project, given that our application is different than the TI board. This ensured our device would respond appropriately to DC arcs at 80 volts or less and be much cheaper to produce than the TI RD-195 evaluation board.

Another industry collaborator that we worked closely with during the design and development of our arc detector was Owen Jong, an Associate Design Engineer at Linear Technology. Mr. Jong's insights were invaluable especially during the integration phase of the arc detector and the smart wall plug. Since the Smart Wall Plug utilizes Linear Technology's LTC3891 controller chip, it was very crucial for us to consult with Mr. Jong to ensure that the smart plug is capable of providing an action such as shutting down the smart wall plug upon arc detection. The controller chip used is quite an intricate controller enabling us to have flexible operation of the smart wall plug with various useful features provided by the chip. However, the fact that it is a 20-pin chip makes it tricky to implement. Having Mr. Jong's help was particularly important to ensure safe and reliable operation of the smart wall plug after the arc detector is integrated. Additionally,

since Linear Technology also manufactures discrete components such as OpAmps, we also received technical advices on selecting proper filtering components within the arc detector circuit.

6.3 Adoptability of AFCI for the Smart DC Wall Plug

The Smart Wall Plug was previously designed to perform basic functions, mainly producing the minimum required output voltage to power a DC load. Since DC loads are not standardized, the converter behind the wall plug will automatically adjust the output voltage that a connected DC load requires. A new version of the Smart Wall Plug was developed to support integration with an AFCI board. These upgrades included a new microprocessor with multiple ADCs, components to power the processor, a faster clock, and pin connectors to interface with the AFCI board. The AFCI developed in this project can be attached to the Smart Wall Plug via easy access pin connectors in one of two ways. First, the AFCI may be connected before the wall plug converter, which represents a typical case to protect the wall-plug (and thus the load) as well as surrounding flammables from any arc occurring between the source(s) and the wall plug. The other way to connect the AFCI circuit is after the wall plug; that is between the wall plug converter and the actual physical connection to a load. This will protect the wall plug and everything else behind it from any arc caused by the load. Ideally, the AFCI circuit is placed both before and after the wall plug converter for safer operation of the wall plug.

Based on the current state of the wall plug and realizing the two possible locations of the AFCI circuit with respect to the wall plug converter circuit, the following points of interest will need to be considered for adoptability of the Smart DC Wall Plug in a residential DC system:

1. **Shutdown function:** The wall plug converter should be able to shut itself down upon detection of an arc. This will be done by having the microprocessor used in the wall plug converter an additional output that connects to the shut-down pin of the controller used inside

the wall plug converter. The controller that is currently being used by the wall plug converter does have a pinout for the shutdown function.

2. **Manual reset:** Based on the UL guideline, manual reset of the AFCI upon detecting a real or false arc is required. Therefore, a small reset button on the cover plate of the wall plug (similar to the GFCI reset button) should be made available for easy access of the manual reset by a user. For practicality, just like the GFCI reset button, the button should be normally pushed down under normal operating condition and pushed out under arc fault condition.

3. **Packaging:** The overall physical dimension of the wall plug converter, AFCI circuits, and relay should be placed in an enclosure that is reasonable in physical size, safe, and easy to install. Under full load, the temperature of the wall converter with the AFCI circuit should be kept low to avoid using forced air cooling (fan). During our tests, minimal heat was generated by the Smart Wall Plug and the AFCI circuit board and should not pose a serious problem. To be safe, however, the enclosure should have ventilation or holes to allow good air flow.

4. **Cost:** The cost of the entire DC wall plug system with the AFCI circuit should be kept low. When mass produced, the cost should be $25-$30 per complete unit not including the relay. This cost assumes only one DC wall plug. Multiple wall plugs for the same AFCI circuit is possible by having two wall plug converters in parallel with each other. With two plugs, the cost is estimated to be between $40-$45 per complete set.

5. **Inrush Current:** The wall plug converter should employ a mechanism for soft-starting the output upon resetting the AFCI relay. This feature protects against inrush current that may be caused by the inductive nature of wires, or by an inductive load. The soft-start function ensures that any inrush energy is prevented from flowing through the wall plug converter, which may cause damage to the converter. The controller that is currently used in the wall plug converter provides a pin that enables us to set soft-start time of the converter by simple adjustment of passive components (resistor and capacitor).

CHAPTER 7:
Market and Project Analysis

7.1 Customer Needs

With an increase in renewable energy usage, a strong need exists to ensure this new generation and usage of power is handled in a safe manner. These new power sources, such as Photovoltaic Solar Panels, generate DC power. Historically, all of the United States power demand was met with AC power. The United States and other developed nations now have to also deal with DC power and do so safely. Developing nations are investing in DC power as a way to slowly build their infrastructure in a renewable and modular manner that is capable of using local power sources to serve small villages and communities.

In small developing areas, utilizing renewables is cheaper, and often necessary, on a smaller scale than large power plants. Some developing areas are attempting to use DC power from generation to load, without ever converting to AC. Doing so will save costs as inverters will not be required, and the losses associated with DC-to-AC power conversion will be eliminated.

DC power, however, has safety risks that are typically reduced by using AC power. Therefore, a need exists to develop technologies that can significantly reduce these risks without converting to AC power. A need also exists in developed nations to generate and transmit DC safely until it is converted to AC.

7.2 Market Research

Most competitors of DC AFCI are Photovoltaic inverter manufacturers that have integrated some DC arc-fault circuit protection functionality into their product. DC arc-fault protection is now required (since 2011 via Section 690.11 of ANSI/NFPA 70 of the National Electrical Code) to newly installed PV systems with a maximum voltage of 80 volts or greater [8]. This requirement has been the primary driver for development of DC arc-fault detection. For example, SMA Sunny Boy, an inverter company, now have their high-voltage inverters fully compliant with the 690.11 requirement. Other major inverter companies include: Enphase Energy, Solar Edge, and PV Powered. Those companies that do have DC-AFCI solutions, however, are very narrow in their functionality as they are designed for, and integrated in, systems with little variance and few unknowns. Customizability of the AFCI technology is non-existent with these solutions.

Texas Instruments recently produced a DC-AFCI product that is stand-alone and although it was designed with PV systems in mind, can be integrated into a variety of systems. The product's design is complex, and the overall product is high in price, gearing it towards very large PV array power facilities. The device contains everything needed on a single PCB, which limits its ability to integrate into systems that surpass the PCB's capabilities. It is also out of reach for smaller facilities that have no need for the several extra features offered by the product that are often not necessary.

Current DC-AFCI solutions are either specialized for the one specific product that company produces (Sunny Boy, Enphase shown in Table 1) or is overly complex resulting in too high of a price point for most needs. All but TI's current solution lack an easy upgrade path; the software controls can't be refined without a new physical device or intervention from the manufacturer. Current solutions can't easily be integrated into new designs and can't utilize components already available in the parent system.

Table 7-1: Competing Products Comparison

	Product Manufacturer & Model	Advantages	Disadvantages
	Texas Instrument RD-195	• Highly Programmable • Stand-alone • Can be connected to variety of systems • Power efficient	• Very high cost • All components required for correct operation • No scaled down version • Cannot design into another PCB
	Sunny Boy SMA-SB500TLUS	• Integrated into a system • Does not require additional programming for this product	• Only works with PV systems • Not upgradable
	Enphase M250	• Programs are not required to run on this specific product • Integrated system	• Programming cannot be tuned • Not versatile • Only provides maximum performance on this system

7.3 Customer Archetype

The typical customer of this product will be other engineering firms looking to integrate this technology into their systems, or people working on smaller applications that want the stand-alone version of the product.

Engineering firms typically take the recommendation of the engineers working on the specific product. That engineer will want designs that are easy to integrate into their system without significant changes to their original design. Our product was specifically designed for integration into other systems and engineered to be minimally invasive to the customer's original system

design. Easy integration allows a decrease in costs and physical space needed to implement final functionality.

Companies entering the DC market space will now need to abide by NEC section 690.11. The technology we provide will allow the customers to easily meet that spec without in house research, development, or lengthy testing.

The stand-alone turnkey solution will cater to smaller system designers, or even individuals that just need to hook a safety system up to their local power sources (PV, Wind, etc.). Ease of connection and low cost of product is necessary in this scenario. Customers in this category will likely be living in rural areas, or developing nations, where maintenance of an AFCI system is unlikely. Therefore, the design must be robust and last as long as the local power sources do (up to 30 years for solar arrays). The standalone version of our product contains few moving parts (relays) – which only move when a conductor-to-ground arc occurs between the AFCI and the source, or AFCI and load. Every other component is solid-state which will help the product last as long as the power sources.

7.4 Marketing Requirements

Table 7-2: Marketing Requirements for AFCI

Marketing Requirements	Engineering Specifications	Justification
1	Meets NEC 690.11 and UL Subject 1699B specifications	Does not fail to detect arc fault
1, 2, 6	Meets NEC 690.11 and UL Subject 1699B specifications	Minimal false detections of arc faults
3, 6	Product will not cost over $40	Marketability and competitive pricing against competitors in the same field
4	Customizable and programmable logic board	Customers and clients will be able to easily integrate the AFCI into their systems
5	MCU by default powers by itself when it receives an input voltage	Stand-alone solution
6	AFCI device uses less than 1.5W	Power efficient

Marketing Requirements
1. Detection reliability
2. Minimal false positive detection
3. Cost effective
4. Easily integrated into client's systems
5. Stand-alone turnkey solution available
6. Power efficient

7.5 Project Analysis

1. **Summary of Functional Requirements:** The AFCI monitors the current flowing from the source to the load to detect, and extinguish, any electrical arc fault that is occurring at the source, the load, and in between.

2. **Primary Constraints:** Challenges associate with this project are mostly caused by the seemingly infinite possible environments and conditions that the AFCI will be used. Several source types, load types, connection configurations, and electrical arcing types have to all be accounted for to ensure reliability. Striking a balance between simplicity that can provide a turnkey solution, and adaptability that allows the AFCI to be integrated in specialized systems will prove challenging.

3. **Economic:** Majority of capital for the AFCI is in research, experimentation, and development. The costs of manufacturing are small compared to initial costs of development. System integrators will want a scalable (up or down) device for use in their own products while basic builders will want a turnkey solution. Once the product development is complete, the estimated cost of manufacturing per device will fall in the $10-$15 range assuming 1,000 unit quantity.

4. **If manufactured on a commercial basis:** The AFCI will be mostly sold to other businesses and manufacturers looking to integrate the system into their products. Our likely customers sell products in the 10,000 unit area.

5. **Environmental:** While all manufacturing produces some waste, the AFCI has no inherently toxic material used. The solder used in manufacturing can be lead free. The device has a beneficial effect on the environment as the technology allows renewable power sources to be built and utilized in a safer manner, which will help foster growth in the renewables sector.

6. **Manufacturability:** No significant manufacturing challenges will greatly hinder this project. While board space is at a premium as we would like the device to be as small as

reasonably possible, the size constraints the project faces is reasonable and will not require complex manufacturing techniques.

7. **Sustainability:** Electrically, the AFCI device should last a considerably long time, likely longer than the system it is protecting. The AFCI has only two moving parts, the relays, which only move when a fault has occurred. Therefore, even the only two moving parts that move do not move frequently, and not at all during typical operation. The AFCI will not typically be used in high heat or extreme conditions, and will typically be placed in a stationary location. Therefore, vibration and heat related issues will not affect the AFCI. The AFCI housing will help protect any accidental bumps or bangs from external forces

8. **Ethical:** The ethics of this product lie mostly in the development. If the development of the product is not done thoroughly, the product may fail. Since this is a safety product, the failure could cause fatalities.

9. **Health and Safety:** Using non-toxic material during manufacturing, such as non-leaded solder allow the actual device to be safe to handle. Proper and successful operation of the AFCI is critical to the safety of the styem it is monitoring.

10. **Social and Political:** This product does not have any social or political issues with design or manufacturing. It does however, have an indirect effect on the social issues of environmental sustainability and the worlds progression towards renewable resources

11. **Development:** The development of this device requires the research and development of new detection techniques that do not currently exist. Complex filtering, power circuitry, layout design, and logic programming are all required for this product to work and will therefore provide a learning opportunity in several disciplines within electrical engineering.

CHAPTER 8:
Conclusions

During an electrical arc, the frequency spectrum of the current flowing through the affected circuit will exhibit noise throughout the studied frequency range of 244 Hz-100 kHz. The distribution of this noise across the spectrum will vary depending on the components used, particularly connected loads and the material of the contacts an electrical arc is arcing across. To create a consistent spectrum, active gain and filters are used to shape the noise into a predictable distribution. That predictable distribution of noise provides a "signature" spectrum for which to compare real time spectral analysis of current through a circuit in an effort to detect the presence of an electrical arc. The microprocessor logic utilizes the smooth nature of the "signature" spectrum to discern the difference between an arc and other interferences such as loads with switching frequencies.

The microprocessor is capable of performing spectral analysis, and sending the appropriate signal to extinguish an electrical arc in well under 2 seconds. The Smart Wall Plug, accompanied by the AFCI board, contains all equipment necessary to detect all four types of electrical arcing: series arcing, parallel load arcing, parallel conductor arcing, and ground arcing on either side of the Smart Wall Plug. The Smart Wall Plug, accompanied by the AFCI board, contains all equipment necessary to extinguish series arcing and parallel load arcing on either side of the Smart Wall Plug. To extinguish Parallel conductor arcs and ground arcs, an external high current relay that is not available onboard the Smart Wall Plug is required.

The design of the AFCI Board as well as the upgrades performed to the Smart Wall Plug allow for the use of consumer grade components, keeping costs to a minimum while maintaining proper functionality. The design chosen for the gain and filter stage of the AFCI prevents significant tolerance stack-up, even with the use of inexpensive components.

During our tests, the final Smart Wall Plug and AFCI board never failed to detect the presence of an electrical arc. In every test case, the appropriate signal to extinguish the arc was sent to either the current controller or the relay in well under the 2 second standard set by UL 1699B.

Tests performed in an attempt to cause a false positive detection (nuisance trips) by the Smart Wall Plug failed, giving evidence to the success of the logic strategy implemented as well as the uniqueness of the "signature" spectrum of an arc. These tests, however, were limited in scope to interferences purposefully created by function generators. Additional testing is recommended using a variety of loads to ensure minimal nuisance tripping in the field.

Future work will include integrating sufficient relays onboard the Smart Wall Plug to allow the extinguishment of parallel conductor arcs and ground arcs without any external parts. Future development will also put all components onto a single PCB to help reduce size and costs. Further research will include further attempts to cause nuisance trips, followed by adjustment of the algorithms used for arc detection.

While nuisance tripping has not been tested as rigorously as desired, detection of an occurring arc by the Smart Wall Plug and AFCI board has been well tested over the course of this project and has proven itself effective, responsive, and safe.

The success of this project furthers the capabilities of the Smart DC Wall Plug and provides another stepping stone to the adoption of DC power amongst developed and developing nations and communities. We are convinced the DC AFCI technology developed in this project will enable better energy efficiency, accelerate adoption of electric vehicles and alternative energy sources, enhance service reliability, and of course, increase safety.

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APPENDICES

APPENDIX A:
Example Arcing Spectra Under Varying Conditions

Appendix A provides the spectrum of a few arcing tests. Note that not all tests performed are provided in this appendix. The presented tests, however, are representative of the concept and of the other tests performed. The inclusion of all other tests would only provide redundancy in this Appendix.

A.1   Arc Test 1 (Figure A-1, Figure A-2)

- Testing Setup: Figure 5-5: Testing Setup 1

- Arcing Device: Copper Cylinder Contacts

- Power Source: HP 6032A = 48 V

- Load 1: OPEN

- Load 2:

    o   Iteration 1: BK Precision 8510 Electronic Load = 9 Ω

    o   Iteration 2: Power Resistor = 9 Ω

- Spectrum Range: 244 Hz-100 kHz

Arc Test 1 shows the difference in the spectrum of two different types of loads. The first iteration uses an active electronic load while the second iteration of this test uses a simple passive power resistor. The impedance of both tests were the same (9 Ω.) Through our tests, the largest differences in the spectra were caused by differences in the type of load used as well as the material of the contacts the electrical arc was arcing across. The impedance of the load (e.g. 6 Ω vs. 20 Ω) made very little, if any, difference in the spectrum. The spectrum during an arc, however, appears by this test to be fairly close to the baseline.
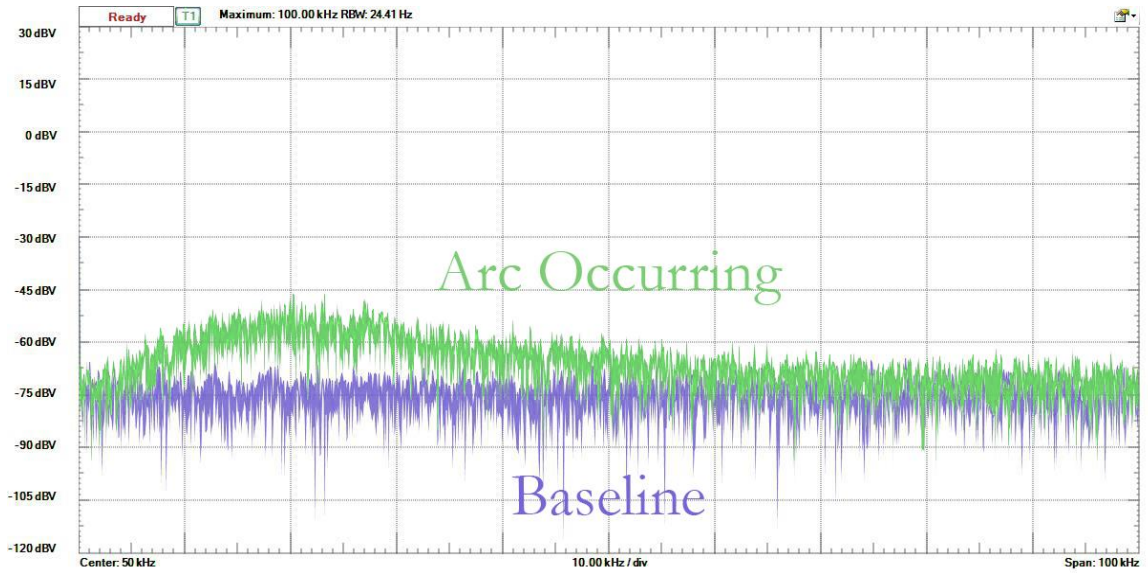
68

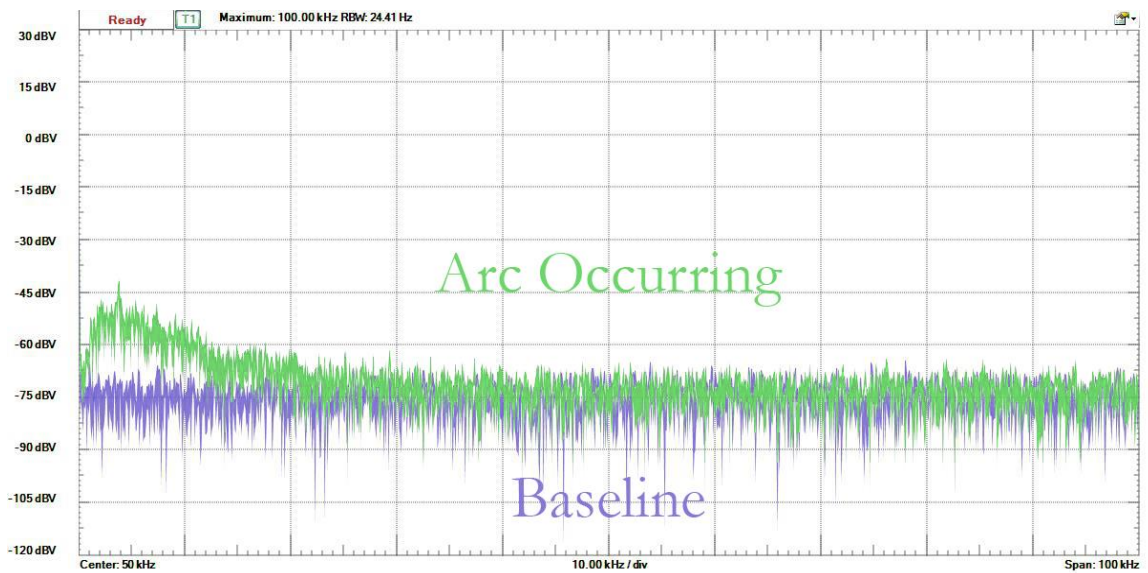**Figure A-1: Arc Test 1, Iteration 1**

Figure A-2: Arc Test 1, Iteration 2

A.2 Arc Test 2 (Figure A-3)

- Testing Setup: Figure 5-5: Testing Setup 1

- Arcing Device: Copper Cylinder Contacts

- Power Source: HP 6032A = 48 V

- Load 1: Power Resistor = 4.5 Ω

- Load 2: BK Precision 8510 Electronic Load = 15 Ω

- Spectrum Range: 244 Hz-100 kHz

This test provides a combination of two loads: a power resistor in parallel with the arcing device, and an electronic load in series with the arc. The resulting spectrum is concerning as arcing spectrum is nearly identical to the baseline noise floor and will be unusable in application.
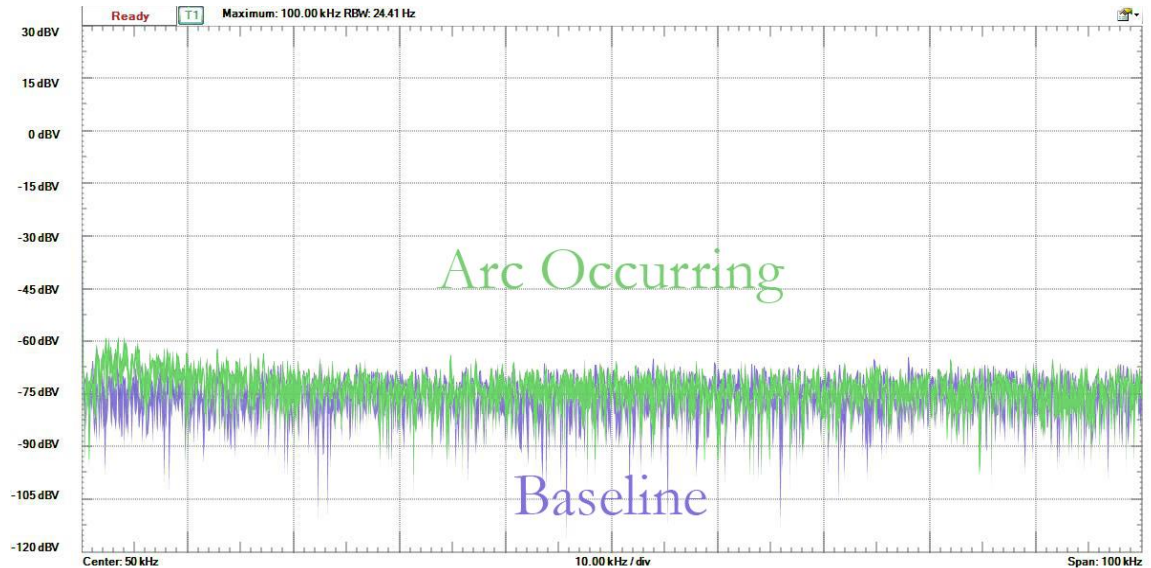

Figure A-3: Arc Test 2, Iteration 1

To provide reassurance that the current transformer was not having a significant effect on the spectrum, a current sensor was used instead of a current transformer. Setup is shown in Figure A-4. The results do not significantly differ between a current sensor and a current transformer.
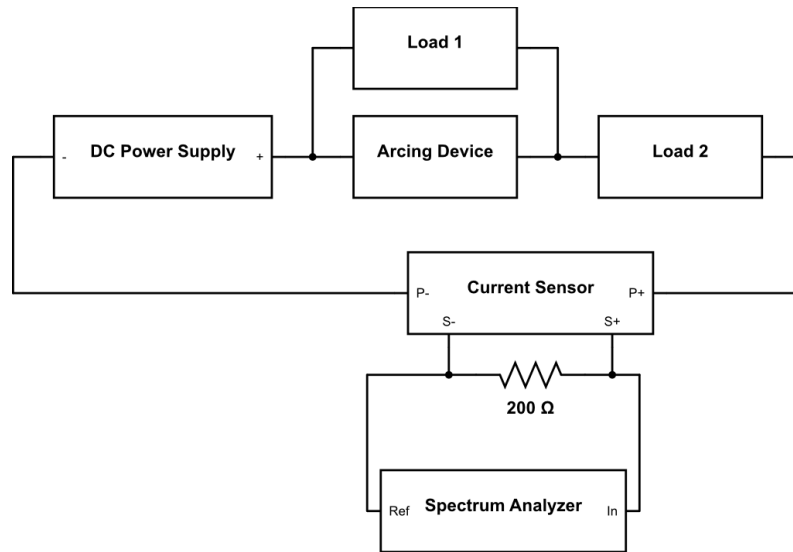

Figure A-4: Testing Setup 2

A.3   Arc Test 3 (Figure A-5)

- Testing Setup: Figure A-4: Testing Setup 2

- Arcing Device: Copper Cylinder Contacts

- Power Source: HP 6032A = 48 V

- Load 1: OPEN

- Load 2: BK Precision 8510 Electronic Load = 7 Ω

- Spectrum Range: 244 Hz-100 kHz

The result shown in Figure A-5, which used the BK Precision 8510 Electronic Load, did not significantly differ from Figure A-1, which utilizes the same load. Slight difference in magnitude is attributed to the different step down ratios used by the transformer versus the current sensor.
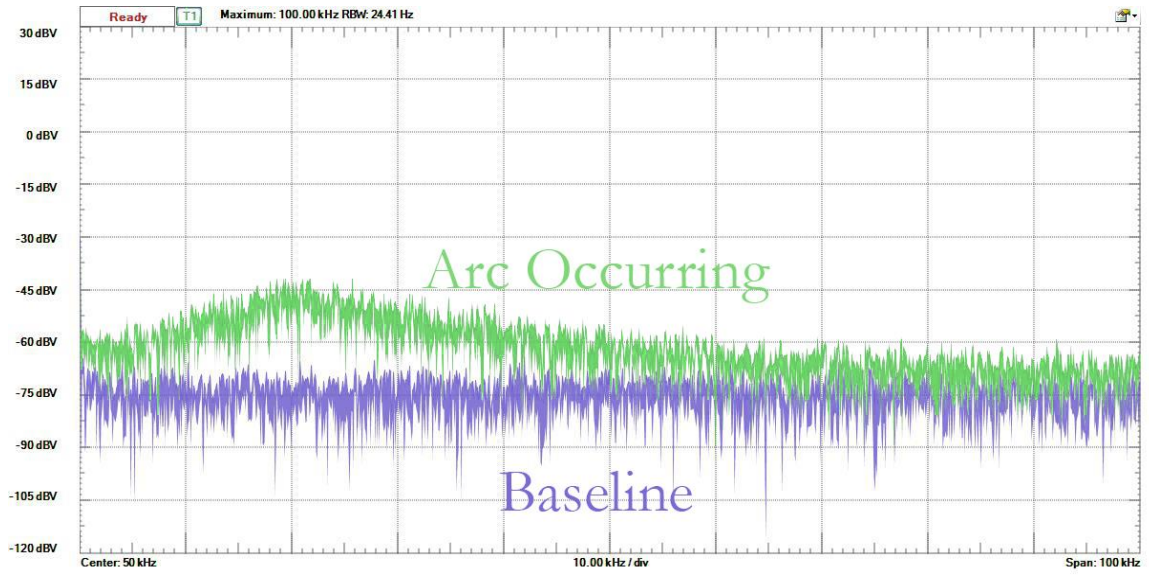
71

Figure A-5: Arc Test 3, Iteration 1

At this point the possibility of lost information due to limited resolution was considered. Arc Test 4 utilizes Testing Setup 5 shown in Figure 5-7 to determine if information has been lost when using a transformer or current sensor.

A.4   Arc Test 4 (Figure A-6, Figure A-7)

- Testing Setup: Figure 5-7: Testing Setup 5

- Arcing Device: Knife Switch

- Power Supply: HP 6032A

    o   Iteration 1: 48 V

    o   Iteration 2: 60 V

- Power Resistor = 6 Ω

- BK Precision 8510 EL = 8 Ω

- Spectrum Range: 244 Hz-100 kHz

Arc Test 4 produces the spectrum by measuring the voltage across a power resistor that is in the main circuit line. This allows the full current amplitude to be used, rather than stepping it down through a transformer before analysis. Figure A-6 and Figure A-7 show an obvious difference in the magnitude during an electrical arc versus the baseline. The overall distribution shape, however, is near identical.
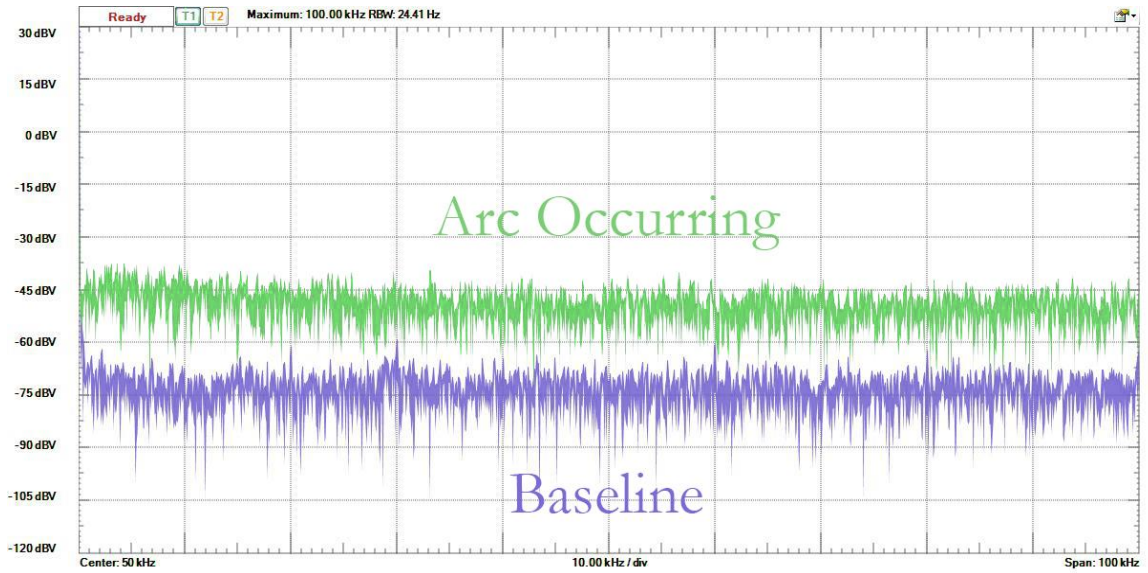
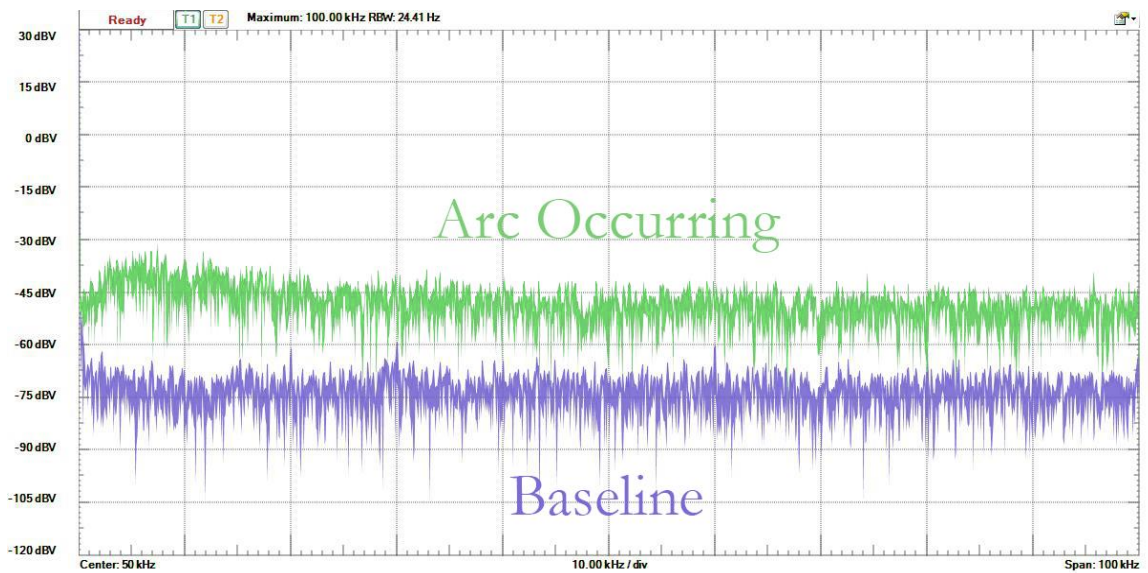**Figure A-6: Arc Test 4, Iteration 1**

Figure A-7: Arc Test 4, Iteration 2

Measuring across a load is not possible in the field. A current transformer is required. To detect the small signals, a low noise operational amplifier is used to gain the signal before analysis.

A.5   Arc Test 5 (Figure A-8, Figure A-9, Figure A-10, Figure A-11, Figure A-12, Figure A-13)

- Testing Setup: Figure 5-9: Testing Setup 6 (Implements Gain)

- Arcing Device:

    o Iteration 1: Cylindrical Copper Contacts

    o Iteration 2: Cylindrical Copper Contacts

    o Iteration 3: Cylindrical Copper Contacts

    o Iteration 4: Aluminum Knife Switch

    o Iteration 5: Aluminum Knife Switch

    o Iteration 6: Cylindrical Copper Contacts

- Power Supply:

    o Iteration 1: HP 6032A = 48 V

    o Iteration 2: HP 6032A = 30 V

    o Iteration 3: HP 6032A = 48 V

    o Iteration 4: HP 6032A = 48 V

    o Iteration 5: HP 6032A = 48 V

    o Iteration 6: HP 6032A = 48 V

- Load 1:

    o Iteration 1: OPEN

    o Iteration 2: OPEN

- o Iteration 3: OPEN

  o Iteration 4: OPEN

  o Iteration 5: Power Resistor = 6 Ω

  o Iteration 6: BP Precision 8510 EL = 10 Ω

- Load 2:

  o Iteration 1: Power Resistor = 9 Ω

  o Iteration 2: Power Resistor = 9 Ω

  o Iteration 3: BP Precision 8510 EL = 10 Ω

  o Iteration 4: BP Precision 8510 EL = 10 Ω

  o Iteration 5: Power Resistor = 9 Ω

  o Iteration 6: Power Resistor = 5 Ω

- Spectrum Range: 244 Hz-100 kHz

- Gain: -180 V/V

The results from this test show a variety of possible spectrum responses. The Load type, and Arcing Device had the most effect on the shape of the response. Voltage, Power Supply, and resistance of the load had little effect on the responses. Having no load in parallel with the arc versus having a load in parallel provided similar spectra; any differences were caused by the type of load used and which load was pulling more current.
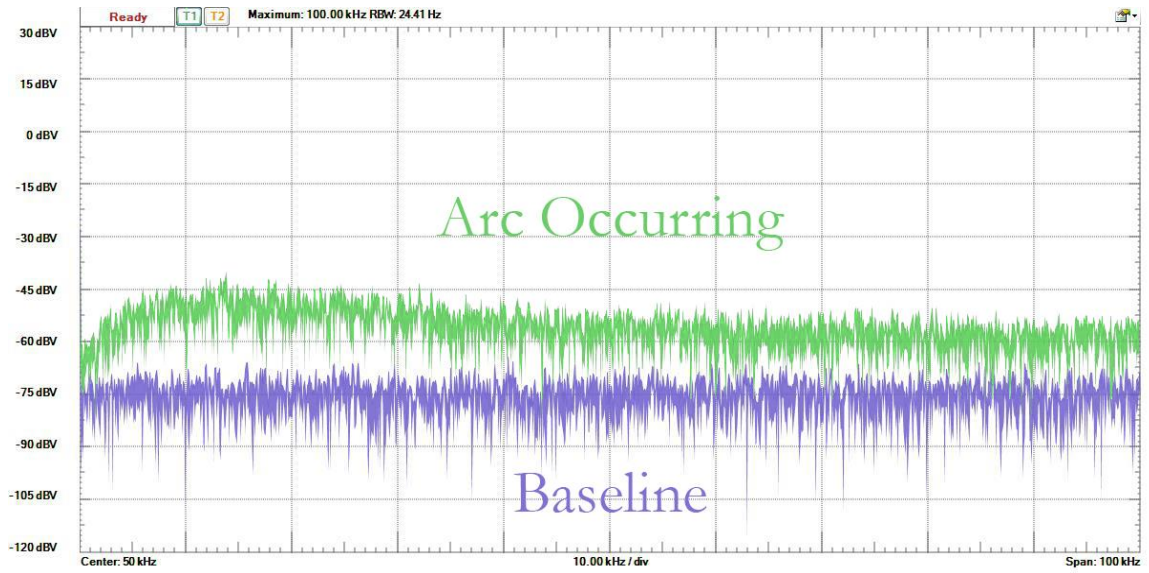
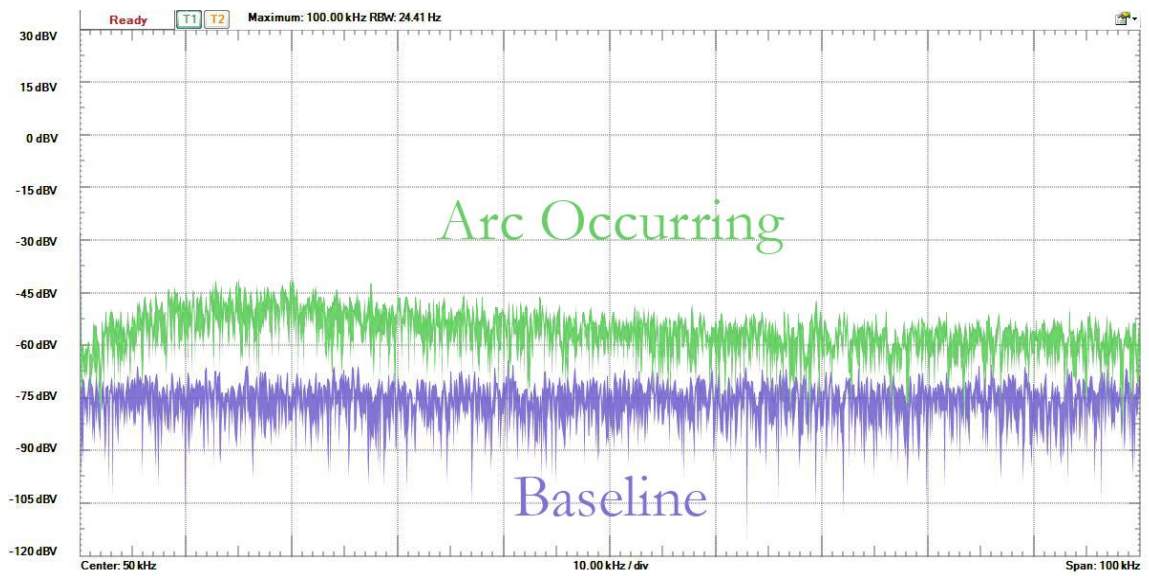**Figure A-8: Arc Test 5, Iteration 1**
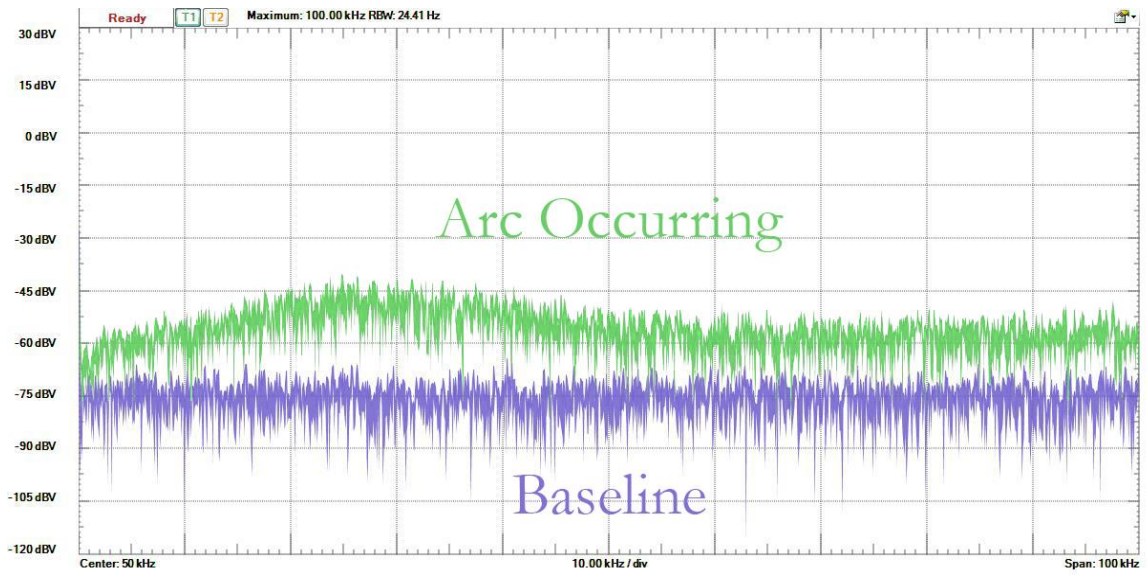

Figure A-9: Arc Test 5, Iteration 2

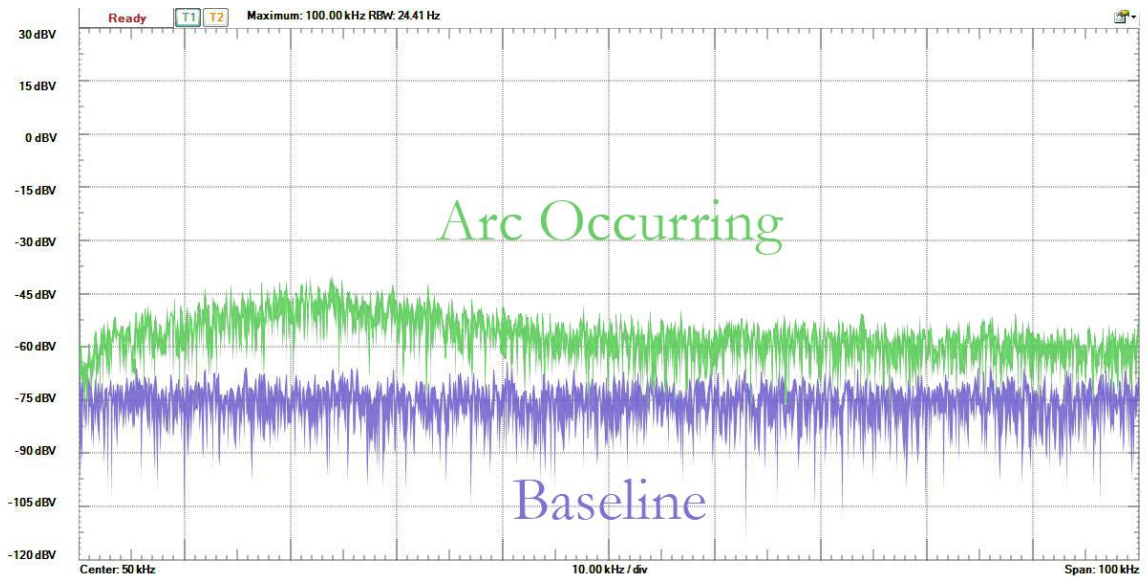**Figure A-10: Arc Test 5, Iteration 3**

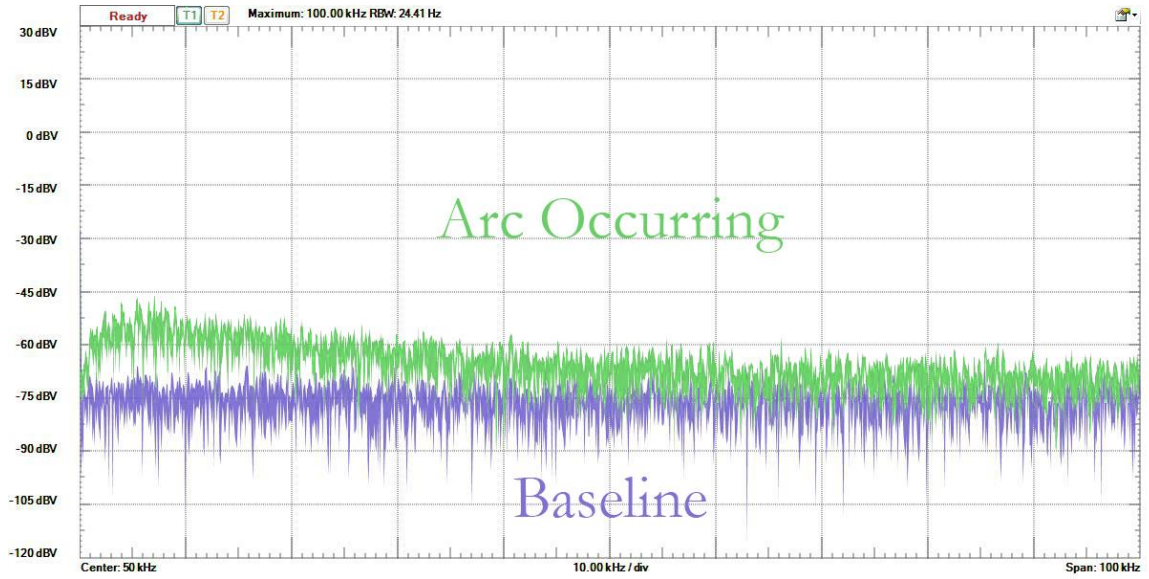**Figure A-11: Arc Test 5, Iteration 4**

Figure A-12: Arc Test 5, Iteration 5

Figure A-13: Arc Test 5, Iteration 6

To test the possibility of a Ground Arc, Arc Test 6 was performed using the setup shown in Figure A-14. It can be seen that in this setup a ground arc is similar to a parallel load arc except the current produced by the arc is not directly returning to the negative terminal. The negative terminal is however connected to ground and is so referenced to the same voltage level.

A.6 Arc Test 6 (Figure A-15)

- Testing Setup: Figure A-14: Ground Arc Testing Setup

- Arcing Device: Knife Switch

- Power Supply: HP 6032A

  o Iteration 1: HP 6032A = 48 V

- Power Resistor = 6 Ω

- Load: BK Precision 8510 Electronic Load = 8 Ω

- Spectrum Range: 244 Hz-100 kHz

Figure A-14: Ground Arc Testing Setup

The results of this test show that noise is still created and detected by the spectrum analyzer. The magnitude of the noise is lower that in series and parallel load tests. Increases gain and sensitivity will likely be needed in the final product to reliably detect this arcing type.
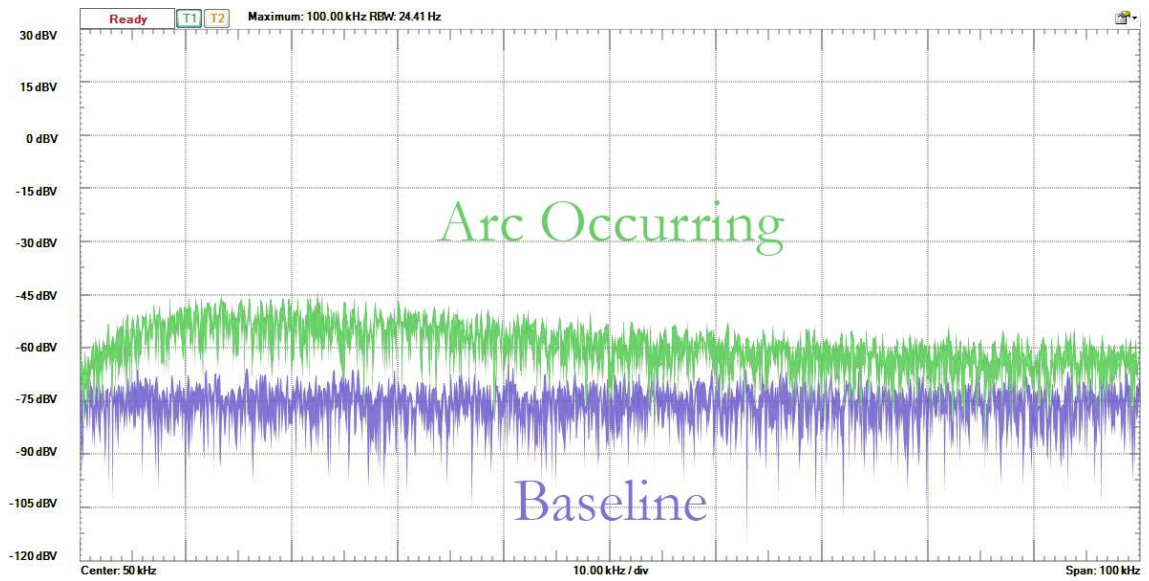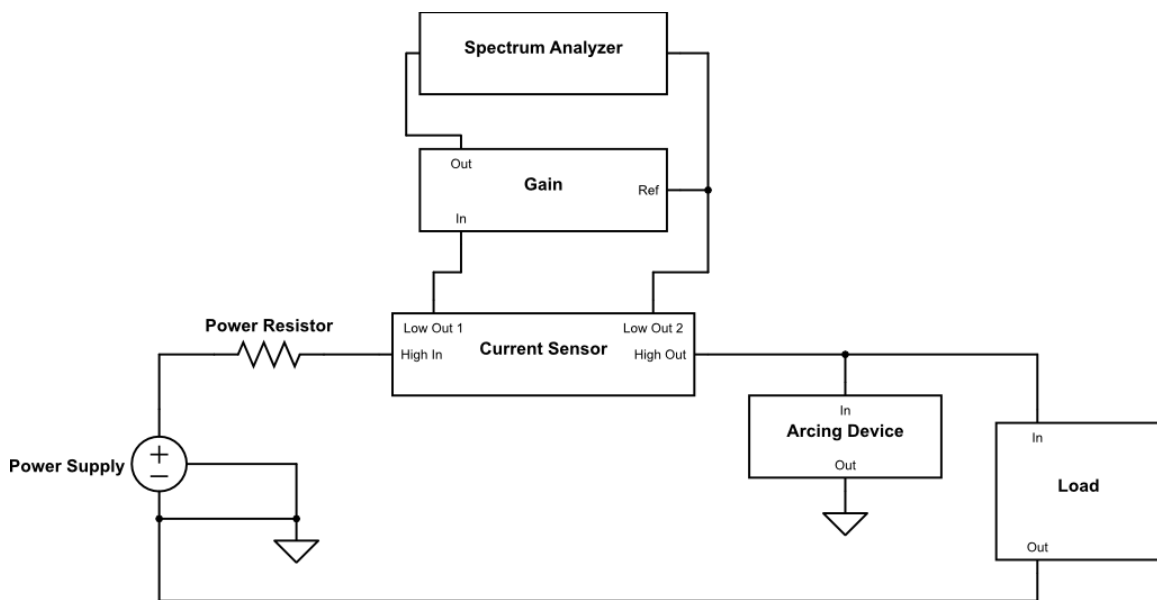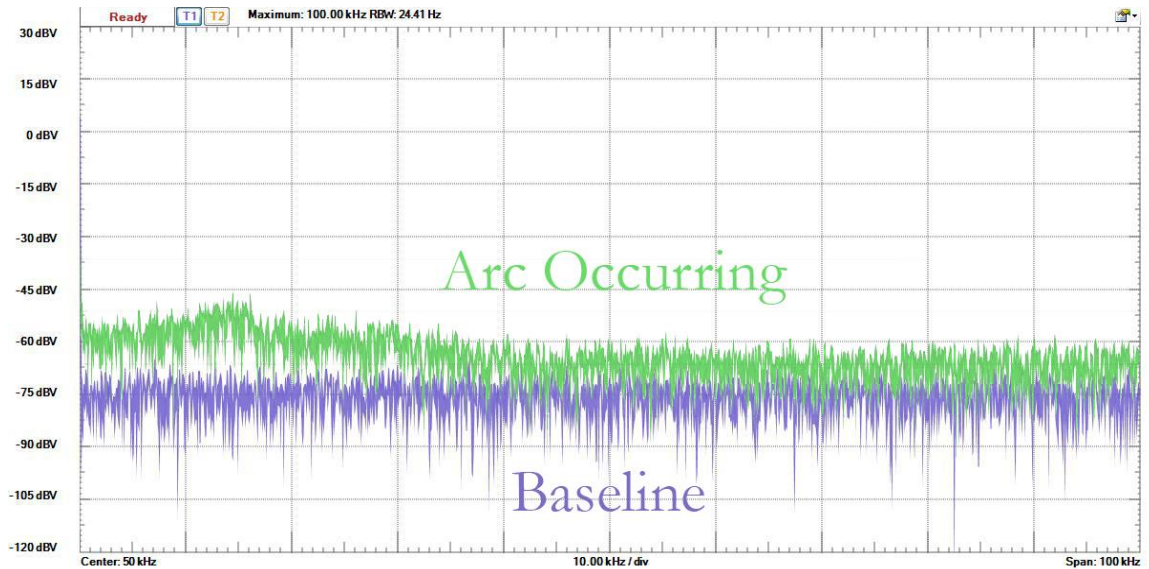

Figure A-15: Arc Test 6, Iteration 1

To test the possibility of a parallel conductor arc, Arc Test 7 was performed using the setup shown in Figure A-16. Two Hall Effect current sensors were used (one per circuit loop), fed through a gain filter, and ultimately to the spectrum analyzer.

A.7   Arc Test 7 (Figure A-17)

- Testing Setup: Figure A-16: Parallel Conductor Arc Test

- Arcing Device: Copper Cylindrical Contacts

- Power Supply 1: HP 6032A

- Power Supply 2: GW Laboratory DC Power Supply GW Model: GPR-6060D

- Electronic Load: BK Precision 8510 Electronic Load

- Spectrum Range: 244 Hz-100 kHz

Figure A-16: Parallel Conductor Arc Test

Figure A-17: Arc Test 7, Iteration 1

The results of Arc Test 7 show noise is created through the circuit, but the magnitude is low. Additional gain and sensitivity in the final product will be required for reliable detection when using a frequency spectrum. As stated in the body of this report, the current through each loop is changed due to the arc and can be easily detected by basic monitoring of the current leaving and returning to each supply.
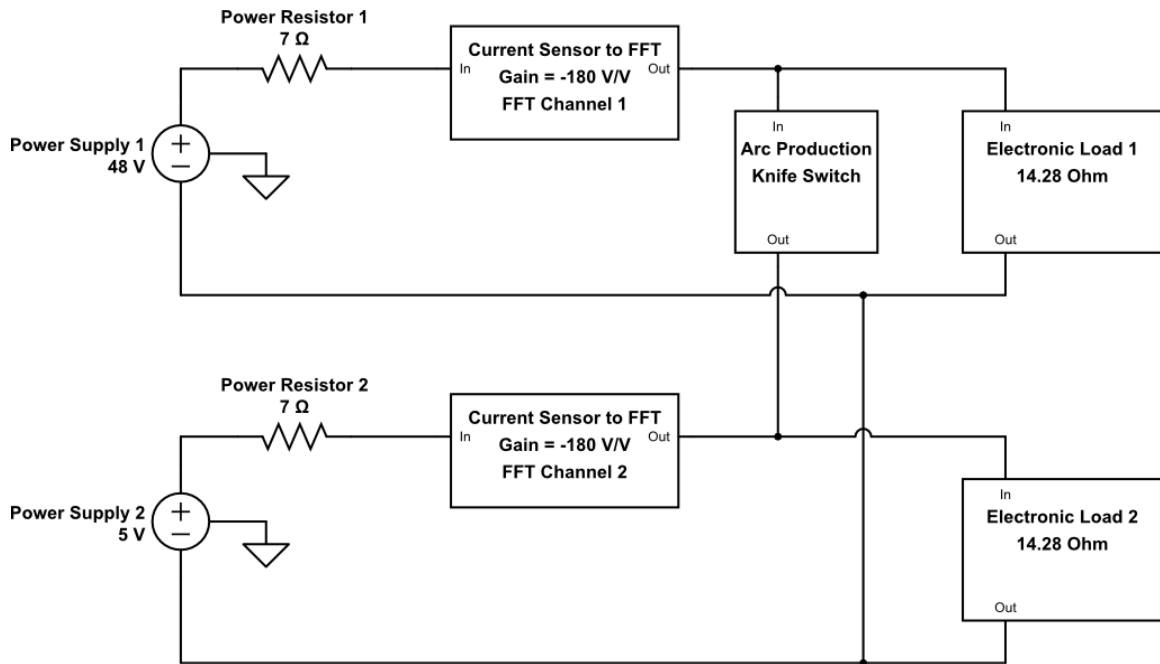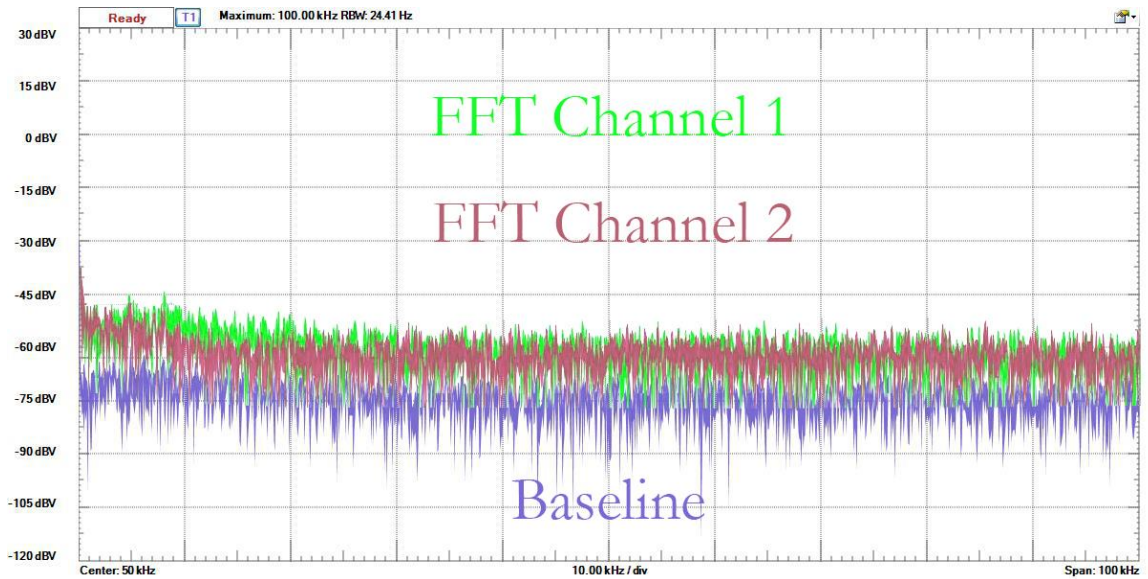
After designing the analog processing circuit – which includes a clamping, gain, filtering, and buffering section – the spectrum during an arc was measured for numerous setup cases. Arc Test 8 shows a few of these tests. The screenshots presented in Arc Test 8 show a high level of consistency. All tests we performed, both for loads in series and parallel with the arc, as well as Ground and parallel conductor arcs, produce the same results seen in Arc Test 8.

A.8   Arc Test 8 (Figure A-18, Figure A-19, Figure A-20, Figure A-21, Figure A-22)

- Testing Setup: Figure 5-15: Testing Setup 7 (Utilizing Complete Clamping, Gain, and Filtering Circuit)
- Arcing Device:
  - Iteration 1: Cylindrical Copper Contacts
  - Iteration 2: Cylindrical Copper Contacts
  - Iteration 3: Cylindrical Copper Contacts
  - Iteration 4: Aluminum Knife Switch
  - Iteration 5: Aluminum Knife Switch
- Power Supply:
  - Iteration 1: HP 6032A = 48 V
  - Iteration 2: HP 6032A = 48 V

- o Iteration 3: Power Ten P83C-25040 = 80 V

- o Iteration 4: HP 6032A = 60 V

- o Iteration 5: HP 6032A = 60 V

- Load 1:

  - o Iteration 1: OPEN

  - o Iteration 2: Power Resistor = 6 Ω

  - o Iteration 3: OPEN

  - o Iteration 4: Power Resistor = 5 Ω

  - o Iteration 5: OPEN

- Load 2:

  - o Iteration 1: Power Resistor = 9 Ω

  - o Iteration 2: BK Precision 8510 Electronic Load = 10 Ω

  - o Iteration 3: Series Combination of Power Resistor = 6 Ω and BK Precision
    8510 Electronic Load = 8 Ω

  - o Iteration 4: Series Combination of Power Resistor = 6 Ω and BK Precision
    8510 Electronic Load = 8 Ω

  - o Iteration 5: Power Resister = 9 Ω

- Spectrum Range: 244 Hz-100 kHz
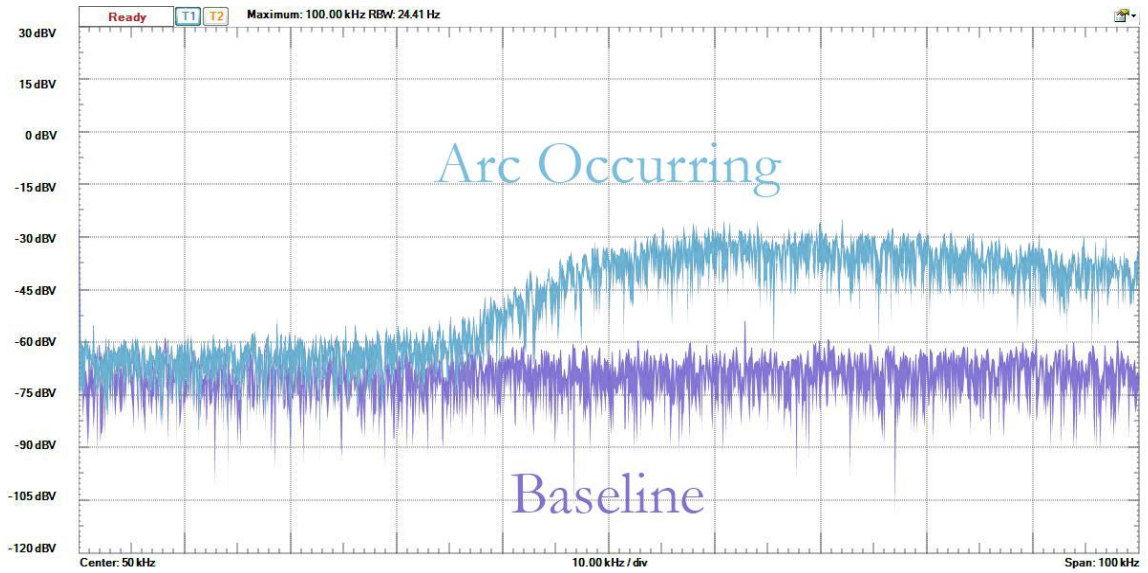
Figure A-18: Arc Test 8, Iteration 1
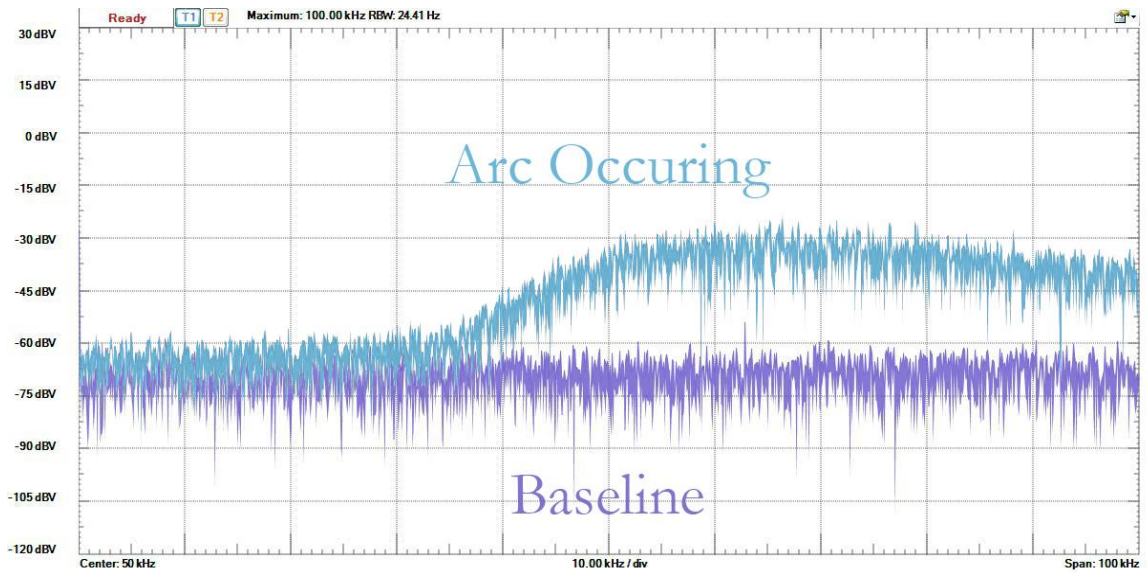
Figure A-19: Arc Test 8, Iteration 2
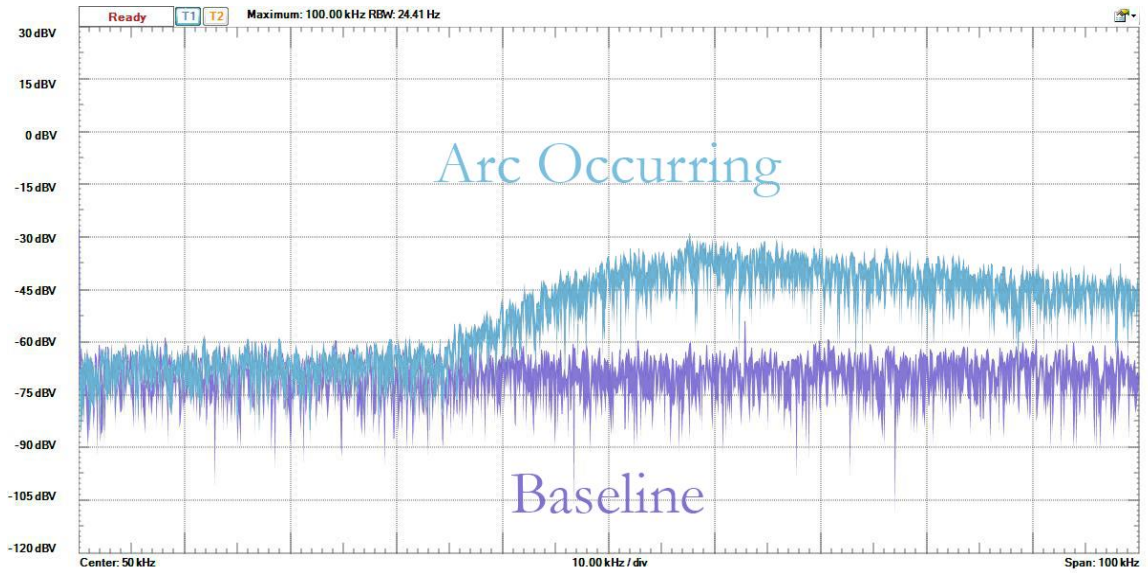
Figure A-20: Arc Test 8, Iteration 3
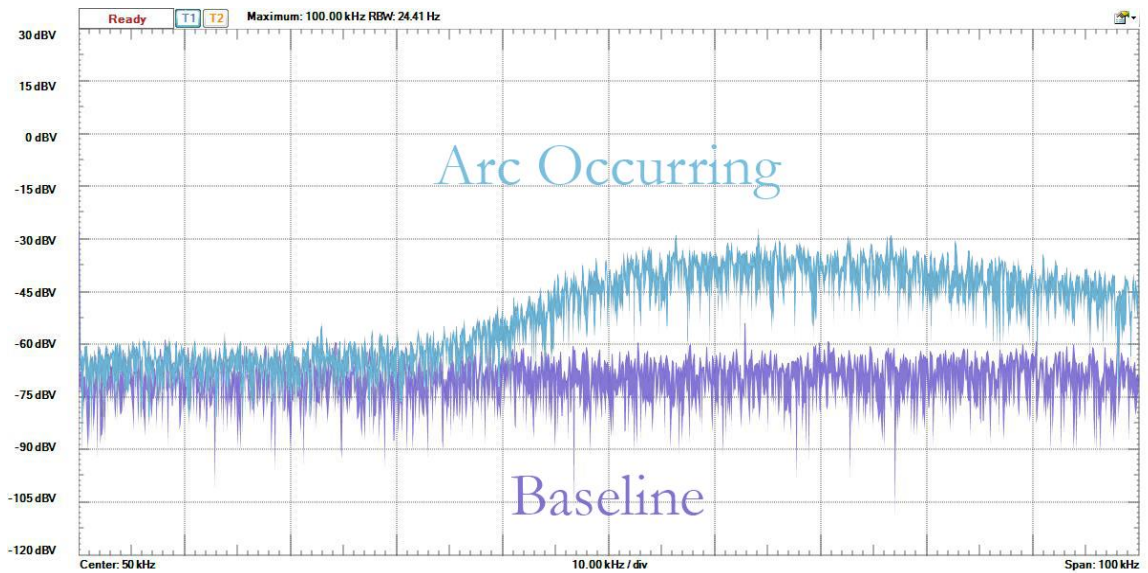
Figure A-21: Arc Test 8, Iteration 4
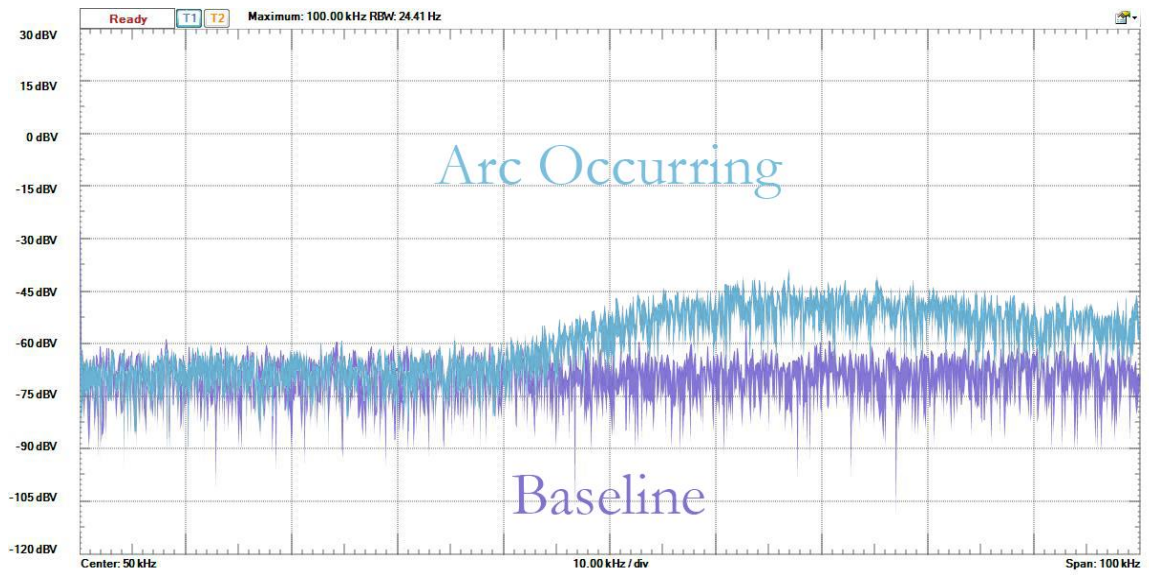
Figure A-22: Arc Test 8, Iteration 5

APPENDIX B:
Setup Components List for Experiments

This Appendix details the components used during setup for experiments shown in the body of

this report.

Figure 5-6:

- Spectrum compilation of various arcing events from test results using Testing

  Setup 1 shown in Figure 5-5

- Individual tests shown in APPENDIX A - "Arc Test 1" through "Arc Test 3"

Figure 5-8:

- Test Setup 5 shown in Figure 5-7

- Power Resistor = 4 Ω

- Electronic Load: BK Precision 8510 Electronic Load = 10 Ω

- Arcing Device: Copper Cylinder Contacts

- More details in APPENDIX A – "Arc Test 4"

Figure 5-10:

- Spectrum compilation of various arcing events from test results using Testing

  Setup 6 shown in Figure 5-9

- Individual tests shown in APPENDIX A – "Arc Test 5" through "Arc Test 7"

Figure 5-11:

- Arcing Device: Knife Switch

- Power Source: HP 6032A = 48 V

- Power Resistor = 6 Ω

- Electronic Load: BK Precision 8510 Electronic Load = 8 Ω

- Spectrum Range: 244 Hz-100 kHz

Figure 5-12:

- Arcing Device: Knife Switch

- Power Source: HP 6032A = 48 V

- Power Resistor = 6 Ω

- Electronic Load: BK Precision 8510 Electronic Load = 8 Ω

- Spectrum Range: 2.44 kHz-1 MHz

Figure 5-16:

- Spectrum Compilation of various arcing events from test results using Testing Setup 7 shown in Figure 5-15

- Provides the final spectrum that will serve as the "signature" spectrum of an electrical arc

Figure 6-2:

- Averages of the microprocessor FFT results of 25 arcing tests using various loads, arcing materials, voltages, and load arrangements

- Testing Setup 8 shown in Figure 6-1

Figure 6-3:

- Standard Deviation of the microprocessor FFT results of 25 arcing tests using various loads, arcing materials, voltages, and load arrangements
- Testing Setup 8 shown in Figure 6-1

Figure 6-4:

- Testing Setup: Figure 6-1: Testing Setup 8
- Arc Occurring: YES
- Arcing Device: Aluminum Knife Switch
- Power Supply: HP 6032A = 48 V
- Load 1: OPEN
- Load 2: BP Precision 8510 EL = 18 Ω
- Sampling Frequency = 250 kHz
- Nyquist Frequency = 125 kHz
- Signal Out = 1 (Microprocessor Detected Arc)

Figure 6-5:

- Testing Setup: Figure 6-1: Testing Setup 8
- Arc Occurring: YES
- Arcing Device: Aluminum Knife Switch
- Power Supply: HP 6032A = 48 V

- Load 1: OPEN

- Load 2: BP Precision 8510 EL = 18 Ω

- Sampling Frequency = 250 kHz

- Nyquist Frequency = 125 kHz

- Signal Out = 1 (Microprocessor Detected Arc)

Figure 6-6:

- Power Supply: HP 6032A = 48 V

- Channel 1: Time Signal Output of Gain and Filtering System

- Channel 2: Shutoff Signal Output from Microprocessor

- Inline Resistive Load: Power Resistor = 9 Ω

- Arcing Device: Aluminum Knife Switch

- Shutoff Signal Delay: 18.302 ms

Figure 6-7:

- Power Supply: HP 6032A = 36 V

- Channel 1: Voltage across Inline Resistive Load

- Channel 2: Shutoff Signal Output from Microprocessor

- Inline Resistive Load: Power Resistor = 9 Ω

- Arcing Device: Aluminum Knife Switch

- Shutoff Signal Delay: 19.82 ms

APPENDIX C:
Gain and Filter Design Specifications

C.1   OpAmp STG1 and STG2 Design
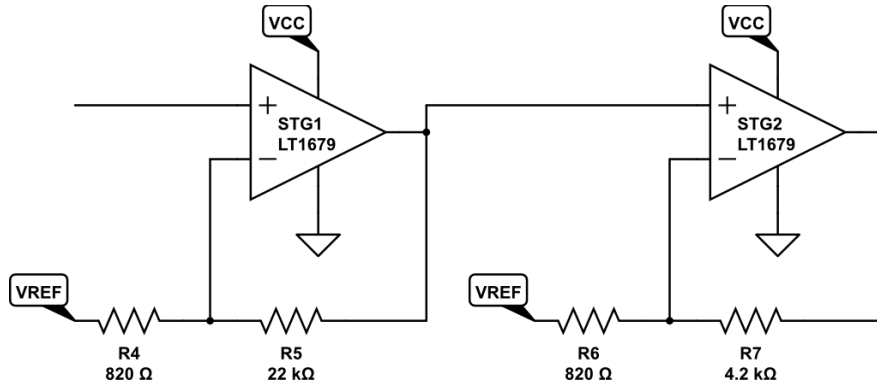
Figure C-1: OpAmp STG1 and STG2 Gain Stages

STG1:

$$Gain_{STG1}: A_v = \left(1 + \frac{R5}{R4}\right) = \left(1 + \frac{22000}{820}\right) = 27.8 \; V/V$$

$$Gain_{STG1} \; (dB): A_v = 20\log(27.8) = 28.9 \; dB$$

STG2:

$$Gain_{STG2}: A_v = \left(1 + \frac{R5}{R4}\right) = \left(1 + \frac{4200}{820}\right) = 6.12 \; V/V$$

$$Gain_{STG2} \; (dB): A_v = 20\log(6.12) = 15.74 \; dB$$

Total (STG1 and STG2):

$$Gain_{Total} = (Gain_{STG1}) * (Gain_{STG2}) = (27.8)(6.12) = 170.1 \; V/V$$

$$Gain_{Total}(dB) = 20\log(170.1) = 44.61 \; dB$$

C.2 OpAmp STG3 Design
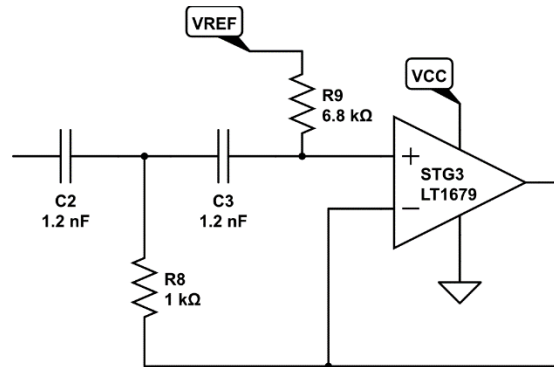
Figure C-2: OpAmp STG3 Filter

$$Transfer\ Function: G(s) = \frac{s^2}{s^2 + 245098s + 102124183007}$$

Cut-Off Frequency: 50850.9 Hz

Quality Factor: Q=1.304

Damping Ratio: ζ=0.383

Oscillation Frequency: 46972 Hz
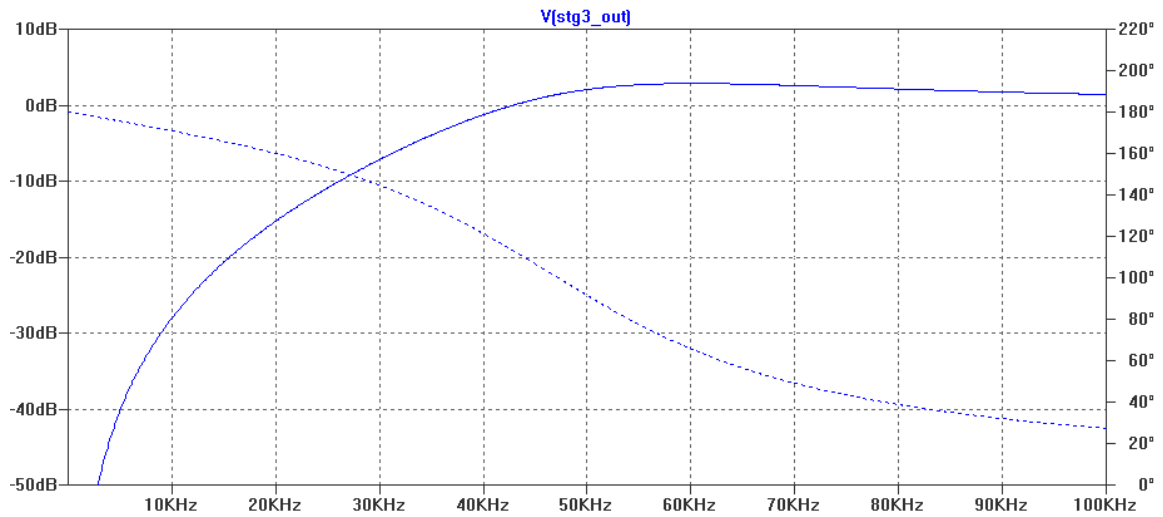
Figure C-3: STG3 Frequency Response

93

C.3   OpAmp STG4 Design
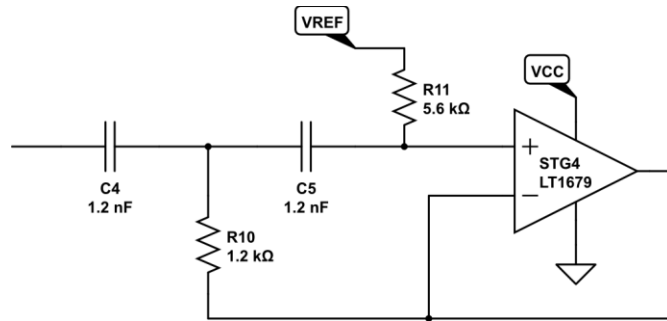
Figure C-4: OpAmp STG4 Filter

$$Transfer\ Function: G(s) = \frac{s^2}{s^2 + 297619s + 103339947090}$$

Cut-Off Frequency: 51162.8 Hz

Quality Factor: Q=1.08

Damping Ratio: ζ=0.463

Oscillation Frequency: 45351 Hz
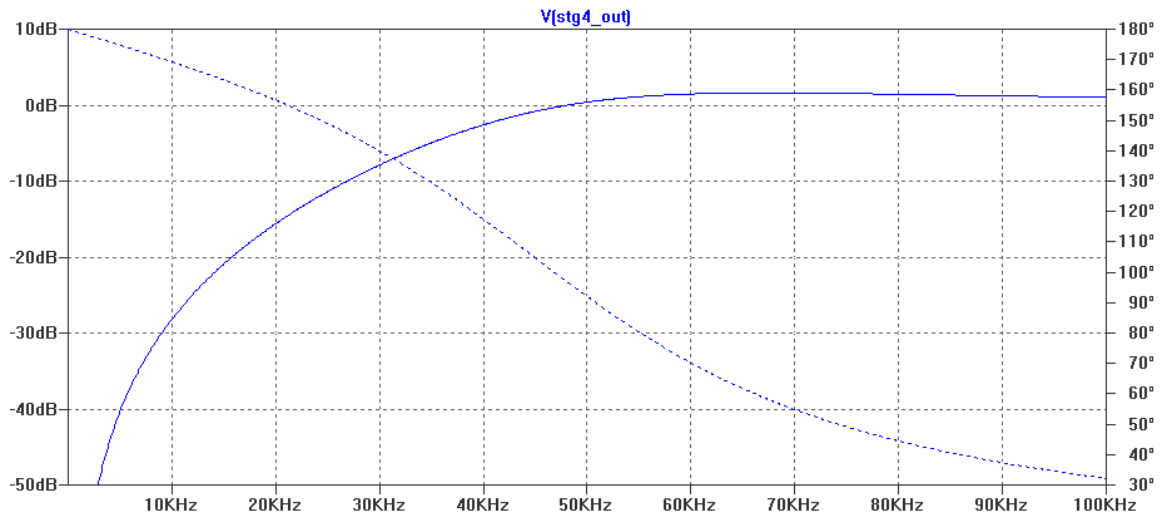
Figure C-5: STG4 Frequency Response

C.4   OpAmp STG5 Design
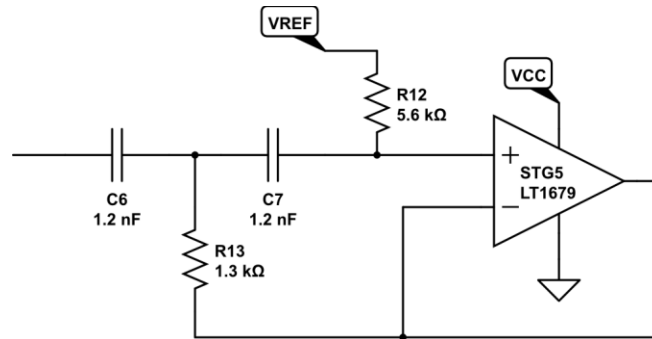
Figure C-6: OpAmp STG5 Filter

$$Transfer\ Function:\ G(s) = \frac{s^2}{s^2 + 297619s + 95390720391}$$

Cut-Off Frequency: 49156 Hz

Quality Factor: Q=1.04

Damping Ratio: ζ=0.482

Oscillation Frequency: 45074 Hz
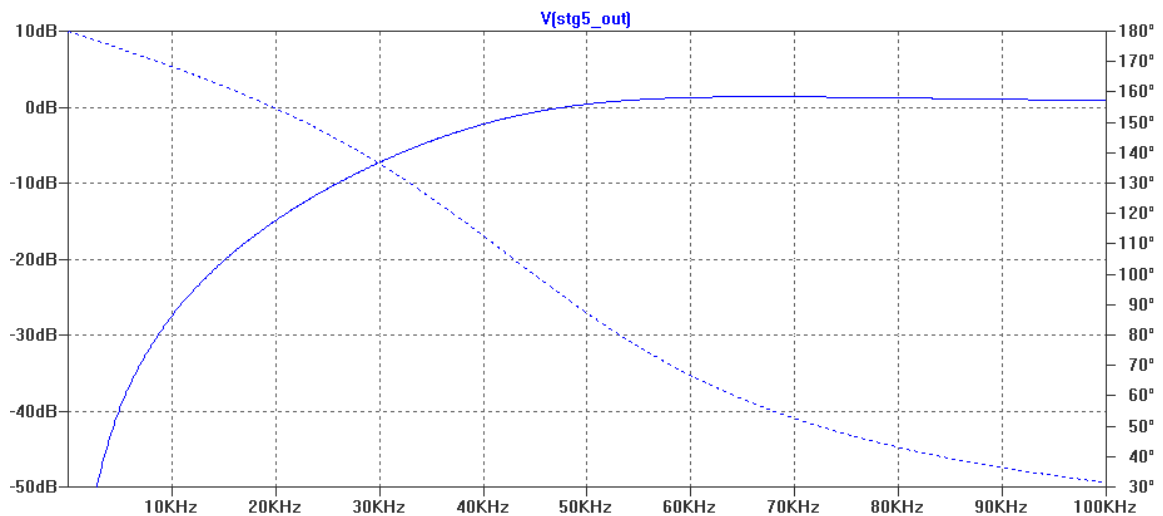
Figure C-7: STG5 Frequency Response

C.5   OpAmp STG6 Design
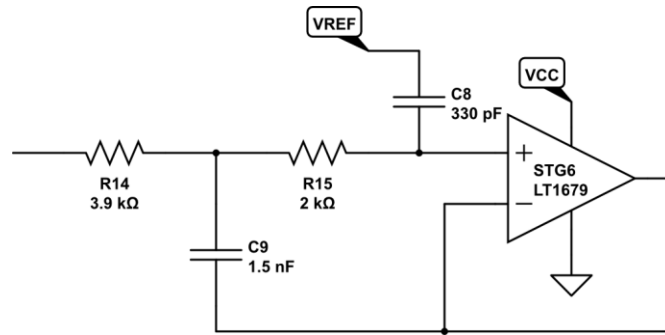
Figure C-8: OpAmp STG6 Filter

$$Transfer\ Function{:}\ G(s) = \frac{s^2}{s^2 + 504274s + 259000259000}$$

Cut-Off Frequency: 80997 Hz

Quality Factor: Q=1.01

Damping Ratio: ζ=0.495

Oscillation Frequency: 70357 Hz
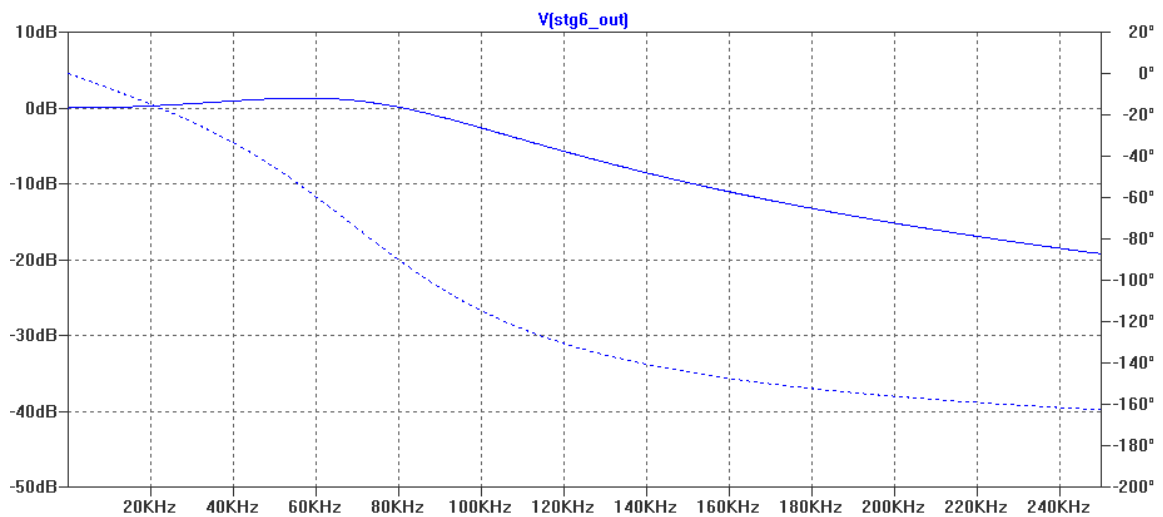
Figure C-9: STF6 Frequency Response

C.6   OpAmp STG7 Design
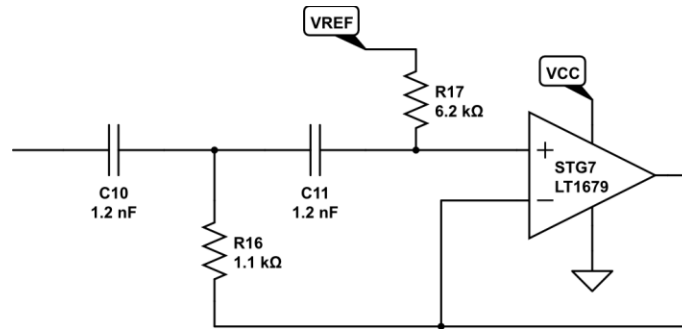
Figure C-10: OpAmp STG7 Filter

$$Transfer\ Function: G(s) = \frac{s^2}{s^2 + 268817s + 101824698599}$$

Cut-Off Frequency: 50786 Hz

Quality Factor: Q=1.19

Damping Ratio: ζ=0.421

Oscillation Frequency: 46061 Hz
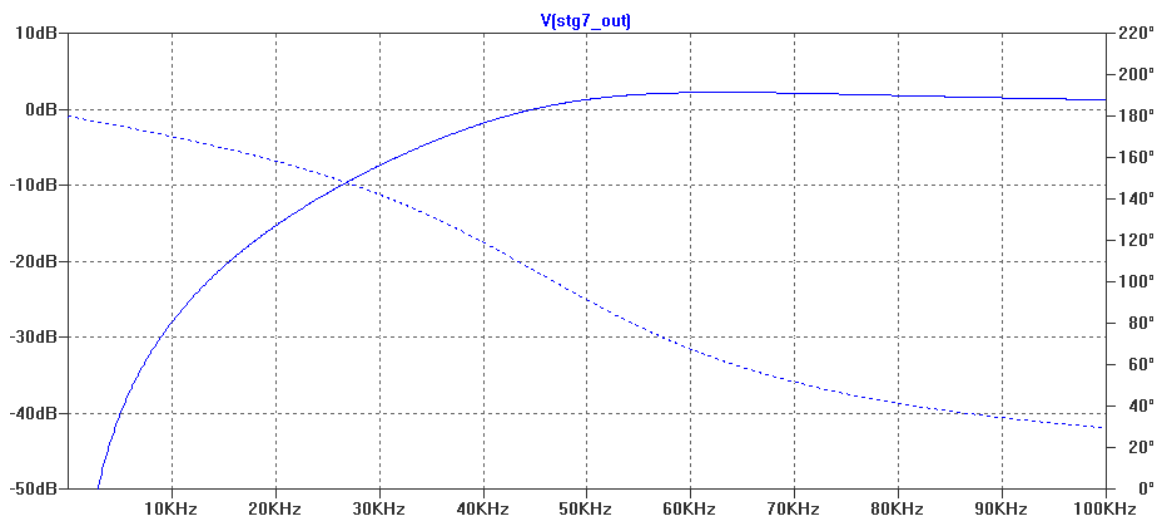
Figure C-11: STG7 Frequency Response

C.7 OpAmp STG8 Design
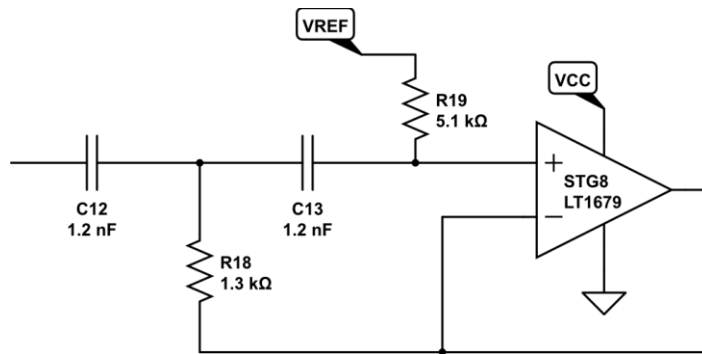
Figure C-12: OpAmp STG8 Filter

$$Transfer\ Function\text{:}\ G(s) = \frac{s^2}{s^2 + 326797s + 104742751802}$$

Cut-Off Frequency: 51509 Hz

Quality Factor: Q=0.99

Damping Ratio: ζ=0.505

Oscillation Frequency: 44462 Hz
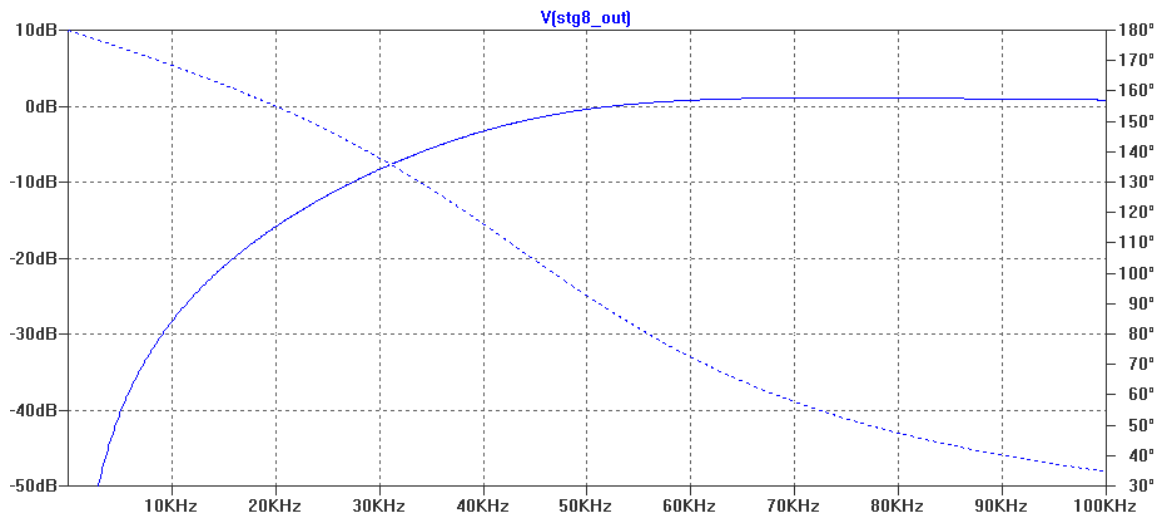
Figure C-13: STG8 Frequency Response

APPENDIX D:
AFCI Spice Simulation
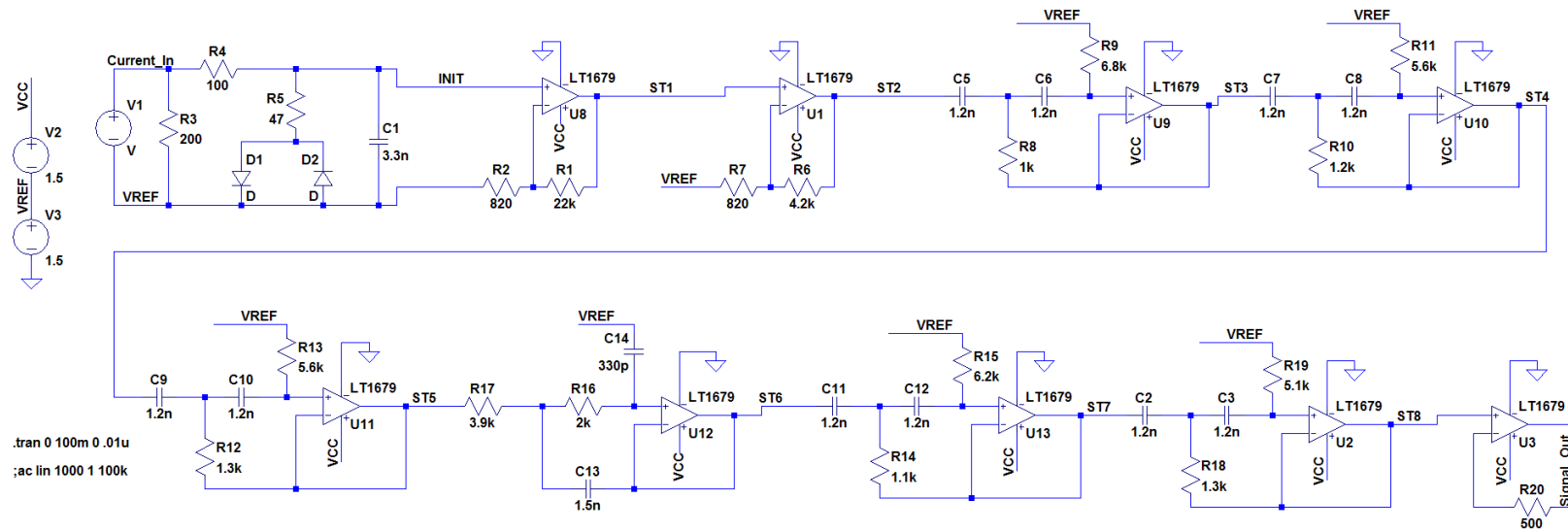
Figure D-1: LTSpice Simulation Schematic

```
* E:\AFCI\FINAL PAPER\Filter New Design 1_25_15\LTOPAMP Design.asc
R1 ST1 N005 22k
R2 N005 VREF 820
R3 Current_In VREF 200
R4 INIT Current_In 100
R5 N007 INIT 47
D1 N007 VREF D
D2 VREF N007 D
C1 INIT VREF 3.3n
C5 N001 ST2 1.2n
C6 N002 N001 1.2n
R8 N001 ST3 1k
R9 VREF N002 6.8k
C7 N003 ST3 1.2n
C8 N004 N003 1.2n
R10 N003 ST4 1.2k
R11 VREF N004 5.6k
C9 N008 ST4 1.2n
C10 N009 N008 1.2n
R12 N008 ST5 1.3k
R13 VREF N009 5.6k
C11 N012 ST6 1.2n
C12 N013 N012 1.2n
R14 N012 ST7 1.1k
R15 VREF N013 6.2k
R16 N011 N010 2k
R17 N010 ST5 3.9k
C13 ST6 N010 1.5n
C14 N011 VREF 330p
XU8 INIT N005 ST1 VCC 0 LT1678
XU9 N002 ST3 ST3 VCC 0 LT1678
XU10 N004 ST4 ST4 VCC 0 LT1678
XU11 N009 ST5 ST5 VCC 0 LT1678
XU12 N011 ST6 ST6 VCC 0 LT1678
XU13 N013 ST7 ST7 VCC 0 LT1678
R6 ST2 N006 4.2k
R7 N006 VREF 820
XU1 ST1 N006 ST2 VCC 0 LT1678
C2 N014 ST7 1.2n
C3 N015 N014 1.2n
R18 N014 ST8 1.3k
R19 VREF N015 5.1k
XU2 N015 ST8 ST8 VCC 0 LT1678
XU3 ST8 N016 Signal_Out VCC 0 LT1678
R20 Signal_Out N016 500
V1 Current_In VREF V
V2 VCC VREF 1.5
V3 VREF 0 1.5
.model D D
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.dio
.tran 0 100m 0 .01u
;ac lin 1000 1 100k
.lib LTC2.LIB
.backanno
.end
```

Figure D-2: Spice Simulation NetList

APPENDIX E:
Smart DC Wall Plug FFT and Arc Analysis Code

```c
/*
* File:   main.c
* Author: Adam Sahr
*
* Created on February 14, 2015, 2:24 PM
*/
/* REV 4
*   STATE: FFT Functionality is operational
*       Logic was added to help prevent false arching trips
*       Logic is located within "check_arching"  function
*       Frequency spectrum average reference bins are created within DMA interrupt
*
*/


#include <stdio.h>
#include <stdint.h>
#include <stdlib.h>
#include <xc.h>
#include <dsp.h>


//CONFIGURATION BITS
// FICD
#pragma config ICS = PGD1            // ICD Communication Channel Select bits (Communicate on PGEC1
and PGED1)
#pragma config JTAGEN = OFF           // JTAG Enable bit (JTAG is enabled)

// FPOR
#pragma config BOREN = ON            // Brown-out Reset (BOR) Detection Enable bit (BOR is enabled)
#pragma config ALTI2C1 = OFF         // Alternate I2C1 pins (I2C1 mapped to SDA1/SCL1 pins)
#pragma config ALTI2C2 = OFF         // Alternate I2C2 pins (I2C2 mapped to SDA2/SCL2 pins)
#pragma config WDTWIN = WIN25         // Watchdog Window Select bits (WDT Window is 25% of
WDT period)

// FWDT
#pragma config WDTPOST = PS32768      // Watchdog Timer Postscaler bits (1:32,768)
#pragma config WDTPRE = PR128        // Watchdog Timer Prescaler bit (1:128)
#pragma config PLLKEN = ON          // PLL Lock Enable bit (Clock switch to PLL source will wait until
the PLL lock signal is valid.)
#pragma config WINDIS = OFF          // Watchdog Timer Window Enable bit (Watchdog Timer in Non-
Window mode)
#pragma config FWDTEN = OFF           // Watchdog Timer Enable bit (Watchdog timer enabled/disabled
by user software)

// FOSC
#pragma config POSCMD = XT           // Primary Oscillator Mode Select bits (XT Crystal Oscillator Mode)
#pragma config OSCIOFNC = OFF         // OSC2 Pin Function bit (OSC2 is clock output)
```

```c
#pragma config IOL1WAY = ON          // Peripheral pin select configuration (Allow only one
reconfiguration)
#pragma config FCKSM = CSDCMD         // Clock Switching Mode bits (Both Clock switching and Fail-
safe Clock Monitor are disabled)

// FOSCSEL
#pragma config FNOSC = PRI            // Oscillator Source Selection (Primary Oscillator (XT, HS, EC))
#pragma config PWMLOCK = ON           // PWM Lock Enable bit (Certain PWM registers may only be
written after key sequence)
#pragma config IESO = OFF             // Two-speed Oscillator Start-up Enable bit (Start up device with
FRC, then switch to user-selected oscillator source)

// FGS
#pragma config GWRP = OFF             // General Segment Write-Protect bit (General Segment may be
written)
#pragma config GCP = OFF              // General Segment Code-Protect bit (General Segment Code protect
is Disabled)


#define Fosc  8000000  //xtal freq
#define Fcy   (Fosc/2)  //instruction freq
#define Fs    250000    //sampling freq up to 330kHz with Fosc = 8MHz
#define SAMPPRD    (Fcy/Fs)-1
#define NUMSAMP    256

#define FFT_BLOCK_LENGTH    256
#define LOG2_BLOCK_LENGTH    8

#define LED     LATGbits.LATG10
#define BASELINE_OFFSET    20

/*used for determining existence of arching in correct shape*/
#define BIN_A   40     //Starting FFT bin of Bin A average
#define BIN_B   60     //Starting FFT bin of Bin B average
#define BIN_C   80     //Starting FFT bin of Bin C average


fractcomplex FFTinput[FFT_BLOCK_LENGTH] __attribute__ ((eds, space(ymemory),aligned
(FFT_BLOCK_LENGTH * 2 * 2)));
fractional bufferA[NUMSAMP] __attribute__((space(xmemory),far,aligned(NUMSAMP)));
fractional bufferB[NUMSAMP] __attribute__((space(xmemory),far,aligned(NUMSAMP)));


fractcomplex twiddleFactors[FFT_BLOCK_LENGTH/2] __attribute__ ((section (".xbss, bss,
xmemory"),far, aligned (FFT_BLOCK_LENGTH*2))); //allocates memory for FFT Twiddle Factors
unsigned int dmaBuffer __attribute__((space(xmemory),near,aligned)) = 0;;
unsigned int i __attribute__((space(xmemory),near,aligned)) = 0;
fractional output[FFT_BLOCK_LENGTH/2];

fractional sig_baseline;  // safe signal baseline with which to compare and determine arching
float sig_bl_float = 0;   // safe signal baseline with which to compare and determine arching intermediate float
value
float sig_baseline_set[4] = {0}; //array to assist the setup of a good baseline
uint16_t count = 0;              //general use counter
```

```c
uint8_t baseline_counter  = 0;      //counter used in set_arch_baseline
uint8_t arching_flag = 0;          //flag to indicate an arch has occurred/is occurring
float freq_bins_avg_f[3] = {0};        //array to hold the averages of specified frequency bins for arch checking;
Float Value
fractional freq_bins_avg[3] = {0};   //array to hold the averages of specified frequency bins for arch checking;
Fract Value
uint8_t arching_counter  = 0;        //counter to indicate continuous arching; helps prevent false trips
uint16_t loop_count = 0;          //counter within DMA interrupt
uint16_t incorrect_shape_counter  = {0};   //counter to count up when the frequency shape is not correct



/* Function Declaration */
void PORT_init(void);
void ADC_init (void);
void TIMER3_init(void);
void DMA_init (void);
void set_arch_baseline(void);
void check_arching(void);


/************************************
* INPUT: N/A
* FUNCTION: Initializes Port I/O settings
* OUTPUT: N/A
************************************/
void PORT_init(void) {
    ANSELA = 0;
    ANSELGbits.ANSG15 = 1;     //configure analog pins
    TRISA = 0x0000;           //configure digital pins
    TRISB = 0x0000;
    TRISC = 0b0000000000000000;
    TRISD = 0b0000000000000000;
    TRISE = 0b0000000000000000;
    TRISF = 0b0000000000000000;
    TRISG = 0b1000000000000000;
}

/************************************
* INPUT: N/A
* FUNCTION: Initializes ADC settings
* OUTPUT: N/A
************************************/
void ADC_init (void) {
    //ADC2 Setup (Current Sense)
    AD2CON1bits.FORM   = 3; // Data Output Format: Signed Fraction (Q15 format)
    AD2CON1bits.SSRC   = 2; // Sample Clock Source: GP Timer 3 starts conversion
    AD2CON1bits.ASAM   = 1; // ADC Sample Control: Sampling begins immediately after conversion
    AD2CON1bits.AD12B  = 0; // 10-bit ADC operation

    AD2CON2bits.CHPS   = 0; // Converts CH0

    AD2CON3bits.ADRC  = 0;  // ADC Clock is derived from Systems Clock
    AD2CON3bits.ADCS  = 0;  // ADC Conversion Clock Tad=Tcy*(ADCS+1)= (1/Fcy)*1 = 250ns
```
103

```
                     // ADC Conversion Time for 10-bit Tc=12*Tad = 3us


   AD2CON1bits.ADDMABM  = 1;  // DMA buffers are built in conversion order mode
   AD2CON2bits.SMPI     = 0; // SMPI must be 0
   AD2CON4bits.ADDMAEN  = 1;  // all results written in ADC1BUF0

   //AD2CHS0: A/D Input Select Register
   AD2CHS0bits.CH0SA= 23; // MUXA +ve input selection (AN20) for CH0 CHANGE THIS FOR
DIFFERNT ANALOG INPUT
   AD2CHS0bits.CH0NA=0;  // MUXA -ve input selection (Vref-) for CH0

   IFS1bits.AD2IF = 0;  // Clear the A/D interrupt flag bit
   IEC1bits.AD2IE = 0;  // Do Not Enable A/D interrupt
   AD2CON1bits.ADON  = 1; // Turn on the A/D converter



}

/***********************************
 * INPUT: N/A
 * FUNCTION: Initializes Timer settings
 * OUTPUT: N/A
 ************************************/
void TIMER3_init(void) {
   TMR3 = 0x0000;
   PR3 = SAMPPRD;
   IFS0bits.T3IF = 0;
   IEC0bits.T3IE = 0;

   //Start Timer 3
   T3CONbits.TON = 1;
}

/***********************************
 * INPUT: N/A
 * FUNCTION: Initializes Direct Memory Allocation (DMA) settings
 * OUTPUT: N/A
 ************************************/
void DMA_init (void) {
   DMA0CONbits.AMODE = 0;  // Configure DMA for Register indirect with post increment
   DMA0CONbits.MODE  = 2;  // Configure DMA for Continuous Ping-Pong mode

   DMA0PAD=(int)&ADC2BUF0; //static address of the peripheral data register (i.e. ADC2)
   DMA0CNT=(NUMSAMP-1);     //number of DMA data requests before storage

   DMA0REQ=21; //DMA communicating with ADC2 peripheral

   DMA0STAL = (unsigned int)&bufferA; //assigns DMA to pull from ADC Buffers
   DMA0STAH = (unsigned int)&bufferA;

   DMA0STBL = (unsigned int)&bufferB;
   DMA0STBH =(unsigned int)&bufferB;
```

```c
    IFS0bits.DMA0IF = 0;   //Clear the DMA interrupt flag bit
    IEC0bits.DMA0IE = 1;   //Set the DMA interrupt enable bit

    DMA0CONbits.CHEN=1;//channel is enabled

    TRISBbits.TRISB1 = 0;
}

/**************************************
 * INPUT: N/A
 * FUNCTION: DMA Interrupt Routine; Performs FFT
 * OUTPUT: N/A
 **************************************/
void __attribute__((interrupt, no_auto_psv)) _DMA0Interrupt(void) {
T3CONbits.TON = 0;              /*needed number of samples reached, stop sampling and perform FFT*/
if(dmaBuffer == 0)
{
    for ( i = 0; i < FFT_BLOCK_LENGTH-1; i++ ) {/* The FFT function requires input data to be in the
fractional fixed-point range [-0.5, +0.5]*/
        FFTinput[i].real = bufferA[i] >> 1;    /* So, we shift all data samples by 1 bit to the right. */
        FFTinput[i].imag = 0;
    }

    FFTComplexIP(LOG2_BLOCK_LENGTH, FFTinput, &twiddleFactors[0], COEFFS_IN_DATA); //
FFT on bufferA

}
else
{
    for ( i = 0; i < FFT_BLOCK_LENGTH-1; i++ ) {/* The FFT function requires input data to be in the
fractional fixed-point range [-0.5, +0.5] */
        FFTinput[i].real = bufferB[i] >> 1;    /* So, we shift all data samples by 1 bit to the right. */
        FFTinput[i].imag = 0;
    }
    FFTComplexIP(LOG2_BLOCK_LENGTH, FFTinput, &twiddleFactors[0], COEFFS_IN_DATA); //
FFT on bufferB
}
dmaBuffer ^= 1;   //toggle dmaBuffer
    BitReverseComplex(LOG2_BLOCK_LENGTH, FFTinput); // Store output samples in bit-reversed order
of their addresses

    SquareMagnitudeCplx(FFT_BLOCK_LENGTH/2, FFTinput, output);// Compute the square magnitude
of the complex FFT output array so we have a Real output vetor

if(count < 16) {    //the first 16 FFT samples will set the arching baseline
    count++;
    set_arch_baseline();
} else {  //once the baseline has been set, create frequency bins to determine the existence of arching each
time an FFT is performed
    for (loop_count = 0; loop_count < 10; loop_count++) {
        freq_bins_avg_f[0] += Fract2Float(output[BIN_A + loop_count]);   //Sums bins 39kHz ->
47.8kHz [bin 40-49]
```

```c
        freq_bins_avg_f[1] += Fract2Float(output[BIN_B + loop_count]);   //Sums bins 58.6kHz ->
67.4kHz [bin 60-69]
        freq_bins_avg_f[2] += Fract2Float(output[BIN_C + loop_count]);   //Sums bins 78.1kHz ->
86.9kHz [bin 80-89]
    }
    freq_bins_avg_f[0] = freq_bins_avg_f[0]/10;    //Obtains average of bins 39kHz -> 47.8kHz; float
    freq_bins_avg_f[1] = freq_bins_avg_f[1]/10;    //Obtains average of bins 58.6kHz -> 67.4kHz; float
    freq_bins_avg_f[2] = freq_bins_avg_f[2]/10;    //Obtains average of bins 78.1kHz -> 86.9kHz; float

    freq_bins_avg[0] = Float2Fract(freq_bins_avg_f[0]/10);     //Obtains average of bins 39kHz ->
47.8kHz; fractional
    freq_bins_avg[1] = Float2Fract(freq_bins_avg_f[1]/10);     //Obtains average of bins 58.6kHz ->
67.4kHz; fractional
    freq_bins_avg[2] = Float2Fract(freq_bins_avg_f[2]/10);     //Obtains average of bins 78.1kHz ->
86.9kHz; fractional
}
T3CONbits.TON = 1;            /*FFT complete, resume sampling*/
_DMA0IF = 0;  //Clear the DMA0 Interrupt Flag

}

/***********************************
* INPUT: N/A
* FUNCTION: Routine to set an arching baseline based on the average of startup low freq FFT values
* OUTPUT: N/A
***********************************/
void set_arch_baseline(void) {
   /*sums the contents of 4 freq bins a set number of times into sig_baseline_set[] array*/
   sig_baseline_set[0] += Fract2Float(output[13]);  //~12.7kHz
   sig_baseline_set[1] += Fract2Float(output[14]);
   sig_baseline_set[2] += Fract2Float(output[15]);
   sig_baseline_set[3] += Fract2Float(output[17]);  //~16.6kHz
   if (count == 16) { //when the set number of sum iterations has been reached
       for (baseline_counter = 0; baseline_counter < 4; baseline_counter++) { //take the average of each
sig_baseline_set[] array bin
          sig_baseline_set[baseline_counter] = sig_baseline_set[baseline_counter]/16;
       }
       sig_bl_float = ((sig_baseline_set[0] + sig_baseline_set[1] + sig_baseline_set[2] +
sig_baseline_set[3])/4) + BASELINE_OFFSET;  //averages the contents of sig_baseline_set[] and
                                                               //adds an offset to the value.
       sig_baseline = Float2Fract(sig_baseline);  //converts the working baseline from float back to fract to be
usable for comparison
   }
}

/***********************************
* INPUT: N/A
* FUNCTION: Routine to check if arching is occurring;
*        arching_counter will increment when the correct frequency spectrum shape is achieved;
*        incorrect_shape_counter will increment when freq_bin_avg is above the baseline, but the spectrum is
not the correct shape;
*        if the incorrect_shape_counter reaches 10, it resets the arching_counter
*        if arching_counter reaches 10, arching_flag is set
* OUTPUT: N/A
```

```c
 **************************************/
void check_arching(void) {
   if((freq_bins_avg[0] > sig_baseline) && (freq_bins_avg[1] > sig_baseline) && (freq_bins_avg[2] >
sig_baseline)) { //if each is greater than signal baseline
        if((freq_bins_avg[0] < freq_bins_avg[1]) && (freq_bins_avg[2] < freq_bins_avg[1])) { //if the middle
bin is higher than the two side bins
           arching_counter++;
           incorrect_shape_counter = 0;
           arching_flag = 1;   //flag to indicate arch has occurred/is occurring
        } else {
           incorrect_shape_counter++;
        }
   } else {
      arching_counter = 0;
   }
   if ((arching_flag == 1) && (arching_counter == 0)) {
      arching_flag = 0;
   }
   if(arching_counter >= 10) {
      arching_counter = 11;   //keeps arching_counter from incrementing indefinitely when program is
running
      arching_flag = 1;       //set flag, indicating arching
   } else if (incorrect_shape_counter >= 10) {
      arching_counter = 0;
      incorrect_shape_counter = 0;
   }
   if(arching_flag == 1) { //if arching has occurred
      LED = 1;   //turn on LED
   } else {
      LED = 0;   //turn off LED
   }
}


/***************************/
int main() {
   PORT_init();          //Initialize I/O ports
   TwidFactorInit (LOG2_BLOCK_LENGTH, &twiddleFactors[0], 0);  /* Sets up twiddle factors; done
once at startup */
   ADC_init();           //Initialize ADC
   DMA_init();           //Initialize Direct Memory Allocation
   TIMER3_init();        //Initialize Timer3 to control FFT ADC
   while (count < 16);   //wait for baseline to be set sets baseline by which to compare arching
   while(1) {
      check_arching();   //call function to check arching
   }
}
```

APPENDIX F:
Glossary

Term	Definition
ADC	Analog-to-Digital Converter
AFCI	Arc Fault Circuit Interrupter
Arc Fault	A high power discharge of electricity between two conductors. This discharge can possibly trigger an electrical fire.
DC	Direct current – unidirectional flow of electrical charge
FFT	Fast Fourier Transform – an algorithm used to compute the discrete Fourier Transform of a time signal
GFCI	Ground Fault Circuit Interrupter
LTSpice	A freeware Spice simulator created by Linear Technology
NEC	National Electrical Code – a common electrical code used throughout the U.S.
OpAmp	Operational Amplifier – differential input, single ended output amplifier
PCB	Printed Circuit Board
PV	Photovoltaic – generating electricity directly from sunlight
Smart Wall Plug	A household outlet designed by Cal Poly for an all direct current household. It automatically adjusts the output voltage based on whatever load/appliance is plugged in.
Spice	Simulation program with integrated circuit emphasis
UL	Underwriters Laboratories