EE 462-01
Electrical Engineering Department

Senior Project

RF Power Harvesting Rectenna

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Abstract

Sustainability is one of today's primary engineering objectives. This principle involves system design that minimizes environmentally harmful energy emissions and resource consumption, and maximizes renewable energy practices [1]. Communication antennas transmit wireless signals that can be converted into usable energy. The Rectenna system described in this report, shown in Figure 1, was designed to accomplish this energy conversion, with -5dBm (316μW) minimum power at the rectifier input. Since typical ambient signal power is in the -70dBm (0.1nW) range, the proposed system could only convert passive, relatively high-power microwave band AC signals to DC. The Rectenna system was designed for 1.9GHz signal reception; however, the greatest ambient 1.9GHz signal power measured in Cal Poly's Microwave Lab was in the -75dBm (31pW) to -70dBm (100pW) range, shown in Table 1. The team provided an external 1.9GHz source (-20dBm to 3dBm) to verify the design.

An inset-fed microstrip patch is used as an energy harvesting antenna; the single patch was then arrayed into a 2x2 planar configuration. The designed patch antenna array has a 3dB larger gain, and 1% increased frequency bandwidth compared to the single patch. However, it is unable to harvest sufficient RF power for energy storage. When capturing multiple-source ambient RF signals, an omnidirectional antenna (captures energy in all directions) should be implemented, rather than a directional patch antenna array.

The Greinacher rectifier [2] converts RF energy into usable DC power which is multiple times the input RF peak voltage. Simulations show the Greinacher rectifier output voltage is a function of the number of stages and peak input voltage. The antenna and rectifier are matched with $|S_{11}|$ less than -21dB and -5dB, respectively, at 1.9GHz to mitigate power losses. A high-efficiency Main Boost Converter (BQ25504) increases rectifier output DC voltage to 3.1V for charge storage on a capacitor (battery). A Self-Oscillating Boost Converter (SOBC) handles startup when the capacitor is initially discharged. A passive switching circuit was developed to enable source-free switching from the SOBC to the Main Boost Converter. The system yields 29% and 12% maximum power efficiency with -1dBm (794μW) and -5dBm (316μW) input power to the rectifier, respectively.

Table 1: Ambient RF Signal Sample, [February 2016]

Measured Frequency (MHz)	Measured Power Level (dBm)
480	-72
756	-79
950	-77
1900	-71

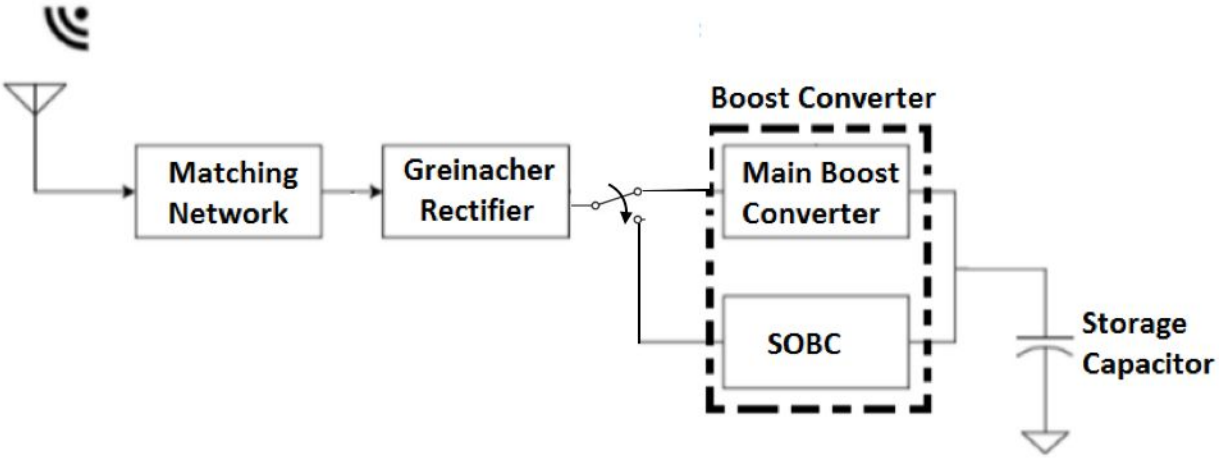


Figure 1: Rectenna Block Diagram

Antenna Design, Analysis, and Test

The patch antenna has a low profile, simple design, and straightforward manufacturing. The antenna was designed in High Frequency Structure Simulator (HFSS) [3] and fabricated using Cal Poly's Protomat S62 precision mill [4]. The specifications include 5dB gain, VSWR less than 2, and 1% minimum frequency bandwidth.

The board was milled on 30 mil height Rogers RO3035 Duroid with a 3.5 dielectric constant [5]. The patch is inset-fed to allow input impedance tuning via x_0, y_0 dimensions (see Fig. 2), and feed length parameters. Single patch dimensions were calculated using the following relations [6].

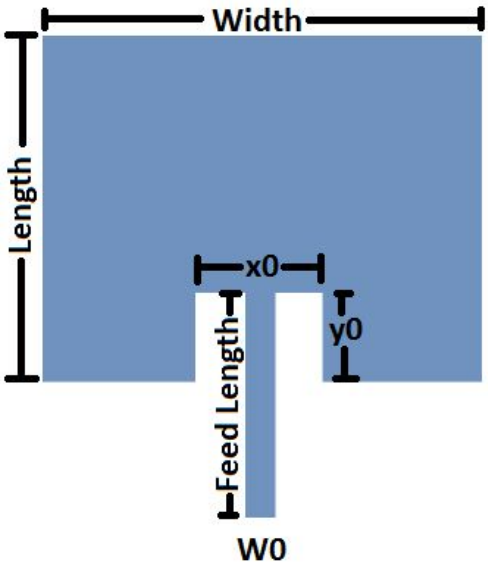


Figure 2: Inset-Fed Patch Antenna

$$Width = \frac{c}{2*f_r}\sqrt{\frac{2}{\varepsilon_r+1}} \quad (1)$$

$$Length = 0.412 * h * \frac{(\varepsilon_{r(eff)}+0.3)(\frac{W}{h}+0.264)}{(\varepsilon_{r(eff)}-0.258)(\frac{W}{h}+0.8)} \quad (2)$$

$$\varepsilon_{r(eff)} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1 + 12\frac{h}{W}\right)^{-1/2} \quad (3)$$

The initial antenna was designed for 1.9GHz operation. The x_0, y_0, and feed length dimensions were tuned in HFSS to control the antenna input impedance for impedance matching. HFSS allows patch antenna parameter optimization and tuning to meet required specifications. "Tuning" refers to controlling individual patch dimensions until the desired antenna parameters are obtained. For example, the patch length was extended to minimize $|S_{11}|$ at 1.9GHz in Figure 3. Increasing the patch length decreases the resonant frequency. Using equations 1-3, the calculated antenna parameters are shown in Table 2.

Table 2: Calculated Patch Antenna Parameter Values

Width, W (mils)	Length, L (mils)	Feed Length, L_F (mils)	$\varepsilon_{r(eff)}$
2072.11	1646.53	28.78	3.32

A single inset-fed patch model was created in HFSS; HFSS optimetrics was used to minimize antenna $|S_{11}|$ in Figure 3. HFSS optimized antenna dimensions using a quasi-Newton method. The simulated -10dB bandwidth is 23MHz (1.2%).

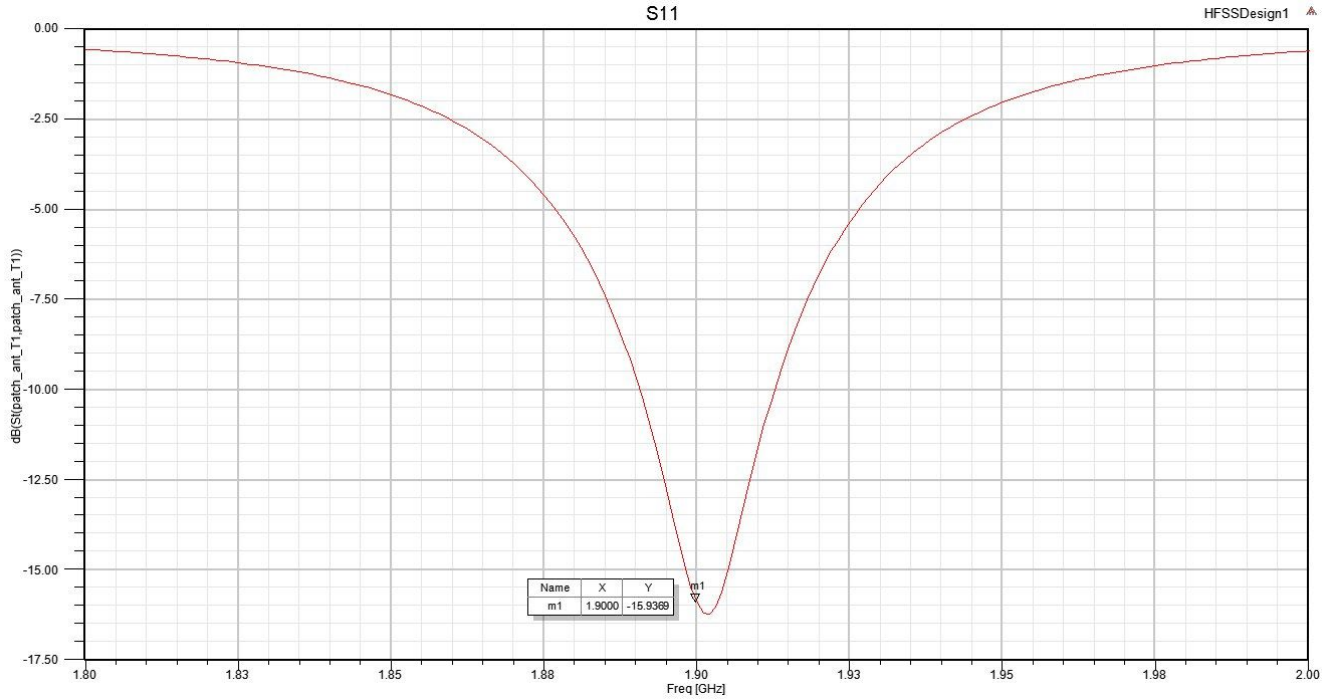


Figure 3: Single Patch Simulated $|S_{11}|$ (dB) vs. Frequency (GHz)

The optimized patch 3D polar gain plot appears in Figure 4; the theta sweep E-plane co-pol radiation pattern appears in Figure 5.

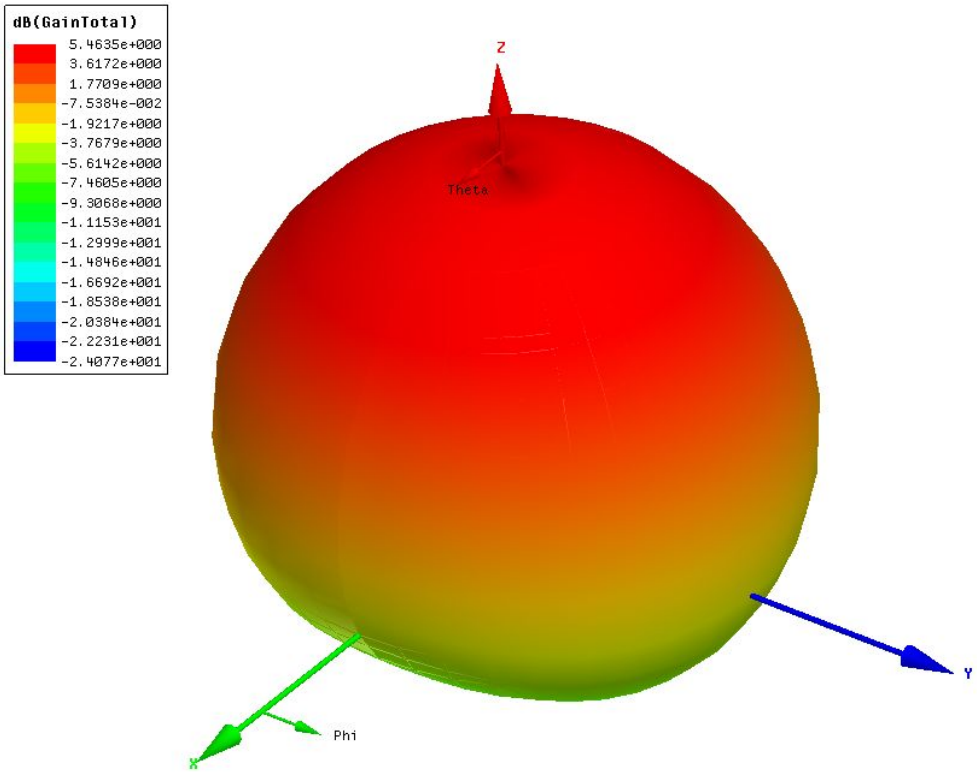


Figure 4: Single Patch 3D Polar Gain Plot (Z-Axis Normal to Patch)

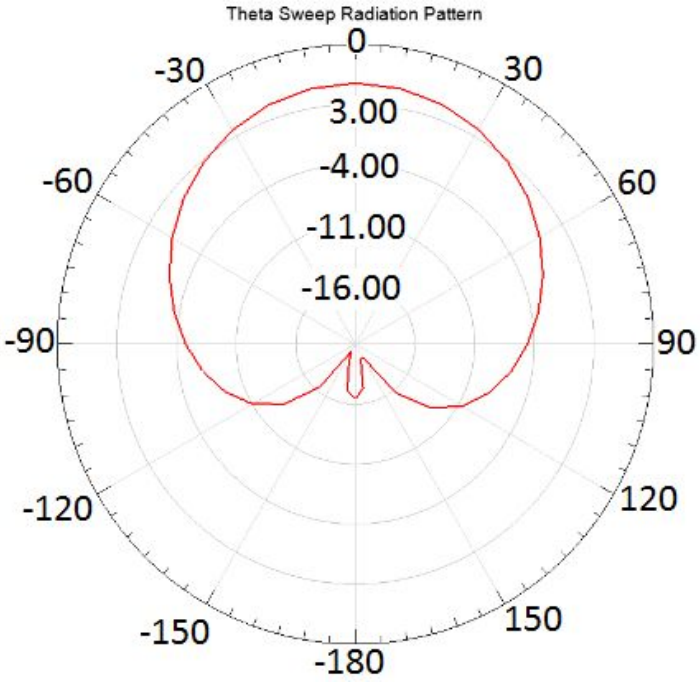


Figure 5: Single Patch Theta Sweep Radiation Pattern (dB), Phi = 0°, f = 1.9GHz (E-Plane, Co-Polarized)

The optimized patch model in HFSS appears in Figure 6.

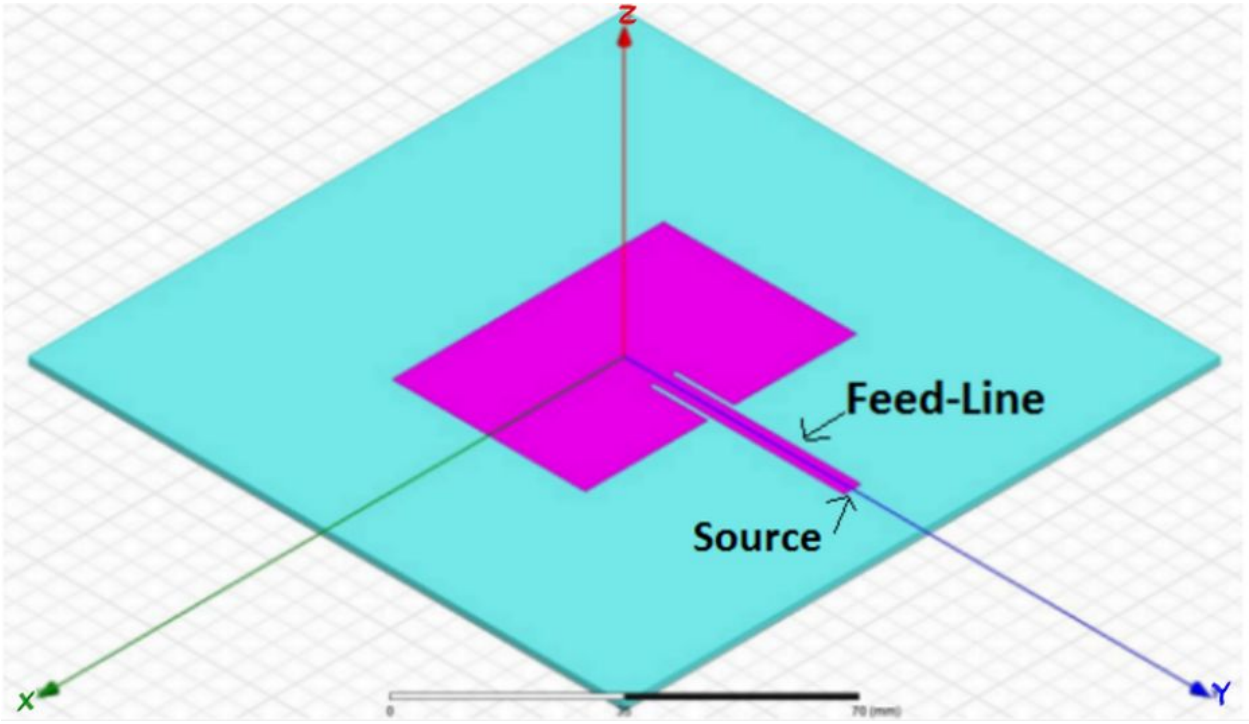


Figure 6: Final Optimized Single Patch

The simulation layout was converted to a Gerber file for fabrication on Cal Poly's milling machine. Figure 7 shows the final manufactured patch.

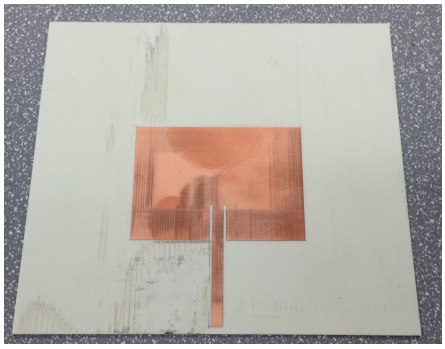


Figure 7: Manufactured Patch Antenna

The antenna's measured $|S_{11}|$ frequency response is shown in Figure 8.

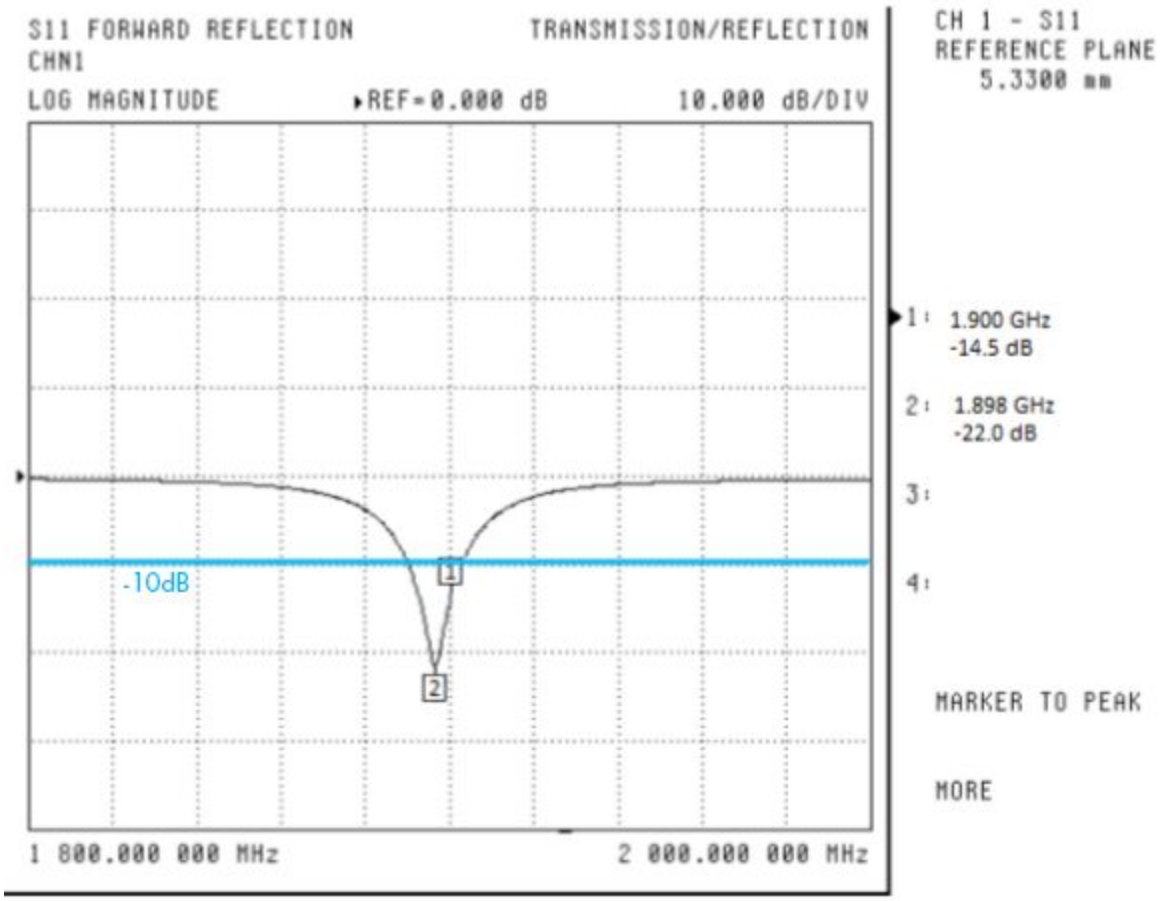


Figure 8: Patch Antenna, Original Design, Measured $|S_{11}|$ vs Frequency

By increasing the patch length, the resonant frequency was tuned to 1.9GHz. Figure 9 shows the tuned patch antenna with hot glue spheres to maintain copper tape position. Figure 10 shows the tuned patch $|S_{11}|$ frequency response with 80MHz (4.2%) -10dB bandwidth.

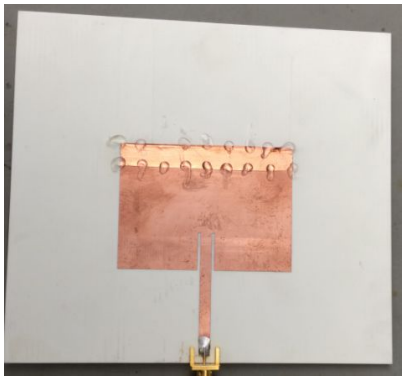


Figure 9: Tuned Patch Antenna

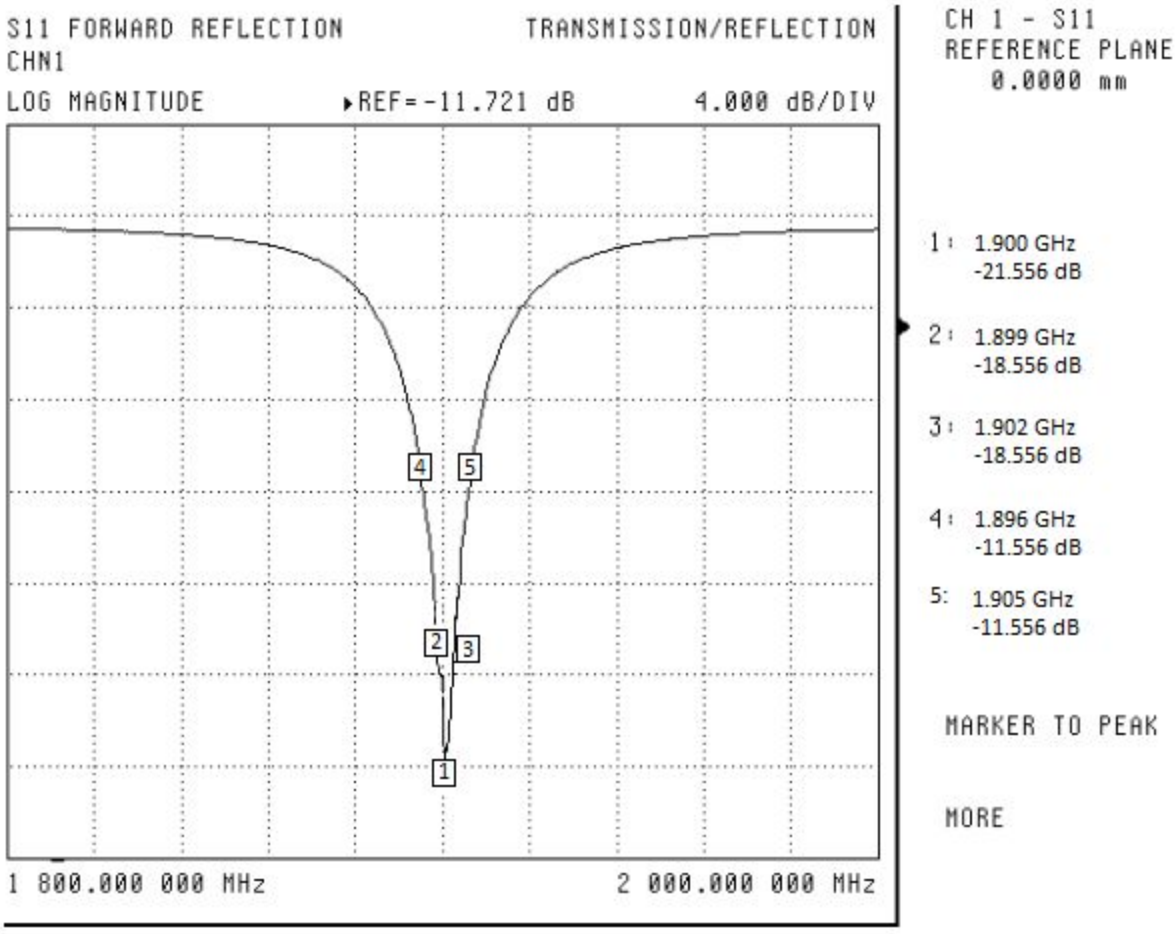


Figure 10: Tuned Patch Antenna Measured $|S_{11}|$ (dB) vs. Frequency (MHz)

The patch antenna was characterized in Cal Poly's anechoic chamber. Patch antenna orientation is shown in Figure 11.

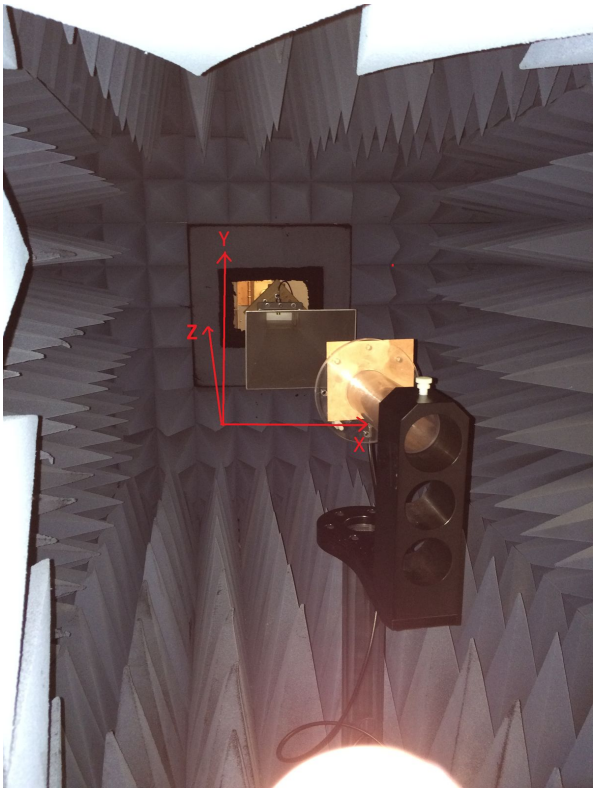


Figure 11: Patch Antenna Orientation and Coordinate System in Cal Poly Anechoic Chamber

The measured radiation patterns are shown in Figure 12. “E co-pol” and “H co-pol” refer to E-plane and H-plane scanning, respectively. Transmit horn and receive patch antenna polarizations are aligned.

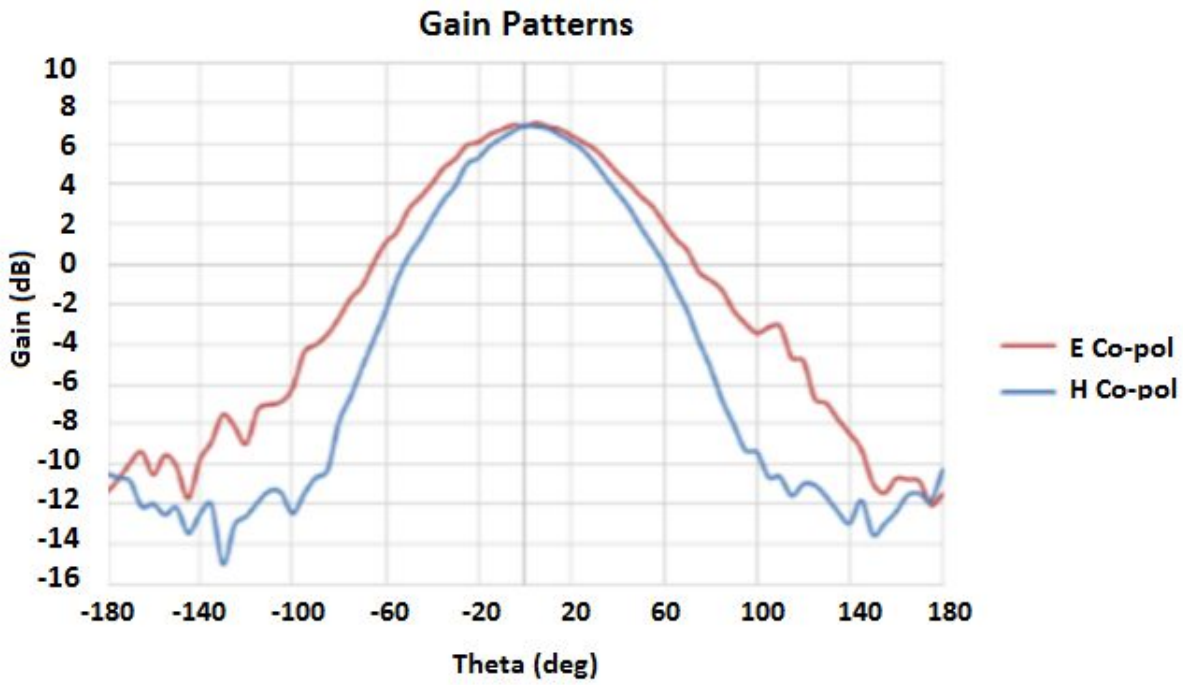


Figure 12: Patch Antenna Gain Measurements

Each pattern's half-power beamwidth (HPBW) is the angular span between half-power angles and around the peak radiation direction. Antenna gain is calculated using (4) where HPBW_E and HPBW_H are the E-plane and H-plane HPBWs in degrees from Figure 12 [6], respectively.

Table 3: Approximate Antenna HPBW Measurements and Gain

Measured $HPBW_E$ (°)	85
Measured $HPBW_H$ (°)	70
Calculated Antenna Gain (dB)	7

$$\text{Antenna Gain} = \frac{41{,}253}{HPBW_E * HPBW_H} \qquad (4)$$

The optimized single patch antenna was duplicated to a 2x2 array for increased gain and comparison to the single patch. Figure 13 shows the initial microstrip inset-fed patch antenna array design. Wilkinson dividers were considered for signal combining; however, board space was exceeded. Instead, traces were combined and optimized in HFSS for 50Ω input impedance. Received signals from each patch antenna must travel identical distances to the detection point for in-phase combining. All patches also required a center-center spacing of a wavelength, and optimal in-phase combining. Figure 14 shows the initial planar array HFSS model.

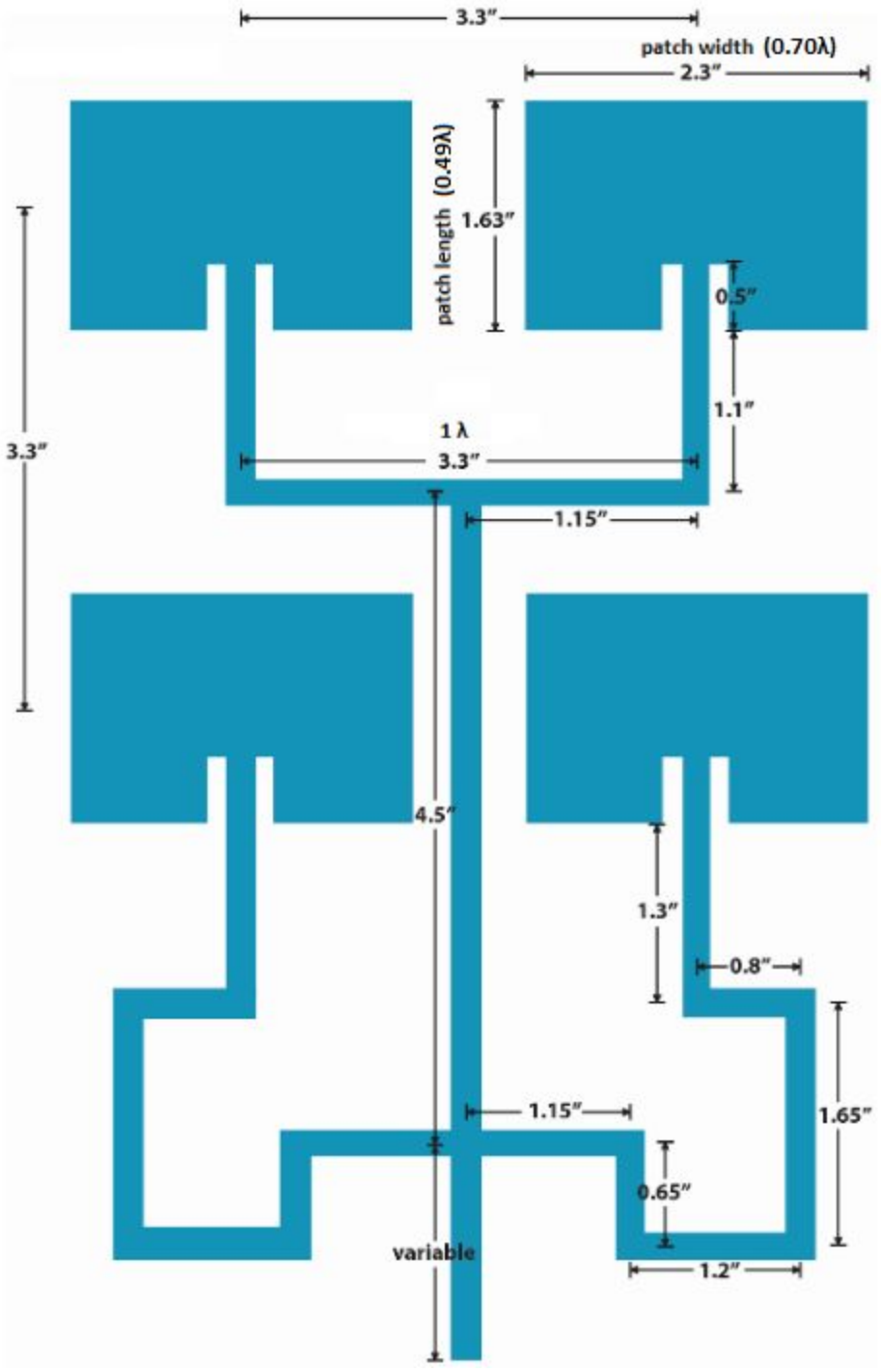


Figure 13: Patch Antenna Planar Array Initial Design

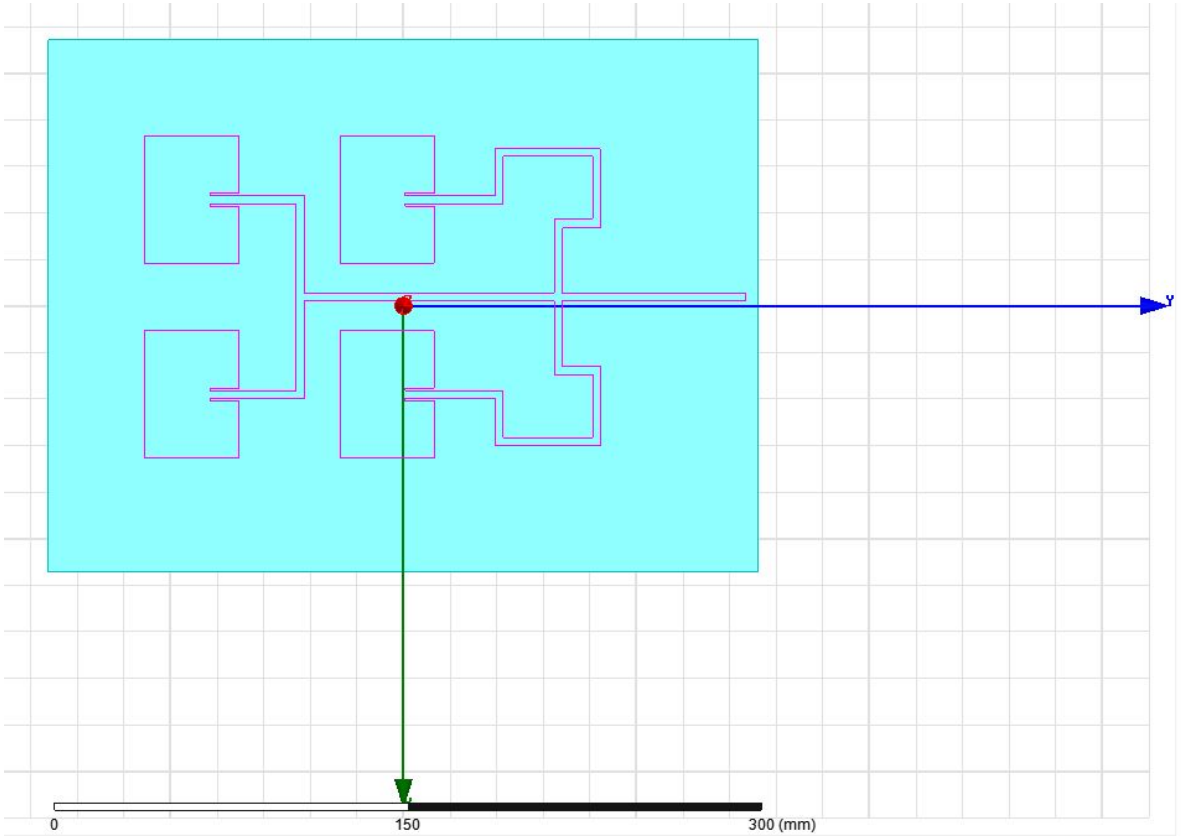


Figure 14: HFSS Patch Antenna Planar Array

This model was simulated in HFSS, and Figures 15 and 16 show the antenna array $|S_{11}|$ and 3D radiation pattern, respectively. The simulated -10dB bandwidth is 20MHz (1.05%).

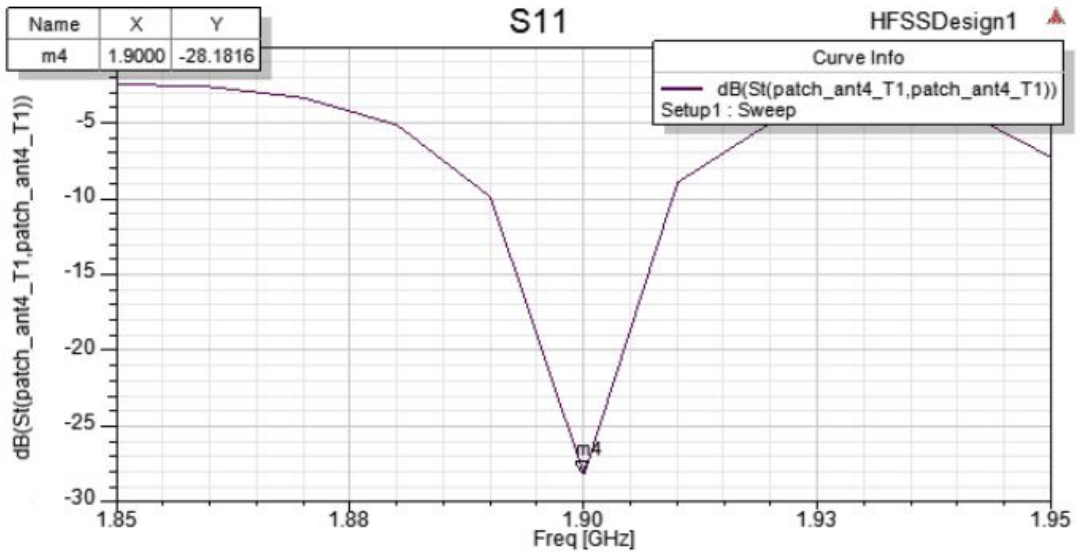


Figure 15: 60mil Dielectric Height Patch Antenna Array Simulated $|S_{11}|$

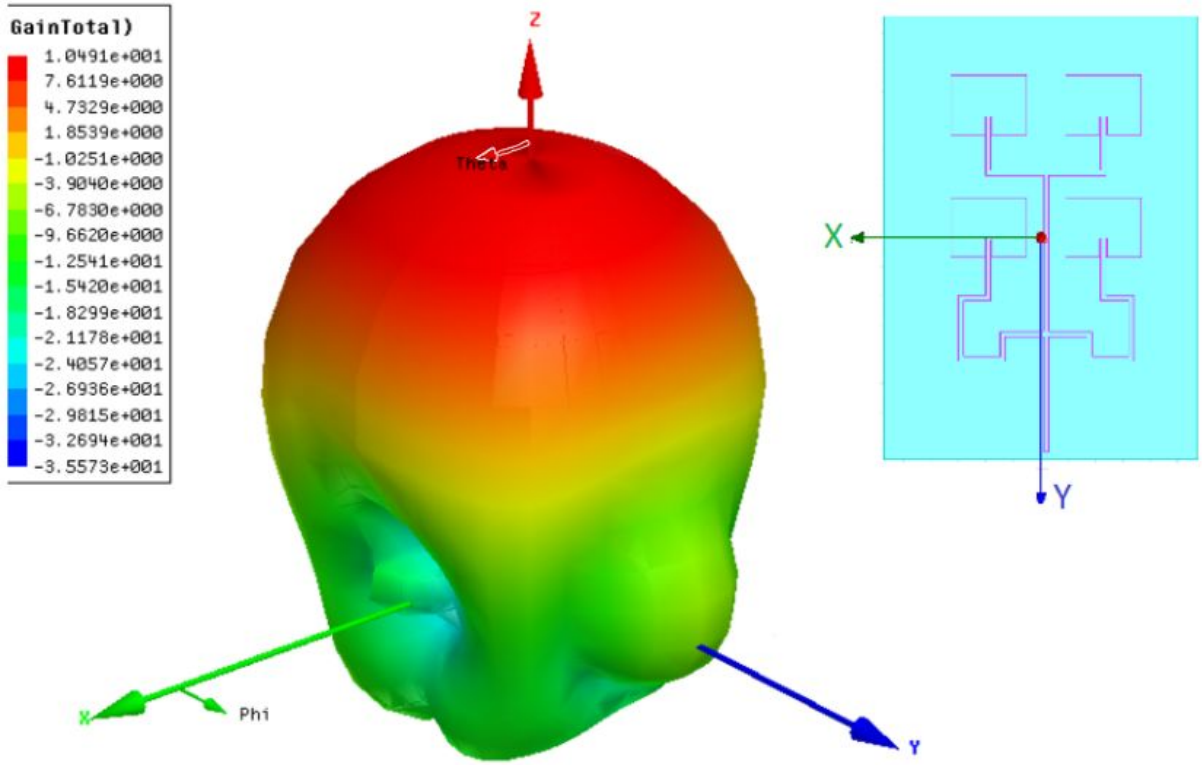


Figure 16: 60mil Dielectric Height Patch Antenna 2x2 Array Simulated 3D Radiation Pattern

The simulation results are summarized in Table 4.

Table 4: Simulated Antenna Array Results @ 1.9GHz

Input Impedance (Ω)	52.0 +j0.3
$\|S_{11}\|$ (dB)	-28.1
VSWR	1.1
Gain (dB)	10.5

The patch array was also simulated on Rogers RO3035 30-mil height dielectric (ε_r = 3.5) for comparison. Figure 17 shows the new simulated 30-mil dielectric height patch antenna array $|S_{11}|$. The -10dB bandwidth is 6MHz (0.3%).

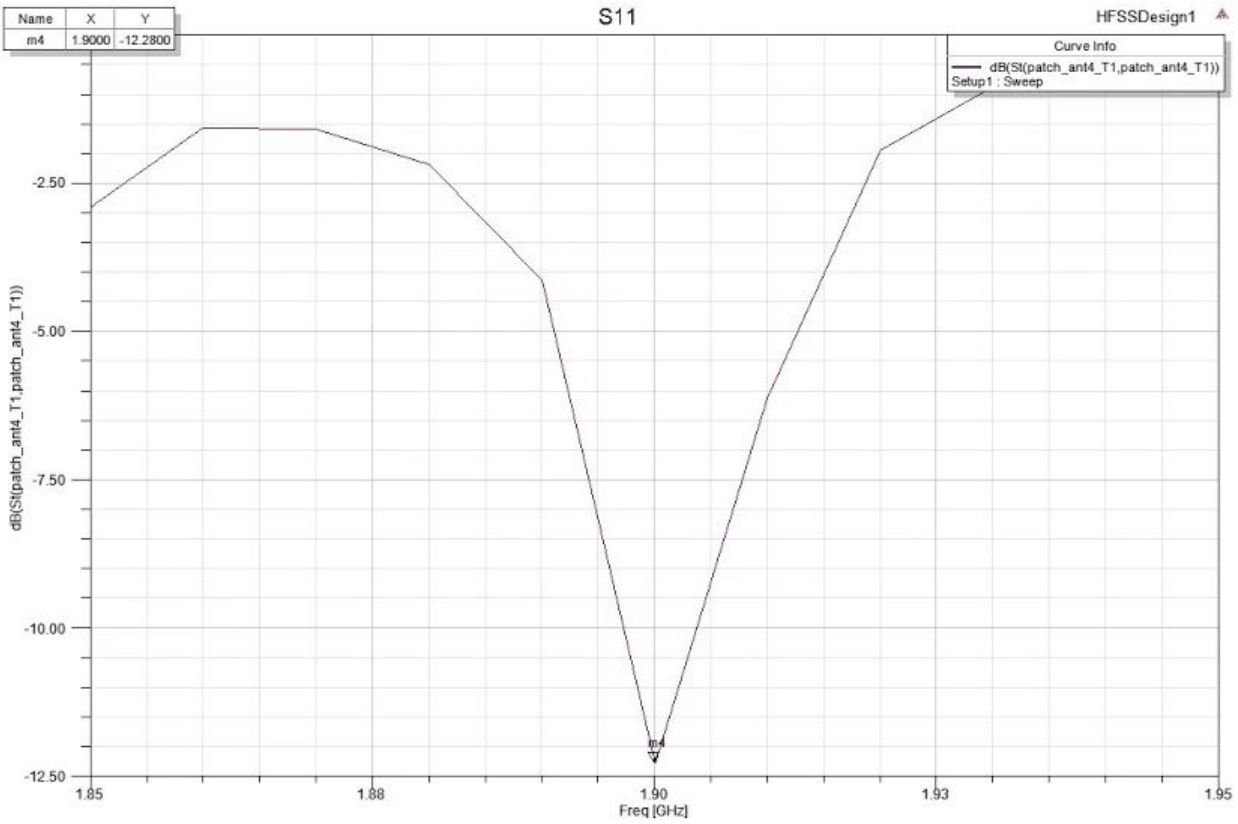


Figure 17: 30mil Dielectric Height Patch Antenna Array Simulated $|S_{11}|$

The 30mil dielectric height array simulation results at 1.9GHz are shown in Table 5.

Table 5: Simulated 30mil Dielectric Height (ε_r = 3.5) Antenna Array Results @ 1.9GHz

Dielectric Height (mils)	**30**	**60**
Input Impedance (Ω)	42.5 + j0.4	52 + j0.1
$\|S_{11}\|$ (dB)	-12.3	-28.0
VSWR	1.64	1.08
Gain (dB)	6.9	10.5

The antenna array was milled on 30mil dielectric height Rogers Duroid 3035 (ε_r = 3.5). The resonant frequency was decreased by increasing all patch lengths, shown in Figure 18. Hot glue spheres maintain copper tape position. Copper tape tuning and Duroid flexibility increases substrate bending sensitivity. Thus, the antenna was re-tuned by applying copper tape only to the feed line, resulting in an antenna less-sensitive to substrate bending in Figure 19. Figure 20 shows the newly tuned $|S_{11}|$. The measured -10dB bandwidth is 100MHz (5.2%).

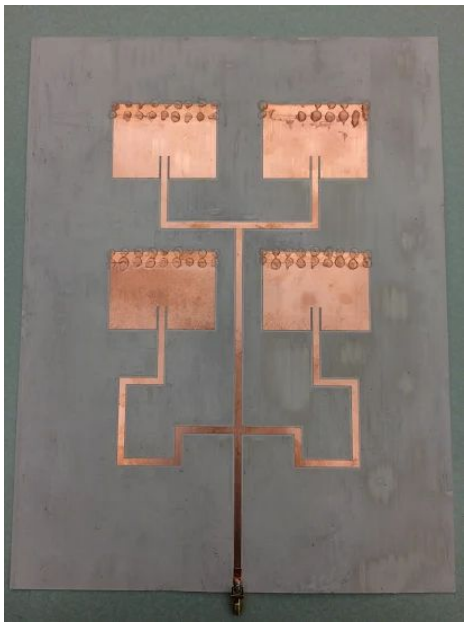


Figure 18: 30mil Dielectric Height Patch Antenna Array Initial Tuning

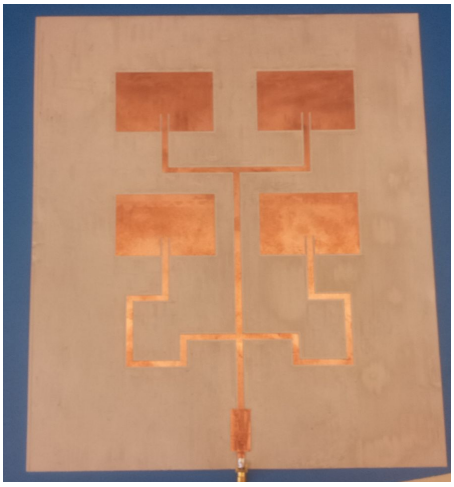


Figure 19: 30mil Dielectric Height Patch Antenna Array Final Tuning

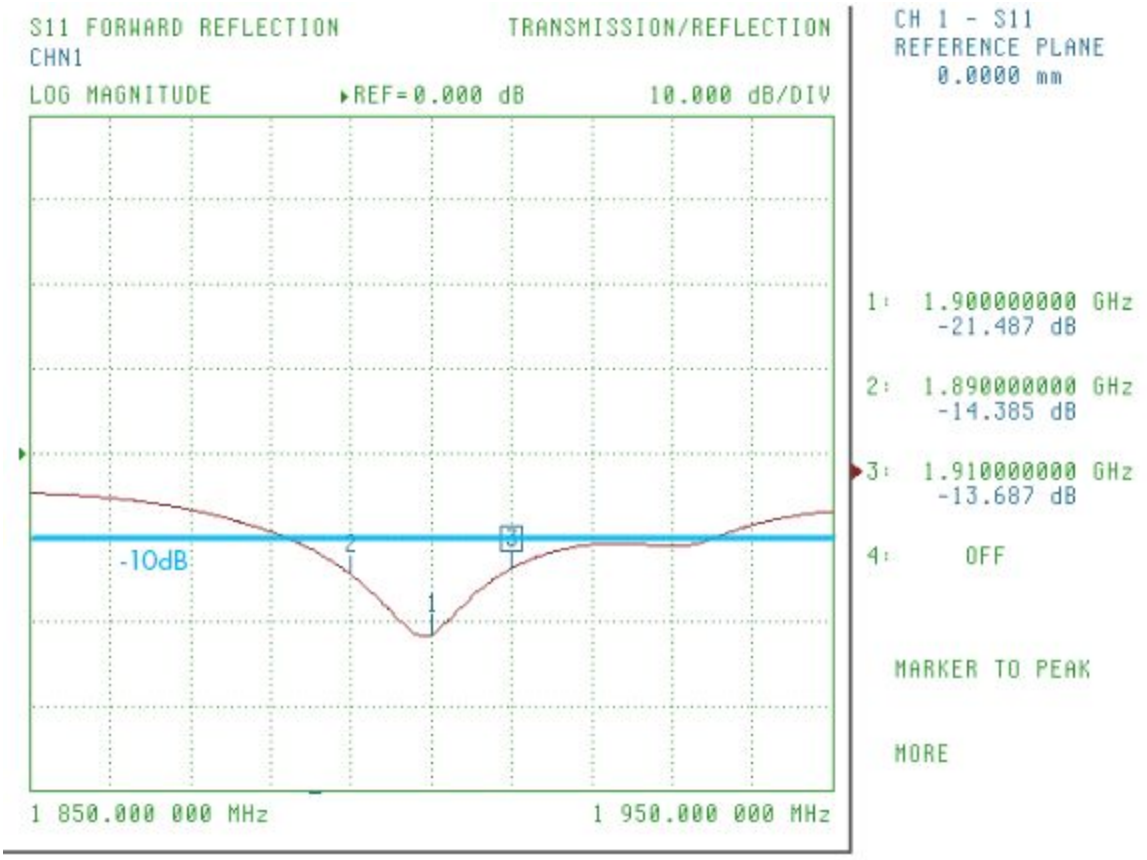


Figure 20: 30mil Dielectric Height Patch Antenna Array Measured $|S_{11}|$

The antenna was characterized in Cal Poly's anechoic chamber. Figures 21-24 show final 30mil dielectric height patch array E- and H-plane, co- and cross-polarized radiation patterns. The E- and H-plane co-polarized main beam peaks are offset due to an alignment issue in the anechoic chamber.

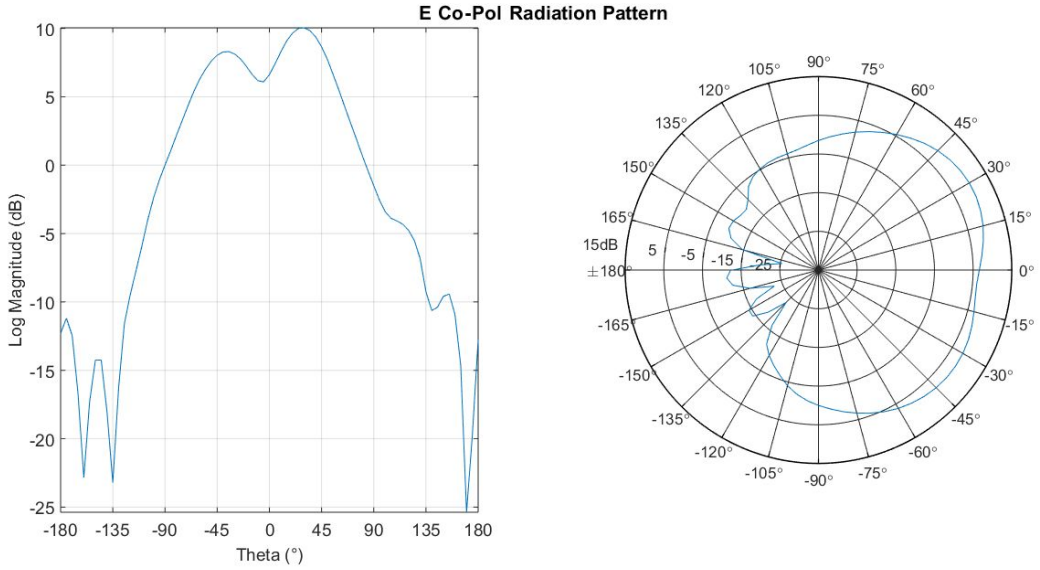


Figure 21: Measured 30mil Dielectric Height Patch Array E-Plane Co-Pol Radiation Pattern

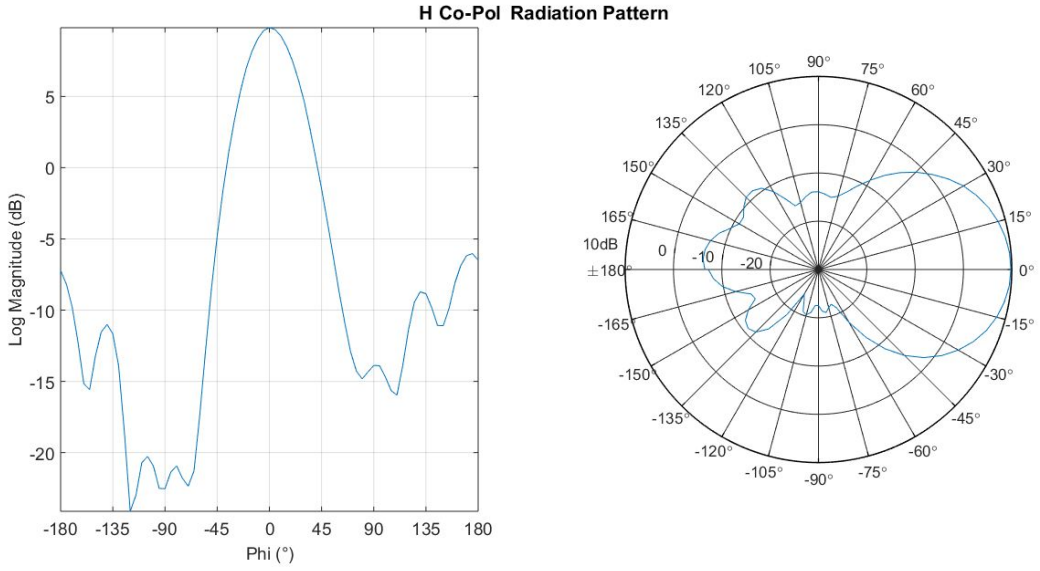


Figure 22: Measured 30mil Dielectric Height Patch Array H-Plane Co-Pol Radiation Pattern

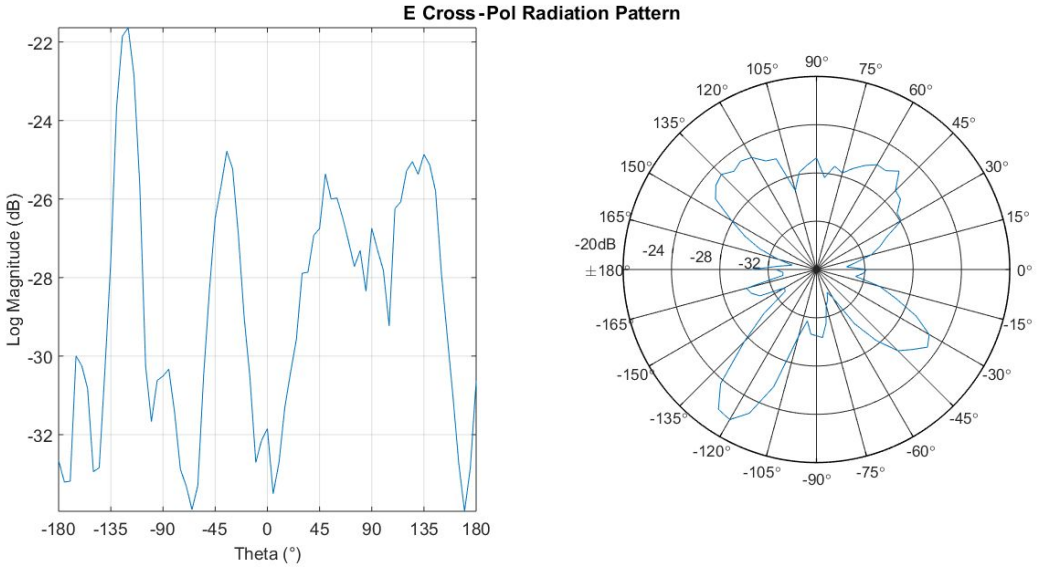


Figure 23: Measured 30mil Dielectric Height Patch Array E-Plane Cross-Pol Radiation Pattern

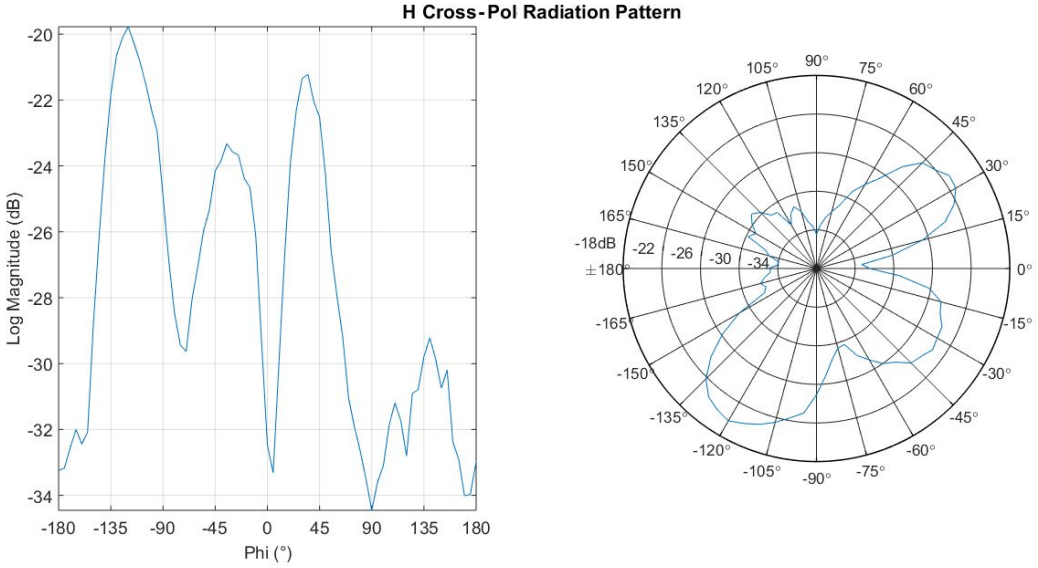


Figure 24: Measured 30mil Dielectric Height Patch Array H-Plane Cross-Pol Radiation Pattern

Rectifier Design, Analysis, and Test

Theory

Rectifiers convert RF power to DC. Single diode and full-wave bridge rectifiers were considered, but the proposed system uses a cascaded Greinacher Rectifier configuration, see Figure 25. Greinacher rectifiers can boost 100mV range input voltages to 200mV or greater by increasing the number of cascaded stages.

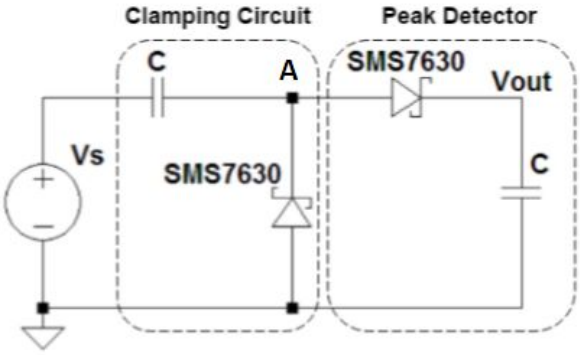
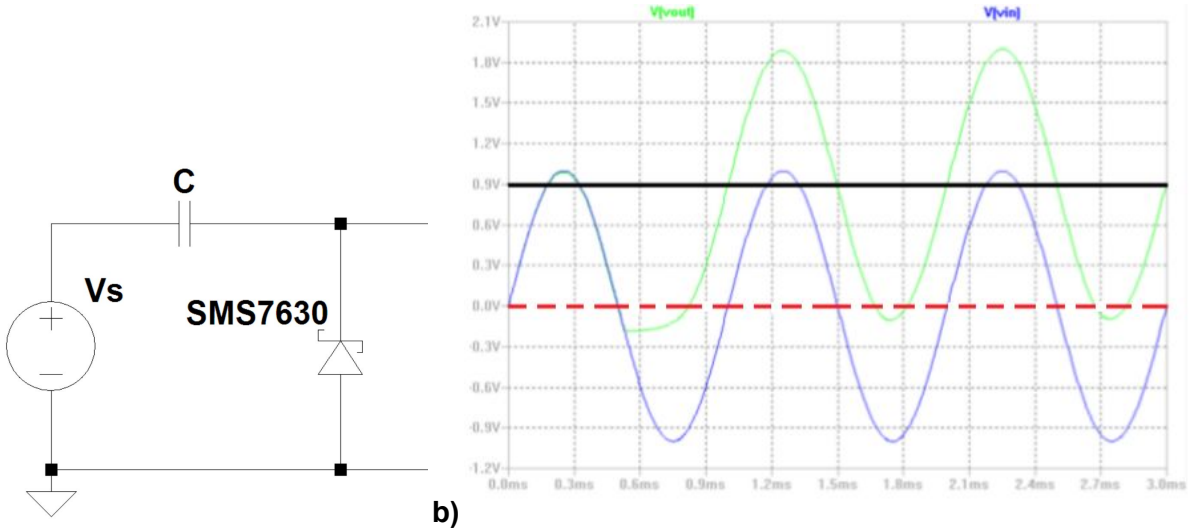


Figure 25: Greinacher Rectifier with Schottky Diodes

The Greinacher rectifier converts AC input voltage into DC voltage twice the input peak voltage. The Greinacher rectifier leverages both the clamping and peak detecting circuits, see Fig. 25 above.



a) **b)**

Figure 26: a) Clamping circuit schematic and b) waveforms illustrating circuit functionality, with dashed and solid lines indicating input and output DC offset respectively.

The clamping circuit applies a DC offset to the input signal. When the waveform approaches its first negative cycle, the diode conducts and the source charges the capacitor's right plate to the source voltage minus the diode forward voltage V_D while the output remains at $-V_D$. When the input voltage increases, the source and capacitor voltages add together at the output. Thus, the output maximum is the peak source voltage V_{sP} plus the capacitor voltage; $2V_{sP} - V_D$. For a $1V_p$ input voltage and 100mV diode forward voltage, Figure 26b shows the output waveform with a 0.9V DC average and 1.89V peak.

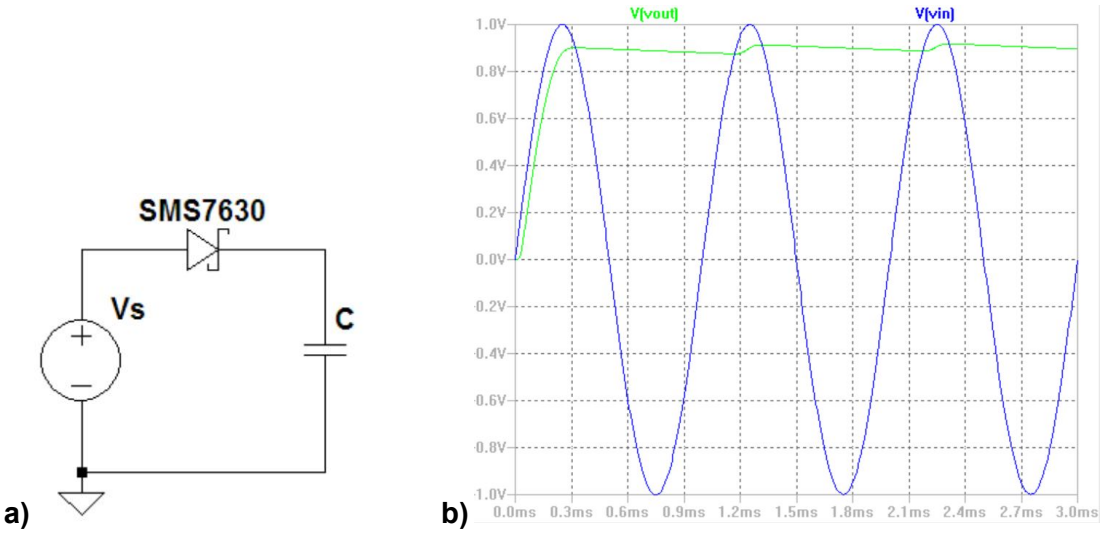


Figure 27: a) Peak detector circuit and b) waveform illustrating circuit functionality.

The peak detector circuit attempts to maintain a constant input peak voltage. On the positive cycle, after the input increases beyond the diode forward voltage, the diode conducts and the source charges the capacitor. When $V_s = V_{sP}$, the output voltage is $V_{sP} - V_D$.

As the input decreases, the diode becomes reversed biased. While reversed biased, leakage current flows through the diode from the capacitor. Capacitor charging and discharging cycles create DC output ripple.

Figure 28 shows the waveforms at the Greinacher rectifier input, at the clamping circuit output (node A), and at the rectifier output (see Figure 25). The clamping circuit introduces the $V_{sP} - V_D$ DC offset at node A. The peak detector maintains the node A peak voltage. The final Greinacher rectifier voltage is defined by (5), where V_{sP} is the peak source voltage, and V_D is the diode forward voltage. To maximize output voltage, V_D must be minimized; hence, Schottky diodes were used.

$$V_{out} = 2(V_{sP} - V_D) \qquad (5)$$

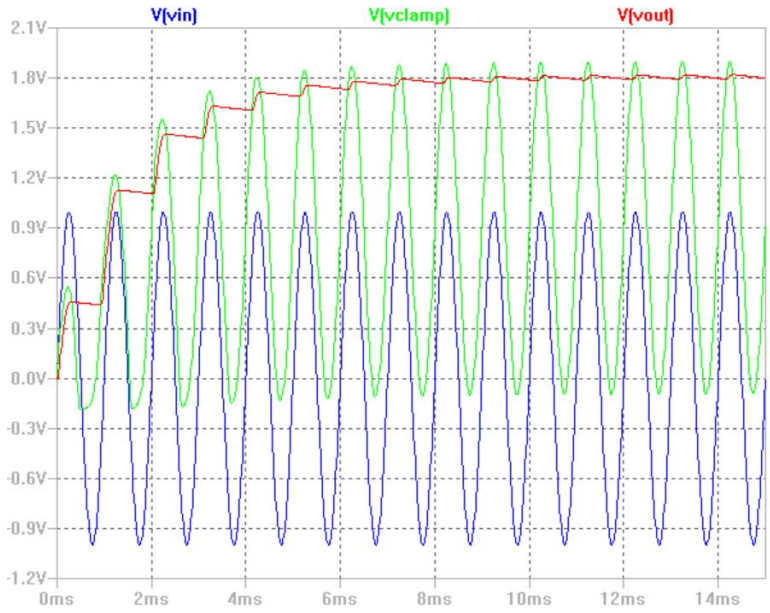


Figure 28: Greinacher Rectifier waveforms at the input, the clamping circuit output (Node A), and the output.

To increase the output voltage, multiple stages can be cascaded. A two-stage cascade is shown in Figure 29; the circuit pattern is identified and extended to N cascaded stages.

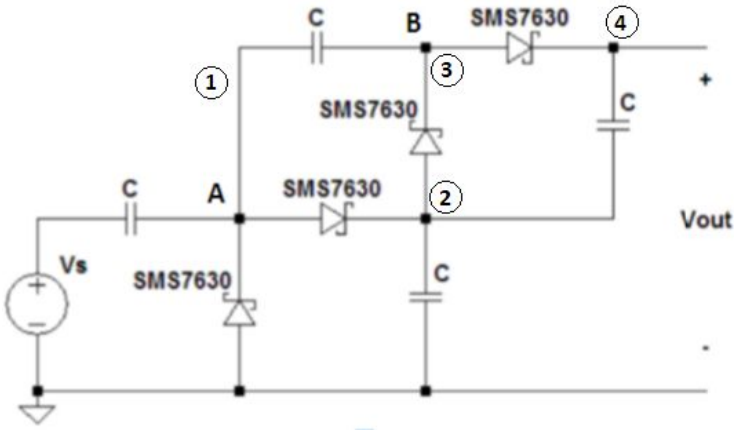


Figure 29: Two-Stage Cascaded Greinacher Rectifier

This configuration is summarized below - reference Figure 29 schematic.

1. Node A signal becomes the second stage input.
2. First stage output is the second stage ground reference.
3. Node B adds $2V_{sP} - V_D$ offset to node A.
4. The second peak detector rectifies the node B signal.

The output voltage relative to the first stage output is $2*(V_{sP} - V_D)$. However, if the overall output is considered between the second stage output and circuit ground, the first and second stage

output voltages add. The individual stage output voltages result in an overall output of $4*(V_{sP} - V_D)$.

The output voltage for N stages, neglecting ripple, is defined by (6), where V_{sP} is the peak input voltage, and V_D is the diode forward voltage.

$$V_{out}(N) = 2N(V_{sP} - V_D) \quad (6)$$

Simulation

A single-stage rectifier is not sufficient for -75dBm (31.6pW) to -70dBm (100pW) range input power levels; thus, cascaded stages was required. Fewer stages reduces cost and size, thus a maximum seven-stage system was tested. Initial simulations were performed at 1kHz to verify circuit operation while ignoring transmission line effects. Output voltages were measured for each cascaded stage to verify with equations. This simulation used a Schottky diode model default in SPICE with a 100mV forward bias voltage. The capacitor values are 1uF and 100uF. The input voltage was a $1V_{pp}$, 0V offset, 1kHz sine wave. Results are shown in Table 6.

Table 6: SPICE Calculations, Rectifier Performance vs. Number of Stages, Sinusoidal Input: $1V_{pp}$, 0V offset, 1kHz

Number of stages	Calculated V_{out} (V)	C = 1μF		C = 100μF	
		V_{out} Unloaded (V)	Ripple amplitude (mV)	V_{out} Unloaded (V)	Ripple amplitude (mV)
1	1.80	1.81	26.13	1.82	0.24
2	3.60	3.56	82.74	3.64	0.80
3	5.40	5.11	169.23	5.46	1.67
4	7.20	6.33	284.61	7.28	2.84
5	9.00	7.08	429.12	9.09	4.35
6	10.80	7.26	600.78	10.91	6.17
7	12.60	6.74	794.84	12.73	8.31

Ripple increases with increasing number of stages and decreasing capacitance. Each stage's capacitance combines in series. Series capacitors reduce capacitance, reducing the RC time constant; thus, output ripple increases. The maximum voltage cannot exceed $2N(V_{sP} - V_D)$. The signal oscillates about a value below V_{sP}. Thus, the output RMS voltage (DC output) value decreases. When the capacitors are all increased from 1μF to 100μF, the ripple was reduced by 2 orders of magnitude. Output voltages measured with 100uF capacitors differed by 1.03% maximum from theoretical calculations. Increasing the capacitance improves output voltage performance, but the circuit response speed is reduced.

Another consideration is the time required to reach maximum output voltage; rectification time. Figure 30 shows ripple and rectification time for 1uF and 100uF system capacitances.

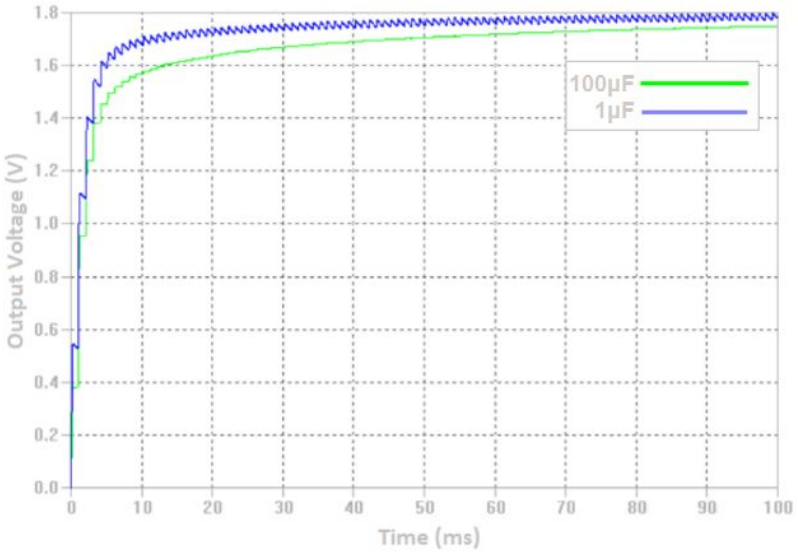


Figure 30: Greinacher Rectifier Ripple and rectification time for a 1kHz sine wave input with 100uF capacitors (green) and 1uF capacitors (blue).

$V_{1\mu F}$ increases to the expected voltage 100 times faster than $V_{100\mu F}$, but with about 100 times the ripple. Rectification time is important because it reduces the system response speed.

The Greinacher rectifier output resistance affects its voltage sourcing capability. The circuit has an output resistance ranging from 6kΩ to 10kΩ, and is nonlinear and load-dependent. Diodes have nonlinear dynamic resistance, increasing impedance matching difficulty. Output voltage ripple originates from leakage current flowing from the capacitor to the load. The RC time constant is inversely proportional to ripple amplitude. This ripple is increased further with more stages, due to the reduced overall circuit capacitance with multiple stages. The load resistance cannot be increased without dissipating additional power. To reduce the ripple without increasing the resistance, the circuit capacitor values were increased to 100µF. Increasing capacitance increases the R-C time constant and rectification time. Figure 31 shows a two-stage rectifier output with 1µF capacitors for 500Ω (V_{out500}), 40kΩ (V_{out40k}), and open circuit ($V_{outOpen}$) load and with 100µF for a 500Ω load (V_{out500} compensated). The 100µF capacitor, 500Ω load configuration shows compensation for decreased R-C time constant.

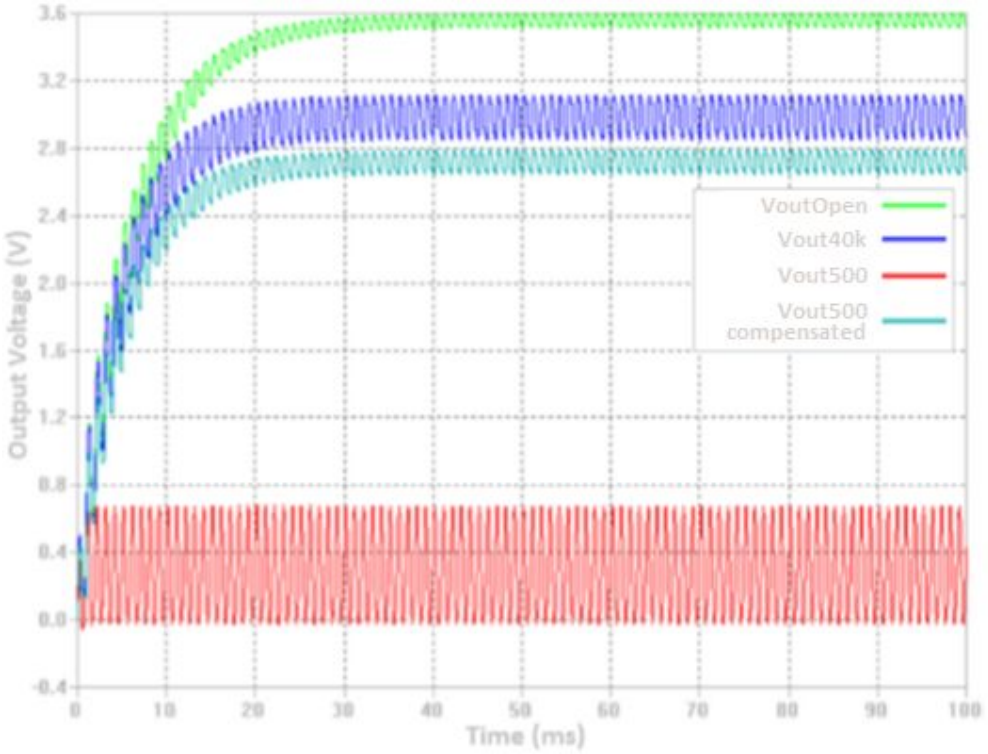


Figure 31: Two-Stage Greinacher Rectifier showing increased ripple under different loading with a $1V_{pp}$, 1kHz input sine wave.

Voltage ripple is inversely proportional to load resistance, as shown in Figure 31. However, with the 500Ω load, the average voltage collapses to about 0.35V. The clamping capacitor did not maintain charge, thus the clamping circuit did not operate. To compensate, 100uF capacitors were used to reduce ripple and allow clamping.

Simulations at 1.9GHz were performed using Keysight's ADS software. Simulations include the SMS7630 diode SPICE model. Capacitor values are decreased six orders of magnitude from the 1kHz design to accommodate the 1.9GHz operating frequency. The 1.9GHz system was initially designed with 100pF capacitors; the final design uses 100nF to reduce ripple. Large capacitors reduce the system's rectifying speed, but at RF frequencies, the output voltage reaches steady-state conditions in less than a second.

The seven-stage rectifier's simulated $|S_{11}|$ is shown in Figure 32.

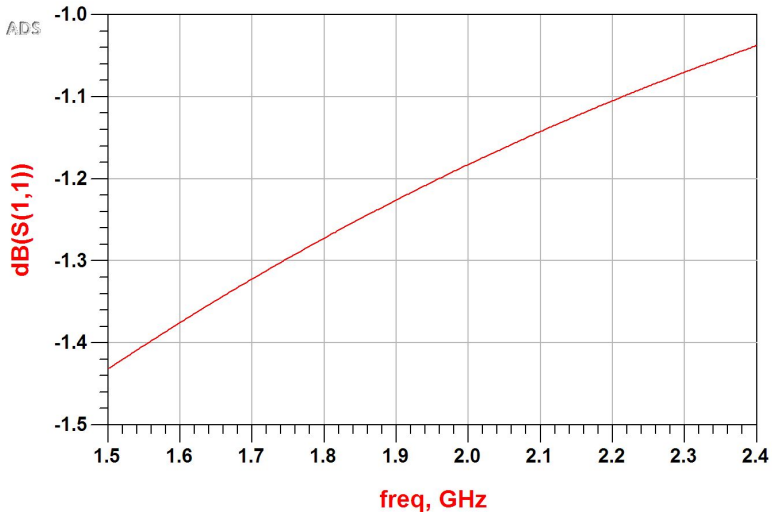


Figure 32: Seven-Stage Greinacher Rectifier simulated $|S_{11}|$

Since the $|S_{11}|$ is greater than -10dB (VSWR > 2) at 1.9GHz, a matching network was designed to match the rectifier to the antenna's 50Ω output impedance. A balanced single-stub matching network (Figure 33) was selected to allow fine-tuning. Using the ADS optimizer, the stub and line lengths were adjusted to minimize $|S_{11}|$ at 1.9GHz. The optimized $|S_{11}|$ is shown in Figure 34.

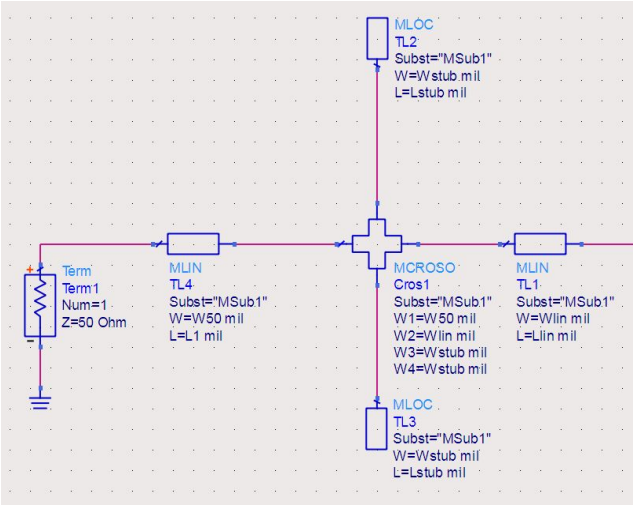


Figure 33: Greinacher Rectifier Balanced single-stub matching network.

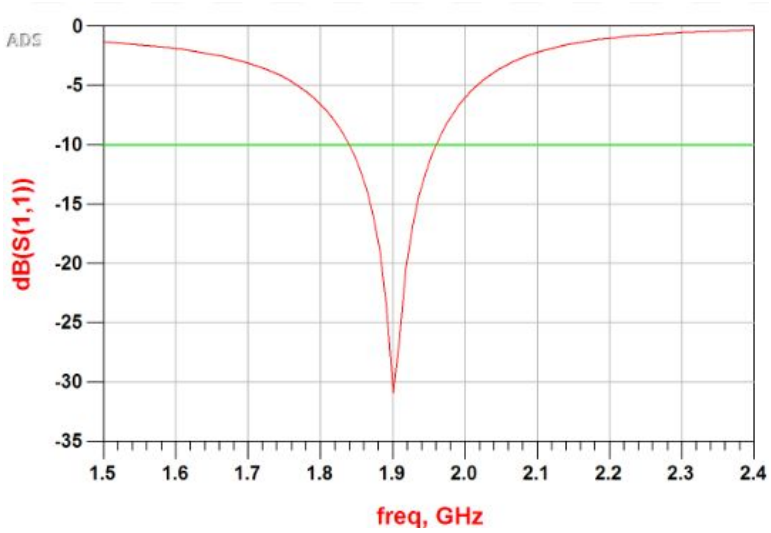


Figure 34: Seven-Stage Greinacher Rectifier simulated $|S_{11}|$ with the matching network.

The final board layout, shown in Figure 35, includes the matching network on the left, and solder pads for diodes and capacitors on the right. Small copper pads reduce the distance between the lumped components to minimize reflections between components. This design was fabricated using an LPKF Protomat S62 milling machine. SMS7630 Schottky diodes with 150mV nominal forward voltage and 26GHz maximum operating frequency are used for this circuit.

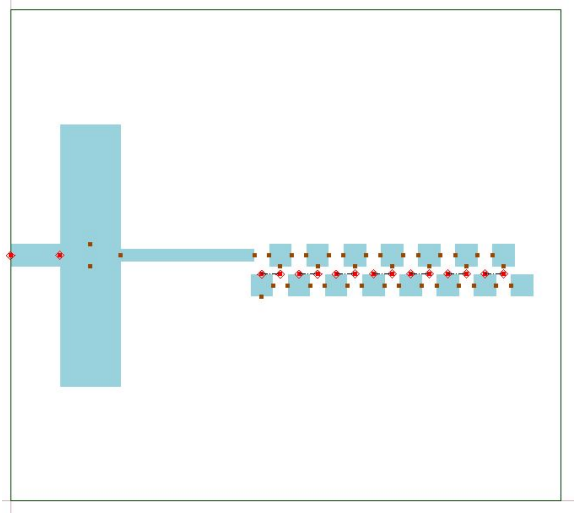


Figure 35: Greinacher Rectifier board layout.

Measurements

DC voltage and $|S_{11}|$ measurements were taken for each cascaded stage for comparison. Stub length tuning was accomplished with copper tape and a utility (X-Acto) knife. Figure 36 shows the measured single-stage Greinacher rectifier DC voltage in millivolts vs. frequency at a 0dBm (1mW) input power level.

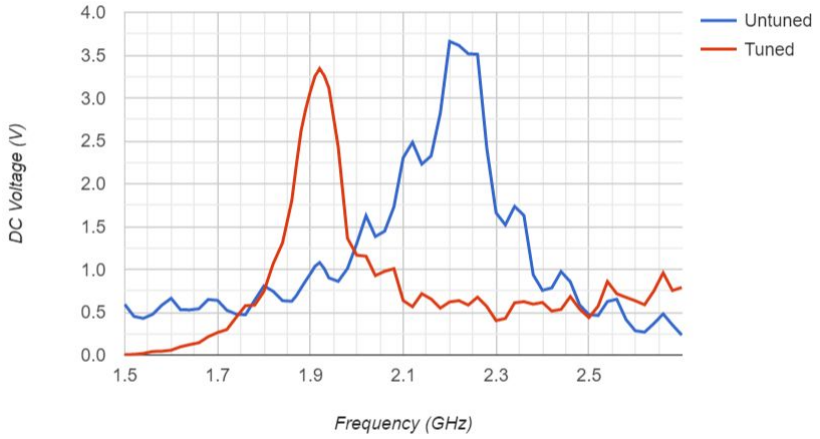


Figure 36: Single-Stage Rectifier Measured DC Output Voltage vs. Frequency at 0dBm Input Power.

The untuned system produced a peak voltage at 2.2GHz instead of 1.9GHz with a 90MHz bandwidth. A $|S_{11}|$ less than -10dB indicates more than 90% of the captured power reaches the rectifier, thus increasing the output voltage. The $|S_{11}|$ is shown in Figure 37.

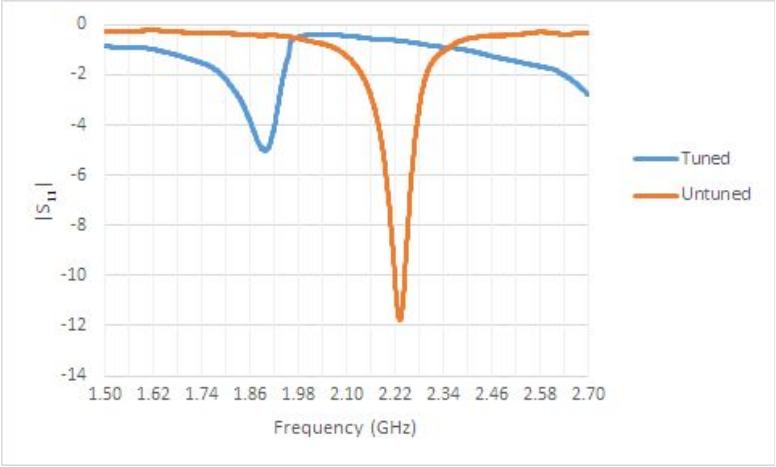


Figure 37: Untuned and Tuned single-stage Greinacher rectifier $|S_{11}|$

Tuned and untuned rectifier $|S_{11}|$ at 1.9GHz are tabulated in Table 7. With additional time, $|S_{11}|$ less than -10dB could be achieved. This result is consistent with the simulated DC voltage plots, since the rectifier output voltage increases with reduced $|S_{11}|$. Measured DC voltage vs. input power level is shown in Figure 38.

Table 7: Measured Rectifier $|S_{11}|$ Before and After Tuning at 1.9GHz

Untuned $|S_{11}|$	-0.43dB
Tuned $|S_{11}|$	-4.99dB

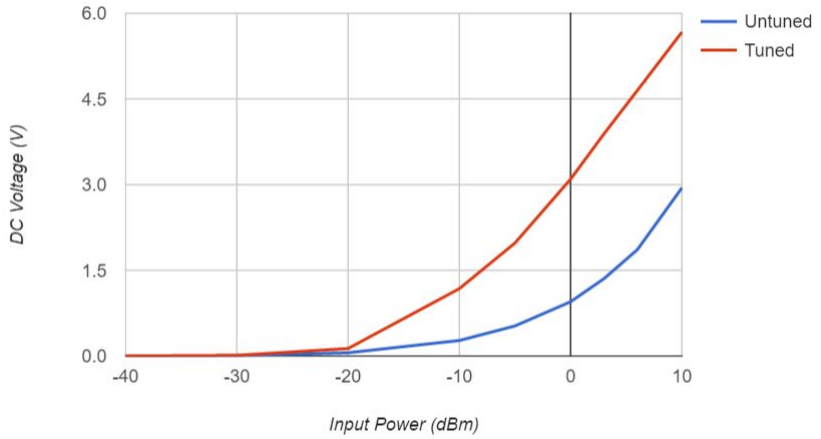


Figure 38: Single-Stage Greinacher Rectifier DC Voltage vs Input Power at 1.9GHz.

A two-stage cascade output voltage at 1.9GHz increased by a factor of 1.46 after tuning with copper tape.

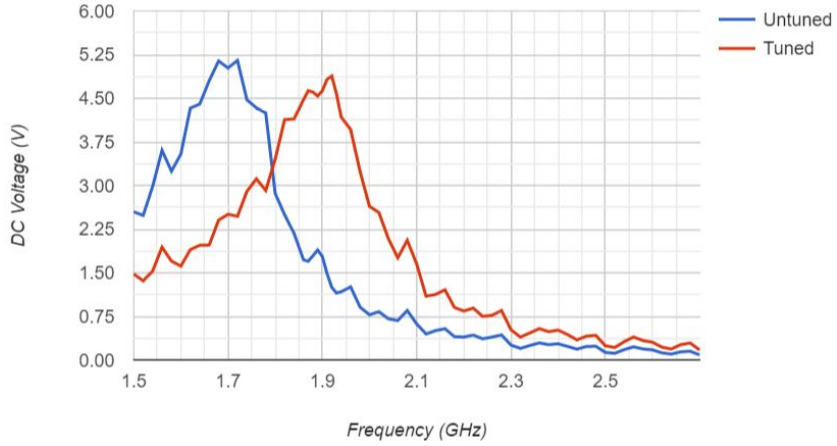


Figure 39: Two-Stage Greinacher Rectifier, DC Output Voltage vs Frequency, 0dBm Input Power

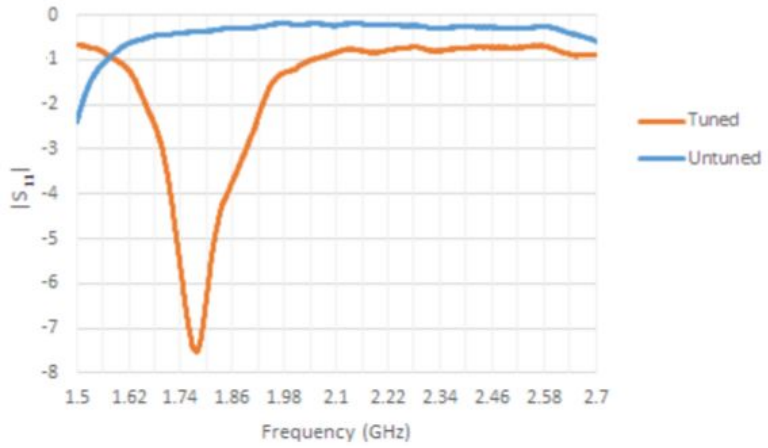


Figure 40: Two-Stage Untuned and Tuned Greinacher Rectifier $|S_{11}|$

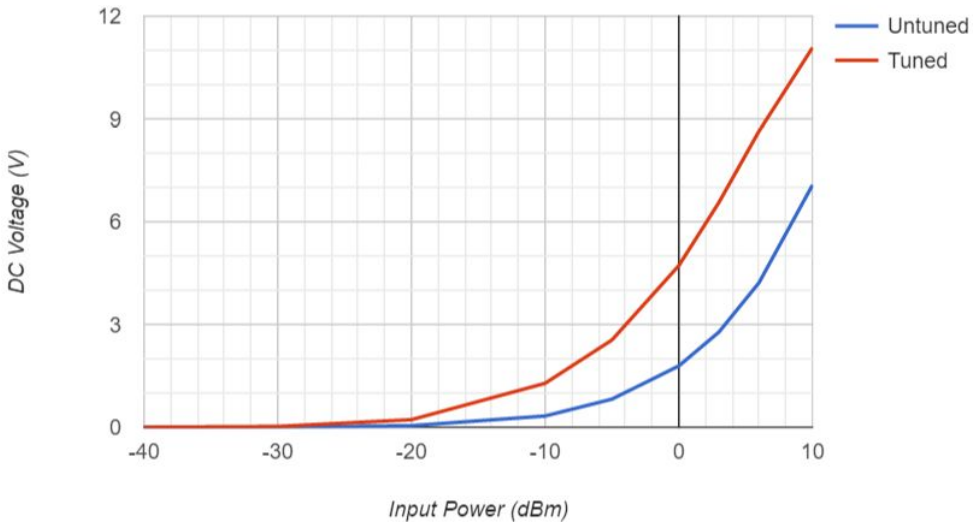


Figure 41: Two-Stage Greinacher Rectifier DC Voltage vs Input Power at 1.9GHz.

A three-stage Greinacher rectifier was constructed; however, a $|S_{11}|$ of -10dB was difficult to achieve with board footprint constraints. The best-case $|S_{11}|$ response with the current matching network appears in Figure 42.

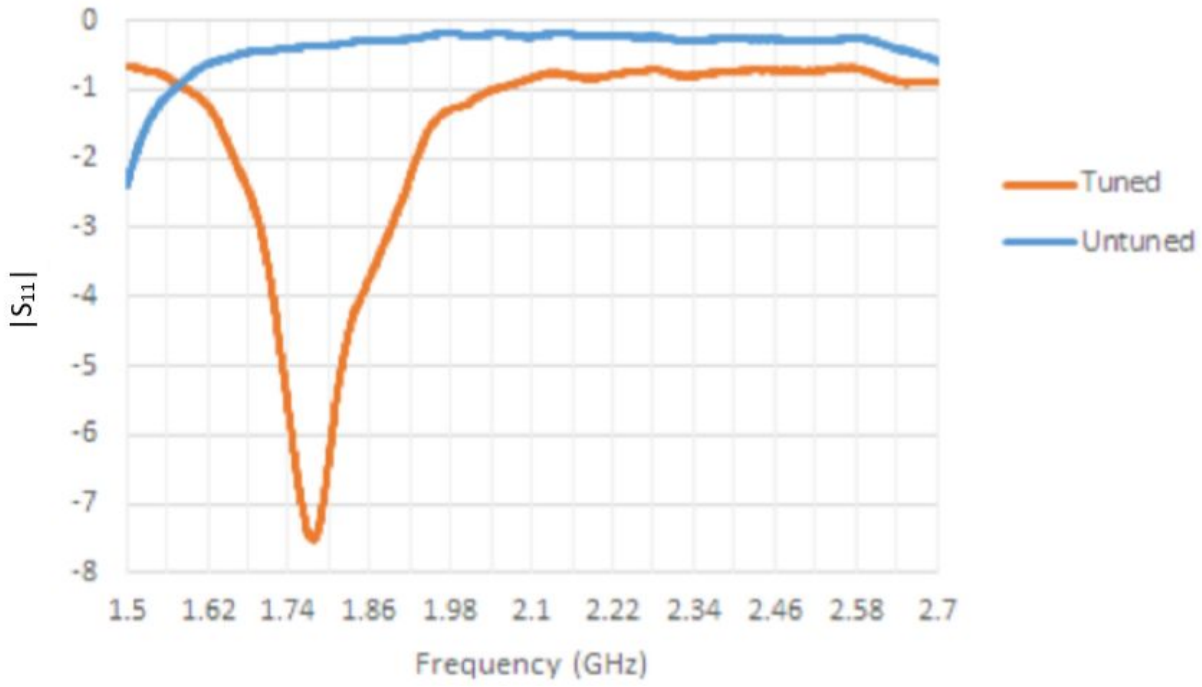


Figure 42: Three-Stage Untuned and Tuned Greinacher Rectifier $|S_{11}|$

Voltage measurements were inferior to the two-stage rectifier, because the two-stage rectifier $|S_{11}|$ at 1.9GHz was about 7dB larger. DC voltage vs frequency and input power is shown in Figures 43 and 44.

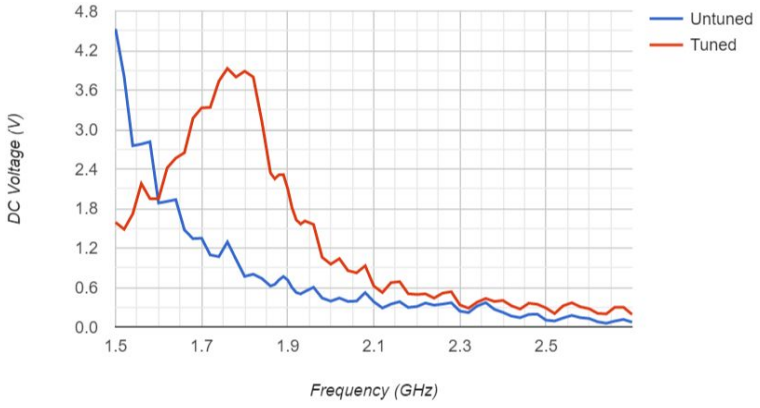


Figure 43: Three-Stage Greinacher Rectifier DC Output Voltage vs Frequency at 0dBm Input Power.

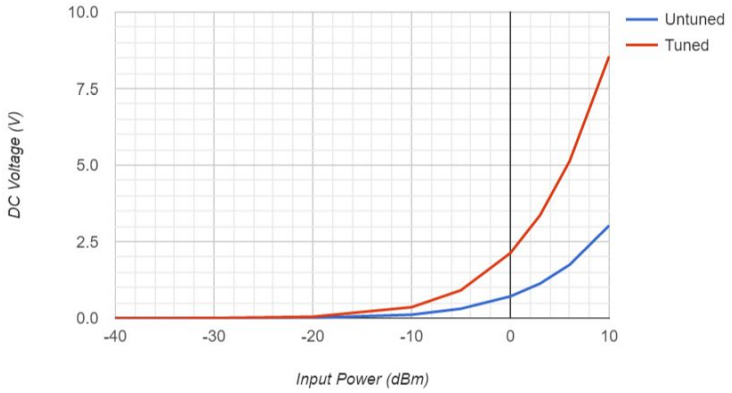


Figure 44: Three-Stage Greinacher Rectifier DC Voltage vs Input Power at 1.9GHz.

A two-stage rectifier was designed and fabricated. Matching performance was unacceptable for three or more cascaded stages due to board footprint limitations.

Figure 45 shows the fabricated circuit output DC voltage vs. input power at 1.9GHz and 500Ω load, the boost converter input resistance.

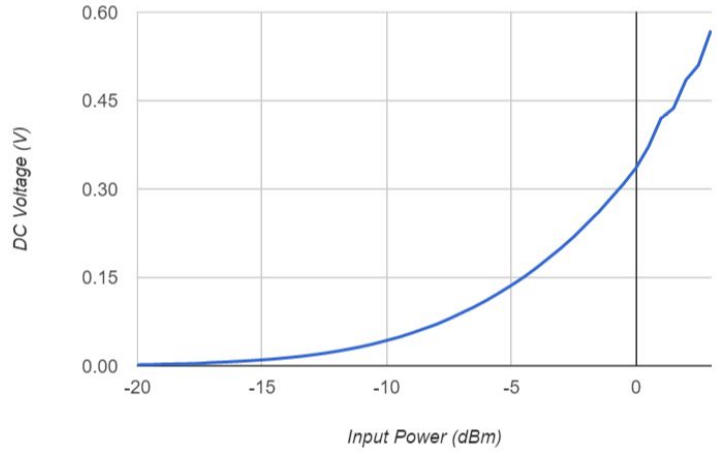


Figure 45: Two-stage Greinacher Rectifier DC Voltage vs Input Power; 1.9GHz with 500Ω load.

The rectifier response (Figure 45) resembles the unloaded case (Fig. 41), but requires -3dBm input power to output the minimum 200mV required by the boost converter. This is greater than ambient power ranging from -75dBm to -70dBm; thus this system cannot be used for ambient RF energy harvesting. A possible alternative for ambient RF energy harvesting includes placing an amplifier before the rectifier; however, this could reduce the overall system efficiency at higher power levels.

To improve future systems, it is suggested to characterize rectifier S-parameters prior to matching network design. To account for solder and final component installation, it is recommended to design the matching network from measured rectifier S-parameters. The matching network could be connected to the rectifier via SMA connectors

Boost Stage Design, Analysis, and Test

The BQ25504 high efficiency boost converter [7] was chosen to boost 80mV to 800 mV input voltages to 3.1V output applied to a 470µF storage capacitor. The 3.1V output can turn on LEDs or power a small microcontroller.

The main boost converter (BQ25504) requires 330mV input voltage when driving a discharged battery; i.e.: cold-start operation. However, if connected to a charged battery, only 80mV is required. A Self-Oscillating Boost Converter (SOBC) charges the battery to a 2.89V threshold before switching to the main boost converter. If the battery voltage decreases below a 2.44V threshold, the SOBC restarts battery charging.

Passive Switch

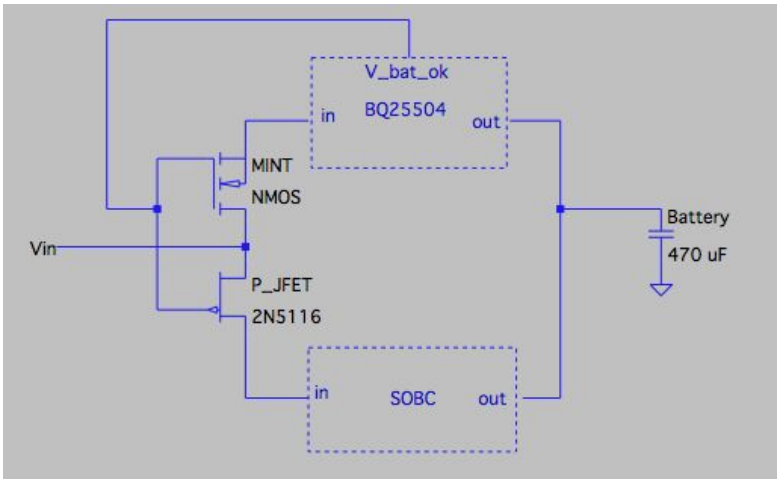


Figure 46: Block Diagram with Passive Switch Implementation

A passive switching network, Figure 46, dictates which boost converter is active. The network accepts input DC voltage from the rectifier and uses the BQ25504's V_BAT_OK flag as the switch control signal.

The V_BAT_OK flag is produced by the main boost converter which senses the battery voltage. The V_BAT_OK flag is set high or low to select the Main Converter or SOBC, respectively.

This window is set by a resistive divider connected to the V_BAT_OK_HYST (Equation 7) and V_BAT_OK_PROG (Equation 8) pins on the BQ25504. Figure 47 shows the BQ25504 schematic with the resistive divider. The hysteretic window is shown in Figures 48 and 49.

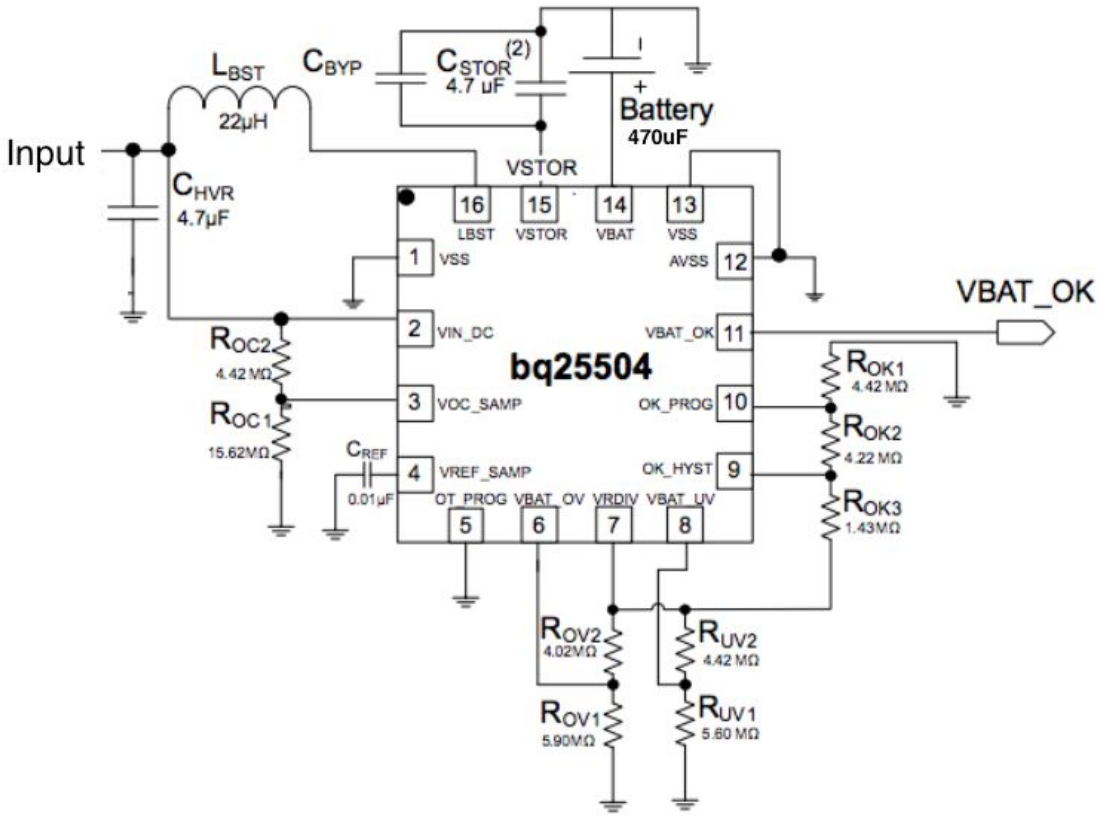


Figure 47: Main Boost Converter Schematic

$$VBAT\_OK\_HYST = VBIAS\left(1 + \frac{R_{OK2} + R_{OK3}}{R_{OK1}}\right) \quad (7)$$

$$VBAT\_OK\_PROG = VBIAS\left(1 + \frac{R_{OK2}}{R_{OK1}}\right) \quad (8)$$

The OK_HYST pin sets the 2.89V upper limit, while the OK_PROG pin sets the 2.44V lower limit for the hysteretic window. Table 8 shows the selected resistor values that create the desired window.

The VBIAS voltage is internally programmed by the BQ25504 IC and is specified between 1.2V and 1.3V.

Table 8: Resistor Values for Programming V_BAT_OK Hysteresis

Resistor	Nominal Value (MΩ)	Measured Value (MΩ)
R_{ok1}	4.42	4.41
R_{ok2}	4.22	4.24
R_{ok3}	1.43	1.42

The resistor sum is maximized (>10 MΩ) to minimize power consumption.

The V_BAT_OK flag features a hysteretic behavior (Figure 48). In the low state, the V_BAT_OK voltage is 0V. In the high state, V_BAT_OK equals the battery voltage.

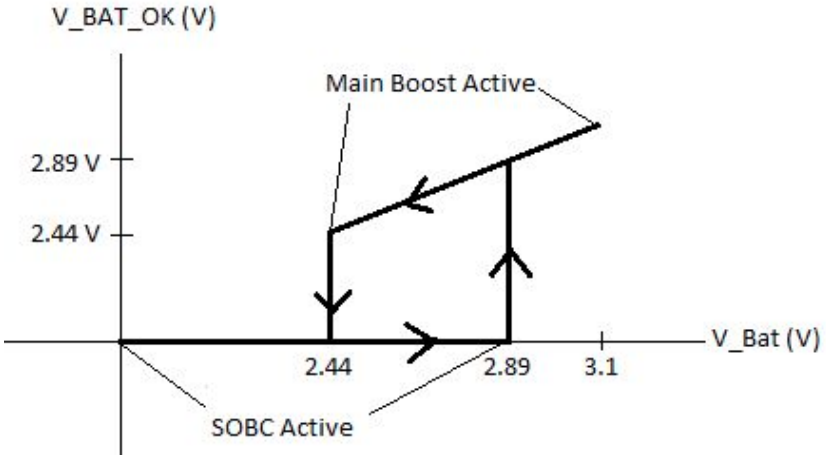


Figure 48: Boost Converter Selection Based on Battery Voltage

The hysteretic window was tested (Figure 49) by applying a ramping voltage onto the V_Bat pin (orange) and observing the V_BAT_OK node (green).

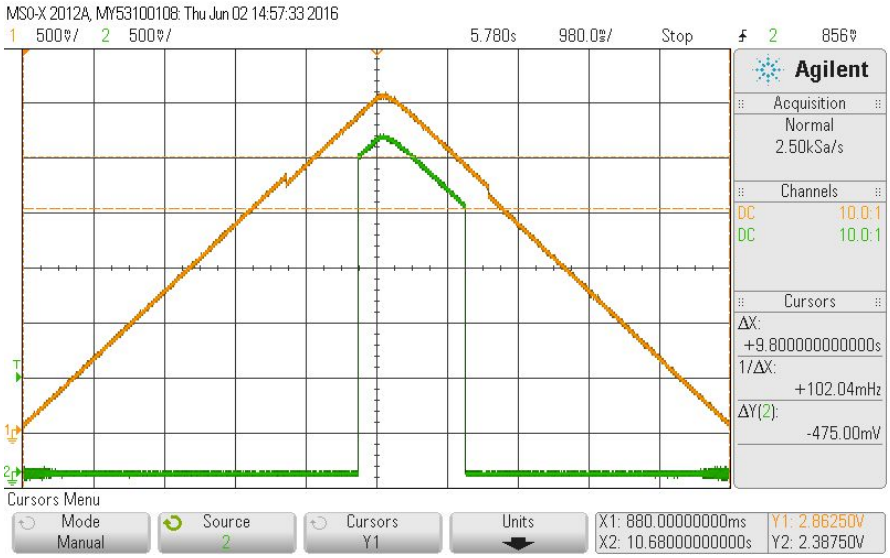


Figure 49: V_BAT Voltage (orange) and V_BAT_OK Voltage (green) vs. Time.

Table 9: Theoretical and Experimental V_BAT_OK Trigger Points

	Calculated (V)	Measured (V)	Percent Error
V_BAT_OK_PROG (lower trigger)	2.44	2.38	2.46%
V_BAT_OK_HYST (upper trigger)	2.89	2.87	0.35%

Theoretical and experimental values differ by less than 3% for both trigger points. This error is attributed to variation in the internally programmed V_BIAS voltage. The BQ25504 refers all voltages to the internally programmed V_BIAS voltage, specified between 1.2 and 1.3V. The midpoint of 1.25V is used for calculating trigger points (Equations 7 and 8). Variation in the V_BIAS voltage results in threshold voltage variations because the BQ25504 uses V_BIAS as its reference.

With the hysteretic window set, the passive switch topology was designed to select which boost converter receives the input voltage, shown in Table 10.

Table 10: Boost Converter Selection Logic

V_BAT_OK VOLTAGE	HIGH	LOW
BOOST CONVERTER	Main Converter	SOBC

The Self-Oscillating Boost Converter (SOBC) accepts the rectifier voltage when the V_BAT_OK pin is set low and is disconnected from the input when the V_BAT_OK pin is set high. A 2N116 P-channel JFET was chosen for a low r_{ds} (100Ω) to minimize loss. The JFET must be non-conducting (pinched off) when the gate voltage (V_BAT_OK) is 2.38V maximum. The 2N116 JFET's pinch-off voltage threshold is 1.5V.

The Main Converter is disconnected from the rectifier output until V_BAT_OK becomes high, thus an N-Channel MOSFET with a threshold voltage less than 2.38V is used. Minimizing on-resistance decreases the drain-source voltage drop and maximizes the boost converter input voltage. The PSMNR90-30BL MOSFET (MINT in Figure 50) was selected; 2.1V maximum threshold voltage and maximum 1mΩ R_{DS} when conducting.

FET SPICE models simulate the passive switch with the boost converters modeled as resistive loads, shown in Figure 50. The Main Converter (BQ25504) datasheet specifies 1.6kΩ typical input resistance. The SOBC input resistance was determined by measuring input voltage and current for input voltages between 0 and 500 mV and 100kΩ, 200kΩ and 300kΩ loads. Typical SOBC input resistance of 800Ω was used for passive switch testing.

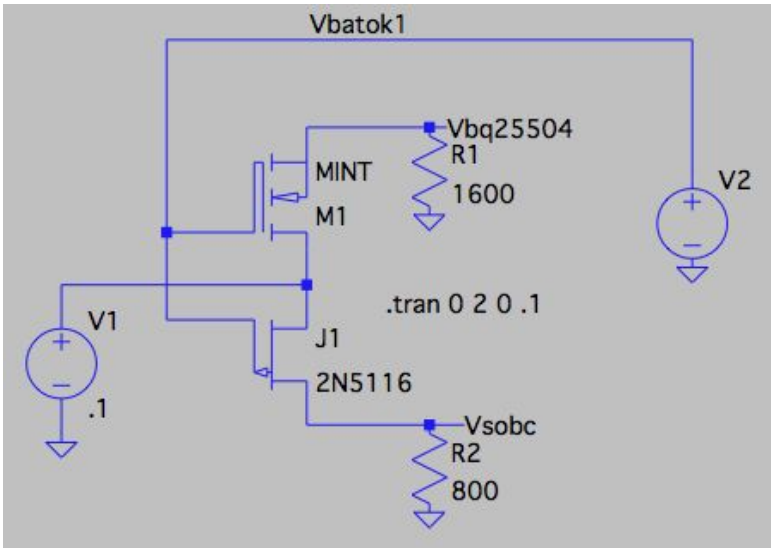


Figure 50: Passive Switch Simulation Schematic

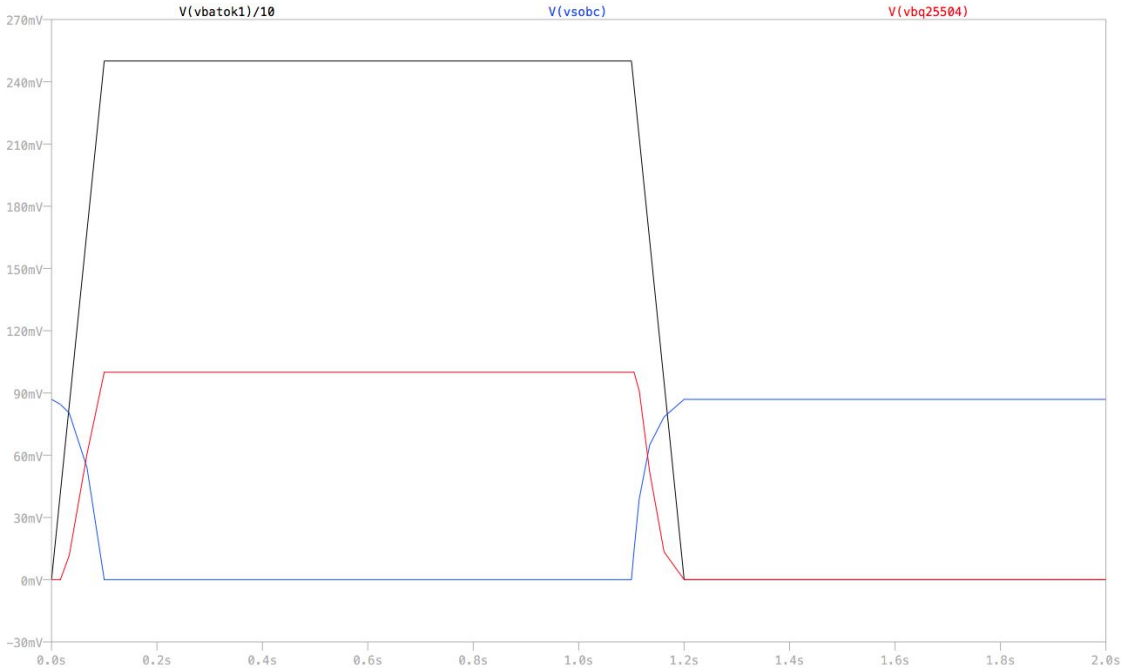


Figure 51: Passive Switch Simulated Switching Voltage (mV) vs. Time (s)

The V_BAT_OK waveform is a square pulse between 0V and 2.5V which simulates the BQ25504. Figure 51 shows V_BAT_OK divided by 10 to allow all voltages to be displayed on one plot. The drain voltage is 0.1V DC simulating the rectifier output voltage. The circuit is built, tested, and compared to simulation predictions. Table 11 compares simulated and experimental passive switch results.

Table 11: Passive Switch Simulated vs. Experimental Results

V_BAT_OK	Boost Converter	Simulated Boost Input Voltage (mV)	Experimental Boost Input Voltage (mV)	Ideal Input Voltage (mV)
0V	V_{SOBC}	89	89.1	100
	V_{main}	0	4.1	0
2.5V	V_{SOBC}	0	5.3	0
	V_{main}	100	99.8	100

Main Boost Converter (BQ25504)

The BQ25504 achieves high efficiency by using Texas Instruments' proprietary nano-power management circuitry, which uses resistive dividers to manage maximum power point tracking. The nano-power management algorithm samples the battery voltage to only draw power every 256ms. The BQ25504 uses this voltage to control its power management circuitry.

The boost converter features a maximum power point tracking system which optimizes converter input impedance based on input voltage. The BQ25504 datasheet [7] advises a VREF_SAMP voltage of approximately 75% of the source's open circuit DC voltage. The rectifier supplies 500mV with open-circuit load at -15dBm input power; the BQ25504 regulates input voltage to 375mV for 75% R_{OC1}, R_{OC2} resistive divider.

$$VREF\_SAMP = VIN\_DC(OpenCircuit)\left(\frac{R_{OC1}}{R_{OC1} + R_{OC2}}\right) \quad (9)$$

The BQ25504 datasheet recommends an R_{OC1}, R_{OC2} sum of 20MΩ to minimize power consumption.

The BQ25504 also features under-voltage protection. This feature is not necessary because if the battery voltage is below 2.38V, the BQ25504 is disconnected and the SOBC is connected. As a result, VBAT_UV is 2.20V, below the 2.38V hysteretic window lower trigger level. V_{BIAS} is internally programmed at 1.25V as the datasheet guarantees a value between 1.2V and 1.3V.

$$VBAT\_UV = VBIAS\left(1 + \frac{R_{UV2}}{R_{UV1}}\right) \quad (10)$$

The BQ25504 regulates the battery voltage to a maximum value, VBAT_OV. This voltage is sustained when there is a surplus of input power. 3.1V is used.

$$VBAT\_OV = \frac{3}{2} VBIAS \left(1 + \frac{R_{OV2}}{R_{OV1}} \right) \quad (11)$$

Table 12: Main Boost Converter, Voltage Threshold Resistor Values

Voltage Setting	Resistor	Resistor Value (MΩ)
VREF_SAMP = 375mV	R_{OC1}	15.62
	R_{OC2}	4.42
VBAT_UV = 2.2 V	R_{UV1}	5.61
	R_{UV2}	4.42
VBAT_OV = 3.1 V	R_{OV1}	5.92
	R_{OV2}	4.02

The BQ25504 IC 3.0mm x 3.0mm package was soldered onto a breakout board for pin access, which introduces parasitic inductance and capacitance. This causes switching noise which degrades circuit efficiency. The noise consumes power at the boost converter switching node. The BQ25504 switching node (V_{LBST}) displays this effect.

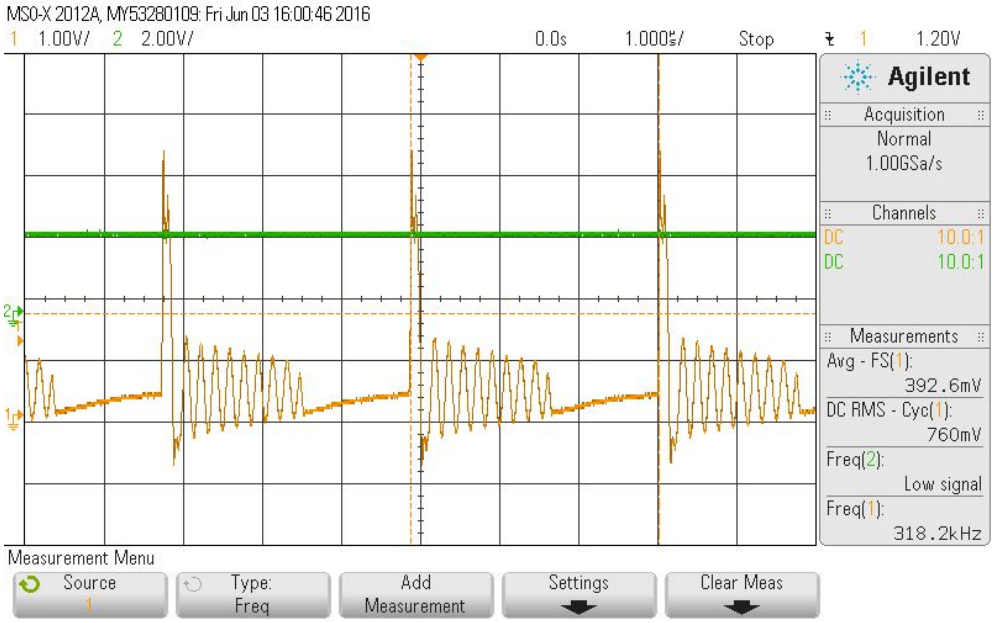


Figure 52: BQ25504 Switching Waveform at V_{LBST} Pin

The BQ25504's efficiency is difficult to test by itself due to input voltage inconsistency. Every 256ms the IC consumes additional power to bias its resistive dividers. A current meter with averaging is needed to measure the input current accurately; however, system efficiency is measurable when the device is interfaced with the rectifier. The Integrated Rectenna section describes operating principles.

Self-Oscillating Boost Converter (SOBC)

The SOBC was designed to boost an 80mV input voltage minimum. The battery is charged to the 2.89V hysteretic threshold voltage to trigger the V_BAT_OK flag. At this voltage, the BQ25504 replaces the SOBC and charges the battery. Figure 53 shows the SOBC schematic.

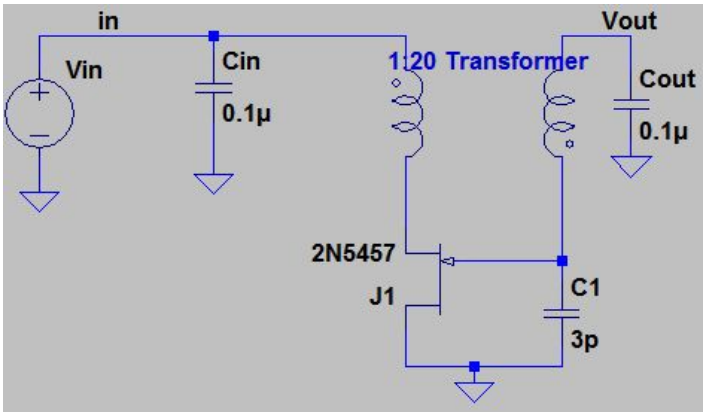


Figure 53: Self-Oscillating Boost Converter (SOBC)

The Self-Oscillating Boost Converter is a modified Joule Thief circuit [8], which creates an oscillating waveform at the 2N5457 JFET gate. The input voltage creates a current through the transformer primary winding. This current induces a 20 times larger current into the JFET's gate due to the 20:1 transformer turns ratio, which forward biases the JFET gate-source PN junction.

The gate-source JFET current charges the output capacitor negatively, and amplifies the drain-source and transformer primary winding currents. Increasing the primary winding current increases the secondary winding current. This positive feedback continues until the JFET saturates, creating a constant drain current. This causes the transformer magnetic field - created by time-varying current - to collapse. The transformer secondary voltage becomes zero. The output capacitor's negative voltage is then applied to the JFET's gate, creating pinching-off (I_{DS} = 0A). This causes the system to return to its initial state and the process repeats itself.

Figure 54 shows the oscillating waveform at the JFET gate.

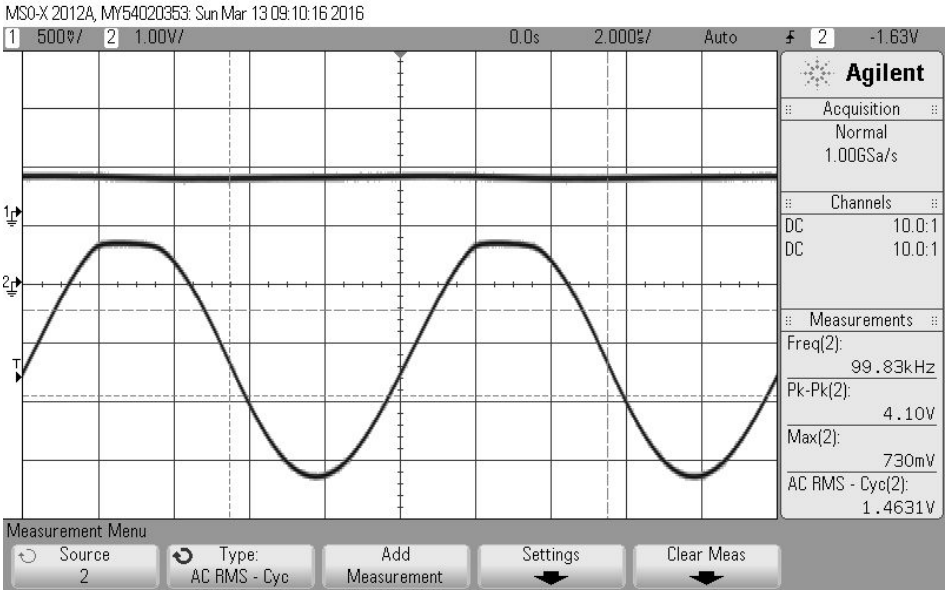


Figure 54: SOBC Input DC Voltage (top) and Gate-Source Voltage (Bottom)

The maximum gate voltage is 730mV. This is the JFET gate-source PN junction 'on' voltage.

The 2N5457 JFET was chosen for its low gate-source pinch-off voltage (-0.6V). Since pinch-off is required for the circuit to begin oscillation, minimizing pinch-off voltage allows for oscillation to commence at lower supply voltages.

The JFET was chosen for its low I_{DSS}: drain saturation current with zero gate-source voltage. Minimizing I_{DSS} decreases the required transistor saturation current. Since the oscillation occurs between saturation and pinch-off, minimizing the required saturation current allows oscillations to occur at lower input voltages (80mV).

Figure 55 shows SOBC input-output voltage characteristics with 100kΩ, 200kΩ, and 300kΩ loads.

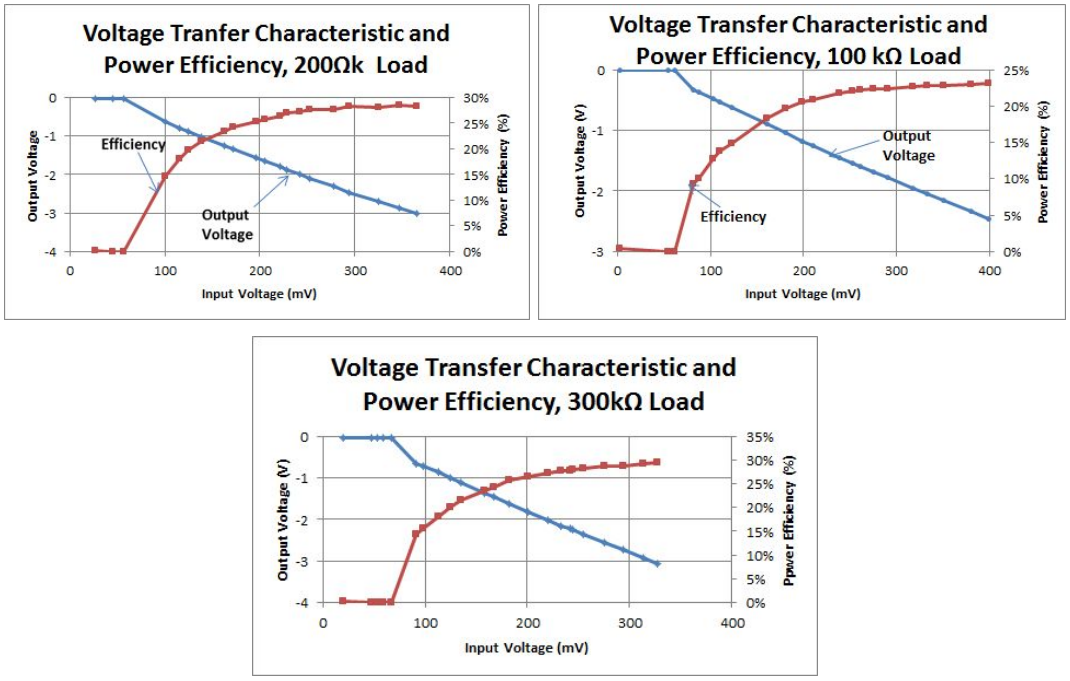


Figure 55: SOBC Output Voltage and Power Efficiency vs Input Voltage

The three load conditions were compared to determine maximum load power transfer efficiency. Measured input current (ammeter) and input voltage yields input power. Output power is calculated from output voltage and load resistance. Figure 56 shows power efficiency and gain vs input voltage for the three load conditions.

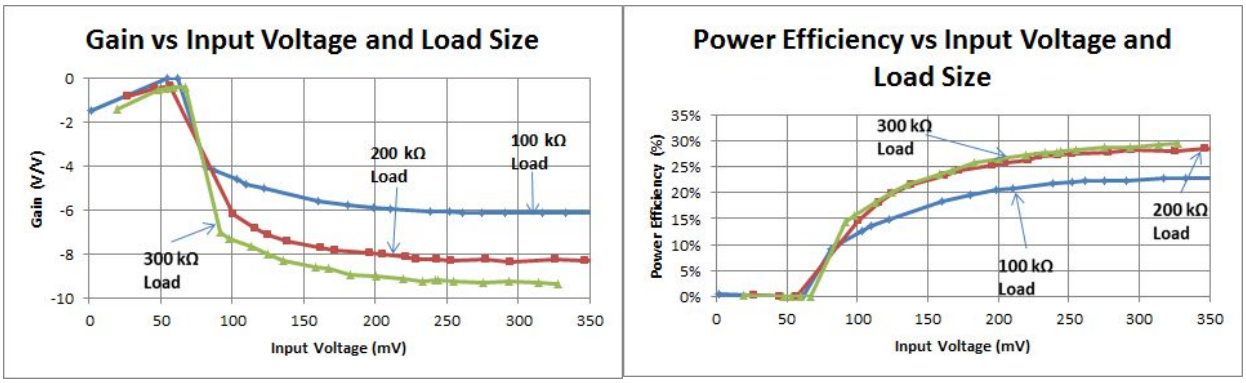


Figure 56: SOBC Gain and Power Efficiency vs Input Voltage and Load Condition

The 300kΩ load yields both the highest efficiency and gain; however, incremental efficiency improvements diminish as load resistance increases. This is supported by the closer proximity

200kΩ and 300kΩ efficiency curves compared to the 200kΩ and 100kΩ load curves. As a result, 300kΩ is the optimum load condition. The efficiency is between 25% and 30% with a 300kΩ load. This is acceptable as the passive boost stage is only designed to boost the battery voltage to 2.89V to power the more efficient active boost stage.

The SOBC output is a negative DC voltage. This poses a problem because the main boost converter outputs a positive DC voltage. Both boost converters are designed to charge a grounded capacitor. For complementary operation, the two boost converters cannot share a common ground due to their opposing output voltages. However, the input voltage must always be referenced to the same ground node. A passive ground switching network is required to implement the design. The input must be referenced to the SOBC ground when the SOBC is used and referenced to the BQ25504 ground when the BQ25504 is used. This was attempted, but could not be achieved due to time constraints. To interface these two boost converters, the proposed Rectenna system uses the low input voltage LTC3108 boost converter instead.

LTC3108 Boost Converter

The LTC3108 boost converter datasheet specifies a 20mV input startup voltage. This is sufficient to charge the output capacitor to 2.89V to turn on the main boost converter. The LTC3108 has four discrete programmable output voltages: 2.3V, 3.3V, 4.1V, and 5.5V. The 3.3V output voltage is chosen to meet the BQ25504's minimum required 2.89V switch threshold. The LTC3108 attempts to boost the battery voltage to 3.3V, but is switched off when battery voltage reaches 2.89V. At this threshold, the BQ25504 begins charging the output.

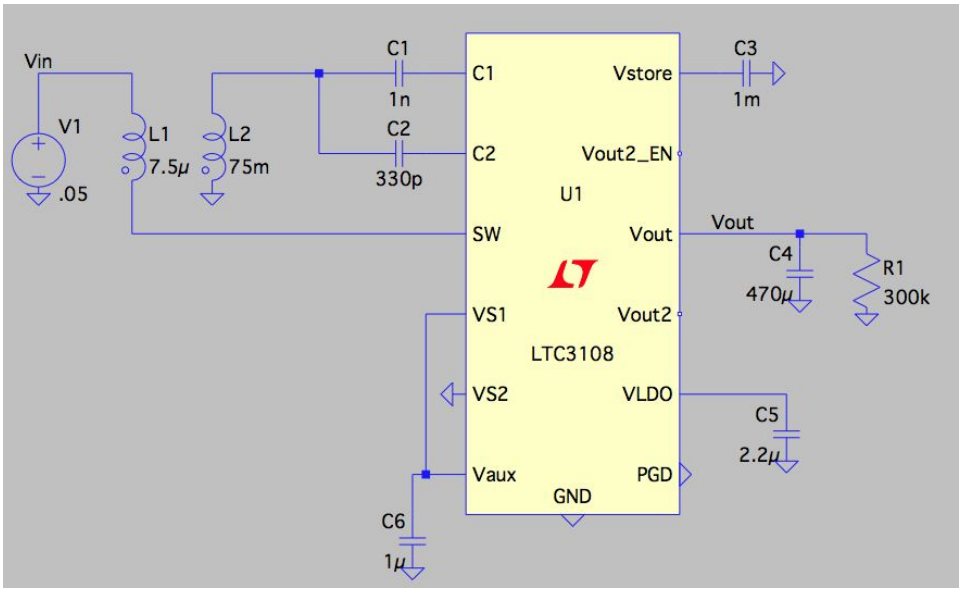


Figure 57: LTC3108 Boost Converter Schematic

The LTC3108 is simulated with a 50mV input voltage and a 300kΩ load resistance.

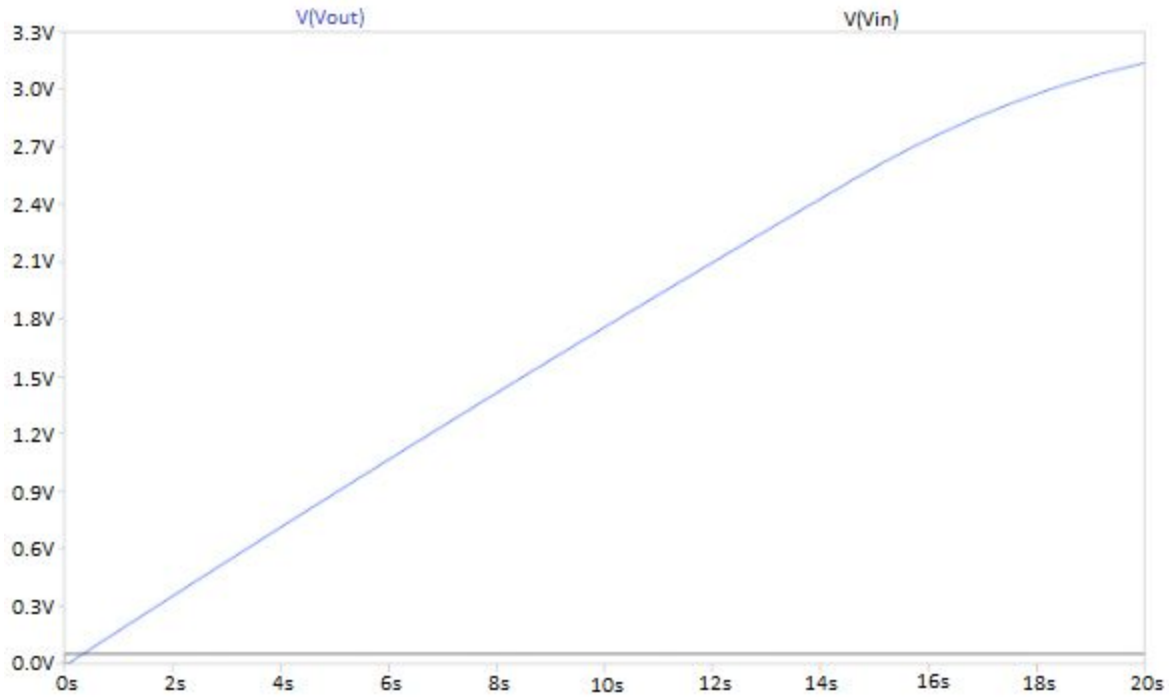


Figure 58: LTC3108 Output Voltage with 300kΩ Load Resistance and 50mV Input vs. Time

The LTC3108 Boost Converter simulation shows that with a 50mV input and a 300kΩ load, it requires 17.5 seconds to charge the battery to the required 2.89V. The LTC3108 switching node is shown in Figure 59.

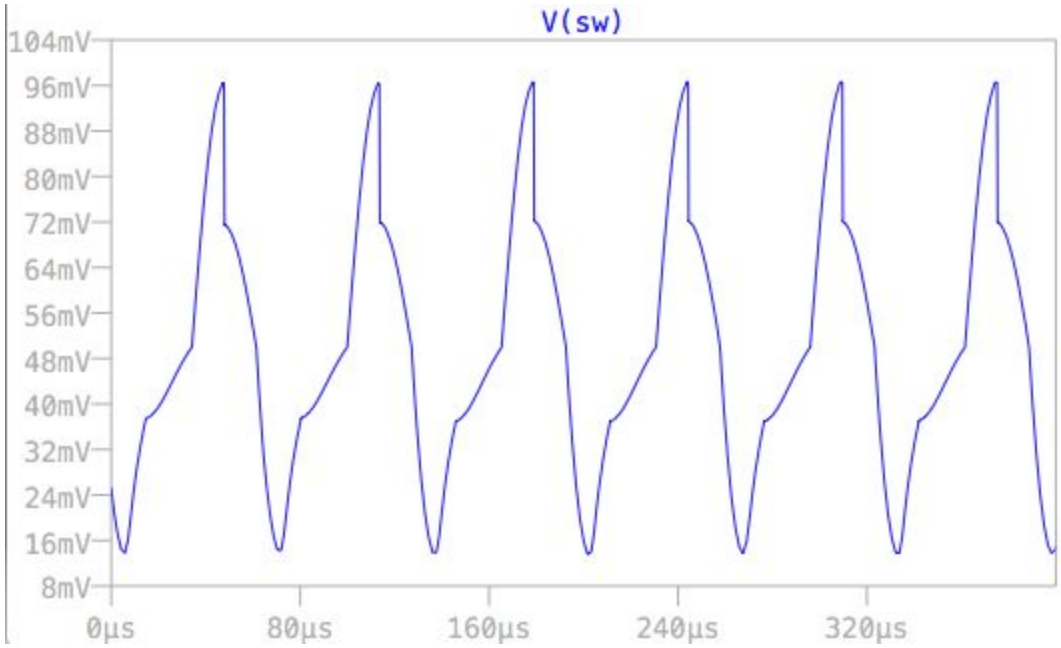


Figure 59: LTC3108 Switching Node Simulation

The circuit was built and tested. Figure 60 shows the measured switching node voltage.

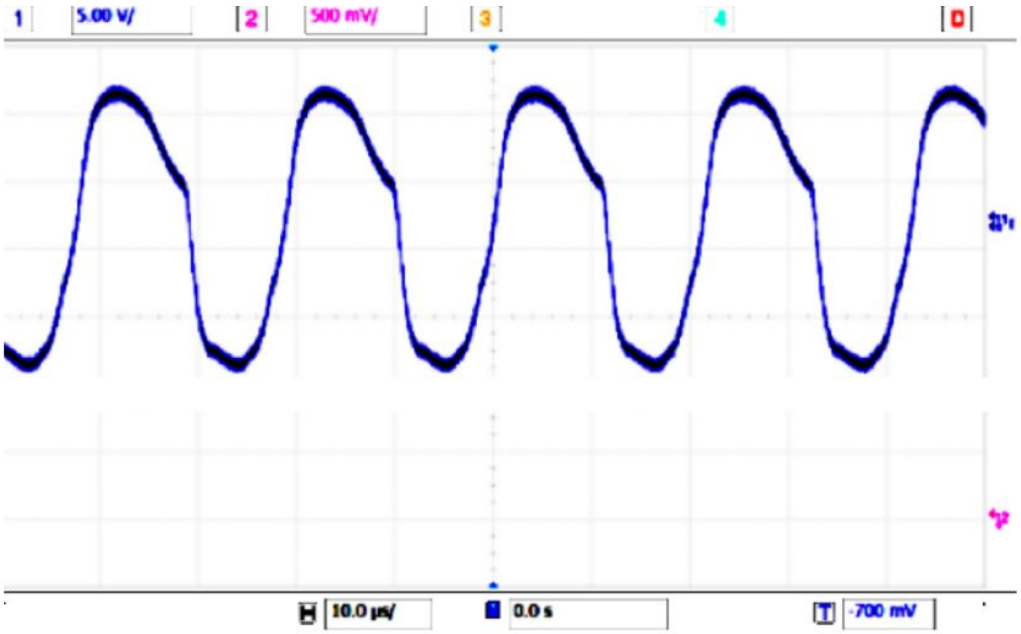


Figure 60: LTC3108 Switching Node Oscilloscope Measurement

The LTC3108 is interfaced with the BQ25504 and the passive switching network. However, glitches on the V_BAT_OK pin prevented proper circuit operation. The LTC3108 charges the storage capacitor, but once the V_BAT_OK pin assumes the high state, it occasionally transitions to the low state causing the LTC3108 to reset.

During integrated Rectenna testing, only the BQ25504 is used. The startup boost converter was omitted and the BQ25504 cold-start circuitry is used. Further research must be conducted to understand and remove the glitch in the BQ25504 V_BAT_OK pin for the boost converter design to function. Additionally, a ground switching network is needed for SOBC system integration.

Integrated Rectenna

The antenna, rectifier, and BQ25504 boost converter were integrated and tested for overall efficiency. Input RF power is measured using a 20dB directional coupler. At an input RF power of -6dBm, voltage began to develop at the output. Between -5dBm and -2dBm the boost converter's cold-start circuitry was active. Until the battery voltage reaches 2.89V, the main boost converter uses its low efficiency cold-start circuitry. This is the stage handled by the SOBC. At -1dBm input power, the main boost converter stage becomes fully active and the cold-start circuitry is disabled. This corresponds to an efficiency increase.

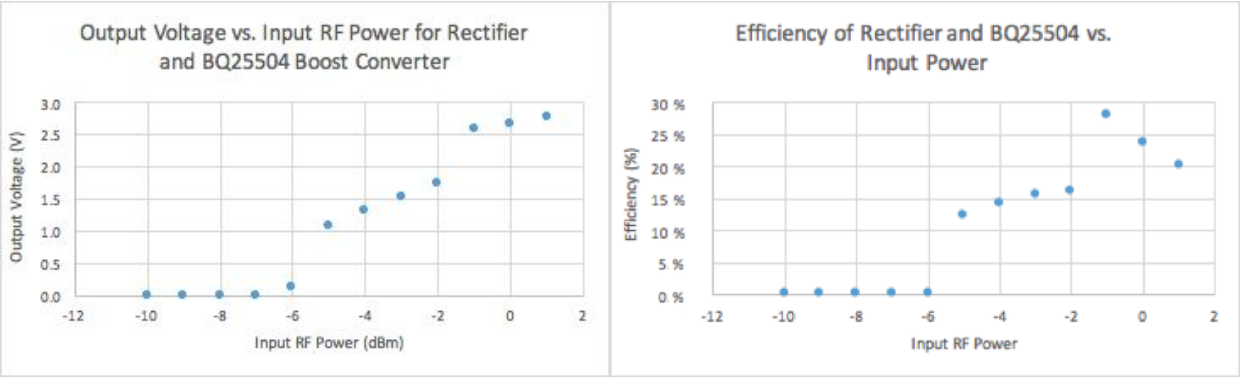


Figure 61: Rectifier and BQ25504 Boost Converter, Output Voltage vs. Input RF Power

The integrated system requires a received power of -1dBm to turn on the main boost converter (BQ25504). This far exceeds power levels found in ambient signals. As a result, the Rectenna cannot be used for ambient RF energy harvesting when combined with the boost converter. The unloaded rectifier results (without the boost converter) are shown in Figure 41 (p. 30).

Conclusions

Overall, the Rectenna implementation in this report is not feasible for general commercial use and may only provide enough power for simple, portable devices. This does not discount the Rectenna concept's feasibility as several commercial solutions are currently under development; e.g.: Freevolt's RF energy harvesting solution [11].

Several potential system improvements are presented in this paper to allow practical use. For example, the matching network should be designed after the rectifier hardware implementation for easier matching. Also, designing a passive ground-switching network to integrate SOBC with BQ25504 would improve startup capability. The ground-switching network is required to use the SOBC and BQ25504 together due to the SOBC's inverted output. Eliminating the V_BAT_OK glitch from the BQ25504 allows for boost converter integration.

A "practical use" recommendation is to employ an omnidirectional antenna, an antenna that radiates equally well in all directions in one plane. Using a directional antenna limits the power harvesting capabilities in certain locations, because it requires directing the antenna at an explicit source. An omnidirectional antenna allows harvesting from many different, albeit smaller, intensity sources.

The RF energy harvesting system presented in this paper is comparable to 2016 IEEE APS Student Design Contest finalists. South University of Technology and China achieved 20% efficiency at -20dBm input power [9]; however, -20dBm appears to be transmitted rather than received power. The Team Waterloo submission [10] also used the Greinacher Rectifier and achieved 20% efficiency at -20dBm input power. The two-stage Greinacher rectifier (without boost converter) efficiency at -20dBm is 23%, shown in Figure 41 (p. 30). This result is slightly better than the two competitors mentioned previously. Although the boost converter increases the output DC voltage, the system efficiency is degraded. Figure 62 shows the Cal Poly two-stage Greinacher Rectifier vs. the Team Waterloo submission.

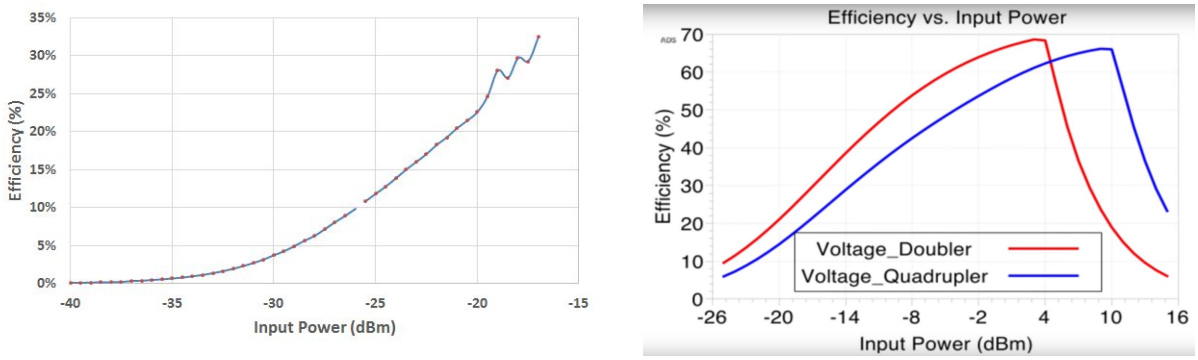


Figure 62: Cal Poly Two-Stage Greinacher (Left) vs. Team Waterloo Rectifier (Right) Efficiency

Appendix A: Senior Project Analysis

1. **Rectenna Functional Requirements Summary**
    a. The Rectenna rectifies captured RF signals and stores the converted DC power in a storage capacitor. In total, the Rectenna has 4 main stages: Antenna, rectifier, boost-converter, and storage capacitor. The harvested RF is rectified by a Greinacher rectifier, converting RF signals to DC power.

2. **Rectenna Primary Constraints**
    a. The first design constraint is receiving a signal that can be successfully rectified by the Greinacher rectifier. The present antenna is only tuned to 1.9GHz. When using the Rectenna in an area where 1.9GHz signals do not exist, a signal cannot be received. The antenna receives a singular frequency with a 1% bandwidth due to size and cost issues. The overall Rectenna output power is a second constraint.

3. **Rectenna Economic Impacts**
    a. The rectenna system is currently not marketable. The first generation Rectenna provides enough power for select applications. For example, radio frequency identification (RFID) tags could possibly use this rectenna system since they are low-power devices.

    b. The predicted project cost was about $130, covering all parts needed to build a single Rectenna system. Each graduating electrical engineering student is allowed $150 for their senior project, increasing starting funds above the project cost. No equipment costs are included in the predicted project cost because all equipment for designing and building the Rectenna are available for student-use in Cal Poly's EE department. There are no current plans to sell Rectenna units to the public. Before Rectenna system profits can be discussed, the design must become marketable.

4. **Time Constraints**
    a. The Rectenna system must be completed by June 2016. This includes the deadline set for the design, testing, and manufacturing. The estimated development time for the entire Rectenna system is 6 months. During this time, all parts must be purchased, individual stages must be tested, and the system must be integrated.

5. **Manufacturing the Rectenna on a Commercial Basis**
    a. RF energy harvesting is not currently available for purchase by the general public. Only engineers interested in pursuing alternative forms of energy or improving upon the technology would be interested in purchasing a Rectenna.

    b. The user incurs no cost when operating the passive Rectenna. Once built, the Rectenna collects power in the storage capacitor, and the user can power an electronic device.

6. **Environmental**
    a. Manufacturing capacitors, resistors, IC's, and any other electrical components harms the environment. Manufacturing plants that produce these components release harmful toxin by-products into the ecosystem. However, the Rectenna system is relatively simple when compared to smartphone, computers, and electronic devices with high numbers of components. Therefore, the overall environmental detriment created by the components needed for the Rectenna is much lower than that of other commercial electronic devices.

7. **Manufacturability**
    a. One of the challenges when manufacturing the Rectenna on a large scale is building antennas that are tuned to different frequencies which may be more prominent in other areas of the world. Assembly line antenna production is difficult to implement since each antenna at a different frequency would require a different tuning process. This problem is resolved with the addition of a tuning circuit or stage in the Rectenna that tunes the antenna to a different frequency and changes the matching network to accommodate. While difficult to implement, this solution is possible.

8. Maintenance

a. The Rectenna currently operates at a cellular frequency which is problematic because the Rectenna potentially “steals” spectral energy from other devices and impedes that device’s functions. A proposed upgrade of the Rectenna is changing the design of the antenna stage and allowing for tuning the antenna to multiple frequencies instead of one. Rectenna design upgrade requires additional labor, components, and manufacturing costs. This increases Rectenna system cost and consumer price.

9. Ethical

a. The Rectenna project does not violate any IEEE code of ethics rules. In fact, the Rectenna project upholds and reinforces many IEEE code of ethics principles. IEEE code of ethics, item #5 states: “to improve the understanding of technology; its appropriate application, and potential consequences.” RF energy harvesting is underdeveloped. By completing a Rectenna design, the project team will extend the technology. Another IEEE code of ethics item upheld by the Rectenna design project is #7: “to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others. “Completion of the Rectenna project involves feedback from peers, professors, and the IEEE itself which espouses better communication and relations between the groups.

b. When examining the Rectenna project using Utilitarianism, the project remains a worthy cause for completion. Utilitarianism specifies the purpose of morality is to improve life by increasing the amount of good things (happiness) in the world and decreasing the amount of bad things (unhappiness). The Rectenna increases overall happiness by reducing energy cost. This energy cost reduction enables less-fortunate people access to free and renewable energy, improving the quality of life. Thus, the project is a worthwhile pursuit.

10. Health and Safety

a. The health and safety concerns of designing and building the Rectenna are, overall, minimal. After rectification, the DC voltages measured are on the order of tens of millivolts, a value that could never harm a human. After boosting the voltage to 3.3V for charging the storage capacitor, there are little to no health risks if a human were to touch the 3.3V node. There are also no health risks associated with 1.9GHz signal reception or overheating of any components.

11. Social and Political

a. The Rectenna system provides clean and renewable energy to the public. The ability to generate power from a renewable resource helps reduce the dependence to fossil fuels of today's society [1]. Reduction of fossil fuels improves the global warming situation, leaving the biosphere more inhabitable for all life. Considering the Rectenna as a device that improves the quality of life for all living creatures on earth means all living creatures have a share in the success of this project.

12. Developmental

a. To understand the boost stage of the Rectenna in the project proposal, the entire subject of DC-DC conversion was considered, including ultra-low voltage DC-DC conversion, since the rectified signal is on the order of microvolts to millivolts.
b. The Rectenna boost stage consists of both an active and a passive boost converter. The passive boost converter is a Self-Oscillating Boost Converter (SOBC). The SOBC charges a storage capacitor when its voltage is below 2.89V. At this voltage, the circuit switches trigger, disconnecting the SOBC and connects the main active boost converter which is more efficient. The main boost converter is the BQ25504 ultra-low power boost converter and is equipped with a maximum power point tracking algorithm that varies the converter's input impedance in order to maximize output power. The BQ25504 has a 330mV cold start input voltage and once running, rectifies voltages as low as 80mV, while operating off 330nA.
c. The Greinacher Rectifier outputs a voltage less than 330mV to operate the main boost converter. The BQ25504 operates as an active component, powering itself through the storage capacitor. If the voltage on the storage capacitor falls below 3.3V, the SOBC reconnects to recharge the capacitor such that the main boost is used. No external power supply is needed.

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