

Electronic properties of CVD graphene: The role of grain boundaries, atmospheric doping, and encapsulation by ALD

Zenas A. Van Veldhoven**, Jack A. Alexander-Webber, Abhay A. Sagade, Philipp Braeuninger-Weimer, and Stephan Hofmann*

Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, United Kingdom

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 $*$ Corresponding author: e-mail sh315@cam.ac.uk, Phone: $+44$ 1223 748346, Fax: $+44$ 1223 748348 ** Also at: Cambridge Graphene Centre, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, United Kingdom

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Grain boundaries and unintentional doping can have profound effects on graphene-based devices. Here we study these in detail for CVD grown poly-crystalline monolayer graphene with two significantly different grain size distributions centered around $10-25 \mu m$ and $100-400 \mu m$. Although the two types of graphene are processed under identical conditions after growth, they show distinct transport properties in field effect transistor devices. While all asfabricated samples showed similar p -type doping, the smaller grain size type graphene with larger number of grain

1 Introduction Graphene is a promising device material for future electronic and optoelectronic applications due to its remarkable properties [1–4]. It can sustain a high mobility, large saturation velocity of charge carriers and high current densities, as well as shows broadband optical adsorption and mechanical stability/flexibility. A critical requirement to realize its potential for industrial applications is not only the manufacturing of highly crystalline, low defect density "electronic-grade" monoor few-layer graphene films, but also their interfacing with current processing technology and existing materials such as conventional metals and dielectrics. Chemical vapor deposition (CVD) has emerged as a viable pathway to develop industrial-scale integrated graphene manufacturing [5–8]. Since the properties of graphene are highly sensitive to its microstructure and environment, including support and exposure to air, solvents and lithography boundaries exhibit lower average mobility. In order to separate out the effects of grain boundaries and doping from ambient exposure on the transport properties, the devices were encapsulated with Al_2O_3 by atomic layer deposition. The encapsulation of large grain samples thereby showed drastic improvements in the performance with negligible doping while the small grain samples are largely intolerant to this process. We discuss the implications of our data for the integrated manufacturing of graphene-based device platforms.

resists, achieving reproducible and reliable device performance is a particular challenge. We focus here on the development of graphene-based field effect transistor devices (GFETs), which exemplifies many aspects of this challenge.

The microstructure of a graphene CVD film links directly to the nucleation density and how the graphene nuclei align and evolve during the growth. When these nuclei meet to form a continuous film, grain boundaries (GBs) can form depending on their relative alignment [7, 9–13]. While individual single-crystal CVD-grown grains have properties equal to the best mechanically exfoliated graphene flakes [14, 15], the detailed influence of GBs on the electric and optoelectronic performance of largearea graphene films remains unclear [16–19]. The particular graphene film microstructure required or sufficient for a given application is often not well defined. Additionally,

the graphene film microstructure can also influence its sensitivity to device processing steps. Air exposure of $SiO₂$ supported graphene films results in typically heavy p-type doping. This is due to charge transfer from adsorbed molecules including oxygen and water vapor, which act as charge trap states changing the charge carrier concentration available for conduction [20, 21]. These adsorbed molecules can further act as charge scattering centers, thus reducing the overall electronic mobility [22]. Atmospheric doping is rarely accounted in studies on GBs, but GBs might act as preferential adsorption sites due to their enhanced chemical reactivity [23], thus amplifying unintentional doping effects. Device fabrication also commonly encompasses direct contact of graphene layers with polymers, such as poly (methylmethacrylate) (PMMA), during transfer and during lithography steps. Complete removal of such polymers from the graphene surface has proven to be difficult [24, 25], and polymer residues can affect both the doping and mobility of the graphene [25–28]. However, the effect of PMMA and atmospheric contamination is difficult to separate as PMMA acts as an absorbent layer for vapors, significantly increasing their effect [29]. Moreover, polymer residues have been observed to preferentially adhere along GBs [30, 31], again highlighting how such contamination effects interlink with the graphene microstructure. 2018 **Solidi B published Exchange Co.** No. You Website the status Solidi B published by WILEY-VCH VERTIC-THE CONSULTER CONSULTER CONSULTER CONSULTER CONSULTER CO

A common strategy to protect graphene layers from some of these detrimental factors is to encapsulate it with a high-k dielectric, such as atomic layer deposited (ALD) alumina (AI_2O_3) [32, 33]. Direct ALD onto SiO_2 supported graphene films has been shown to reduce unintentional doping by passivating charged impurity scattering sites (mainly OH^- group at the SiO_2 – graphene interface) and by acting as a gas barrier against atmospheric dopants [32].

Here, we specifically explore the effect of the average grain size of the graphene CVD film on GFET device characteristics before and after encapsulation by Al_2O_3 . The ALD encapsulation allows us to decouple the effects of atmospheric and substrate doping (which are reduced during encapsulation), from the effects of GBs and polymer residues. We compare transport properties of polycrystalline graphene with average grain dimensions of the order of $10-20 \mu$ m, representing common commercial CVD films, to graphene with an order of magnitude larger grain sizes of $100-400 \,\mu m$, achieved by lowering the CVD nucleation density using the same Cu catalyst. Our data show that such larger average grain size offers significant advantages in terms of processability.

2 Experimental Graphene CVD was performed in a cold wall reactor (Aixtron Black Magic Pro) using Cu catalyst foil $(25 \mu m)$ thick, Alfa Aesar purity 99.98%). The graphene grain size was controlled by varying the annealing phase, CH4 pressure, and growth time. We focus on two types of polycrystalline graphene films, referred to from here onwards as type A and B. For both types the Cu foil was initially slowly heated to 1065 °C in a mixed H_2/Ar environment (50/200 sccm) at 100° C min⁻¹. Once the

Figure 1 SEM images of graphene grains on Cu foil for different growth conditions, type A (a) and type B (b). The red line outlines a single graphene grain with typical diameter, L_G . The change in nucleation density and resulting grain size is clearly visible between type A and type B.

growth temperature was reached, the Cu foil was kept in H2/Ar (50/200 sccm) for 120 min for type A and 30 min for type B, respectively. Graphene was subsequently grown in an H₂/Ar gas environment (26/250 sccm) using 7 (9) sccm of CH4, for 4 h for type A and 45 min for type B, respectively. Samples were cooled in 250 sccm Ar to room temperature. The total pressure at all process stages was 50 mbar.

Separate calibration runs were performed under identical growth conditions, but with the growth stopped before a continuous graphene film formed. Figure 1 shows scanning electron microscopy (SEM) analysis of the nucleation density and shape of graphene grains for the type A and B recipes, respectively. Type A samples show a low nucleation density (16 grains per $mm²$), resulting in a grain size, L_G , ranging from 100 to 400 μ m, whereas type B samples show a much higher nucleation density (1600 grains per mm²) and thus smaller L_G , ranging from 10 to $25 \mu m$.

The graphene films were then transferred to 300 nm $SiO₂/Si$ wafer support using a wet transfer method with PMMA as sacrificial transfer layer and ammonium persulfate as Cu etchant. After transfer, the PMMA layer was removed using acetone and IPA. GFET device structures were fabricated by optical lithography. Graphene channels with an equal length and width of $25 \mu m$ were defined by oxygen plasma etching and Ni (60 nm) electrodes were then deposited by sputter coating and subsequent lift-off. The encapsulation was carried out by depositing 80 nm Al_2O_3 at 120 °C with a standard atomic layer deposition (ALD) recipe using TMA and water precursors in alternating pulses.

All electrical measurements were performed in ambient conditions at room temperature using a Keithley 4200 semiconductor characterization system. In total, seven devices were measured for both types A and B.

3 Results and discussion Figure 2 shows a schematic of the fabricated three terminal FETs. Figure 3a and b shows representative measured transfer characteristics of sample types A and B, whereby a bias voltage $V_{ds} = 10 \text{ mV}$ was applied between the source–drain contacts and the gate voltage V_G on the Si substrate was swept at a rate of 1 V s^{-1} .

Figure 2 Schematic of the three terminal FET for type A and B graphene devices.

All as-fabricated (unencapsulated) samples show doping levels with Dirac point voltages (V_{CNP}) around 40 V, but type-B samples exhibit significantly lower average currents and hence lower mobility (μ) values. Figure 3c highlights the variation of hole mobilities for these devices with statistical means of $\mu_h(A) = 1887.58 \pm 259.5 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ and $\mu_h(B)$ $= 443.47 \pm 84.09 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ for sample types A and B,

respectively. The observed mobility values are in the range of reported mobilities for CVD graphene on $SiO₂$ substrate and defined device dimensions [16–19]. This can be rationalized by comparing the average graphene grain size, (Fig. 1), to the device channel length. For type A samples, L_G exceeds the channel length, hence a GB-free path across the channel can be expected (Fig. 2). In contrast, for type B samples carriers will have to cross multiple GBs through the channel (Fig. 2). Our results, therefore, indicate that charge carriers scatter at the GBs, lowering their mobility.

Figure 3a and b also shows the comparison of the devices after the graphene channel was covered by 80 nm ALD Al_2O_3 . Interestingly, despite identical processing conditions, the effects of the encapsulation are quite different for the two types of samples. Encapsulated type A samples show a $V_{\text{CNP}} \sim 0 \text{ V}$ and symmetric, ambipolar transfer curves. In contrast, for type B samples doping levels

Figure 3 Typical $I_{ds}-V_G$ curves for the type A (a) and type B (b) before and after encapsulation. The distribution of the hole mobility (c) and Dirac point voltages (V_{CNP}) (d) before and after encapsulation for both grain size samples. The boxes show the interquartile range (from the 25th to the 75th percentile) and the mean (dashed line) and median (solid line), the patterned boxes correspond to the data from the unencapsulated samples and the unpatterned boxes to the encapsulated samples. The whiskers indicate the 1st and 99th percentile and the " \times " the minimum and maximum.

Figure 4 A schematic representation of the detrimental possibilities discussed in the text for sample A and B before (a,b) and after (c,d) encapsulation, respectively. The black line shows a graphene layer on a $SiO₂$ substrate with atomic roughness less than 1 nm. The multiple dashed lines in Al_2O_3 denote the amorphous nature of the film.

remain high with V_{CNP} values above 15 V. Figure 3c and d shows the device to device variation in hole mobility and V_{CNP} for type A and B devices. While the encapsulation process leads to higher mobility values, such improvement is much more significant for type A samples.

In order to rationalize these observations, Fig. 4 schematically shows a cross-sectional view of the graphene channel highlighting the various interfaces and potential contaminations and defects. It is well known that the $SiO₂$ support is not atomically flat (compared to h -BN) and in addition its surface always contains large number of $OH^$ bonds. Furthermore, polymer process residues preferentially attach to the graphene at defects, wrinkles, GBs, etc. Thus more polymer contamination of the graphene surface is expected for samples with a higher GB density. The ALD encapsulation process will drive off adsorbed molecules and lower the concentration of OH^- groups at the graphene interface. Since such adsorbants are known to act as scattering centers, their removal will increase the average graphene mobility, as seen in Fig. 3. The deposited Al_2O_3 layer will act as a gas barrier, protecting the graphene from subsequent ambient exposures and deleterious doping, consistent with our observation of V_{CNP} around 0 V for encapsulated type A samples. In addition, the deposited high-k dielectric also helps to screen the Coulomb scattering of the remnant charge impurity centers for electrons [34–36], hence the increase in electron conduction in both types of samples that we observe (Fig. 3a and b).

However, we have not performed additional processes to clean the graphene surface (such as annealing in inert ambient), and our processing is prone to leaving polymer residues onthe graphene. Such polymer contamination can act as heterogeneous nucleation sites for the ALD process, and hence significantly affect the barrier and dielectric properties of the ALD Al_2O_3 layer. In addition, it can also trap initial adsorbants including air and water molecules, which are encapsulated below the ALD layer and lead to device performance variations. The major difference between type A and B type samples here is the higher GB density for the latter, which makes type B samples more susceptible to polymer contamination and consequently makes it harder to directly grow athin, high-quality ALD layer. HencetypeB samples do

not show any drastic improvements in their transport properties (Fig. 3). Sagade et al. [32] highlighted the importance of the quality of the graphene $-$ Al₂O₃ interface in determining the ultimate device performance. Our results suggest that polymer contamination and grain boundaries may have additional effects on other device characteristics such as hysteresis and long-term stability that would be of particular interest for future work.

4 Conclusions We studied integrated manufacturing pathways for GFETs relevant to a wide range of device applications from photodetectors to bio-sensors. We focussed on the effect of the average grain size of the graphene CVD device layer, statistically comparing GFET device characteristics before and after ALD dielectric deposition on the graphene. Our study thereby does not target mobility superlatives, but reliable, reproducible transport characteristic and mobility values exceeding $1000 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ on commonly used SiO_2 support. Independent of any direct effect of GBs on the graphene film properties, our data clearly shows that graphene films with larger average grain size offer significant process advantages. In particular, they are less prone to attract process polymer contamination and allow more homogenous, higher-quality thin ALD films to be grown directly onto them. Current commercially available large-area CVD graphene films often have average grain sizes less/or similar than that of our type B graphene film. Our results motivate that an increase in average graphene grain size to above $100 \mu m$, corresponding to more than an order of magnitude increase relative to current commercial films, should be targeted for large area graphene film applications. 2016 Second of the Company of the Company

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