A thermalization energy analysis of the threshold voltage shift in amorphous indium gallium zinc oxide thin film transistors under positive gate bias stress

K. M. Niang,[1] P. M. C. Barquinha,[2] R. F. P. Martins,[2] B. Cobb,[3]

M. J. Powell,[4] and A. J. Flewitt[1,a]

1. Electrical Engineering Division, Cambridge University, J J Thomson Avenue, Cambridge CB3 0FA, United Kingdom

2. i3N/CENIMAT, Department of Materials Science, Faculty of Science and Technology, Universidade NOVA de Lisboa and CEMOP/UNINOVA, Campus de Caparica, 2829-516 Caparica, Portugal

3. Holst Centre/TNO, High Tech Campus 31, 5656AE Eindhoven, The Netherlands

4. 252, Valley Drive, Kendal LA9 7SL, United Kingdom

ABSTRACT

Thin film transistors (TFTs) employing an amorphous indium gallium zinc oxide (a-IGZO) channel layer exhibit a positive shift in the threshold voltage under the application of positive gate bias stress (PBS). The time and temperature dependence of the threshold voltage shift was measured and analysed using the thermalization energy concept. The peak energy barrier to defect conversion is extracted to be 0.75 eV and the attempt-to-escape frequency is extracted to be 10^7 s^{-1}. These values are in remarkable agreement with measurements in a-IGZO TFTs under negative bias illumination stress (NBIS) reported recently (A. J. Flewitt and M. J. Powell, J. Appl. Phys. 115, 134501 (2014)). This suggests that the same physical process is responsible for both PBS and NBIS, and supports the oxygen vacancy defect migration model that the authors have previously proposed.

[a] Author to whom correspondence should be addressed. Electronic address: ajf@eng.cam.ac.uk .

Amorphous indium gallium zinc oxide (a-IGZO) has been widely recognized as a promising alternative to hydrogenated amorphous silicon (a-Si:H) for the semiconducting channel in thin film transistors (TFTs) for display applications. This is due to the high field effect mobility, high transparency, and possibility of low temperature deposition which makes a-IGZO suitable for flexible substrates such as plastic and paper.[1,2] Particular attention has been paid to TFT stability which is vitally important for commercial exploitation. In devices fabricated with a high-quality gate dielectric and low defect density interfaces, a-IGZO TFTs exhibit a positive shift in the threshold voltage (V_{th}) under positive bias stress (PBS),[3-5] a negative shift under a negative gate bias illumination stress (NBIS),[6,7] and almost no shift under negative gate bias in the dark. Possible mechanisms for threshold voltage shifts include a change in the defect distribution in the channel semiconductor or charge trapping in the gate insulator and/or at the insulator-channel interface. The time and temperature dependence of the threshold voltage shift during stress and recovery has been generally fitted to a stretched exponential model, where the time constant and the stretch parameter have been extracted.[3-7] These values vary largely owing to the different stress conditions used. Moreover these parameters do not directly offer further insights into threshold voltage shift mechanisms and additional electrical measurement[7] or device simulation[5] are often employed in an attempt to gain some further physical understanding.

On the other hand, a thermalization energy analysis allows two parameters with some physical interpretation to be extracted from bias stress data: the distribution of energy barriers to the bias stress process, and an associated attempt-to-escape frequency which is related to charge carrier localization.[8] Such an analysis has previously been used to describe a microscopic model for defect creation which explains the threshold voltage shift in a-Si:H TFTs under bias stress.[9-11]

The concept of the thermalization energy starts with the assumption that a material contains a number of sites which may be converted into defects by some means (a gate bias, for

example). Each site has a particular energy barrier to the conversion process, and so the material as a whole will have a distribution of energy barriers, $D(E)$. An attempt is made to overcome this energy barrier at each site ν times per second, and this is known as the attempt-to-escape frequency. To a first-order approximation, after a time, *t*, and at a temperature *T*, all the states with an energy barrier less than or equal to the thermalization energy,

$$E_{th} = k_B T \ln(\nu t) \quad (1)$$

will have been converted to defects (i.e. sites with the lowest energy barrier are statistically likely to be converted most quickly). Here, k_B is the Boltzmann constant. In this way, the time and temperature dependence of the threshold voltage shift is correlated to energy and that energy can be represented in a distribution curve. The maximum of this distribution is a measure of the energy barrier to the threshold voltage shift process and ν is the frequency of the attempts made to overcome this barrier.

Recently, Flewitt and Powell applied this analysis to a-IGZO TFTs under NBIS. They extracted an energy barrier of 0.65 – 0.75 eV and an attempt-to-escape frequency of 10^6 – 10^7 s^{-1}, and based on these results they proposed an oxygen vacancy defect migration model to explain the threshold voltage shift process in a-IGZO TFTs under NBIS which they suggested should be valid for PBS also.[12] However, their work did not include a thermalization energy analysis of experimental PBS data; this is the subject of this paper.

The a-IGZO TFTs subjected to PBS have a bottom-gate structure consisting of a 30 nm a-IGZO channel layer deposited by rf magnetron sputtering from a 2:1:2 In_2O_3:Ga_2O_3:ZnO target and 200 nm PECVD SiN_x deposited at 180 °C. The source and drain contacts are made from a Ti/Au double layer deposited by e-beam evaporation, while the gate electrode is a 100 nm thick sputtered Mo layer. The back channel of the TFTs is passivated with a spin-coated SU-8 layer.

The channel width and length are 90 μm and 15 μm respectively (W/L = 6). The device operates in accumulation mode with a threshold voltage of 1.1 V, a field effect mobility of 37 $cm^2\ V^{-1}\ s^{-1}$ (at V_{DS} = 0.1V), a switching ratio over 10^9 and a sub-threshold slope of 0.3 V dec^{-1}. Before the bias stress experiments, the devices were annealed at 200 °C for 1 hour in order to equilibrate the defect density in the channel material. The gate transfer characteristics of the devices were then measured at room temperature using a Wentworth probe station inside a Faraday cage with a HP4140B dual voltage source picoammeter. The device was then heated to the bias stressing temperature using a low noise HP6642A DC power supply and resistive heater. The temperature was measured with a K-type thermocouple. An electric field of 1 MV cm^{-1} over and above the threshold electric field was then applied across the gate insulator in order to have the same bandtail carrier density in all samples during bias stressing. The drain-source current, I_{DS}, was measured as a function of time whilst applying a drain-source voltage, V_{DS}, of 0.1 V. A low V_{DS} was used to minimize any perturbation to the uniform field in the dielectric layer produced by the stressing gate-source voltage, V_{GS}. Gate transfer measurements were performed at the start and end of each bias stress measurement, and measurements were made at temperatures of 65, 85 and 105 °C for times up to 80,000 s. Between measurements at different temperatures, the device was annealed again at 200 °C for 1 hour with no applied bias to restore its initial conditions. It should be noted that the same device was used repeatedly to give the bias stress data presented to allow straightforward comparison, although many measurements have been made of a number of such devices.

Figure 1 shows the gate transfer characteristics of the a-IGZO TFT at the start and end of the bias stress performed at 65, 85 and 105 °C. The drain-source current measured as a function of stressing time is shown in the inset of Fig. 1. At 65 °C, the threshold voltage, which is ~1 V

initially, is increased to the stressing voltage of 20 V after ~80,000 s. As expected, increasing the temperature decreases the time taken to reach the stressing voltage, taking only ~ 50,000 s at 85 °C and ~ 10,000 s at 105 °C. The parallel transfer curves above threshold before and after the stress measurements indicate that no degradation of the device occurs due to bias stress (i.e. there is no structural change in the a-IGZO material).

Figure 2 shows the normalised threshold voltage shift, $\Delta V_n(t)$, as a function of gate bias stressing time. $\Delta V_n(t)$ is defined by

$$\Delta V_n(t) = \frac{V_{th}(t) - V_{th}(0)}{V_{th}(\infty) - V_{th}(0)} \qquad (2)$$

where $V_{th}(t)$ is the threshold voltage after some stressing time t, $V_{th}(0)$ is the threshold voltage before stressing and $V_{th}(\infty)$ is the value to which the threshold voltage is tending after a long stressing time. The normalised threshold voltage shift can in turn be presented as a function of energy using Eq. 1 as shown in Fig. 3(a). The fit parameter, ν, is determined by systematically trying different values for ν in Eq. 1 and replotting the $\Delta V_n(t)$ data as a function of energy. If the value for ν is incorrect then the $\Delta V_n(t)$ curves for the three temperatures will not overlap. Figure 3(a) shows that an optimal overlap occurs for $\nu = 10^7$ s^{-1} in this study. Also shown as a solid line is the stressing data fitted to a stretched hyperbola [9]

$$\Delta V_n(t) = 1 - \left[\exp\left(\frac{E_{th} - E_A}{k_B T_0} \right) + 1 \right]^{-2} \qquad (3)$$

where E_A and $k_B T_0$ represent a measure of the characteristic energy barrier for the process and the width of the energy distribution. As the threshold voltage shift is a cumulative process (all sites with an energy barrier less than or equal to E_{th} are converted), then the distribution of energy barriers $D(E)$ is obtained in Fig 3(b) by differentiating the curves in Fig. 3(a). A peak value E_{max} of 0.75 eV and a full width at half maximum ~0.1 eV are obtained. These values are compared

with those previously extracted for NBIS in a-IGZO in Table I. The most remarkable feature of these results is that the attempt-to-escape frequency and peak energy are the same for both processes. This suggests that the same fundamental mechanism is responsible in both cases.

The authors have previously considered the processes that might be responsible for bias stress effects in a-IGZO TFTs, and set out five key features that any microscopic model must explain. [12] With some minor refinement in the light of the quantitative thermalization energy analysis of PBS experimental data in this study, these are:

1. a negative shift in the threshold voltage occurs for negative gate bias and a positive shift occurs for positive gate bias;

2. illumination with light is required to induce a negative threshold voltage shift, whereas positive threshold voltage shifts occur both with and without illumination;

3. the threshold voltage shift is metastable, and the rate of shift is strongly temperature-dependent in the range from room temperature up to ~400 K when structural changes are not occurring;

4. the energy barrier to the instability mechanism is ~0.75 eV; and

5. there is an attempt-to-escape frequency of $\sim 10^7\ s^{-1}$ associated with the instability process.

The authors then proposed an oxygen vacancy migration model. The key feature of the model is that, unlike in a-Si:H, the threshold voltage shift in a-IGZO TFTs is not due to a defect creation process, but to a change in the energy distribution of states in the band gap upon defect migration. Under PBS, the field-induced electrons encourage the conversion of charged V_O^{2+} oxygen vacancy states in the upper part of the band gap to uncharged V_O oxygen vacancy states in the lower part of the band gap, with the energy barrier to the process being caused by the need for an oxygen 2– ion to migrate through an intermediate interstitial state. The number of defect states in the lower part of the band gap (called D_e states) is increased while those in the upper

part of the band gap (called D_h states) is decreased by the same amount. The process may be summarised as

$$D_h^{2+} + [O(—M)_n + 2e] \rightarrow D_h^{2+} + O_i^{2-} + D_e \rightarrow O(—M)_n + D_e \quad (4)$$

where $O(—M)_n$ is an *n*-coordinated oxygen atom neighbouring the D_h site, $[O(—M)_n + 2e]$ represents electron localization close to such a site, and O_i^{2-} is an oxygen ion migrating through an interstitial (barrier) site. This rearrangement of the defect pool affects the Fermi level and, in this case, the increase of states in the lower part of the band gap pulls the Fermi level away from the conduction band when the gate bias is removed, thus resulting in a positive threshold voltage shift, as observed experimentally. The reverse process (which is dominant in NBIS) is expressed as

$$D_e + [O(—M)_n + 2h] \rightarrow D_e + O_i + D_h^{2+} \rightarrow O(—M)_n + D_h^{2+} \quad (5)$$

Carrier localization close to the defect migration site is always necessary. Under no bias and in equilibrium, the reaction rate of both processes in Eq. 4 and 5 are the same, and so there is no change in the net distribution of defect states in the band gap. However, under PBS, the positive gate bias moves the Fermi level towards the conduction band edge, resulting in the increased occupation of conduction band tail states, which are localized states, and the process in Eq. 4 is favoured over that in Eq. 5. D_e sites are formed at the expense of D_h sites. Under NBS, the Fermi level remains in the upper part of the band gap due to the high charge neutrality level, and so hole localization, as required in Eq. 5, does not occur, and no change in the defect distribution results. It is only upon illumination that the quasi Fermi level for holes is moved into the lower part of the band gap and hole localization occurs, leading to a negative threshold voltage shift, as observed experimentally.

As shown pictorially by the authors in Fig. 4 of Ref. 12, the barrier to defect redistribution is always the movement of an oxygen atom or ion through an interstitial site in this

model, and this should determine the energy barrier for the process. The peak in the energy barrier distribution for NBIS and PBS is extracted to be ~0.75 eV in both cases, but there is a difference in the width of the energy distribution for the two cases. The full width at half maximum (FWHM), which is ~k_BT_0, is ~0.1 eV in PBS but ~0.25 eV in NBIS (Table I). A key difference between the two processes in the vacancy migration model is that PBS requires the movement of an O^{2-} ion whereas in NBIS the migrating oxygen atom is uncharged. Robertson and Guo have used *ab initio* modelling to calculate the oxygen interstitial formation energy for the most stable position in a-IGZO.[13] The formation energy of an uncharged interstitial is ~0.6 eV and is independent of the Fermi energy, whereas that for the interstitial with a 2– charge varies with Fermi energy from a maximum of ~0.6 eV. This suggests that the charged ion is more sensitive to variations in local disorder, and that this results in the greater width of the energy distribution for NBIS compared with PBS, but the magnitude of the energy barrier is similar, as measured in this work.

The observation that the attempt-to-escape frequency is also approximately the same for PBS and NBIS (~10^7 s^{-1}) suggests that the charge localization length for both processes (Eqs. 4 and 5) is similar. The measured attempt-to-escape frequency is approximately a factor of 10^6 smaller than phonon frequencies (~10^{13} s^{-1}), and so localization volume is larger by a similar factor compared with the volume of space occupied by an electron in a bond, meaning that localization length is increased by ~10^2. Therefore, assuming bond lengths ~0.1 nm, this gives a localisation length ~10 nm for both processes.[8] Kamiya *et al.* have investigated carrier transport in disordered amorphous oxide semiconductors.[14] They find that transport is best described by a percolation model in which carriers have to overcome barriers to conduction of varying height which are separated by a characteristic length, L_i. Their observations suggest that L_i must be much greater than the mean free path of the carriers, which is less than ~1 nm for electrons.[14]

Our experimental results are consistent with this model and we conclude that the localized electrons and holes in the [O(—M)$_n$ + 2e] and [O(—M)$_n$ + 2h] states are both confined by the same spatial regions, between the transport barriers, defined by L_i. Therefore, the localization length and hence measured attempt-to-escape frequency for both NBIS and PBS are the same.

In conclusion, stressing of a-IGZO TFTs under positive gate bias (PBS) has been performed, and a thermalization energy analysis applied to extract quantitative information about the energetics of the process involved. Both the energy barrier and attempt-to-escape frequency extracted for PBS are the same as the values extracted in a previous analysis of NBIS data. This suggests that the same microscopic process is responsible for both effects. This is consistent with an oxygen vacancy migration model for instability in a-IGZO TFTs that has been previously proposed by the authors. The model is also consistent with the increased width of the distribution of energy barriers for NBIS compared with PBS that is measured.

The research leading to these results has received funding from the European Community's 7th Framework Programme under grant agreement NMP3-LA-2010-246334. Financial support of the European Commission is therefore gratefully acknowledged. The work has also received funding from FEDER through the COMPETE 2020 Programme and National Funds through FCT–Portuguese Foundation for Science and Technology under the Project No. UID/CTM/50025/2013.

[1] E. Fortunato, P. Barquinha, and R. Martins, Adv. Mater. **24**, 2945 (2012).

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature **432**, 488 (2004).

[3] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, Appl. Phys. Lett. **93**, 093504 (2008).

[4] M. E. Lopes, H. L. Gomes, M. C. R. Medeiros, P. Barquinha, L. Pereira, E. Fortunato, R. Martins, and I. Ferreira, Appl. Phys. Lett. **95**, 063502 (2009).

[5] K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, Appl. Phys. Lett. **95**, 013502 (2009).

[6] M. D. H. Chowdhury, P. Migliorato, and J. Jang, Appl. Phys. Lett. **98** (2011).

[7] M. D. H. Chowdhury, P. Migliorato, and J. Jang, Appl. Phys. Lett. **102**, 143506 (2013).

[8] R. B. Wehrspohn, S. C. Deane, I. D. French, and M. J. Powell, Thin Solid Films **383**, 117 (2001).

[9] S. Deane, R. Wehrspohn, and M. Powell, Phys. Rev. B **58**, 12625 (1998).

[10] R. Wehrspohn, M. Powell, S. Deane, I. French, and P. Roca I Cabarrocas, Appl. Phys. Lett. **77**, 750 (2000).

[11] R. B. Wehrspohn, S. F. Lin, A. J. Flewitt, W. I. Milne, and M. J. Powell, J. Appl. Phys. **98**, 054505 (2005).

[12] A. J. Flewitt and M. J. Powell, J. Appl. Phys. **115**, 134501.1 (2014).

[13] J. Robertson and Y. Guo, Appl. Phys. Lett. **104**, 162102 (2014).

[14] T. Kamiya, K. Nomura, and H. Hosono, Appl. Phys. Lett. **96**, 122103 (2010).

Type of TFT	Type of Stress	ν [s^{-1}]	E_{max} [eV]	k_BT_0 [eV]
a-IGZO BG TFT	PBS	10^7	0.75	~0.1
a-IGZO BG TFT	NBIS	$10^6 – 10^7$	0.65 – 0.75	~0.25

Table I. Comparison of the attempt-to-escape frequency, peak energy and width of the distribution of energy barriers to the threshold voltage shift process for a-IGZO bottom gate (BG) TFTs under PBS (data from this work) and NBIS (data from Ref. 12).

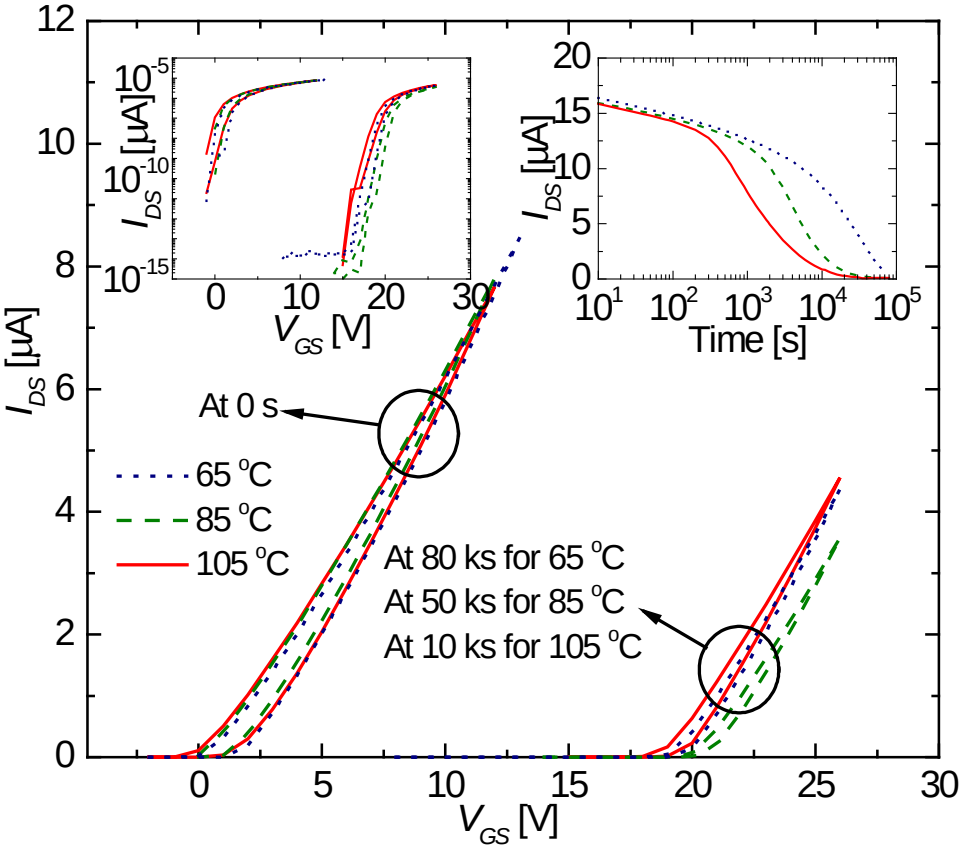

Fig. 1. Gate transfer characteristics before and after gate bias stressing of a-IGZO BG TFTs at temperatures of 65, 85 and 105 °C. Shown inset left is the same data plotted on a logarithmic current axis and shown inset right is the corresponding drain source current, I_{DS} as a function of bias stressing time.

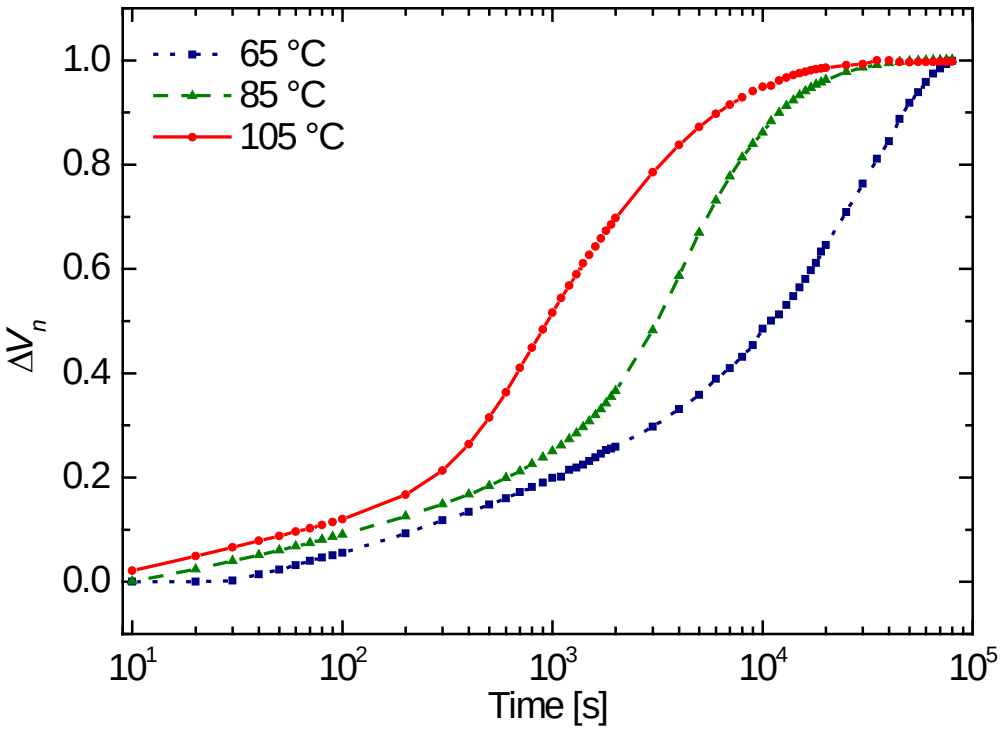

Fig. 2. The normalised threshold voltage shift as a function of bias stressing time at temperatures of 65, 85 and 105 °C.

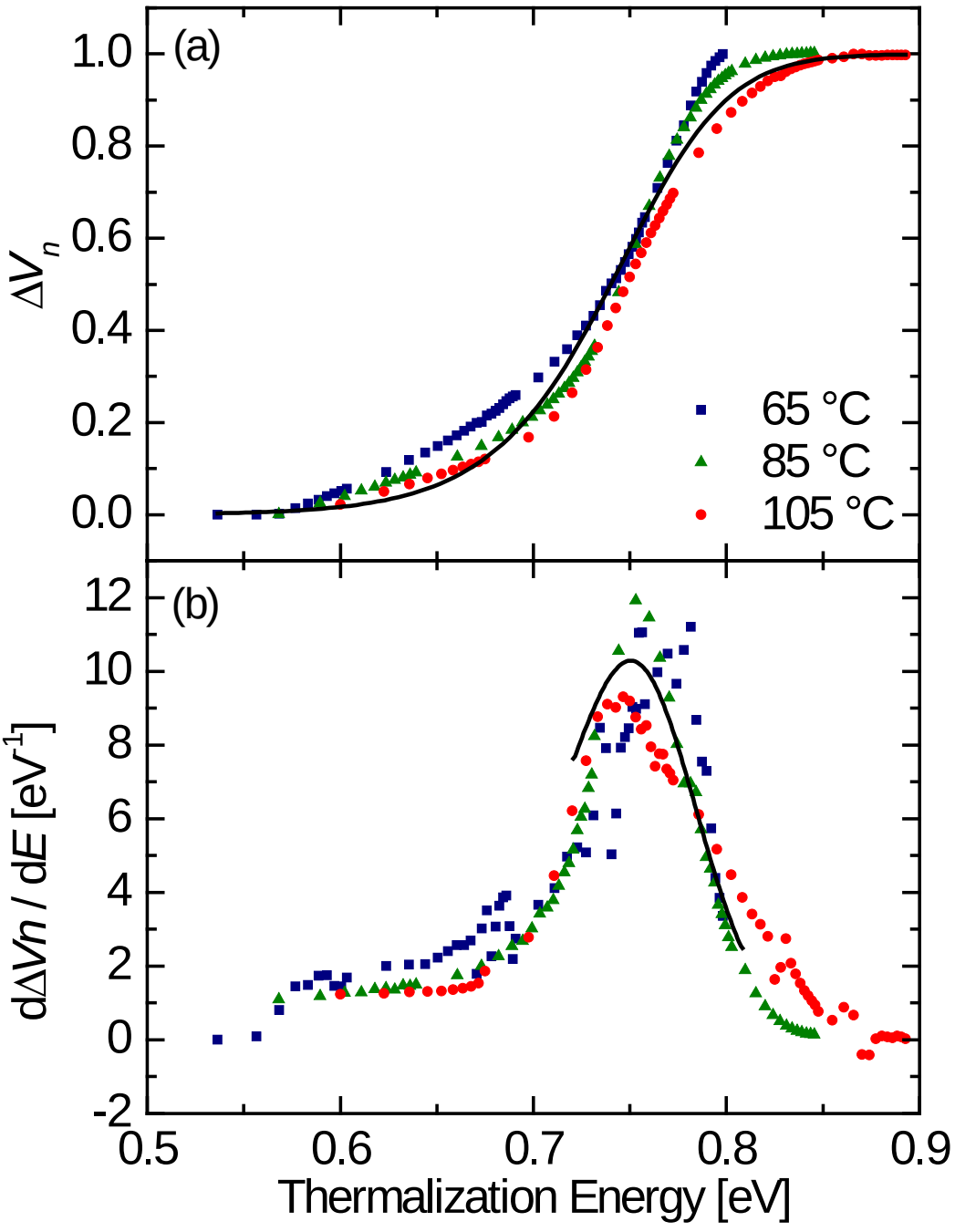

Fig. 3. (a) The normalised threshold voltage shift as a function of thermalization energy at temperatures of 65, 85 and 105 °C. The optimal overlap is achieved with an attempt-to-escape frequency, $\nu = 10^7$ s^{-1}. The solid line is a fit ($R^2 = 0.982$) based on a stretched hyperbola. (b) shows the corresponding derivatives with respect to the thermalization energy. The solid line is a fit based on the derivative of a stretched hyperbola.