Extremely Uniform Tunnel Barriers for Low-Cost Device Manufacture

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***Abstract*— We report on the final steps needed to achieve the level of control over the properties of single tunnel barriers of AlAs needed to allow the manufacture of high-volume low-cost microwave and millimeter-waves detectors. We achieve a 1% standard deviation of the current–voltage characteristics across 2-in wafers and average currents from different wafers varying by 1%, when modeling shows that a monolayer error in the AlAs barrier layer thickness would result in a 270% change in the same electrical characteristics.**

***Index Terms*— Semiconductors, tunnel devices, molecular beam epitaxy, manufacture.**

I. Introduction

WHEREAS quantum confinement and hot electron injection using heterojunctions has resulted in commercially successful electronic devices (quantum well lasers, high electron mobility transistors, heterojunction bipolar transistors and heterojunction Gunn diodes), electron tunneling through one or more thin barrier layers has not yet been commercialized [1]. There are many prototype devices using tunneling and resonant tunneling as the basis of their operation have been demonstrated on a one-off basis that exhibit superior figures of merit for computing and both microwave and optical communications, but they have so far not been exploited because the required level of reproducibility for high-volume low cost manufacture (typically less than 5% variation about a pre-specified mean for electronic device characteristics) has never been demonstrated [1]. This is particularly important as some of these devices are potential components for low power systems of the type needed for pervasive sensor networks.

The asymmetric spacer layer (ASPAT) diode, which incorporates a single tunnel barrier of AlAs in a crystal of GaAs with an asymmetric doping profile, shares the same detectivity of a Schottky barrier, but has several other advantages: (i) zero bias operation, (ii) very low added noise, (iii) much reduced sensitivity to ambient temperature, (iv) wide dynamic range with especially a high sensitivity to low incident powers, and (v) a high resistance to pulse burn-out [2], [3]. One reason for the lack of manufactured devices has been the inadequate control over the crystal growth process to achieve the very high yield to the very tight tolerances needed to allow pick-and-place technology to be used in making hybrid circuits. We have recently produced devices with a less than 1% variation in the average dc I-V characteristics between wafers, and a 1% standard deviation of the same dc I-V characteristic within wafers for square devices of 30μm to 100μm side. This is well below the variability normally tolerated for discrete devices in hybrid circuits, which is typically 3-5%.

TABLE I
THE MBE LAYER SEQUENCE

Layer	Thickness (nm)	Doping (cm^{-3})
7 GaAs	300	$4x10^{18}$
6 GaAs	5	$4x10^{17}$
5 GaAs	5	Undoped
4 AlAs	2.84	Undoped
3 GaAs	100	Undoped
2 GaAs	5	$4x10^{17}$
1 GaAs	350	$4x10^{18}$
0 GaAs	Substrate	n^+

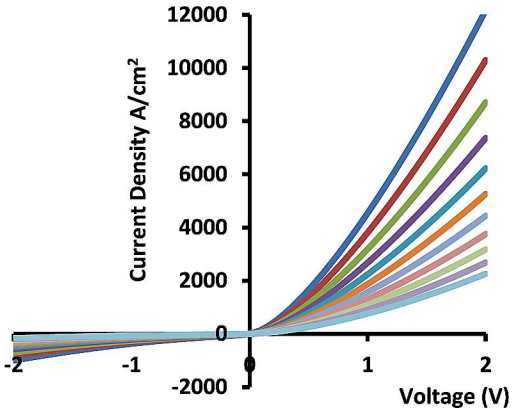

Fig. 1. Current-density voltage characteristics of a GaAs/AlAs/GaAs diode showing the extreme sensitivity to the thickness between 9 (top) and 11 (bottom) monolayers of the AlAs layer in forward bias in increments of 0.2 monolayers.

II. Theory

The tunneling probability for electron transport through a barrier is exponentially sensitive to (i) the height of the barrier (ii) its width, and (iii) the energy at which it is incident on the barrier [4]. For the structure given in Table 1, the

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simulations in figure 1 show how the I-V characteristics of a diode vary as the thickness of the AlAs barrier varies from 9 to 11 monolayers, with a drop of 270% for every extra layer of AlAs, and an increase in current of 5% for every one percent of GaAs that alloys with AlAs in the barrier layer. The barrier height is determined by details of the semiconductor band-structures and is ∼1eV here, involving the X-valley in AlAs and the Γ valley in GaAs. These simulations used the Silvaco© ATLAS commercial package.

In the last 2 decades, a great deals of attempts at controlling the tunnel barrier for this device were made. Initial results showed 300% current variations from device to device from different wafers, mainly due to inadequate control over the layer thickness [5]. Because of the superior level of in-situ diagnostics in an MBE machine we have focused for the last 20 years on this technology [5], [6]. By introducing a sacrificial calibration layer, it was possible to get this wafer to wafer variability down to less than 50%, and the in-wafer variation to 30%, still not good enough [7].

A detailed study of tunneling electrons has given us the key insight [8]. Using the analysis of electron microscopy images [9], we have a coherence area for tunneling electrons given by

$$S_c = l_c^2 = (\pi/16)(h/m^* v_t)^2$$

where h is Planck's constant, l is the coherence length, m* is the electron effective mass and v_t is a measure of the transverse electron velocity of the tunneling electron at the point of the last collision can be approximated here by the lateral thermal velocity $m^* v_t^2 = kT$, where k is Boltzmann's constant and T the absolute temperature in Kelvin, which for GaAs, with $m^* = 0.067 m_e$, gives $l_c = 0.15\mu$m, or about ten times the de Broglie wavelength of the tunneling electron (given by λ=h/p where h is Plank's constant and p the electron momentum). This means that any given electron is sampling and averaging compositional variations occurring on a scale smaller than 0.15μm diameter in deciding what are the local thickness and height of the barrier. Variations on scales larger than 0.15μm diameter in local thickness and height of the barrier would be observed as variations in the tunneling current. It is quite possible to have a large (up to 300%) variation in current from device to device if there are incomplete layers on either side of the AlAs barriers on a lateral scale larger than 0.15μm, and electrons would locally be sampling between 9 and 11 monolayers. The individual layers on either side of each GaAs/AlAs interface need to have the same average thickness everywhere on the wafer at a scale of 0.15μm or larger to within <2% to eliminate this form of variability.

III. Experimetal Results

We have previously focused on a technique to achieve the very sharp interfaces between completed layers, and we recently reported being able to achieve very high wafer-to-wafer [10] and the run-to-run [11] reproducibility of this diode. There was a remaining 20% linear variation of the current from devices across the wafer (caused by a 0.06 monolayers maximum variation in the AlAs layer thickness) which we could attribute to the geometry of the growth machine – the AlAs cell is off axis and the three wafers rotate in their own plane during growth [10]. The simulations fit the data for 10.0 monolayers, and the lack of device-to-device variability indicated that the problem of incomplete layers had been eliminated at both interfaces. The growth conditions for the tunnel diodes were designed to ensure both electronic quality and uniformity of the high band gap AlAs material. In particular the growth rate for the barrier was kept at around 0.2 A°/sec and the Arsenic to Al flux ratios was kept closer to 1 to ensure stoichiometric growth conditions which we have demonstrated to lead to very high quality materials even at low growth temperatures [11]. These are the key attributes for both uniformity and reproducibility of the tunnel diodes reported here.

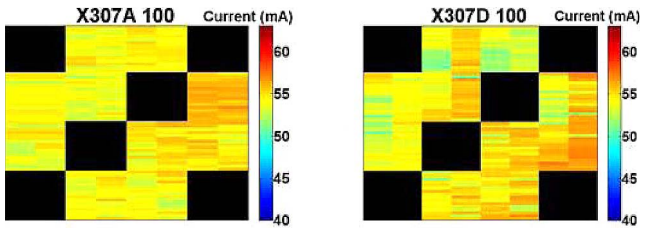

Fig. 2. Wafer maps showing the current measured on (∼320) 100μm square diodes at a forward bias of 0.5V. Note the extreme uniformity compared with those reported in (3) and (8). For both wafers, the standard deviation of the currents across the wafer is of order 1% of the average current, and the average currents from the two wafers agree within 1%. The black fields are unprocessed wafer regions. Note: seven wafers were grown on a platen at a time in a configuration of a central wafer (D above) and six around it (of which A is one): hence the claim of uniformity equivalent to a single 8" wafer. The black spaces are fields protected for further use. The mask has 10 subfields each with 32 diodes of 100μm square, all of which have been measured: there is one mesa measured per pixel in the diagrams above.

The key result reported in the letter is taking this process to a production MBE machine capable of growing over an 8" wafer. We have now refined our design to achieve greater microwave detection efficiency, and repeated our process using a larger production machine: a RIBER V100HU (HU=High Uniformity). Our new results (see Figure 2) have eliminated the cross-wafer variation, and have a standard deviation of 1% in the current-voltage characteristics across and between wafers grown at the same time. In order to achieve these results we have focused on growing as complete monolayers at both AlAs/GaAs interfaces as is possible across the growth front.

Devices were fabricated on three 2-inch substrates simultaneously using a full wet-etched process. Epitaxial layers were first etched into fields of square mesa diodes using a non-selective ortho-phosphoric based etchant H_3PO_4:H_2O_2:H_20 (3:1:50) to isolate the ASPAT. Front and back alloyed ohmic contacts consisting of 50nm AuGe, 12.5nm Ni and 200nm Au were then thermally evaporated and annealed at 410 °C for one minute. This provided a low (∼0.10Ω·mm) contact resistance as determined from Transmission line Method (TLM) characterization study. The full-wafer layout consisted of a total of 16 fields, with 6 left intentionally blank for future testing studies. Within the 10 used fields, a total of 456 devices with a mesa dimension of 100×100 μm^2 down to 5×5 μm^2 were available to be manually measured for this study.

The standard deviation of the variation of the current-voltage characteristics between devices at the same position

on different wafers, as shown in [11, Fig. 2] was of order 4%: this form of comparison eliminates the cross-wafer variation obtained from the research MBE reactor geometry. Here the 1% variation is a major step forward, as this applies to all devices across all wafers. The device-to-device variation seen in earlier work without the extreme care we have taken to achieve full integer monolayers of AlAs is still absent. Historically, the efforts to generate a balanced pair of diodes for frequency multiplication have been limited by the ability to get two device performances within a few percent of each other: here any diode pair would be satisfactory.

IV. Conclusions

In terms of the simulations in Figure 1, the results are consistent with achieving a barrier thickness that is constant to within <0.1 monolayers across the wafers of 2" diameter, i.e. less than a 0.03nm in thickness variation seen by the tunneling electrons. We checked this out by calculating the tunnel barrier transmission coefficients on the basis that the tunnel barrier thickness was taken from a Gaussian distribution of half-width σ_t, and calculating the half-width of the resulting tunneling current σ_I, when averaged over the 10,000 coherence areas represented by 100μm square diode. The 1% value for σ_I is only possible if σ_t is less than 1% or 0.1 of a monolayer in ten monolayers. Preliminary TEM results indicate a barrier that is 2.83 ± 0.03nm with both interfaces extremely abrupt [12]: other metrology techniques do not have the precision or accuracy implied by the tunnel currents. Note smaller diodes at 60 μm^2 square show the same narrow distribution of currents, the useful millimeter wave diodes will have a diameter of order $<10\mu$m, and could yet still show a wider variability from limited size-dependent lithographical control. We think that this represents the limit that can be achieved by any known growth technique. It achieves an extreme aspect ratio of control in our samples of 1: 5×10^{11} for an 8" wafer. Our result also indicates that this device, and by extension other tunnel devices, are capable of the reproducibility required for low-cost manufacture.

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