# A 60-Channels ADC Board for Space Borne DBF-SAR Applications

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*Abstract*— A 60-Channels ADC (Analog to Digital Converter) board for space borne Digital Beam Forming (DBF) Synthetic Aperture Radar (SAR) applications is described. The purpose of the board is to digitize analog signals detected by a dual band SAR receiving array operating at X and Ka band. It contains 48 high speed ADCs, which sample synchronously the incoming data of the antenna front end at Ka band. Other 12 ADCs are used to sample the coming data from the X band antennas. The board is composed by an analog section, a digital section and a clock distribution network used to synchronize the ADCs. Output digital signals from the board are routed to digital boards were are processed in the Digital Beamforming Network (DBFN).

Index Terms—Radar, SAR, Digital beamforming, Data acquisition.

# I. INTRODUCTION

This paper presents a 60-channels ADC board for space borne Digital Beam Forming (DBF) Synthetic Aperture Radar (SAR) applications proposed in the project DIFFERENT. DIFFERENT is abbreviated of "digital beam forming for low-cost multi-static space-borne synthetic aperture radars". The project currently still in progress, is collaborated amongst several leading universities, research institutes and companies in Europe. The aim of DIFFERENT project is to develop a low-cost, low weight, highly integrated, dual-band (X & Ka) dual-polarized DBF-SAR instrument to overcome the limitations of current SAR systems and pave the way to small satellites formation flying missions.

# II. DBF-SAR ARCHITECTURE

To solve the existing problems of traditional SAR systems, a multi-static SAR system based on formation flying small satellites is proposed in DIFFERENT project [1] [2]. In this SAR system, the transmitting and receiving antennas are separated and mounted on separate satellites, enabling a lager freedom of operation and increasing the sensitivity due to the reduction of transmitter/receiver

switches. A shared-aperture, dual-band (X & Ka) dualpolarized radiation board is used in this project to guarantee a compact size, low cost SAR system. Radiating elements are integrated in a RF board with 60 MMICs (Monolithic Microwave Integrated Circuit). The function of each RF MMIC unit is to down-convert the received V- and H-pol signals to an intermediate frequency (IF) band. The downconverted signals are routed to the ADC board described in this paper. 60 ADCs (one for each channel) are integrated in the board. After digitization, the signals are routed to 6 digital boards were are processed in the Digital Beamforming Network (DBFN).



Fig. 1 ADC Board PCB stackup

# III. ADC BOARD ARCHITECTURE

The purpose of the ADC board is to digitalize the baseband signals provided by the RF board. A 10 layers PCB stackup (Fig.1) has been used to integrate Analog to Digital Converters (ADCs), distribution networks, filters, capacitors and connectors. The ADC board is composed by three sections: an analog section, a digital section and an area dedicated to power lines. High-speed digital signal lines have been routed separately on the upper layers of the stackup (digital section) to prevent coupling with RF carriers on the lower part of the stackup (analog section).

The baseband signals coming from the analog section are digitalized by 60 ADCs (Texas Instruments ADS5527)

integrated in the upper layer of the board. 48 ADC are used for the Ka-band channels and 12 for the X band channels. Proper synchronization between ADCs is guaranteed by a clock distribution network. Power lines have been routed on dedicated layers (layers L7-L8 in Fig. 1).

# A. Analog Section

The lower part of the board stackup (Fig. 1) is dedicated to the analog baseband signals coming from the dual band array printed on the RF board. The IF signals are routed from the RF to the ADC board by means of 6 RF/ADC connectors (Samtec ERF8). A low pass filter and a decoupling capacitor is used for each IF differential channel. Inside the board, the signals are routed to the upper layers using simple vertical vias. Fig. 2 shows one of the four analog sections at Ka band. Twelve analog IF differential signals are routed to twelve ADCs using equal length paths to guarantee phase coherence. Also two sections at X band are integrated in the ADC board. Each X-band section manages six channels.



Fig. 2 Analog part for Ka band (layer L10)



Fig. 3 Digital section at Ka-band. Different colors are used to show different layers (laers from L1 to L5 are shown)

# **B.** Digital Section

The upper side of the board stackup (Fig1) hosts 60 ADCs (48 for the Ka band and 12 for the X band). Texas Instruments ADS5527 have been used. Fig. 3 shows one digital section for the Ka band with 12 ADCs. The board

accommodates four sections at Ka and two at X band. Digital signals at the output of the ADCs are routed to the digital boards using FMC connectors. A multilayer distribution network of equal length striplines have been used to guarantee signals synchronization.

#### C. Clock Distribution Network

Clock coherence between the 60 ADCs is guaranteed through an integrated differential clock distribution network realized in microstrip technology on the upper layer of the ADC board. A star configuration (Fig. 4), with a clock generator (FXO-LC535-210) on the center, has been used to distribute a 210MHz Low Voltage Differential Signal (LVDS). Low Skew Differential Clock Distribution Chips (IDT 8516) have been used for power division. The clock signal has been delivered to 60 ADCs and to the 6 digital boards via the ADC/DGT connectors. Fig. 5 shows the simulated clock signal at the input of the ADCs.

### **CONCLUSIONS**

The architecture of a 60-Channels ADC Board for space borne Digital Beam Forming SAR Applications has been presented. The purpose of the board is to digitize the analog signals detected by the receiving antennas of the SAR. Output digital signals from the board are routed to digital boards were are processed in the Digital Beamforming Network (DBFN).



Fig. 4 Clock distribution network (microstriplines in layer L1 are shown).



Fig. 5 Simulated clock signal at the input of ADCs

# REFERENCES

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