ANALYSIS AND DESIGN OF A WIDE DYNAMIC RANGE PULSE-FREQUENCY MODULATION CMOS IMAGE SENSOR

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Abstract

Complementary Metal-Oxide Semiconductor (CMOS) image sensor is the dominant electronic imaging device in many application fields, including the mobile or portable devices, teleconference cameras, surveillance and medical imaging sensors. Wide dynamic range (WDR) imaging is of interest particular, demonstrating a large-contrast imaging range of the sensor. As of today, different approaches have been presented to provide solutions for this purpose, but there exists various trade-offs among these designs, which limit the number of applications. A pulse-frequency modulation (PFM) pixel offers the possibility to outperform existing designs in WDR imaging applications, however issues such as uniformity and cost have to be carefully handled to make it practical for different purposes. In addition, a complete evaluation of the sensor performance has to be executed prior to fabrication in silicon technology.

A thorough investigation of WDR image sensor based on the PFM pixel is performed in this thesis. Starting with the analysis, modeling, and measurements of a PFM pixel, the details of every particular circuit operation are presented. The causes of dynamic range (DR) limitations and signal nonlinearity are identified, and noise measurement is also performed, to guide future design strategies. We present the design of an innovative double-delta compensating (DDC) technique which increases the sensor uniformity as well as DR. This technique achieves performance optimization of the PFM pixel with a minimal cost an improved linearity, and

is carefully simulated to demonstrate its feasibility. A quad-sampling technique is also presented with the cooperation of pixel and column circuits to generate a WDR image sensor with a reduced cost for the pixel. This method, which is verified through the field-programmable gate array (FPGA) implementation, saves considerable area in the pixel and employs the maximal DR that a PFM pixel provides. A complete WDR image sensor structure is proposed to evaluate the performance and feasibility of fabrication in silicon technology. The plans of future work and possible improvements are also presented.

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Abbreviations

2-D	Two-dimensional
3-D	Three-dimensional
3-T	Three-Transistor
4-T	Four-Transistor
ADC	Analog-to-Digital Converter
AND	Logical conjunction
APS	Active Pixel Sensor
BSI	Back-Side Illumination
CCD	Charge-Coupled Device
CDS	Correlated-Double Sampling
CF	Conversion Factor
CG	Conversion Gain
CMOS	Complementary Metal-Oxide Semiconductor
dB	Decibel
DC	Direct Current
DDC	Double-Delta Compensating
DN	Data Number
DPS	Digital Pixel Sensor
DR	Dynamic Range
DSC	Digital Still Camera

DSLR	Digital Single-Lens Reflex
DSNU	Dark Signal Non-Uniformity
FD	Floating Diffusion
FF	Fill Factor
FOM	Figure of Merit
FPGA	Field-Programmable Gate Array
FPN	Fixed-Pattern Noise
fps	Frames Per Second
FSI	Front-Side Illumination
GBP	Gain-Bandwidth Product
HDR	High-DR
I/O	Input/Output
IC	Integrated Circuit
IR	Infrared
LSB	Least Significant Bit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
MTF	Modulation Transfer Function
NMOS	n-channel MOSFET
NOR	Logical Nor or Joint Denial
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PD	Photodiode
PFM	Pulse-Frequency Modulation
PMOS	p-channel MOSFET
PPS	Passive Pixel Sensor

PRNU	Photo Response Non-Uniformity
PWM	Pulse-Width Modulation
$Q_{\mathbf{FW}}$	Full Well Capacity
QE	Quantum Efficiency
QVGA	Quarter Video Graphics Array
r.m.s.	root-mean-square
SNR	Signal-to-Noise Ratio
SOC	System on Chip
SXGA	Super Extended Graphics Array
TDI	Time-Delay Integration
TSV	Through-Silicon Via
TTFS	Time-to-First-Spike
TTS	Time-to-Saturation
VHDL	VHSIC Hardware Description Language
VHSIC	Very-High-Speed Integrated Circuits
WDR	Wide-DR
XOR	Exclusive Disjunction
Σ-Δ	Sigma-Delta

1 Introduction

With the development of electronic imaging devices [1–10], the way that images are recorded has shifted from traditional films to semiconductor fabricated sensors. Every material used in semiconductor processes has an individual response to photons. When the photons reach the sensor, they penetrate into the material and are absorbed at different depths. The absorbed photons will release their energy to generate electron-hole pairs inside the material. The photodetector device is designed to separate the electrons and holes, and they are collected to form a photocurrent. Photocurrent is used as a measure of light intensity, and digital images can be generated from the information.

Compared with the film-based photograph, a digital image has the advantages of low cost and post-processing availability. However, the noise is much higher, even producing visible artifacts. Dynamic range (DR), the imaging range from the lowest detectable light intensity to the highest, is also comparatively low, so some details in dark or bright regions may disappear. Affected by these two factors,

the overall image quality becomes less attractive. For some specific scenes, the electronic imaging devices can not provide satisfying images.

Despite the good image quality, the film industry has almost disappeared in the 21^{th} century due to the high cost of film production and development. In contrast, there continues to be strong investment in research and evolution of electronic imaging devices. In this work, the CMOS image sensor will be discussed, and the focus is the strategy for DR extension. The objective is to provide new designs for high-DR (HDR) or wide-DR (WDR) CMOS image sensors using commercial CMOS technology.

1.1 About CMOS Image Sensor

1.1.1 Development

The history of CMOS image sensor began in the late 1960s when a photodiode operated in the accumulation mode was first reported [11, 12] with several other successful demonstrations [1, 13, 14]. Just shortly after these implementations and publications, another technology for image sensors, the charge-coupled device (CCD), arose and became a primary competitor [15, 16]. Since then, much research effort resulted in the commercial productions of both technologies, however the CCD has dominated and been massively manufactured, mostly due to its superior

image quality.

The dominance of CCD was not overtaken until less than a decade ago, when an implementation demonstrated a new pixel structure that was able to provide advanced noise cancellation technique in CMOS technology [17]. Consequently, this demonstration made the CMOS image sensor able to compete with the CCD in image quality. In addition, its capability of integration with CMOS chips is a huge advantage over the CCD since the cost to realize system on chip (SOC) is much lower. As a result, more research effort has been invested in the development of CMOS image sensor with a target of low-cost and high-quality devices for various usages. Currently, the shrinking dimensions of CMOS fabrication technology benefits the design of a smaller pixel, but issues due to the small components arise and have to be resolved to provide continually satisfactory performance.

1.1.2 Applications

CMOS image sensors are widely used in different applications, including consumer products, autonomous devices, and biomedical engineering. These cover a wide range of image sensors with low- and high-end requirements. In general, the low-end demands contain chips with low resolution or less quality, such as mobile devices (cell phone, tablet, laptop), surveillance and security cameras, and teleconference and broadcast camcorders. On the other hand, the high-end requirements usu-

ally come from digital cameras (DSC or DSLR), autonomous sensors (in robot or satellite), and biometric or medical imaging, which require a large resolution and sometimes better image quality. Fig. 1.1 consists of some typical applications for CMOS image sensors.

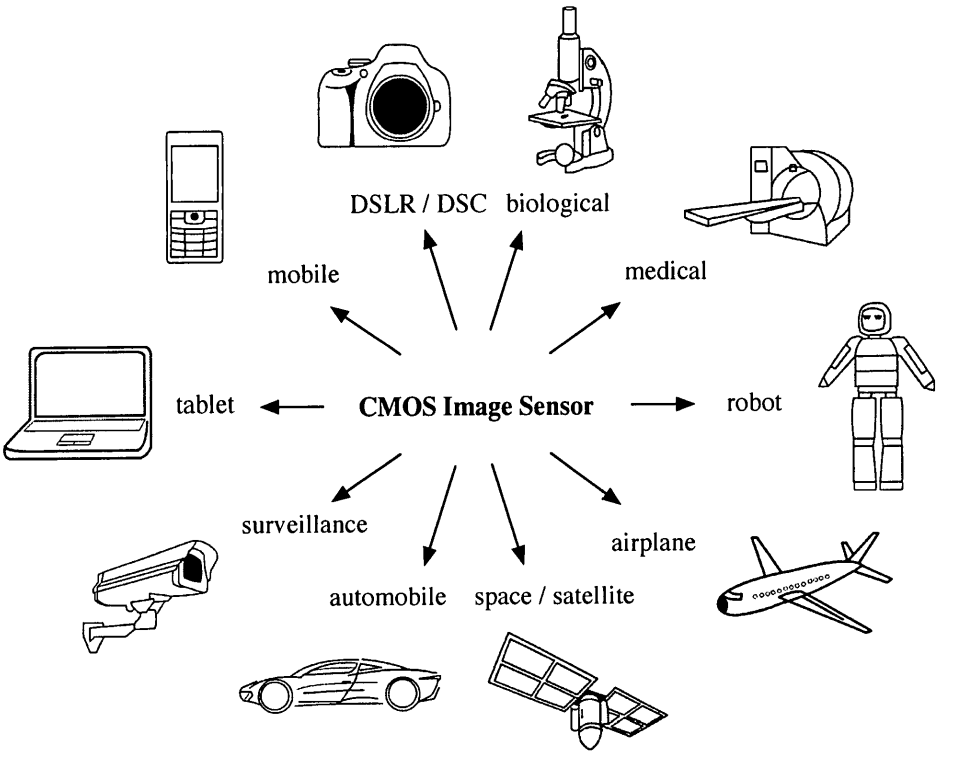


Figure 1.1: The applications of CMOS image sensor.

In addition to these common applications, there are also important but less obvious uses for CMOS image sensors, such as the linear scanning for industrial or machine vision and sensors on toys or small devices for specific purposes. In addition, infrared (IR) night vision, X-ray radiology, and range imaging (gesture

recognition) are also emerging fields of interest.

1.1.3 Current Trends

CMOS image sensors were successful in replacing the use of film and have become the most dominant device in the imaging industry. The reasons that it burgeoned are the low cost of production, the possibility to perform additional signal processing, and a very wide range of implementations to satisfy different application requirements. Although the available native DR is still lower than what film has achieved (typically between 80 to 100 dB [18]), it can actually be increased by different techniques, which will be reviewed in Chapter 2, to provide satisfactory DR. However, there exist drawbacks or inevitable trade-offs when using these approaches, which eventually degrades the overall sensor performance. The use of WDR imaging has become more common in many kinds of occasions recently, leading to an increasing demand for WDR image sensors. Even though other parameters, such as noise and frame rate, are still of concern, WDR imaging remains a priority target for the development of CMOS image sensors. Nevertheless, it is expected that different new approaches will still be introduced to provide a better solution for this issue.

1.2 Research Overview

The available pixel designs for WDR imaging have been presented by many researchers; in this work a frequency-based pixel, sometimes considered one type of digital pixel, is selected for this purpose. This choice is based on the parameters of interest and potential of performance improvement which will be discussed in the later chapter. Recently, a study by Wang et al. demonstrated the successful implementation of a frequency-based pixel with a DR of 130 decibel (dB) [19]. Although a large DR performance was achieved, this work considered only the measurement of transfer curve and lacked other important information for a CMOS image sensor. With the already presented work and demonstrated principle, a more complete analysis is necessary.

1.2.1 Goal Statement

Operational Analysis: The operation of a frequency-based pixel is characterized by its self-reset mechanism [19], however it has not been fully analyzed yet. In fact, this is important in terms of determining the achievable specifications and providing design optimization strategies. In addition, circuit modeling, which is useful to assist the design process, was also neglected in the earlier work and has to be addressed carefully.

Performance Optimization: Since the operation of frequency-based CMOS image sensor is not totally understood, the performance optimization, including but not limited to DR, was not previously reported. Since the applications of CMOS image sensors cover a large range, a sensor's performance has to be fully optimized according to the needs or requirements of each individual condition. So far, optimization methods have not been provided to exceed the current performance bottleneck or to improve some of them; therefore more detailed studies are still necessary.

Systematic Design: The pixel does not exist in isolation, but as part of a complete image sensor system. In order to fully realize the performance of the pixel at the system level, readout and other support circuitry must be carefully considered during the design phase. In addition, any possible performance-optimization methods have to be implemented in accordance with the system to support the principle of image sensor operation.

1.2.2 Research Strategy

This work will be performed starting from the transistor-level analysis and expanded to the whole-system architecture design to achieve WDR imaging. First, some analytical derivations or calculations are performed to verify the concept and

to identify important design parameters of a frequency-based pixel. DR and linearity will be investigated by both HSPICE simulations and practical measurements on fabricated sensors. In addition, some simplified circuit models will be derived to realize the causes of certain issues, such as signal nonlinearity and noise performance. At the same time, a technique to increase the sensor uniformity and DR will be proposed, and verified by conducting circuit design and Monte Carlo simulations. Next, a signal sampling method that minimizes the pixel cost while retaining the benefits of the frequency-based pixel will be designed and presented. Specifically, this method will consist of the column circuit design in conjunction with the pixel design to achieve the objective of WDR imaging. Lastly, some synthesized images from the proposed image sensor structure will help demonstrate its actual benefit toward imaging applications.

1.3 Contributions

The contributions of this work can be categorized into three groups: pixel-level analysis and modeling; methods to improve pixel performance; and a complete WDR image sensor structure which is able to demonstrate its outstanding characteristics. Each is briefly introduced as follows.

1.3.1 Analysis of Pixel DR, Linearity, and Noise

Important design parameters, including various current sources in a pixel, will be studied to find their influences on DR, and the simulation-extracted results are used to support the analysis. The root cause of signal nonlinearity is explained and understood starting from the detailed operation of pixel to the modeling derivation. In addition, the effects from different comparator reference voltages will also be taken into consideration to find the optimized operation. Noise measurements are performed as well to establish a noise model that helps quantify the noise response of the pixel.

1.3.2 Technique for Performance Improvement

Sensor uniformity is a primary challenge in the frequency-based pixel design, therefore an improvement technique is designed in the pixel level to reduce the offsets of the main sources of non-uniformity. This technique is intended to improve the sensor uniformity to an acceptable level by compensating for the comparator offset between every two integrations. In addition, it also serves to improve the DR and linearity. Since this technique increases not only the uniformity but also the linearity, the subsequent signal processing is simplified.

1.3.3 Complete WDR Image Sensor Structure with Innovative Multiple-Sampling Method

A new sampling technique for the frequency-based pixel is proposed in order to achieve the goal of WDR imaging with an efficient pixel (in terms of smaller size and better circuit usage). This sampling method is composed of two-level samplings, where one is in the pixel and the other is in the column; each of them is further split into two parts to generate a total of four samplings. Consequently, the multiple-sampling technique achieves more than 100-dB DR to provide a sufficient imaging range. Moreover, a complete image sensor structure, including the proposed techniques, is designed to evaluate the expected performance of this work for future implementation in silicon technology. Lastly, the specifications of different modified versions of this structure are also discussed to address the flexibility of this design.

1.4 Thesis Organization

This thesis is organized as follows. Chapter 2 reviews the important parameters related to performance targets for image sensors. In addition, the primary WDR imaging techniques are also briefly introduced and compared to develop the background and motivation of this research. In Chapter 3, the complete study of the

frequency-based pixel is presented, including the constraints of DR, modeling of pixel operation to address linearity, and noise measurement. In addition, design suggestions will be given. Chapter 4 provides an innovative circuit design technique to improve the sensor uniformity and DR, which is demonstrated with thorough simulations. Following is the efficient multiple-sampling technique applied to the frequency-based pixel in Chapter 5, demonstrating the designs of pixel and column circuits to realize WDR imaging. Measurement results of implementation in a field-programmable gate array (FPGA) are presented as well to support the feasibility of this structure. In Chapter 6, a whole image sensor architecture is presented, combining the conclusion of previous analysis and techniques, to evaluate the performance that will be achieved upon implementation in silicon technology. Finally, the conclusion of this work and suggested future work are summarized in Chapter 7. The work which is used to support the selected research subject is presented in Appendix A.

2 Review of WDR CMOS Image Sensors

A CMOS image sensor is a specific division of IC design with important parameters related to not only circuitry but also optical aspects. In this chapter, a brief background review is presented to introduce the fundamentals of CMOS image sensors. After that, those important parameters are briefly mentioned and some visual examples are included to illustrate those phenomena. Popular WDR imaging techniques used in CMOS image sensors are introduced as well. A comparison in terms of those important parameters is presented to provide the background of further work.

2.1 Background

2.1.1 Photodetector

Semiconductor materials are used to detect photons by their photo-sensitive characteristics. In common CMOS technologies, a junction constructed by p-type and n-type materials has a region which is depleted [20]. The depletion region is formed

when the free holes in p-type material and free electrons in n-type material diffuse across the junction. The holes diffuse into the n-type region and leave negatively charged ions in the p-type region, and the reverse applies to the electrons. Therefore, the depletion region (or space-charge region) is created and a built-in potential results.

The depletion region and built-in potential are utilized to create the photodetector [2, 11]. When a photon is absorbed anywhere near the depletion region, a separation of electron-hole pairs may occur, and the potential will determine the direction of movement (or flow) of electrons and holes. In order to illustrate the process of photocurrent formation, a cross-section of p-n junction is shown in Fig. 2.1. Some photons reaching the depletion region are absorbed, transferring their energy to outer-shell electrons and generating electron-hole pairs. The built-in potential then forces the holes to move toward the p-type region and the electrons toward the n-type region, and the moving holes and electrons result in an electrical current which is called the photocurrent. With different photon densities, different magnitudes of photocurrent are generated, and they are further used to represent the pixel signal.

In order to utilize a p-n junction as a photodiode, its bias condition has to be carefully chosen. Fig. 2.2 shows a sketch of the current-voltage (I-V) curves with two different conditions (dark and illuminated) for a p-n junction. Three modes

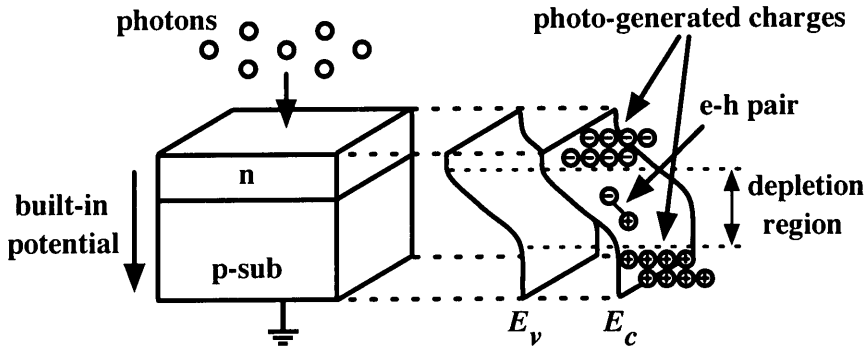


Figure 2.1: A cross-section view of p-n junction and the band diagram. The separated electrons and holes form the photocurrent.

can be observed, which are the avalanche [21–23], photodiode [11, 12], and solar cell [24, 25] modes. The p-n junction normally operates in the photodiode mode to serve the need of a pixel or an image sensor. When the photodiode is in darkness, the net current (flowing from p-type to n-type region) is negative but very close to zero. This non-zero current is mostly the thermally activated diffusion current of the junction, usually called the dark current. When it is illuminated, the absolute net current becomes larger because of the photocurrent, i.e. I_{ph}, which is subject to change with different amounts of electron-hole pairs generated and separated by the built-in potential. According to this diagram, the p-n junction has to be reversely biased to operate as a photodiode. Note that the junction will be in the avalanche mode if the reverse bias is too large, or in the solar cell mode if it is less than zero.

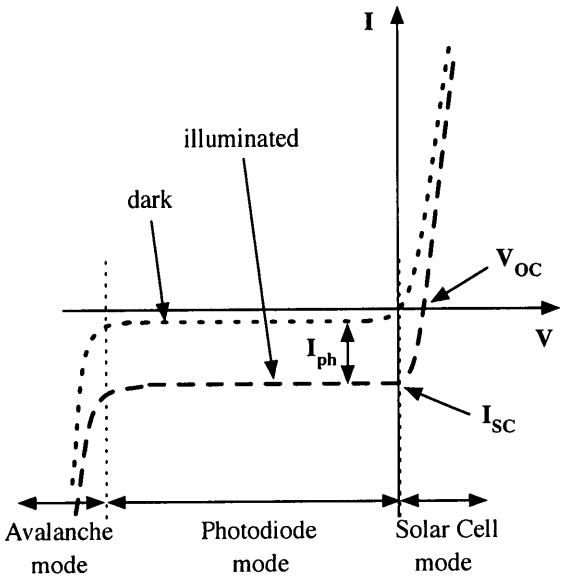
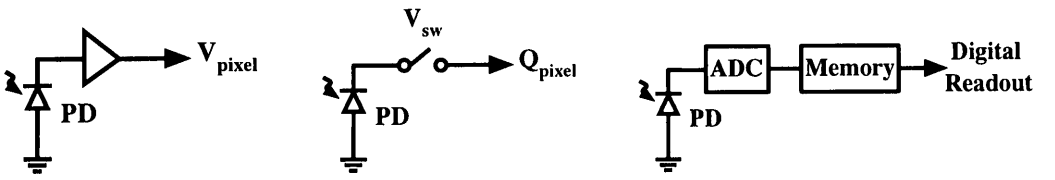


Figure 2.2: The I-V curves of a p-n junction photodiode in dark and illuminated condition. V_{OC} and I_{SC} are the open-circuit voltage and short-circuit current when there is illumination applied, respectively.

2.1.2 Pixel

A pixel is the fundamental element of a CMOS image sensor, and the imaging array normally contains a large number of pixels (usually in 2-D) to capture images. Inside the pixel are one photodetector and the necessary circuit to perform signal readout and/or processing. Depending on the principle of pixel operation, it can be referred to as an active pixel sensor (APS) [10, 26], a passive pixel sensor (PPS) [11], or a digital pixel sensor (DPS) [4, 27]. The block diagrams of these structures are shown in Fig. 2.3.

The APS usually equips the pixel with an amplifier or a buffer, which must be



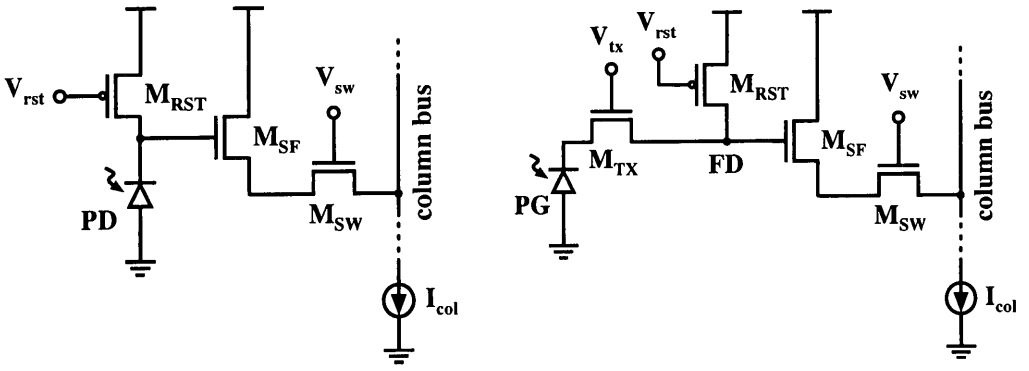
(a) (b) (c)

Figure 2.3: The block diagrams of (a) APS, (b), PPS, and (c) DPS structures.

an active device and can be built with only one transistor (or MOSFET) or up to several. On the contrary, the PPS does not contain any active device except a switch (as a passive device) to transmit signal when selected. The DPS consists of more complex blocks, normally an analog-to-digital converter (ADC) or a sigma-delta (Σ-Δ) operand with a memory cell, to perform in-pixel signal processing. Since different pixel structures have different advantages and disadvantages, they are adopted according to individual design requirements.

Currently, most pixel designs use the APS structure which provides better noise performance and a smaller size. As such, two conventional APS structures are shown in Fig. 2.4, where Fig. 2.4(a) is the three-transistor (3-T) [10] and Fig. 2.4(b) is the four-transistor (4-T) APSs [17].

There are three transistors in common for both the 3-T and 4-T APSs, including the reset (M_{RST}), source follower (M_{SF}), and switch (M_{SW}) transistors. The function of M_{RST} is to reset the photodiode (PD) or floating diffusion (FD) after each



(a) (b)

Figure 2.4: The schematics of (a) 3-T and (b) 4-T APSs. I_{col} is used to provide bias current for M_{SF}.

charge integration. M_{SF} is a single-transistor buffer and the active device in the pixel. M_{SW} is used to connect the pixel signal to the column bus when it has to be read out. The extra transistor in the 4-T APS is the transfer gate (M_{TX}) which is used to separate the photodetector (sometimes a photogate, PG [6, 28], or pinned photodiode, PPD [17]) from the FD. It can be used to perform some advanced operations to reduce a few particular noise sources, such as the correlated-double sampling (CDS) technique [6, 29–32] to subtract part of the noise from reset phase.

In general, several concerns are linked to the pixel design, such as its size (pixel pitch), active region (where photons penetrate and get absorbed), and periphery effect. Fig. 2.5 is used to understand these issues by sketching a 3-D, 2 × 2 pixel model. First, the pixel size directly determines the image quality, where a smaller one often leads to more details in an image, and small size becomes a common goal

of designing a pixel. However, a smaller pixel usually has more issues to deal with, for example noise, sensitivity, crosstalk, and non-uniformity. In addition, the pixel in CMOS technologies contains not only the photodetector but also at least several transistors, where the ratio of active region and whole pixel area is defined as the fill factor (FF) and is displayed as a percentage. FF is a measure of the area that is able to receive photons in a pixel and therefore has obvious impact on the optical performance. When it is larger, the sensor's optical efficiency is higher. There is also optical (spatial) crosstalk between pixels for image sensor, which is due to the imperfection of light path causing unwanted refraction. This kind of refraction may make photons fall into neighboring pixels and get absorbed. In addition, there are also photo-electrons generated outside the depletion region which diffuse to the neighboring pixels for collection.

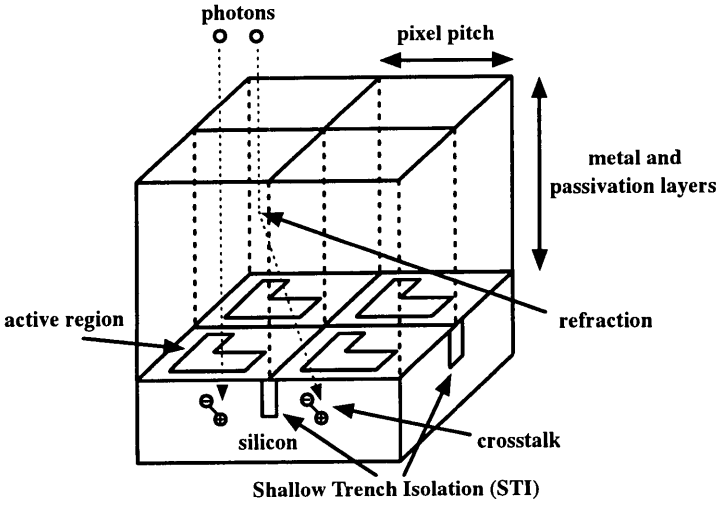


Figure 2.5: The illustration of concerns for pixel design.

2.1.3 CMOS Image Sensor System

CMOS image sensors are composed of three parts: the pixel array, signal access and control, and readout and processing circuits. A general image sensor block diagram is shown in Fig. 2.6. The pixel array has tens of thousands of pixels where each of them captures the photons injected into its photodetector and outputs a single signal according to the number of captured photons in the pixel area. An image is built with the combination of these spatially sampled signals. The access and control signals, normally including the row and column level, determine the operation of every pixel through the row lines and the signal readout procedure. The readout circuit, usually allocated row by row, accesses the signal from every pixel in the same row of the array through the read lines, or executes necessary calculations to reduce noise. In addition, the signal may continue with a column- or chip-level ADC to convert the analog signal into the digital domain. Finally, the signal is processed through auto-gain and other signal-processing units and output off-chip with the data buffers.

The typical pixel readout procedure is shown in Fig. 2.7. The operation modes of a CMOS image sensor include the rolling and global shutter modes, where the former has asynchronous integration times for each row and the latter integrates the signal of all pixels in a frame at the same time. In general, the rolling shutter

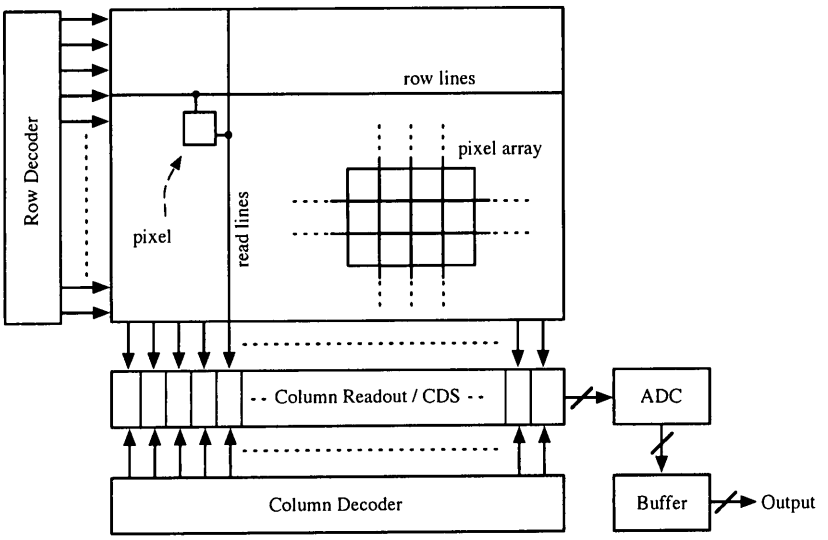


Figure 2.6: The block diagram of an image sensor, consisting of the pixel array, row and column decoders, column readout, signal processing (ADC) and output buffer.

mode comes with a lower pixel design complexity and a lower speed. The details of each imaging mode are explained as follows.

In the rolling shutter operation, the signal readout is executed row by row. In the figure, when row A finishes the integration and is being read out, each pixel of this row will be connected to its corresponding read line, and the readout circuit will read and store its data for final output. Meanwhile, row B is approaching its finish of its integration and all its pixels will be read out after all the signals of row A stored in the readout circuit have been completely acquired. Once the pixels of row B are connected to the read lines for signal readout, those of row A will move

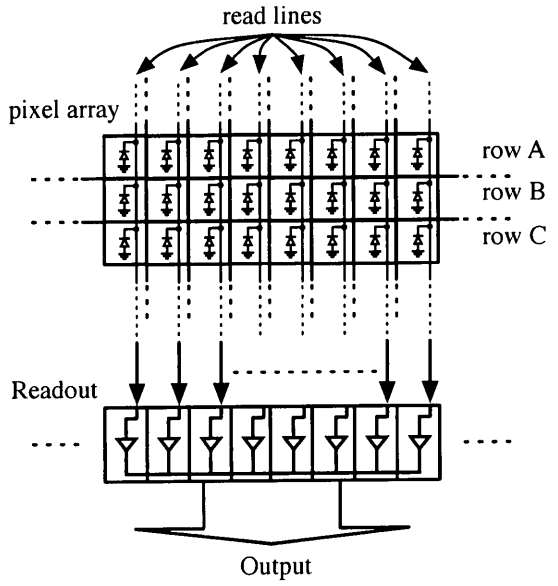


Figure 2.7: The block diagram of pixel array and the readout circuit, illustrating the readout procedure.

into the next integration stage for the following frame, and row C is approaching its finish of integration and becomes the next that will be read out. This process will start from the top of the array to the bottom in order to generate one single frame, and it repeats again to read out the next frame.

The readout procedure is much simpler for the global shutter mode. All pixels of the imaging array will start and finish their integrations at the same time, and individual data will be held in a storage of each pixel for readout (hence the pixel is more complex). The necessity of a more complex pixel design is due to the fact that the column readout circuitry can only handle the signals from one particular

row, thus each pixel requires additional circuit to preserve its captured signal. Nevertheless, the readout circuit will perform the same procedure as the rolling shutter mode to read out the entire pixel array.

In general, a rolling shutter mode is ideal for applications with no demand for capturing high-speed moving objects, since the shutter runs row by row and may create image distortion. In addition, it usually comes with a less complex pixel design. For imaging objects like flying birds or moving people, the global shutter mode offers a synchronous shutter that acquires information at the same (right) time. However, the cost is its larger pixel due to the requirement of additional storage in it. Although an off-array storage may prevent the use of a complex pixel, it is difficult to implement with a very large array since a large amount of signal lines is required and cannot be realized in layout.

2.2 Performance Overview

The important parameters of CMOS image sensors can be categorized into three groups: the image, circuit, and optics groups. In general, the DR, temporal (random) and spatial noise, and linearity are directly related to the image appearance and quality, whereas the frame rate, power, full well capacity (Q_{FW}), and conversion gain (CG) or conversion factor (CF) are related to circuit design; quantum efficiency (QE), sensitivity, and angular response are the optical performance that takes spec-

tral response into account. In this chapter, most of those image- and circuit-related parameters will be covered because this work is executed from a circuit-design perspective, while those affected by spectral response will be addressed in the last chapter.

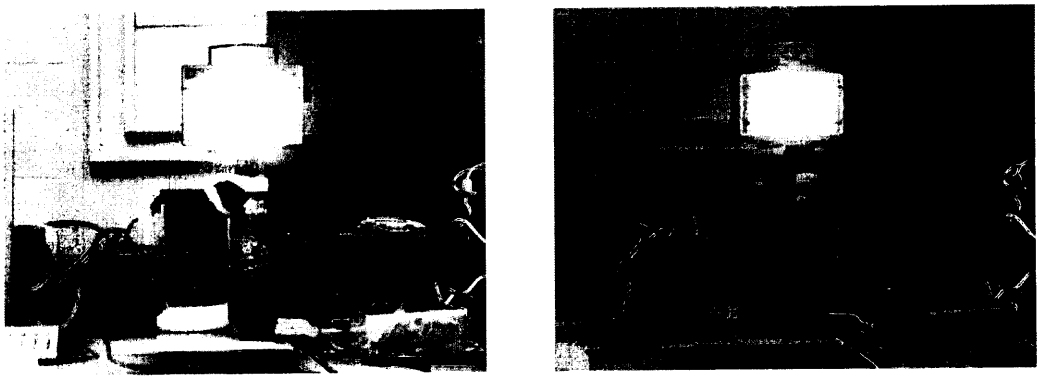
2.2.1 Dynamic Range

Since CMOS image sensors became popular about two decades ago, the study of WDR CMOS image sensor design has always been interesting to researchers due to its great potential of improvement. The DR in photography is typically defined as the luminance range of a scene being photographed; in a film or digital imaging system, it can be regarded as the limits of the recordable luminance range. Mathematically, it is used to represent the power ratio of the highest and the lowest detectable light intensities and is expressed in units of dB. Table 2.1 shows the illuminance range encountered in our living environment. According to the numbers, the maximum DR is more than 180 dB, which is greater than any existing sensors or even the human eyes. The difference between regular and WDR image sensors can be directly observed in the images shown in Fig. 2.8. In Fig. 2.8(a), the image shows a DR of 50 dB where the bright region (the bulb) is saturated; on the contrary, the same region is clearly captured in Fig. 2.8(b) where a DR of 100 dB is achieved. As a result, improving the DR of CMOS image sensors becomes necessary

for many applications, such as the biomedical imaging, automobile, security and surveillance, videoconference, and high-end photography.

Table 2.1: Illuminance of Living Environments

Illuminance (lux)	Condition
0.0001	Starlight
0.01	Quarter moon
0.1–1	Full moon
3–5	Twilight
50	Family room
80–100	Hallway
300–700	Office lighting
1,000	Overcast day
10,000–30,000	Full daylight
30,000–150,000	Direct sunlight



(a) (b)

Figure 2.8: Synthesized images (320 × 240) of a (a) regular and (b) a WDR image sensors, respectively.

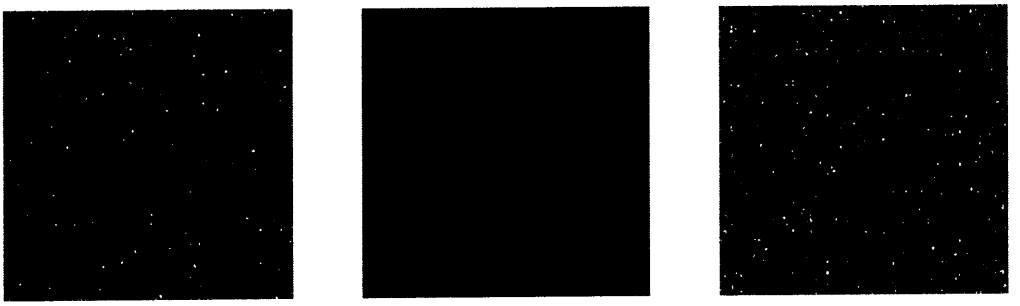
As of today, there are many designs featuring WDR imaging and providing over 100-dB DR. These sensors are usually categorized into six groups: (a) logarithmic

type, (b) multimode method, (c) clipping or well capacity adjustment, (d) global or local integration time adjustment, (e) time-to-saturation (TTS) or time-to-first-spike (TTFS) approach, and (f) pulse-frequency modulation (PFM) or pulse-width modulation (PWM). In later sections, the existing WDR imaging techniques for CMOS image sensors will be introduced separately to demonstrate their advantages and disadvantages on several important parameters. In addition, a comparison of them will also be summarized based on excerpts from the overviews presented in [33, 34] to provide the background for continuing study.

2.2.2 Temporal and Spatial Noise

In addition to DR, parameters such as the signal-to-noise ratio (SNR) and fixed-pattern noise (FPN) are also important because they play important roles in determining the image or video quality. The SNR of a CMOS image sensor is a ratio of the output- or input-referred signal to the equivalent temporal noise, and it is usually 30 to >50 dB with conventional designs. Generally, its visual impact can be seen in consecutive frames. FPN is one kind of spatial noise and has two components, including the dark signal non-uniformity (DSNU, illumination-independent) and photo response non-uniformity (PRNU, illumination-dependent), and can be seen in one single image with all pixels equally illuminated. In most cases, a value below one twentieth (1/20) of the temporal noise is desired to make this type of

noise invisible to human eyes. In Fig. 2.9, three images demonstrate the effects of temporal noise over the entire array [Fig. 2.9(a)], spatial noise across different columns [Fig. 2.9(b)], and a combining effect of two types of noise [Fig. 2.9(c)].



(a) (b) (c)

Figure 2.9: Simulated images (128 × 128) with the effects of (a) 20-dB SNR and (b) 5% column FPN, respectively. The combined result of previous two effects is shown in (c).

It is notable that in a real CMOS image sensor, FPN can be pixel-, column- or row-wise, depending on the design of pixel and the operation mode of the array. The example shown in Fig. 2.9(b) only assumes the column FPN, which is the most prominent FPN of current CMOS image sensors because of column-wise readout circuits. The pixel FPN is normally invisible when its value is significantly below the temporal noise, but it still depends on the pixel design and can be very large in some cases.

2.2.3 Linearity

The linearity of a CMOS image sensor is defined as the relationship between the output signal (data number, DN) and incident light intensity (number of photons). Since the output signal will be processed by an image processing unit (often a gamma correction) before displayed, its linearity is important to ensure the process of correction is accurate. In general, linearity is related to the photodiode characteristic under different bias conditions, in-pixel buffer, and column- or chip-level amplifiers. Fig. 2.10 illustrates the signal path and points out those affecting components or blocks. Currently, the nonlinearity is most prominent both in low-light conditions (due to the temporal noise) [35] and near saturation level (due to non-uniform photodiode capacitance) [36].

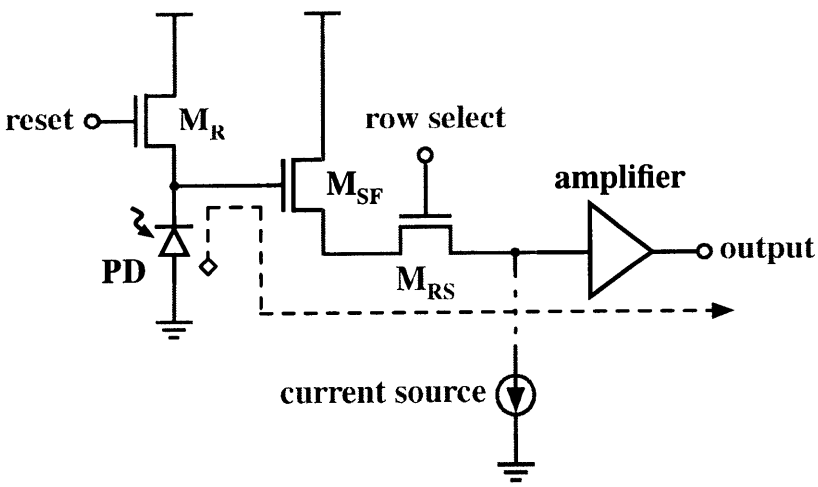


Figure 2.10: The signal path (dashed line) within a conventional CMOS image sensor. The black components are the primary causes of the signal nonlinearity.

2.2.4 Frame Rate

The use of CMOS image sensors covers a large variety of applications, including low-resolution recorders for purposes like on-the-fly videoconferencing and security surveillance, or high-resolution cameras such as digital single-lens reflect (DSLR), space exploration, and biomedical imaging. Since the frame rate requirement differs greatly between various applications, it is difficult to set a standard for frame rate. However, a 30–60 frames per second (fps) is normal for regular video purposes; furthermore, it can be up to more than 1,000 fps in some special applications. On the other hand, the frame rate can be as low as 3–5 fps or lower for specific and high-quality imaging systems where the target of interest is fixed or the quality of image is critical. Nevertheless, the common standard for frame rate of a typical image sensor is usually 30 fps for regular usage.

2.2.5 Other Circuitry Performance

The other pixel performances of interest include the Q_{FW}, CG or CF, dark current, and power consumption. Q_{FW} is used to represent the charge capacity of one photodetector, normally with a unit of electrons (e^-). Currently, this number is between 1,000 to 100,000 with regular CMOS technologies and depends on the actual pixel size (or photodetector active region). CG or CF is the conversion

ratio of the signal in voltage or DN to the collected electrons (V/e^- or DN/e^-). Normally, a large CG or CF provides a higher responsivity but with a smaller Q_{FW}. Dark current is the current generated without any illumination, demonstrating the internal noise component or minimum detectable signal of a photodetector, and it usually comes with a unit of ampere per photodetector area (A/cm^2). The figure of merit (FOM) for power consumption in CMOS image sensors is often calculated by dividing the total power consumption of one image sensor for one single frame by the number of pixel counts and can be represented as W/frame per pixel to evaluate the power consumption of each single pixel. Currently, the power FOM of CMOS image sensor is between 10 and 500 nW/frame per pixel, primarily depending on the pixel architecture.

2.2.6 Optical Performance

The optical performances of CMOS image sensors are normally presented with respect to spectral response. The wavelengths concerned are normally between 400 and 700 nm, i.e., within the visible-light spectrum of human eyes (390–750 nm) [37]. In particular, QE calculates the ratio of collected electrons to incident photons with different light wavelengths; sensitivity defines the electrical response of the pixel under a given illumination over a fixed period of time for white light (V/lux·s). For angular response, it measures the photo-response of the pixel with different angles

of incident light in the horizontal and vertical direction and is usually represented as a percentage with respect to the result with normal illumination.

2.3 Review of WDR Imaging Techniques

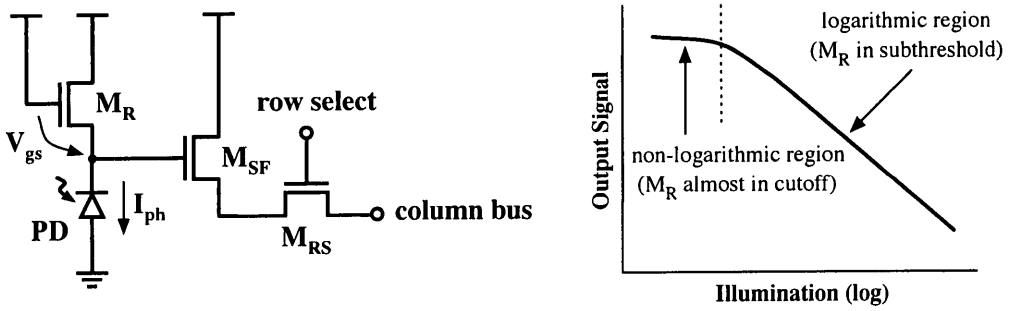
WDR imaging techniques have been studied and presented by many authors, using either the APS or DPS structures. Passive pixel devices are not typically used for WDR imaging design because of limitations due to their structure and poor noise performance. Therefore, only the APS is popularly used while some designs based on the DPS still exist for particular purposes. In this section, six different WDR imaging techniques are briefly introduced. The logarithmic, multimode, integration time adjustment, and clipping pixels are based on the APS, whereas the time-to-saturation or time-to-first-spike, and pulse-frequency or pulse-width modulation pixels can be considered as DPS when they are implemented to output a digital signal. The basic schematic or diagram of each technique will be shown and its operating mechanism will also be discussed.

2.3.1 Logarithmic Pixel

The logarithmic pixel, similar to the 3-T APS structure, was proposed to provide WDR imaging by using a current-mode pixel operation [38–42]. The only difference in circuit between the logarithmic pixel and 3-T APS is that the reset transistor is

replaced by a diode-connected NMOS, as M_{R} shown in Fig. 2.11(a). Since the reset control no longer exists, this pixel structure will function in a continuous manner where the photodiode is used as a current source. According to the photocurrent value, this diode-connected transistor will conduct the same amount of current and generate a corresponding gate-source voltage V_{gs} following the equation given by

$$V_{\mathrm{gs}} = \frac{nkT}{q} \cdot \ln \frac{I_{\mathrm{ph}}}{I_{\mathrm{s}}} + V_{\mathrm{T}} \tag{2.1}$$



(a) (b)

Figure 2.11: (a) A logarithmic pixel circuit schematic and (b) its photo-signal transfer curve. The non-logarithmic region is due to the non-ideality response of M_{R} when a very small current (photocurrent) conducts.

where k is the Boltzmann constant, T is the temperature in Kelvin, I_{ph} is the photocurrent, n is the ideality factor, I_{s} is the current at the onset of weak inversion, and V_{T} is the threshold voltage of M_{R}. As shown in Fig. 2.11, the relationship between the photocurrent and source voltage of M_{R} (or the gate voltage of M_{SF}) has a logarithmic response which compresses and converts a wide photocurrent

range of more than 10^5 magnitude, or 100 dB, into only several hundred mV or less. A typical photo-signal response of the logarithmic pixel is shown in Fig. 2.11(b), illustrating the logarithmic compression (the x-axis is in log scale).

The logarithmic pixel is a simple structure which features WDR imaging capability without using more than three transistors. Generally, a logarithmic pixel can reach a DR of more than 100 dB using current CMOS processes. However, the largest drawback is the higher noise response which leads to the visual artifacts in images. Since the V_{T} variation of M_{R} can be over 50 mV, the output signal directly suffers from a relatively large deviation. In addition, the photo-signal response is only about several tens of mV per illumination decade in the compressed region, so the contrast resolution is very poor (i.e. details may be lost). This issue is even more serious for the low-light region, as the figure shows. Another notable drawback is the temperature-dependent response which can be directly observed in (2.1). Briefly speaking, the logarithmic pixel achieves WDR imaging with a relatively simple design, but its image quality is difficult to improve under current technologies.

2.3.2 Multimode Pixel

The multimode pixel combines the operation of a 3-T APS and the logarithmic pixel together to extend the DR without dealing with the poor photo-signal response of

the latter. In general, the pixel functions as a 3-T APS when the pixel does not saturate; if it saturates under a strong illumination, it will switch to a logarithmic pixel which in general has a strong light detection capability [43–45]. The schematic of a multimode pixel can be the same as shown in Fig. 2.11(a) except the gate of reset transistor (M_{R}) is either connected to a low voltage (ground) or high voltage (V_{DD}) to facilitate both regular (linear) and logarithmic operations. It can also be modified to different structures according to specific requirements using six or seven transistors inside the pixel [39, 44, 46, 47]. A possible transfer curve of the multimode pixel is shown in Fig. 2.12, including two different operations.

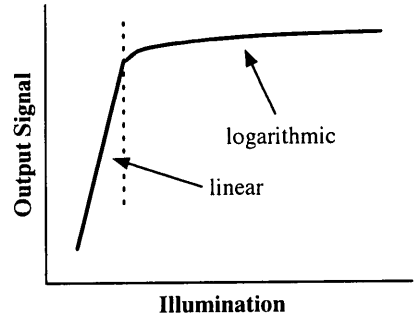


Figure 2.12: Transfer curve of a multimode pixel.

The multimode pixel combines the linear and logarithmic responses together, therefore the overall DR is easily extended to more than 100 dB. Generally, the low- to mid-light region is covered by the linear operation and up to 50–60 dB, and the high-light region will be supported by the logarithmic compression. However, the characterization of logarithmic response requires more effort in terms of image

or color reproduction which results in a higher cost of post-processing. As a result, this type of sensor can only be found in some monochrome applications. Moreover, determining the mode to be executed will require additional time or control circuits and signals, so the frame rate or power consumption is sacrificed. Nevertheless, the multimode pixel still provides a simple solution to WDR imaging applications without a complex pixel design and keeps an acceptable FF for small pixel design.

2.3.3 Global- or Local-Integration Time Adjustment Pixel

Techniques that incorporate the use of dual or multiple integration times in an image sensor to extend DR have been used by many authors [29, 31, 48–57]. Some of them have a globalized-control integration time [29, 49–54] and the others use a localized-control (or autonomous) integration time [55–57]. The concept of global-integration time adjustment pixel is to sample the pixel signal after a predefined integration time regardless of the amount of integrated charges in each pixel. By repeating the sampling method twice with one long and one short integration time or multiple times, the overall DR can be up to 121.8 dB [53]. On the other hand, the local-integration time adjustment pixel automatically adjusts the integration time of every pixel according to its received light intensity. In general, conditional reset circuitry is required for this type of sensor to sense when reset should occur.

The concepts of time adjustment pixels are further explained by the illustration

in Fig. 2.13, including the sketches for both types. In this figure, S_{H} is with a high illumination and S_{L} uses a low-light source. In addition, there are two integration times used in this example, including a long (T_{L}) and a short (T_{S}) period. In the curve of S_{H}, we notice it saturates within T_{L} due to a large photocurrent, thus its actual light intensity can not be acquired upon readout at T_1. However, this signal is then reset and re-integrates with a short integration time (T_{S}), and a recognizable output is finally generated (V_{H}) at T_2.

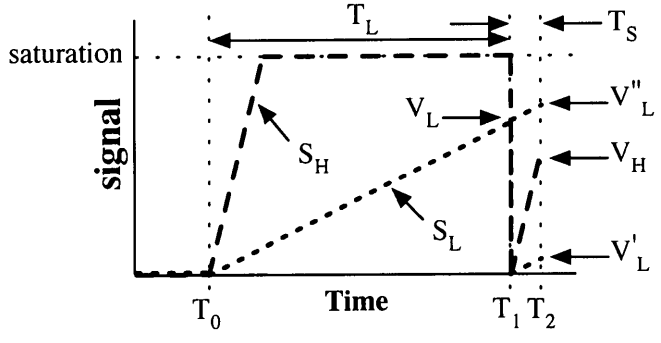


Figure 2.13: The concepts of global- and local-integration time adjustment pixels. S_1 and S_2 are integration voltages with low and high light, respectively.

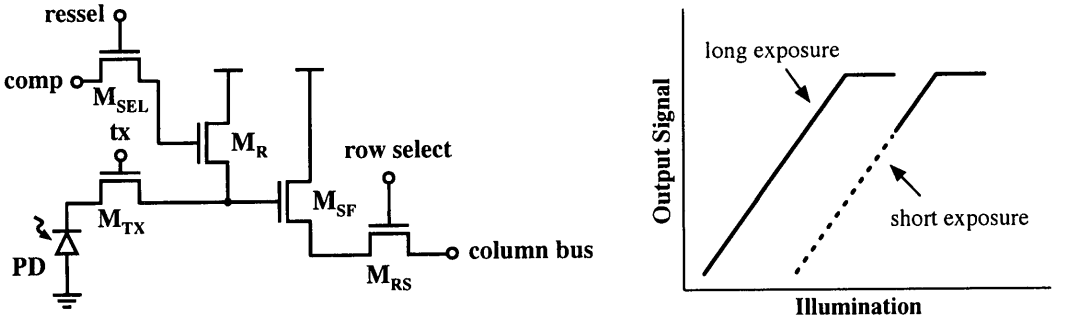
The difference of global- and local-integration time adjustment pixels can also be understood through S_{L}. In a globalized-control pixel, reset occurs at T_1 even though the signal does not reach saturation. Therefore, two readout voltages (V_{L} and V_{L}') are generated at T_1 and T_2, respectively, where normally only V_{L} is utilized due to its higher SNR. In a localized-control pixel, the reset is not triggered since S_{L} does not reach saturation at T_1, and only one voltage (V_{L}'') is generated for readout

at T_2. In general, the localized-control pixel has a regular $(T_L + T_S)$ integration time for signals not reaching saturation, but its conditional reset circuitry is more complex than the globalized-control one.

The easiest way of implementing this type of pixel is with a conventional 3-T or 4-T pixel operating in a multiple-capture mode. In this mode, the operation of pixel is identical with the regular one and saves the cost of pixel development. However, each of the multiple integration times will be shorter than the original, if the frame rate does not change, since multiple exposures will be performed within the same period. A possible solution to extend the integration time is overlapping the different exposures [53, 54].

For those pixels using a localized-control integration time, the pixel will be larger due to the presence of conditional reset circuitry, as shown in Fig. 2.14(a). The conditional reset circuitry is composed of M_{SEL} in this figure (and can be with more transistors if further operations or processing are required) which controls the reset operation of M_R according to the comparator output (comp). This signal is usually a result generated according to the present pixel signal. Fig. 2.14(b) shows the photo-response of this type of pixel, where the saturation levels for long and short exposures are equal.

The largest advantage of this type of pixel is that the extended DR has the same photo-sensitivity as the original, hence the calibration of output signal or color re-



(a) (b)

Figure 2.14: (a) A local-integration time adjustment pixel with its conditional reset circuitry and (b) its photo-response transfer curve (the dashed line is the overlap between two integrations and is not utilized in readout).

production is much easier (post-processing is still required, though). However, the SNR dip between any two adjacent exposures is problematic and a challenge for design (see Fig. 2.15). In general, the dip becomes large when the two different integration times differ greatly in their amounts which are used to further extend the DR. In fact, the performance of this type of sensor depends strongly on the bandwidth or resolution of back-end signal processing circuit, which becomes another constraint for this pixel design. Also, a post-processing unit is usually required to synthesize the signals and generate the final output.

The cause of SNR dip is further explained by using the illustration shown in Fig. 2.16, which shows the signal and noise outputs in a conventional photodiode. Under constant illumination, both the signal and noise increase with time,

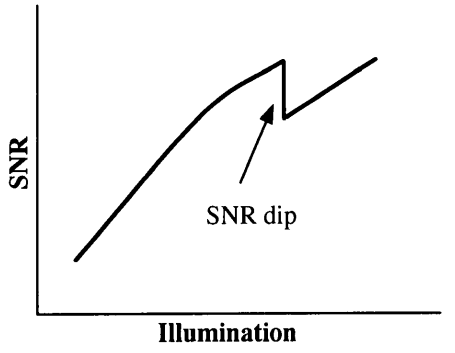


Figure 2.15: The SNR of integration time adjustment pixel with two exposures, showing the SNR dip.

where the noise component includes a time-dependent (photon shot noise), which is usually the square root of the signal, and a time-independent (reset noise) part. According to the definition of SNR, it can be understood as the difference between the signal and noise curves. Obviously, SNR increases with integration time and has a particularly low value when the integration time is very short. As a result, the SNR of a time adjustment pixel will consist of at least two portions, where the consecutive SNR curve experiences a drop at the switching point determined by the length of T_{L} and T_{S} (and other even shorter integrations if used).

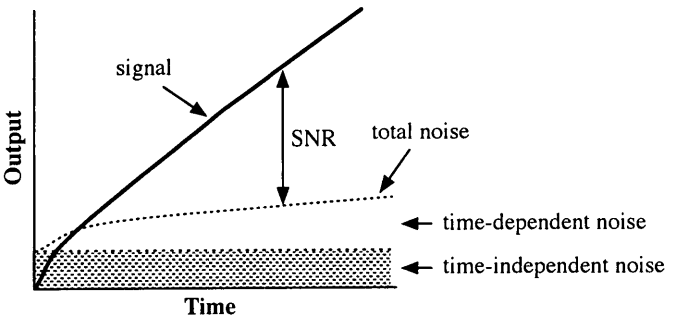


Figure 2.16: The formation of SNR in a photodiode. While signal increases with time, there are time-dependent and -independent noises associated which limit SNR performance for very short time integrations.

This dip can be further quantified by considering the principle of SNR calculation. Theoretically, the SNR (of the long integration time) can be expressed as

$$\mathrm{SNR}_{\mathrm{long}} = 20 \cdot \log(\frac{S_{\mathrm{long}}}{N_{\mathrm{long}}}) = 20 \cdot \log(\frac{S_{\mathrm{long}}}{\sqrt{S_{\mathrm{long}} + N_{\mathrm{read}}}}) \tag{2.2}$$

where S is the collected signal charge and N is the corresponding noise charge within any given integration times, and N_{read} is the read noise level, which is not affected by the signal or illumination. Since the switching point of a time adjustment pixel usually occurs when the saturation of the long (or longer) integration time occurs, the actual dip can be estimated from this point. As such, the SNR is given by (2.2). Alternatively, the signal can be acquired from the short (or shorter) integration time. Under this condition, the collected signal charge will become $(S_{\mathrm{long}} \times T_{\mathrm{S}}/T_{\mathrm{L}})$ since the illumination remains the same and only the integration time changes. Accordingly, the SNR (of the short integration time) can be written as

$$\mathrm{SNR_{short}} = 20 \cdot \log(\frac{S_{\mathrm{short}}}{N_{\mathrm{short}}}) = 20 \cdot \log(\frac{S_{\mathrm{long}} \times \frac{T_{\mathrm{S}}}{T_{\mathrm{L}}}}{\sqrt{S_{\mathrm{long}} \times \frac{T_{\mathrm{S}}}{T_{\mathrm{L}}} + N_{\mathrm{read}}}}). \tag{2.3}$$

Consequently, the SNR dip can be derived by subtracting (2.3) from (2.2) and expressed as

$$\begin{aligned} \mathrm{SNR_{dip}} &= 20 \cdot \log(\frac{S_{\mathrm{long}}}{N_{\mathrm{long}}}) - 20 \cdot \log(\frac{S_{\mathrm{short}}}{N_{\mathrm{short}}}) \\ &= 20 \cdot \log \cdot (\frac{T_{\mathrm{L}}}{T_{\mathrm{S}}} \cdot \sqrt{\frac{S_{\mathrm{long}} \times \frac{T_{\mathrm{S}}}{T_{\mathrm{L}}} + N_{\mathrm{read}}}{S_{\mathrm{long}} + N_{\mathrm{read}}}}). \end{aligned} \tag{2.4}$$

Typically, N_{read} is relatively low compared with S_{long}, therefore (2.4) can be simplified as

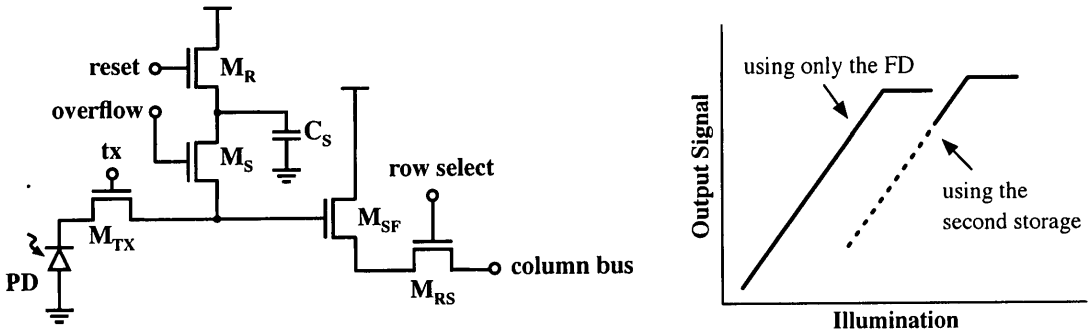
$$\begin{aligned} \mathrm{SNR_{dip}} &\approx 20 \cdot \log \cdot (\frac{T_{\mathrm{L}}}{T_{\mathrm{S}}} \cdot \sqrt{\frac{S_{\mathrm{long}} \times \frac{T_{\mathrm{S}}}{T_{\mathrm{L}}}}{S_{\mathrm{long}}}}) \\ &= 20 \cdot \log \cdot \sqrt{\frac{T_{\mathrm{L}}}{T_{\mathrm{S}}}}. \end{aligned} \tag{2.5}$$

According to (2.5), the SNR dip can be quantitatively estimated for performance evaluation. When $T_{\mathrm{S}} = (1/10) \times T_{\mathrm{L}}$, DR is increased by 20 dB and the SNR dip is 10 dB. As a result, we conclude that the SNR dip is determined by the difference of two adjacent integrations and amounts to 10 dB for every 20-dB DR improvement. This result also implies that a 100-dB DR achieved through the integration time adjustment method has a potential 20-dB SNR dip, assuming the original DR is 60 dB and only two different integrations are implemented.

2.3.4 Clipping Pixel

The root cause of DR limitation in a 3-T or 4-T pixel is the Q_{FW}, which is directly related to the equivalent capacitance at the photodiode. Accordingly, the clipping pixel was invented by using an adjustable reset gate voltage to change Q_{FW} at different points within one integration [58]. The recent version of this technique adds a second storage capacitor, either by using a transistor or a capacitor which can be switched in to change Q_{FW}, in the same pixel to utilize a larger Q_{FW} and extend DR to the high-light region. This idea has been implemented in many designs and achieves a DR of more than 100 dB [36, 59–66]. A schematic showing the concept of clipping pixel is shown in Fig. 2.17(a), and the transfer curve demonstrating the DR extension is shown in Fig. 2.17(b). From this figure, it is clear that the clipping pixel has a different saturation level for its second exposure, unlike the integration time adjustment pixel. It is also notable that a clipping pixel is mostly based on a 4-T pixel which provides the possibility of charge holding or transferring when two or more samplings are utilized.

Since a clipping pixel usually has at least two transfer curves with different characteristics (one with original storage and another one with added storage), it is obvious that a computational signal post-processing unit is required, similar to the integration time adjustment pixel, to calculate or synthesize the final output. This is



(a) (b)

Figure 2.17: (a) The schematic of a clipping pixel using a second storage capacitor and (b) its photo-signal transfer curve (the dashed line is the overlap between two integrations and is not utilized in readout).

a general drawback with the clipping pixel using a second charge capacity. Another disadvantage of this pixel is the decrease in frame rate (usually reduced by half) since two periods of integration are required to collect the necessary information for WDR imaging. Although the cost of using this type of pixel is high, possibly due to the usage of additional CMOS process and mask, the achievable DR is over 200 dB [60] which is much higher than other existing techniques. The SNR dip still exists in this type of sensor, but it can be less obvious than that of the integration time adjustment pixel if carefully designed [65].

2.3.5 Time-To-Saturation (TTS) or Time-To-First-Spike (TTFS) Pixel

Since the saturation level of a pixel is determined by Q_{FW}, a design using a TTS or TTFS pixel was utilized to avoid this constraint [67–70]. The idea of this type of sensor is to encode the time information when each pixel has reached its predefined saturation level. Typically an in-pixel comparator is required. The memory unit can be either analog or digital, depending on the design method and requirement of signal processing. A general schematic of this type of pixel is shown in Fig. 2.18. By using this method, the DR will not be restricted by the limited Q_{FW}. Actually, the design challenge of this type of pixel is similar to that for the integration time adjustment pixel, i.e. the bandwidth or digital resolution of periphery circuitry, if a very large DR is required.

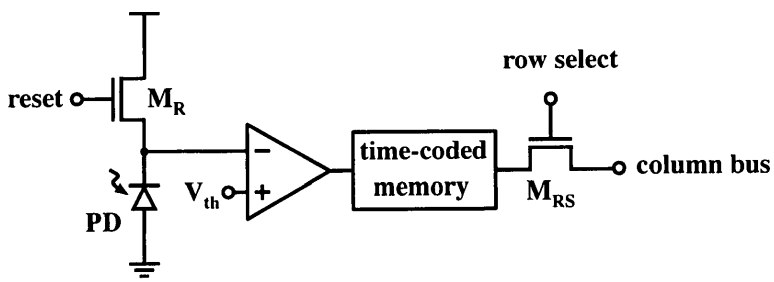


Figure 2.18: The schematic of a TTS pixel with a memory cell.

The time-coding algorithm is shown in Fig. 2.19 with three different strengths of light intensities. According to this figure, the integration time required for V_{PD} to reach V_{th} after reset (V_{rst}) will be used as a reference of light intensity and

stored in the in-pixel memory. When a weak illumination is applied to the pixel, a long integration time happens (T_3); on the other hand, a short integration time (T_1) occurs when a strong illumination is applied. Consequently, these different integration times can be coded and stored as a reference of the signal intensity.

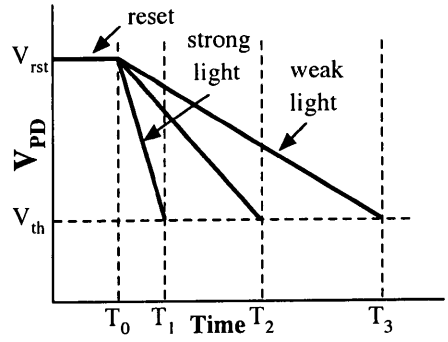


Figure 2.19: The time-coding algorithm of TTS pixel. T_1, T_2, and T_3 are the saturation times of each individual integration after reset (T_0), with strong, medium, and weak light intensities, respectively.

Since a comparator and a memory cell is usually required by this type of pixel, its transistor count is much greater than the previously mentioned pixels which are based on the APS. Therefore, the use of this pixel relies on the application and constraints, such as the targeted DR and pixel pitch. Although the FF is sometimes as low as less than 10%, its linear output characterization is advantageous in certain conditions.

2.3.6 Pulse-Frequency Modulation (PFM) Pixel

The development of a PFM pixel, sometimes called the PWM pixel due to different methods of signal processing, was first demonstrated by the idea of intensity-to-frequency converter [71]. Currently, many CMOS pixels achieve WDR imaging by using this in-pixel signal conversion technique, which is also called the Σ-Δ conversion [19, 72–79]. The achievable DR of this type of pixel is more than 140 dB, satisfying most of the WDR imaging applications. A schematic of the PFM pixel is shown in Fig. 2.20, including a comparator and a latch in the pixel. The reference voltage (V_{ref}) sets a threshold to determine when a pulse signal is generated and a reset is triggered.

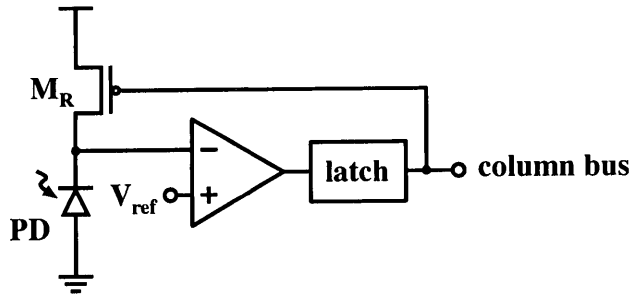


Figure 2.20: The schematic of PFM pixel.

Since the PFM and PWM pixels also contain comparators, their sizes are also relatively large, similar to the TTS or TTFS pixel. As a result, the use of this type of pixel is limited to some specific conditions where a large pixel (or low FF) is allowed or a smart sensor is to be built. On the other hand, the advantage of this large pixel

is its relatively linear photo-response benefited from removing the use of a source follower buffer [19, 77–79]. Although the non-uniformity of photodiode capacitance still exists, its effect on signal nonlinearity can be minimized by operating the photodiode in the most linear region. In general, the concept of PFM or PWM pixel is similar to the TTS or TTFS pixel, where the DR is not limited by the Q_{FW}. The primary difference is that there are multiple integrations (resets) in the PFM or PWM pixel but only one in the TTS or TTFS pixel. The operation of light-to-frequency conversion of a PFM pixel is illustrated in Fig. 2.21 with a changing light intensity over time.

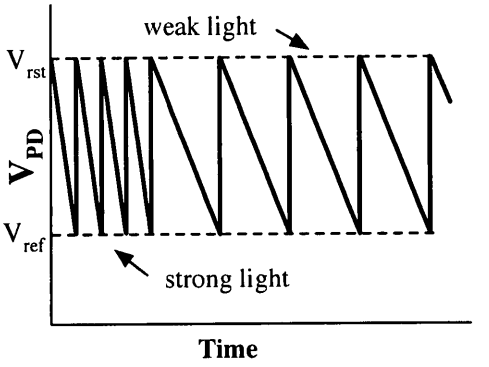


Figure 2.21: The light-to-frequency operation of a PFM pixel, starting from a strong light (high frequency) to a weak light (low frequency). Output frequencies can be controlled by adjusting V_{ref}.

The feasibility of PFM pixels has been investigated by many authors, but several issues remain with this type of pixel. In spite of the large pixel size, the mismatch-induced FPN is still high compared with the conventional APS and conventional

pattern noise reduction techniques do not apply. In addition, a complete study of the achievable DR has not been presented yet. As a result, the PFM pixel has not been widely adopted for commercial applications.

2.4 Overall Comparison

To summarize the mentioned techniques in terms of those important parameters related to circuit design, we performed a complete survey of the existing publications which demonstrated successful implementations of the WDR image sensor [19, 29, 36, 38–41, 44, 50, 53–55, 61, 62, 65, 67–69, 73, 78, 80–83] and summarize the results in Table 2.2. The parameters included are the pixel size, DR, SNR (for temporal noise), FPN (for spatial noise), linearity, frame rate, and power. The performance metrics that involve spectral response are not included because they are not in the scope of this study. Note that only those using a CMOS process of 0.18 μm to 0.5 μm are considered to exclude the possible performance deviation due to different technologies.

From this table we notice that APS-based structures have a much smaller pixel pitch, between 4.5–10 μm (only a few with up to 25 μm). Although the logarithmic and multimode pixels achieve a DR of more than 100 dB easily, the SNR or FPN does not satisfy some high-demand applications, nor was the linearity characterized (the logarithmic response normally has a poor performance in this aspect). Alter-

Table 2.2: Comparison of Major WDR Pixels

Parameter / Variation	Pixel Pitch[1]	DR (max)[2]	SNR (max)[2]	FPN[3]	Nonlinearity[3]	Frame Rate[4]	Pixel Count	Power[5]
Logarithmic	7.5–24	100–120	32–42	2.5–3.8	N/A	8–30	110k–4.2M	24–170
Multimode	5.6–27.15	112–143	44-55	1.4–11.4	N/A	N/A	256–100k	30–200
Integration Time Adjustment	5.6–10	86–121	32–48	0.1–1	0.5	7.5–20	1k–5.2M	10–35
Clipping	4.5–7.5	90–143	48–49	N/A	N/A	30–60	4k–300k	N/A
TTS or TTFS	15–37.5	70–120	58	1.7–4.6	N/A	30	1k–20k	33–340
PFM or PWM	23–50	110–130	23–56	>5	<0.1	8.5–60	4k–72k	80–250

[1] Unit: μm.
[2] Unit: dB.
[3] Unit: %.
[4] Unit: fps.
[5] Unit: nW per framer per pixel.

natively, the integration time adjustment and clipping pixels have high SNR or low FPN, but require complex readout approaches to reach more than 100-dB DR. In addition, SNR dip is common for the APS-based pixels with multiple-readout implementation (except the logarithmic pixel). DPS-based (or time- and frequency-based) pixels use a larger size of 15–50 μm where an area-consuming comparator and memory cells are needed. The DR and SNR of this type of sensor can be very high without requiring complex designs, but the FPN is unacceptably high. Another advantage of this group of pixels is the relatively-high signal linearity which is observed among the PFM pixels. However, the primary drawback of the time-based pixels is the small pixel counts resulting from either the large pixel pitch or the readout approach.

In summary, the APS-based pixels have small pixel pitch and large pixel count but use a complex readout method and suffer from the SNR dip, whereas the time-based pixels reach high DR as well as SNR but have a poor FPN and sometimes limitations on array size. The conclusion also implies that more design potential may be available for the time-based pixels if a strategy can effectively reduce the FPN and the pixel count increases to at least 100k to meet the requirement of certain applications.

2.5 Summary

In this chapter, those important parameters from a circuit perspective, including the DR, temporal and spatial noise (SNR and FPN), linearity, and frame rate, have been discussed to illustrate important considerations when designing WDR CMOS image sensor. In addition, six popular techniques of achieving WDR imaging are also briefly reviewed, and their advantages and drawbacks are discussed. Current techniques of realizing WDR imaging have achieved over 100 dB easily, however the SNR dip remains a challenge for the current designs, and high FPN is a concern for time-based pixels. Finally, a detailed comparison of several figures of merit for a range of published WDR image sensors is used to provide quantitative background for the work in this thesis. Based on this, we believe that there is potential of improve the performance of time-based pixels to better utilize their larger DR and higher linearity.

3 Analysis and Design of the PFM Pixel

In Chapter 2, the circuit aspects of the different WDR imaging techniques were compared. The summary suggests that several issues remain with the APS structure, including the SNR dip, noise- and Q_{FW}-limited DR, and sometimes the higher temporal and spatial noises. An early work on a two-step readout APS design with fabrication in CMOS, presented in Appendix A, shows that DR is seriously restricted by the noise and Q_{FW}, and cannot be easily increased under current CMOS technologies. Although the achievable pixel size is small and attractive to many applications, the difficulty of dealing with those mentioned issues still prevents the adoption in certain imaging conditions, such as high-quality or medical imaging which requires a very low noise level and a large DR. On the other hand, the time-based pixels can have better performance (except the FPN), but the pixel size is much bigger. In fact, the selection of pixel design (system) depends on the requirement of each specific application, and there are always trade-offs when using any technique or strategy.

In this work, the target is to achieve a WDR CMOS image sensor design based on the PFM pixel with low FPN, high linearity, and smooth and high SNR. The desired frame rate is at least 30 fps, satisfying the requirements of most video applications. The resolution of the sensor will be between QVGA (320 $\times$ 240) and SXGA (1280 $\times$ 1024) to support applications including online videoconference, surveillance, and medical imaging. While APS-based WDR pixels are not capable of providing a uniform SNR and require more effort in terms of processing or calibrating the final WDR output signal, the time- or frequency-based pixels do provide a solution to achieve these targets by avoiding the limitation of pixel Q_{FW}. Among these two techniques, the frequency-based pixel has even less constraint for the periphery circuits and is a better candidate for smart sensor design. As a result, we choose to use the PFM pixel to design a WDR image sensor with those merits previously mentioned and will explore solutions to its other limitations.

Previous research on the PFM pixel is focused on the concept implementation and functional results [19, 75, 76], without any detailed analysis and modeling to assist design optimization. In general, these existing studies focus on the implementation of the concept and basic operational experiments. Although the concept of PFM pixel has been demonstrated to work properly, the lack of systematic design strategy still hinders future development, not to mention the actual performance in terms of FPN is not comparable to those based on APS. As a result, we perform

several investigations to disclose the optimum design method for a WDR PFM pixel with important parameters, including linearity and noise, considered [84].

3.1 Principle of the PFM Pixel

Before describing the analysis of the PFM pixel, its principle is introduced by demonstrating its complete operation. In Fig. 3.1, the schematic of PFM pixel is shown again with the difference of reset and reference voltage defined as V_{diff}, which can be written as

$$V_{\text{diff}} = V_{\text{rst}} - V_{\text{ref}} \tag{3.1}$$

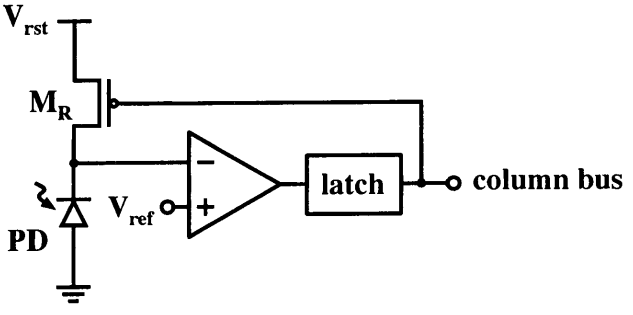


Figure 3.1: The schematic of a PFM pixel. V_{diff} is the voltage room for each integration.

where V_{rst} is the reset voltage and V_{ref} is the reference voltage connected to the comparator. In general, V_{rst} is equal to V_{DD} but can be of different values. In (3.1), V_{diff} represents the necessary integrated photo-signal voltage to produce a pulse signal in each integration cycle, if the photodiode is successfully reset to V_{rst}.

The detail of the process is illustrated in Fig. 3.2, and the operation is described as follows.

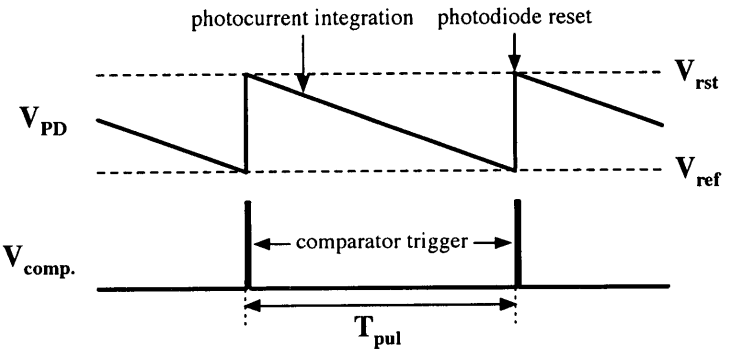


Figure 3.2: The illustration of PFM pixel operation. T_{pul} is a pulse signal with its duration inversely proportional to the intensity of photocurrent.

Photocurrent Integration: The photocurrent (I_{ph}) is generated by the incident photons, and the induced free electrons will accumulate at the site of C_{PD}, the equivalent capacitance of the photodiode. This causes V_{PD} to drop at a rate determined by the flow of free electrons and is assumed to be proportional to the incident light intensity.

Comparator Trigger: Once V_{PD} is lower than V_{ref} , the comparator will generate a trigger signal which is used to turn on the reset transistor. This process is a self-reset operation for the PFM pixel (and also called Σ-Δ conversion).

Photodiode Reset: When the reset transistor is turned on, a reset current (I_{rst}) will start charging C_{PD}. Consequently, the result of this charging is to reset C_{PD} back to the reset level (V_{rst}) given that the delay of comparator is usually long enough. Ideally, this step finishes when V_{PD} is pulled up to V_{rst} and the comparator accordingly fires an off signal to turn off the reset transistor. After the reset transistor is turned off, the operation completes and moves to next integration phase.

Generally, the PFM pixel repeats these three steps to produce a periodic signal dependent on I_{ph}. The integrating voltage room per cycle is controlled by V_{diff} (Q_{FW} is also controlled by C_{PD}), and the pulse-frequency period is determined by the adjacent reset pulses and referred to as T_{pul}. Ideally, T_{pul} is only controlled by the slope of integration, which is a linear function of I_{ph} and given by

$$T_{\text{pul}} = \frac{C_{\text{PD}} \cdot V_{\text{diff}}}{I_{\text{ph}}}. \tag{3.2}$$

As a result, T_{pul} can be controlled by adjusting V_{diff} when C_{PD} and I_{ph} (illumination) are fixed. The generated pulse-frequency signal is eventually recorded by different methods suggested in [19, 75, 81] according to the application requirements. Among different signal-processing approaches, the most straightforward is implementing a digital counter to acquire the number of resets within a fixed period of time [19], which is also the targeted investigation of this work.

3.2 Design Strategy toward WDR Imaging

The DR of PFM pixels is believed to be extremely large and sometimes theoretically claimed to be unlimited. Actually, the operation of a PFM pixel is a process of current charging and discharging, so the dark current (I_{dark}) of the photodiode and the leakage (off) current (I_{leak}), as well as the reset (on) current (I_{rst}) of the reset switch, together with the photocurrent (I_{ph}) must be considered for DR analysis. A simplified circuit model of the photodiode and reset transistor is shown in Fig. 3.3 to illustrate the analysis.

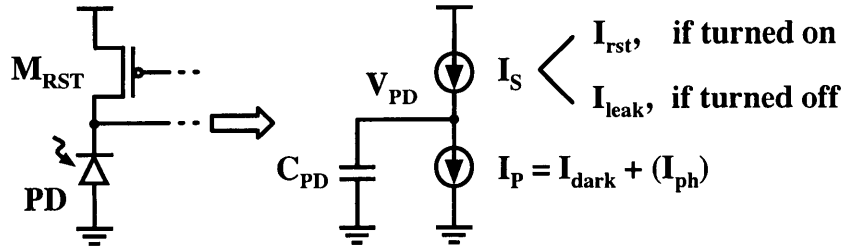


Figure 3.3: A simplified photodiode and reset transistor circuit model for DR analysis.

In this figure, I_{S} can be either the reset current, if the reset transistor is turned on, or the leakage current if it is turned off. I_{P} is the photodiode dark current plus any amount of photocurrent if there are any incident photons absorbed by the photodiode. In addition, C_{PD} is assumed to be constant throughout the whole integration. When the integration takes place and the pixel is in a complete dark condition (i.e., no photocurrent will be generated), I_{dark} is discharging and I_{leak} is

charging C_{PD}. In this case, the lower DR bound of a functional PFM pixel will be restricted by the larger of these two values. When I_{dark} is larger, the integration process functions normally regardless of I_{leak} since the net current ($I_{\mathrm{leak}} - I_{\mathrm{dark}}$) is negative and C_{PD} is discharged. On the contrary, if I_{leak} is larger, the net current is positive and C_{PD} will be continually charged, and the comparator will never switch. As a result, a smaller I_{leak} (than I_{dark}) is necessary for a PFM pixel to operate properly when no illumination is applied to the photodiode. Otherwise, a portion of the photo-signal will be lost, especially in low-light conditions, by an amount of $I_{\mathrm{leak}} - I_{\mathrm{dark}}$.

However, a minimized I_{leak} is not always beneficial to PFM pixels and it can itself be a cause of signal loss. In Fig. 3.4, the leakage current and the reset to leakage ratio with different widths and lengths of thick- and thin-oxide PMOSs in the sub-threshold region are extracted from simulation results, using a 0.18-μm CMOS process. As the result shows, the magnitude of I_{leak} is dominated by the gate oxide thickness instead of its size. Typically, a thicker oxide causes a larger threshold voltage and lowers the sub-threshold leakage, so I_{leak} can only be changed up to a factor of 20 by adjusting the size of the transistor. Besides, the ratio of I_{rst} and I_{leak} is unrelated to the size of transistor and keeps an almost constant value. Although I_{rst} will not affect the performance at zero illumination (or low illumination), it directly relates to the highest $I_{\mathrm{ph}} + I_{\mathrm{dark}}$ level that a PFM pixel

can handle. Once $I_{\text{ph}} + I_{\text{dark}}$ is larger than I_{rst} with a very strong illumination, the pixel will no longer perform self-reset operation since the reset transistor is unable to counter-charge C_{PD}, and no pulse-frequency signal can be generated.

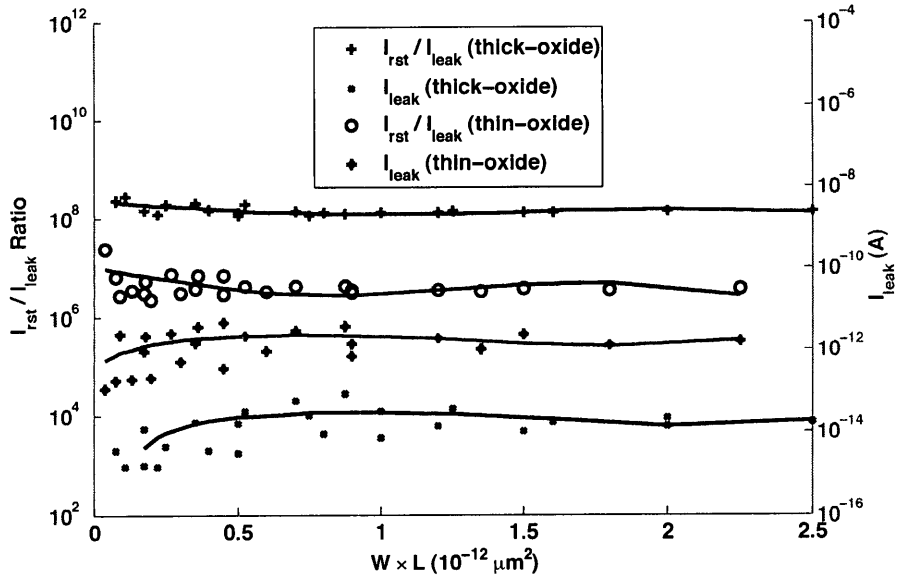


Figure 3.4: The values of $I_{\text{rst}}/I_{\text{leak}}$ and I_{leak} of thick-oxide and thin-oxide PMOSs (solid lines are fitted curves) extracted at room temperature (25 °C). The x-axis indicates the transistor gate area.

According to the above descriptions, the DR of a PFM pixel is normally constrained by the ratio of I_{rst} and I_{leak}. However, a minimized I_{leak}, which leads to a smaller I_{rst}, sets DR to be the ratio of I_{rst} and I_{dark} since I_{leak} is smaller than I_{dark}. The DR is therefore reduced by the amount of $20 \cdot \log(I_{\text{dark}}/I_{\text{leak}})$. The relationship between I_{rst}, I_{leak}, and I_{dark} is further illustrated in Fig. 3.5, where the ratio of I_{rst} and I_{leak} is assumed constant. First, I_{leak} is larger than I_{dark} in Fig. 3.5(a). As such, DR is not affected by I_{dark}, but the low-light scene is lost (the slash line

area). On the contrary, when I_{leak} is smaller than I_{dark} [Fig. 3.5(b)], the low-light information is kept. However, DR is reduced by the previously mentioned amount (the backslash line area), i.e., the maximum photocurrent detection is lowered. As a result, we conclude that the maximum DR available in the PFM pixel can be simply given by

$$20 \cdot \log\left(\frac{I_{\text{rst}}}{\max\{I_{\text{leak}}, I_{\text{dark}}\}}\right) \tag{3.3}$$

which is determined by the larger of I_{leak} and I_{dark}. In Fig. 3.5(c), I_{leak} is set equal to I_{dark}. In this case, no low-light information is lost nor DR will be sacrificed.

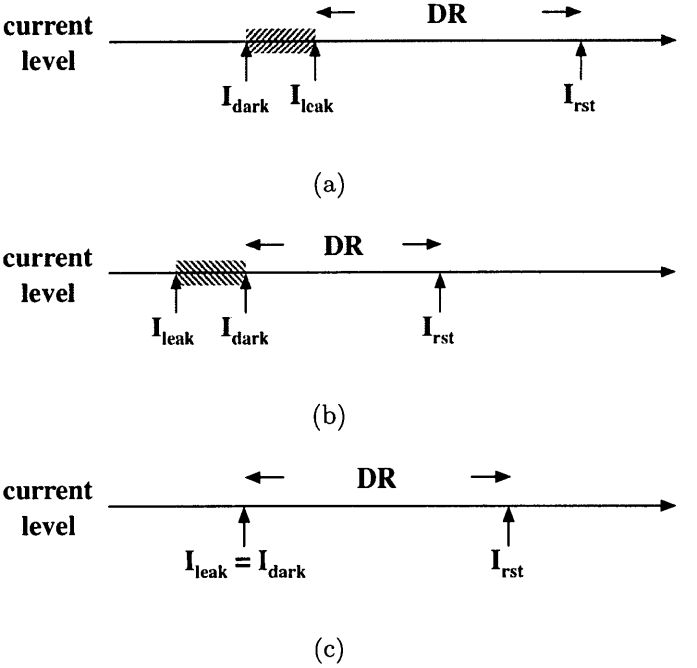


Figure 3.5: Relationship between DR and I_{rst}, I_{leak}, and I_{dark}. Two cases are with (a) larger I_{leak} and (b) smaller I_{leak}, respectively. (c) An equal I_{leak} and I_{dark} provides the possibility of highest DR and keeping the low-light information.

The maximum DR that the PFM pixel offers is also estimated from the extracted value of I_{rst} and I_{leak} in Fig. 3.4, assuming $I_{\text{leak}} \geq I_{\text{dark}}$. According to the values, the ratio of I_{rst} and I_{leak} is about 10^8 for thick-oxide and 3×10^6 for thin-oxide PMOSs. It implies that a DR of 160 dB or 130 dB is the maximum available, depending on the choice of reset transistors. The difference is primarily due to the thick-oxide transistors having a lower leakage than thin-oxide ones.

Based on the above discussions, the available DR is strongly related to the photodiode and reset transistor designs. The I_{leak} depends on the size of reset transistor, and the best design strategy to maintain a low-light imaging range and a highest DR is keeping $I_{\text{leak}} \approx I_{\text{dark}}$. Since I_{dark} is virtually proportional to the area of photodiode, the size of reset transistor should be selected based on the area of the photodiode. For large photodiodes (5 μm $\times$ 5 μm or larger), the reset transistor with a wide channel is selected, offering a higher I_{leak}; on the contrary, a long-channel reset transistor is used with small photodiodes since I_{leak} will be smaller. It is notable that a very small I_{leak} is beneficial to increase the signal frequency, although it leads to the loss of the high-light imaging region. A summary of the selection strategy is listed in Table 3.1 to simplify the conclusion.

Table 3.1: Design Strategy of I_{leak}

Result \ Condition	$I_{leak} > I_{dark}$	$I_{leak} = I_{dark}$	$I_{leak} < I_{dark}$
DR	maximum DR	maximum DR	smaller DR
Applied Scene	bright	regular	dark

3.3 Analysis, Measurement, and Modeling of Signal Linearity

Signal linearity is a very important figure of merit of CMOS image sensors, given that the image calibration and/or color reproduction are almost necessary for every application. Having a perfectly linear signal between illumination and output will help simplify or remove the calculation required to calibrate the signal, and therefore the overall cost is reduced. The signal nonlinearity of conventional APS is normally below 2% [36, 85–88], however these numbers were mostly reported without using the full-signal swing (i.e. neglecting the near-saturation region). In addition, the nonlinearity becomes problematically large when any of the existing WDR imaging solutions is used. On the other hand, the PFM pixel, which stores the same amount of charges within every integration, is believed to have a higher signal linearity.

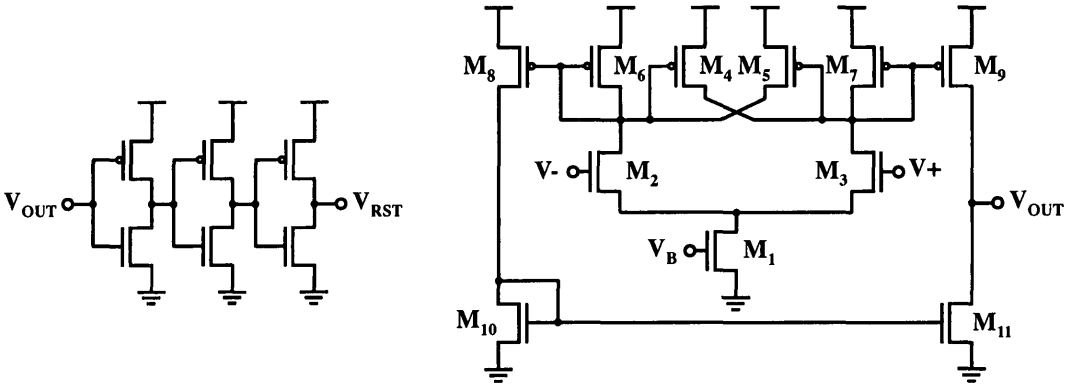
In this section, the signal linearity of a PFM pixel is analyzed with respect to different illumination intensities and V_{diff}, using a circuit analysis. In addition, measured data from a sample PFM pixel is obtained to support the analysis. De-

tailed models of the operational processes inside the PFM pixel are derived step by step to clarify the design constraints and to develop an appropriate optimization strategy.

3.3.1 Specification of PFM Pixel and Measurement Setup

Before the analysis is presented, the specification of the sample PFM pixel is introduced and the setup of measurement system is described. The method and approach of obtaining the pixel signal under different conditions is presented as well.

The pixel block diagram is shown in Fig. 2.20. The photodiode uses n^+ and p-substrate diode and has an area of 104.35 μm^2. A thick-oxide PMOS is used for reset. The latch circuit is composed of three basic inverters to create step-pulses for accurate reset operation [19] [see Fig. 3.6(a)]. The comparator is a single-ended structure designed using a symmetrical operational transconductance amplifier (OTA), shown in Fig. 3.6(b). It has the benefits of high gain and reasonable design complexity, compared with other popular amplifier structures. The width and length of each transistor of this comparator are listed in Table 3.2, and the pixel and comparator specifications are summarized in Table 3.3.



(a) (b)

Figure 3.6: Circuit schematic of (a) latch and (b) symmetrical OTA-based comparator.

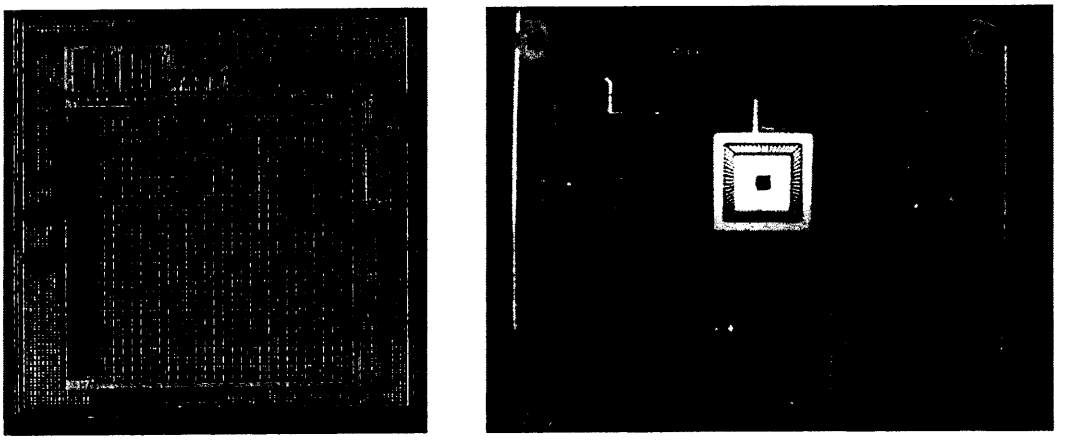
Table 3.2: Transistor Size of Comparator

Transistor	W/L (μm)	Multiplier
M_1	1.97/0.3	2
M_2, M_3	1.97/0.3	3
M_4, M_5, M_6, M_7	1.94/0.3	1
M_8, M_9	1.94/0.3	4
M_{10}, M_{11}	1.97/0.3	2

Table 3.3: Pixel and Comparator Specification

Technology	0.18-μm 1P6M CMOS
Pixel Size	23 μm $\times$ 23 μm
Photodiode Type	n^+/p-substrate
Fill Factor	25%
V_B (I_{bias})	0.3 V (12 μA)
GBP	1.6 GHz
Slew Rate	580 V/μs

The microphotograph of the measured chip [89] and a testing board designed to attach the chip are shown in Fig. 3.7. A 1.2-V supply voltage is applied to the core circuitry to operate the pixel with minimized power consumption. The bias level for V_{B} is 0.3 V to drive M_1 of the comparator above weak inversion but below saturation, where a highest gain-bandwidth product (GBP) occurs. A tungsten bulb, powered by a switchable current supply, is used to provide the necessary illumination. An integrating sphere (Fig. 3.8) is also used to keep the lighting uniform. The light source is capable of providing an illumination range between 1 and 162,900 lux, a range of 104 dB. The output signal (V_{RST}) from the latch of the pixel is not only connected to the gate of M_{RST} but also directly captured by a mixed-signal oscilloscope. The measured pulse width (T_{pul}) is defined to be the period between the start of one reset (when reset is turned on) and the start of the next reset. V_{diff} is varied from 0.01–0.15 V with a minimum step of 0.01 V.



(a) (b)

Figure 3.7: The (a) chip microphotograph and (b) testing board for the measurement.

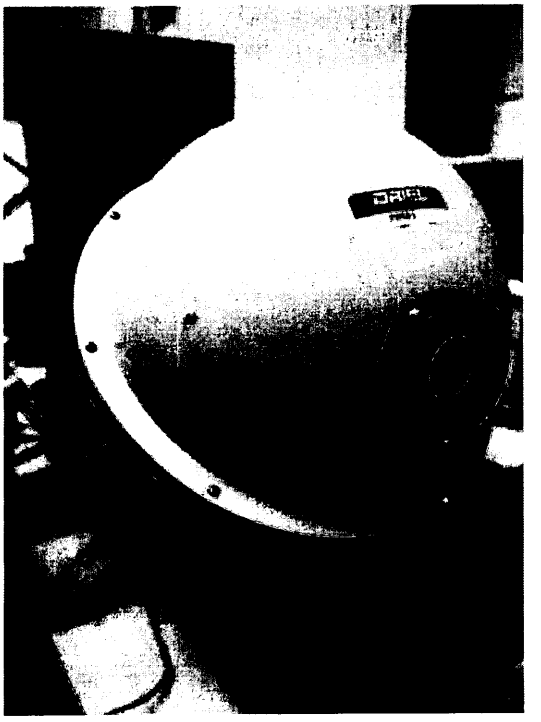


Figure 3.8: The integrating sphere (front; Oriel 70481) and lamp housing (rear; Oriel 66180).

3.3.2 Analysis of Pulse Period

It is necessary to consider the detailed operation of the PFM pixel in order to analyze its pulse period and to develop the appropriate models. Although a simplified operation of PFM pixel has been shown in Fig. 2.21, it is not enough to assist in this study due to factors that are commonly neglected, including the delay of the integration process and the actual reset period. As a result, a more complete operation of PFM pixel is shown in Fig. 3.9 and is used to help proceed with the analysis.

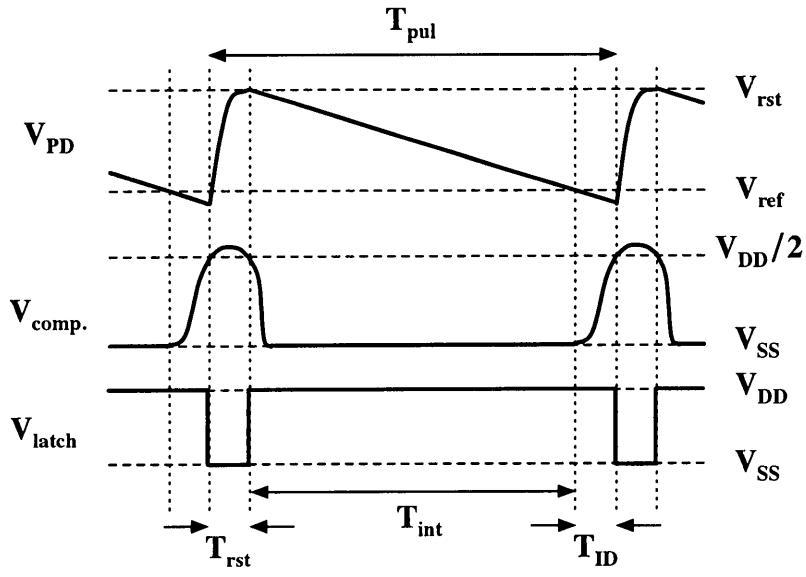


Figure 3.9: A practical PFM pixel operation (not to scale). T_{pul} is the pulse width, consisting of T_{rst}, T_{int}, and T_{ID}.

This figure suggests that three major time blocks should be considered for the PFM pixel analysis. In addition to the integration time period (T_{int}), the integration

delay period (T_{ID}) and the reset period (T_{rst}) are also included in one complete signal (T_{pul}). In previous studies, only T_{int} was discussed and the analysis of signal linearity was neglected or incomplete [19, 76, 81]. However, the real condition is that T_{ID} and T_{rst} have crucial and notable impacts on the signal linearity and must be fully investigated. Therefore, these three time periods have to be analyzed individually to completely understand the design constraints of PFM pixel when a high signal linearity is required.

V_{diff} is one important parameter required for the analysis, and its value is controlled by an external bias (V_{ref}). V_{diff} not only determines the duration of integration (i.e. output frequency) but also affects the performance of the comparator when comparing V_{PD} to V_{ref}. This in turn affects significantly the signal linearity. In this section, the effects of T_{ID} and T_{rst} are disclosed by combining both the simulation and measurement results with explicit explanations. In addition, the simplified models for both time periods are also derived. The varying parameters for the analysis also include the illumination intensity, which affects the small-signal characteristics of the comparator. In simulation, I_{ph} is assumed to vary over 6 decades to match the experimental setup, which supports a DR of over 100 dB.

3.3.3 Photocurrent Integration Period (T_{int})

Regardless of whether the pixel is under illumination or not, there is always a current discharging C_{PD} (assuming I_{leak} is smaller than I_{dark}). The current is represented by $(I_{\text{ph}} + I_{\text{dark}} - I_{\text{leak}})$, so T_{int} can be given by

$$T_{\text{int}} = \frac{C_{\text{PD}} \cdot V_{\text{diff}}}{I_{\text{ph}} + I_{\text{dark}} - I_{\text{leak}}}. \tag{3.4}$$

Although C_{PD} will change with different applied reverse bias voltages, it is assumed to be constant here to simplify the analysis. This is reasonable since the nonlinearity is only prominent when a very small V_{diff} (such as 0.005 V or less) is used. As a result, T_{int} is inversely proportional to I_{ph} if I_{dark} and I_{leak} are small. This integration period varies, according to illumination intensities, by 5–7 decades and can be between 100 ms and 10 ns in a regular design using common CMOS technology.

The linearity of T_{int} also depends on the design of the photodiode and reset transistor. When I_{dark} is very close to I_{leak}, (3.4) can be simplified to give (3.2) and the integration is highly linear over the whole imaging range. However, if I_{dark} is not close to I_{leak}, the linearity degrades when I_{ph} becomes comparable with I_{dark} and I_{leak}. The influences of I_{dark} and I_{leak} are futher illustrated in Fig. 3.10, where there exists distortion when I_{leak} is not equal to I_{dark} in the low-light region. As a result, a design of equal I_{dark} and I_{leak} not only maximizes DR but also maintains

a linear charge integration for the PFM pixel in low-light regions.

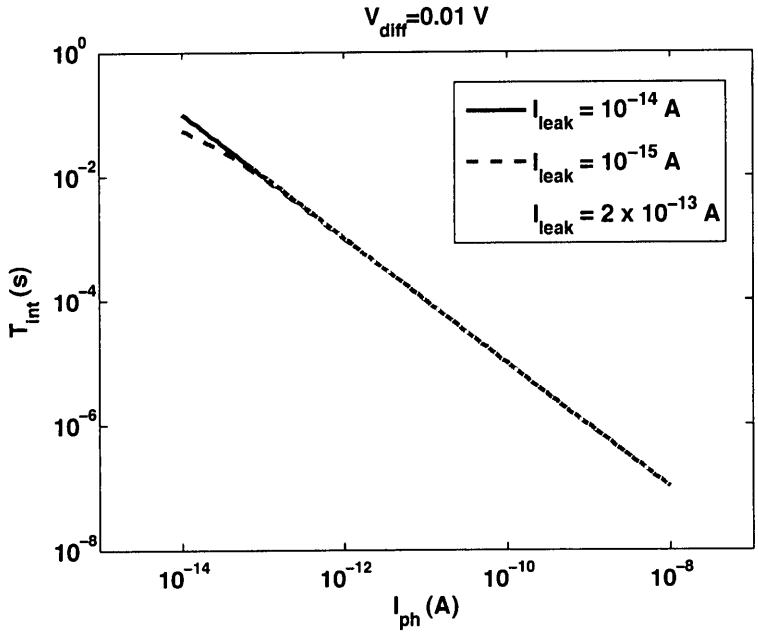


Figure 3.10: The modeled T_{int} with different I_{leak} values. I_{dark} is set to 10^{-14} A.

3.3.4 Integration Delay (T_{ID})

The integration delay of a PFM pixel is a period that is often ignored but can be important. It defines a short period of time right after the actual charge integration completes. In general, when V_{PD} drops below V_{ref}, the comparator will generate a trigger signal to begin the self-reset process to re-start the integration. Ideally, the comparator outputs the signal at the instant that V_{PD} becomes lower than V_{ref} (assuming its DC gain and slew rate are infinite), so T_{ID} is almost zero and can be dropped out of the analysis. However, the DC gain and slew rate are finite, making

T_{ID} significant. Although T_{ID} is a necessary period that allows the comparator to respond properly, an overlong one potentially degrades the signal linearity and is not preferred. As a result, a detail analysis of T_{ID} is necessary to understand its impact.

The analysis of T_{ID} is not straightforward since it is a composite of the static and dynamic responses of the comparator. In fact, we believe T_{ID} includes the time (T_{rpd}) required by the comparator to respond to the input (i.e., when the difference between V_{ref} and V_{PD} is big enough) and the propagation delay time (T_p) for charging the output of comparator from V_{SS} to roughly half of V_{DD}, as Fig. 3.9 shows. As a result, we suggest that T_{ID} is particularly affected by the DC gain and bandwidth of the comparator.

In Fig. 3.11, the simulated T_{ID} is plotted with different values of V_{diff} and I_{ph} (the simulations are performed using HSPICE). The technology used is the same 0.18-μm CMOS technology used for chip fabrication. From the results, two phenomena can be observed. First, T_{ID} is almost independent of V_{diff} since different V_{diff} levels do not greatly change the characteristics of the comparator within the used voltage range. Second, T_{ID} decreases as I_{ph} gets larger, which is reasonable due to the fact that a higher I_{ph} discharges C_{PD} faster. In addition, we notice that T_{ID} does not always decrease linearly with increasing I_{ph}, which is the cause of nonlinearity. Therefore, it can be understood as the consequence of the propagation delay time

of the comparator and will be carefully analyzed with modeling derivation and measurement.

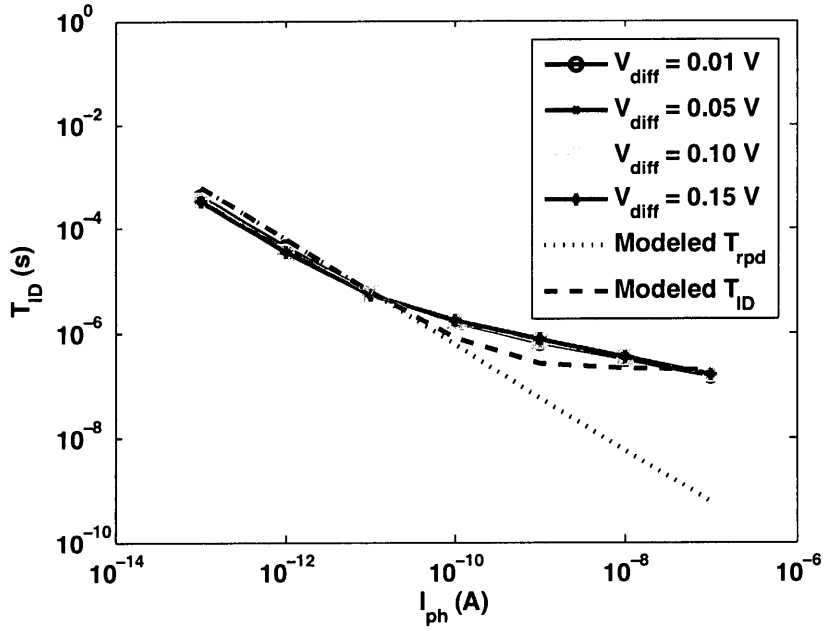


Figure 3.11: The simulated and modeled T_{ID}. The dotted line is only the T_{rpd}, and the dashed line is the combination of T_{rpd} and T_{p}.

The nonlinearity of T_{ID} in this figure suggests that at least two mechanisms are responsible for the complete behavior, similar to what we discussed previously. Therefore, we use the two defined terms, T_{rpd} and T_{p}, to describe these mechanisms, and they will be analyzed accordingly. First, the analysis of T_{rpd} starts with its behavior, which is the short period of time required for V_{PD} to discharge until the difference between itself and V_{ref} is big enough to trigger the comparator. As a result, the minimum input voltage difference ($V_{\mathrm{in.min}}$) between V_{PD} and V_{ref} to

invert the comparator output from V_{SS} to $\frac{1}{2}V_{DD}$ is given by

$$V_{in.min} = \frac{\frac{1}{2}V_{DD} - V_{SS}}{A_V} \tag{3.5}$$

where A_V is the DC gain of comparator. Therefore, T_{rpd} is derived from (3.5) and written as

$$\begin{aligned} T_{rpd} &= \frac{C_{PD} \cdot V_{in.min}}{(I_{ph} + I_{dark} - I_{leak})} \\ &= \frac{C_{PD} \cdot (\frac{1}{2}V_{DD} - V_{SS})}{A_V \cdot (I_{ph} + I_{dark} - I_{leak})} \end{aligned} \tag{3.6}$$

According to the equation, T_{rpd} decreases proportionally when I_{ph} increases in the low-light region, like the simulated result shown in Fig. 3.11 (the dotted line). However, as I_{ph} gets larger, there is a bending shown in the simulated lines which is not modeled by T_{rpd}, and is explained by the propagation delay time (T_p). The modeling of T_p involves the small-signal behavior of the comparator, which starts by assuming a unit step signal, V_{in}, as the input for the comparator. Although the comparator in our design has more than one pole, we find by simulation that the dominant pole is far away from the second pole and therefore we approximate it to be a single-pole system. As a result, T_p is derived from the comparator transfer function and simplified as

$$T_{\mathrm{p}} = \tau_{\mathrm{c}} \cdot \left(\frac{1}{1 - \frac{V_{\mathrm{in,min}}}{2 \cdot V_{\mathrm{in,min}}}}\right) = \tau_{\mathrm{c}} \cdot \ln(2) \tag{3.7}$$

where τ_{c} is the time constant of comparator. By combining (3.6) and (3.7), a modeled T_{ID} is shown (the dashed line in Fig. 3.11). By comparing the simulated and modeled T_{ID} lines, we find this simplified model roughly describes the response and sets the lower bound of T_{ID} which can be used to analyze the impact on signal linearity. There is a little mismatch when I_{ph} gets higher and it is believed to result from the ignored higher-order effects of the comparator.

We further define the total integration period (T_{INT}, or $T_{\mathrm{int}} + T_{\mathrm{ID}}$) as the period between the start of photocurrent integration (when reset is turned off) and the start of reset process (when reset is turned on) to compare the ideal and actual integrations, i.e., T_{int} and T_{INT}. In Fig. 3.12, the measured results of ($T_{\mathrm{int}} + T_{\mathrm{ID}}$) with respect to different illuminations and V_{diff} are shown, and the dotted lines (T_{int}) are the results where T_{ID} is subtracted. According to this figure, there is consistency between the modeling and measurement, where a linear response of T_{INT} exists at the low-light (illumination or I_{ph}) region and a departure from linearity occurs when the light intensity gets stronger. The pure integration curves, without the integration delay T_{ID}, are relatively linear, as expected. In addition, it is clear from the figure that a larger V_{diff} leads to a higher linearity, which is due to the proportionally increased T_{int} that makes T_{ID} less significant. We can also conclude

that the nonlinearity is supposed to be prominent when a stronger illumination is applied.

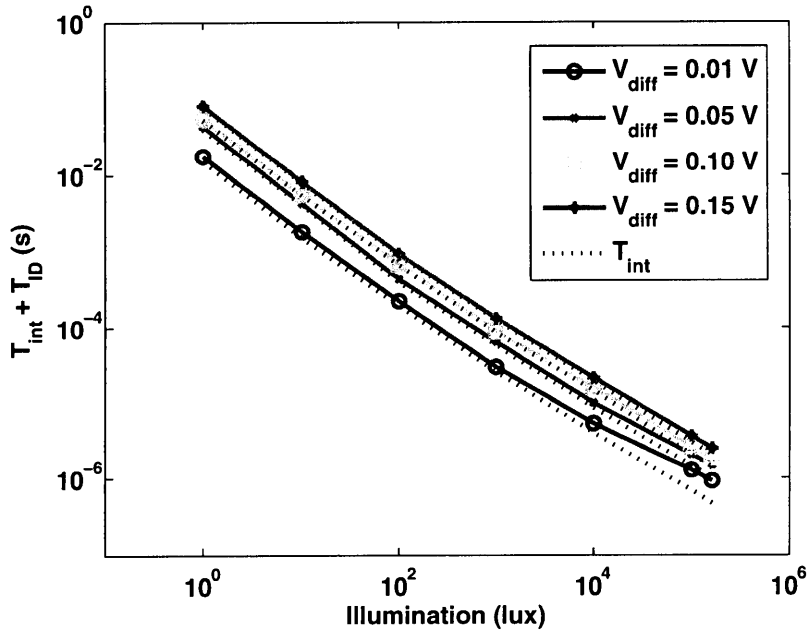


Figure 3.12: The measured $T_{\text{int}} + T_{\text{ID}}$. The dotted lines are generated from subtracting T_{ID} to show the pure integration curve, which is linear throughout the entire region.

The reason that the signal linearity increases with V_{diff} is that the larger V_{diff} does not change T_{ID} but leads to a larger T_{int}. Thus, the ratio of T_{int} to T_{ID} becomes larger and the linearity is barely affected by T_{ID}. However, choosing a higher V_{diff} sacrifices (decreases) the output frequency and limits the speed (frame rate) accordingly. On the other hand, the degraded linearity only occurs when the input illumination is large, which suggests that a smaller V_{diff} can still provide linear

imaging performance under the low-light conditions. As a result, the selection of V_{diff} ultimately depends on the frame rate, DR, and signal linearity requirement of each individual application.

To compare the individual effect of T_{rpd} and T_{p} on signal linearity in different illumination conditions, we generate Fig. 3.13 to separately display these two periods with respect to I_{ph}. V_{diff} is not a variable in this figure since it does not have any impact on T_{ID} or the signal linearity as previously discussed. According to this figure, the responding time T_{rpd} decreases proportionally as I_{ph} increases, while the propagation time T_{p} is a constant in the entire illumination range. Therefore, we can conclude that the root cause of signal nonlinearity is the propagation delay time (T_{p}), one component of T_{ID}. When T_{rpd} and T_{p} become equal at around $I_{\text{ph}} = 10^{-10}$ pA, the effect of T_{p} starts to degrade the linearity. Since T_{p} is the primary problem, it is obvious that the linearity can be improved by pushing the dominant pole of comparator further back. As such, τ_{c} will be reduced and T_{p} will become shorter. This method will, however, inevitably increase the cost (in terms of pixel area and power) to implement such a comparator in a PFM pixel. Nevertheless, the trade-off between τ_{c} and the cost of comparator has to be determined with respect to performance requirements when designing a PFM pixel, especially if the linearity is considered.

From the above analysis and modeling, we discover the existence of T_{ID} as well

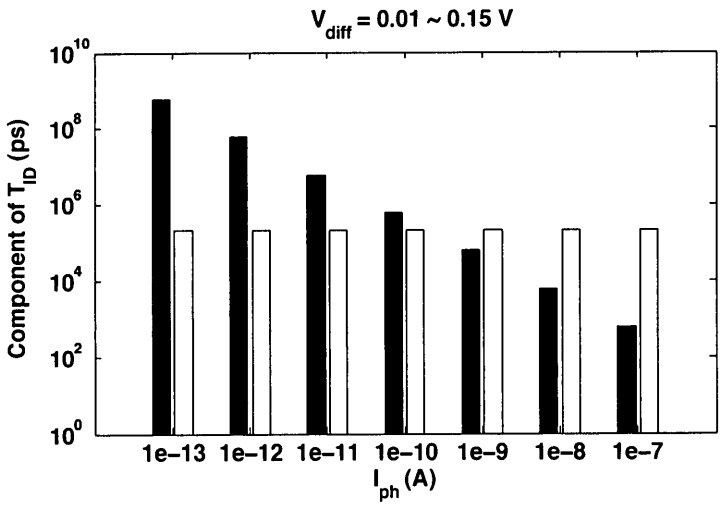


Figure 3.13: The comparison of simulated T_{rpd} (decreases as I_{ph} gets higher) and T_{p} (remains constant) of T_{ID}. The black and white rectangles represent T_{rpd} and T_{p}, respectively.

as its impacts to signal linearity under different operating or lighting conditions. This conclusion will help understand the detail of charge integration of a PFM pixel and provide useful design strategies for different purposes.

3.3.5 Reset Period (T_{rst})

In a PFM pixel, the reset operation is often considered ideal (as a very short period) and neglected, but its presence does affect the overall signal linearity. First, we define T_{rst} as the period (i.e., the on interval of the reset transistor) for a complete reset process. When the reset transistor is turned on, the reset current (I_{rst}) starts charging C_{PD} with a target of V_{rst}. The completion of reset is supposed to make the comparator output flip over again to turn off the reset transistor, and the

reset process is completed. In this study, we consider that the reset period can be determined by the charging time of C_{PD} from V_{ref} to V_{rst} (called T_{ch}) and the propagation delay time of comparator (T_{pr}), which will be discussed accordingly. The charging time T_{ch} primarily depends on the magnitudes of T_{ID} and V_{diff} since the total integrating voltage includes both the excess voltage drop due to T_{ID} and V_{diff}. This period is also affected by I_{ph} and I_{rst}, which determines the speed of charging. As a result, T_{ch} is calculated by dividing the total accumulated charges at C_{PD} within $(T_{ID} + T_{int})$ by the net reset current, $I_{rst} - (I_{ph} + I_{dark})$, and it can be written as

$$T_{ch} = \frac{C_{PD} \cdot V_{diff} + (I_{ph} + I_{dark} - I_{leak}) \cdot T_{ID}}{I_{rst} - (I_{ph} + I_{dark})} \tag{3.8}$$

where a constant, net reset current throughout the entire process is assumed to simplify the derivation. In addition, according to the fundamental transistor current model, I_{rst} is further written as

$$I_{rst} = \mu_p \cdot C_{ox} \cdot \frac{W_{rst}}{L_{rst}} \cdot [(V_{DD} - V_{tp}) \cdot V_{diff} - \frac{V_{diff}^2}{2}] \tag{3.9}$$

where the reset transistor is in the triode region, μ_p is the mobility constant, C_{ox} is the dielectric constant, W_{rst} and L_{rst} are the width and length, V_{tp} is the threshold voltage, of the reset transistor. In (3.8), since T_{ID} is almost independent of V_{diff}, i.e. the latter numerator remains constant, T_{ch} is smaller when V_{diff} is chosen to be

small. In addition, an even much smaller T_{ch} is also available by either decreasing T_{ID}, achieved by allowing a larger pixel area and higher power consumption (thus propagation delay reduces), or maximizing I_{rst} resulted from a thin-oxide gate reset transistor.

Although the start of propagation delay T_{pr} is not explicitly identified, we assume it begins when the charging period T_{ch} completes to proceed with the analysis. A step input, V_{diff}, at C_{PD} is assumed again to simplify the derivation. Similar to the way we derived (3.7), T_{pr} is written as

$$T_{\text{pr}} = \tau_{\text{c}} \cdot \ln\left(\frac{1}{1 - \frac{V_{\text{in.osc}} + V_{\text{ex}}}{2 \cdot (V_{\text{diff}} + V_{\text{ex}})}}\right) \tag{3.10}$$

where $V_{\text{in.osc}}$ is the minimum input voltage to enable the reset process, and V_{ex} is the extra voltage room created by the period of T_{ID} and written as

$$V_{\text{ex}} = \frac{(I_{\text{ph}} + I_{\text{dark}} - I_{\text{leak}}) \cdot T_{\text{ID}}}{C_{\text{PD}}} \tag{3.11}$$

From (3.10), T_{pr} is strongly related to V_{ex} and may be very small when the value of $(V_{\text{in.osc}} + V_{\text{ex}})/[2 \cdot (V_{\text{diff}} + V_{\text{ex}})]$ is small. In fact, this happens when V_{ex} is small, and I_{ph} has to be small under this condition according to (3.11).

Although T_{pr} should explain the behavior of T_{rst} quite well, we find there is another phenomenon existing inside T_{rst} which has to be considered for low-light conditions. Despite of the propagation delay time, the comparator has to charge

C_{PD} with a limited amount of current when reset, therefore its slew rate might further restrict T_{rst}. The period constrained by the slew rate is defined as T_{SR}, which is the lower boundary of T_{rst} and defined as

$$T_{SR} = \frac{C_{la} \cdot A_V \cdot V_{in.osc}}{I_{out}} = \frac{A_V \cdot V_{in.osc}}{SR} \tag{3.12}$$

where C_{la} is the latch input capacitance, and I_{out} and SR are the output current and slew rate of the comparator, respectively. As a result, the total reset period T_{rst} can be given by

$$T_{rst} = T_{ch} + T_{pr} + T_{SR}. \tag{3.13}$$

Note that the slew rate is not considered in the analysis of T_{ID} since the other two analyzed periods (T_{rpd} and T_p) are relatively large and therefore it is neglected to simplify the work.

Fig. 3.14 shows that the simulated (solid lines) and modeled (dashed lines) T_{rst} have good consistency across different values of I_{ph} and V_{diff}. According to the curves, T_{rst} has a nearly constant value when I_{ph} is relatively small and an increasing trend at large I_{ph}. This phenomenon is consistent among different V_{diff}. According to (3.8), (3.10) and (3.12), we find T_{ch} is almost negligible unless I_{ph} is very close to I_{rst}, or $I_{ph} > I_{rst}/10$, which is not a case that could happen in practice (i.e., $I_{ph} > 10^{-6}$ A). As a result, T_{ch} can be of no (or very low) impact on

T_{rst}. Actually, the difference of T_{rst} among various V_{diff} levels is primarily affected by V_{diff} itself since the larger the step input for the comparator, the faster the T_{pr}. Besides, the increase of V_{ex} with I_{ph} due to the nonlinear T_{ID} causes the increased T_{pr} because the minimum input required by the comparator also increases with V_{ex}. In addition, the lower boundary of T_{rst} at the low-light region (where T_{pr} is small) is dominated by T_{SR}. Overall, the increasing T_{rst} is driven by V_{ex} which is directly controlled by T_{ID}, according to (3.11).

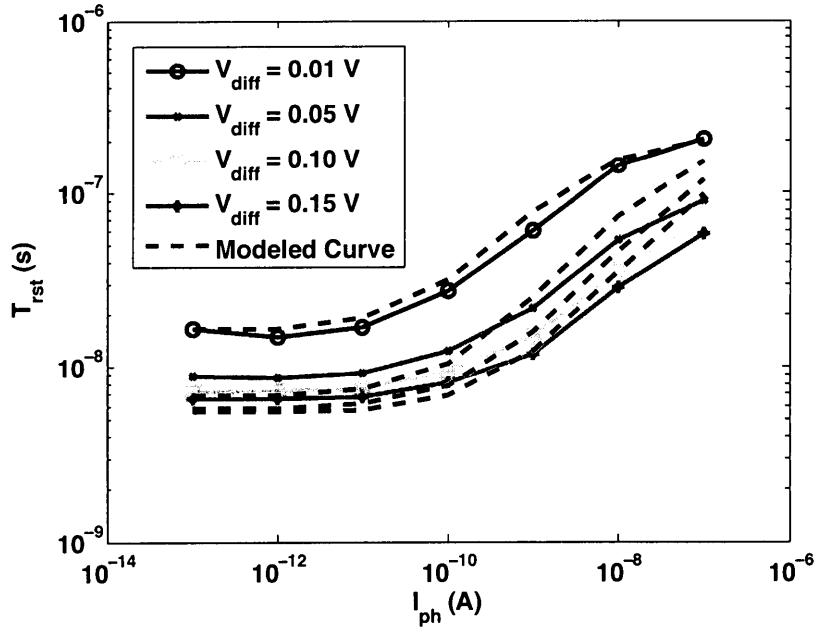


Figure 3.14: The simulated T_{rst} with different V_{diff} levels. The dashed lines are computed from the modeling through (3.8) to (3.13).

In order to support the simulation and modeling results, the measurement results of T_{rst} are collected with the same V_{diff} values and plotted in Fig. 3.15. Al-

though the plotted curves are not smooth (due to the resolution limit and quantization noise of instrument), the results are still consistent with the simulations and support the correctness of the modeling. In addition, T_{rst} is not likely to decrease at the low-light region even with a very large V_{diff} since T_{SR} is nearly constant and is not controlled by V_{diff}.

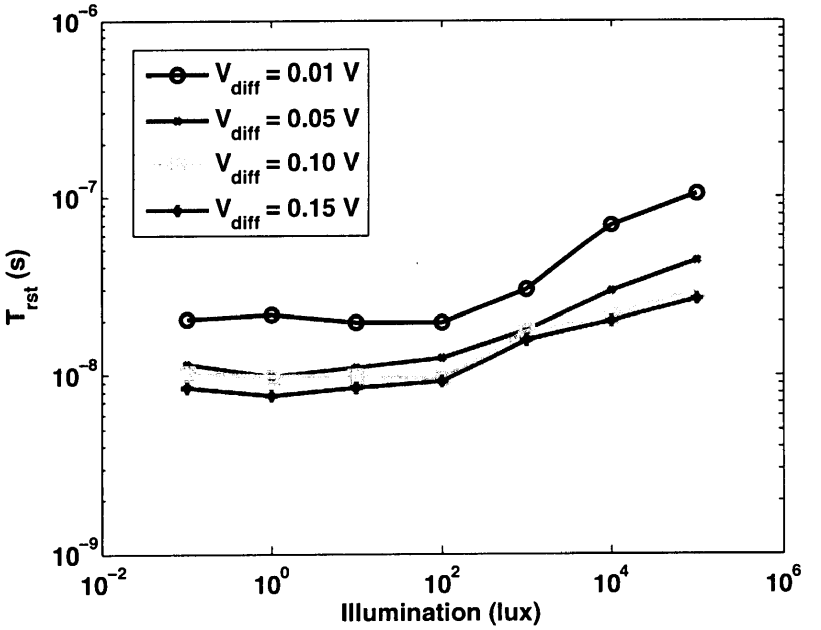
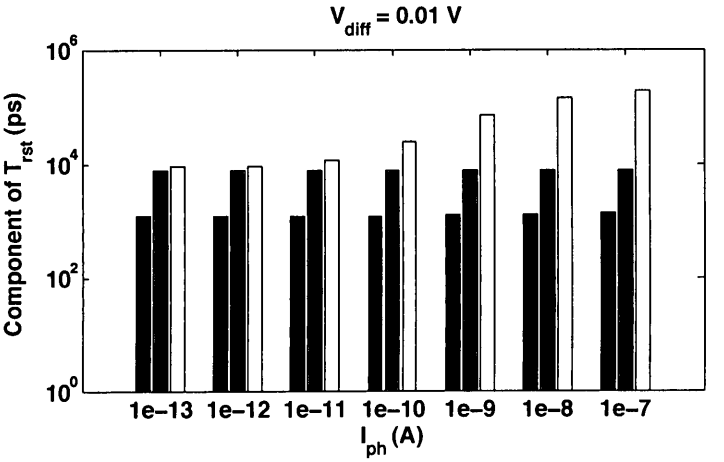


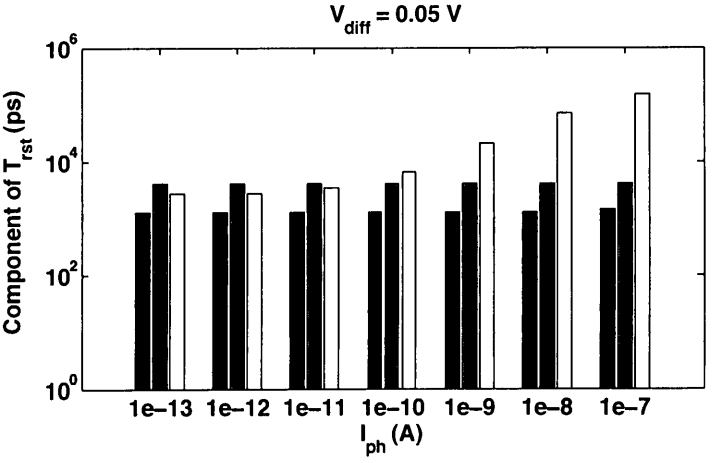
Figure 3.15: The measured T_{rst}. The resolution of the mixed-signal oscilloscope is set to 1 ns to measure the length of each reset period. T_{rst} remains constant and starts increasing when the illumination gets stronger; it also increases with a smaller V_{diff}.

In order to further realize the impacts of T_{ch}, T_{pr}, and T_{SR} on the total reset period T_{rst} at different V_{diff} and I_{ph} levels, we separate their values from modeling and plot those having the same V_{diff} with respect to different I_{ph}, as shown in Fig. 3.16.

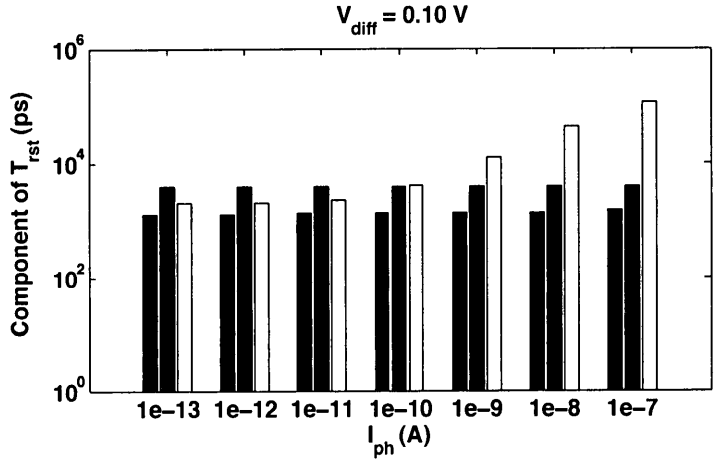
The results with $V_{\text{diff}} = 0.01$–0.15 V are shown in Fig. 3.16(a) to Fig. 3.16(d). There are several observations we can conclude from these figures. First of all, T_{ch} is constant (with respect to I_{ph}) and can be neglected unless V_{diff} is very large, which is not the case discussed here. Second, T_{SR} is also constant as I_{ph} increases, and it has influence at low I_{ph} values, especially when V_{diff} is large. Third, T_{pr} increases as I_{ph} increases, so it dominates at the high I_{ph} values; at the low I_{ph} values, it is only prominent when V_{diff} is small. In general, these findings lead to a conclusion that both T_{SR} and T_{pr} play important roles in determining T_{rst}, which is a factor of the signal nonlinearity of a PFM pixel. When a small V_{diff} is used, T_{pr} is the most dominant component of T_{rst}; on the contrary, T_{SR} has to be considered with T_{pr} when a large V_{diff} is used. The influences of these analyzed components are not straightforward, rather a mutual and complex relationship that exists among these variables has been studied and discussed, and it can be used or adopted toward any designs using this type of PFM pixel.


V_{diff} = 0.01 V
10^6
10^4
10^2
10^0
Component of T_{rst} (ps)
1e−13 1e−12 1e−11 1e−10 1e−9 1e−8 1e−7
I_{ph} (A)

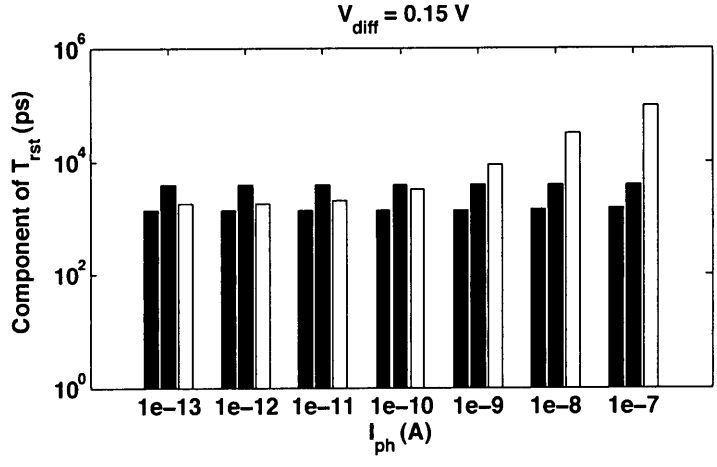
(a)


V_{diff} = 0.05 V
10^6
10^4
10^2
10^0
Component of T_{rst} (ps)
1e−13 1e−12 1e−11 1e−10 1e−9 1e−8 1e−7
I_{ph} (A)

(b)



(c)



(d)

Figure 3.16: The comparison of simulated T_{ch} (remains constant), T_{SR} (remains constant and decreases with a large V_{diff}), and T_{pr} (increases as I_{ph} gets stronger or with a small V_{diff}) of T_{rst} with (a) 0.01, (b) 0.05, (c) 0.10, and (d) 0.15 V V_{diff}, respectively. The black, grey, and white rectangles represent T_{ch}, T_{SR}, and T_{pr}, respectively.

3.3.6 Overall Linearity

The overall signal linearity of a PFM pixel is evaluated by considering the effects of T_{ID} and T_{rst} with the integration period T_{int}. Based on the simulation results, T_{int} is plotted in the same graph with T_{ID} and T_{rst} and shown in Fig. 3.17. To clarify the impacts, only those results with 0.01- and 0.15-V V_{diff} are displayed in this figure. As the figure shows, T_{ID} intersects T_{int} at some point when I_{ph} gets higher. In addition, and more problematically, this happens at a lower I_{ph} level, when a small V_{diff} is chosen, since T_{int} becomes smaller but T_{ID} does not change with V_{diff}. The reason that T_{int} intersects T_{ID} is that it does not decrease proportionally to T_{int} at larger values of I_{ph}, as indicated by (3.5) to (3.7). Nevertheless, choosing a small V_{diff} will definitely increase the speed of PFM pixel but decrease the linearity of imaging at the high-light region.

On the contrary, T_{rst} has a different mechanism, and generally increases with I_{ph}. It is relatively small compared to T_{ID} and can be neglected when I_{ph} is small. However, it keeps increasing as I_{ph} increases and eventually crosses T_{ID}. Unlike T_{ID} which simply degrades the signal linearity, the increasing T_{rst} causes T_{pul} to increase, rather than to decrease as designed, with I_{ph} after T_{rst} crosses T_{ID}. In other words, the crossing point determines the upper DR boundary, and it becomes lower in the x-axis with a smaller V_{diff}. In summary, a small V_{diff} causes more nonlinearity of the

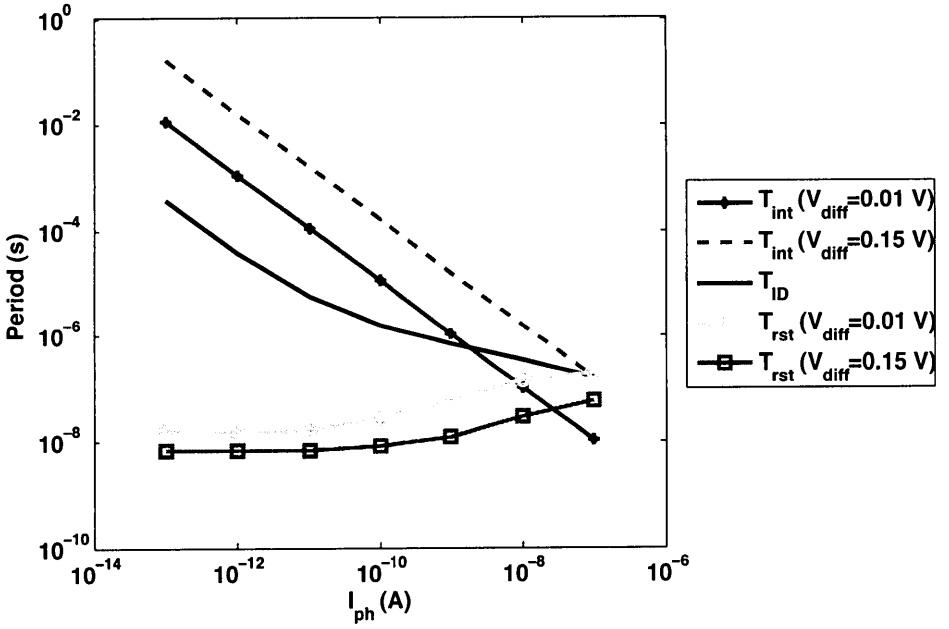


Figure 3.17: The comparison of the three time periods (T_{int}, T_{ID}, and T_{rst}) with V_{diff} of 0.01 and 0.15 V, respectively. T_{ID} is the same regardless of V_{diff}.

signal and a lower DR. This finding is important since it was not expected before the measurement was performed. It is believed that the problem can be solved if T_{ID} is optimized by using a higher-bandwidth comparator. This phenomenon has to be taken into consideration when designing a WDR image sensor, in particular for high-light imaging.

We also performed a detailed measurement to observe the signal nonlinearity using a step of 0.01 V for V_{diff} from 0.01 to 0.15 V. The measurement results are shown in Fig. 3.18, along with the ideal curve (the dashed lines), which only considers the integration period (T_{int}) and leaves T_{ID} and T_{rst} ignored. The left-

most line in the figure is measured with a 10-lux illumination intensity, and the right-most one is 100,000 lux, to cover a DR of 80 dB.

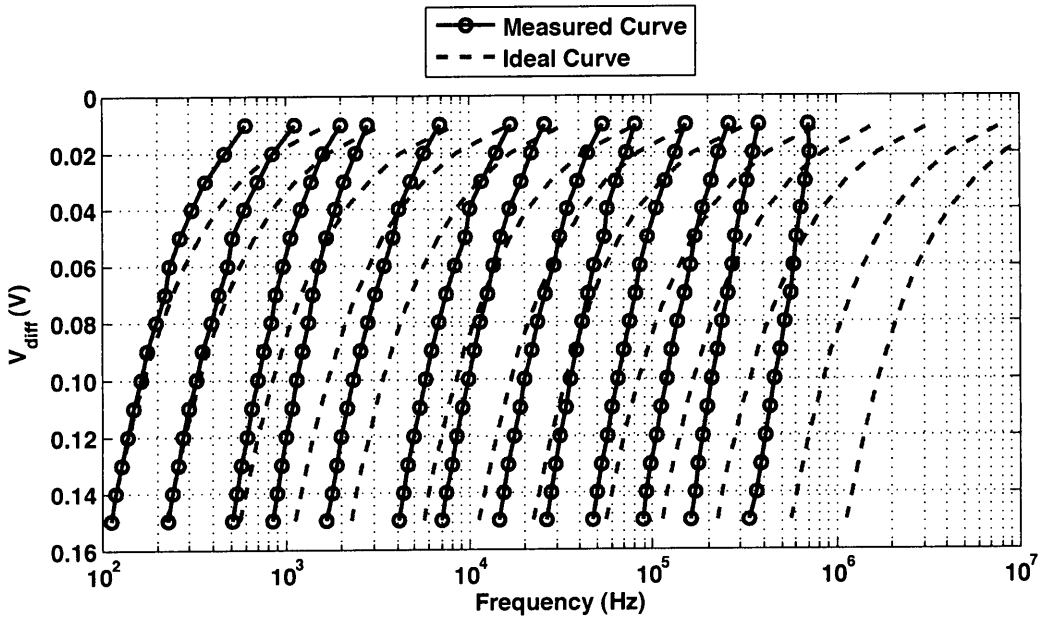


Figure 3.18: The measured relationship between V_{diff} and signal output frequency with different illuminations. The dashed lines present the ideal conditions, only taking T_{int} into account.

In this figure, it is observed that the output frequency (both measured and ideal) increases as V_{diff} decreases since the necessary accumulated charges to complete each integration is proportional to V_{diff}. The output frequency also increases when the illumination is stronger. By comparing the two groups of curves, we notice that there is a drop of frequency, which is attributed to the impact of T_{ID} according to the previous analysis and is associated with two phenomena. Firstly, the output frequency does not increase as expected when V_{diff} gets smaller (the two

left-most curves). Secondly, the actual output frequency becomes much lower than the ideal curve with increasing illumination (e.g., all curves with 0.15-V V_{diff}). The frequency loss of the signal is between 2 to 20 times according to the measurement results. Overall, the presence of T_{ID} limits the pixel from achieving higher output frequencies.

3.4 Temporal Noise and Overall Consideration

The PFM pixel produces pulse signals rather than a voltage output, unlike the APS. Accordingly, the temporal noise measurement is conducted by obtaining the root-mean-square (r.m.s.) offset error of a series of pulse signals. For all pulse signals with the same illumination, the average noise is a combination of photon shot noise, reset noise, comparator input-referred noise, latch noise, and substrate induced noise [90]. In this work, we only consider the shot noise and reset noise, which are the dominant noise sources in regular CMOS image sensors [35]. In addition, the error is measured with respect to the signal frequency, which is the reciprocal of the pulse width (T_{pul}), and the integration voltage (V_{diff}), since these two parameters directly affect pixel performance. The illumination intensity and V_{diff} used in the measurement are equal to those used in Fig. 3.18. Each single measurement samples 1,000 pulses to obtain the average output frequency and r.m.s. error. An example of the measurement is shown in Fig. 3.19, consisting of

the interval of every integration with three different V_{diff}, including 0.01, 0.08, and 0.15 V.

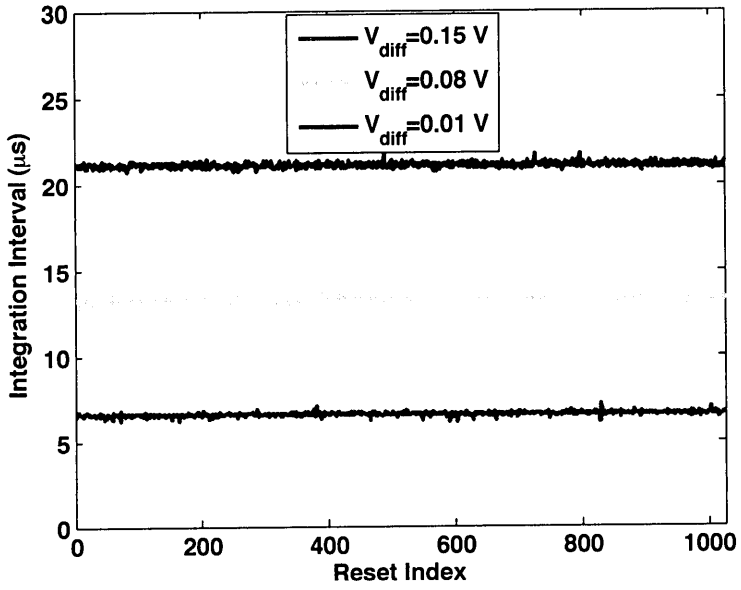


Figure 3.19: Measured interval of every single integration of a PFM pixel with V_{diff} of 0.01, 0.08, and 0.15 V, respectively.

The error in percentage of each point of the data is used to plot the 2-D noise graph shown in Fig. 3.20. According to this figure, the offset level is lower if a large V_{diff} is chosen and higher if a small V_{diff} is selected. The result is consistent with the conventional noise analysis for regular CMOS active pixels when only the reset and shot noise sources are considered, which can be given by [35]

$$\overline{V_{\text{n.rst}}^2} + \overline{V_{\text{n.shot}}^2} \approx \frac{kT}{C_{\text{PD}}} + \frac{q(I_{\text{ph}} + I_{\text{dark}})}{C_{\text{PD}}^2} \cdot (T_{\text{int}} + T_{\text{ID}}) \tag{3.14}$$

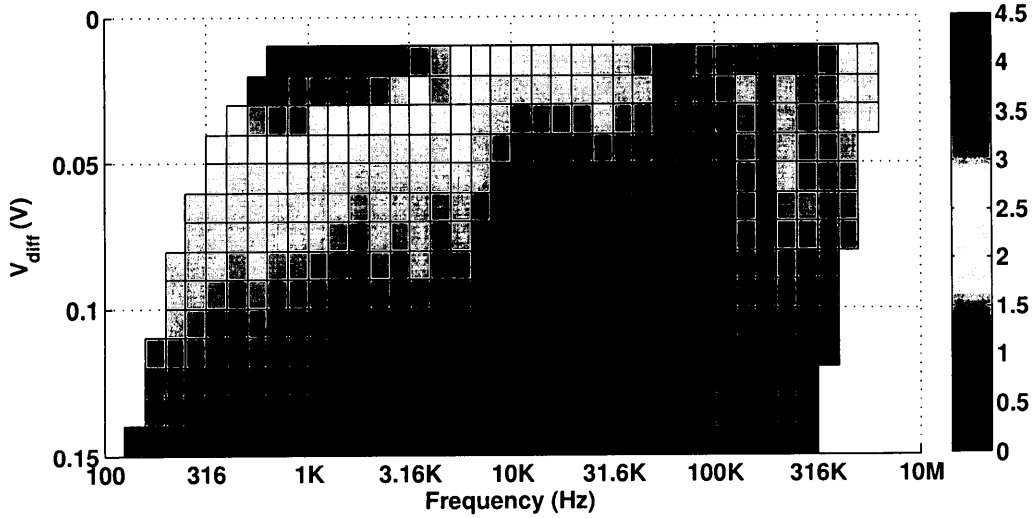


Figure 3.20: The measured PFM pixel temporal noise. The r.m.s. error is plotted with respect to V_{diff} and the self-reset frequency.

where k is the Boltzmann constant, T is the temperature in Kelvin, and q is the electronic charge. In the PFM pixel, V_{diff} can be regarded as a variable reciprocal to T_{int}. As a result, when V_{diff} is larger, the SNR is expected to increase according to (3.14). Although this formula predicts the noise floor well, part of it is higher than expected, exceeding 3% or more when the illumination is below 100 lux and the pulse frequency is below 1 kilohertz (kHz). The extra noise, which is not predicted by using the conventional pixel noise model, is believed to be the result of a higher flicker, or $1/f$, noise when it operates at low frequencies. The top of the noise floor surface is around 4.5% and is located at the most top-left where a 10-lux illumination is applied and a 0.01-V V_{diff} is used. The noise floor gradually declines

either with a stronger illumination or a larger V_{diff} to a value of about 1%. Note that the increasing noise at higher illuminations (over 100-kHz output frequency) is possibly due to the unstable light source. This graph shows a clear relationship between the noise, V_{diff}, and output frequency of the PFM pixel. It also suggests that the $1/f$ noise should be taken into consideration for the PFM pixel applications which focus on WDR imaging or operates at low frequencies. A three-dimensional (3-D) noise surface graph, shown in Fig. 3.21, is further generated to show the noise distribution over different frequencies and V_{diff}.

It is notable that the final output is usually a result of accumulated samplings and subject to a SNR improvement of $\sqrt{N}$ [91], where N is the number of samplings. This can be seen in Fig. 3.22, which shows a square-root-decreasing behavior of the noise. This figure suggests that the SNR can theoretically reach as high as 70 dB when the number of resets exceeds 1,000 (see Fig. 3.23).

The results indicate that the SNR performance of a PFM pixel can be very high if the sampling method is based on the counting of resets, achieves over 60 dB without difficulty. However, it is not observed in a real image since there exists other noise sources that will degrade the image quality or SNR. These sources will be further investigated in a later chapter where the design of a complete CMOS image sensor is introduced.

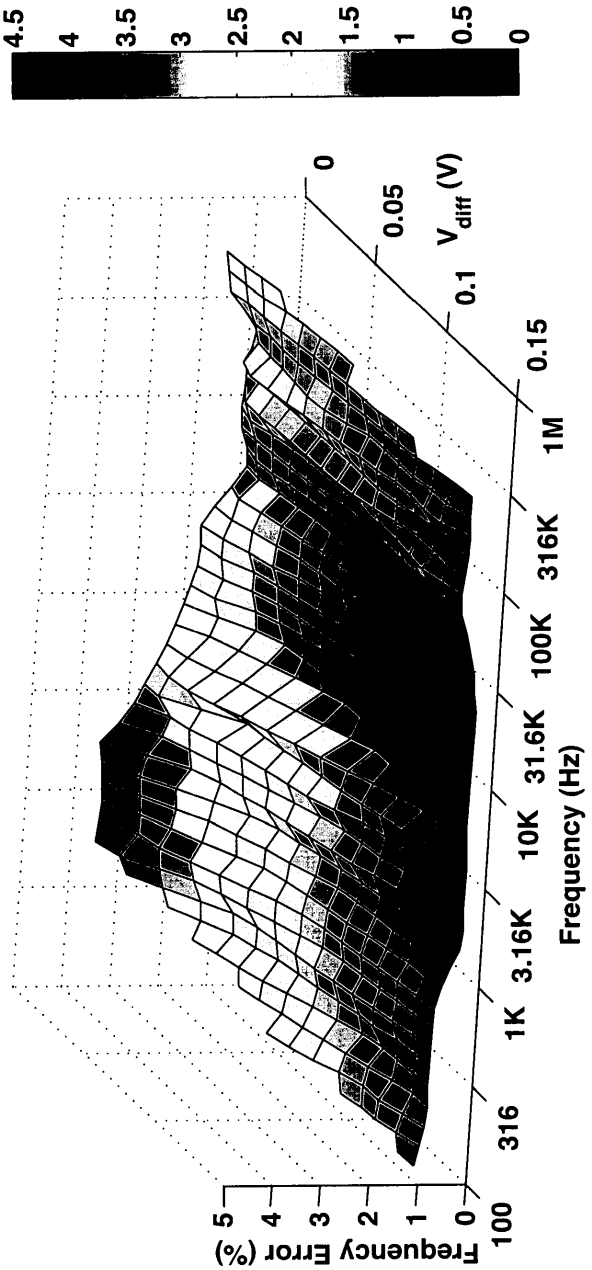


Figure 3.21: The 3-D temporal noise surface of Fig. 3.20.

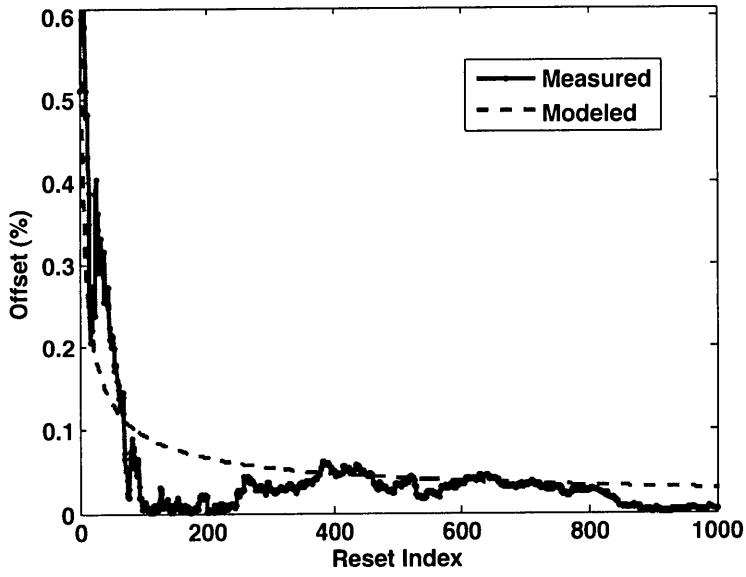


Figure 3.22: The r.m.s. offset of the result in Fig. 3.19, using the cumulative offset ($V_{\text{diff}} = 0.8$ V). The dashed line is generated following the $\sqrt{N}$ rule.

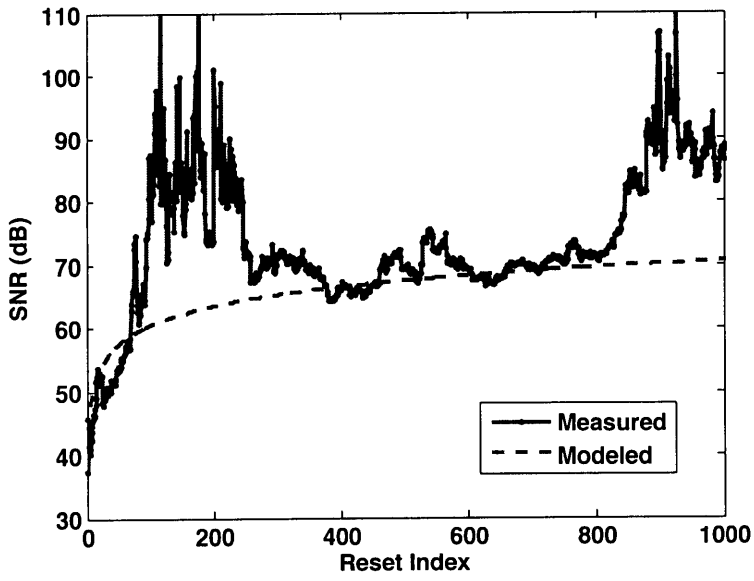


Figure 3.23: The calculated SNR of Fig. 3.22.

3.5 Summary

In this chapter, a complete study, including theoretical analysis, circuit modeling and simulation, and pixel measurement, of the PFM pixel for a CMOS image sensor is presented. The scope of this research includes the study of DR, linearity, and temporal noise. Several pixel parameters are explored to investigate their effects on system performance. In addition, a PFM pixel using 0.18-μm CMOS process is tested to support this work.

The available DR in a PFM pixel is defined in terms of photodiode dark current I_{ph}, reset transistor leakage current I_{leak} and reset current I_{rst}. It is found the PFM pixel reaches 130- to 160-dB DR with typical sub-micron CMOS processes. The suggested design approach is that, while I_{leak} should be equal to I_{dark} to reach a maximum DR and keep the low-light information, the best choice ultimately depends on the systematic consideration. Signal linearity is thoroughly analyzed to incorporate all necessary variables. It is found that the integration delay time (T_{ID}) is the primary cause of signal nonlinearity. From the simplified circuit modeling and analysis, we conclude that a wide-bandwidth comparator, with a relatively higher-building cost, will effectively reduce T_{ID}. Reset period, T_{rst}, is not the major concern for nonlinearity, but it may disable the operation of PFM pixel when its value exceeds the integration time (T_{int}). As a result, it is a potential upper-DR

constraint. Noise performance with respect to V_{diff} and the output frequency is also examined. We graphically describe the noise response under different operating parameters using a 3-D noise model and find it consistent with the conventional noise modeling. The theory of $\sqrt{N}$ SNR improvement is also discussed, supported by the measurement result.

Although there exists different comparator topologies, the selected reference design properly meets the requirements for this investigation. A comparator can actually be built with fewer transistors which has a shorter propagation delay and lower power consumption, however this delay is necessary to ensure the correct operation of a PFM pixel. Without sufficient delay, the reset operation may not complete. In addition, the lower slew rate and gain will also directly or indirectly increase T_{ID} and T_{rst}. Dynamic comparators can also be integrated into the PFM pixel to reduce the power consumption, however a very high-speed clock signal, which may result in a serious clock feedthrough, is required to ensure every comparison is performed accurately without adding any delay to T_{int} and affecting the signal linearity. Overall, the reference comparator provides a propagation delay which is long enough to operate the PFM pixel correctly without generating excess noise from additional controls. As a result, the impacts from different parameters of comparator can be successfully studied and analyzed.

This chapter successfully investigates the PFM pixel with detailed circuit anal-

ysis and measurements from several performance aspects. Those design parameters of interest have been identified, and design suggestions or optimization methods are discussed. The content of this chapter is important in terms of providing necessary information for the development of PFM pixels.

4 Uniformity and DR Improvement of PFM Pixel

The analysis and optimization for the PFM pixel has been conducted and presented to assist its development toward appropriate applications [84]. Those important parameters, including DR, signal linearity, and noise have been carefully studied and the corresponding design strategies are discussed. However, a CMOS image sensor usually contains hundreds of thousands of pixels in order to generate an image. As a result, the PFM pixel is still not particularly favored in practice because of its relatively poor uniformity, or pixel-wise FPN, which is reported to be more than 5% [19, 73, 78, 92]. Non-uniformities in a typical APS are reduced by the CDS technique, but this approach is not directly applicable to the PFM pixel since it is only practical when operating in the voltage (charge) domain. An additional issue is that the high-light imaging range in a PFM pixel is degraded by the reset period, which deteriorates with illumination [84]. This problem is directly associated with the propagation delay of the comparator and can not be greatly

improved within any particular CMOS technology.

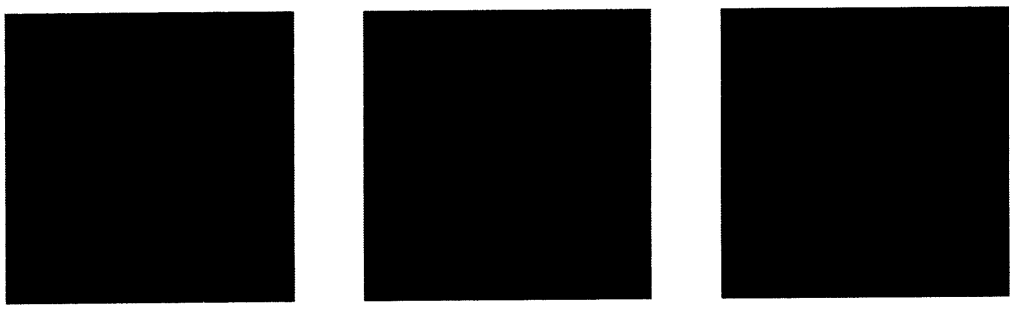
In this chapter, we design a double-delta compensating (DDC) technique in an effort to reduce the FPN and to extend DR for the comparator-based PFM pixels [93]. This technique, based on pixel switched-circuit design, is simulated to verify its feasibility in a common CMOS process. The concept of this technique will be throughly introduced, and the following context will demonstrate its circuit realization in different approaches. We also compare the simulation results for different designs and include explanations for performance differences in order to provide a path for future development.

4.1 Drawbacks of PFM CMOS Image Sensor

4.1.1 Sensor Uniformity of PFM Pixel

The non-uniformity of a CMOS image sensor includes pixel and column FPN, and sometimes row FPN, as discussed in Chapter 2. In general, these non-uniformities are generated from the mismatches between pixels (include both the photodiode and source follower), column readouts or analog-to-digital conversion characteristics, and the variation over the row-control signals. However, the behavior of a PFM pixel is different because it incorporates the signal digitization inside the pixel. As such, column-level mismatch does not exist since the readout will be in the

digital domain rather than in the voltage (analog) domain. As a result, the FPN of a PFM pixel is only pixel-wise, and no effort is required to handle the column (or row) FPN. Fig. 4.1(a) and Fig. 4.1(b) show the FPN difference of two images generated from a conventional APS and a PFM image sensor. Note the effect of pixel FPN of Fig. 4.1(b) is similar to the temporal noise of Fig. 2.9(a) but is not time-variant.



(a) (b) (c)

Figure 4.1: The simulated images (128 × 128) with (a) the pixel (1%), column (5%), and row (2%) FPN of a conventional APS, and (b) with pixel FPN (5%) of a PFM pixel. (c) The calibrated image of (a) with the column and row FPN removed.

Although Fig. 4.1(a) looks more unacceptable due to the various FPN sources, the column and row FPN can effectively be suppressed with either the circuit design or post-processing calculation. The calibrated image, shown in Fig. 4.1(c), removes those vertical and horizontal artifacts and results in a better visual appearance than Fig. 4.1(b). As a result, the FPN contained in the images from the PFM pixel has

to be carefully treated to improve its quality for display purposes.

As previously mentioned, the output pulse frequency of a regular PFM pixel is determined by (3.2). In order to generate a higher output frequency which is favored by many applications, a smaller V_{diff} is apparently necessary. However, the sensor uniformity will be seriously affected by the smaller V_{diff}, where its cause can be explained as follows.

The definition of (3.2) assumes the value of V_{diff} to be precisely controlled. In fact, this becomes problematic when the scope of discussion expands to a large pixel array rather than a single pixel. Even if an identical V_{ref} can be supplied to every pixel, a problem arises from the offset voltage of the comparator (V_{off}), which has a normal distribution with a mean value of approximately 5–15 mV, depending on the circuit design, layout strategy, and process control. Although comparator designs with a low offset voltage are available [94, 95], they are not directly usable by the PFM pixel due to their complexity or their operational mechanisms.

When V_{off} is taken into consideration, (3.2) will be rewritten as

$$T_{\text{pul.offset}} = \frac{C_{\text{PD}} \cdot (V_{\text{diff}} + V_{\text{off}})}{I_{\text{ph}}}. \tag{4.1}$$

where V_{off} can be positive of negative values. It is clear that the actual output pulse ($T_{\text{pul.offset}}$) is affected by the summation of both V_{diff} and V_{off} in (4.1). Therefore, once V_{diff} becomes small, V_{off} becomes relatively large and starts to affect the out-

put. The array-wise non-uniformity of V_{off} will eventually result in unequal pulse frequencies for the same illumination and therefore increase the FPN. Recent studies of the PFM pixel have confirmed this issue, reporting a FPN of at least 5%, which is unacceptably high for most applications [19, 75, 78, 81, 92]. As a result, an approach that solves the problems of using a small V_{diff} is necessary to better utilize the PFM pixels.

4.1.2 Self-Reset Operation Limited DR

The DR of a PFM pixel has been analyzed and modeled in Chapter 3, where the reset, leakage, and dark currents altogether determine its range. However, we also noticed that the reset period (T_{rst}) of each integration phase can not only degrade the signal linearity but can also reduce the total DR. This happens when T_{rst} crosses the integration delay period (T_{ID}) in the high-light region. Since this problem gets worse when a small V_{diff} is chosen, the actual DR of a PFM pixel may be reduced if a small V_{diff} is used.

In order to explicitly understand the cause of the limited DR, an illustration is shown in Fig. 4.2. As normally understood, the propagation delay of a comparator is due to the signal path between the input and output. In this case, it is from V^- to V_{OUT} since the photodiode signal is connected to V^-. First, we assume V^- is higher than V^+ (connected to V_{ref}) and V_{OUT} is low (nearly or equal to ground)

when the integration takes place. At this moment, V_A is higher than V_B since the current flowing through M_2 is smaller than that of M_1. Since the photocurrent continues discharging C_{PD}, V^- will fall below V^+ at some point, and V_A will start decreasing (and V_B increasing), driving V_C to decrease at the same time. When V_A drops below V_B, and V_C becomes lower than the threshold voltage of M_8, V_{OUT} will rise until its value enables the self-reset which charges V^- to a higher (than V^+) level. As such, the input signal has to pass several nodes (V_A–V_C) in the comparator to generate the final output, and the time involved within this process is the cause that leads to a limited DR in the high-light region. Although it is not applicable to every individual condition, the mechanism and root cause are similar and can be adapted to other designs using a different comparator structures.

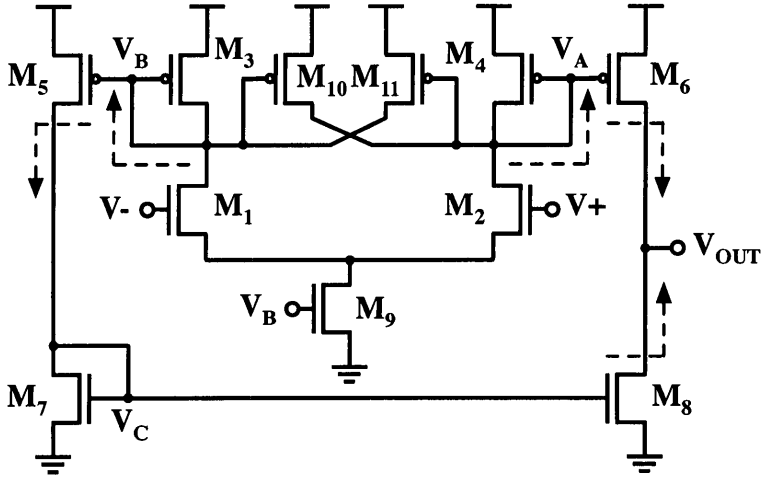


Figure 4.2: The circuit schematic of symmetrical OTA-based comparator with arrows indicating the signal path when the value of V^- drops across that of V^+.

The limitation of the DR can be further observed from the simulation. An example of the PFM pixel output (frequency) versus photocurrent is shown in Fig. 4.3. V_{diff} is 0.01 V and the simulated photocurrent range is 5 fA to 5 nA, a range of 120 dB. C_{PD} is 1 fF and V_{DD} is 1.2 V. The pixel schematic of simulation is the same as shown in Fig. 2.20. According to the result, the pulse-signal frequency increases as the photocurrent increases and starts to bend in the high-light region (due to the integration delay T_{ID}). However, it is clear that after the photocurrent reaches 1 nA, the output frequency starts to decrease, which is because of the overlong T_{rst}. This phenomenon reduces the DR which should have been more than 120 dB according to the analysis in Chapter 3.

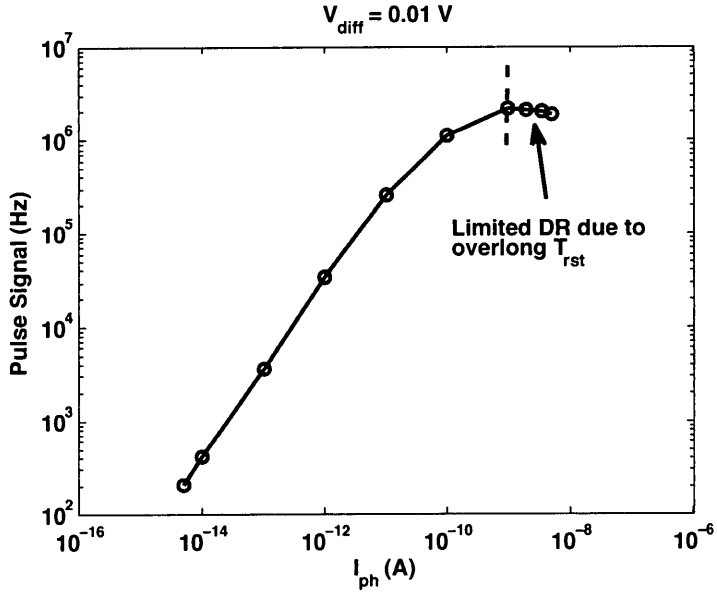


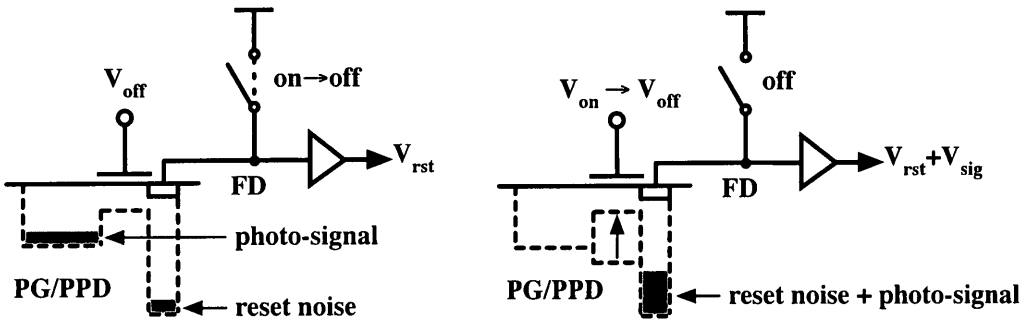
Figure 4.3: The simulated output frequency versus photocurrent. The upper bound of DR is indicated by the dashed line.

Obviously, if the propagation delay of comparator can be reduced, the DR will increase in the high-light region. However, the limitations of pixel size, power consumption, and operational method restrict the use of different comparator structures which have a lower propagation delay. Therefore, a new circuit design strategy is necessary that recovers the achievable DR without greatly changing the comparator design. The desired targets of the design include the small count of extra transistors and an unchanged operational principle of the PFM pixel.

4.2 DDC Technique

In a conventional APS, CDS is often implemented to remove the FPN, which is normally due to the reset noise and device mismatches [32, 88, 96]. Its idea is usually realized in the voltage domain, where the difference of two signals (photo and reset) is generated to represent the FPN-removed signal. Its concept is further explained by the illustration shown in Fig. 4.4.

In Fig. 4.4(a), the APS integrates the photo-signal in the PG or PPD, and by the end of this process a reset is executed to empty the FD. This operation, though, is not ideal, and a reset noise is generated at the FD. Followed by the completion of reset, a signal will be read out from the pixel, i.e. V_{rst}, which also includes any mismatch. After the readout, the photo-signal will be transferred from the PG or PPD to FD by turning on the transfer gate [Fig. 4.4(b)]. As such,



(a) (b)

Figure 4.4: The operation of CDS technique in an APS using the transfer gate. (a) The pixel output is only the reset noise (V_{rst}). (b). Photo-signal is transferred to FD and the pixel output is the reset noise plus photo-signal ($V_{\text{rst}} + V_{\text{sig}}$). The difference of these two readouts is the reset noise-free signal.

the FD will contain both the reset noise and photo-signal. When the transfer is completed, the pixel will output another signal, $V_{\text{rst}} + V_{\text{sig}}$, as the noise-included signal. Eventually, the two readouts will be subtracted to generate a reset-noise-free signal. Consequently, the FPN caused by the reset noise is removed using the CDS technique.

In a PFM pixel, this idea is not directly applicable because of the multiple integrations and because the signal conversion occurs in synchronization with the integrations. However, we find there is a possibility to implement the concept of CDS if the whole integration process is unfolded in the time domain. Since V_{off} of the comparator is often regarded as a voltage source at one of the two input nodes, it can actually be compensated within two consecutive integrations if the

input connections and the polarities of comparator are both switched. In addition, by creating the switching mechanism, the propagation delay can be potentially decreased since the signal path is virtually shortened. As a result, DR is expected to recover to its theoretically available level.

In order to solve the previously mentioned problems, we propose a DDC technique that implements a pixel-level circuit operation [93]. This idea is illustrated in Fig. 4.5, and its design perspective is explained accordingly. To facilitate the concept of a CDS-like behavior in the time domain, a switching operation of the comparator is designed as shown in the figure. The two modes illustrate the conditions between the switching operation, where V_{off} is connected to the positive node and V_{ref} (Mode 1) or the negative node and V_{PD} (Mode 2).

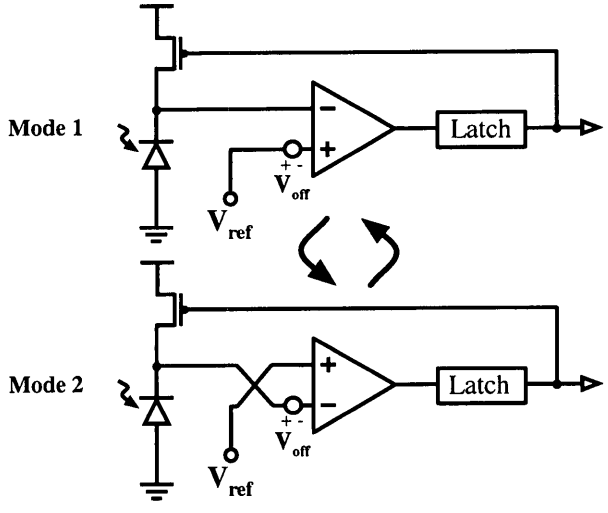


Figure 4.5: The concept of DDC technique. The pixel operation will change between two modes for each integration. The comparator has to switch its polarity while leaving the offset voltage where it is.

The most important feature of this approach is that V_{off} has to remain in the same place during the operation. This is because this offset voltage is intended to be cancelled within every two integrations, therefore it must be switched to V_{ref} and V_{PD} in sequence during any two signal integrations. As such, the comparator has to be modified to achieve this implementation. The idea of reducing the pixel FPN and increasing the DR will be discussed separately.

4.2.1 FPN Reduction

In Fig. 4.5, when the integration begins, the pixel is at the initial state (Mode 1). Since the offset voltage is attached to the positive input of comparator, the actual integration voltage is V_{diff} plus V_{off}. Thus, the potential of C_{PD} has to change an amount of $(V_{\text{diff}} + V_{\text{off}})$, or V^+, to trigger the comparator. Once the integration completes and the trigger signal is sent, the input connections and the polarities of comparator will be both exchanged, and the pixel is in the second state (Mode 2). Therefore, the next integration will have an integration voltage of V_{diff} minus V_{off}, and the potential drop of C_{PD} has to be $(V_{\text{diff}} - V_{\text{off}})$, or V^-, to trigger the comparator. After the second integration finishes and another trigger signal is generated, the input connections and the polarities of comparator will be switched back again (Mode 1). As the procedure repeats, every two integrations will have a total integration voltage given by

$$\begin{aligned} V^+ + V^- &= (V_{\text{diff}} + V_{\text{off}}) + (V_{\text{diff}} - V_{\text{off}}) \\ &= 2 \cdot V_{\text{diff}}. \end{aligned} \tag{4.2}$$

According to (4.2), V_{off} is cancelled within every two integrations using the DDC technique. In Fig. 4.6, the compensation of V_{off} is further illustrated by showing the voltage on C_{PD} (V_{PD}), where an ideal integration voltage (V_{ideal}) and two practical with V_{off} (V_{PD1}, V_{PD2}) are plotted. V_{ideal} is the ideal V_{PD} waveform without V_{off}, and V_{PD1} and V_{PD2} are the conditions with a negative and positive V_{off}, respectively. When the DDC technique is not used, the output frequency changes with the varying V_{off} (the dotted lines). V_{PD1} has a slower output frequency (since V_{diff} increases) and V_{PD2} becomes faster (since V_{diff} decreases). On the contrary, when applying this technique, V_{off} is compensated within every two consecutive integrations. The average frequencies of V_{PD1} and V_{PD2} (the solid lines) will equal that of V_{ideal} regardless of the value of V_{off}. As a result, the FPN is suppressed when the DDC technique is utilized in a PFM pixel.

The actual FPN reduction is also quantitatively derived. Based on the switching algorithm and assuming the readout block is a counter, the offset is completely cancelled when the count is even. If the count is odd, the offset will still be cancelled within every two integrations, but that due to the last single integration will remain

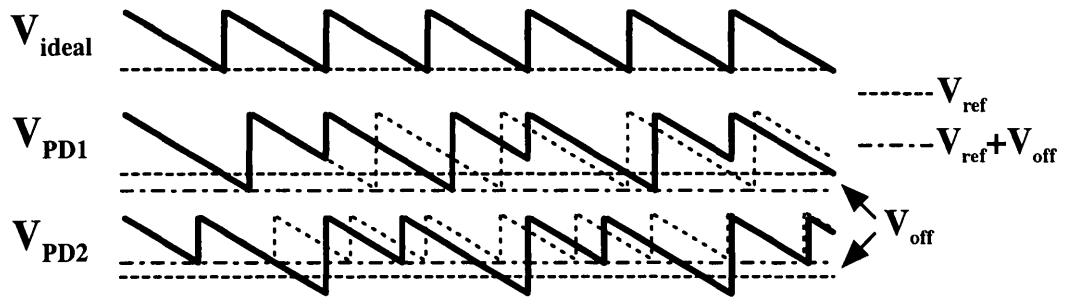


Figure 4.6: The illustration of FPN reduction process. The solid and dotted lines are the results with and without implementing the DDC technique, respectively. The horizontal dashed and dash-dot lines represent the levels of V_{ref} and V_{ref} plus any amount of V_{off}, respectively. By using the DDC technique, every second pulse is compensated by the switched V_{off} and remains synchronized with the ideal waveform (the solid lines of V_{ideal}, V_{PD1} and V_{PD2}), whereas without DDC the signals continually drift away from the ideal (the dotted lines of V_{PD1} and V_{PD2}).

and contribute to the final FPN, which can be formalized and is given by

$$e_{\text{ddc}} = e_{\text{o}} \cdot \frac{\text{R}(N, 2)}{N} \tag{4.3}$$

where e_{ddc} and e_{o} are the FPN with and without DDC technique, $\text{R}(a, b)$ is the function of calculating the remainder of a divided by b, and N is the count. A simulated plot shown in Fig. 4.7 compares the FPN difference of PFM pixel with and without the DDC technique by referencing (4.3). A regular FPN of 5% is assumed (i.e. $V_{\text{off}}/V_{\text{diff}} = 0.05$) to comply with the current level reported by others. The count (number of resets) is from 1 to 1,000 to show the result with a 10-bit resolution and a linear configuration. As seen, the FPN remains at the same level regardless of the count without DDC; however, it reduces quickly and significantly

to less than 1% throughout the most imaging region with the DDC technique. Although the extra switching may induce additional noise, the improvement is very prominent and will benefit the overall performance of PFM pixel.

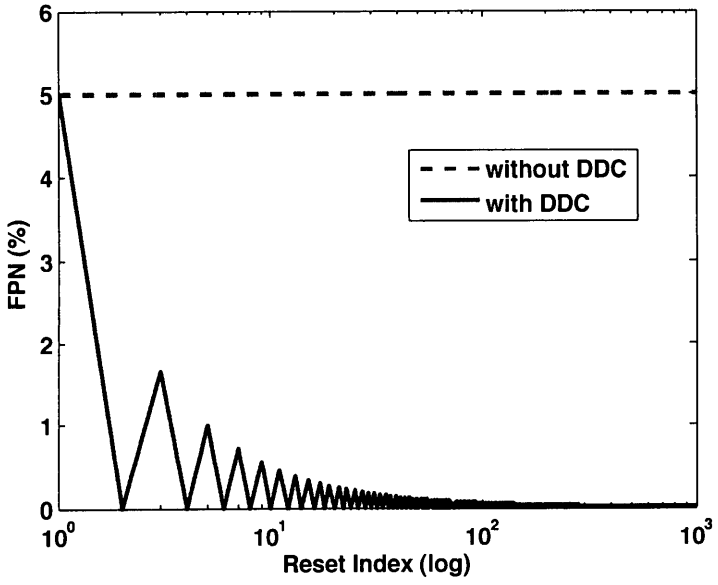


Figure 4.7: The FPN of a PFM pixel with and without the DDC technique. The FPN ideally falls to zero on even counts.

4.2.2 DR Extension

The extension of DR can be explained by the illustrations shown in Fig. 4.8. In the two figures, the voltages at the integration node (V_{PD}), the comparator output (V_{comp}), and the gate of reset transistor or the output of latch (V_{r}) are magnified to show the details of reset operation. Fig. 4.8(a) is the regular condition, and

Fig. 4.8(b) is that with the DDC technique.

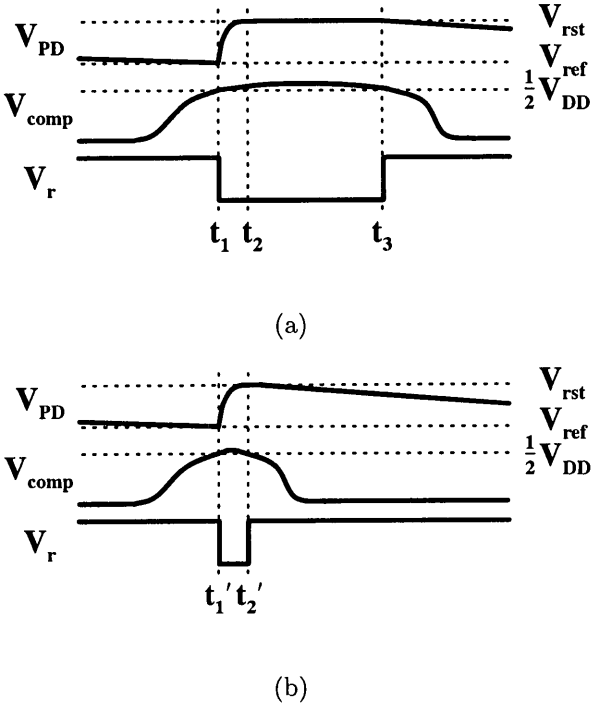


Figure 4.8: The illustrations of reset operation (a) without and (b) with the DDC technique.

In Fig. 4.8(a), when the reset starts (t_1), $V_{\rm PD}$ increases due to the reset current charging. The reset is completed in a very short period where $V_{\rm PD}$ is pulled up to $V_{\rm rst}$, which starts forcing the comparator to output a low signal (t_2). However, $V_{\rm r}$ will not be turned off until another period of time (t_3–t_2) passes to have $V_{\rm comp}$ drop below the threshold ($\frac{1}{2}V_{\rm DD}$). In Chapter 3 and [84], this period is investigated and found to be dominated by the propagation delay of the comparator, and it becomes longer when the intensity of illumination (i.e. $I_{\rm ph}$) increases. Therefore, the pulse period will be mostly determined by the propagation delay period instead of by

the actual reset charging period, especially in high-light conditions; the DR is thus reduced.

By implementing the DDC technique, DR can be increased in the high-light region since this technique potentially reduces the usually overlong reset period. In Fig. 4.8(b), the reset operation is identical to that of Fig. 4.8(a) when the reset starts (t_1') and V_{PD} is eventually reset to V_{rst} (t_2'). After the reset is done, the added DDC technique will exchange the polarities of comparator, so its reset period will be shortened by skipping the propagation delay of comparator. Note the best time for the switching to occur is the instant moment the reset is complete. The switching will make V_{comp} drop quickly without being delayed, and V_{r} is turned off right after the reset completes. Therefore, the reset period is reduced from t_3–t_1 to t_2'–t_1'. Accordingly, the reset period will be less prominent when the illumination gets strong (the integration period is short), and DR can be extended in this high-light region.

This concept of extending DR is attractive since it provides a solution of bypassing the propagation delay, which is an inevitable consequence of using a comparator. However, the real challenge is to implement a switching mechanism that executes the desired function at the right time, i.e. before the reset is getting too long and after the reset finishes. Also, this design should not cost (in terms of area and power) as much as the other designs that provide a very short propagation delay

or have a small V_{diff} but are difficult to integrate into the PFM pixel.

4.3 Circuit Implementation of the DDC Technique

According to Fig. 4.5, the proposed method to remove FPN and increase DR includes two switching mechanisms. One is the switching between the input signals (V_{PD} and V_{ref}) and the comparator input nodes; the other is the input polarities of the comparator itself. The former is accomplished rather simply by using four PMOSs to create the switches, the latter requires more effort to accomplish. This design perspective results in the block diagram of the proposed PFM pixel shown in Fig. 4.9. In this figure, a switched-polarity comparator is required to implement the DDC technique. One control signal (S) is also used, changing its state every time when a pulse signal is generated from the latch (i.e., one single reset occurs). $\overline{S}$ is the inverse of S and can be generated by simply using an inverter, so the number of control signals remains one. The signal source for S is actually difficult to generate because the image array contains many pixels operating asynchronously (if the in-pixel counter is used) and each requires its individual control signal. Fortunately, the least significant bit (LSB) of each counter not only records the pixel signal but also changes its state at the end of every integration. As a result, we directly use it for the control signal, and no external control signal is required. Its operation is further explained as follows.

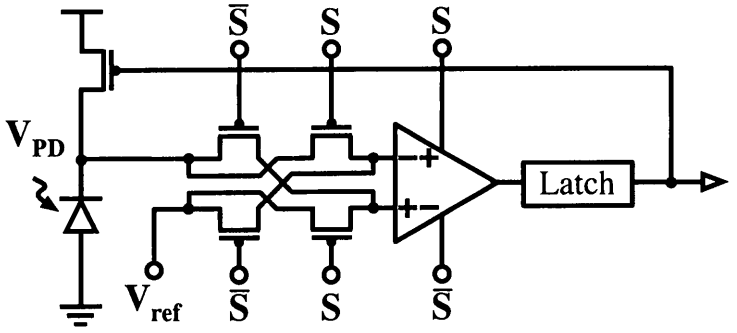


Figure 4.9: The block diagram of the proposed PFM pixel with the switching mechanisms.

Before the pixel begins its operation, the in-pixel counter is reset to 0 (and LSB (S) is 0). When S is low, $V_{\rm PD}$ is connected to the top node of comparator which is in the negative configuration and also controlled by S and $\overline{S}$, and $V_{\rm ref}$ is connected to the positive node. Since $V_{\rm PD}$ is higher than $V_{\rm ref}$, the comparator output is low (0). The charge integration then takes place as a regular PFM pixel until $V_{\rm PD}$ drops below $V_{\rm ref}$. A reset (high) signal will be generated from the comparator and starts resetting (charging) $V_{\rm PD}$ after a very short time. Meanwhile, the counter receives the reset signal as a pulse signal and its LSB changes from 0 to 1 (S is 1). As S and $\overline{S}$ change, $V_{\rm PD}$ will be connected to the bottom node of comparator which is now in the negative configuration due to S and $\overline{S}$, and $V_{\rm ref}$ is still connected to the positive node (the top node). Since $V_{\rm PD}$ has been charged back to $V_{\rm rst}$ (i.e. the negative node is higher than the positive node) when the switching is executed, the comparator output will become 0 and the next charge integration continues as

normal. Only until V_{PD} crosses V_{ref} again will the LSB change to repeatedly alter the configuration. This process will continue to realize the idea of DDC technique. Note the latch output is the inverse of the comparator.

Although the design of the switched-polarity comparator is more complex than the switching between the signals and the comparator inputs, three different circuit designs are still proposed to achieve the objective. The reference design is as shown in Fig. 4.2, and these proposed designs will be separately discussed and analyzed below.

4.3.1 Input-Switched Comparator

The first proposed switched-polarity comparator is shown in Fig. 4.10. The idea of implementing the switching mechanism is based on the input-switched concept where the primary mismatch leading to the offset is assumed to be at the input pair. The four added PMOS transistors are placed between the source nodes of the input pairs and the gates of the second stage amplifier. As illustrated in Fig. 4.9, these four transistors are controlled by S and $\overline{S}$ to perform the switching as a whole. When S is low, the left input transistor is the negative node. On the contrary, it becomes the positive node when S is high.

The advantage of this design, considering the exchanging of the input pair, is that the mismatches will be completely cancelled, so any impact of the two tran-

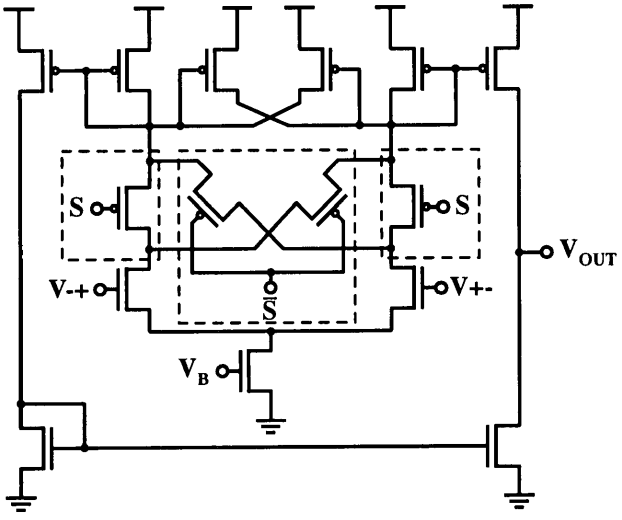


Figure 4.10: The input-switched comparator.

sistors can be lessened. However, these added transistors are located on the paths where there are currents flowing, so the comparator characteristics may change due to the transresistance (r_o) of the switches. In addition, the input voltage range will reduce by an amount of $(i_{bias}/2) \times r_o$, where i_{bias} is the bias current controlled by V_B. Besides, the switches may become a new noise source since they are directly connected to the input pair. Nevertheless, this design might still function as desired if the small-signal characteristics are carefully considered in the design stage.

4.3.2 Output-Switched Comparator

The second proposed switched-polarity comparator is shown in Fig. 4.11. Opposite to the first design, this comparator implements the switching mechanism by adding

four PMOS transistors at the output stage, assuming the offset is dominated by mismatches there. The transistors are inserted to flip the single-ended output, shown in the region marked by the dashed rectangles. The control signal is the same, using only S and $\overline{S}$. When S is low, the output signal comes from the right output stage; when S is high, the signal comes from the left side.

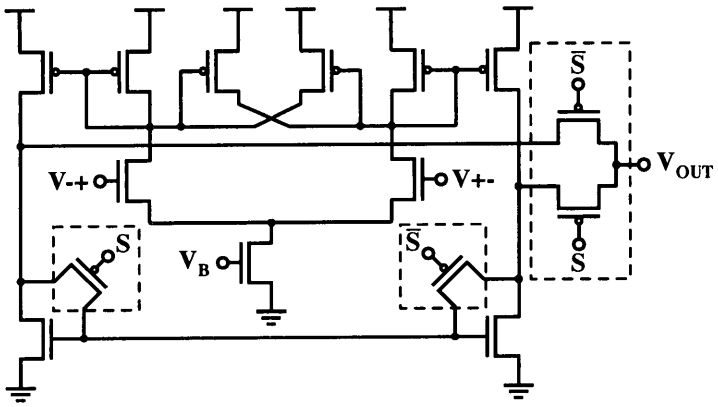


Figure 4.11: The output-switched comparator.

Since this structure leaves the first stage untouched, the input voltage range and the primary comparator characteristics are not affected. The two transistors used to flip the second-stage amplifier conduct no current, so the switching will not change the small-signal operation. The primarily drawback of this design is actually related to the two transistors controlling the output node. Because the output stage will output current, the r_o of the added transistors will change the output voltage by $i_{out} \times r_o$ where i_{out} is the output current. Consequently, it might

potentially generate another delay time which can affect the integration delay time (T_{ID}) and reset period (T_{rst}) and lead to another offset.

4.3.3 Interstage-Switched Comparator

The third proposed switched-polarity comparator is shown in Fig. 4.12. Unlike the previous designs, this method exchanges the entire connection between the first and second stages instead of only flipping the input pair or the output node. The same control signals (S and $\overline{S}$) are used as well. This structure assumes that the primary mismatch is from the first stage and inserts four PMOS transistors between the outputs of first stage and the inputs of second stage. The comparator will have a negative input at the left input transistor when S is low and a positive input at the left when S is high.

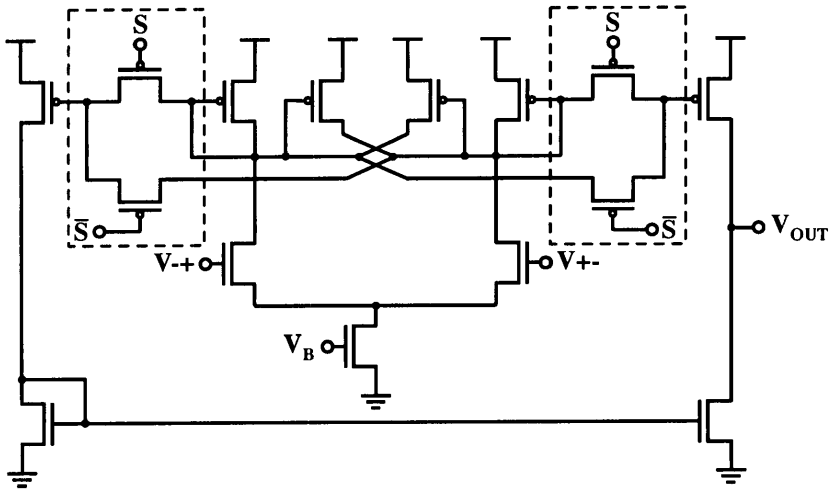


Figure 4.12: The interstage-switched comparator.

In this structure, the first and largest advantage is that the added transistors do not conduct any current but merely act as signal switches, so the comparator characteristics are expected to be almost the same as the original. In addition, there is no input- or output-voltage range reduction (as for the previous two designs), as neither the input and output stages are modified. The switching point, between the first and second stages, is able to suppress the offset from the gain (first) stage which is believed to be the primary source of mismatches.

4.3.4 General Consideration

The sizes of these added switches are not easily determined since the function of them will cause additional temporal noise and any mismatches will eventually appear in the final pixel output, or the FPN. Besides, the concern over the pixel size still exists, so a smaller transistor (in terms of gate area) is better. However, since the switches are used for signal transmission or current flow, their width should be large to reduce the effects of a large r_o and additional thermal noise. As a result, we decide to design these transistors with a gate width and length of 0.3 and 0.18 μm, respectively, to accommodate these needs.

In brief, this design approach, no matter which comparator structure is used, has the potential to remove the problematic FPN within present PFM pixels and to extend DR at the same time. Its feasibility lies on the proper function of the

switching mechanism and the modified comparator design. Moreover, the cost of implementing the DDC technique is only eight transistors, where four are for switching between the signals and the comparator inputs, and the others for the switched-polarity comparator.

4.4 Analysis and Simulation Result

The proposed DDC technique with a switched-polarity comparator was simulated in a 0.18-μm CMOS process, using the Monte Carlo method to evaluate the pixel performance with various process and temperature variations. Each of the parameter sets for the Monte Carlo simulations is executed with 100 samples, and the variation of these pulse widths (frequencies) is calculated and treated as the FPN. Since a higher output frequency is preferred under the same illumination, V_{diff} is set to 0.01 V. This small value also best displays the impact of V_{off} on the FPN. C_{PD} is 1 fF, I_{ph} is 5 fA to 20 nA, and V_{DD} (V_{rst}) is 1.2 V. The regular temperature is 40 degrees Celsius. In order to fully consider the impacts of various V_{off} when the used technology node is adjusted in terms of mismatch, we use two simplified parameter sets to include all reasonable and possible assumptions. The variations, which in general have a normal distribution, are summarized in Table 4.1. The first set (A) directly models the V_{off} at the positive or negative node of the comparator, and the second set (B) applies mismatches on the width (W) and V_{th} of every

transistor inside the pixel. The 3σ values are either assigned with a realistic value or calculated according to the library model to closely estimate the real condition.

Table 4.1: Parameter Sets and Values

Item \ Set	A	B	
Parameter	V_{off}	W	V_{th}
3σ	5, 10, and 15 mV	2.52–12.6%	2.8–19 mV

The simulation is performed by using each set individually, with the schematic shown in Fig. 4.13. The LSB outputs of the counter ($D0$ and $\overline{D0}$) are connected to S and $\overline{S}$, respectively. The simulated pulse signal is stored and analyzed to display the photo-response transfer curve and to calculate the FPN and DR. Note that the bit count of the counter is not important since the waveform (or each integration) of pulse signal determines the performance of DDC technique.

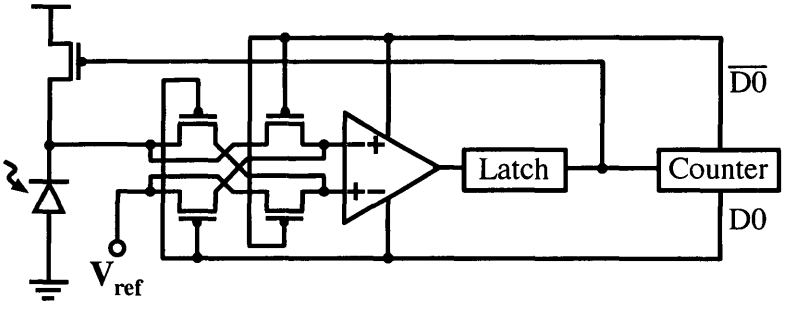


Figure 4.13: The schematic for FPN simulation with the DDC technique.

An example of the simulations is shown in Fig. 4.14, illustrating the reset voltage

(V_r) waveforms under different conditions. The example is generated using an I_{ph} of 1 nA and a V_{diff} of 0.01 V to show the impacts of having a V_{off} and using the DDC technique. There are three figures included, where the top one displays the ideal V_r waveform assuming neither V_{off} is induced from any mismatches nor the DDC is implemented; it shows the original, expected pulse width (frequency). The middle adds a V_{off} of 3 mV, resulting in a V_r waveform which has a larger pulse period than the top. Obviously, the resulting pulse drifts away from the ideal and thus the effect of comparator mismatches, i.e. the FPN, is observed. Finally, the bottom uses the same V_{off} as the middle while the DDC technique is also implemented, showing that the output pulse has two different widths. One is a longer pulse width adding the V_{off} and the other is a shorter period with the V_{off} compensated (i.e., subtracting V_{off} from V_{diff}), and the summation of any two consecutive pulse periods will equal two of the ideal periods.

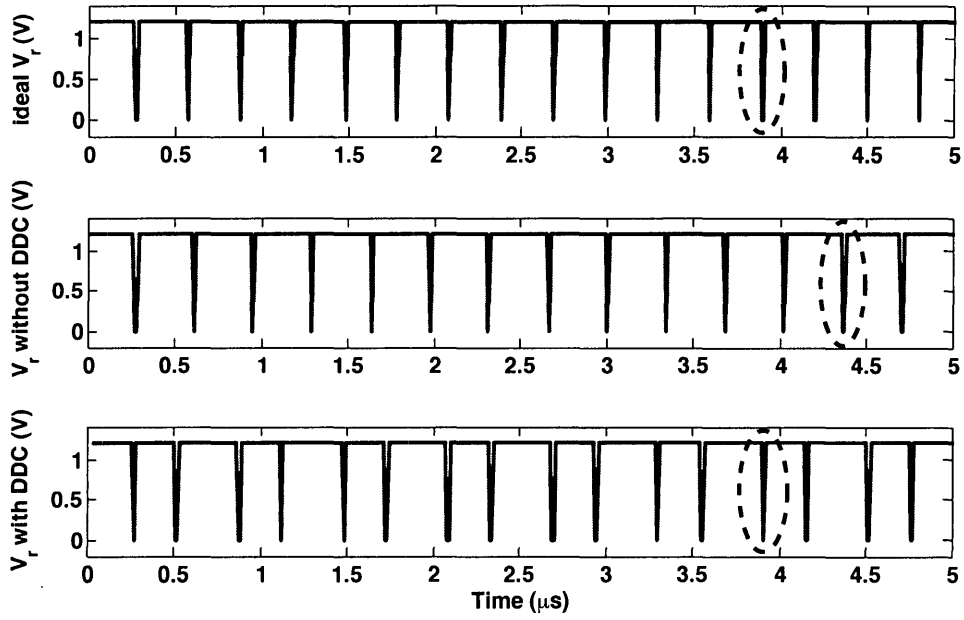
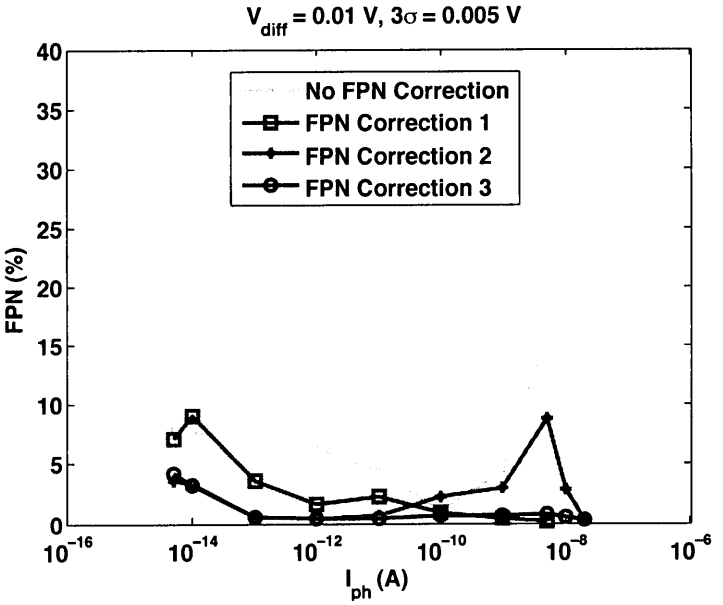


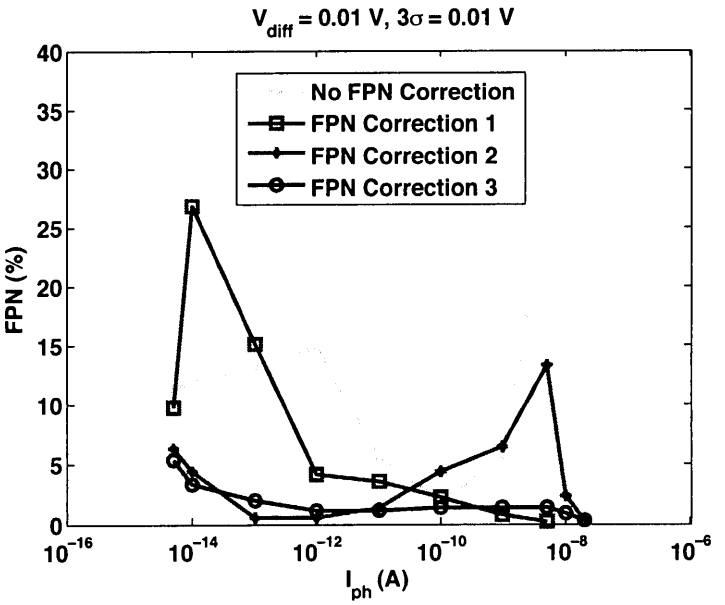
Figure 4.14: The simulated V_{r} waveforms of PFM pixel without V_{off} and the DDC (top), with V_{off} and without the DDC (middle), and with V_{off} and the DDC (bottom), respectively. The dashed ovals highlight the thirteenth reset pulses to show the function of the DDC technique in compensating the V_{off}.

4.4.1 FPN with V_{off} Variations

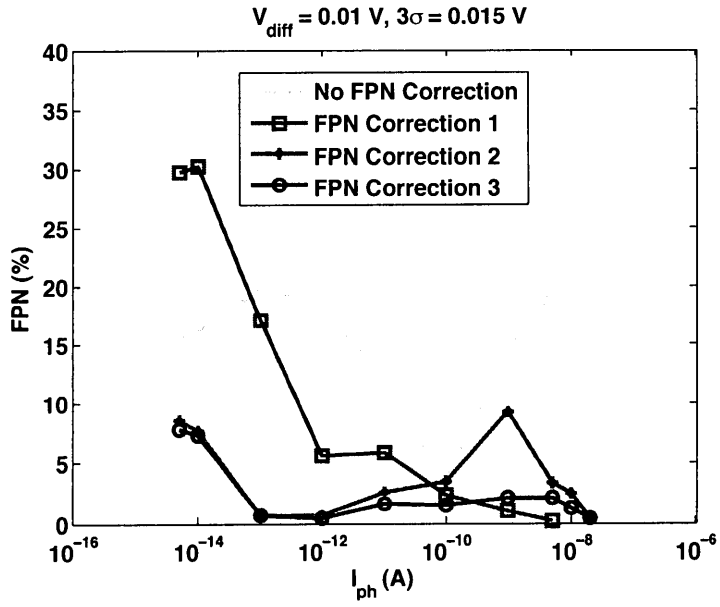
Three figures in Fig. 4.15 show the simulation results using three different V_{off} variations, including a 3σ value of 5 (□), 10 (○), and 15 mV (+), respectively. The average FPN for the baseline pixel (without FPN correction) is between 5% and 15%, depending on the value of variations, which increases with V_{off} and is unacceptably large. This amount of FPN is close to those that have been reported [19, 73, 78, 92], demonstrating that value of V_{off} is appropriate in our simulations. On the other hand, the results using the proposed DDC technique achieve the FPN reduction by different amounts, depending on the structure of switched-polarity comparator. It is noticed that the input-switched comparator design (FPN correction 1) successfully reduces the FPN in the high-light region while the output-switched comparator design (FPN correction 2) particularly reduces the FPN in the low-light region. Lastly, the interstage-switched comparator design (FPN correction 3) outperforms the previous two with a 1–3% average FPN using the proposed DDC technique, regardless of the value of variations. In particular, the FPN is reduced from an average of 15% to less than 3% when the 3σ is 15 mV, as shown in Fig. 4.15(c).


V_{diff} = 0.01 V, 3σ = 0.005 V
No FPN Correction
FPN Correction 1
FPN Correction 2
FPN Correction 3
FPN (%)
I_{ph} (A)

(a)


V_{diff} = 0.01 V, 3σ = 0.01 V
No FPN Correction
FPN Correction 1
FPN Correction 2
FPN Correction 3
FPN (%)
I_{ph} (A)

(b)



(c)

Figure 4.15: The simulated FPN with a 3σ value of (a) 5 (□), (b) 10 (○), and (c) 15 mV (+), respectively. FPN correction 1, 2, and 3 represent the DDC implemented with an input-switched, output-switched, and interstage-switched comparators, respectively.

The reasons that the interstage-switched comparator outperforms the others are explained as follows. First, any active switches of the input-switched comparator design draw currents and cause a voltage drop, therefore an offset on the signal paths is generated. According to the results, the FPN is a lot higher in the low-light region, and this is because of the offset being input stage current-dependent. As a result, when the photocurrent is small, the transmitting signal suffers more from the mismatches of switches, eventually resulting in a longer or shorter propagation delay even with the DDC technique. Second, the output-switched comparator has two switches determining the output signal connection and also conducting current when they are active. Therefore, any voltage offset of these switches will result in an advance or a delay on the generated reset pulse signal. In addition, the mismatches of switches will further affect the degree of advance or delay and cause a higher FPN. Since the cause is not input-dependent, its impact is only prominent when the integration period is short, i.e. in the high-light region. However it performs well in the low-light region, as expected. Lastly, the interstage-switched comparator avoids both the input- and output-dependent issues, so its resulting performance in terms of FPN reduction meets the target of proposed DDC technique.

According to the results, we conclude that the successful implementation of the DDC technique requires not only the correctness of switching mechanism but also a proper design of the switched-polarity comparator. Nevertheless, the V_{off}-

induced FPN can be reduced to an acceptable level by using the DDC technique to compensate the variation within every two integrations.

4.4.2 FPN with Width and V_{th} Variations

Instead of using a simplified offset voltage source at the comparator input node, the layout and process variations are considered for all transistors in the pixel so as to simulate the real condition in another way. The selected parameters, transistor width and V_{th}, are usually dominant and the first to be considered for variation assumption. According to the suggestions given by the library of the process, these variations are 2.52–12.6% for width and 2.8–9 mV for V_{th}, depending on the size of each transistor in the pixel. The FPN calculated from the simulations using these variations is shown in Fig. 4.16.

In this figure, we find the DDC technique can only reduce the FPN caused by the layout and process variations with a proper switched-polarity comparator design. According to the figure, the result using the input-switched comparator (FPN correction 1) does suppress the FPN, however the improvement is not satisfying, as discussed previously. Secondly, the result using the output-switched comparator (FPN correction 2) is worse than that without the DDC technique. We believe that the generated reset pulse is very sensitive to the mismatches of the switches which choose the output node during the switching mechanism, therefore its FPN is very

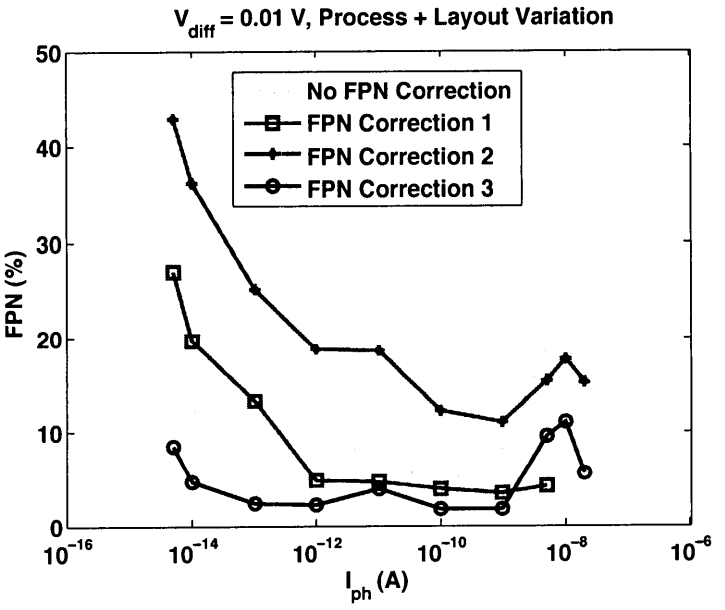


Figure 4.16: The simulated FPN with transistor width and V_{th} variations.

high. The reason that this phenomenon is not observed in the simulation using V_{off} variations is because that analysis does not include any mismatch for the added switches. Lastly, the FPN is successfully reduced with the interstage-switched comparator (FPN correction 3). Overall, the average FPNs under the proper transistor width and V_{th} variations are 3% and 10% for the PFM pixel with and without DDC technique, respectively, if the interstage-switched comparator is used.

In addition to the FPN improvement achieved by the DDC technique, the results of Fig. 4.15 and Fig. 4.16 also show that the FPN generally decreases as I_{ph} increases until around 100 pA and increases again after that point, except the one using the interstage-switched comparator. This is due to the changing dominance of T_{pul} by

T_{int} and T_{rst} discussed in Chapter 3. When the dominance of T_{int} decreases with increased illumination at the low-light region, the impact of V_{off} decreases as well (since T_{int} depends on T_{diff} and T_{off}), so the FPN is less prominent. Once T_{rst} starts to increase and become a primary component of T_{pul} at the mid- to high-light region, V_{off} will have significant impact on T_{pul}. Accordingly, FPN is again degraded by its dependency on T_{rst}.

4.4.3 Extended DR

In Fig. 4.17, the transfer curves of PFM pixel with and without the DDC technique are plotted. The data are generated by calculating the average pulse frequency with respect to the photocurrent. The results include three different comparator designs used to achieve the DDC. According to this figure, the conventional PFM pixel has an early saturation in simulation when I_{ph} exceeds 1–5 nA, which is due to the increasing reset period (T_{rst}) discussed previously, and the resulting DR is approximately 106–120 dB. This value is a little lower than the ideal value of 130–160 dB when there is no delay occurring within the signal modulation process.

On the other hand, there are several observations concerning the transfer curves with the DDC technique. First, the result using the input-switched comparator (FPN correction 1) has almost the same DR where the early saturation occurs after I_{ph} exceeds 3–5 nA, and it is believed that this design can not reduce the

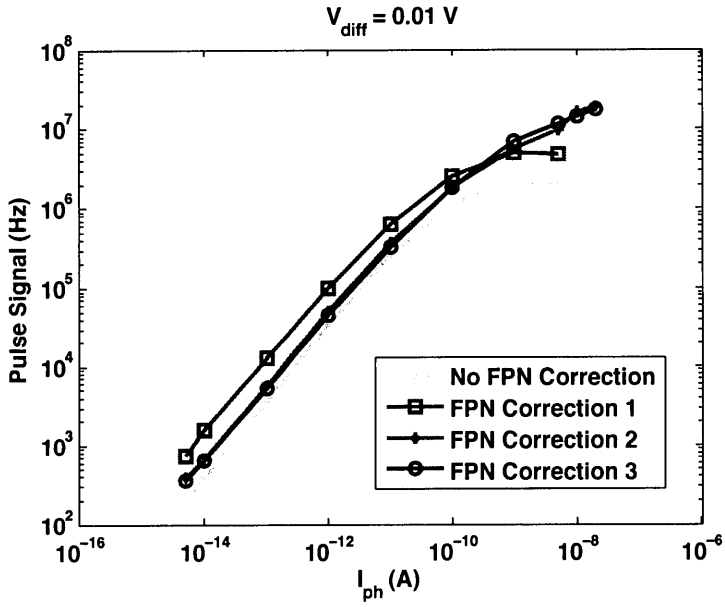


Figure 4.17: The simulated transfer curves with the DDC technique using different proposed comparator designs, compared to that without the DDC.

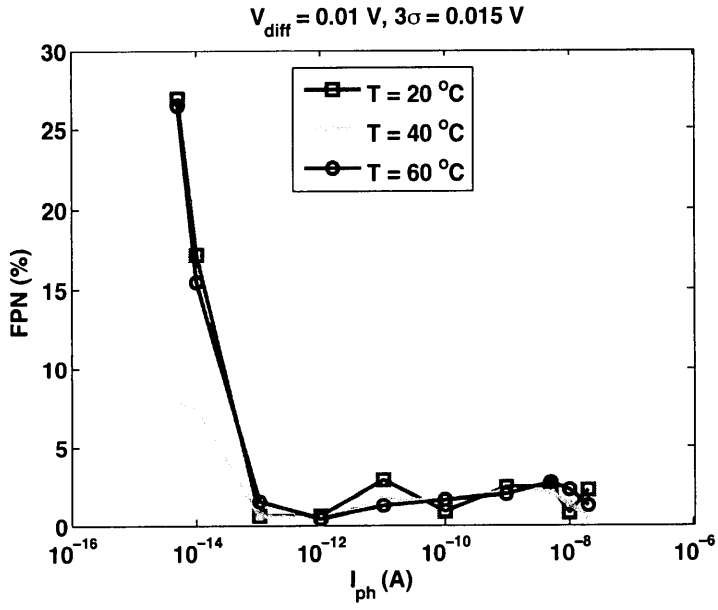
reset period since the delay due to the first stage is likely to increase. The only difference is that the pulse frequency increases by 3–4 times. However, the results using the output-switched and interstage-switched comparators extend DR in the high-light region where the saturation happens beyond 20 nA. According to the curves, the bending that leads to an early saturation is relieved, so both DR and linearity increase. From the simulation result, the achieved DR is over 132 dB, or an extension equivalent to 12–26 dB. The success of reducing the reset period can be seen from the curves where the average pulse frequencies increase a small amount in the low-light region. The highest output frequency is also boosted to 20 MHz from the original 2 MHz. In general, the results demonstrate that the DDC

technique can improve DR to nearly its theoretical amount when the switched-polarity comparator is well designed.

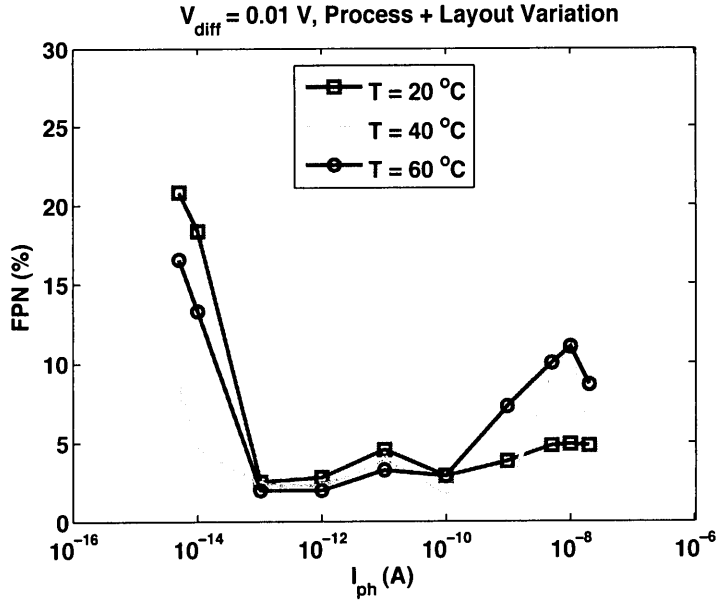
4.4.4 FPN with Temperature Variations

The previous simulation results show that the interstage-switched comparator outperforms the others in terms of meeting the targets of the DDC technique, achieving a relatively low FPN and successfully extending DR by at least 12 dB. In order to further examine the stability of this comparator, the effects of temperature are simulated. The simulated FPN results using the interstage-switched comparator with 20, 40, and 60 degrees Celsius are shown in Fig. 4.18, where the results contain the assumptions of V_{off} as well as width and V_{th} variations, respectively.

According to the two figures, the interstage-switched comparator has stable FPN performance with various temperatures from 20 to 60 degrees, regardless of using a V_{off} source or inducing the mismatch variations. The results further confirm that the DDC technique with a well-designed comparator is able to reduce the FPN of the PFM pixel. In addition, the transfer curves with different temperatures are also plotted in Fig. 4.19, where the increased DR still reaches an average of 20 dB among the results. Overall, these results support the usability of the proposed DDC technique with different temperatures.



(a)



(b)

Figure 4.18: The simulated FPN with (a) V_{off} (3σ = 0.015 V), and (b) width and V_{th} variations, using different temperatures. The comparator is the interstage-switched design.

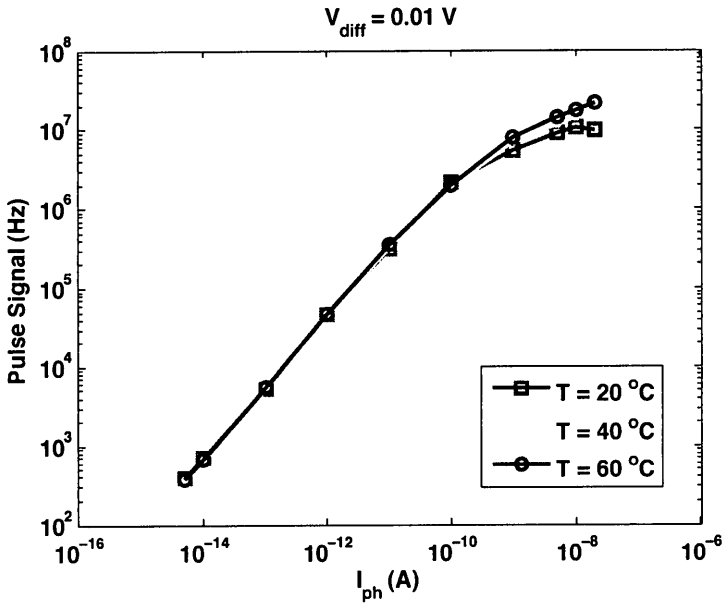


Figure 4.19: The simulated transfer curves with different temperatures.

4.5 Summary

In this chapter, a DDC technique for the PFM CMOS image sensor is proposed to reduce the FPN and to increase DR. This method only requires eight additional transistors, where four of them are used for switching input connections, and the others in a switched-polarity comparator. Although these extra transistors may potentially lead to a larger pixel pitch or smaller FF, it is still useful with those designs equipping with an in-pixel memory cell.

This technique was simulated using HSPICE and Monte Carlo method in a 0.18-μm CMOS process. Various parameters, including the offset voltage, transistor width and threshold voltage, are used to verify the feasibility of this technique.

According to the preliminary results, the DDC technique successfully reduces the FPN induced from the comparator offset voltage to 1–3%. The effect due to the layout and process variations is also reduced to less than 3%. This technique also extends DR by 12–26 dB, achieved by reducing the usually overlong reset period at high illuminations. The successful implementation of DDC technique lies on the use of a interstage-switched comparator which provides the desired functions. Simulations with temperature variation were also completed to further demonstrate the stability of this technique. These improvements are relatively important to help achieve a high-quality (low FPN and WDR) image sensor, which was previously a challenge when using PFM pixels. Overall, the DDC technique can be implemented with a minimum cost in any PFM pixel that uses a comparator.

5 Quad-Sampling WDR CMOS Image Sensor

The detailed studies, including DR, linearity, and noise, of the PFM pixel have been successfully executed in Chapter 3. The scope of the investigation includes useful information such as the theoretically available DR, factors and methods of improving the signal linearity, and noise performance of the PFM pixel. In addition, an innovative DDC technique is also proposed with sufficient simulations to show its feasibility in Chapter 4. This technique recovers the maximum achievable DR and reduces the usually large pixel FPN to an acceptable level. However, a complete CMOS image sensor structure considers not only the pixel-level performances but also the overall system design. In this chapter, a structure is presented to demonstrate a new, systematic approach that achieves WDR imaging and reduces the fabrication cost in terms of pixel size and power consumption using the PFM pixel [97]. The implementation on an FPGA board and measurement results are also provided to show the performance of this new structure.

5.1 Objective of Proposed Structure

Currently, different signal processing methods are applied to the PFM pixels, dealing with the pulse signals according to the applications. The most straightforward method among them is to implement a digital counter in each pixel to convert the frequency-domain signal into the digital domain [19, 81]. The recorded signal of each counter will be read out by the off-array circuitry and reconstructed as an image or used for post-processing. In earlier chapters, the maximum available DR of a PFM pixel has been analyzed and is believed to be of 130–160 dB [19, 84]. However, the actual DR that one single readout offers primarily depends on the bit number of the counter, which means an N-bit counter will generate a DR of $(20 \cdot \log 2^N)$ dB, assuming the noise is below one DN. Consequently, it becomes impractical to achieve a 120-dB DR using the PFM pixel since it requires a 20-bit in-pixel counter, which costs a large pixel area and degrades the sensor's modulation transfer function (MTF). Furthermore, a 22- to 27-bit counter will be required to achieve the confirmed DR of 130–160 dB. In addition to the large counter, data readout lines are also a problem for layout consideration. Specifically, either space (parallel readout) or time (serial readout) is lost to achieve signal readout. Apparently, a solution is necessary to reduce the amount of digital circuitry in the pixel, while utilizing the available or maximum DR (i.e. achieving WDR imaging) of the

PFM pixel.

In the following sections, a WDR image sensor structure using the PFM pixel with an innovative quad-sampling technique is introduced and presented with details. This technique is implemented as a cooperation between the pixel and column circuits to reduce the pixel size, specifically the bit number of the in-pixel counter. Firstly, the concept of this technique and its design strategy are described. The complete WDR image sensor structure and its operation, noise analysis, and the relationship between frame rate and array size are also analyzed. The implementation uses an FPGA board to efficiently realize this idea with flexibility to adjust original design according to needs. Finally, the measurement results are provided to show the achieved overall performance, including the transfer curves, DR, and SNR performance.

5.2 Quad-Sampling Technique for PFM Pixel

Recently, multiple-sampling techniques have been used in many designs, in particular for the WDR imaging applications [29, 34, 49–57]. Although this technique is a simple and useful approach to achieve WDR imaging, successful implementations of it were only found with the conventional APS structures. Based on those successful designs, we believe that it is possible to apply the idea of multiple-sampling to the PFM pixel with a proper arrangement. Consequently, we integrate this technique

into the PFM pixel to reduce the digital circuit and achieve a WDR imaging capability [97]. Since this work is intended to propose a complete CMOS image sensor design, a careful systematic design over not only the pixel but also the column circuit is required.

First, the concept of using multiple-sampling technique with the PFM pixel is described as follows. The primary objective is to reduce the digital circuit, essentially the counter, in the pixel, without losing the available DR that a PFM pixel can potentially reach. Therefore, assuming the in-pixel counter is reduced to only 5 bits, the DR will be $20 \cdot \log(2^5)$, or 30 dB. This result indicates that the bit number of the counter is directly related to the available DR within one regular sampling, so the goal to reduce the pixel circuit seems to be unachievable. However, an existing technique, where multiple reset potentials were used to change the sensitivities to different illuminations and increased DR to 96 dB, was successfully implemented [58]. In that work, the idea of using different sensitivities for the PFM pixel was realized by utilizing different sampling periods to accommodate different intensities of illumination. A similar method can be implemented in the PFM pixel. If the counter is divided into two parts with different sampling periods, then the total available DR after combining the signals will increase and is given by

$$20 \cdot (\log N_1 + \log N_2) \tag{5.1}$$

where N_1 and N_2 are the maximum counts in the first and second sampling periods, respectively. The summation of N_1 and N_2 can be further written as

$$N_1 + N_2 = 2^{N_P} \tag{5.2}$$

where N_P is the bit number of the in-pixel counter. The DR extension is achieved by assigning different sampling times for N_1 and N_2, and N_1 will determine the ratio of the two sampling periods with a relationship given by

$$N_1 = \frac{T_1}{T_2} \tag{5.3}$$

where T_1 and T_2 are the first and second sampling periods, respectively. According to (5.1)–(5.3), an overall DR curve with respect to different N_1/N_2 ratios is plotted in Fig. 5.1. When N_1 equals N_2, the DR can be maximized. Therefore, by using the same N_P of 5 and assuming N_1 and N_2 are equally 16, the DR is extended to 48 dB.

(5.3) is necessary to ensure that there is no sampling gap or overlap between the two sampling periods, as illustrated in Fig. 5.2. In this figure, the photo-signal transfer curves are shown with different ratios of T_1/T_2. If T_1/T_2 is larger than N_1, a sampling gap is generated (the dashed line); on the contrary, there will be an overlap between the two samplings if T_1/T_2 is less than N_1 (the dotted line). As a result, following (5.3) strictly is necessary in order to generate a continuous

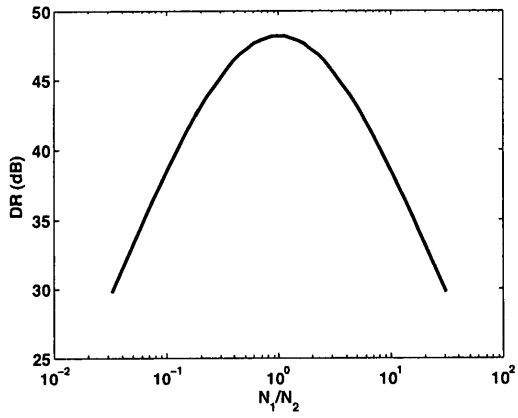


Figure 5.1: The calculated overall DR with different N_1/N_2 ratios.

sampling response between the different samplings (the solid line).

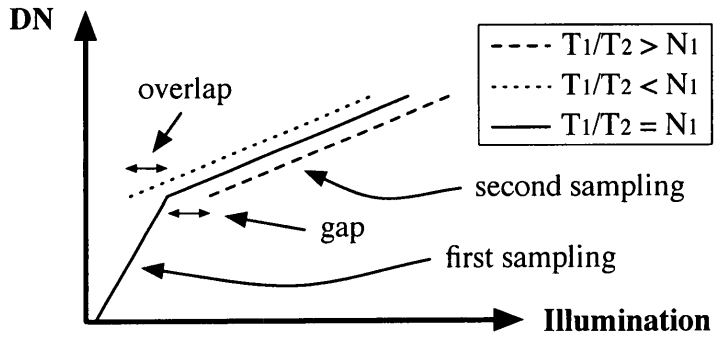


Figure 5.2: The illustration of sampling gap and overlap. A gap or an overlap may exist if (5.3) is not met.

According to this scheme, it seems to be possible to divide the 5-bit in-pixel counter into four equal parts, i.e. 8 counts each, to generate a DR of 72 dB, and this number can be even higher if more parts are used. However, doing that results in a fast-varying sensitivity during different samplings and a low signal resolution for each sampling, which are not preferred for image capture and display.

In general, the low resolution is acceptable for the high-light region imaging like other approaches [10, 47, 58], but it is not appropriate for low- or medium-light imaging since the contrast of the resulting image will be seriously distorted when seen by human eyes. This issue may be recovered by post-processing or calculations before display, but more cost (time and power) are required as well. Nevertheless, having two samplings within the pixel-level is almost the threshold when only a few bits are allocated. As a result, achieving a DR of more than 100 dB is not possible when limiting the in-pixel counter to only several bits (5 bits in this work).

In order to further increase the DR with a small PFM pixel that only uses a 5-bit counter, column-level sampling is also required. Since the in-pixel samplings include the low-light region signals, the column-level sampling can be utilized to capture the signals of medium- to high-light region where the output pulse frequencies are relatively high. This arrangement means the column-level sampling period for each individual pixel can be very short, and thus a rolling shutter operation can be realized. There are two advantages of implementing such column-level sampling. First, the column circuit does not occupy any pixel area nor decreases the FF, so there is more design flexibility. Second, the rolling shutter operation can help to increase the image sensor's frame rate. As a result, this column-level sampling will be combined with the in-pixel sampling, and the approach to implement it is explained as follows.

When the image sensor starts sampling, the in-pixel counter will record a 5-bit signal which contains 48-dB DR of information (if N_1 equals N_2, as previously mentioned). After the in-pixel sampling, the information will be passed to the column-level counter which has been reset beforehand, and the column-level sampling is executed as an extra signal in addition to the data received from each pixel. At this stage, one behavior decision has to be made to determine whether the column sampling will be executed. If the signal saturates (reaches more than 2^5 counts) during the in-pixel sampling, then the column sampling will be executed; otherwise the sampled pixel data will be kept untouched in the column-level circuit until the final readout.

Based on the above idea, a column circuit with a counter is designed, and the bit number of this counter is assumed to be N_C. When N_C is 8, the DR provided by the column circuit is $20 \cdot \log(2^8 - 2^5)$, or 47 dB. As a result, the overall DR will be 95 dB with $N_P = 5$ (N_1 and N_2 are equally 16) and $N_C = 8$. However, the maximum available DR of the PFM pixel has been investigated and is more than 130 dB [19, 84], so the overall DR should be further improved in this structure. Similar to the previous splitting method used for the in-pixel counter, the column counter is also divided into two parts and the DR can be given by

$$20 \cdot (\log N_3 + \log N_4) \tag{5.4}$$

where N_3 and N_4 are the allocated numbers of counts for the third and fourth sampling periods (first and second in the column level), respectively. Once more, the summation of N_3 and N_4 is equal to the size of column-level counter minus that of the in-pixel counter (since the pixel value will be transmitted to the column) and given by

$$N_3 + N_4 = 2^{(N_C - N_P)} \tag{5.5}$$

In order to prevent any sampling gap or overlap, the ratios of the second and third samplings as well as the third and fourth samplings must follow the two relationships which are similar to (5.3) and given by

$$N_2 = \frac{T_2}{T_3} \tag{5.6}$$

$$N_3 = \frac{T_3}{T_4} \tag{5.7}$$

where T_3 and T_4 are the third and fourth sampling periods, respectively.

Although DR is intended to be maximized, N_3 and N_4 are not chosen to be equal since we would like the medium-light scene be captured by an uniform resolution with as large a range as possible. On the contrary, N_3 and N_4 should be chosen to be close or equal if a very large DR is desired. In this work, we use an 8-bit column

counter ($N_C = 8$) which provides a conventional bit depth for display purposes. Consequently, N_3 is 192 and N_4 is 32 to increase DR by about 30 dB in the high-light region and to fit into the 8-bit counter. Ultimately, the overall DR becomes 124 dB and is enough for most applications.

5.3 Proposed WDR CMOS Image Sensor Structure

According to the proposed quad-sampling technique, a WDR CMOS image sensor based on the PFM pixel is designed, and its schematic of the pixel and column circuits are shown in Fig. 5.3. The small enclosed area inside the pixel block is the basic configuration of a PFM pixel, and the remaining part as well as the column readout are the proposed circuits that implement the quad-sampling concept. The details of each circuit block and performance analysis will be presented accordingly.

5.3.1 Pixel Design

The pixel includes a photodiode, a reset transistor, a comparator and a latch, which are the typical components of a PFM pixel. In addition, a 6-bit counter (the most significant bit (MSB) is used as a saturation flag), an XOR control, a pixel-read-control switch (M_{RP}), a second-sampling-decision switch (M_{SSD}) and row-select switches (M_{RS0}–M_{RS6}) are implemented to perform the in-pixel sampling process, whereas there are only the counter (usually 10-bit or more) and row-select

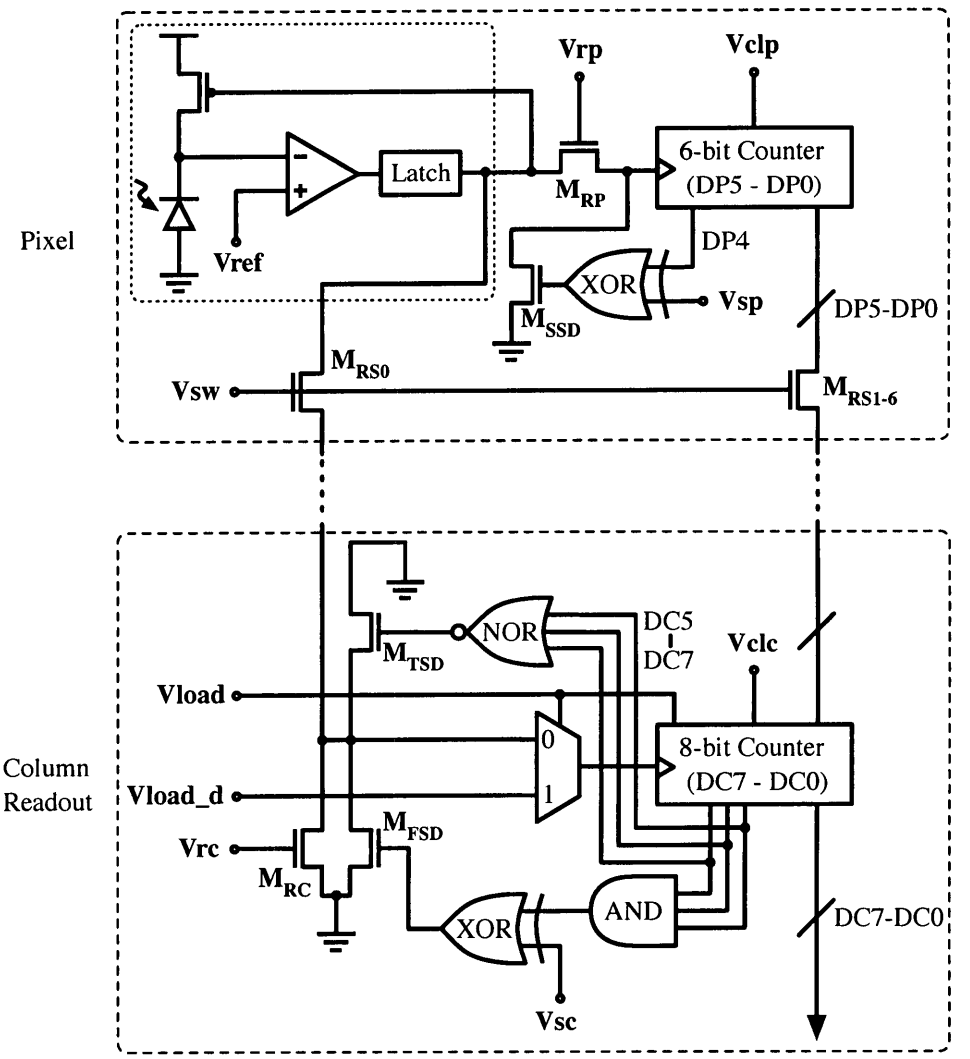


Figure 5.3: The schematic of proposed quad-sampling WDR image sensor structure, including the pixel and column readout.

switches for a regular PFM pixel. The XOR control is used to determine whether the second sampling will be executed (if N_1 saturates; DP4 = 1) or not (if N_1 does not saturate) by controlling M_{SSD}. M_{RP} is turned off to stop the sampling when the in-pixel data is being transferred to the column counter, and M_{RS0}–M_{RS6} are turned on when the column circuit begins to load the in-pixel data and execute the third and fourth samplings. This pixel design successfully reduces the total in-pixel transistor count to 110 compared to 450 transistors to achieve a DR of 120 dB with a 20-bit counter.

5.3.2 Column Readout Design

The column readout circuit has an 8-bit counter, a multiplexer, NOR and XOR controls, an AND gate, third- and fourth-sampling-decision switches (M_{TSD} and M_{FSD}) and a column-read-control switch (M_{RC}). The multiplexer will ensure that the column counter correctly loads the in-pixel data by sending a trigger signal after the pixel-level operation completes. The NOR control is used to determine whether the third sampling will be executed (if N_2 saturates) or not (if N_2 does not saturate) by controlling M_{TSD}, and the XOR control as well as the AND gate will decide whether the fourth sampling will be executed (if N_3 saturates) or not (if N_3 does not saturate) by controlling M_{FSD}. Lastly, M_{RC} is turned on after the fourth sampling completes to hold the data in all column counters for readout purpose.

5.3.3 Control Signal and Timing Diagram

In the proposed schematic, a total of eight control signals are used for the quad-sampling operation to achieve WDR imaging, and the detailed timing diagram is shown in Fig. 5.4. Four signals (V_{clp}, V_{sp}, V_{rp} and V_{sw}) are distributed in order and asynchronously to each row of the pixel array for the row operation, and the others (V_{clc}, V_{load}, V_{sc} and V_{rc}) control the column readout synchronously for the column operation. V_{load_d} is the same signal as V_{load} but with a delay time of about 10 ns or shorter to trigger the loading of column counter. Table 5.1 summarizes the proposed values for N_1–N_4 and T_1–T_4 where the row integration (or sampling) time is 17 ms and the column sampling time for each pixel is 62.82 μs. The complete operation of the WDR image sensor is described as follows.

Table 5.1: Assigned Values of N and T

Counter	N_1	N_2	N_3	N_4
Value	16	16	192	32
Sampling Time	T_1	T_2	T_3	T_4
Value	16 ms	1 ms	62.5 μs	320 ns

The sampling of one single frame starts when the in-pixel counter has been reset by V_{clp}. Once V_{clp} is turned off, the first sampling starts (t_1) with a given period of T_1. During T_1, if the number of resets (i.e., number of counts) reaches N_1, the fifth bit of the in-pixel counter (DP4) will become high and the XOR control in the

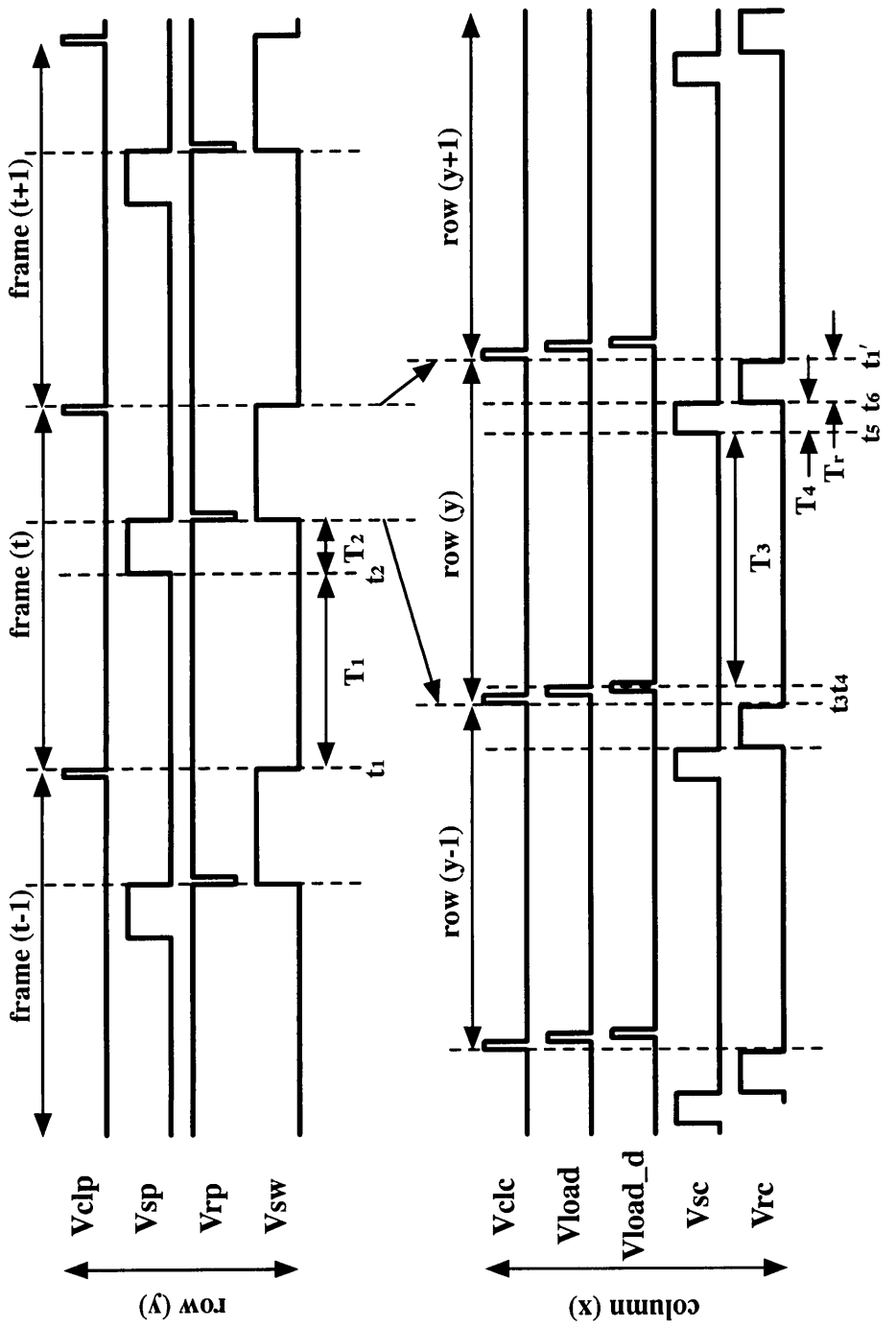


Figure 5.4: The timing diagram for proposed quad-sampling technique.

pixel will enable a constant reset by pulling the reset signal to ground. Therefore, the in-pixel counter will stop counting until T_1 completes. If the number of resets does not reach N_1 during T_1, the counting will continue until V_{sp} goes high to start the second sampling (t_2). At this stage, if the first sampling has not been disabled during T_1 (i.e., DP4 is low), the XOR control will still force a constant reset and the second sampling will not be executed. On the contrary, if N_1 saturates during T_1 (i.e., DP4 is high), the XOR control will not force a constant reset and the second sampling will start counting on top of N_1 for another period of time assigned by T_2. The second sampling as well as the in-pixel sampling finish when V_{sp} is turned off and V_{sw} is turned on (t_3). Meanwhile, V_{rp} is turned off to disconnect the pixel pulse signals from the pixel counter and to hold the captured number.

Before the column-level sampling starts, the first task is to reset the column counter and then load the in-pixel data into it. Therefore, V_{clc} is turned on to reset the counter; after the reset completes (V_{clc} is off), V_{load} is set high to switch the multiplexer from the sampling mode to the loading mode. The signal V_{load_d} is used to generate a delayed trigger signal which correctly loads the in-pixel data into the column counter. After V_{load} is turned off (t_4), the third sampling will start counting on top of ($N_1 + N_2$) for another period of time (T_3). In this period, if the second sampling has not been stopped (i.e., DC5 is still low), the NOR control will enable M_{TSD} and force a ground signal to the input of counter since both DC6 and DC7

are also low after the reset completes. Therefore, the third sampling will not be executed and the data received in the column counter will be held. Instead, the third sampling will only be executed if N_2 saturates during T_2 (i.e., DC5 becomes high) which makes the NOR control disable M_{TSD} to keep from interfering the sampling process. Once more, the third sampling may still be stopped anytime during T_3 when N_3 saturates and DC5–DC7 become high. On this condition, the AND gate will send a high signal, and the XOR control will connect the ground to the input of counter through M_{FSD}. Therefore, the column counter will stop counting until T_3 completes. If N_3 does not saturate during T_3, the counting will continue until V_{sc} goes high to start the fourth sampling (t_5). Following the same approach, the fourth sampling may not be executed if the third sampling has not been stopped (i.e., at least one of DC5–DC7 is low) and the AND gate outputs a low signal to make the XOR control force a constant reset by turning on M_{FSD}. On the contrary, if N_3 saturates during T_3 (i.e., DC5–DC7 are high), the AND gate will output a high signal which keeps the XOR control from affecting the sampling process, and the fourth sampling will start counting on top of $(N_1 + N_2 + N_3)$ for a very short period of time (T_4). The fourth sampling as well as the column-level sampling will not finish until N_4 saturates or V_{sc} is turned off. After all the sampling processes complete, V_{rc} is turned on to start the readout process (t_6) which will last for a period of time, T_{r}, until all data in the column counters have been acquired

in parallel or in serial. Once this operation is completed, V_{rc} is turned off and the column circuit will finish the previous samplings [row (y)], and the samplings for next row in line [row (y+1)] begin by turning on V_{clc} to reset the column counters (t_1').

As an alternative to the timing diagram, a flowchart is shown in Fig. 5.5 to logically illustrate the operational sequence of the proposed quad-sampling technique. The decision blocks are made of the logic gates, and the holding of data is done by the sampling-decision switches, including M_{SSD}, M_{TSD}, and M_{FSD}.

5.3.4 SNR Analysis

The SNR of proposed quad-sampling WDR image sensor structure is analyzed by considering the PFM pixel temporal noise and quantization noise. The temporal noise of a PFM pixel has been measured and reported [84], however the fact that the multiple-reset operation reduces the temporal noise similar to the condition of a time-delay integration (TDI) image sensor [90, 91] should also be taken into consideration. In addition, the quantization noise, as another primary noise source in a modulation system, is also calculated and modeled. This noise is relatively prominent especially when the pixel structure is a multiple-sampling system. Two models will be derived to provide a fundamental analysis toward the final noise in accordance with the temporal noise, and the SNR can be derived consequently.

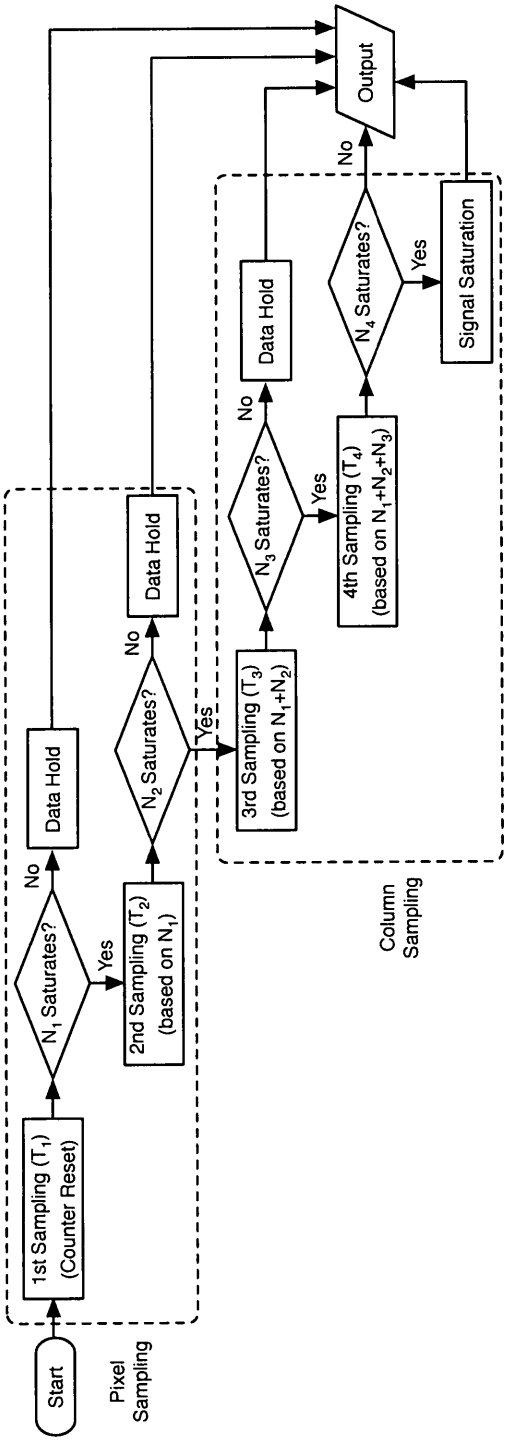


Figure 5.5: The flowchart of proposed quad-sampling technique.

5.3.4.1 Pixel Temporal Noise

According to [84], the temporal noise of PFM pixel can be simply modeled by the photon shot noise ($\overline{V_{\text{n.shot}}^2}$) and reset noise ($\overline{V_{\text{n.rst}}^2}$) which are given by

$$\overline{V_{\text{n.shot}}^2} = \frac{q(i_{\text{ph}} + i_{\text{dc}})}{C_{\text{PD}}^2} \cdot T_{\text{int}} = \frac{q \cdot V_{\text{diff}}}{C_{\text{PD}}} \tag{5.8}$$

and

$$\overline{V_{\text{n.rst}}^2} = \frac{kT}{C_{\text{PD}}} \tag{5.9}$$

where i_{ph} and i_{dc} are the photocurrent and dark current, respectively, and T_{int} is the time of each integration. In fact, there are more than these two noise sources in the pixel, but only the dominant two are considered to simplify the modeling. According to this model, the pixel temporal noise is calculated using various V_{diff}. In addition, the total temporal noise, whichever is one kind of white noise, is also subject to a $\sqrt{N}$ increment where N is the number of resets or integrations. However, the signal SNR will actually increase by $\sqrt{N}$ since the accumulated signal is N times larger than one single integration. The accumulated signal after N samplings is therefore given by

$$V_{\text{sig.accu}} = N \cdot V_{\text{diff}} \tag{5.10}$$

where the integration which does not reach one V_{diff} threshold is neglected since it will not be sampled. Therefore, the final SNR considering only the temporal noise is derived by using (5.8)–(5.10) and given by

$$\begin{aligned} SNR_{\text{TN}} &= 20 \cdot \log \frac{V_{\text{sig.accu}}}{\sqrt{N \cdot (\overline{V_{\text{n.shot}}^2} + \overline{V_{\text{n.rst}}^2})}} \\ &= 20 \cdot \log \frac{\sqrt{N} \cdot V_{\text{diff}}}{\sqrt{(\overline{V_{\text{n.shot}}^2} + \overline{V_{\text{n.rst}}^2})}} \end{aligned} \tag{5.11}$$

where a $\sqrt{N}$ improvement is seen, as expected.

In the previous study, the pixel temporal noise is also found to be higher when running at low frequencies due to the $1/f$ noise, but the difference is not large enough to affect the SNR and hence can be neglected in the analysis. According to (5.11), the SNR is primarily affected by the number of resets N and the selected V_{diff}.

5.3.4.2 Quantization Noise

Since the operation of the PFM pixel is essentially a voltage-to-frequency conversion, its sampling process will inevitably induce quantization noise. The root cause of this noise is that each pixel operates independently, however the sampling processes are synchronous either in row or column level, i.e., related row- or column-wise. An illustration of the quantization noise is shown in Fig. 5.6 to help

understand its formation.

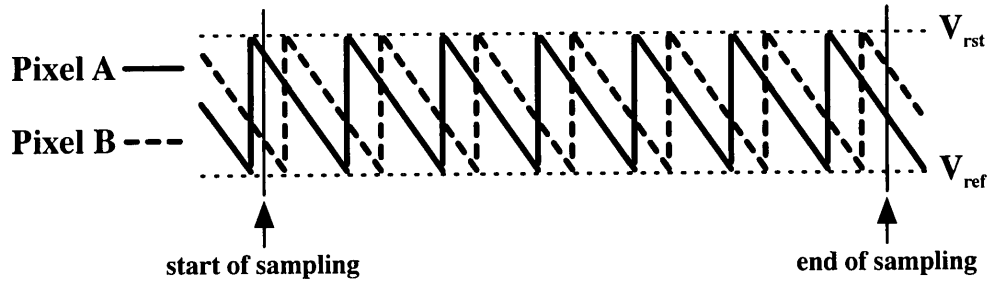


Figure 5.6: The V_{PD} waveforms of two pixels, showing the quantization noise due to synchronous sampling.

In this figure, the V_{PD} waveforms of two randomly chosen pixels of an array are displayed, and the start and end of one sampling are indicated. The photons received by the two pixels are assumed equal, thus both the pulse frequencies (or the slopes of integration) and the sampling results are expected to be the same. However, assuming the two pixels are running asynchronously, i.e., the resets happen at different times, the resulting sampled signals will possibly have one count difference if the phase difference is large enough. The example shows that the counts of two different pixels are six (Pixel A) and seven (Pixel B), respectively, without any mismatches (such as V_{off}) and temporal noise (such as the reset or shot noise), which is the effect of quantization noise.

The analysis of quantization noise begins by assuming the average value of counts is N for a set of X, or $\mathrm{E}[X] = N$. Therefore, the actual value of counts will be either the largest previous ($\lfloor N \rfloor$) or the smallest following ($\lceil N \rceil$) integer,

according to the illustration in Fig. 5.6. In addition, the probabilities that $\lfloor N \rfloor$ and $\lceil N \rceil$ happen can be simply derived as $(N-1)/N$ and $1/N$, respectively. As a result, the variance of $\mathrm{E}[X] = N$ is calculated and given by

$$\mathrm{Var}(X) = (N - \lfloor N \rfloor)^2 \times \frac{N-1}{N} + (\lceil N \rceil - N)^2 \times \frac{1}{N} \tag{5.12}$$

and the standard deviation of this set is

$$\sigma = \sqrt{\mathrm{Var}(X)}. \tag{5.13}$$

Therefore, the SNR due to the quantization noise is calculated by using (5.12)–(5.13) and given by

$$SNR_{\mathrm{QN}} = 20 \cdot \log \frac{N}{\sigma}. \tag{5.14}$$

The derivation of quantization noise results in two findings. First, the quantization noise is independent of the pixel temporal noise. Second, the SNR is determined by the average value N and increases proportionally with either N or the pulse frequency.

By using (5.8)–(5.14), both the pixel temporal noise and quantization noise can be calculated for the proposed quad-sampling WDR image sensor. According to the formulas, it is found that the quantization noise is much greater than the

pixel temporal noise, and they can be different by a factor of 10^2 to 10^3 depending on the light intensity. Obviously, this proposed quad-sampling structure has a SNR which is effectively dominated by the quantization noise. Consequently, it is not difficult to predict the SNR performance of this type of sensor in the design phase. Most important of all, the SNR dip is expected to disappear according to the formulas, and instead replaced by a continuous SNR curve. Since this quad-sampling structure accumulates the sampled signals on top of the previous value, the signal SNR is higher than the others without using the accumulation technique. In summary, the successful removal of the SNR dip is a positive and encouraging achievement among the WDR image sensors using multiple-sampling structures.

5.3.5 Array Size and Frame Rate Analysis

Although the proposed quad-sampling technique is beneficial to provide a WDR imaging with minimum cost, the practically achievable array size and frame rate are still very important in terms of determining its possible field of application. Since this technique incorporates both pixel and column operations to complete the signal readout, an analysis is required to determine the limits of operation. Considering that the proposed WDR image sensor operates in a rolling shutter mode and the timing diagram of Fig. 5.4, the maximum row size will be given by

$$y \leq \frac{T_1 + T_2}{T_3 + T_4 + T_r} + 1 \tag{5.15}$$

assuming the array has x (in column) $\times$ y (in row) pixels. The maximum column size is therefore given by

$$x \leq \frac{T_r}{T_u} \tag{5.16}$$

where T_u is the readout time for each counter data in column. As a result, the array can be 320 $\times$ 240 running at 60 fps if $T_u = 20$ ns and the values of N in Table 5.1 are used.

Since the array size is primarily restricted by the ratio of pixel sampling time ($T_1 + T_2$) and column sampling time ($T_3 + T_4$), it can actually be increased to megapixels by adjusting the assigned values of N_1–N_4 (also T_1–T_4). For instance, if $N_1 = N_2 = N_4 = 32$ and $N_3 = 160$, the maximum array size can be 1280 $\times$ 1024 and the DR is 134 dB running at 30 fps. However, the costs to boost the array size and DR are the increased in-pixel counter (7-bit instead of 6-bit) and the reduced frame rate (the wider the DR, the longer the sampling time). In addition, the transfer curve of this pixel will also change, providing more details of the dark region.

5.3.6 Auto-Compressed Sampling

The proposed quad-sampling technique for the PFM pixel is essentially an on-the-fly compression implementation that effectively achieves WDR imaging. During various sampling periods, the pulse-frequency signal that contains more than 100-dB DR is automatically compressed into an 8-bit resolution by using different sampling periods. As a result, this data can be treated as a corrected result and directly used in regular monitors or displays. Compared with other multiple-sampling WDR image sensors which require certain degree of post-processing to synthesize or correct the final images, this proposed structure saves cost and time, and its output format fits most mainstream devices. In addition, the output signal can still be either calibrated by applying other gamma-correction algorithm or linearized according to the given sampling times since each individual sampling process is linear (assuming the imaging range does not include the very high-light regions or the nonlinearity is very little).

5.4 Implementation on FPGA Board

The verification of this proposed quad-sampling technique was performed by combining a fabricated, conventional PFM pixel [19] (the region enclosed by the dotted line in Fig. 5.3) and an FPGA board (Fig. 5.7) to test the desired operations. The

pixel is the same as shown in Fig. 3.7 and its specifications are summarized in Table 3.3. The reset signal (or output) of the pixel was directly connected to an input pin of the FPGA board to provide the pixel pulse-frequency signal for the measurement. In addition, the required pixel and column control signals were supported by a data generator (Tektronix DG2020A) and a pod (Tektronix P3420), and a tungsten bulb powered by a switchable current supply (Fig. 5.8) was used for the experiment. A light integrating sphere was also utilized to provide uniform illumination. Overall, this testing arrangement provided the light intensities from 0.7 to 87,000 lux, an equivalent range of 102 dB.

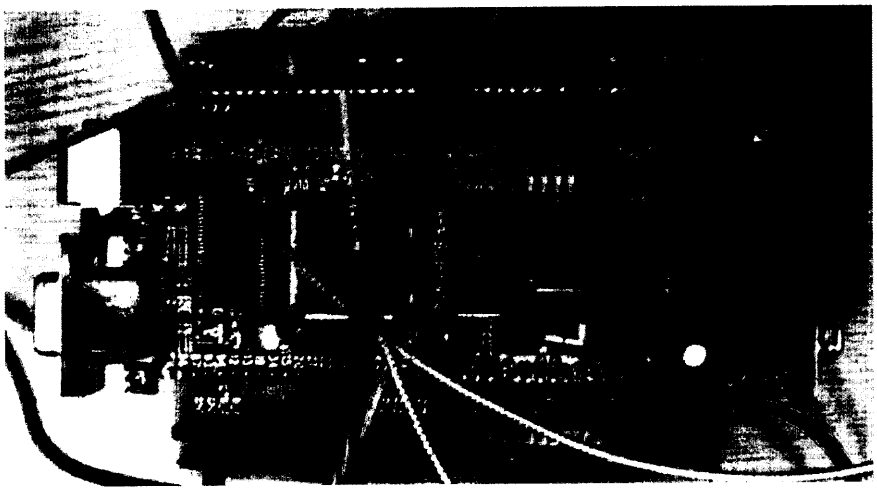


Figure 5.7: The FPGA board (XESS XSA Board v1.2) used to implement the proposed quad-sampling structure.

The remaining components of Fig. 5.3, including the multiplexer, counters, logic gates and switches, were implemented on the FPGA board using the VHDL lan-

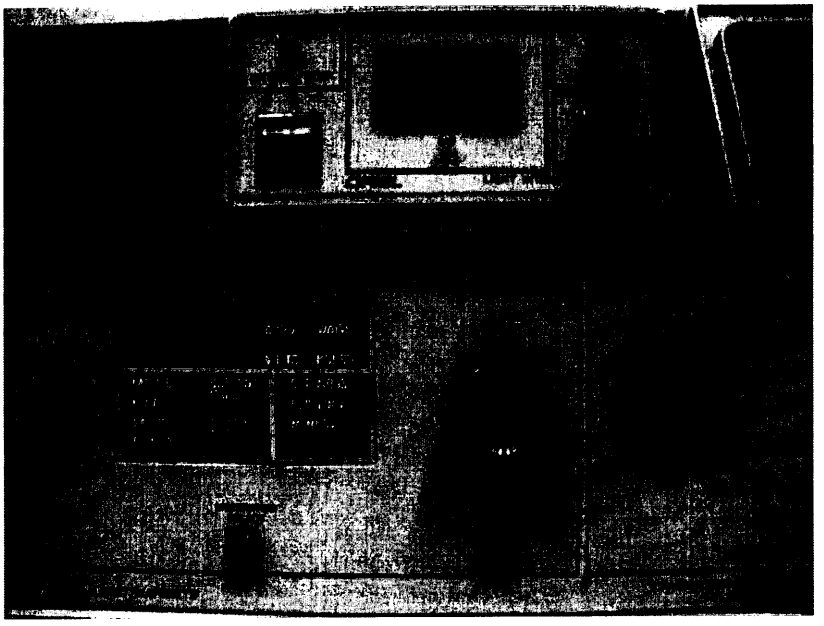


Figure 5.8: The radiometric power supply (top; Oriel 68931) and light intensity controller (bottom, Oriel 68850) for the lighting.

guage. During the measurement, the final 8-bit value (DC7–DC0) was acquired by a logic analyzer and later converted to an integer (i.e., DN) for analysis. Eventually, the output of each selected illumination level was averaged from multiple results (more than 100 samplings), and the SNR was also calculated. Appendix B shows the VHDL codes used to realize the proposed design.

The used equipments for measurements are similar to those used in Chapter 3. A lighting house which was powered by a current source provided the light source, and an integrating sphere was used to generate uniform illumination. The tested sensor was attached to a PCB board, and a pattern generator was programmed to implement the control signals. The complete diagram of the experimental setup is

shown in Fig. 5.9.

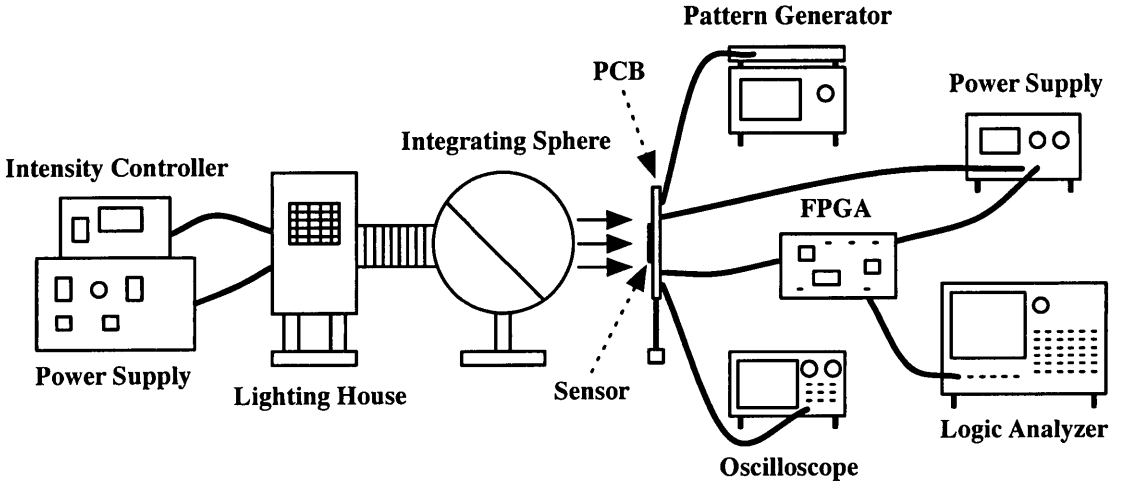


Figure 5.9: The block diagram of experimental setup, including the lighting units (power supply, intensity controller, lighting house, and integrating sphere), a pattern generator, a logic analyzer, an oscilloscope, an FPGA, and the device under test (PCB and sensor).

5.5 Experimental Results

The experimental results were measured by using different V_{diff} and frame rates in order to observe different output transfer curves and SNRs. In separate measurements, an ideal clock generator replaced the sample pixel, so that the complete DR performance of WDR image sensor could be evaluated. The simulated results of the derived formulas, including the transfer curve and SNR, will be shown with the measured results to demonstrate their correctness.

5.5.1 Measurements with Sample Pixel

5.5.1.1 Different V_{diff}

The transfer curves with different V_{diff} are shown in Fig. 5.10, where V_{diff} are 0.01, 0.05, 0.10, and 0.15 V, respectively. According to the figures, DR is maximized when a minimum V_{diff} is used (0.01 V). This larger DR is due to the extension of imaging range in the low-light region. If a larger V_{diff} is selected, the pulse frequency will become smaller (because each integration is longer) and the counter will hardly count anything with the same sampling time. Among all figures, the transfer curves from the first two samplings and part of the third sampling are measured, demonstrating the functionality of the proposed quad-sampling WDR image sensor structure. Although the instruments were unable to provide higher illumination intensities for the experiment, the maximum DR from the results is still 98 dB when $V_{\text{diff}} = 0.01$ V. In addition, the simulated results are plotted with the dashed lines, showing a reasonably linear relationship between the illumination and output pulse frequency in each sampling period. It is observed that the linearity decreases entering the high-light regions, consistent with the analysis in Chapter 3.

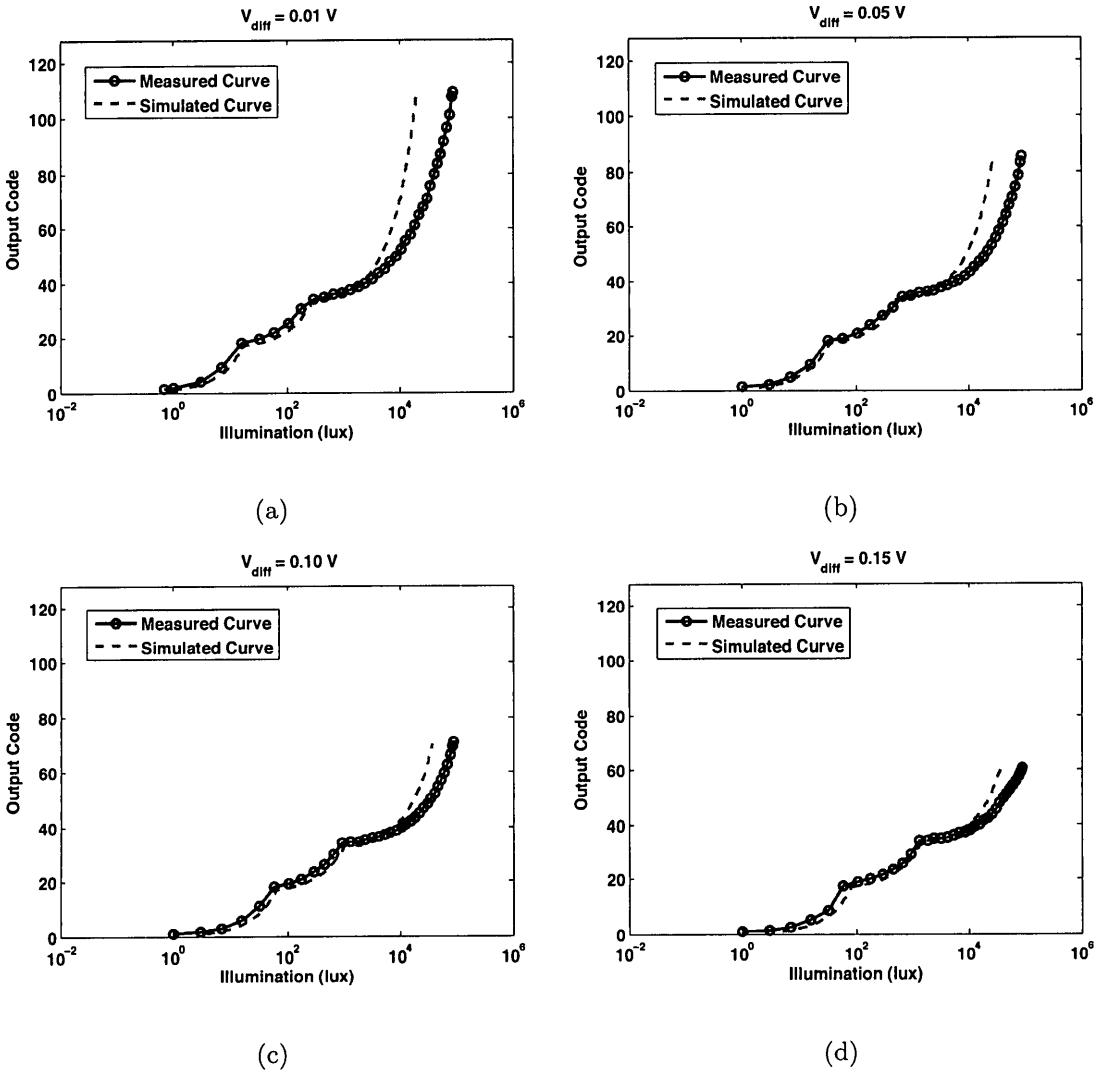


Figure 5.10: The measured transfer curves with V_{diff} of (a) 0.01, (b) 0.05, (c) 0.10, and (d) 0.15 V, respectively. Using a 0.01-V V_{diff} can achieve a highest DR. The signal nonlinearity can be observed by comparing with the simulated curves (dashed lines).

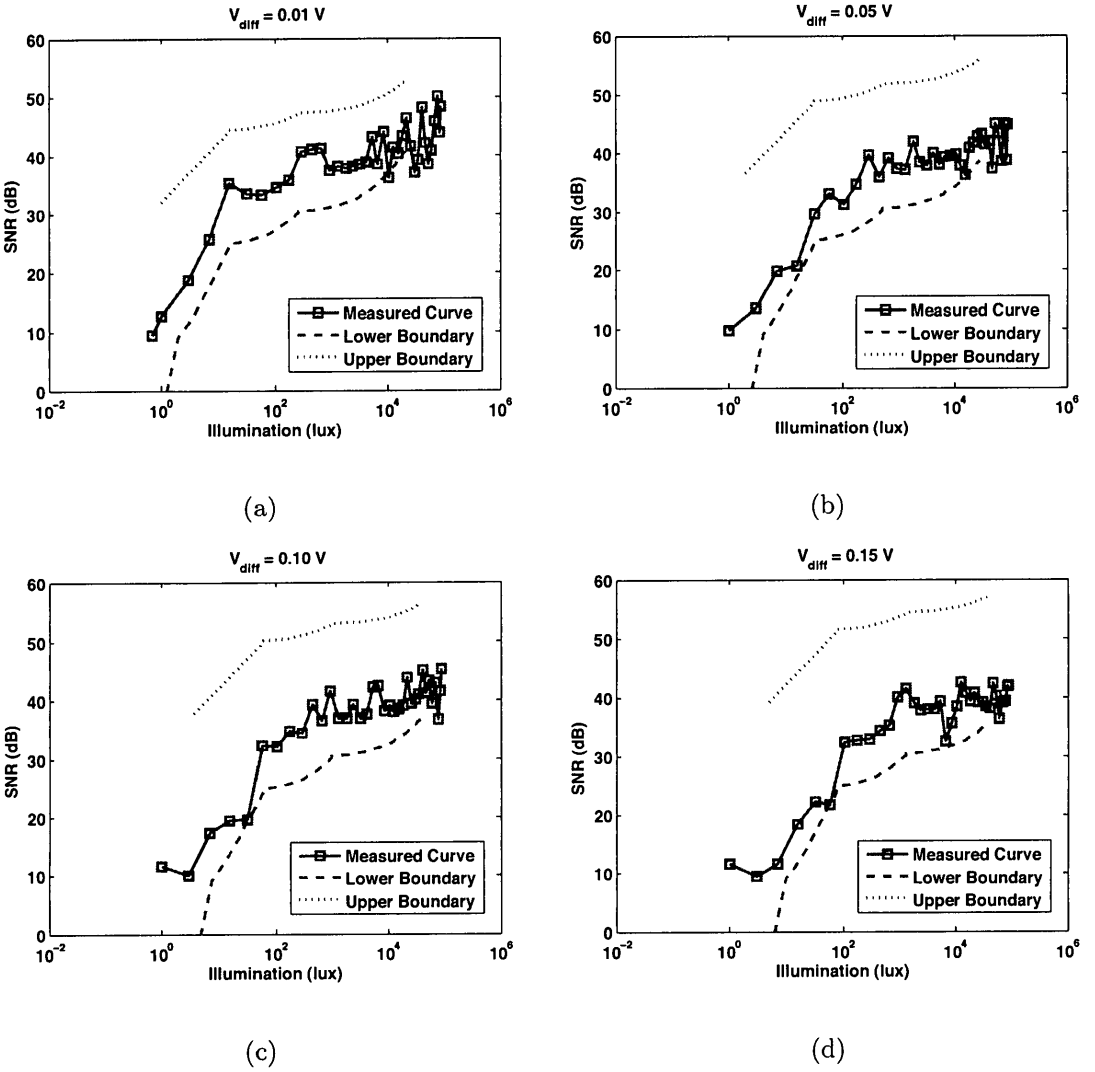


Figure 5.11: The measured SNRs with V_{diff} of (a) 0.01, (b) 0.05, (c) 0.10, and (d) 0.15 V, respectively. The predicted lower boundary (quantization noise) and upper boundary (pixel temporal noise) are drawn in the dashed and dotted lines, respectively.

Instead of the transfer curve, the SNR of each measurement result in Fig. 5.10 is also plotted in Fig. 5.11. According to these figures, we find the SNR does not suffer from SNR dip at every switching point which is a common drawback of multiple-sampling WDR image sensors [34, 50, 51, 53]. In addition to the measured result, the simulated lower boundary (due to the quantization noise) and upper boundary (due to the pixel temporal noise) of the SNR are also displayed in these figures, and two observations are noted from the results. First, the quantization noise primarily determines the SNR; second, the pixel temporal noise does not (or barely) affect the SNR since it follows the $\sqrt{N}$ rule. We also noticed that the measured SNR curves do not touch the upper boundary defined by the pixel temporal noise with different V_{diff}, and this can be explained as follows.

In general, the final SNR is determined by the total of temporal noise and quantization noise. However, it is easier to understand their individual impact on the final SNR by separating these two noises and displaying each on the same graph. Based on the operational principle of PFM pixel, the quantization noise is randomly generated as illustrated in Fig. 5.6. Therefore, the measured SNR curves will gradually increase with the lower boundary, which has been observed from these figures. Occasionally, these curves do reach the lower boundary at some points, which represents the state with a maximum sampled quantization noise. When the sampled quantization noise is not the maximum, the SNR will

increase by either a small value or a large amount since the quantization noise can vary between half DN and zero. In general, the quantization noise is determined by the actual sampled pulse frequency and assigned sample time. If the average count comes with a fraction, chances are that a higher quantization noise will be generated. Therefore, it results in the oscillations of the measured SNR curves. Nevertheless, the fact that the measured SNR does not fall below the modeled curve supports the previous analysis and argument.

In addition, by increasing V_{diff}, the SNR is typically expected to increase. However, the upper boundary becomes higher while the measured SNR curves remain at roughly the same amplitude, regardless of the higher V_{diff}. As a result, the upper boundary is not necessarily the actual SNR limit, but only shows the achievable SNR if no quantization noise exists. This phenomenon also supports the feasibility of using a very small V_{diff}, since the upper boundary is at least 15 dB higher than the lower boundary with a 0.01-V V_{diff}. According to these observations, we can conclude that only the quantization noise affects the final SNR.

Overall, the proposed WDR image sensor structure that uses the PFM pixel with quad-sampling technique has a predefined SNR which can be easily characterized in the design phase. In addition, since the pixel temporal noise is not important to the SNR (only the quantization noise matters), a small V_{diff} can actually be used in favor of generating higher output frequencies to support a higher frame rate.

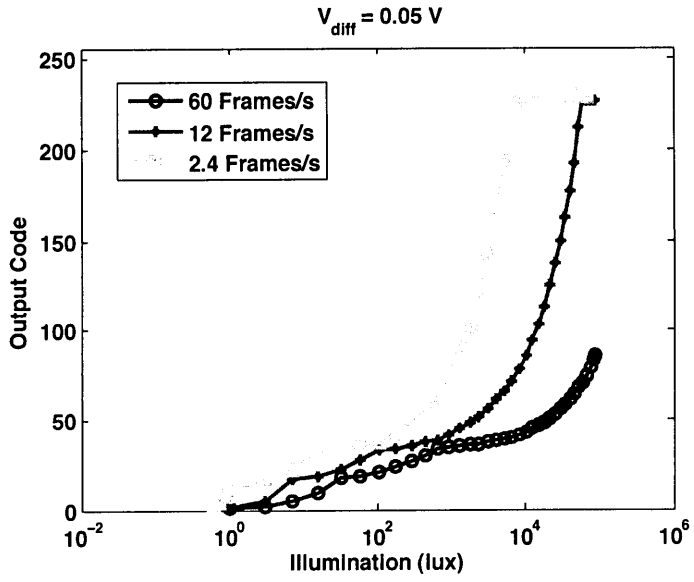
5.5.1.2 Different Frame Rate

The assigned values of T_1–T_4 were altered by multiplying 5 and 25, respectively, in order to investigate the performance changes with different frame rates. The modified values are summarized in Table 5.2, and V_{diff} is chosen to be 0.05 V. By using these parameters, the transfer curves and SNRs are measured and shown in Fig. 5.12. Note that although only one pixel was used, the pixel rate still equals the frame rate based on the designed structure and timing diagram within the array size given by (5.15) and (5.16).

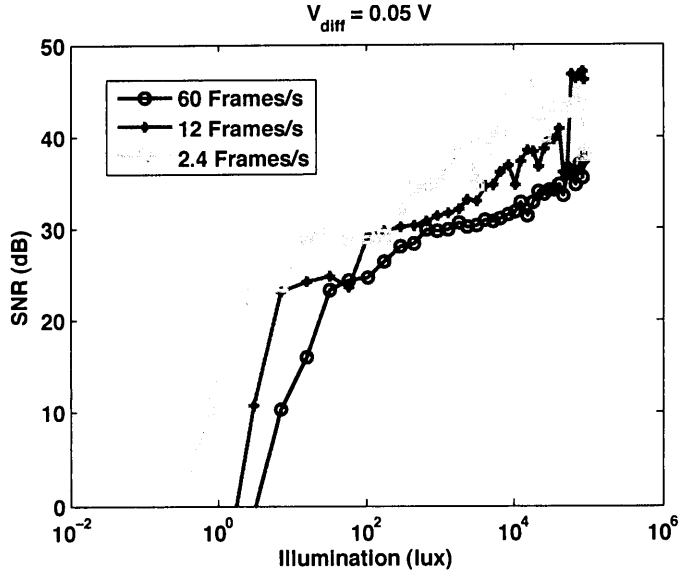
Table 5.2: Modified Values of T

Sampling Time	T_1	T_2	T_3	T_4
Set 1 (12 fps)	80 ms	5 ms	312.5 μs	1.6 μs
Set 2 (2.4 fps)	400 ms	25 ms	1.5625 ms	8 μs

According to Fig. 5.12(a), the fourth sampling (second sampling of the column level) is executed when the frame rate is set lower (12 or 2.4 fps) to have N_1–N_3 saturate within T_1–T_3, respectively. It is also found that the transfer curve with a frame rate of 2.4 fps reaches its minimum imaging region at about 0.8 lux illumination. This phenomenon is due to that the total of photocurrent and dark current ($I_{\text{ph}} + I_{\text{dark}}$) being less than the leakage current (I_{leak}) and the base frequency, $(I_{\text{ph}} + I_{\text{dark}} - I_{\text{leak}})/(C_{\text{PD}} \cdot V_{\text{diff}})$, no longer exists. In this figure, DR



(a)



(b)

Figure 5.12: The measured (a) transfer curves, and (b) SNRs with frame rates of 60, 12, and 2.4 fps, respectively. V_{diff} is 0.05 V.

with lower frame rate increases due to the extended imaging range in the low-light region (the high-light region is not tested due to the limited light source). The SNRs of the three curves are also shown in Fig. 5.12(b), showing that the SNR is only relevant to the number of counts (resets). On reaching the threshold of the third sampling (DN = 224), the SNR is about 45 dB, demonstrating a reasonably good image performance. Nevertheless, the benefits of having a lower frame rate are obviously a wider DR and a better SNR.

5.5.2 Signal Linearity

The signal linearity of this proposed structure is evaluated using the transfer curve shown in Fig. 5.10(a), which uses a 0.01-V V_{diff}. Since every sampling accumulates on the value of previous sampling in this approach, each of them has to subtract their preceding sampling value set by N_1–N_3 to generate the original transfer curve, except the first one. Therefore, the second sampling will subtract N_1 (16), and so on so forth. The calculated results are displayed in logarithmic scale, as shown in Fig. 5.13. Although part of the third sampling and the fourth are not shown due to the limited illumination intensity, the result still demonstrates the signal linearity within the tested range. In addition, the first-order line fits of all samplings are also displayed (the dashed line).

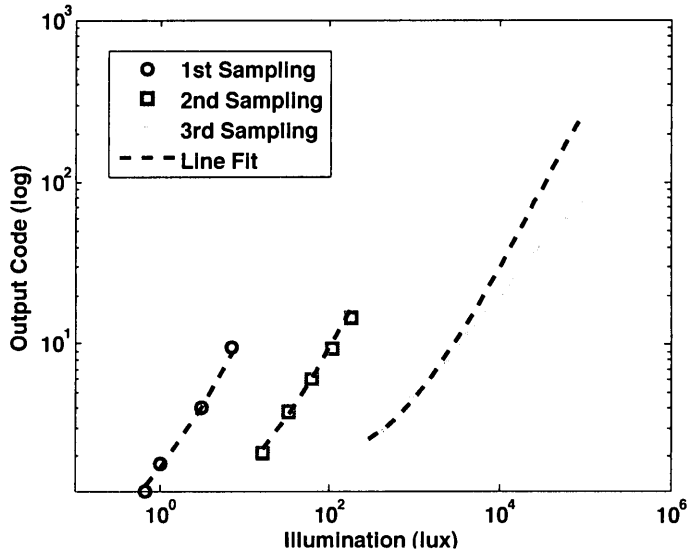


Figure 5.13: The recalculated transfer curves of three individual sampling periods. The dashed lines are the first-order line fits of each sampling.

It is clearly seen from the calculated results that the first and second samplings have quite high linearity within its own range. When the illumination increases, the third sampling starts to show a certain degree of non-linearity. In general, linearity decreases as the illumination increases due to the impact of T_{ID} and T_{rst}. This is consistent with the analysis in Chapter 3. The slope of each sampling in Fig. 5.10(a) and the correlation coefficients (r) of Fig. 5.13 are summarized in Table 5.3. The ratios of slopes between any two consecutive samplings are also included, which are expected to be the same or very close as defined in (5.3) and (5.6), i.e. 16 in the proposed design. This phenomena also concludes that the output signal can be easily calibrated based on N_1–N_3.

Table 5.3: Signal Linearity of Individual Sampling

Sampling Order	Slope (DN/lux)	Ratio w.r.t. Prior Sampling	r
1st	1.6835	N/A	0.9983
2nd	0.1042	16.156	0.9973
3rd	0.0057	18.281	0.9846

5.5.3 Measurement with Clock Generator

Since the lighting bulb could not provide sufficient illumination range (in particular the high-light region) to perform a complete measurement over the proposed quad-sampling WDR image sensor, a clock signal was used to replace the sample pixel. This ideal clock signal can provide any frequencies ranging between 10 Hz to 100 MHz, where we use a range from 15 Hz to 25 MHz, corresponding to a DR of 124 dB if the relationship between the illumination and pulse frequency is completely linear. The experimental results of the proposed WDR image sensor using the quad-sampling technique and that without this technique are plotted in Fig. 5.14.

In this figure, the complete four samplings of the proposed WDR image sensor are measured as expected, with a total DR of 124 dB. This number meets the target of design and the transfer curve is very close to the simulated curve. The DR extension is 76 dB in comparison with the conventional PFM pixel when an 8-bit resolution is used. In addition, it is also found that the DR extension benefits from moving the lowermost and uppermost 32 counts to the low- and high-light regions,

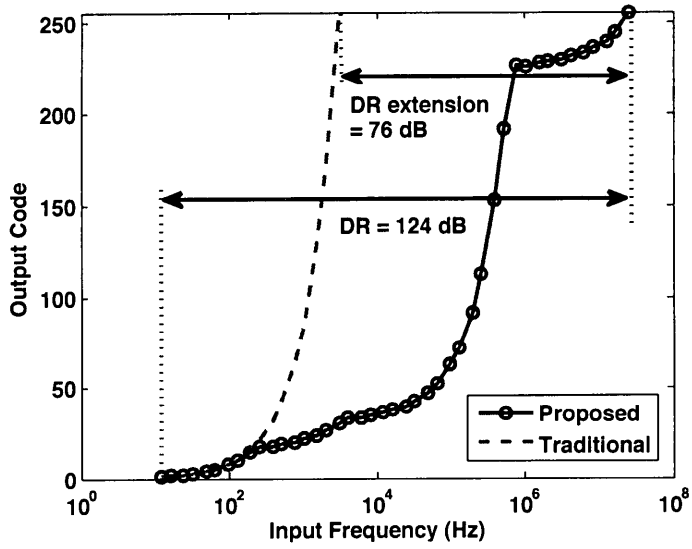


Figure 5.14: The measured transfer curve using a controlled clock generator. The dashed line represents the conventional PFM pixel transfer curve with a DR of only 48 dB.

respectively. Note that the transfer curve in the figure can be moved horizontally by having different sampling times, i.e. different frame rates. Specifically, this curve moves rightward on the x-axis when the sampling times decrease or the frame rate increases, and vice versa.

5.5.4 Sensor Performance

The completed experiments and theoretical analysis have demonstrated the feasibility of the proposed quad-sampling technique in achieving a WDR imaging with minimum pixel cost. The design parameters, operating environment, and achieved sensor characteristics are summarized in Table 5.4. It is notable that sensitivity

is expected to increase if a proper image sensor fabrication process is used (with anti-reflection coating, canyon above active region, and micro-lens), and the frame rate can increase at the same time.

Table 5.4: Sensor Specifications

Supply Voltage	1.2 V (core) / 2.5 V (I/O) 9 V (FPGA)
In-pixel Counter	6 bits
Data Width	8 bits
Sensitivity	85 Hz/lux
Sampling Method	Quad-Sampling (two samplings in pixel, two samplings in column)
Array Size	320 × 240 (proposed) 1280 × 1024 (achievable)
DR	98 dB (with Sample Pixel) 124 dB (with Clock Signal)
Maximum SNR	>45 dB (with Sample Pixel) 48 dB (with Clock Signal) Both without SNR Dip
Frame Rate	60 fps (30 fps with larger array)

5.6 Summary

A quad-sampling technique for WDR CMOS image sensor using the PFM pixel is designed and presented in this chapter, achieving a DR of 124 dB and operating at 60 fps in rolling shutter mode. The pixel array is 320 × 240, and can be up to 1280 ×

1024 with a modified design. The idea of implementing the WDR imaging is realized in the pixel and column circuit designs, and this concept is verified by the FPGA implementation. A sample PFM pixel fabricated in a 0.18-μm CMOS process is used to help confirm the feasibility of the proposed technique. The quad-sampling technique is meant to work with the PFM pixel and successfully reduces the in-pixel counter to only 6 bits. Column-sampling is facilitated to complete the WDR imaging. This structure is adjustable for different DR and array size requirements with just a few modifications. On-the-fly signal compression is executed during the samplings, so no additional post-processing is required for display purposes. As well as directly usable output, the high linearity of the PFM pixel also provides an easy image correction capability. The SNR is a predefined value, simply affected by the quantization noise but not the pixel temporal noise. From the experimental results, the SNR exceeds more than 45 dB and satisfies most requirements.

6 Performance Study of Quad-Sampling WDR CMOS Image Sensor with DDC Technique

In the previous chapters, sufficient fundamentals have been analyzed and presented, including the complete study of DR, linearity, noise of PFM pixels, techniques to reduce FPN and to extend DR, and a quad-sampling approach for the practical realization of a WDR image sensor. These studies complete important investigations required for the continued development of the PFM pixel. In this chapter, a complete WDR image sensor design based on the PFM pixel will be proposed. This implementation is presented at a schematic level, and the anticipated performance is also simulated. In addition, the flexibility of the design will be demonstrated by altering the design slightly and discussing the performance change. This early analysis will provide a reference before the real implementation of the WDR image sensor in silicon technology.

6.1 Preliminary Image Sensor Design

A complete block diagram of the WDR image sensor, which incorporates the DDC and quad-sampling techniques, is designed and shown in Fig. 6.1. This figure consists of a system-level diagram that illustrates the overall image sensor design using the proposed PFM pixel. In this sensor system, the row decoder controls all pixels to perform the rolling shutter operation through the row lines, and the column control is responsible for the execution of column sampling. The column decoder is used to read out the data stored in the column counter serially through V_{ro}. The supply lines are allocated generously to distribute V_{DD}, V_{SS}, V_{ref} and V_{B} to every pixel. A thick-oxide reset transistor will be chosen for the reset switch to maximize DR, and the photodiode area will also be designed according to its size. The DDC technique with a interstage-switched comparator is adopted to improve the actual DR and to reduce FPN. As previously mentioned, the pixel pitch is expected to be much smaller due to the saved area of digital circuitry inside the pixel. The in-pixel transistor count is 110 and the pixel pitch can be 10–15 μm depending on the selected technology.

The timing diagram of this image sensor is the same as shown in Fig. 5.4, and the array size of this preliminary work is set to 320 $\times$ 240, or 76.8k pixels, using the integration times summarized in Table 5.1. In addition, the sensor runs at 60 fps and

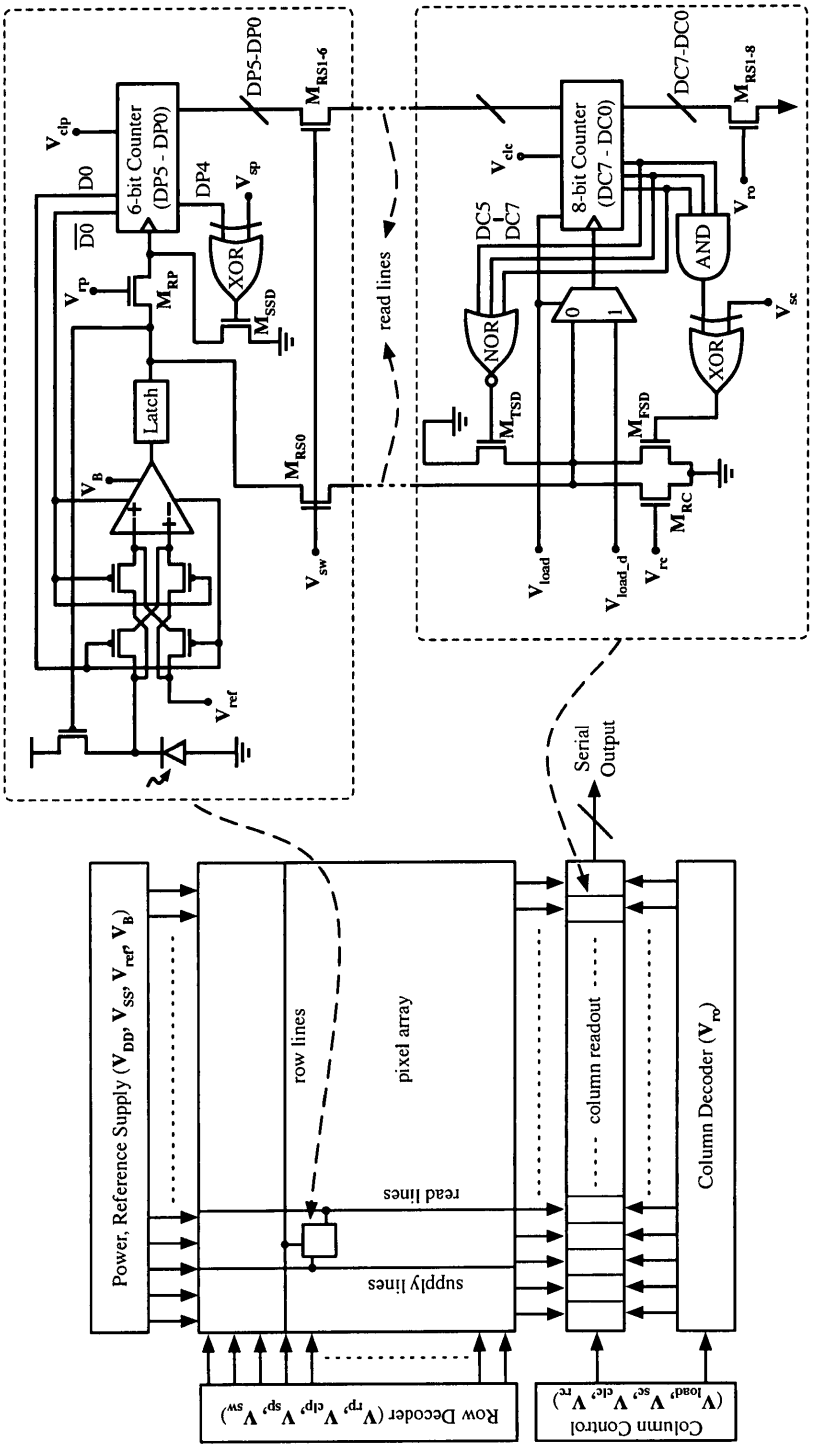


Figure 6.1: The block diagram of proposed WDR image sensor.

covers a DR of 124 dB. The expected pixel FPN is around 2%, whereas the column and row FPN are theoretically very small and barely noticeable. A maximum 48-dB SNR is also expected from the sensor without the SNR dip. The comparison of expected performance of this proposed WDR image sensor and a traditional PFM image sensor using the same pixel pitch are summarized in Table 6.1.

Table 6.1: Comparison of Proposed and Conventional WDR Image Sensors

Type	Proposed	Conventional
Technology	0.13–0.35-μm CMOS	
Pixel Pitch[1]	10–15 μm	
Array Size[1]	320 × 240	
Supply Voltage	0.8–1.5 V (core) 1.8–3.3 V (I/O)	
Photodetector	p-n junction	
FF[1]	20–35%	15–25%
In-pixel Counter	6 bits	8 bits
Column Counter/Memory	8 bits	
Data Resolution	8 bits	
A/D Converter	N/A	
Sensitivity[2]	80–400 Hz/lux	
Nonlinearity[3]	<0.8%	<0.1%
DR[2]	124 dB	48 dB
Maximum SNR[2]	48 dB	
pixel FPN[3]	1–3%	5–10%
column / row FPN[3]	~0%	
Frame Rate[2]	60 fps	

[1] From calculations.
[2] From measurements.
[3] From simulations.

Although the used technology in the previous chapters is 0.18-μm CMOS process, the comparison in this table considers processes between 0.13 and 0.35 μm, which are common for CMOS image sensor fabrication as of today. The pixel pitch is calculated with a fixed photodiode area and other circuits built with the specified feature size. Based on the assumption, the proposed structure has a higher FF (20–35%) than the conventional design (15–25%) due to the reduced in-pixel counter, and the output data has the same data width. A/D converter is not used since each pixel outputs a digitized signal.

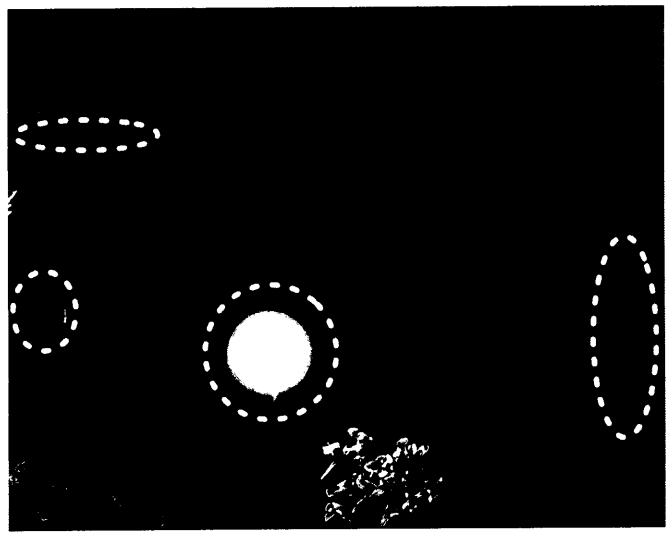
6.2 Simulated Image Quality

The performance demonstration of the WDR image sensor design before realizing it in silicon technology is performed by image synthesis according to the sensor transfer curve. In the beginning, three images with long, medium, and short integration times of a WDR scene, including a light bulb and several surrounding dark regions, are put together with a total of 24-bit resolution to cover a DR of 144 dB. Using a MATLAB simulation, this image is then processed in two ways, as if it was captured by the proposed and conventional image sensors using the PFM pixel. The considered parameters include the transfer curve, DR, SNR, and FPN. Note that the numbers used for the synthesis are those summarized in Table 6.1.

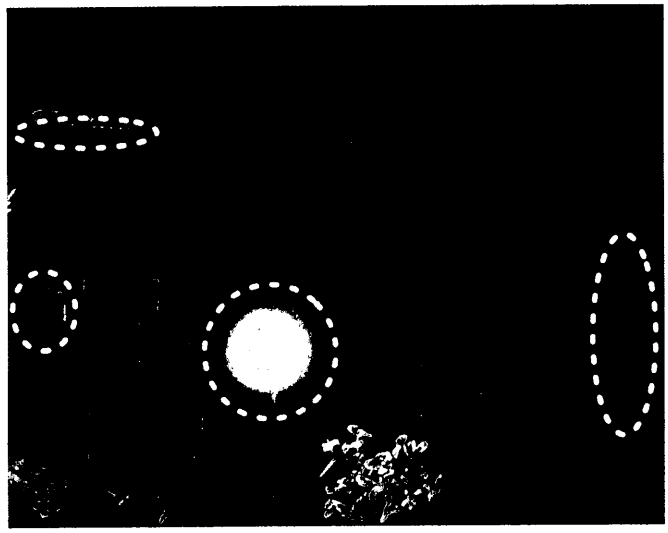
The synthesized images using the simulated and measured numbers are shown

in Fig. 6.2, where Fig. 6.2(a) is the image with proposed WDR image sensor and Fig. 6.2(b) is with the conventional design. From the two images, it is noticeable that the image from the proposed structure contains more information in the low- and high-light regions than the conventional (marked by the dashed oval). To be more specific, the contour of the bulb as well as some details inside the lamp cover can be recognized, and a few very low-light regions still contain useful information in Fig. 6.2(a). On the contrary, these details are not visible in Fig. 6.2(b), so WDR imaging capability is not available.

In addition to DR, the images have a significant quality differences due to the FPN, where Fig. 6.2(a) has a FPN of 2%, while it is 7.5% in Fig. 6.2(b) which results in an intense visual artifact in the image. Considering that the pixel pitch and other specifications (such as the array size, sensitivity, SNR, and frame rate) are similar, the proposed WDR image sensor structure successfully achieves a better image quality by enormously increasing DR and reducing the FPN. In addition, the fill factor and power consumption are likely to be better when using this proposed design. Overall, the results show the benefits of the DDC and quad-sampling techniques and provides a clear demonstration on the improvement upon image quality.



(a)



(b)

Figure 6.2: The synthesized images of a PFM image sensor with an 8-bit resolution using (a) the quad-sampling as well as DDC techniques, and (b) the conventional approach. The marked regions indicate the difference of two images in the low- and high-light region, demonstrating the DR improvement. The pixel FPN are 2% and 7.5%, respectively.

6.3 Modified Quad-Sampling Technique

According to Chapter 5, the proposed quad-sampling technique can be adjusted to achieve different specifications in terms of the array size, DR, and frame rate. In this section, we change the values of N_1–N_4 and T_1–T_4 to those previously mentioned and summarized in Table 6.2. The maximum array size will become 1280 × 1024, and the DR increases to 134 dB; the trade-off is that the frame rate will reduce to 30 fps.

Table 6.2: Modified Values of N and T

Counter	N_1	N_2	N_3	N_4
Value	32	32	160	32
Sampling Time	T_1	T_2	T_3	T_4
Value	32 ms	1 ms	31.25 μs	195 ns

An updated schematic of the modified pixel and column circuits is shown in Fig. 6.3, where the pixel fill factor is expected to decrease due to the bit-increased counter (from 6 bits to 7 bits). There are only a few minor changes to accommodate the modified quad-sampling operation, including the added switch (M_{RS7}) in the pixel and the input-reduced NOR gate (3-input to 2-input).

Similarly, an image using the modified quad-sampling design is synthesized and shown in Fig. 6.4. In this figure, more details of the low-light region are captured and seen since this modified design essentially has longer first and second integra-

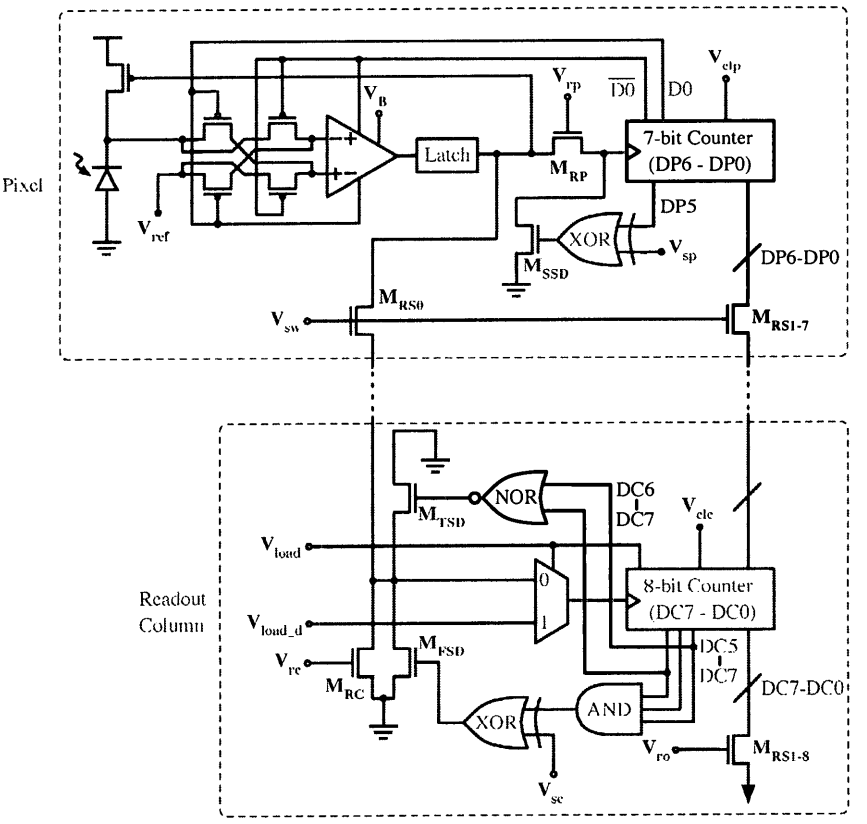


Figure 6.3: The schematic of modified quad-sampling pixel and column readout structure. The changed blocks are shown in black.

tion (sampling) times which provide better resolution of the dark contrast. This improvement is obvious in the marked regions where more dark information is available while the high-light region (lighting bulb) remains the same. In general, this example shows the flexibility of the quad-sampling technique, which can be changed according to specific needs or different performance targets. It is notable that the effect of temporal noise is also seen in certain very dark regions.

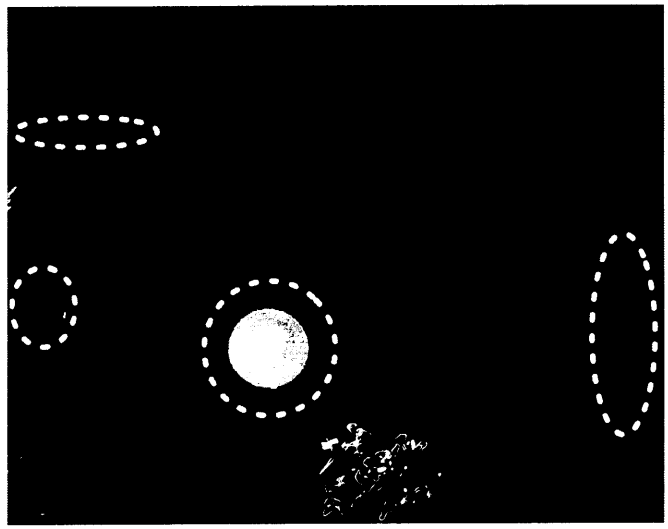


Figure 6.4: The synthesized image of a PFM image sensor with an 8-bit resolution using the modified quad-sampling as well as DDC techniques.

6.4 Summary

In this chapter, a complete WDR image sensor structure using the proposed DDC and quad-sampling techniques is presented. This structure successfully assembles

these techniques to realize an innovative WDR image sensor. In addition, a specification comparison of the proposed and conventional CMOS image sensor based on the PFM pixel is also shown using the calculation, measurement, and simulation results. Although the pixel pitch is not increased (and the fill factor is even slightly increased), the sensor reaches at least 124-dB DR and the FPN is reduced to an acceptable level of 1–3%. Nonlinearity is less than 1%, and the SNR remains high without SNR dip. Images demonstrating the performance of this design are also synthesized to clearly display the improvement.

Some other performances, such as the pixel crosstalk and substrate coupling from the digital signals, may not be evaluated without a real fabricated chip, however these issues are not critical given that a sufficient layout protection can be used toward the photodetector to reduce these unwanted noises. In addition, there are new technologies that can be used to directly solve or reduce these concerns and will be discussed in the last chapter. Nevertheless, the concepts and targets of this thesis can be well demonstrated through the presented works, in particular for the FPN and DR.

In general, the achieved performances are convincing according to the completed analysis through sufficient measurements and simulations, and this structure is believed to be ready for fabrication test once a proper fabrication process and suitable technologies are selected.

7 Conclusion

This thesis has considered a range of issues critical to the design of a practical PFM-based image sensor. The work completes the study of PFM pixel, including DR, linearity and temporal noise aspects, which were not completely understood in the past. In addition, an innovative DDC technique is proposed to reduce the problematic FPN (a spatial noise) among the PFM pixels as well as to increase the achievable DR and linearity. At last, a cost-effective, quad-sampling image sensor structure is designed to realize WDR imaging with a reduced cost in terms of a smaller pixel pitch and lower power consumption. By combining all the finished analysis and proposed designs, a low-cost and low-FPN WDR image sensor based on the PFM pixel can be implemented, providing an imaging performance comparable to those using the APS structure.

7.1 Research Summary

7.1.1 Analysis and Modeling of PFM Pixel

7.1.1.1 DR Optimization

The limitation on DR of the PFM pixel is investigated and found to be the result of reset, leakage, and dark current. Regardless of the actual value of reset current, DR is determined by whichever the larger between the leakage and dark current. In general, the rule of thumb to maximize DR and keep the low-light imaging ability is to make the leakage current very close to the dark current. A thick-oxide fabrication process which provides a lower leakage current of the reset transistor is also beneficial in increasing DR.

7.1.1.2 Linearity Modeling

The linearity of the PFM pixel is thoroughly investigated and several circuit models are developed to describe the mechanisms that lead to signal nonlinearity. Instead of the integration process, the integration delay and reset periods are also studied to find the root cause of nonlinearity. Appropriate models are given to support the simulation and measurement results, and the effects of each period are understood. Consequently, two important findings emerged. First, the integration delay degrades the linearity in the high-light region; second, the reset period will

affect (decrease) the upper boundary of DR since it increases with the illumination. The cause of these phenomena is the comparator propagation delay which can be modified (shortened) if a different (higher) bandwidth is achieved.

7.1.1.3 Noise

A complete noise measurement with respect to the output pulse frequency and different V_{diff} is performed to observe the noise performance. The result shows that the noise floor is primarily dominated by V_{diff} and can be estimated by using shot and reset noise models. In addition, there is also $1/f$ noise when the output frequencies are low, which increases the temporal noise from 2% up to 4.5%. Nevertheless, the overall SNR is still subject to a $\sqrt{N}$ improvement if a multiple-sampling readout is implemented.

7.1.2 Approach for FPN and DR Improvement

To suppress the serious FPN issue that has previously limited the application of PFM pixels, a DDC technique is designed and simulated. This approach adds only eight additional transistors in the pixel to realize the idea of switching the input connections as well as the polarity of comparator while leaving the V_{off} where it is. According to the simulation results, this technique successfully reduces the FPN from a usual 5–10% to an average of 1–3%, which shows a great improvement in

terms of image quality. In addition, both DR and linearity are increased. The observed DR extension is 12–26 dB, reaching the maximum available of a PFM pixel, and the linearity also becomes better as can be directly seen from the transfer curve.

7.1.3 Quad-Sampling Technique for WDR Imaging

Normally, a regular PFM pixel using a sampling readout with a counter is not likely to provide a 120-dB DR unless the counter is built with more than 20-bit resolution. This huge amount of digital circuitry means a very large pixel area (and cost) is inevitable. However, we apply the multiple-sampling readout which is popularly used in the APS to the PFM pixel to achieve WDR imaging and efficient pixel design at the same time. In addition to implementing the strategy, it is further evolved into a quad-sampling technique where multiple counting is implemented at both the pixel level and the column levels. The verification of this design is completed in an FPGA board in coordination with a sample fabricated PFM pixel. A 124-dB DR, 320 $\times$ 240 array size, and 60 fps design is achieved, with a potential of altering these parameters according to specific needs. In addition, the sampling strategy performs an automatic compression algorithm which makes the output directly usable by the displays without applying any image correction algorithm.

7.1.4 Quad-Sampling WDR Image Sensor with DDC Technique

A WDR image sensor structure using the proposed techniques and studies is designed for future implementation in silicon technology. This structure comprises the pixel array, the column readout, and the horizontal and vertical decoders, and it is intended to operate in a rolling shutter mode (or global shutter mode with a lower frame rate). Synthesized images with the new and conventional PFM pixels display the improvement under the same pixel pitch design, especially the DR and FPN. The flexibility of this structure is also discussed with an example of boosting the array to 1280 $\times$ 1024 and increasing the DR to 134 dB. With just a very few modifications of the pixel and column circuits, it achieves different specifications for other possible purposes.

7.2 Future Work

7.2.1 Design Optimization

A common target of designing a CMOS pixel is to reduce the pixel pitch which directly determines the fabrication cost versus image quality trade-off. This objective has been successfully achieved by the proposed quad-sampling technique which moves parts of the sampling to the column level. However, the achieved pixel pitch is still at least 3–10 times larger than that of the APS-based WDR image sen-

sors. As a result, more efforts can be done to continue the work of pixel pitch optimization (reduction).

The idea of transistor sharing between two or four adjacent pixels has been implemented to reduce the pixel pitch or to increase the FF, particularly for the very small pixel-pitch APS-based sensors [32, 54, 98–101]. Similarly, it is possible to apply the same concept to the proposed PFM pixel-based WDR image sensor. In Fig. 7.1, a pixel block diagram is shown, illustrating the sharing of sampling circuit between two pixels. In this figure, six additional switches are added to select the pixel for sampling operation, and an extra row signal (V_{ps}) will be required to choose between the two pixels.

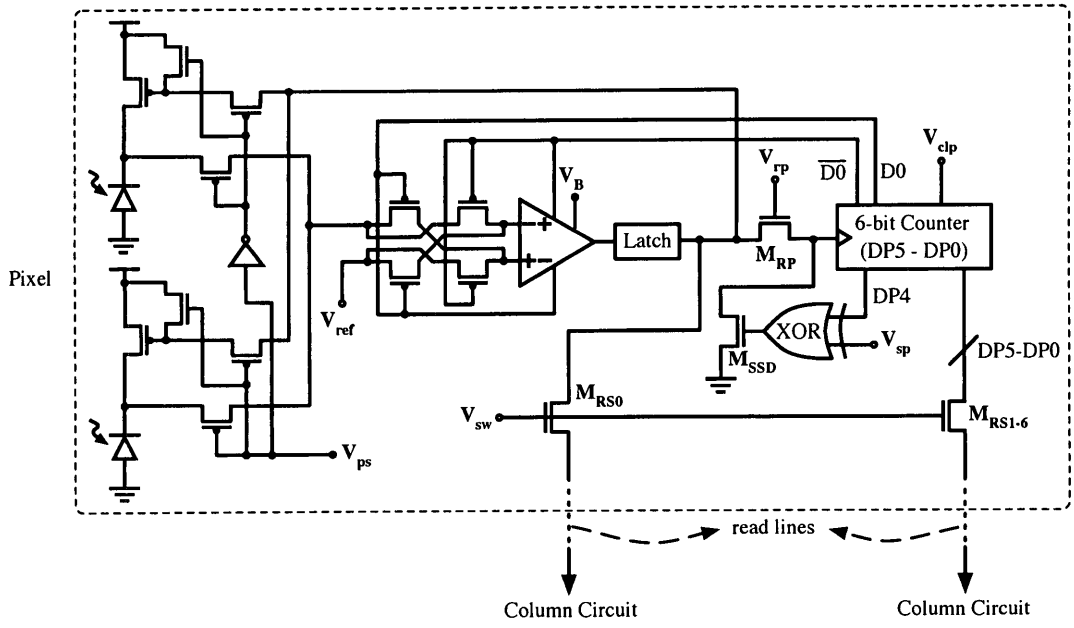


Figure 7.1: The pixel block diagram demonstrating the sharing of sampling circuit used in the quad-sampling WDR image sensor between two pixels.

According to the diagram, the pixel pitch is expected to decrease further by a substantial amount since the whole sampling circuit, including the comparator, the counter, and circuitry to perform the DDC and quad-sampling techniques, is shared by two pixels. On the other hand, if the size of photodetector is also reduced, the entire pixel can be even smaller with an expected value of 7–8 μm. Although the cost of achieving a smaller pixel is the lower frame rate which becomes half when the two-sharing pixel is used, this method is still useful for applications that dot not need high frame rates.

7.2.2 Chip Implementation

This work has completed an entire investigation toward the WDR image sensor design based on the PFM pixel. Since the scope of this research covers every important aspect, including the pixel- and column-level designs, approach to reduce FPN and to increase DR as well as linearity, and efficient sampling method to achieve WDR imaging, it is expected that the fabrication of this new WDR image sensor structure will meet the targeted performance. However, the critical optical performance, which is primarily determined by the fabrication technology, can not be easily estimated at the design stage and must be measured through experiments. These parameters, including QE, sensitivity, and angular response, will be acquired when the sensor is fabricated. In addition, some circuitry performances, such as

Q_{FW}, CG, dark current, and FOM of power, can be measured and calculated to completely address the sensor performance. Lastly, the image quality of this new sensor, in particular the DR, SNR, and FPN, will be formally quantified with the actual images it acquires.

7.2.3 Future Prospects for PFM Sensors

In this thesis, the PFM sensor has been carefully studied, and several techniques were proposed to improve its performances. The direct contribution of this work is to reduce the pixel pitch and improve FPN of this type of pixel. Although the evaluation results show that its usability can be significantly increased by the reduced cost and improved noise performances, the pixel size, or the FF, is still not comparable to that of the APS, which currently utilizes a pitch of 2–3 μm. This implies that the PFM sensor's optical performances, including the MTF, QE, and sensitivity, will be lower, thus the applicable conditions are limited, especially for those requiring the low-light imaging capability.

A possible solution to make the FF of PFM sensor comparable to the regular APS's is likely the use of new fabrication technologies. One approach is back-side illumination (BSI) process [99, 102, 103] [Fig. 7.2(a)], which has become popular recently and is believed to be a future trend that replaces the conventional front-side illumination (FSI) technology [Fig. 7.2(b)]. According to the figures, the BSI

process offers a wider and shorter light path, therefore the sensor's optical performances can be improved. However, the dark current of this technology is also higher, and a challenge to deal with if the low-light imaging capability is required.

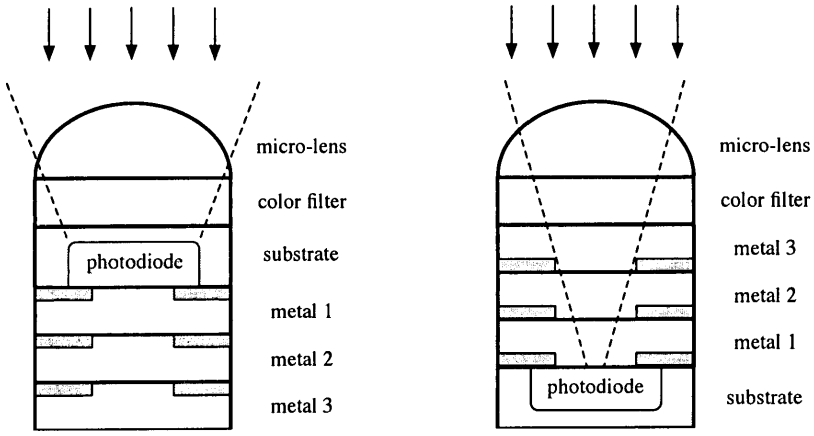


Figure 7.2: (a) BSI and (b) FSI technologies for CMOS image sensors. The metal stack can be further increased without affecting the light path using the BSI process.

Another alternative is to use the through-silicon via (TSV) technology, which was recently used to create 3-D image sensors [104, 105]. As such, it can be applied to the fabrication of an image sensor to release the constraints on pixel pitch. A concept diagram of utilizing this technology is given in Fig. 7.3, showing that multiple silicon layers can be combined together with the original photodetector layer vertically through appropriate vias and bumps. Since most of the circuitry that typically resides in the substrate layer can be moved to other silicon layers, the pixel pitch can be reduced and the FF can be very large. In this example,

the analog circuitry is moved to the silicon layer beneath the substrate, and the digital is further in the second layer. Consequently, there exists only the photodiode and reset transistor in the substrate, thus the pixel's optical performances can be significantly improved. Although this technology is attractive to the development of PFM sensor, the current via size is still at least a few microns, and is definitely a key issue prior to the practical implementation of small pixel array.

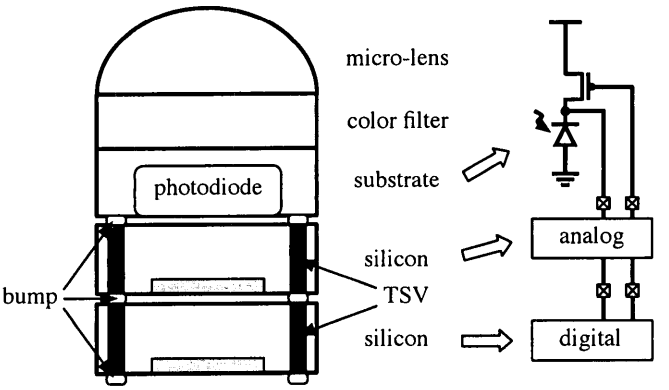


Figure 7.3: The concept diagram of TSV technology applying to the BSI CMOS image sensor.

As the need for more DR grows continuously, the benefits of the PFM pixel will make it the best candidate for future image sensor design. Meanwhile, the evolving technologies, including the shrinking feature size of CMOS processes and various advanced fabrication and packaging techniques, will also assist in elaborating the PFM pixel. In conclusion, the results presented in this thesis provide useful information and methodologies, and successfully demonstrate some possibilities for its future development.

A Two-Step Readout APS

A.1 Introduction

A two-step readout APS is designed and tested to evaluate the achievable DR of APS-based CMOS image sensor. This objective is realized by proposing a two-step readout pixel, which utilizes two different readout characteristics to provide a large voltage swing in an effort to increase Q_{FW}. The measurement result can be used to conclude the DR limitation of an APS system.

A.2 Sensor Design

A.2.1 Two-Step Readout Pixel Analysis

We use a PMOS as a common-source amplifier to replace the conventional NMOS source follower, in order to design a two-step readout pixel [106]. The proposed pixel schematic is shown in Fig. A.1. A PMOS reset transistor (M_{RT}) hard-resets FD and PD to V_{DD}, so a maximum potential for charge accumulation and a short reset pulse are achieved. The common-source amplifier (M_A) converts the charges at FD to a voltage when readout is performed. It is notable that M_A inverts the input signal, unlike the source follower in the conventional APS. The diode-connected NMOS (M_C) is designed to operate with M_A to generate a linear voltage output. It could operate in either the saturation region (providing bias current) or the triode region (a voltage-dependent resistance). The row-select transistor (M_S) is the same as a normal APS. M_{TX} is included to hold the charges at FD by turning it off when the pixel is read out. As the figure shows, the wasted signal room at FD is very small, and V_O is mainly limited by V_{DSA} (drain-to-source voltage of M_A) and V_{GSC} (gate-to-source voltage of M_C) which change according to V_{FD}. In addition, the photodiode can be replaced by photogate with an additional gate control signal. The simplified pixel transfer curve is derived below.

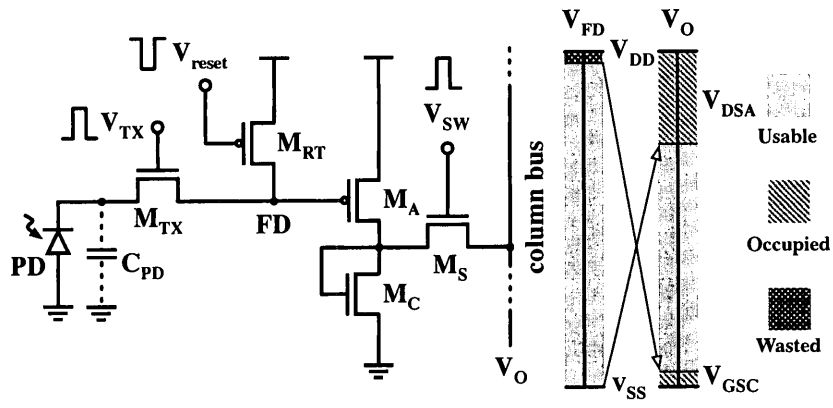


Figure A.1: The schematic of proposed two-step readout active pixel structure. The photodiode can be directly replaced by a photogate since M_{TX} is used.

M_{A} and M_{C} in subthreshold: The use of PMOS for M_{A} is beneficial when the potential at FD is low, since M_{A} will not be in the cutoff region. However, when the potential is high and close to V_{DD}, M_{A} will operate in subthreshold (or deep-subthreshold) and only conducts a very small current. To cooperate with the tiny current, M_{C} is designed to work in the subthreshold region as well. Therefore, the relationship between V_{O} and V_{FD}, assuming M_{S} is ideal, can be derived as

$$V_{\mathrm{O}} = V_{\mathrm{TN}} + n_2 \cdot \left[V_{\mathrm{T}} \cdot \ln\left(\frac{I_{\mathrm{DP0}}}{I_{\mathrm{DN0}}}\right) + \frac{V_{\mathrm{DD}} - V_{\mathrm{FD}} - V_{\mathrm{TP}}}{n_1} \right] \tag{A.1}$$

where V_{T} is the thermal voltage, V_{TN} and V_{TP} are the threshold voltages, I_{DN0} and I_{DP0} are the drain currents at $V_{\mathrm{GS}} = V_{\mathrm{th}}$, and n_2 and n_1 are the slope factor, of NMOS and PMOS, respectively. Furthermore, n_1 and n_2 are given by

$$n = 1 + \frac{C_{\mathrm{D}}}{C_{\mathrm{OX}}} \tag{A.2}$$

where C_{D} and C_{OX} are the capacitances of the depletion and oxide layers of the transistor, respectively. From (A.1), we can find that V_{O} is proportional to V_{FD} with a factor defined by

$$\frac{n_2}{n_1}. \tag{A.3}$$

M_{A} and M_{C} in saturation: When V_{FD} is lower than $V_{\mathrm{DD}} - V_{\mathrm{TP}}$, M_{A} is in the saturation region. In this case, M_{C} is also adjusted to operate in saturation. The

relationship between V_O and V_{FD} is then derived from the conventional transistor current formula as

$$V_O = V_{TN} + \sqrt{\frac{K_P \frac{W_P}{L_P}}{K_N \frac{W_N}{L_N}}} \times (V_{DD} - V_{FD} - V_{TP}) \tag{A.4}$$

where K_N and K_P are the dielectric constants of the gate oxide, W_N/L_N and W_P/L_P are the widths and lengths, of the NMOS and PMOS, respectively. Note that the effect of channel length modulation (CLM) is ignored to simplify the derivation. From (A.4), it is observed that V_O is proportional to V_{FD} with another factor given by

$$\sqrt{\frac{K_P \frac{W_P}{L_P}}{K_N \frac{W_N}{L_N}}}. \tag{A.5}$$

Based on (A.3) and (A.5), the pixel has two different factors for the transfer curve. When the photo-signal is low, i.e. V_{FD} is high, the factor is higher since the ratio of n_2/n_1 is usually more than unity for common CMOS processes. On the other hand, this factor becomes lower when the photo-signal is high because K_P is normally smaller than K_N (assuming the transistors' widths and lengths are identical). The real condition of the pixel transfer curve (from V_{FD} to V_O) is more complicated than the simplified analysis of (A.1) and (A.4), however this simplified analysis is enough to predict the pixel output response and provide design directions. Besides, the transfer curve shows that the pixel is able to generate useful information for both low and high V_{FD} by operating the in-pixel amplifier in either subthreshold or saturation.

To realize the voltage gain of the in-pixel amplifier, we calculate its small-signal gain using a reasonable simplification. The gain can be derived and given by

$$A_V = g_{mp} \cdot (\frac{1}{g_{dsp}} // \frac{1}{g_{dsn}} // \frac{1}{g_{mn}}) \tag{A.6}$$

where g_{mp} and g_{mn} are the transconductances, g_{dsp} and g_{dsn} are the conductances, of PMOS and NMOS, respectively. Since g_{dsp} and g_{dsn} are tens to hundreds of magnitude higher than g_{mn} in most cases, the gain can be simplified to

$$A_V \approx \frac{g_{mp}}{g_{mn}}. \tag{A.7}$$

The values of g_{mp} and g_{mn} are strongly dependent on the drain current, thus the small-signal gain is not constant like a conventional APS. The design of M_A

and M_C, however, can be adjusted to provide different transfer curves according to individual applications.

A.2.2 Noise Analysis

The pixel's temporal noise is calculated as follows, assuming the photodiode capacitance is linear throughout the entire integration process. The mean square noise voltages of the reset and shot noises are commonly quoted to be [35]

$$\overline{V_{\text{n.reset}}^2} = \frac{kT}{C_{\text{pd}}} \tag{A.8}$$

and

$$\overline{V_{\text{n.shot}}^2} = \frac{q(i_{\text{ph}} + i_{\text{dc}})}{C_{\text{pd}}^2} \cdot t_{\text{int}} \tag{A.9}$$

where T is the temperature in degrees kelvin, C_{pd} is the photodetector capacitance, i_{ph} and i_{dc} are the photocurrent and dark current, and t_{int} is the integration time. The readout noise is analyzed by using the small-signal circuit model of the pixel structure shown in Fig. A.2. It consists of M_A, M_C, and M_S, where g_{ma} and g_{mc} are the transconductances of M_A and M_C, g_{ds} is the conductance of M_S, C_O is the bit-line-referred capacitance, and $I_{\text{MA}}(t)$, $I_{\text{MC}}(t)$, and $I_{\text{MS}}(t)$ are the equivalent thermal noise sources of M_A, M_C, and M_S, respectively. The bit-line-referred mean square noise voltages due to M_A, M_C, and M_S are given by

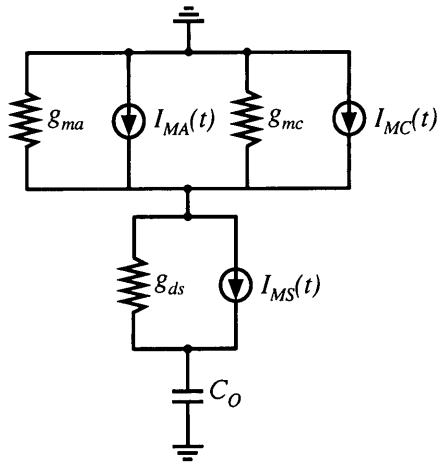


Figure A.2: Small-signal model for noise analysis during readout.

$$\overline{V_{\text{n.MA}}^2} = \frac{2}{3}\frac{kT}{C_{\text{O}}}\frac{g_{\text{ma}}g_{\text{ds}}(g_{\text{ma}}+g_{\text{mc}})(g_{\text{ma}}+g_{\text{mc}}+g_{\text{ds}})}{(g_{\text{ma}}g_{\text{mc}}+g_{\text{ma}}g_{\text{ds}}+g_{\text{mc}}g_{\text{ds}})^2} \tag{A.10}$$

$$\overline{V_{\text{n.MC}}^2} = \frac{2}{3}\frac{kT}{C_{\text{O}}}\frac{g_{\text{mc}}g_{\text{ds}}(g_{\text{ma}}+g_{\text{mc}})(g_{\text{ma}}+g_{\text{mc}}+g_{\text{ds}})}{(g_{\text{ma}}g_{\text{mc}}+g_{\text{ma}}g_{\text{ds}}+g_{\text{mc}}g_{\text{ds}})^2} \tag{A.11}$$

and

$$\overline{V_{\text{n.MS}}^2} = \frac{kT}{C_{\text{O}}}\frac{g_{\text{ma}}+g_{\text{mc}}}{g_{\text{ma}}+g_{\text{mc}}+g_{\text{ds}}}. \tag{A.12}$$

Note that the sizes of M_{A} and M_{C} are chosen to achieve the desired pixel pitch.

The transfer gate (M_{TX}) also contributes to the temporal noise while it is turned on and the signal is transferred from PD or photogate to FD. According to [107], it can be modeled as a shot-noise-like noise source as (A.9) shows.

A.2.3 System Architecture

A complete sensor block diagram is shown in Fig. A.3 [108]. Three different pixel arrays are implemented, each of 36 × 96 (effective 32 × 92) pixels. Each pixel is 5 μm × 5 μm. A row decoder is shared by these arrays and used to control the pixel operation, including reset, integration, and readout. Each column readout circuit is equipped with an voltage-to-frequency converter and a 10-bit counter, and a column decoder is used to determine the readout sequence. The data stored in the counter is sent out serially with a 10-bit data width.

A.2.4 Timing Diagram

The control signal for the pixel is similar to a conventional 4-T APS. The sensor has a rolling shutter mode, and the reset and row-select have typical operations. The V_{TX} signal, however, is set high when the integration completes and the accumulated charges are ready to be transferred to FD. After transmission, it is set low to hold the charges at FD, while the column readout circuit, which requires a short period of time to execute the readout process, is operational. Since a voltage-to-frequency converter is used, no extra control signal is required by the column readout circuit. Instead, the reset and enable signals are necessary for the counters to reset after its signal is sent off-chip, and to re-start the counting procedure when reading the next pixel. A complete timing diagram is shown in Fig. A.4.

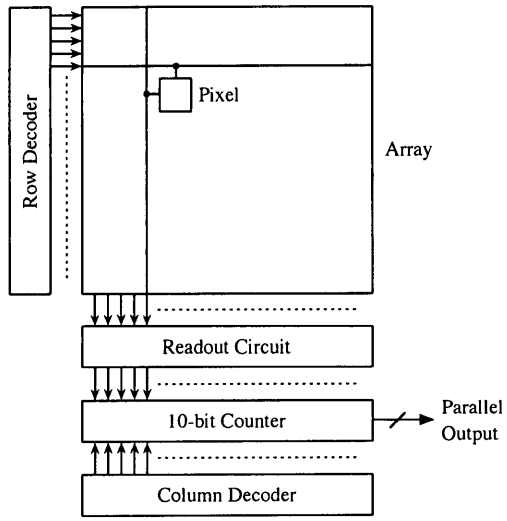


Figure A.3: The block diagram of proposed two-step readout image sensor.

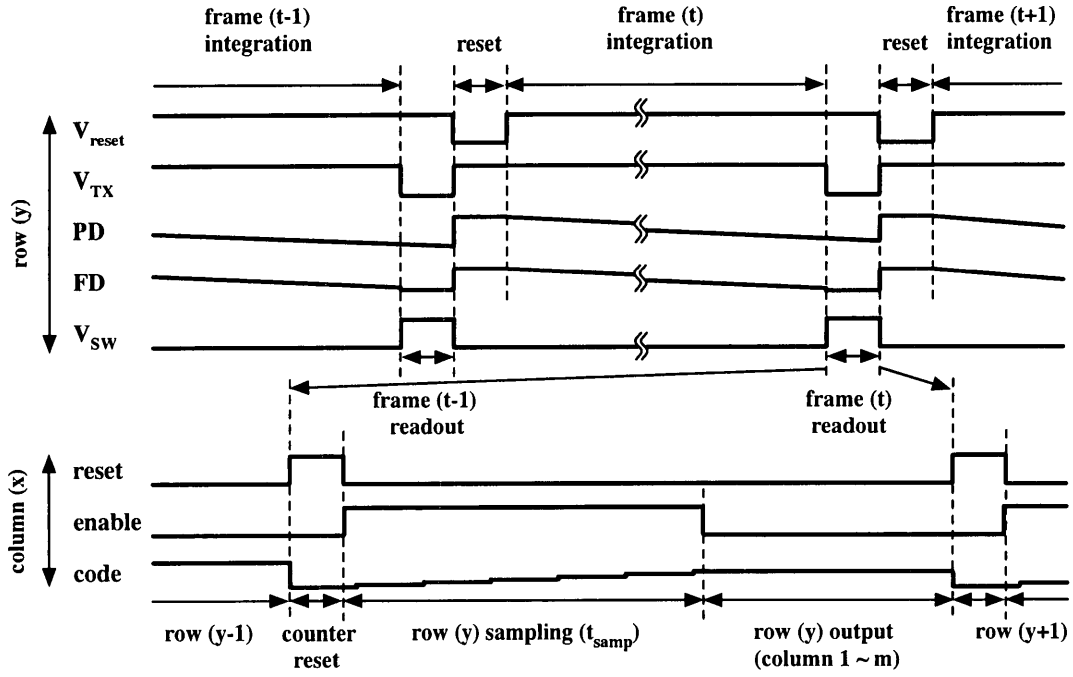


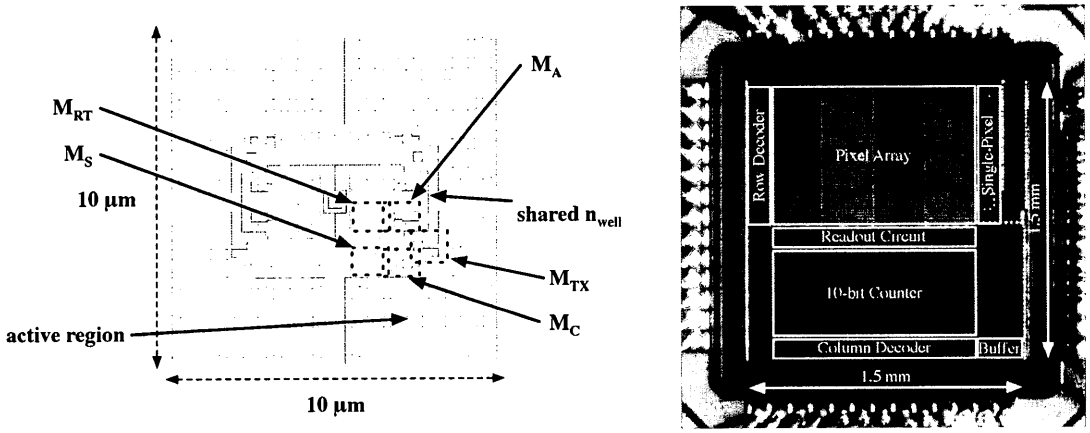
Figure A.4: Timing diagram for the two-step readout active pixel (not to scale).

The imager operation is described as follows. A reset signal (V_{reset}) is first set to low to reset each pixel and set to high to start integration. After the integration completes, V_{SW} goes high when V_{TX} is set to low which holds the charges at FD and maintains a relatively stable potential. When V_{SW} is high, the column readout procedure starts with a reset signal for all counters (reset high). This reset period must be long enough to have all pixel signals settle on each column bus, and it is 5 μs in this design. After reset, a short period of time is given (t_{samp}) at enable for the output frequency to be sampled. After sampling, enable is set to low and the data in counter is sent out column by column. After signal readout, another reset signal is given to reset the counter for the next row. At the same time, V_{reset} is set to low for those pixels which finish signal readout to start a new integration of next frame.

A.3 Sensor Fabrication and Experimental Setup

The design uses two PMOSs in the pixel, therefore an n-well layer is necessary. In order to keep the FF of this 5 μm $\times$ 5 μm pixel as high as possible, we use a shared n-well layout technique [109]. As Fig. A.5(a) shows, the n-well region is placed in the center of four adjacent pixels to save the area for pixel active region. It is noteworthy that the use of n-well will create another p-n junction in the pixel and it may attract or generate some free carriers in the substrate by forming a latchup. This layout arrangement also slightly affects sensor's MTF and signal uniformity between adjacent columns. To avoid its behaving as another photodiode, it is necessary to block the incident light from reaching this area. In this design, this area is covered with top-layer metal.

The design was fabricated using a 0.13-μm 1-poly 8-metal CMOS process with a die size of 1.5 mm $\times$ 1.5 mm. The power supply is 1.25 V for the core (analog) circuitry and 2.5 V for the I/O. The photomicrograph of the fabricated sensor is shown in Fig. A.5(b). It was attached to a testing board which was designed for the electro-optical measurement, as shown in Fig. A.6. A tungsten bulb was used with an integrating sphere to provide a stable light source between 1 and 100,000 lux, and the required control signals were provided through a pattern generator. A mixed-signal oscilloscope was used to measure the performance of different pixel designs. The array parallel output was logged by a logic analyzer for image construction and further calculation, and the master clock rate for the imager was 400 KHz.



(a) (b)

Figure A.5: A 2 × 2 pixel array layout (n^+/p-sub photodiodes).

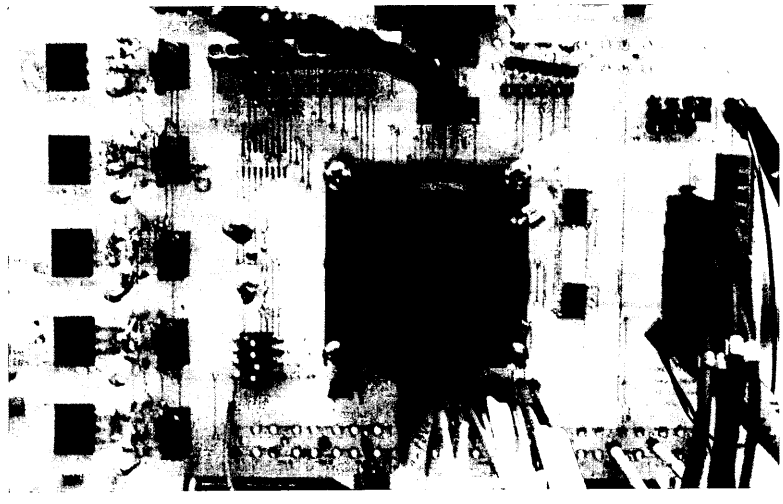


Figure A.6: The PCB board attached with measured chip and lens.

A.4 Experimental Results

A.4.1 Measurements of Transfer Curve and SNR

The pixel design was verified by performing single pixel measurements. The integration time was 16 ms and measurement results are plotted in Fig. A.7.

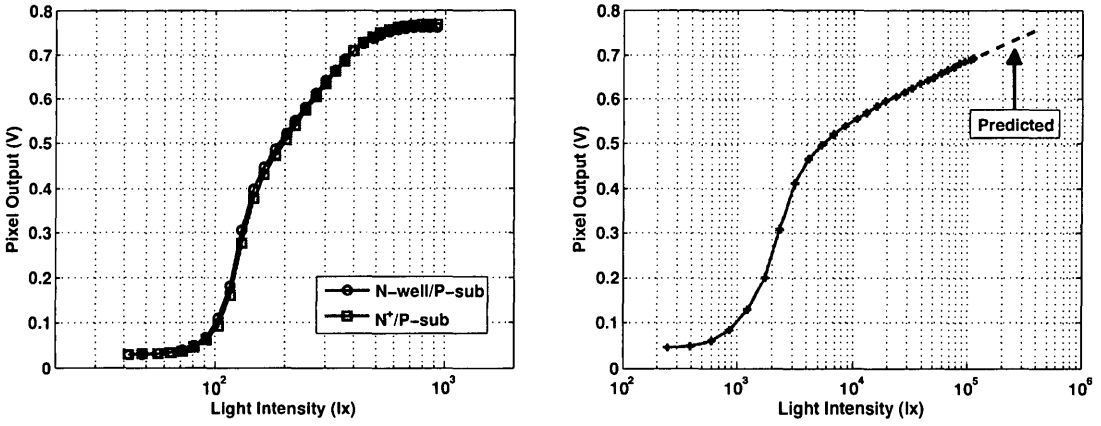


Figure A.7: The measured transfer curves of (a) n-well/p-sub and n^+/p-sub pixels, and (b) photogate. The photodiodes have similar photoresponses. Photogate has a much lower sensitivity but a higher DR. The predicted line shows that a 61-dB DR is possible.

The results of n-well/p-sub and n^+/p-sub photodiodes are presented in the same graph, as shown in Fig. A.7(a). Although the junction depth of n-well is deeper than n^+, the difference of the transfer curves from the two photodiodes is not obvious. Generally, n-well/p-sub photodiode has better sensitivity than n^+/p-sub [110], however the phenomenon is less obvious in sub-micron processes. Moreover, in the design the active area for n-well/p-sub photodiode is smaller by 28%. The result for the photogate is plotted individually in Fig. A.7(b) since the imaging range is much higher than the other two. This is because the use of poly gate creates a much deeper Q_{FW} which is a benefit for the photogate.

We can observe from the two figures that the pixel output response has two steps. When the incident light intensity is low, the output increases with a higher sensitivity due to the calculations we derive in (A.1). This higher sensitivity starts changing when the input signal gets stronger and the pixel output voltage is above 0.4 V. As (A.4) predicts, the sensitivity decreases due to a typically larger K_{P}, and it

results in an extension of the high-light scheme detection. Note that the photogate pixel output does not reach the threshold of the second region within the available illumination. There is a nonlinear response when the pixel output voltage is below 0.1 V. This is because when V_{DSN} is small, the subthreshold current is expressed by

$$I_{\mathrm{DN}} = I_{\mathrm{DN0}} \cdot \exp^{\frac{V_{\mathrm{GSN}} - V_{\mathrm{TN}}}{n_2 V_{\mathrm{T}}}} \cdot (1 - \exp^{\frac{-V_{\mathrm{DSN}}}{V_{\mathrm{T}}}}) \tag{A.13}$$

where the second exponential term of (A.13) will not be negligible when V_{DSN} is small, and an exponential effect is observed on the output, as the results show.

From the two figures, we also observe that the sensitivity of photogate is only about one-fifth of that of photodiodes in the 8-metal layer standard CMOS process. The lower sensitivity is the result of opaque poly silicon gate used for creation of depletion region. The trade-off of using photogate is the increase of depletion region (i.e., the Q_{FW}) and an extending DR. Although the instrument is not sufficient to provide higher illumination for the measurement, it is predicted that the photogate pixel has a DR of about 61 dB.

In a typical 3-T or 4-T APS structure, the noise floor increases with the output signal, dominated by the photon shot noise. However, the noise floor gets lower when the output signal is high in the proposed design. This is because of the lower gain of the pixel amplifier which suppresses shot noise. Based on the measured noise value, we can calculate the pixel SNR as shown in Fig. A.8. The maximum SNR for each of the three pixels reaches more than 50 dB. The SNR is below 40 dB for lower pixel signal (especially for n-well/p-sub pixel) which is due to the noise spike observed from the measurement [106]. Photogate pixel has more than 5 to 8 dB SNR advantage at this range which is a benefit of using this structure.

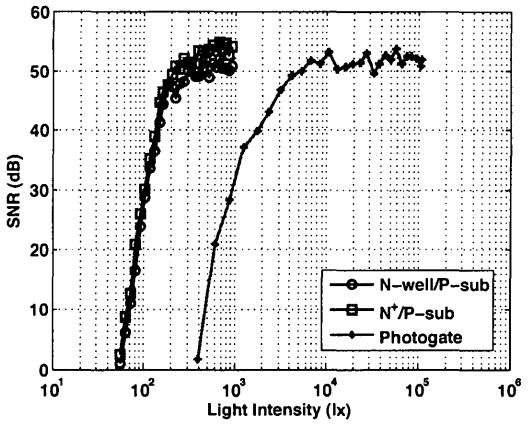


Figure A.8: Measured pixel SNR.

A.4.2 Image Acquisition

The performance of the imaging array is tested with a constant illumination intended to have each imaging array at approximately 50% saturation level. The imager frame rate is set at 60 fps. From the acquired images shown in Fig. A.9, we observe that there is offset between odd and even columns resulting in stripes which greatly affect the image appearance. This is believed to be because of the mirrored layout orientation between odd and even columns used to fit the pixel. Although the design has an originally large column FPN due to layout orientation, a less than 0.50% value is still calculated within columns of the same layout orientation. Pixel FPN is also calculated (with the same column) and is below 0.16% for the three imaging arrays. Temporal noise is also measured at below 0.59%. The results show that n-well/p-sub photodiode pixel array has a larger temporal noise and column FPN, while the photogate pixel array has the best performance.

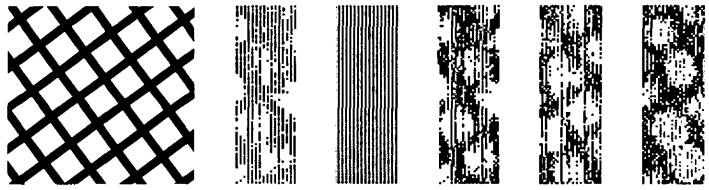


Figure A.9: The sample pattern is shown in (a). (b) is the raw image captured by the n-well/p-sub pixel array. (c) shows the column FPN between odd and even columns induced by the layout orientation. The processed image for n-well/p-sub, n^+/p-sub, and photogate pixel arrays are shown in (d), (e), and (f), respectively, with column offsets adjusted.

A.5 Limitations of APS for WDR Imaging

In this appendix, a two-step readout APS structure is presented, demonstrating a method to fully read out Q_{FW}. However, the maximum achieved DR is still below 61 dB, and it is dominated by the noise floor and Q_{FW}. As a result, DR can not reach 100 dB unless the usable voltage range is increased by 100 times, i.e., $V_{DD} = 120$ V, which is not practical at all. This work suggests that a multiple-sampling or time-based image sensor are necessary for WDR imaging.

B FPGA Implementation

B.1 VHDL Codes

B.1.1 AND Gate

```
entity and_3 is
    Port ( a : in std_logic_vector (0 downto 0);
           b : in std_logic_vector (0 downto 0);
           c : in std_logic_vector (0 downto 0);
           f : out std_logic_vector (0 downto 0));
end and_3;

architecture Behavioral of and_3 is

begin
    process(a,b,c)
    variable var_s1: std_logic_vector (0 downto 0);
    begin
        var_s1 := a and b;
        f <= var_s1 and c;
end process;

end Behavioral;
```

B.1.2 NOR Gate

```
entity nor_3 is
    Port ( a : in std_logic_vector (0 downto 0);
           b : in std_logic_vector (0 downto 0);
           c : in std_logic_vector (0 downto 0);
           f : out std_logic_vector (0 downto 0));
end nor_3;
```

```
architecture Behavioral of nor_3 is

begin
    process(a,b,c)
    variable var_s1: std_logic_vector (0 downto 0);
    variable var_s2: std_logic_vector (0 downto 0);
    begin
        var_s1 := a or b;
        var_s2 := var_s1 or c;
        f <= not var_s2;
end process;

end Behavioral;
```

B.1.3 XOR Gate

```
entity xor1 is
    Port ( a : in std_logic_vector (0 downto 0);
           b : in std_logic_vector (0 downto 0);
           f : out std_logic_vector (0 downto 0));
end xor1;

architecture Behavioral of xor1 is

begin
    f <= a xor b;

end Behavioral;
```

B.1.4 In-pixel Counter

```
entity counter_6b is
    Port ( clk : in std_logic;
           reset : in std_logic;
           d : out std_logic_vector(5 downto 0);
 d4 : out std_logic_vector(0 downto 0));
end counter_6b;
```

```
architecture Behavioral of counter_6b is
    signal count :std_logic_vector(5 downto 0);

begin
    process (clk, reset) begin
        if (reset ='1') then
            count <= (others=>'0');
    elsif (rising_edge(clk)) then
            count <= count + 1;
        end if;
    end process;

    d <= count;
    d4 <= count(4 downto 4);
end Behavioral;
```

B.1.5 Column Counter

```
entity counter_9b is
    Port ( clk : in std_logic;
           reset : in std_logic;
           load : in std_logic;
           i : in std_logic_vector(5 downto 0);
          d : out std_logic_vector(8 downto 0);
          d5 : out std_logic_vector(0 downto 0);
          d6 : out std_logic_vector(0 downto 0);
          d7 : out std_logic_vector(0 downto 0));
end counter_9b;

architecture Behavioral of counter_9b is
    signal count :std_logic_vector(8 downto 0);

begin
    process (clk,reset)
        variable temp : std_logic_vector(5 downto 0);
    begin
        if (reset ='1') then
            count <= (others=>'0');
        elsif (rising_edge(clk)) then
```

```
            if (load='1') then
                temp := i;
                count (5 downto 0) <= i;
    else
                count <= count + 1;
            end if;
        end if;
    end process;

    d <= count;
    d5 <= count(5 downto 5);
    d6 <= count(6 downto 6);
    d7 <= count(7 downto 7);
end Behavioral;
```

B.1.6 Multiplexer

```
entity mux1 is
    Port ( d0 : in std_logic;
           d1 : in std_logic;
           sel : in std_logic;
           muxout : out std_logic);
end mux1;

architecture Behavioral of mux1 is

begin
    muxout <= d0 when (sel='0') else
              d1;

end Behavioral;
```

B.1.7 Readout Switch

```
entity mux4 is
    Port ( d0 : in std_logic_vector(5 downto 0);
           d1 : in std_logic_vector(5 downto 0);
           sel : in std_logic;
           muxout : out std_logic_vector(5 downto 0));
```

```
end mux4;

architecture Behavioral of mux4 is

begin
    muxout <= d0 when (sel='0') else
              d1;

end Behavioral;
```

B.2 FPGA Block Diagram of Quad-Sampling Design

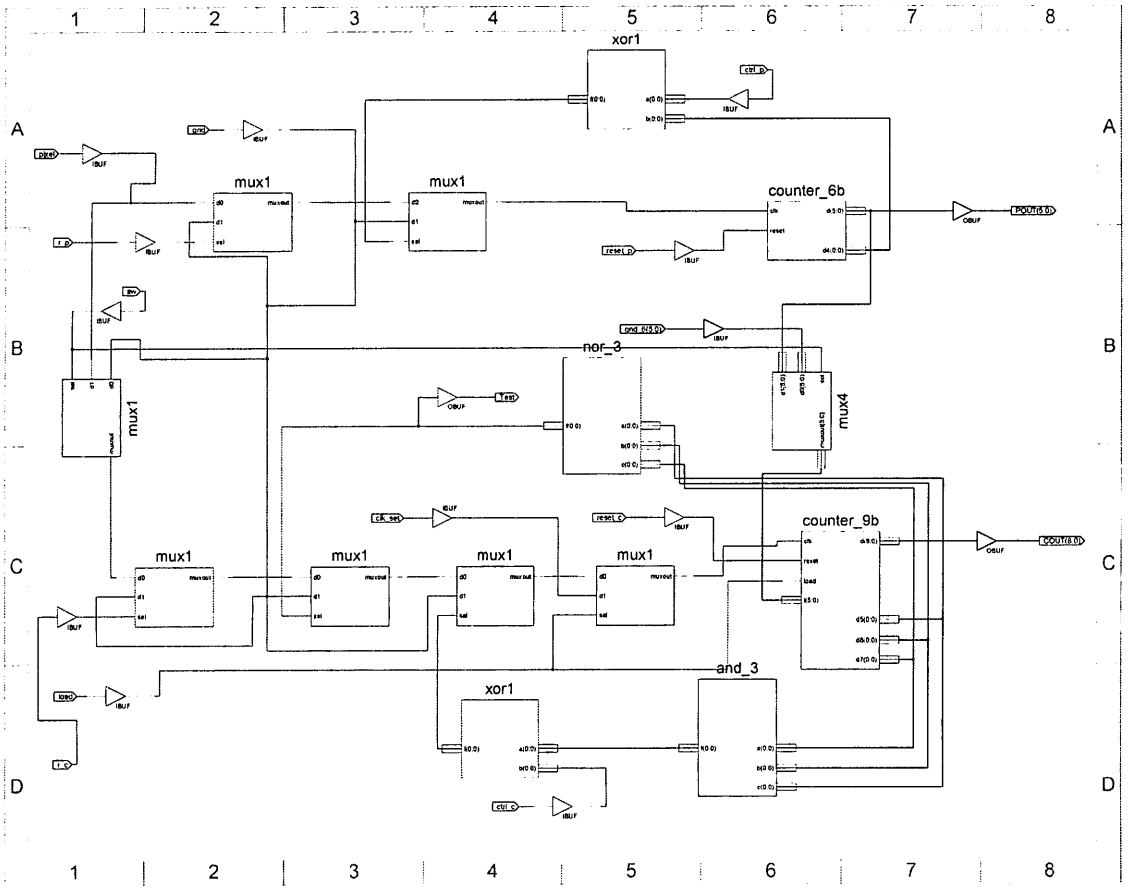


Figure B.1: The block diagram of quad-sampling structure.

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