IMPACT OF MATERIALS DISORDER ON GRAPHENE HETEROSTRUCTURE DEVICES

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Corey Alexander Joiner

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IMPACT OF MATERIALS DISORDER ON GRAPHENE HETEROSTRUCTURE DEVICES

Approved by:

Dr. Eric Vogel, Advisor
School of Materials Science and Engineering
Georgia Institute of Technology

Dr. Lin
School of Materials Science and Engineering
Georgia Institute of Technology

Dr. Vladimir Tsukruk
School of Materials Science and Engineering
Georgia Institute of Technology

Dr. Jiang
College of Physics
Georgia Institute of Technology

Dr. Faisal Alamgir
School of Material Science and Engineering
Georgia Institute of Technology

Date Approved: August 08, 2016

Dedicated to my wife and family

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LIST OF SYMBOLS AND ABBREVIATIONS

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
APS	Ammonium Persulfate
BiSFET	Bilayer Pseudo-Spin Field-Effect Transistor
BTBT	Band to Band Tunneling
CMOS	Complementary Metal Oxide Semiconductor
CNP	Charge Neutral Point or Dirac Point
CVD	Chemical Vapor Deposition
DI	Deionized Water
DOS	Density of States
FET	Field-Effect Transistor
FWHM	Full Width at Half Maximum
GFET	Graphene Field-Effect Transistor
hBN	Hexagonal Boron Nitride
HOPG	Highly Oriented Pyrolytic Graphite
IPA	Isopropyl Alcohol
IR	Infra-Red
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NDR	Negative Differential Resistance
NMOSFET	n-type Metal Oxide Semiconductor Field-Effect Transistor
PMMA	Poly(methyl methacrylate)
RF	Radio Frequency
SEM	Scanning Electron Microscopy

SKPM	Scanning Kelvin Probe Microscopy
SymFET	Symmetric (tunneling) Field-Effect Transistor
TDMAH	Tetrakis(dimethylamido) Hafnium
TDMAT	Tetrakis(dimethylamido) Titanium
TEM	Transmission Electron Microscopy
TFET	Tunneling Field-Effect Transistor
TMA	Trimethyl Aluminum
TMD	Transition Metal Dichalcogenide
XPS	X-Ray Photoelectron Spectroscopy

SUMMARY

This work is focused on characterizing the impact of material based disorder on the properties of graphene based vertical tunneling heterostructures. The motivation and challenges for replacing silicon for low power digital electronics has been presented. The status of the research on graphene based digital electronics is critically reviewed. Scalable methods for synthesizing large area two dimensional materials including graphene, molybdenum disulfide, and hexagonal boron nitride are integrated into a complex CMOS fabrication process to investigate the impact of disorder on the properties of vertical graphene based heterostructures for low power digital electronics.

The foci for this study were 1) reducing the disorder in the form of contaminants and defect generation in the graphene structure introduced during the CMOS fabrication process 2) elucidating the impact of disorder on vertical tunneling in a graphene based vertical heterostructure 3) investigating the impact of sequential two dimensional material synthesis on the disorder and electrical performance of the fabricated heterostructures. The major findings of this work can be summarized by the following:

- The CMOS fabrication process was found to introduce contaminants in the form of polymeric residues that reduced the lateral conduction of the graphene. Thermal decomposition of the residues resulted in the introduction of defects in the graphene. A chemical etching method utilizing a sacrificial titanium layer removed via HF etching effectively removed the contaminants without damaging the graphene.
- Dielectric tunneling barriers were deposited by atomic layer deposition (ALD). The tunneling mechanism of the deposited barriers was found to be

defect mediated tunneling which is undesirable for the graphene based heterostructures. By reducing the thickness of the tunneling barriers, direct tunneling became the dominant tunneling mechanism. By altering the tunneling barrier, the possibility of barrier engineering to tailor the electrical characteristics of the graphene heterostructure device was experimentally shown. Despite direct tunneling being the dominant tunneling mechanism for thin dielectric barriers, the electrical properties with ALD deposited dielectrics was found to be inadequate. Graphene of various domain sizes was used to assess the impact of disorder induced by the graphene on the heterostructure electrical properties. No change in the electrical properties was observed indicating the underlying substrate and interlayer dielectric are the limiting sources of disorder suppressing the heterostructure electrical properties.

- Following recent reports utilizing exfoliated materials, two dimensional materials (molybdenum disulfide and hexagonal boron nitride) complimentary to graphene were utilized as tunneling dielectrics to further improve the device performance over conventional dielectric materials. The direct synthesis of complimentary two dimensional materials on graphene was shown to introduce defects into the graphene structure and to suppress the electrical properties of the graphene. Trapping of electrons due to the large number of trap states in the as synthesized molybdenum disulfide was shown to drastically suppress the tunneling current in the graphene vertical heterostructure compared to exfoliated materials.

- Hexagonal boron nitride was used as a buffer layer between the graphene electrode and underlying SiO_2 substrate to determine the impact of the substrate on the graphene heterostructure performance. A large area synthesized hexagonal boron nitride buffer layer was shown to improve the lateral conduction of the graphene. Contrary to reports of exfoliated materials, the introduction of a hexagonal boron nitride tunneling barrier was shown to reduce the mobility of the graphene due to increased scattering as a result of defects in the hexagonal boron nitride as well as contamination introduced during the transfer process. The lateral conductance of the graphene was shown to be improved in the graphene vertical heterostructure with a hexagonal boron nitride buffer layer, but was insufficient to improve the vertical tunneling of the heterostructure. Improved synthesis methods to reduce the intrinsic defects in the as synthesized hexagonal boron nitride is necessary to further improve the graphene heterostructure performance.

Overall, the research presented here provides important insights into the use of graphene based heterostructures for digital electronic applications. We provided methodology for integrating graphene into a CMOS fabrication process, suggest potential pathways for tailoring the device characteristics through barrier engineering, and demonstrate the current limitations of two dimensional heterostructures. We find the limiting factor to be the materials used in support of graphene.

CHAPTER 1: INTRODUCTION

1.1 Moving Beyond Si

The 1956 Nobel Prize in physics was awarded for the discovery of transistor action in germanium. Discovered in 1948[1-3], the transistor soon began replacing vacuum tubes in a wide variety of applications due to its small size and high reliability of operation. Germanium remained the material of choice for semiconductors until ~1960, when silicon began to dominate as the semiconducting material of choice.[4]

Silicon overtook germanium as the material of choice for several main reasons. First, germanium has a band gap of 0.67 eV, diminishing the reliability of germanium based transistors at elevated temperatures. The 1.1 eV bandgap of silicon allows for reliable operation at typical operating temperatures of up to 100°C.[5] Second, processing breakthroughs in silicon purification and diffusional doping at Bell Labs in the 1950s drastically improved the yield and ease of fabrication for silicon based transistors.[4] Third, silicon oxide forms a high quality interface with silicon with a low concentration of interfacial traps and serves as an excellent electrical insulator.[6] Fourth, silicon is extremely abundant in the Earth's surface allowing for cheaper acquisition of the material. Fifth, the development of the integrated circuit in 1960 allowed manufacturing of many interconnected devices on a single surface of silicon paving the way for the modern computer chip.[7]

The advent of silicon as the semiconducting material of choice and the integrated circuit gave rise to an ever increasing demand for increased computing power. This demand for more computing power requires manufacturers to continually increase the number of transistors on a single silicon chip. The need to produce silicon chips at lower

prices further pushes manufacturers to reduce the size of the transistor, allowing for more transistors per unit area. This drive for reducing the size of the transistor gave rise to what has become known as Moore's Law.

In 1965, a cofounder of Intel, Gordon Moore, observed that in response to this demand the silicon electronics industry doubled the number of devices per chip every 18 months.[8] The doubling of devices per chip was managed by scaling devices, increasing the chip size, and ever more inventive chip designs to utilize space more efficiently. Gordon Moore's observation has since become prophetic as the semiconductor industry has maintained this steady pace of innovation for the last 50 years as shown in Figure 1.

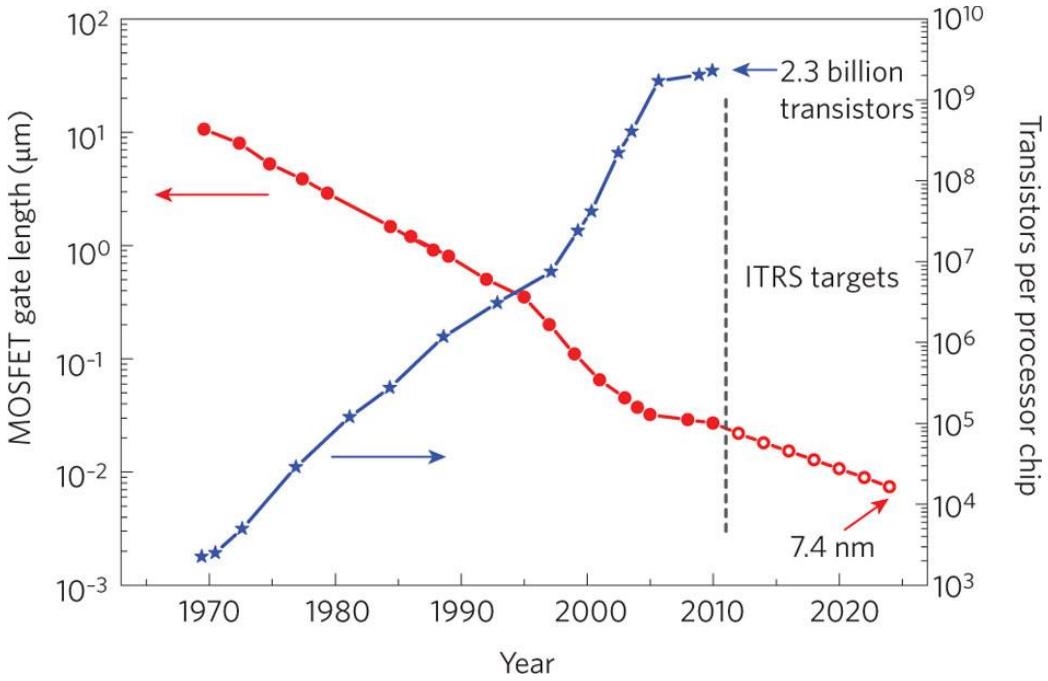

Figure 1 Evolution of the gate length of commercial MOSFETs (filled red circles) and projected targets (open red circles). As a result of reduced size, the transistor count per chip (blue stars) has increased. Reprinted by permission from Macmillan Publishers Ltd: *Nature Nanotechnology* 5, 487-496 (2010).[9]

Maintaining Moore's law has not come without challenges. In the 1970's, Moore's law was said to be reaching its end due to the limitations imposed by contact lithography and the wavelength of visible light.[10] In response, Perkin-Elmer developed the projection scanner in 1973.[11] Rather than relying on direct contact to achieve the patterning, a lens is used to project an image of the pattern. Initial designs projected a 1:1 scale image of the pattern. Five years later with the introduction of the stepper, photolithography was able to be performed on sections of the wafer by projecting a mask image on one area then moving to the next as opposed to the entire wafer at once. The combination of the stepper and projection lithography allowed the semiconductor industry to project mask patterns at much higher resolutions enabling projected patterns to be smaller than the physical mask used to create them. The limitations of using visible light for patterning were overcome in 1982, with the development of photoresists sensitive to ultra-violet light at IBM.[12] The development of new photoresists and a switch from mercury lamps to ultra violet excimer lasers allowed the semiconductor industry to continue downscaling.

In the mid 80's, 500 nm was proclaimed the ultimate scaling limit as source/drain resistance increased to non-feasible values. In response, the semiconductor industry developed silicides with the first silicide made out of tungsten reducing the resistivity by an order of magnitude.[13] The introduction of silicides marked the first limitation overcome by a change in material used for the transistor. A decade later and 100 nm is proclaimed as the ultimate scaling limit due to reduced mobilities in the silicon with scaling and reduced performance of the aluminum interconnects. This limitation was overcome by the introduction of germanium in the silicon channel and the replacement of

aluminum interconnects with copper.[14, 15] The introduction of germanium strains the silicon, increasing the mobility by up to 25% while using copper resulted in a reduction in the resistivity of the interconnect by half.

By 2004 the industry had yet again reached a fundamental limit on the technology used to pattern devices leading to the development of immersion lithography which allows patterning up to an order of magnitude smaller than the wavelength of light used.[16] Yet another limitation was reached by 2007 at the 50 nm scale with the inability of the silicon dioxide to prevent gate tunneling at the dimensions needed. In response, Intel announced the use of hafnium oxide as the gate dielectric. The higher dielectric constant of hafnium allows thicker gate dielectrics while maintaining the same electric field in the channel. The thicker gate drastically reduced the gate leakage current allowing the continuation of downscaling of silicon based devices we see today.[17]

The semiconductor industry is facing another challenge in the continued downscaling of transistors and adherence to Moore's law. With transistors approaching dimensions of sub 10 nm, short channel effects and gate leakage can no longer be overcome with the material systems in use today.[18-20] The continued scaling of devices has resulted in leakage from tunneling currents through the oxide no longer being negligible,[21-24] reduced device reliability due to short channel effects,[25-30] and a substantial increase in power dissipation.[31, 32]

As the MOSFET is scaled to smaller dimensions, the magnitude of the electric field applied between the source and drain approaches the magnitude of the electric field applied at the gate causing short channel effects. This results in the gate no longer controlling the transistor behavior. This is further exacerbated by variability in the device

processing. As the device dimensions begin to approach single nanometers in size, a change of 1 nm in the device dimensions can significantly alter the device behavior.

Figure 2 shows threshold voltage as a function of gate length for a NMOSFET with a V_T = 0.65 V, doping concentration of 1x10^{18} cm^{-3}, 2 nm oxide thickness, and at 1 μm channel length as the NMOSFET approaches single nanometer channel lengths. The change in threshold voltage is calculated from equation 1.[33]

$$V_{Tnew} = V_T - \frac{qN_aW_{dm}r_j}{C_{ox}L}\left(\sqrt{1+2\frac{W_{dm}}{r_j}}-1\right) \quad (1)$$

Where V_{Tnew} is the reduced threshold voltage, V_T is the threshold voltage for an equivalent long channel device, q is the charge of an electron, N_a is the dopant concentration, W_{dm} is the depletion width which is a function of C_{ox} and N_a, and r_j is the implantation depth of the source and drain wells (20 nm as shown).

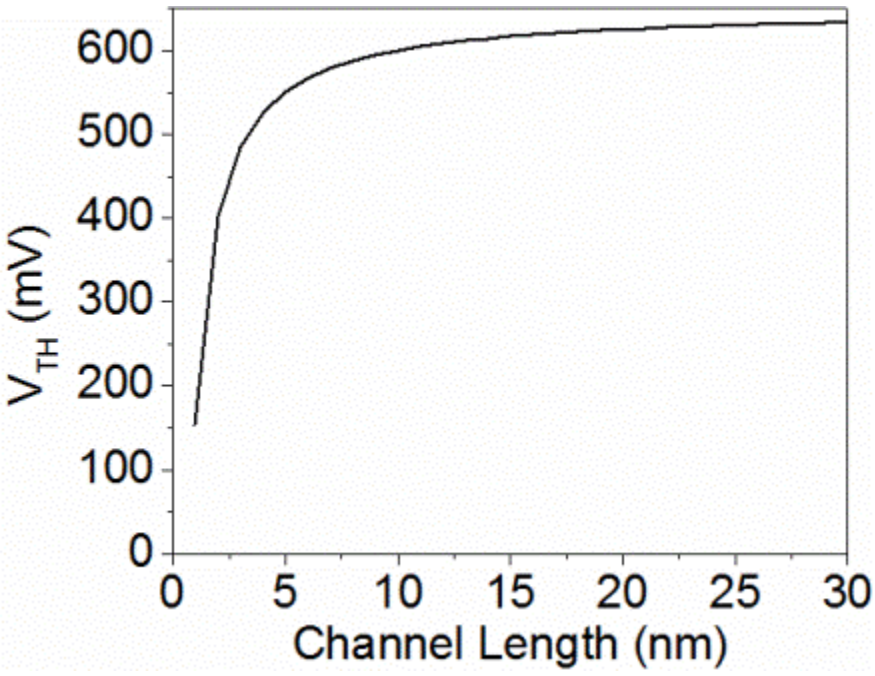

Figure 2 Threshold voltage of a MOSFET as a function of channel length.

Short channel effects currently limit the scalability of the Si MOSFET.[18, 19, 34] Short channel effects limit the scalability of the silicon transistor by making the methods used to reduce the impact of short channel effects prohibitively expensive to continue as the device scales.[19] These effects arise in the traditional MOSFET from the increasing electric field in the device channel as the device becomes smaller. Traditional methods for combating short channel effects include scaling of the oxide thickness, increasing the substrate donor concentration, and halo implanting.[18-20, 24, 34-36] Combating short channel effects becomes more difficult and expensive as scaling continues.

Despite significant efforts, solutions addressing the difficulties of continuing traditional scaling of the MOSFET have not been found. Even if solutions are found to address random dopant fluctuations and reduce device variations in patterning, the subthreshold swing of the traditional MOSFET cannot be scaled below 60 mV/decade at room temperature.[33, 37] Alternative methods for achieving a performance increase for digital logic applications are required. Two of the most promising methods currently being developed are high mobility channels and alternative transistor designs.[38-45] Graphene is a promising material for both methods of moving past the traditional Si based MOSFET.[46-50]

1.2 Physics of Graphene

Graphene is a two-dimensional material comprised of carbon atoms arranged in a honeycomb lattice. Theoretically discussed as early as 1947[51-53], with attempts to isolate a single layer of graphite in the form of ultra-thin graphite carried out as early as 1966[54], graphene is a promising material for future electronic applications. With the isolation of a single atomic layer of graphite using the "scotch tape method" in 2004[55], research into

the unique electrical properties of graphene and its future use in electronics has been researched heavily over the past decade.

Large efforts into graphene growth on the wafer scale have been carried out due to graphene's promise as a material for future electronics due to a number of unique qualities arising from the electronic structure and 2D nature of graphene. These qualities include mobilities as high as 10,000 $cm^2\ V^{-1}s^{-1}$ reported on SiO_2[56], mobilities in excess of 200,000 $cm^2V^{-1}s^{-1}$ for suspended graphene[57], and observations of the quantum hall effect near room temperature[56, 58]. Due to the unique properties of graphene, graphene is being researched for applications in a variety of fields including spintronics due to long spin injection lifetimes in graphene[59], gas sensors able to detect single gas molecules[60], nanoribbon interconnects with resistivity comparable to copper[61], ballistic transport devices due to large mean free paths and relativistic charge carriers[62], and RF applications due to the high mobility of graphene resulting in large cutoff frequencies.[63]

A two-dimensional allotrope of carbon with a bond distance of 1.42 Å, graphene is composed of two trigonal sub lattices, labelled A and B, which results in graphene having two atoms per unit cell, as seen in Figure 3.[64]

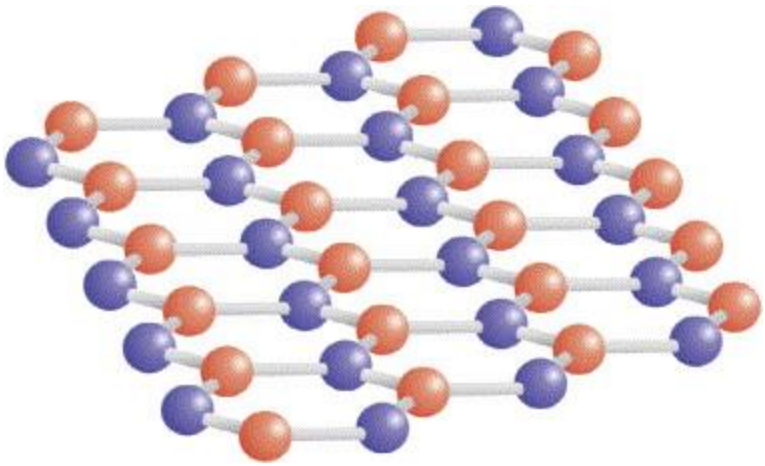

Figure 3 Graphene lattice showing the A and B sub lattice (blue and red respectively). Reprinted from Materials Today, Vol 10, M.I. Katsnelson, Graphene: Carbon in Two Dimensions, Pages 20-27, Copyright (2007), with permission from Elsevier .[64]

Graphene is comprised of sp^2 hybridized carbon atoms arranged in a hexagonal lattice formed by a σ bond from the hybridization of the $2s^2$ orbital and the $2p_x$ and $2p_y$ orbitals forming the in plane bonds. The out of plane $2p_z$ orbital is the only orbital involved in conduction within graphene, forming a π band with the neighboring carbon atoms.[65] The electronic structure of graphene arising from the hybridization of the orbitals and symmetry of the sub lattices can be described by a tight-binding approximation and gives two points in which band crossing occurs in the Brillouin zone, labelled K and K', around which the dispersion relation is linear, as seen in Figure 4.[64]

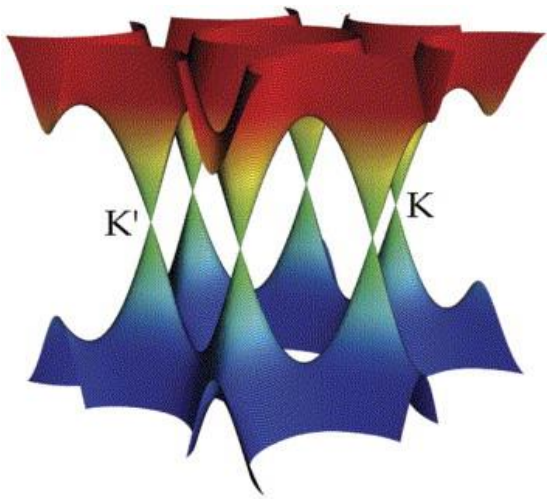

Figure 4 Graphene Brillouin zone showing the Dirac points at the K and K' points. The linear dispersion and touching of the valence and conduction band can be seen at the K points. Reprinted from Materials Today, Vol 10, M.I. Katsnelson, Graphene: Carbon in Two Dimensions, Pages 20-27, Copyright (2007), with permission from Elsevier .[64]

The dispersion relation is given by

$$E(k) = \pm t\sqrt{3 + h_o(\vec{k})} \tag{2}$$

$$h_o(\vec{k}) = 2\cos(\sqrt{3}k_y a) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right) \tag{3}$$

Where t is the nearest neighbor interaction energy and a is the interatomic bond length with magnitudes of 2.9 eV and 1.42 Å respectively. The positive sign in the dispersion relation corresponds to the conduction band and the negative sign corresponds to the valence band.[64] Setting $E(\vec{k})$ to zero in the $E(k)$ dispersion relation results in six points in which the bands coincide on the Brillouin zone (K and K' points). The six points can be sub divided into two sets of three points separated by reciprocal lattice vectors as shown in Figure 5.

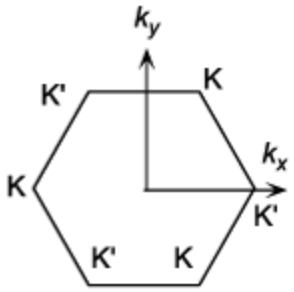

Figure 5 Graphene Brillouin zone depicting equivalent K and K' positions. Equivalent points are connected by reciprocal lattice vectors.

The lattice vectors for these points, also known as the Dirac points, are given by

$$\vec{K} = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right) \tag{4}$$

$$\overrightarrow{K'} = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right) \tag{5}$$

Around the Dirac points($within \sim \pm 1\ eV$), the dispersion relation can be represented in a simpler form as given by

$$E = h v_f \left|\vec{k}\right| \tag{6}$$

$$v_f = \frac{1}{\hbar}\left(\frac{3at}{2}\right) \tag{7}$$

Where v_f is the Fermi velocity, a is the atomic spacing of 1.42 Å, t is the nearest neighbor interaction energy of 2.9 eV. The density of states is given by

$$DOS = \frac{E}{2\pi\hbar^2 v_f^2} \tag{8}$$

The linear dispersion relation results in unique properties such as the vanishing of the density of states at the Dirac point and charge carriers behaving as massless Dirac fermions traveling at a Fermi velocity of 10^6 m/s.[66] The electric field effect can be used to induce charges into the graphene channel as well.[67] Depending on the applied field,

the Fermi level can be moved into the conduction or valence band, resulting in an ambipolar graphene channel. Under ideal circumstances, graphene would have a Fermi energy and density of states of zero ($E = 0$ in the DOS equation). Under real circumstances, graphene exhibits induced charge carriers from the underlying substrate, impurity charges introduced from the atmosphere or device processing, as well as thermally generated carriers. These induced charge carriers present without an electric field effectively result in graphene based devices which are always on. With a typical I_{on}/I_{off} ratio, the ratio of the measurable current in a device in the on state and off state respectively, of 5-10 (typically orders of magnitude larger for a silicon based transistor), novel device architectures are required for graphene to find an application in digital electronics.

1.3 Graphene Synthesis

1.3.1 Exfoliation

The exfoliation of a single layer of graphene was first reported by Novoselov and Geim in 2004[55] and resulted in the awarding of the Nobel Prize in 2010. Using what has become known as the scotch tape method, crystals of graphite are repeatedly peeled apart in order to thin the crystal and yield monolayer to few layer graphene. There are several sources of graphite used for the exfoliation method including highly oriented pyrolytic graphite (HOPG), Kish graphite, and natural graphite. HOPG and Kish graphite are synthetically formed graphite with typical domain sizes of ~10μm while naturally occurring graphite can have domains of several millimeters.

A single layer of graphene absorbs 2.3% of incident light. This makes a single layer of graphene unobservable by the naked eye. Exfoliated flakes of graphene are identified

using optical interference and Raman spectroscopy.[68, 69] A 300 nm thermal SiO2 has a violet-blue coloration. The addition of a graphene layer introduces interference of the light which shifts the coloration to a true blue. This shifting of color allows the identification of single to few layer graphene based off of the contrast.[68] Raman spectroscopy also allows the identification of single to few layer graphene due to the presence of unique Raman features of the graphene.[69]

While easy to produce and yielding exceptional quality graphene, exfoliated flakes are often too small for TEM, XPS, etc. The small size of the flakes and the random distribution disallows large scale fabrication of exfoliated devices.[70] Individual patterning of each flake is required which results in a large time commitment for fabricating exfoliated devices. For this reason, exfoliated graphene is commonly used for proof of concept and physics experiments where "perfect" graphene is a necessity. The stochastic nature of the exfoliated flakes makes exfoliated graphene unsuitable for manufacturing purposes.

1.3.2 Epitaxial Growth

An alternative method for graphene synthesis is the epitaxial growth of graphene on SiC. First reported in 2004[71], the epitaxial growth of graphene on SiC is formed by sublimating the Si out of 6H-SiC at ~1300 °C.[72, 73] An indeterminate number of graphene layers (controlled by time) are formed on the C face of the 6H-SiC while a self-limiting formation of graphene occurs on the Si face. While multiple layers form on the C face, the layers have been reported to be decoupled from each other and behave as individual layers of graphene. [74, 75]

Epitaxial growth of graphene results in large single crystalline sheets of graphene. Epitaxial growth of graphene can result in exceptional quality graphene with mobilities greater than 100,000 cm^2/Vs being reported.[76] While epitaxial growth from SiC does allow for large scale synthesis of graphene devices, the use of SiC for graphene growth would require a full paradigm shift in the electronics industry making SiC based graphene economically prohibitive for use in digital electronics.

1.3.3 Reduced Graphene Oxide

The third common method for producing graphene is reduced graphene oxide. Graphene oxide is an oxidized graphene product capable of being dispersed in an aqueous environment.[77-79] This dispersal into an aqueous environment allows graphene oxide to be cast onto a surface at ease by methods such as spin coating. After dispersing the graphene oxide flakes across the surface, the graphene oxide can be reduced to yield a conductive continuous film.[80-82]

Chemical reduction of graphene oxide is a common means of producing reduced graphene oxide. Hydrazine monohydrate is one of the most common reductants used due to a lack of side reactions with solvents typically used for graphene oxide dispersal.[83] The reduction from chemical methods is often incomplete as shown by the C 1s XPS spectra shown in Figure 6 which shows the presence of C-N, C-O, C=O, and C(O)O groups still present after chemical reduction.[84] These residual chemical groups attached to the graphene drastically change the electrical performance of the graphene. Currently, no simple pathway exists for the removal of these groups which reduces the usability of chemical reduction for the production of pristine graphene from graphene oxide.

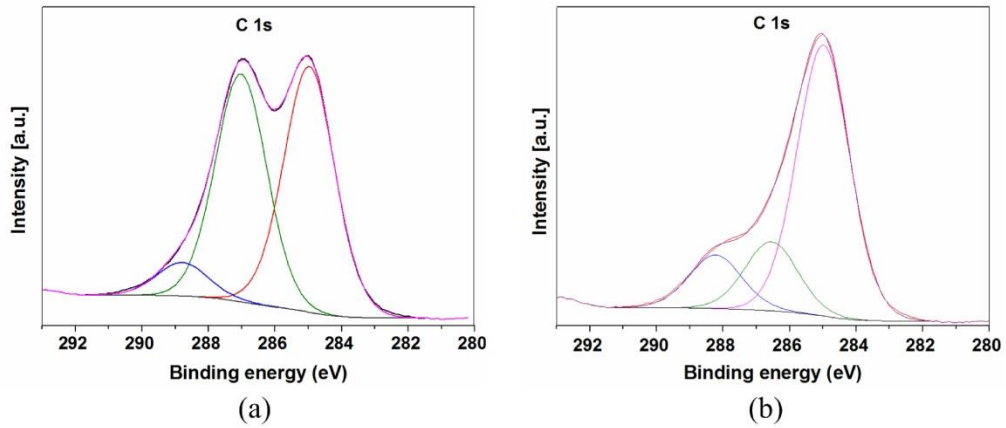

Figure 6 (A) C 1s XPS spectrum of graphene oxide. (B) C 1s XPS spectra after chemical reduction. Reprinted with permission from G. Sobon, *et al*. Optics Express, 20 (17), 19463-19473 (2012). Copyright (2012) The Optical Society.[84]

Thermal reduction is another common method for the reduction of graphene oxide. Graphene oxide heated to 1050 °C will produce carbon oxide species which leave the graphene oxide as carbon dioxide gas.[85] The gas generates pressure between the stacked layers aiding in the exfoliation of the layers.[86] One result of the thermal reduction of graphene oxide is a high degree of structural damage to the graphene. Up to 30% of the graphene oxide mass is lost during thermal reduction resulting in a porous graphene network.[87, 88] The increased defect density results in increased scattering centers and reduced conductivity of the reduced films compared to pristine graphene.

The final commonly used method for the reduction of graphene oxide is electrochemical reduction.[81] Graphene oxide is dispersed between two electrodes and linear sweep voltammetry in a buffer solution is used to reduce the film. The resultant films have conductivities comparable to pristine graphene and show negligible defect generation in the graphene films.[89-91] While effective at producing high quality graphene films, the reduction of graphene oxide by electrochemical reduction has not been shown

on a large scale. The lack of scalability for the electrochemical method precludes its use for high performance electronics.

1.3.4 Chemical Vapor Deposition

The most common method for large scale high quality graphene synthesis is chemical vapor deposition.[92-94] In this method, a metallic substrate is heated to ~1050 °C before introducing a carbon source. The s carbon source, in most cases methane, is cracked at the hot metal surface providing a source of activated carbon.[95] The growth method of the graphene is dependent upon the metal substrate used. For example, Cu and Ir substrates result in nucleation and growth of graphene while Ni, Co, and Ru substrates result in an absorption and precipitation process.[95-103] Cu is the most prevalent choice of substrate as it results in a self-limiting reaction at the surface of the Cu allowing for highly uniform large area monolayers of graphene.[104-109]

The transition metal synthesis substrate acts as a catalyst. Either the partially filled d-orbitals or the formation of intermediate compounds provide a pathway for the formation of graphene. Co, Ni, and Cu have progressively filled 3d shells suggesting progressively less reactive configurations.[110] Co and Ni provide intermediate compounds in the form of metastable carbide phases at high temperature while Cu forms only soft bonds by transferring charge from the π electrons in the sp^2 hybridized carbon to the empty 4s shell of the Cu. In a typical synthesis process,[111] Co and Ni result in multilayer graphene formation while Cu is limited to a monolayer of graphene on the surface.[111-113]

The Ni-C phase diagram is shown in Figure 7. At typical graphene growth temperatures of 800-1000°C, carbon forms a metastable solid solution with Ni. As the temperature decreases, the carbon solubility in the Ni decreases. This results in carbon

segregating out of the metastable Ni_3C phase to form Ni metal and graphene/graphite.[114] The carbon preferentially diffuses at the Ni grain boundaries leading to an increased graphene growth rate. This causes polycrystalline Ni to exhibit a large variance in the number of graphene layers grown across the Ni substrate.[111, 115] Control over the number of formed layers can be achieved by using a single crystalline synthesis substrate such that the diffusion rate of the carbon is homogeneous across the entire substrate.[116] The large lattice mismatch between graphene and Ni results in polycrystalline graphene formation. For substrates such as Co with a small lattice mismatch with the graphene, the synthesized graphene is in registry with the underlying substrate allowing for single crystalline graphene synthesis.[117] The growth process for Co and Fe is similar to the Ni growth process as predicted by the similarities in the metal-carbon phase diagrams.

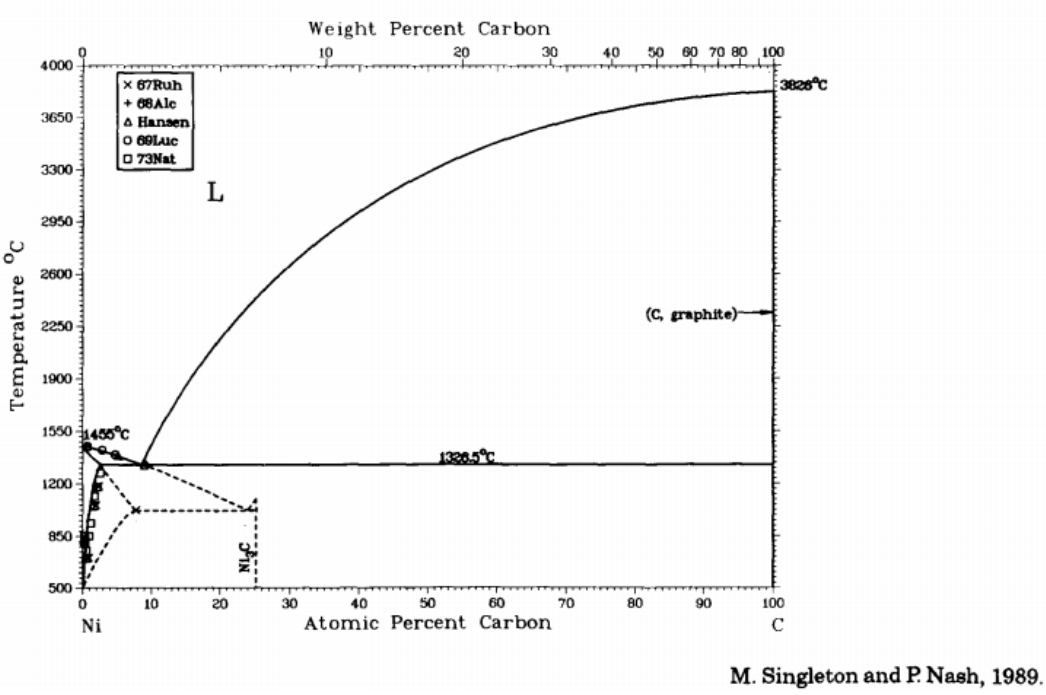

Figure 7 Ni-C (graphite) and metastable Ni-Ni_3C phase diagram. Reproduced from Bulletin of Alloy Phase Diagrams, The C-Ni (Carbon-Nickel) System, volume 10, 1989, pages 121-126, M. Singleton and P. Nash with permission of Springer.[114]

In contrast, the low solubility of carbon in Cu of 0.008% by weight and lack of carbide formation leads to a surface mediated growth of graphene on copper. Typically, methane gas is introduced over a heated copper substrate (~1000°C).[110, 113] The carbon precursor cracks upon contact with the catalytic substrate. Carbon diffuses across the surface of the copper and forms graphene islands at high energy sites (Cu grain boundaries, impurity atoms, defect sites, etc.) on the copper surface.[95, 118, 119] A schematic representation of the growth process is shown in Figure 8. As additional carbon is added, it either diffuses across the copper surface and attaches to a pre-existing graphene island or forms a new nucleation site and the hydrogen is desorbed. Eventually, the graphene islands coalesce into a single patchwork of graphene domains.[118-121] The growth of graphene stops after the Cu surface is completely covered. This results in predominantly single layer graphene (~95%) growth on copper.[122] The domain size of graphene on Cu can be controlled primarily by controlling the high energy states on the Cu surface, changing the pressure of the reactor, and changing the temperature of the reactor.

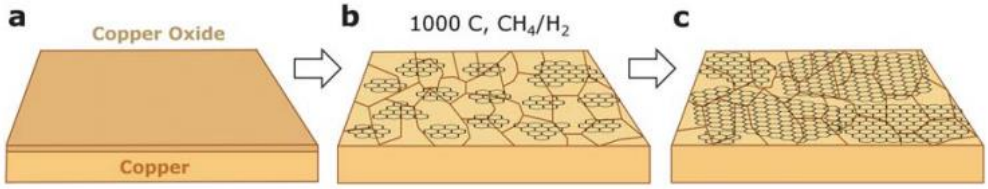

Figure 8 Schematic illustrating the three main stages of graphene growth on copper by CVD: (A) copper foil with native oxide; (B) the exposure of the copper foil to CH4/H2 atmosphere at 1000 C leading to the nucleation of graphene islands; (C) enlargement of the graphene flakes with different lattice orientations Reproduced from C. Mattevi *et al*. *J. Mater. Chem.* 21, 3324-3334 (2011) with permission of The Royal Society of Chemistry.[110]

The system background pressure and temperature play a critical role in determining the domain size of the synthesized graphene on copper.[112, 113, 123] The synthesis temperature and pressure impact the copper catalyst annealing, carbon diffusion on the copper surface, formation of stable graphene nuclei, and the graphene crystal growth. Figure 9 shows the impact of temperature on the graphene nucleation density/domain size at atmospheric pressure. As seen, the nucleation density is strongly influenced by the synthesis temperature. The nucleation density of graphene changes by 5 orders of magnitude across a temperature span of 130°C corresponding to an activation energy of ~ -9eV as shown in Figure 9C. The dependence of the graphene domain size on temperature is shown in Figure 9D. The activation energy for graphene crystal growth is found to be ~5 eV.[123]

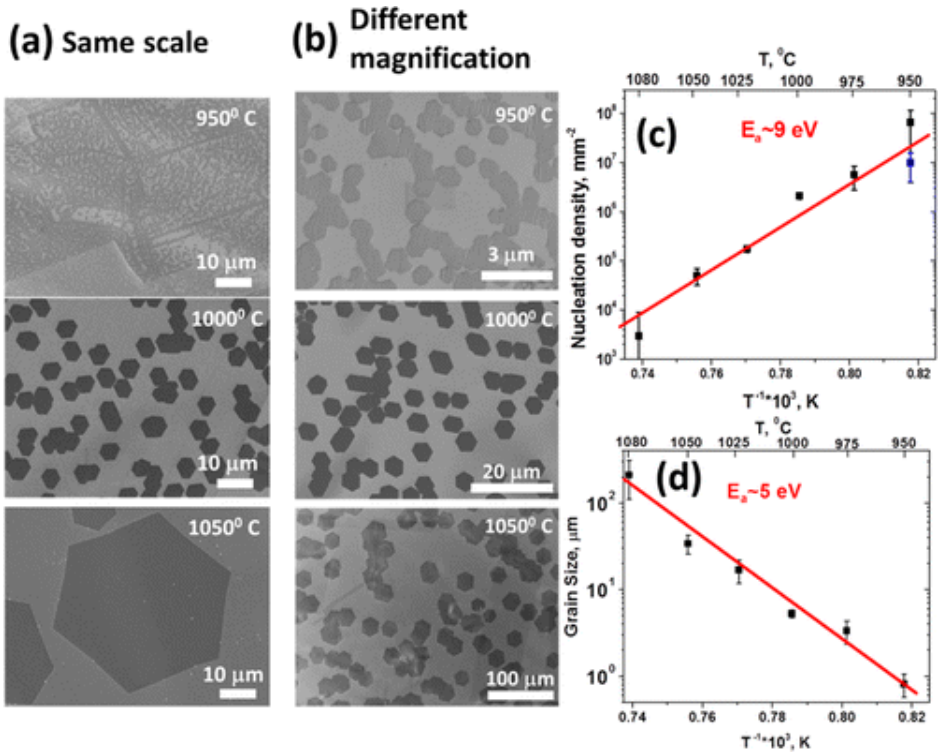

Figure 9 Temperature dependence of the nucleation density and graphene domain sizes for atmospheric pressure CVD: P_{H2}/P_{CH4} = 1800 (A) SEM images of graphene grains grown at different temperatures for constant partial pressures of H_2 (19 Torr) and CH_4 (10.5 mTorr). (B) Same as in A at different magnification. (C) Arrhenius plot for the nucleation density. Blue point shows nucleation density at 950°C for sample annealed at 1080°C. (D) Arrhenius plot for the grain size. Reprinted with permission from I. Vlassiouk *et al*. *The Journal of Physical Chemistry C*. 117, 18919-18926 (2013). Copyright (2013) American Chemical Society.[123]

Similar temperature trends are seen for low pressure (less than 500 mTorr) CVD synthesis of graphene. A strong temperature dependence with an activation energy of ~ -4 eV is found for low pressure CVD.[123] The nucleation density and grain size is found to be strongly dependent on the methane partial pressure. The graphene nucleation process is dependent on gas precursor adsorption, dehydrogenation of the carbon, diffusion of carbon on the surface, and formation of graphene nuclei which is in competition with the carbon desorption process.[110, 112, 123]

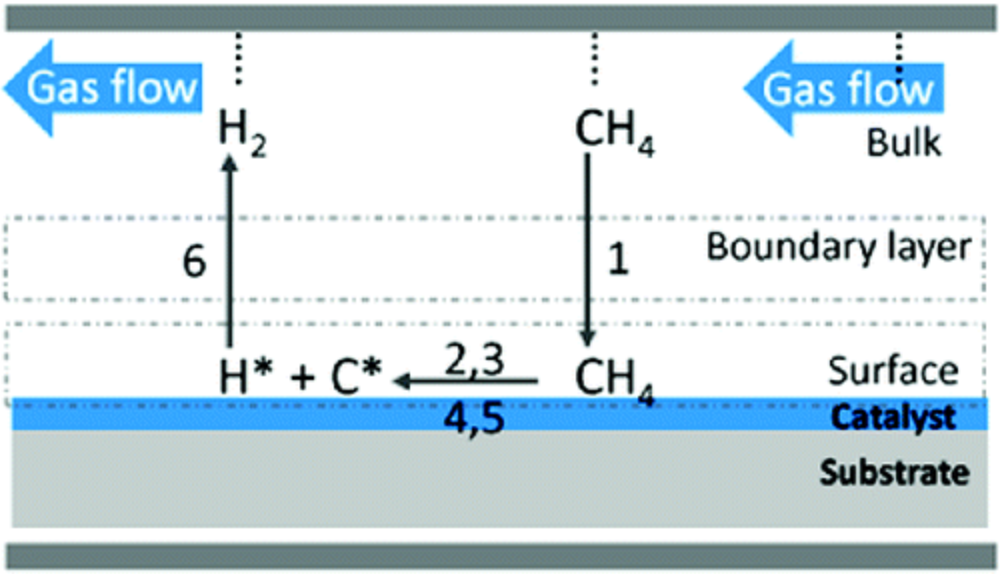

Figure 10 Schematic representation of the graphene synthesis process on Cu. Reprinted with permission from S. Bhaviripudi *et al*. *Nano Letters*. 10, 4128-4133 (2010) Copyright (2010) American Chemical Society.[112]

As shown in Figure 10, the gas flow in a graphene CVD process creates a boundary layer above the surface of the catalytic substrate. The carbon precursor introduced in the main gas flow must diffuse across the boundary layer, attach to the surface of the copper, diffuse across the surface of the copper, and attach/form a graphene nucleation site.[110, 112, 123, 124] After the activated carbon attaches to the graphene lattice, the hydrogen must desorb from the surface and diffuse back through the boundary layer. Hydrogen which does not diffuse back across the boundary layer (or diffuses to the substrate surface again) can react with carbon species on the surface to reform Volatile C_xH_y gas species. This synthesis process of graphene can ultimately be controlled by (i) the flux across the boundary layer or (ii) the flux across the surface of the catalytic substrate. The equations describing these fluxes are shown in equation 9 and 10.[112]

$$F_{ms} = \frac{D_g}{\delta}\left(C_g - C_s\right) \quad (9)$$

$$F_{sr} = K_s C_s \quad (10)$$

Where F_{ms} is the flux across the boundary layer, F_{sr} is the flux at the substrate surface, D_g is the gas diffusion coefficient, δ is the thickness of the boundary layer, K_s is the surface reaction constant, C_g is the concentration of the carbon source in the gas flow, and C_s is the concentration of active carbon at the substrate surface. At steady state, the mass transport across the boundary layer is equal to the consumption of active carbon at the substrate surface. Setting equation 9 equal to equation 10 and eliminating C_s gives equation 11 where F_{tot} is the steady state total flux.

$$F_{tot} = \left[\frac{K_s D_g}{\delta\left(K_s + \frac{D_g}{\delta}\right)}\right] C_g \quad (11)$$

From this equation it can be seen that there are three possible synthesis regimes for graphene. The first regime, $D_g/\delta >> K_s$ results in a surface controlled reaction.[110, 112, 113, 123, 125] When $D_g/\delta << K_s$, mass transport through the boundary layer is limiting and multiple graphene layers can form.[126, 127] When $D_g/\delta \sim K_s$ a mixed regime occurs. For typically graphene synthesis at atmospheric, $D_g/\delta << K_s$ resulting in a mass transport limited synthesis process. In this regime, the geometric effects of the gas flow and chamber design strongly influence the graphene synthesis process.[112] A variation in the thickness of the boundary layer results in a reduction in the active carbon species concentration at the surface. As gas transport through the boundary layer is more difficult in this regime, it is also more difficult for hydrogen species to leave the substrate surface after carbon adsorption. The hydrogen concentration at the substrate surface will reattach to the carbon species effectively etching the formed graphene. The reduced concentration of active carbon and increased hydrogen etching result in a smaller critical nuclei size.

This results in an increase in nucleation density and reduction in grain size for graphene growth at atmospheric pressure.

Early reports of graphene on copper showed reduced electrical performance compared to exfoliated graphene.[95, 119, 128] The reduced electrical performance was due to smaller domain sizes, wrinkles, contamination, etc. More recent reports of graphene growth show that the domain size can be controlled by controlling the nucleation density on the copper foil.[104-106, 129] Step edges created in the copper rolling process, contamination, and defect sites provide high energy sites for the nucleation of graphene. By treating the copper foil in acetic acid prior to growth, step edges can be reduced and surface contaminants removed. Introducing hydrogen annealing of the copper foil prior to growth removes step edges and defects by restructuring the surface of the copper foil. Introducing oxygen prior to the growth binds oxygen to the defect sites and reduces the nucleation density of the graphene. By incorporating these various methods, high quality graphene of variable grain size can be synthesized.[104-106]

Low pressure CVD growth of graphene on copper foils is the growth method used for the synthesis of graphene used in this study. A complex processing and integration scheme utilizing standard CMOS processes is used in fabricating the graphene based devices and only large-area synthesized materials are used.

1.4 Current status and limitations

1.4.1 Single Layer Graphene

Significant efforts have been made in creating FETs to replace Si utilizing single layer graphene. Research efforts into graphene FETs has been motivated by the

scalability of graphene to nanometer sizes, potential for ballistic transport, linear current-voltage characteristics, and high current densities.[55]

In order to be a viable replacement for the Si MOSFET in digital electronics, future replacement technologies need to offer switching ratios between 10^4 and 10^7, n- and p-channel FETs with symmetrical threshold voltages, and low static power dissipation.[9, 18, 130, 131] Graphene is a gapless semimetal which means devices with channels made of graphene cannot be turned off. The switching ratio of a single layer graphene transistor is ~10.[46, 119, 128, 132-134] This is well below the minimum switching ratio of 10^4 needed to compete with Si based MOSFETs.

Significant efforts have been made to introduce a bandgap into graphene in order to increase the switching ratio. These efforts can be classified into three categories: (i) graphene nanoribbons [135, 136] (ii) functionalization [137-140] (iii) strain engineering.[141-145] The most promising method is currently the fabrication of graphene nanoribbons.

As a graphene channel is reduced to widths below 20 nm, a bandgap greater than 200 meV is formed that is inversely proportional to the width of the ribbon. Nanoribbons with widths down to 2 nm have been reported with a switching ratio of 10^6.[146, 147] While promising, real devices will have some degree of rough edges and widths which will cause the bandgap to change along the length of the device.[148] The edge roughness further impacts the variability in graphene nanoribbons as graphene nanoribbons of similar design but slightly different edge states can have significant differences in electronic behavior.[9, 149]

In order for graphene single layers to be a viable replacement for Si, very narrow nanoribbons with atomically smooth edges will be needed. Reducing the edge roughness

of the graphene nanoribbon will be a significant challenge for modern semiconductor fabrication processes. A perfect edge state of the graphene nanoribbon may not work either. The valence and conduction band of the graphene becomes more parabolic as the bandgap increases. The effective mass of the carriers increases as the bands become more parabolic and the mobility is reduced. By opening a bandgap in the graphene, the material properties that make graphene promising (ultra-high mobility and massless carriers) begin to diminish or disappear. If a bandgap of 1.1 eV similar to Si were introduced into graphene, the graphene mobility would be lower than the mobility of Si.[150] While the scalability of graphene nanoribbons has been shown to be superior to traditional MOSFETs, it has not be determined if the improved scalability will offset the reduced mobilities of the graphene nanoribbon.

1.4.2 Bilayer Graphene

A bandgap can be introduced by application of an electric field when two graphene layers have a Bernal stacking arrangement.[151] In the Bernal stacking arrangement, the second graphene layer is offset from the first layer such that half of the carbon atoms are located above the atoms of the first layer and the other half lie in the center of the hexagon of the first layer.[152] The electrostatic control of a bilayer graphene FET has been reported. By using a dual gated structure, the Fermi level can be controlled electrostatically and a non-zero bandgap can be opened.[153]

Bilayer graphene in its natural state is a gapless semiconductor as seen in Figure 11D. By using a dual gated structure as shown in Figure 10A-B, two electrostatic effects can be induced which are dependent on the two induced electric fields shown in Figure 10C. The difference between the top and bottom electrical displacement fields leads to a

shifting of the Fermi energy. The average of the two fields breaks the inversion symmetry and opens a bandgap as shown in Figure 11D. By applying voltages to the top and bottom gate such that the net difference in the fields is 0, the bandgap of the bilayer graphene FET can be varied up to 250 meV without changing the Fermi level of the graphene.[153]

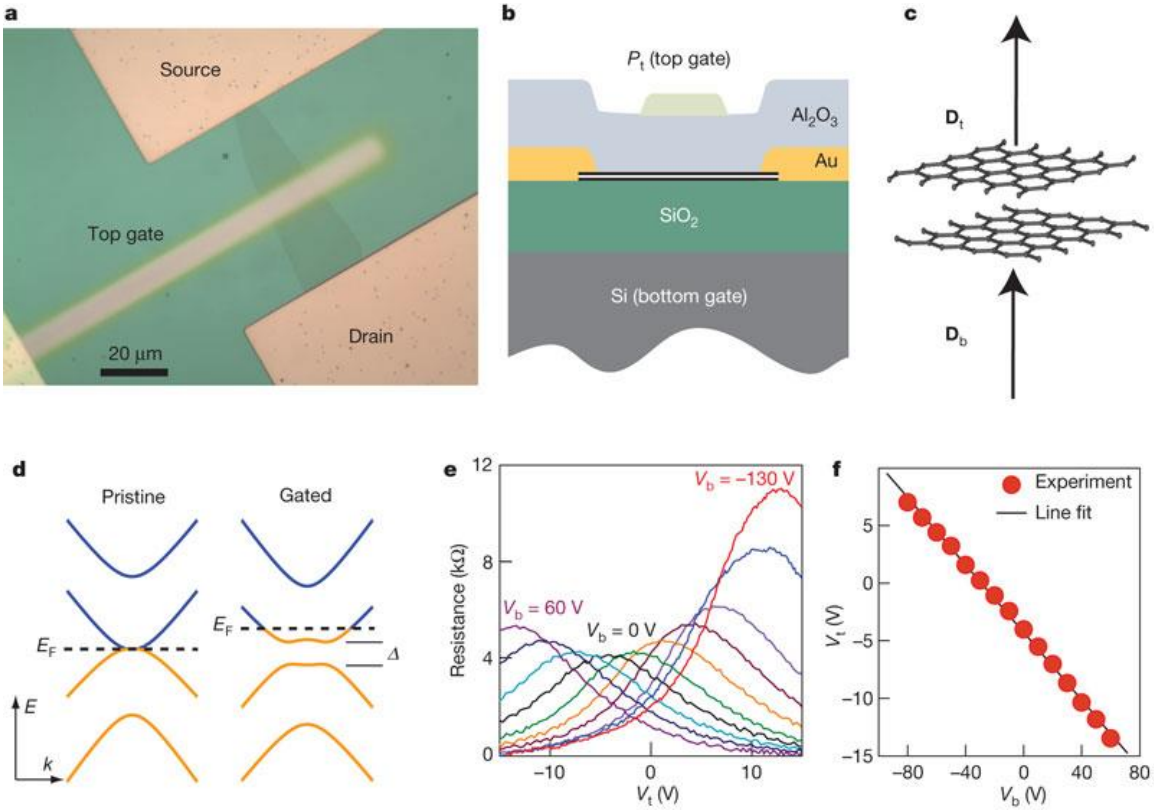

Figure 11 (A) Optical microscopy image of the bilayer device (top view). (B) Illustration of a cross-sectional side view of the gated device. (C) Sketch showing how gating of the bilayer induces top (Dt) and bottom (Db) electrical displacement fields. (D) Left, the electronic structure of a pristine bilayer has zero bandgap. (k denotes the wave vector.) Right, upon gating, the displacement fields induce a non-zero bandgap Δand a shift of the Fermi energy EF. (E) Graphene electrical resistance as a function of top gate voltage Vt at different fixed bottom gate voltages Vb. The traces are taken with 20 V steps in Vb from 60 V to -100 V and at Vb = -130 V. The resistance peak in each curve corresponds to the CNP (δD = 0) for a given Vb. (F) The linear relation between top and bottom gate voltages that results in bilayer CNPs. Reprinted by permission from Macmillan Publishers Ltd: Y.Zhang *et al*. *Nature*. 459, 820-823 (2009) copyright (2009).[153]

The report for the dual gated control of the bilayer graphene bandgap was reported in 2009. Since then, no significant advancements have been made. The largest switching ratios achieved for bilayer FETs are only ~100, much lower than the 10^4 minimum of conventional MOSFETs. This limits the viability of bilayer graphene for digital logic applications. Furthermore, bilayer graphene structures have been predominantly fabricated from exfoliated graphene. While some reports of Bernal stacked graphene have been reported by CVD growth, a reliable scalable synthesis method for Bernal stacked graphene remains elusive.[154, 155]

1.4.3 Vertical Heterostructures for Tunneling Devices

One subset of graphene devices proposed for digital logic applications are the tunneling field effect transistors (TFETs). TFETs can either be fabricated in a lateral planar geometry as in a traditional MOSFET or in a vertically stacked structure as shown in Figure 12.[156] Previous reports of lateral TFETs have shown to be incapable of providing large enough on currents.[157, 158] The current in a TFET is proportional to the active tunneling area in the device. For a scaled lateral TFET, the cross sectional area of the device limits the maximum current. As the length of the active area is larger than the thickness, a vertical geometry provides a relatively larger tunneling current compared to a lateral geometry due to the increased tunneling area.[159] Graphene based vertical TFETs incorporate a graphene/insulator/graphene junction where a potential is applied across the junction resulting in charge carriers from one graphene sheet tunneling across the insulating layer to the other graphene sheet. Due to the electronic structure of graphene, the TFETs using graphene layers as the source of the charge carriers can exhibit unique

electronic characteristics. Several vertical tunneling based devices have been proposed to take advantage of the electronic structure of graphene.

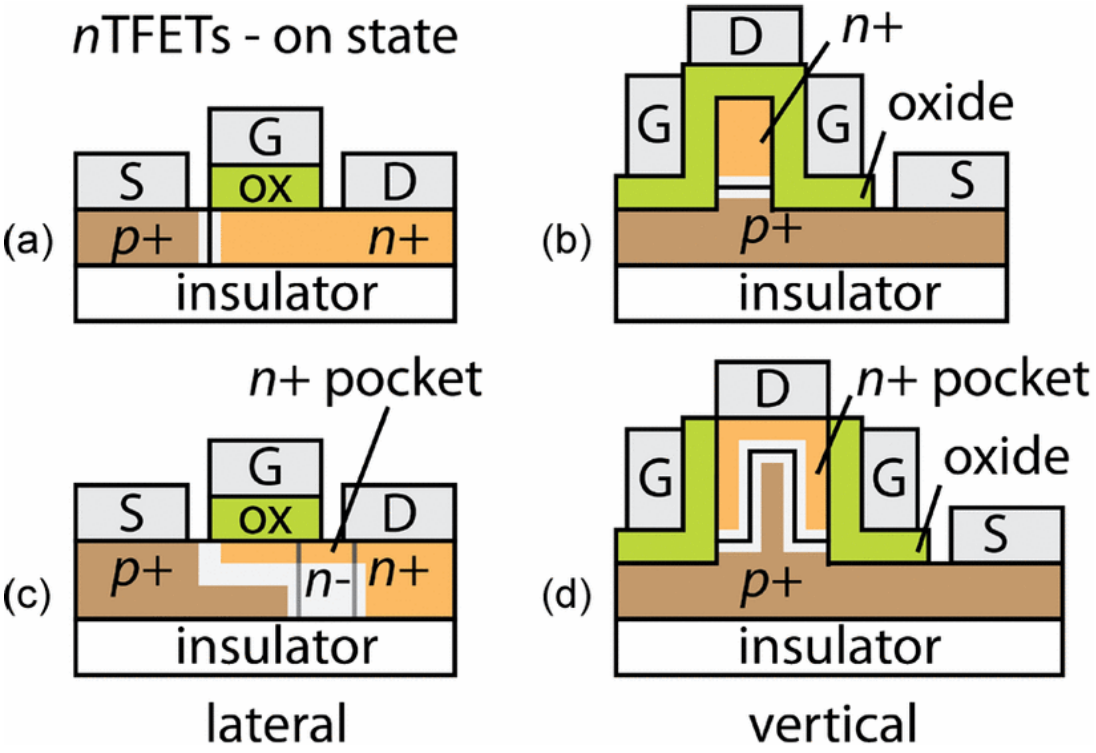

Figure 12 Two approaches for n TFETs. The upper row shows (A) single-gate lateral and (B) double-gate vertical structures in which the gate field originates from the surface, perpendicular to the orientation of the tunnel junction internal field. The lower row n TFETs have an n+ pocket under the gate in a (C) lateral and (D) vertical geometry. The pocket acts to increase the area of the tunnel junction and aligns the tunnel junction internal field with the gate field to lower the subthreshold swing. Copyright (2010) IEEE. Reprinted, with permission, from A.C. Seabaugh, Q. Zhang, Low-Voltage Tunnel Transistors for Beyond CMOS Logic, Proceedings of the IEEE, Dec. 2010.[156]

One such device proposed is the bilayer pseudospin field effect transistor (BiSFET) shown in Figure 13.

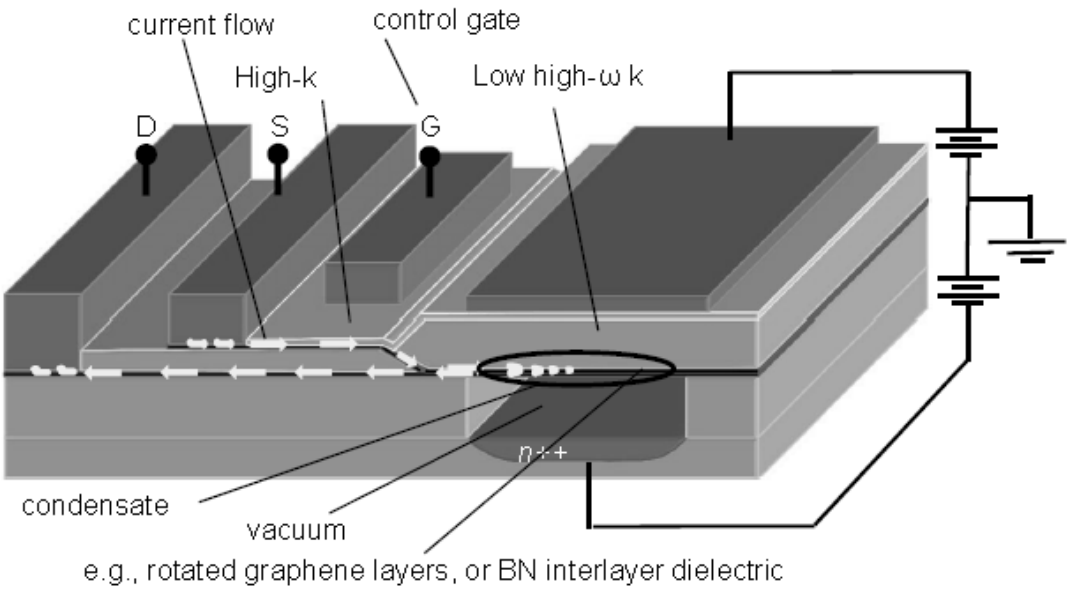

Figure 13 BisFET structure. Decoupled graphene layers oppositely doped (n and p type) by the source and drain contacts can generate a Bose-Einstein condensate when close enough and properly biased. Reproduced with permission from *ECS Transactions*, **45**, (4) 3-14 (2012). Copyright 2012, The Electrochemical Society[160]

The BiSFET is based off of the formation of a Bose-Einstein condensate, a state of matter predicted by Einstein and Bose in which the wave functions of all particles in the system (behaving as bosons) collapse into a single quantum state with overlapping wave functions.[160] The Bose-Einstein condensate has been experimentally shown to exist in other systems in temperatures ranging from μK to nK.[161, 162] In graphene, the Bose-Einstein condensate has been theoretically predicted in temperatures approaching 300K.[163] The BiSFET is made from two independently contacted graphene monolayers separated by a thin dielectric. The top and bottom gates allow for one graphene sheet to be n type doped while the other is p type doped. By applying an external field via the control gate, the opposite charge carriers in the two graphene sheets can form a condensate, greatly reducing the tunneling resistance between the two layers. This results

in a switch like behavior in which all of the charge carriers in the graphene sheets can be moved from one sheet to the other with the application of an external field.[163]

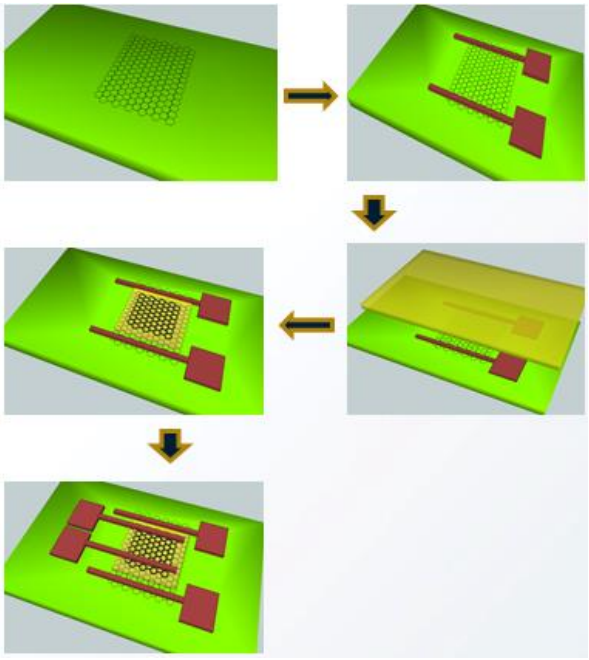

Figure 14 Process flow and final device structure for the fabrication of the SymFET architecture. First a graphene monolayer is transferred to the substrate of choice and patterned. Metal contacts for the first layer are deposited followed by the deposition of the tunneling barrier. The second graphene layer is deposited, patterned, and independently contacted.

Another proposed device for digital logic application is the SymFET shown in Figure 14 and 15A. The SymFET is a tunneling field effect transistor utilizing single-particle direct tunneling as a means for operation.[50] Using two independently contacted graphene layers separated by a dielectric, one graphene layer can be n type doped while the other is p type doped. The tunneling current between the two graphene sheets can be modulated using an external electrical field. Due to the linear dispersion relation in graphene, when the Dirac point of the graphene layers is not aligned, only a small number of carriers

satisfy momentum conservation and can tunnel from one sheet to the next. Shown in figure 6b-d, there is a large peak in the current resulting in negative differential resistance in the SymFET structure when the Dirac points of the two graphene sheets align allowing for a large number of carriers to satisfy momentum conservation and tunnel through the tunneling barrier.[164]

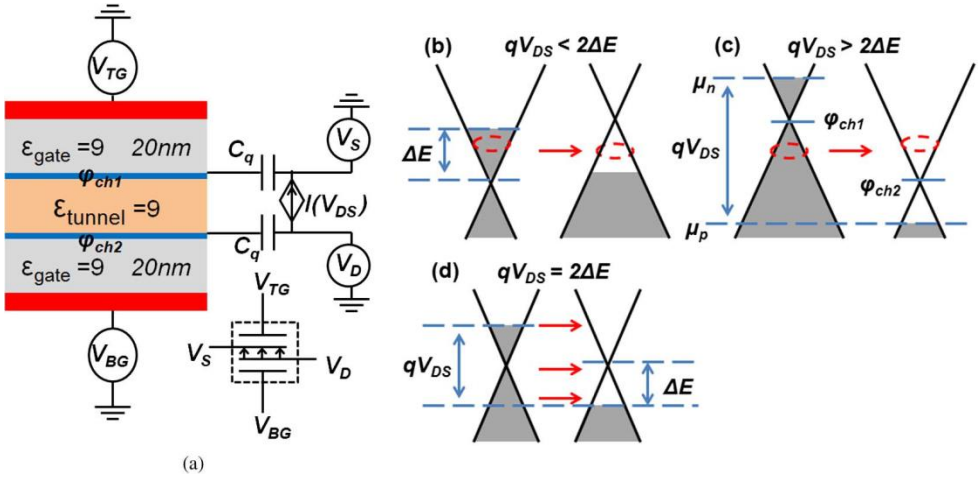

Figure 15 (A) SymFET device architecture and operation. Two graphene sheets (blue) separated by an interlayer dielectric with a potential placed between the sheets. The dopant level of the sheets is modulated by their respective gates and the potential between the sheets aligns the Dirac point. (B) When the potential applied is less than the energy difference between the graphene Fermi levels, only a small number of carriers can conserve momentum and tunnel through the barrier. (C) When the potential applied is greater than the energy difference. Only a small number of carriers can satisfy momentum conservation. (D) When the potential equals the energy difference every carrier in the energy states between the Fermi levels of the two graphene sheets can obey momentum conservation and tunnel through the barrier. Copyright (2013) IEEE. Reprinted, with permission, from P. Zhao, R.M. Feenstra, G. Gu, D. Jena, SymFET: A Proposed Symmetric Graphene Tunneling Field-Effect Transistor, IEEE Transactions on Electron Devices, March . 2013.[50]

This negative differential resistance (NDR) and device operation has been experimentally shown using exfoliated graphene sheets separated by a hexagonal boron nitride (hBN) layer as seen in Figure 16A and 16B.[165]

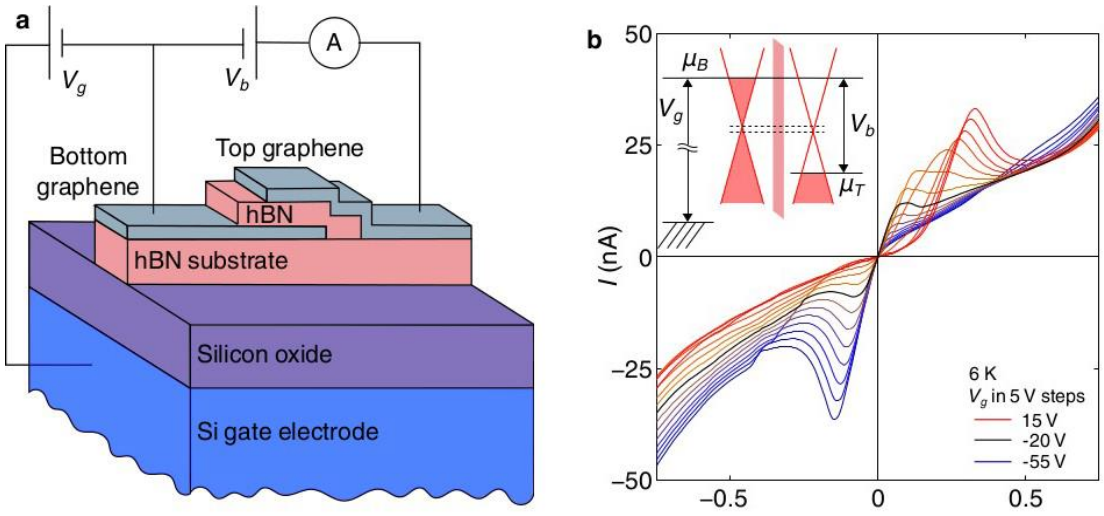

Figure 16 (A) Device structure exhibiting negative differential resistance. Two independently contacted graphene sheets separated by an hBN tunneling barrier. The substrate acts as a gate to modulate the Fermi level of the bottom graphene sheet. (B) Id-Vd curve at various back gate voltages showing the NDR of these devices. NDR was shown at temperatures of 6K to 300K. Reproduced with permission from L. Britnell *et al*. *Nature Communications*. 4, 1794 (2013). [165]

The presence of NDR using exfoliated graphene and hBN serves as a proof of concept for the device architecture. Future work will need to be done utilizing scalable processes such as CVD grown graphene/hBN.

One common trait between the two presented structures for digital logic is their reliance on well-ordered materials. For both the BiSFET and SymFET, the device operation is greatly influenced by the presence of disorder in the system. In the case of the BiSFET, disorder quenches the formation of the Bose-Einstein condensate.[166] In the

case of the SymFET, disorder can result in reduced tunneling currents and an unobservable negative differential resistance.[50] For both structures, disorder can arise from the materials used in the system.

1.5 Sources of materials disorder

1.5.1 Processing Induced Disorder

The most obvious source of disorder in the graphene films arises from the processing of the graphene films to be used in these devices. During the processing of devices, graphene is typically exposed to a variety of chemicals which have been shown to be difficult to remove, such as poly (methyl methacrylate) (PMMA) and the photoresists used in standard photolithography processes.[167-169] A wide variety of techniques have been developed for removal of these residues with varying degrees of success. The most common method used in the removal of residues is thermal decomposition of the contaminants.[132, 170, 171] Thermal decomposition has been studied in ultra-high vacuum, atmospheric conditions, forming gas conditions, and under an inert atmosphere. Atmospheric, forming gas, and inert atmosphere conditions have been shown to be ineffective at completely removing residues from the graphene channel while ultra-high vacuum annealing has been shown to return graphene to its intrinsic state.[132, 172] Recently, concerns on the effects of thermal decomposition have been raised. Reports of thermal decomposition resulting in a closer bond between graphene and the underlying substrate have been presented.[172, 173] The shortened bond distance results in increased phonon scattering from the underlying substrate, resulting in more disorder introduced into the system. Further concerns with thermal decomposition involve scission of the

polymers used during processing and the reactivity of the radicals formed from polymer scission reacting with the defect sites of the graphene.[172, 173]

Electric current annealing of fabricated devices is another common method of residue removal. Effective at the individual device level, electric current annealing is inadequate for wafer scale cleaning.[174] While systematic studies of these cleaning methods as they effect individual graphene layers has been performed, little information is available to describe how these cleaning methods impact the remainder of the device architecture. Alternative cleaning methods that do not degrade the graphene performance are required.

1.5.2 Physical Structure Induced Disorder

Another source of disorder arising from the graphene grown utilizing CVD processes are the grain boundaries formed due to the nucleation and growth process of the graphene domains.[92, 95, 122, 128, 175, 176] Transport across the grain boundaries is slightly reduced within the graphene layer.[177-181] The varying size of the graphene domains also has an additional effect beyond the introduction of the grain boundaries themselves. For two polycrystalline sheets of graphene, there will be a random distribution of orientations between the two layers for operation in the SymFET and BiSFET. This random distribution of orientations will result in varying degrees of interaction between the two layers for the BiSFET and will result in greater dispersion in the negative differential peak position of the SymFET as well as reduce the overall tunneling current of the device.[160]

A wafer scale method for the mapping of the orientation on a wafer scale has been proposed in which Raman spectroscopy is used in the determination of the orientation

between layers.[182] Raman spectroscopy is a technique in which a photon is absorbed by the specimen of interest, promoting an electron.[69] The electron can then undergo a variety of pathways to relax back into the unexcited state, emitting a photon in the process. The energy of the emitted photon is dependent on the relaxation pathway followed, which is in turn dependent on the electronic structure being probed. By measuring the energy of the emitted photon, detailed information pertaining to the electronic structure of the specimen can be derived. In the case of graphene, three dominant phonon modes are typically used for characterization. The first of these phonon modes is the D peak. The D peak can be a double resonance or single resonance process, where the resonance refers to the number of phonon interactions in the pathway. Another aspect of the D peak is the requirement of a defect in order for the transition to occur. In intrinsic graphene, the D peak occurs at ~1350 cm^{-1}.[69, 183, 184] The second peak in the graphene Raman spectrum is the G peak. The G peak is a single resonance process and results from the excitation and relaxation of an electron in which only a single point in K-space is involved. The G peak occurs at ~1580 cm^{-1}.[69, 183, 184] The Third peak in the graphene Raman spectrum is the 2D peak. The 2D peak is a double resonance process in which two opposite wave vectors are involved. The 2D peak is the overtone of the D peak, but due to the involvement of two opposite wave vectors, no defects are required for the presence of the 2D peak. The 2D peak occurs at ~2700 cm^{-1}.[69, 183, 184] A schematic of the relaxation pathways associated with each Raman peak can be seen in Figure 17.

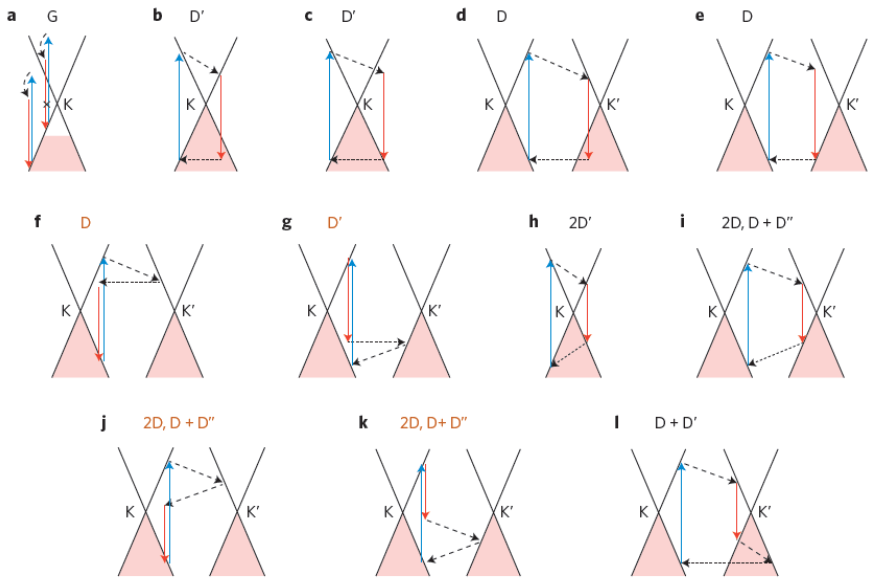

Figure 17 Raman modes of graphene. The prominent peaks in graphene are the G, D, and 2D peaks generated by Raman modes a, d, e, f, i, j, k, and l. Gold labels represent minimal contributions to the Raman signal. The D', 2D', and D'' peaks are low intensity Raman peaks which are not typically used in characterizing graphene via Raman spectroscopy. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology Vol 8, Issue 4, Pages 235-246, copyright (2013).[183]

A detailed analysis of the 2D peak position, Full width half max (FWHM), and relative intensity to a single layer of graphene can be used to determine the distribution of orientations, Figure 18 depicts a "misoriented" bilayer within graphene devices.

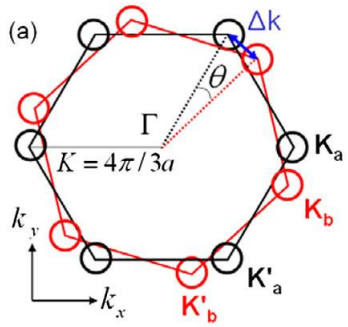

Figure 18 Two graphene sheets depicted by their Brillouin zones. An oriented graphene layer would fall directly on top of the previous layer. The misorientation angle as measured by Raman is the rotation of the Dirac points from the center position. Reprinted with permission K. Kim *et al*, Physical Review Letters, Volume 108, 246103 (2012). Copyright (2012) by the American Physical Society.[182]

As can be seen in Figure 19D, the area of the 2D peak for a graphene bilayer can be compared to the 2D peak area of a single layer allowing for orientations between 10 and 20 degrees to be mapped. The 2D area can also be used to determine an orientation less than 10 degrees or more than 20 degrees. Orientations less than 10 degrees can then be determined by analyzing the FWHM and blue shift of the 2D peak as seen in Figure 19B and 19C.[182]

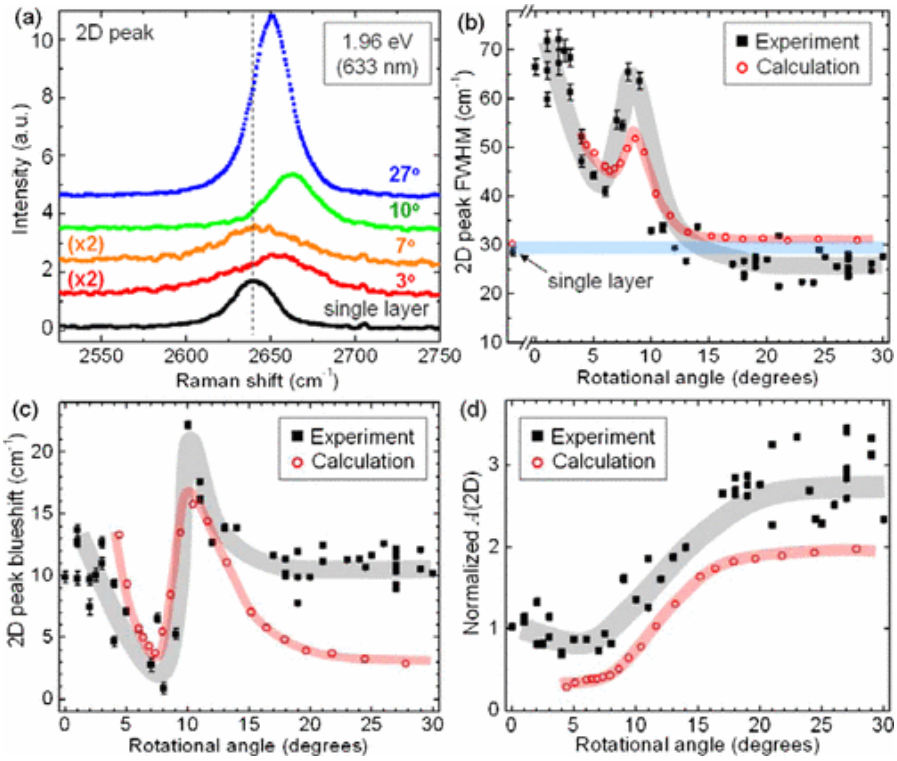

Figure 19 Rotational-angle dependence of Raman 2D peak. (a) Graphene 2D peak for rotated double-layer and single-layer graphene. The vertical dashed line represents the center of single-layer 2D peak. (b) Rotated double-layer graphene 2D peak FWHM. We have fitted the 2D peaks with a single Lorentzian peak for simplicity. The black squares and red circles are the experimental and theoretical calculation values. The blue horizontal area represents the experimental value from single-layer graphene. The grey (experiment) and red (calculation) areas are guides to the eye. (c) Rotated double-layer graphene 2D peak blue-shift in respective to the value from single-layer graphene. (d) Integral intensity of 2D peak. Experimental and calculation values were normalized to the single-layer value. Reprinted with permission K. Kim *et al*, Physical Review Letters, Volume 108, 246103 (2012). Copyright (2012) by the American Physical Society.[182]

Raman spectroscopy can also be used to determine the number of graphene layers, doping concentrations in the graphene, strain, edge states, and defect concentration in the graphene layer using the position and FWHM of the 2D, G, and D peaks together.[183] The effect of the orientation on the electrical properties of bilayer devices, and more specifically the SymFET/BiSFET, has not been experimentally determined.

1.5.3 Disorder at the Interfaces

Graphene is a one atom thick layer of carbon. The electrical properties of the graphene are highly influenced by the interaction of the graphene surface with any adjacent materials.[132, 185-187] In the case of graphene on SiO_2, the electrical properties of the graphene can become limited due to the scattering of carriers in the graphene by charged impurities and surface phonons.[188, 189] For this reason, the mobility of graphene on SiO_2 is reduced by several orders of magnitude compared to suspended graphene.[189] The silanol groups at the surface of the SiO_2 also degrade the performance of the graphene FET by causing unintentional p-doping and hysteresis in the graphene FET.[190] This makes the development of buffer layers which can be integrated into a CMOS fabrication process necessary for graphene electronics.

The opposing side of the graphene is equally as important as the substrate side. The conventional method for depositing dielectrics is atomic layer deposition. In the case of graphene, direct deposition using atomic layer deposition has been an issue. The basal plane of graphene is free of dangling bonds and does not provide nucleation sites.[191, 192] Methods commonly employed for depositing dielectrics on graphene include (i) metal oxidized at ambient seeding layers[193] (ii) functionalization of the graphene by ozone treatment[194] (iii) and plasma assisted deposition[195]. The deposition of dielectrics on graphene using ozone and plasma assisted deposition techniques have been shown to degrade the graphene characteristics. The degradation has been attributed to damage to the graphene, increased phonon scattering from the dielectric, and trapped charges either in the dielectric or at the graphene/dielectric interface. Whether or not conventional ALD dielectrics and the required seeding layer to deposit them are of high enough quality to

make graphene FETs viable has yet to be determined. Furthermore, the necessity for a seeding layer limits the scalability of the oxide thickness. Graphene based two dimensional heterostructures have been studied to overcome the limitations of traditional insulating substrates/dielectric barriers.

Two dimensional heterostructures have been predominantly created by mechanical exfoliation.[49, 196-199] Single layers of the constituent materials are exfoliated from a bulk crystal source and mechanically stacked to form the vertical heterostructure. Hexagonal boron nitride is a commonly used two dimensional material for graphene based two dimensional heterostructures. The mechanical layering of graphene on hBN has been shown to drastically improve the electrical properties of graphene.[200-203] This improvement has been attributed to the strong in-plane ionic bonding which leaves the hBN surface free of dangling bonds and surface traps, the atomically planar surface which suppresses rippling in the graphene, and the relatively high energy phonon modes of hBN compared to SiO_2 which result in reduced scattering compared to the SiO_2.[204]

One potential problem in the use of hBN with graphene arises due to the similarity in the hBN and graphene structure.[205] When graphene is in contact with hBN, the relatively small lattice mismatch (1.8%) results in the formation of a moiré pattern. The moiré pattern formed is dependent on the lattice mismatch and rotation angle between the layers as shown in Figure 20.

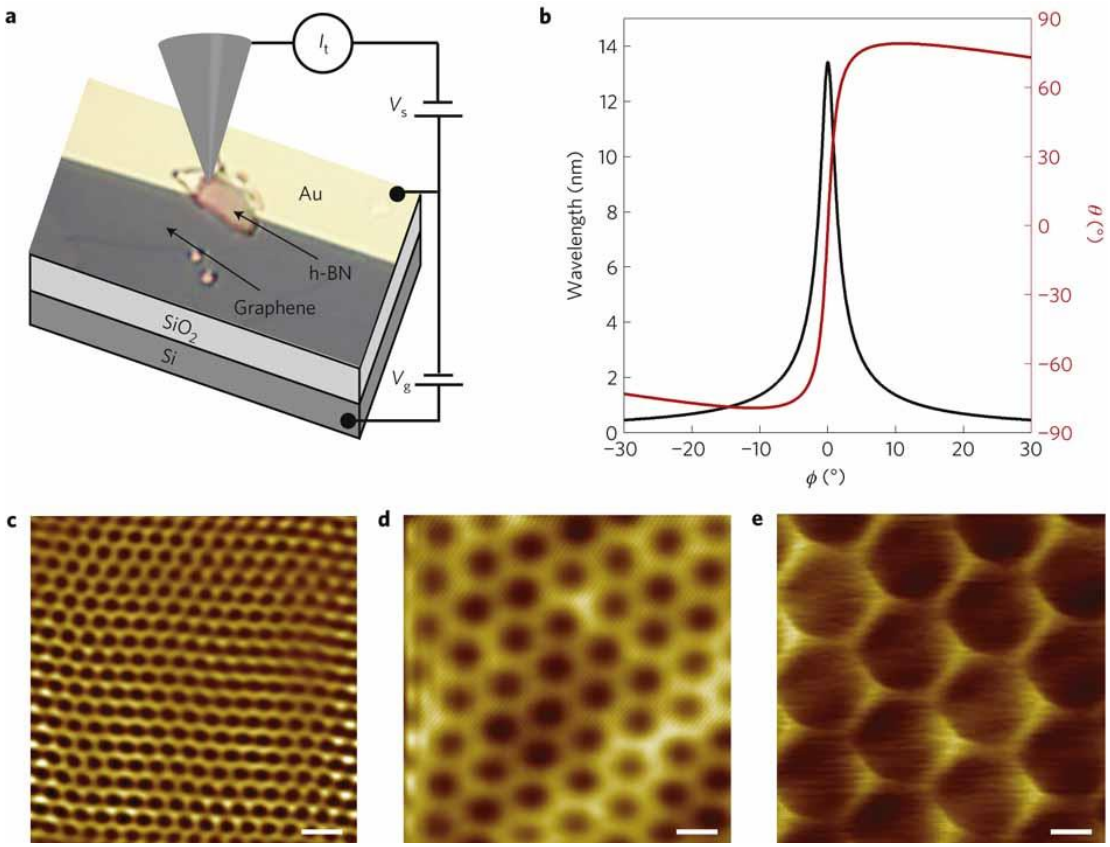

Figure 20 (A) Schematic of the measurement set-up showing the STM tip and an optical microscope image of one of the measured samples. (B) Superlattice wavelength (black) and rotation (red) as a function of the angle between the graphene and hBN lattices. (C-E) STM topography images showing (C) 2.4 nm (D) 6.0 nm (E) 11.5 nm moiré patterns. Typical imaging parameters were sample voltages between 0.3 V and 0.5 V and tunnel currents between 100 pA and 150 pA. The scale bars in all images are 5 nm. Reprinted by permission from Macmillan Publishers Ltd: Nature Physics. M. Yankowitz *et al*. Volume 8, Issue 5, Pages 382-386 copyright (2012)[205]

The moiré pattern can be characterized by the wavelength of the periodic structure defined by equation 12.

$$\lambda = \frac{(1+\delta)\alpha}{\sqrt{2(1+\delta)(1-\cos\phi)+\delta^2}} \qquad (12)$$

Where δ is the lattice mismatch, α is the graphene lattice constant, and ϕ is the rotation angle. For hBN, when ϕ = 0 the moiré wavelength reaches a value of 13.4 nm. This degree of order between the hBN and graphene gives rise to a periodic potential which

alters the band structure of the graphene as shown in Figure 21.[205] The periodic potential gives rise to superlattice Dirac points in the graphene which can effectively open a bandgap. The impact on the graphene band structure is dependent on the moiré pattern wavelength. Shorter wavelengths do not impact the graphene band structure.[206] For this reason, two dimensional materials with larger lattice mismatch are of interest for graphene heterostructures.

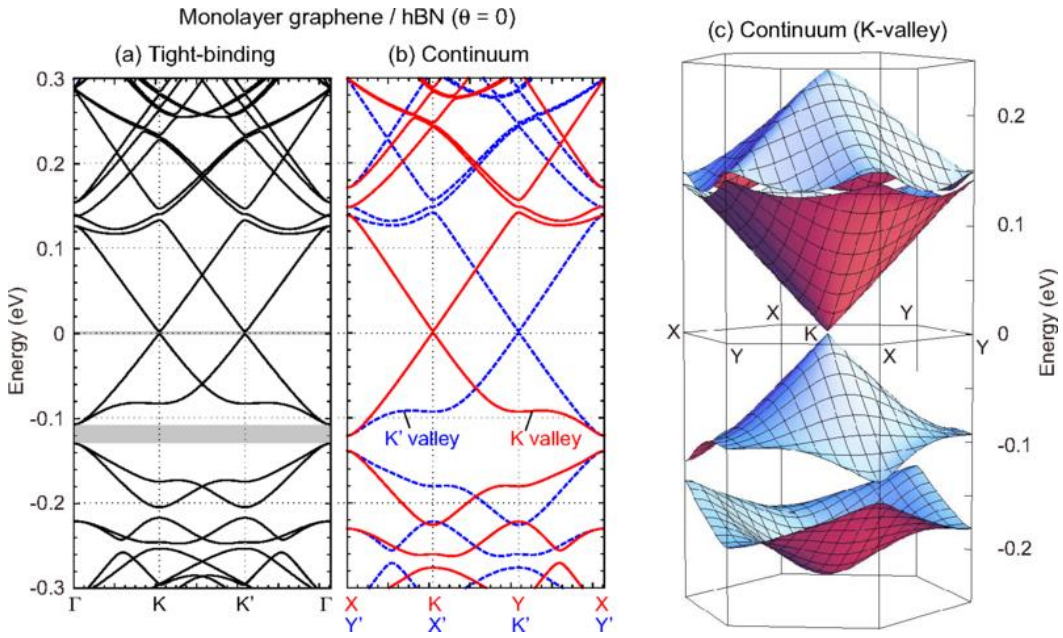

Figure 21 Band structures of monolayer graphene/hBN system with θ = 0° calculated by (a) the tight-binding model and (b) the effective continuum model. (c) Three-dimensional plot of the first and second electron and hole bands of K-valley, calculated by the continuum model. Reprinted with permission from P. Moon, M. Koshino. *Physical Review B*. 90, 155406 2014. Copyright (2014) by the American Physical Society.[207]

The transition metal dichalcogenides (TMDs) have been of particular interest for graphene based heterostructures.[206, 208, 209] The TMDs are expected to improve the electronic properties of graphene due to the lack of dangling bonds, atomically smooth surface, and reduced phonon scattering similar to hBN. Naturally occurring TMD crystals

have a higher inherent defect concentration compared to hBN.[206] Due to this, the TMDs have not shown the similar predicted improvements to the graphene electrical properties as seen for hBN.[210, 211] The large defect concentrations have been experimentally shown to result in significant charge trapping and reduced electron mobilities in graphene/MoS_2 heterostructures.[206, 210] The observed reduction in electron mobilities is due to charge fluctuations which arise from the line and point defects within the TMD structure. The impact of these defects for a vertical tunneling heterostructure has not been explored. Initial reports of the direct synthesis of complimentary two dimensional materials on graphene have shown degradation of the underlying graphene or nanocrystalline domain sizes of the synthesized material.[212-215] The use of CVD synthesized hBN and graphene has shown to have less improvement of the graphene in-plane electrical transport compared to exfoliated materials as a result.[214] Initial reports of MoS_2 synthesized on graphene by molecular beam epitaxy has shown similar results.[215] The impact of the increased disorder due to the direct synthesis of the complimentary two dimensional materials on the vertical transport in a graphene based heterostructure has not been determined.

1.6 Other applications of graphene

In any application using graphene, graphene will be placed on and ultimately be placed on by other materials. Methodologies for synthesizing and fabricating graphene devices will be required to make graphene viable in any application space. Understanding the impact of adjacent materials and how to minimize any negative effects will be necessary. The work presented in this dissertation analyzes how material based disorder impacts the electrical behavior of a graphene tunneling field effect transistor, but the

derived knowledge pertaining to synthesizing graphene, depositing materials on graphene, cleaning contamination, and processing of graphene in general can be applied to an arbitrarily large application space which utilizes graphene. A few selections of alternative applications of graphene in which this work can be applied are briefly discussed.

1.6.1 Photodetectors

Graphene is a gapless semimetal making it an ideal candidate for deep IR photodetectors.[216-218] The lack of a bandgap allows graphene to absorb any wavelength of light making graphene an ideal broad spectrum photon detector. While thermal fluctuations will still introduce noise into graphene detectors, novel device architectures taking advantage of the two dimensional nature of graphene have been developed to overcome this limitation.[219, 220]

One design for a photon based detector is shown in Figure 22. Two graphene sheets are separated by a thin dielectric as shown in Figure 22A. The bottom graphene sheet acts as a FET with a deposited source and drain contacts. As light is incident on the top layer of graphene, an electron hole pair is generated. The electron can then tunnel through the dielectric barrier separating the electron hole pair before recombination as shown in Figure 22C.[220] This generates a net positive charge on the top graphene layer. This charge produces a gating effect on the bottom graphene layer allowing photo detection through a change in the current of the bottom layer. This device architecture allows tunability in the detected wavelength of light by adding an additional gate below the bottom graphene layer. By changing the Fermi level of the bottom graphene sheet, the detectable wavelengths of light can be tuned.[220]

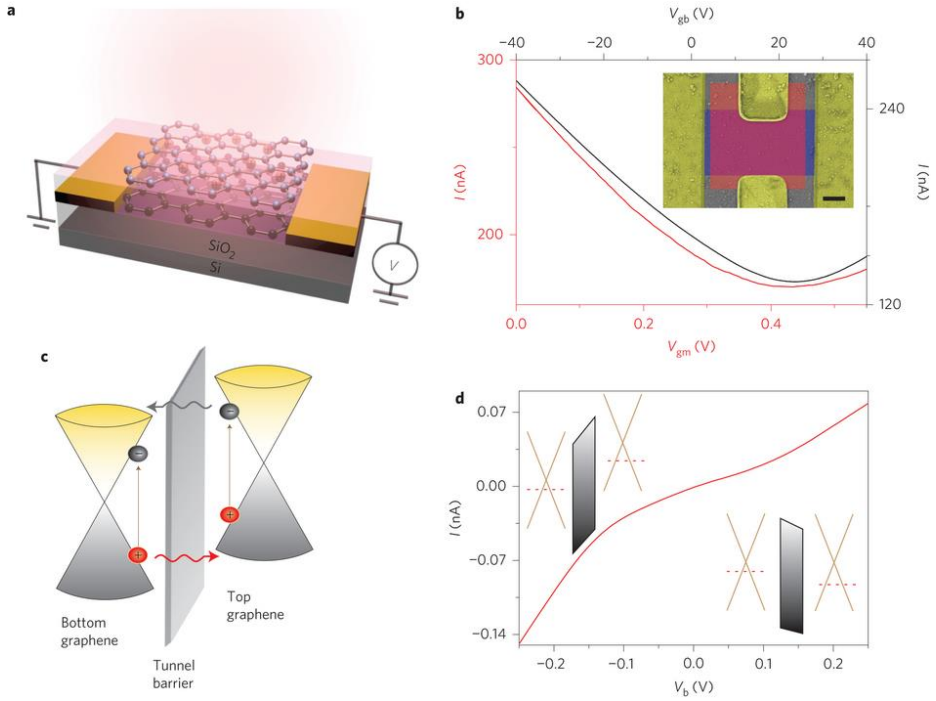

Figure 22 (A) Schematic of device structure. (B) Black (right and top axes): transfer curve for bottom graphene layer using a silicon back gate (V_{gb}). Red (left and bottom axes): transfer curve for top graphene layer using the bottom graphene as the gate (V_{gm}). From these transport curves, we calculate the Fermi energies of the top and bottom graphene layers to be 4.756 eV and 4.655 eV, respectively. Inset: False-color scanning electron microscopy (SEM) image of the device. The gold areas indicate the metal electrodes and the purple and red areas the bottom and top graphene layers, respectively. Scale bar, 1 µm. (C) Schematic of band diagram and photo excited hot carrier transport under light illumination. Electrons and holes are represented by grey and red spheres, respectively. Vertical arrows represent photoexcitation, and lateral arrows represent tunneling of hot electron (grey) and hole (red). (D) Vertical tunneling current as a function of bias voltage applied across two graphene layers. The bottom layer is grounded, and bias voltage is applied to the top layer. Inset: Schematic band diagrams under forward and reverse bias. Red dashed lines indicate the Fermi levels of the graphene layers. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology C.H. Liu *et al*. Volume 9, Issue 4 Page 273-278, copyright (2014)[220]

Graphene photodetectors based off thermal detection have also been experimental shown. One such graphene photodetector utilizes the photo thermoelectric effect when graphene is contacted by two dissimilar metals.[219] When the light is incident upon the

graphene, the electrons become heated. Due to the dissimilar metals in contact with the graphene, a potential gradient forms across the metal/graphene/metal junction. A thermoelectric current is generated due to the potential gradient which serves as the detection mechanism. The fabricated thermoelectric graphene photodetector performance was comparable to current state of the art room temperature detectors for THz detection.

1.6.2 Interconnects

Graphene is a promising candidate for future interconnect technologies due to the large mean free path of electrons in graphene as well as the high current densities achievable.[221-225] Graphene interconnects used to connect graphene based transistors would additionally reduce contact resistances further improving circuit performance.[226] Graphene interconnects have been shown to offer improvements over Cu interconnects for future interconnect scaling.

Figure 23 shows the potential improvement in delay over copper interconnects at various interconnect lengths when the interconnect width is 14 nm. A ~10% improvement at short interconnect lengths and ~45% improvement in circuit delay at long interconnect lengths can be achieved with high quality graphene (suspended graphene meets these conditions) interconnects free of extrinsic scattering sources. As the quality of the graphene interconnect diminishes, a small improvement can still be seen for short interconnect lengths, but low quality graphene (CVD graphene on SiO_2) is worse than an equivalent copper interconnect at long interconnect lengths.[227]

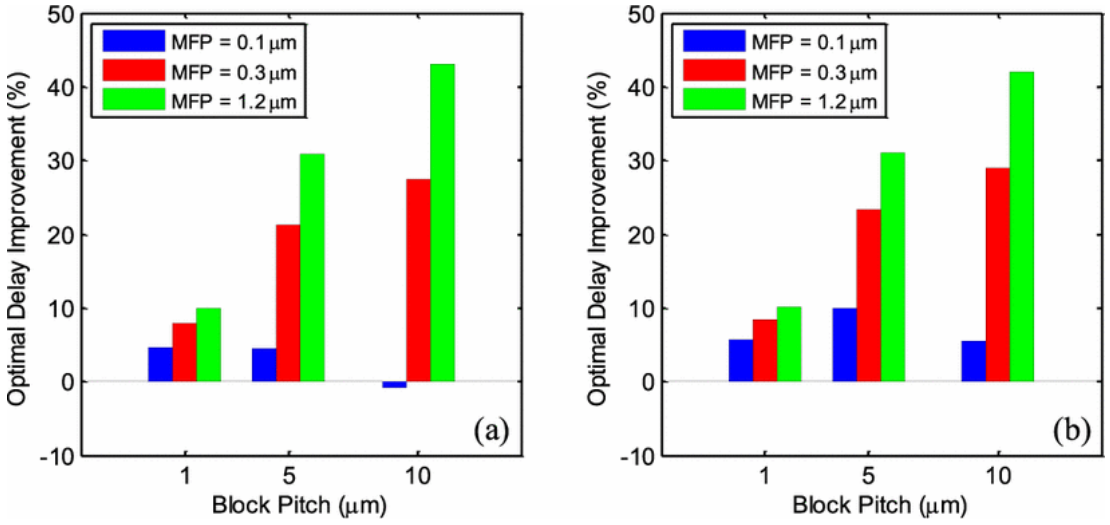

Figure 23 Optimal delay improvement versus block pitch for various MFP values at low supply voltage V_{dd} = 0.5 V with (A) normal threshold voltage and (B) high threshold voltage devices. © [2015] IEEE. Reprinted, with permission, from C. Pan *et al*, Technology/Circuit/System Co-Optimization and Benchmarking for Multilayer Graphene Interconnects at Sub-10-nm Technology Node. IEEE Transactions on Electron Devices, May 2015.

1.6.3 Diffusion Barrier

Graphene can also be introduced as the diffusion barrier for copper interconnects as seen in Figure 24.[228-233] As a diffusional barrier, graphene promotes higher current densities, higher breakdown voltages, and lower resistivity of the copper interconnects in addition to preventing the Cu from diffusing into the underlying Si/SiO_2.[231-233] Similar to the direct use of graphene as an interconnect, the performance of a graphene/Cu stack as the interconnect is dependent on the quality of the graphene. Higher quality graphene serves as a better diffusional barrier and graphene which exhibits reduced scattering from edge states, impurities, and other extrinsic scattering factors results in higher current densities and reduced resistivity of the interconnect structure.[231, 233]

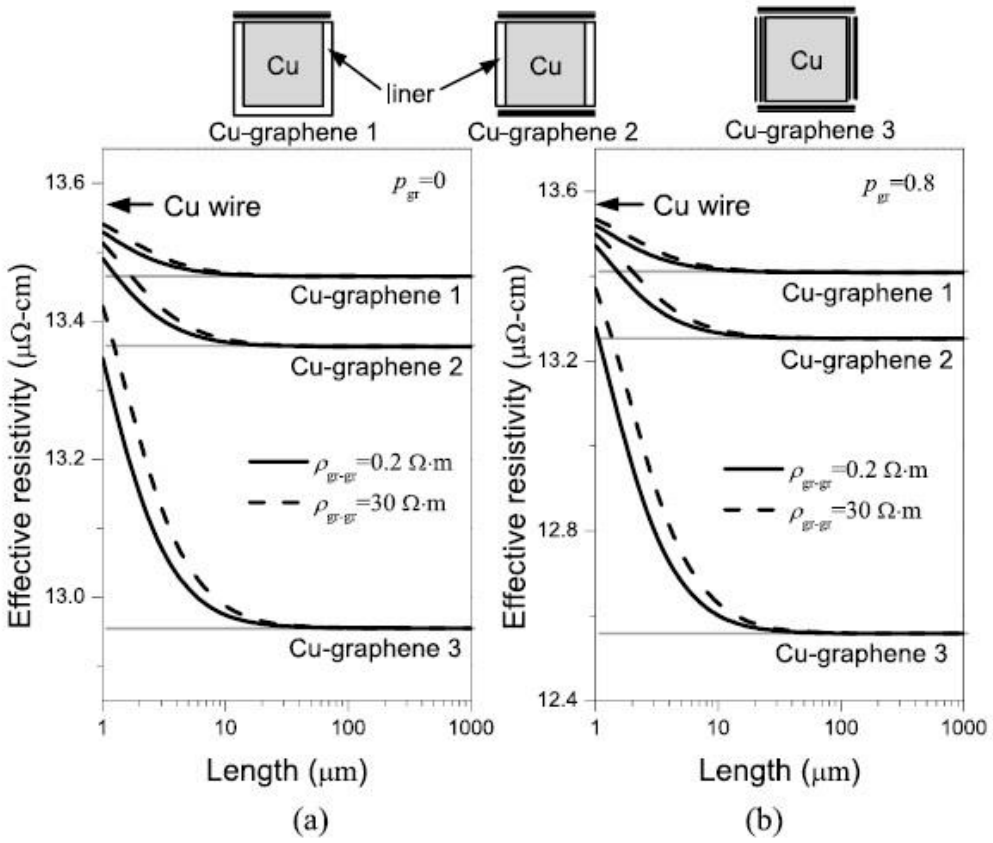

Figure 24 Effective resistivity of Cu-graphene heterogeneous interconnects versus interconnect length. (A) p_{gr} = 0; (B) p_{gr} = 0.8. © [2015] IEEE. Reprinted, with permission, from W.S. Zhao *et al*, Electrical Modeling of On-Chip Cu-Graphene Heterogeneous Interconnects. IEEE Electron Device Letters, May 2015.[233]

1.6.3 Chemical Sensors

Graphene sensors have been shown to be capable of detecting a single gas molecule on the graphene surface.[234] The adsorption of a gas molecule on the graphene surface results in a charge transfer between the graphene and adsorbed gas molecule, similar to other solid-state sensors. [235]Graphene has been explored as an ideal candidate for biosensing, gas/vapor sensing, and electrochemical sensors. Graphene is the ideal candidate for these applications due to its two dimensional structure, room temperature stability, and high mobility.[236-238] The two dimensional structure of graphene allows

graphene to be minimally invasive. The high mobility results in reduced signal distortion. The stability of graphene allows the fabrication of graphene chemical sensors that do not require auxiliary heating, which reduces the complexity of graphene based sensors.[239, 240] All of these properties of graphene make it the ideal candidate for many sensing applications.

CHAPTER 2: GOALS AND ORGANIZATION

2.1 Goals

While significant work has been conducted on proving the viability of the graphene based electronics, very little work has been conducted on understanding how graphene can be integrated into a traditional CMOS fabrication process and what the impact of the fabrication process will be on the graphene. The goals of the work presented in this dissertation are (i) to develop a materials processing and integration scheme for large-area two dimensional materials (ii) determine the impact of contamination and disorder on vertical and horizontal electrical transport in graphene based vertical heterostructures (iii) elucidate the role of material synthesis/processing on the introduction of disorder in the vertical heterostructure and how this disorder impacts electrical transport. These goals will be achieved by fabricating and studying a large number of SymFET structures with a variety of tunneling barriers, graphene domain sizes, and processing conditions.

2.2 Organization

Chapter 3 discusses the experimental techniques used in the dissertation. It includes the synthesis of the 2D materials used in the dissertation, the transfer process of the 2D materials, and discussion on the techniques used for sample fabrication including e-beam evaporation, atomic layer deposition, spin coating, and photolithography. The physical characterization techniques used in the dissertation are presented as well as the electrical characterization methods. This chapter serves as a general overview of how these characterization techniques are used. The specific process parameters and experimental details are provided in the subsequent chapters.

Chapter 4 presents the development of a cleaning process to remove contaminants arising from the processing of graphene. Thermal decomposition of the contaminants and its impact on the graphene electrical properties are presented and discussed. A thermal decomposition in a hydrogen containing atmosphere is shown to significantly reduce process contaminants while thermal decomposition in an inert atmosphere is ineffective. Thermal processes of removing contamination are further shown to result in damage to the graphene structure. A wet chemistry cleaning process utilizing a sacrificial Ti layer etched by a dilute HF solution is introduced. The electrical results following the sacrificial Ti layer are compared to the graphene without any additional cleaning and exposure to HF without the sacrificial Ti layer. The deposition and removal of the Ti layer is shown to be the most effective methodology for removing processing contaminants from the graphene and results in the best electrical performance of all cleaning methods studied. The sacrificial Ti cleaning method is utilized to remove processing contaminants in all subsequent studies.

Chapter 5 discusses the fabrication and electrical characterization of graphene tunneling junctions with atomic layer deposited dielectric barriers. A variety of tunneling barriers are deposited and the tunneling current is shown to be dependent on the tunneling barrier deposited. Furthermore, engineering of the desired tunneling characteristics is shown to be possible by engineering the tunneling barrier to give the desired characteristics. For tunneling barriers thicker than ~ 3 nm, the tunneling is shown to be dominated by trap assisted tunneling. By scaling the thickness of the tunneling barrier, direct tunneling is shown to be the dominant tunneling mechanism. While direct tunneling as the dominant tunneling mechanism is necessary for the observance of NDR,

no NDR is observed for any of the fabricated devices. The graphene grain boundaries are investigated as the source of disorder limiting the observance of NDR and are found to have a negligible impact on the tunneling current.

Chapter 6 reports on the use of a two dimensional material, MoS_2, as the dielectric barrier for the graphene tunneling structure. MoS_2 is directly synthesized on graphene at two different temperatures. While the direct synthesis of MoS_2 is shown to be detrimental to the underlying graphene, significantly less sulfur is shown to be incorporated into the graphene at reduced synthesis temperatures. It is suggested that the presence of Mo acts as a catalyst to incorporating sulfur into the graphene. The impact of the graphene on the MoS_2 synthesis process is investigated and any impact is found to be negligible. An e-beam deposited Mo layer of 1 nm thickness is found to form a highly uniform trilayer of MoS_2 regardless of whether the MoS_2 is synthesized on SiO_2 or graphene. The electrical properties of the individual graphene layers as well as the tunneling characteristics of the devices are presented. The direct synthesis of MoS_2 on graphene is shown to greatly degrade the graphene electrical properties. Graphene tunneling junctions with directly synthesized MoS_2 cannot be modulated. Graphene tunneling junctions with a transferred MoS_2 tunneling barrier are compared to the directly grown samples showing that the impact on the graphene is a result of the synthesis process and not inherent in a graphene/MoS_2/graphene junction. The tunneling current of the transferred MoS_2 devices is presented and compared to theory.

Chapter 7 expands upon chapter 6 using a hBN two dimensional material as the tunneling dielectric. In addition, an hBN buffer layer is placed between the graphene and SiO_2 in order to reduce the scattering caused by the SiO_2 phonon modes. The electrical

performance of the graphene with and without the hBN buffer layer is compared. The hBN buffer layer is shown to significantly increase the mobility of the graphene. The mean free path of the graphene is calculated from the mobility measurements and shown not to be limiting the coherence length of the tunneling structure. The tunneling characteristics of the fabricated devices are measured and no NDR is observed. This suggests component of the graphene TFET is the coherence within the tunneling barrier.

Chapter 8 presents suggestions for further improvement of the work including improvements to the synthesis processes for the complimentary two dimensional materials to graphene, using other two dimensional materials as electrodes instead of graphene, directly synthesizing the two dimensional materials on the target substrate, and suggested process improvements to the current fabrication process.

Chapter 9 presents a summary and general discussion of the dissertation work.

CHAPTER 3: EXPERIMENTAL METHODS

3.1 Materials Synthesis

3.1.1 Graphene Synthesis

Graphene was synthesized on 99.8% copper foils of 25 μm thickness (Alfa Aesar 13382) in a CVD FirstNano EasyTube 3000 advanced CVD system. The copper foil was placed in glacial acetic acid for one minute and rinsed with DI water prior to being placed in the furnace load lock. After placing the copper foil in the load lock, the load lock was purged by pumping the load lock down to 20 mTorr then backfilling with argon. After purging in the load lock, the copper foil was loaded into the CVD chamber. The chamber was then purged under a constant argon flow of two liters per minute for eight minutes before being pumped to a base pressure of $8x10^{-7}$ Torr. After reaching base pressure, the chamber was heated to 1000°C at a rate of 180°C per minute under a constant Ar/H_2 flow of 200 sccm and 15 sccm respectively at a pressure of 250 mTorr. After reaching 1000°C the copper foil was annealed under a constant Ar/H_2 flow of 200 sccm and 15 sccm respectively for 10 minutes. After annealing, the Ar flow was shut off and CH_4 was introduced to the chamber at a flow rate of 45 sccm as a carbon precursor for a total gas flow of 45 sccm CH_4 and 15 sccm H_2 at 250 mTorr for 6 hours. The graphene was synthesized during this time. After the 6 hour synthesis step, CH_4 and H_2 flows were shut off and the chamber was flushed with Ar at a flow rate of 2 lpm. The furnace was cooled under a constant Ar flow of 2 lpm at a pressure of 2 Torr at the natural cooling rate of the system (initial cooling rate of ~200°C per minute with a total cooling time of 1.5 hours to

reach room temperature) to room temperature. After reaching room temperature the Ar flow was shut off and the graphene was removed from the furnace.

3.1.2 Molybdenum Disulfide Synthesis

Molybdenum disulfide was synthesized either on a SiO_2/Si substrate (300 nm oxide formed by dry oxidation at 1000°C) or on graphene transferred to a SiO_2/Si substrate. Prior to synthesis, a 1 nm film of Mo metal was deposited on the substrate of choice by e-beam evaporation in a Denton Explorer e-beam evaporation system at 0.3 Å/s. The synthesis substrate was then placed into a furnace equipped with a vacuum pump and pumped down to base pressure (~$5x10^{-6}$ Torr). After evacuating the chamber, the synthesis substrate was annealed for 30 minutes at 300°C in a 4:1 Ar/H_2 atmosphere to reduce the natural oxide formed on the Mo upon exposure to atmosphere after e-beam deposition. During the annealing step, a separate sulfur container was heated to 160°C to generate sulfur vapors. After annealing, the chamber was cooled and pumped to base pressure. The vacuum valve was then closed creating a static environment in the furnace. Sulfur vapors were introduced to the static chamber raising the pressure to ~20 mTorr. After sulfur introduction, the static chamber was backfilled to 5 Torr with Ar. The chamber was then heated to the synthesis temperature of either 820°C or 1020°C and left for 1 hour. The chamber was then purged with Ar at process temperature followed by cooling to room temperature under a constant Ar flow. The thickness of the synthesized MoS_2 was controlled by the initial Mo deposition thickness. The deposited thickness of 1 nm resulted in the synthesis of a trilayer MoS_2 film.

3.1.3 Hexagonal Boron Nitride Synthesis

The hexagonal boron nitride used in this study was supplied by Professor Gong Gu of the University of Tennessee Knoxville. The hexagonal boron nitride was grown on Ni using an atmospheric CVD process in a hot wall furnace. Nickel foils (25 μm thick, 99.5% Ni, Alfa Aesar) were used as the synthesis substrate. Ammonia borane (BH_3-HN) was sublimed at 120°C and delivered to the CVD chamber by a Ar:H_2 carrier gas. The synthesis time for the hBN formation is ~10 minutes followed by rapid cooling of the substrate. The growth process on Ni results in 3-7 layers of hBN as identified by TEM cross-sectional characterization.

3.2 Sample Fabrication

3.2.1 Transfer of 2D materials

3.2.1.1 Graphene

A wet transfer process was used to transfer the graphene from the copper growth substrate to the substrate of interest for each study. First, poly methyl(methacrylate) (PMMA 996k Sigma Aldrich 182265) was dissolved in chlorobenzene at a concentration of 46 mg/mL. The PMMA was coated onto one side of the graphene coated copper by spin coating at a rate of 3000 rpm for 60 seconds and allowed to dry overnight. As graphene forms on both sides of the copper foil during synthesis, the reverse side of the foil not protected by PMMA was etched in an Oxford Endpoint RIE to remove the graphene on the backside of the foil. The etch was done at a pressure of 100 mTorr with a 25 watt O_2/Ar plasma (25 sccm O_2 and 5 sccm Ar flow) for 30 seconds. The Cu/Gr/PMMA stack was then floated Cu side down in two consecutive nitric acid baths (3:1 H_2O:HNO_3) for 60 seconds each to begin the copper etching process. Following the

nitric acid etch, the Cu/Gr/PMMA stack was transferred to an ammonium persulfate (0.5M) (APS) bath for two hours (floating copper side down). During this two hour etch, the Cu/Gr/PMMA stack becomes completely transparent. The stack is then transferred to a second APS bath for ~18 hours to remove any residual Cu that may remain. The now Gr/PMMA stack is rinsed with deionized water (DI), transferred to an isopropyl alcohol (IPA) bath to remove residual water, and fished out of IPA to the substrate of interest. After drying under a constant low pressure N_2 flow, the Gr/PMMA stack on the desired substrate is heated to 220°C at a rate of 20°C/min on a hot plate and baked at 220°C for 5 minutes. The sample is then soaked in acetone for 2.5 hours to remove the PMMA coating.

3.2.1.2 MoS_2

MoS_2 synthesized on 300 nm SiO_2 was transferred to the target sample using a wet transfer process similar to the graphene wet transfer process. PMMA was spun onto the MoS_2 at 3000 rpm for 60 seconds and allowed to dry overnight. The $Si/SiO_2/MoS_2$/PMMA stack was submerged in buffered oxide etch (BOE) for several hours until the MoS_2/PMMA stack was released from the surface (typically overnight). The MoS_2/PMMA stack was transferred to 3 consecutive DI water baths for 60 seconds each to remove any residual BOE contamination. The MoS_2/PMMA stack was fished out of the last DI water bath to the target substrate and dried under a constant low pressure N_2 flow. The sample was heated to 220°C at a rate of 20°C/min on a hot plate and baked at 220°C for 5 minutes. The sample is then soaked in acetone for 2.5 hours to remove the PMMA coating.

3.2.1.3 hBN

Hexagonal boron nitride films synthesized on Ni foils were transferred to the target substrate by a modified wet transfer process. The Ni/hBN films were coated with PMMA by spin coating at 3000 rpm for 60 seconds and allowed to dry overnight. The sample was floated uncoated side down in Copper Etchant 100 ($FeCl_3$ and HCl solution) overnight. The hBN/PMMA stack was rinsed in a DI water bath for 60 seconds, transferred to an IPA bath to remove residual water, and fished onto the target substrate from the IPA. After drying under a constant low pressure N_2 flow, the sample was heated to 220°C at a rate of 20°C/min and baked at 220°C for 5 minutes. The sample was then soaked in acetone for 2.5 hours to remove the PMMA coating.

3.2.2 Spin Coating

Spin coating was performed using a BLE Delta 20 spin coater. Samples were mounted to a 4" Si carrier wafer using Kapton tape for spin coating. PMMA used for transferring of the 2D films was dispersed at 1000 rpm (1000 rpm/s acceleration) for 15 seconds before accelerating to 3000 rpm at a rate of 1000 rpm/s and spinning at 3000 rpm for 60 seconds. The thickness of the PMMA film was measured to be ~50 nm by ellipsometry.

SC 1813 positive photoresist was used for the optical lithography definition of the samples in this study. SC 1813 photoresist was manually dispensed to the stationary wafer followed by a dispersion step at 1000 rpm for 15 seconds. The sample was accelerated at a rate of 1500 rpm/s to 4500 rpm and spun for 60 seconds. A soft bake prior to lithographic exposure was performed at 115°C for 60 seconds. The thickness of the SC 1813 after spin coating was ~1.2 μm.

3.2.3 Photolithography

Contact lithography was used to define the structure of the fabricated devices in a Karl Suss TSA MA-6 mask aligner. SC 1813 positive photoresist of 1.2 μm thickness was used for all patterning. The photoresist was exposed to 435 nm light for a total dosage of 120 mJ/cm^2 while in hard contact with a fused silica/chromium photomask. Following exposure, the substrate was submerged in MF 319 developer for 60 seconds then rinsed under flowing DI water. A multilevel mask set (up to 8 levels) was used in the fabrication of the devices fabricated in this study.

3.2.4 Metal Deposition

Metal deposition was performed in either a Denton Explorer e-beam evaporator or CHA Mark 40 e-beam evaporation system. The e-beam chamber was pumped to a base pressure of at least 2x10^{-6} Torr before depositing material. Metals of thickness less than 10 nm were deposited at a rate of 0.3 Å/s. Thicknesses above 10 nm were deposited at a rate of 1 Å/s. The thickness of the deposited film was measured in situ using a quartz crystal resonant sensor. Metal patterns were defined using a lift-off process in which the definition of the metal contacts was patterned in SC 1813 photoresist using contact lithography. The metal was deposited using e-beam evaporation to fill the contact shaped holes in the resist layer. The resist layer was removed by soaking in acetone which in turn lifted off the unwanted metal leaving behind only the metal deposited in the contact regions.

3.2.5 Dielectric Deposition

Dielectrics were deposited by atomic layer deposition (ALD) in a Cambridge Nanotech Plasma ALD system. All depositions were performed at 250°C. Trimethyl

aluminum (TMA) was used as the Al precursor. Tetrakis(dimethylamido)hafnium (TDMAH) was used for the Hf precursor. Tetrakis(dimethylamido)titanium (TDMAT) was used for the Ti precursor. Water was the oxygen precursor for all depositions. The dielectrics were deposited at a rate of ~1 Å/cycle and thicknesses were confirmed by ellipsometry.

Due to the inert basal plane of the graphene, a seeding layer was necessary to nucleate the deposition of ALD dielectrics on graphene. For this purpose, a Ti metal layer of 1-2 nm thickness was deposited by e-beam evaporation and allowed to naturally oxidize in air. The formed TiO_x layer served as the seeding layer for subsequent dielectric deposition in the ALD system.

Dielectric regions were defined using a wet etch process. The dielectric layer was uniformly deposited across the entire surface of the sample. SC 1813 photoresist was spun onto the dielectric surface and patterned using contact lithography. The dielectric areas of interest were protected by the resist layer and the unwanted dielectric layers were exposed. The samples were placed in a 100:1 HF:DI solution and etched at a rate of 1 nm per 45 seconds of etch time.

3.3 Characterization

3.3.1 Ellipsometry

Ellipsometry was performed with a Woolam M-2000 spectroscopic variable angle ellipsometer. All ellipsometry measurements were performed at angles from 65 to 75 degrees with a 5 degree step. The acquisition time at each step was five seconds. Cauchy models were used to fit the experimental data in order to determine the measured thicknesses.

3.3.2 Atomic Force Microscopy (AFM)

Atomic force microscopy was performed with a Veeco Dimension 3100 scanning probe microscope. Silicon cantilevers coated with Al on the reflex side with a pyramidal silicon tip of 1-2 nm radius and a spring constant of 37 N/m were used for imaging. All topographic images were acquired in tapping mode with a tip velocity less than 15 μm/s. AFM scan data was analyzed using Gwyddion analysis software. RMS roughness values were calculated from the entire scan area unless otherwise noted.

3.3.3 Scanning Kelvin Probe Microscopy (SKPM)

Scanning Kelvin Probe Microscopy measurements were performed using a Veeco Dimension 3100 scanning probe microscope. Pt/Ir coated silicon cantilevers with a pyramidal tip of radius 30 nm and a spring constant of 3 N/m were used for SKPM measurements. The topography of the sample was measured in tapping mode on the trace and retrace scan. The SKPM measurement was performed during the interleave scan at a constant height of 5 nm.

3.3.4 Raman Spectroscopy

Raman Spectroscopy was performed in a Thermo Nicolet Almega XR Dispersive Raman Spectrometer with a 488 nm laser at a spot size of 0.7 μm. All measurements were conducted in ambient conditions. All Raman spectra were collected by exposures of 2 seconds and 10 integrations.

3.3.5 X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy was performed in a Thermo Scientific K-Alpha XPS system with a monochromatic Al Kα X-ray source and a hemispherical analyzer in

Constant Analyzer Energy (CAE) mode (50 eV pass energy, 0.1 eV step size). The X-ray spot size was varied from 400 μm to 30 μm dependent on the size of the feature of interest. High resolution elemental scans were performed with 10 integrations and 15 seconds per scan.

3.3.6 Electrical Measurements

Electrical measurements were conducted using a Keithley 4200-SCS semiconductor parameter analyzer. A lakeshore TTPX cryogenic probe station was used for all vacuum and low temperature measurements. Liquid nitrogen was used to cool the probe station to as low as 77 K. Electrical measurements were also conducted using a Cascade summit 12000 semi-automatic probe station. Electrical measurements conducted in the Cascade probe station were conducted under a constant flow of nitrogen at room temperature and ambient pressure. Measurements conducted in vacuum were annealed at 80°C for ~18 hours to remove residual contamination from the environment prior to taking measurements.

The electrical properties of the individual graphene layers were extracted using a constant mobility model developed by Kim *et al*. A two point probe measurement setup is used. The resistance of the graphene at a fixed drain bias is measured as a function of the applied back gate voltage. The measured resistance is modelled using equation 13.

$$R_{tot} = R_{con} + \frac{N_{sq}}{\sqrt{n_o^2 + n_{ind}^2}e\mu} \quad (13)$$

Where R_{tot} is the total resistance, $R_{contact}$ is the contact resistance, N_{sq} is the number of squares, n_o is the intrinsic carrier concentration, n_{ind} is the induced carrier concentration from the back gate, e is the charge of an electron, and μ is the mobility. The induced

carrier concentration is determined as a function of the Dirac point of the graphene as shown in equation 14.

$$n_{ind} = \frac{[V_{Dirac} - V_{BG}]C_{ox}}{q} \quad (14)$$

Where V_{Dirac} is the Dirac point of the graphene, V_{BG} is the applied back gate voltage, C_{ox} is the capacitance of the back gate oxide, and q is the charge of an electron. The total resistance is modelled using $R_{contact}$, n_o, μ, and the Dirac point of the graphene as fitting parameters and compared to the measured resistance of the graphene channel. A least squares approach is used to minimize the error between the modelled resistance and the experimental resistance.

CHAPTER 4: CLEANING GRAPHENE

4.1 Introduction

One key issue preventing graphene from being fully integrated into conventional complementary metal oxide semiconductor (CMOS) processing is the sensitivity of graphene to processing conditions.[60, 241-243] The transfer of CVD grown graphene and the conventional photolithography processes used in the fabrication of graphene devices have been shown to leave behind residue negatively impacting device performance.[244] To date, several techniques for the cleaning of graphene such as electrical current annealing,[174] plasma cleaning,[245] and chloroform treatments[170] have been used with varying degrees of success. Electrical current annealing has been shown to be an effective means for cleaning individual graphene devices, but has shown limited success in removing residues from large graphene areas. Plasma cleaning processes reported in the literature involve highly reactive oxygen and hydrogen species as well as ion bombardment which results in defect generation in the graphene sheets.[246, 247] Chloroform cleaning treatments are not desirable due to its toxicity. Therefore, other methods for the removal of residues introduced during processing are needed in order to fully incorporate graphene into traditional CMOS processing.

4.2 Thermal Cleaning

Thermal decomposition of the contaminants is one potential method for cleaning graphene. The main contaminant species after processing the graphene, PMMA, thermally decomposes at temperatures approaching 300 °C.[248] By heating the fabricated devices to 300 °C, the polymeric contaminants will decompose and be removed from the

surface. In this study, back gated graphene FETs fabricated from the same copper foil (i.e. graphene grown during the same growth run) and transferred to a substrate cleaved from the same Si/SiO_2 wafer were used to reduce run-to-run variations. The devices were fabricated using conventional photolithography for patterning and e-beam deposition to deposit Ni/Au capped contacts. The first set of devices, labelled "as-is", were soaked in acetone for 2 hours after device fabrication. The second set of devices, labelled "nitrogen", were heated to 300 °C in a nitrogen environment at atmospheric pressure for 3 hours followed by a 2 hour soak in acetone. The third set of devices, labelled "forming gas", were heated to 300 °C for 3 hours in a 10% H_2/90% N_2 environment at atmospheric pressure followed by a 2 hour soak in acetone. For both the nitrogen and forming gas samples the applied heating rate was 10 °C per minute. 15-20 devices of each set were fabricated and measured.

XPS was used in order to assess the effectiveness of the cleaning procedures at removing the PMMA contaminants. The C 1s XPS spectrum was used to monitor the presence of PMMA before and after cleaning. Lorentzian peak shapes of fixed position and width were used to fit the graphene C 1s component peaks. Gaussian-Lorentzian cross product peak shapes of fixed position, width, and constrained area ratios were used to fit the PMMA component peaks. Positions, widths, and area ratios for the PMMA spectrum were taken from Lhoest *et al.*[249] A Shirley background correction was used in all spectra. Shown in Figure 25A, the graphene C 1s XPS spectrum has a primary peak at 284.4 eV corresponding to the sp^2 C-C bonds (pink) which makeup the structure of the graphene. The secondary peak accounts for the inherent asymmetry of the sp^2 C-C peak (dark green). The linear combination of all component peaks forms the overall shape of

the C 1s spectrum (orange). The graphene with PMMA C 1s spectrum, shown in Figure 25B, contains the sp^2 C-C peak from the graphene located at 284.4 eV, the sp^3 C-C peak from the PMMA located at 284.8 eV (red), the C-C(O)-O peak located at 285.6 eV (green), the C-O peak located at 286.7 eV (blue), and the C=O peak located at 288.9 eV (light blue). Figure 25C shows the C 1s spectrum after heating the sample in a nitrogen environment. The C 1s spectrum contains sp^2 C-C contributions from the graphene, sp^3 C-C contributions, C-C(O)-O contributions, C=O contributions, and C-O contributions suggesting the sample is still heavily contaminated. Figure 25D shows the C 1s spectrum of the forming gas sample. The C 1s spectrum shows contributions from the graphene as well as the PMMA component peaks.

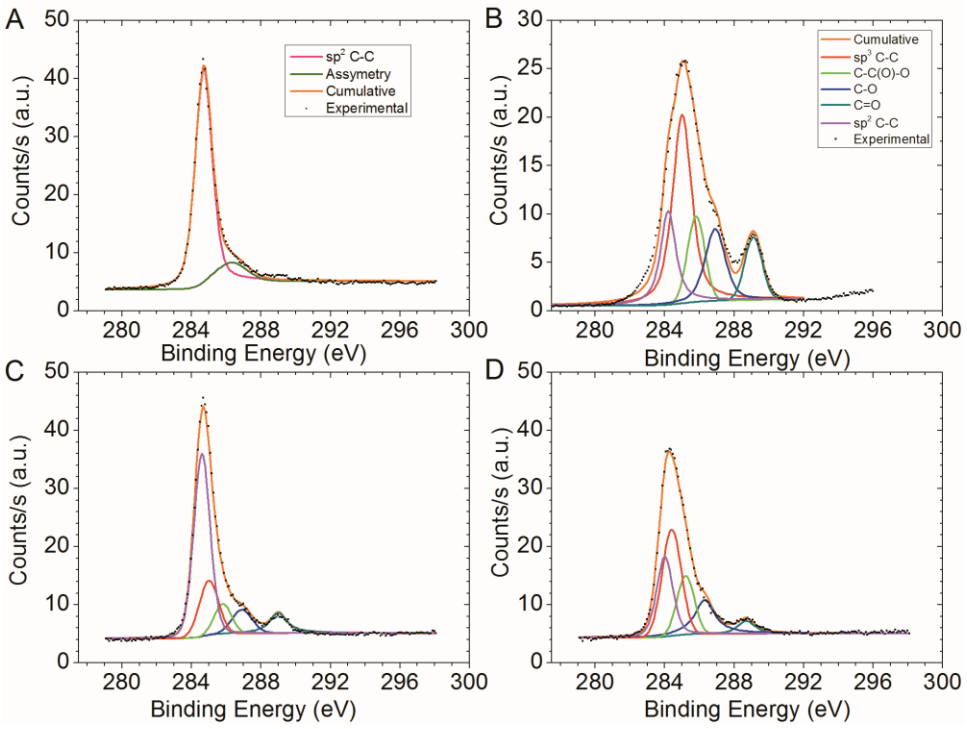

Figure 25 (A) C 1s spectra for intrinsic graphene. (B) Deconvolution of the C 1s spectrum for graphene before cleaning (C) Deconvolution of the C1s spectrum for graphene after exposure to forming gas at 300°C for 3 hours. (D) Deconvolution of the C 1s spectrum for graphene after exposure to nitrogen at 300°C for 3 hours.

The area ratio of the graphene C 1s component to the overall C 1s area is used to determine the percentage of the C 1s spectrum that is derived from the graphene. As the PMMA is removed, a greater amount of the C 1s spectrum will be derived from the graphene components. The effectiveness of the cleaning procedure is determined by the percentage of the C 1s spectrum derived from the graphene component compared to the graphene before cleaning. Heating under nitrogen results in a slight increase of 6% in the sp^2 contribution percentage indicating heating under a nitrogen environment is a poor method of removing contamination from the surface. Heating under forming gas shows a significant increase of 25% in the sp^2 contribution percentage indicating a significant reduction in contamination.

The area ratios of the PMMA component peaks can be used to determine whether the contamination present after heating remains PMMA or is a redeposited decomposition product. The peak area percentages shown in Table 2 show a reduction in the C=O and C-O component areas indicative that the bulk of the contamination on the sample heated under nitrogen is no longer PMMA. This indicates decomposition of PMMA without removing the polymeric decomposition products from the surface. The increase in the relative sp^2 contribution percentage indicates a marginal decrease in the total amount of contamination after heating under nitrogen with the bulk of the decomposition products redepositing on the graphene. When heating in a forming gas environment, the area ratios of the PMMA component peaks are consistent with PMMA as shown in Table 1. This suggests partial decomposition of the PMMA into volatile species which leave the surface of the graphene. Contamination that remains on the sample is still structurally PMMA. Full decomposition of the PMMA may be possible with additional heating time.

Table 1 Peak area ratios (referenced to peak at 284.8 eV) from the XPS fittings shown in Figure 25.

Sample	284.8 eV	285.6 eV	286.7 eV	288.9 eV	284.4 eV
Before Cleaning	1	0.5	0.5	0.5	.60
Nitrogen	1	0.51	0.49	0.14	.73
Forming Gas	1	0.5	0.5	0.5	3
PMMA	1	0.5	0.5	0.5	0

The effectiveness of the cleaning methods was further quantified by atomic force microscopy (AFM). An AFM topography image of the as-is graphene is shown in Figure 26. The topography shows a dense covering of contamination. The contamination is a near continuous film of 2-5 nm in height as shown in the extracted height profile. The overall roughness of the as-is graphene sample was found to be 3.3±0.8 nm.

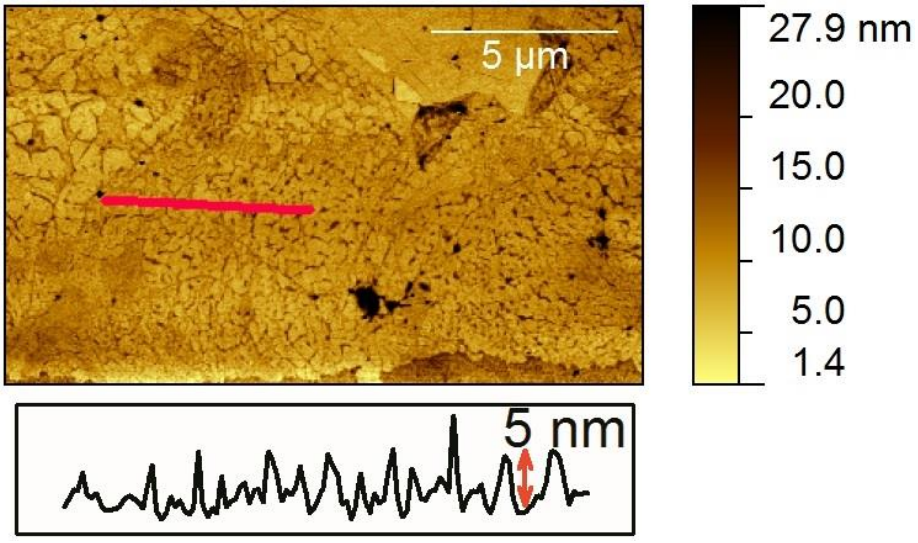

Figure 26 AFM topology of graphene after processing without any additional cleaning procedures. The height profile is taken from the line scan outlined in red.

Heating the graphene in a nitrogen environment results in the contamination migrating to form clusters as shown in Figure 27. The clusters of contamination measure ~7 nm in height and cover the majority of the graphene surface. The graphene in between the clusters shows sub nanometer roughness values of the same magnitude as the underlying substrate roughness of 0.4±0.2 nm. The clusters of contamination cover 55.62% of the surface of the nitrogen sample.

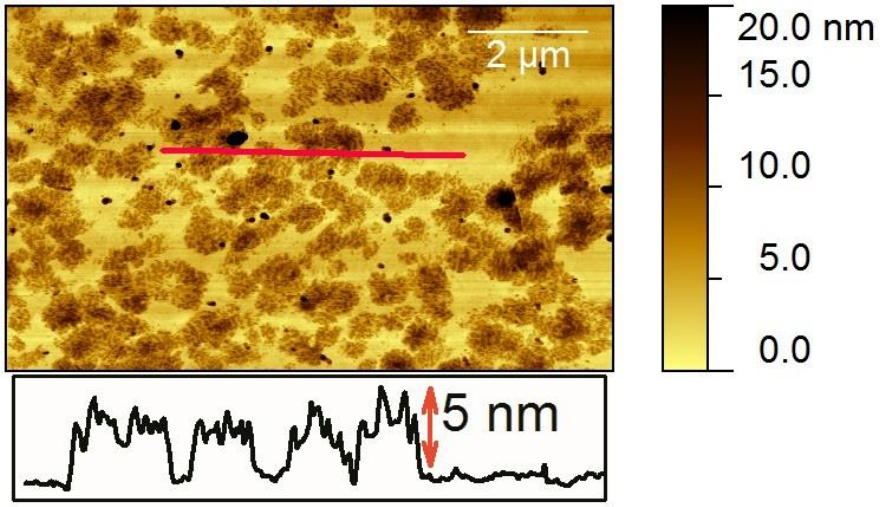

Figure 27 AFM topography image of graphene after exposure to a nitrogen environment at 300°C for 3 hours. Height profile is taken from the line scan shown in red.

In comparison, heating the graphene sample in a forming gas environment results in an overall surface roughness of 0.92±0.3 nm. Similar to heating under nitrogen, the forming gas sample shows clustering of the contaminants after heating as shown in Figure 28. The clusters have an approximate height of 7 nm and a surface coverage of 14.65%.

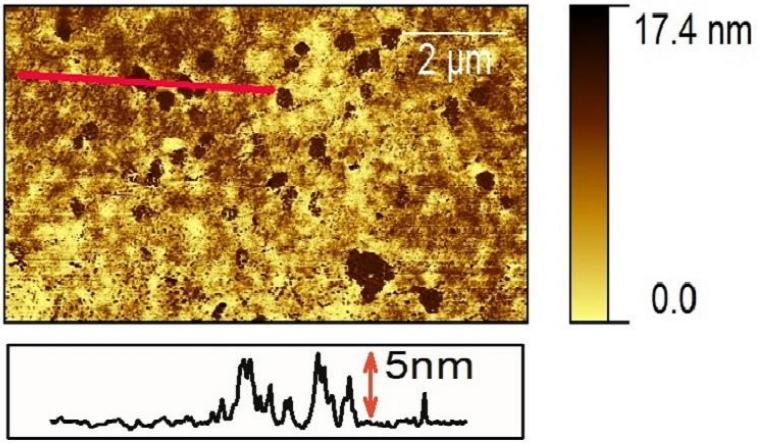

Figure 28 AFM topography of graphene after exposure to a forming gas environment at 300°C for 3 hours. The height profile is taken from the line scan shown in red.

Structural analysis of the graphene before and after cleaning is performed by using Raman spectroscopy. The Raman spectra for each cleaning condition are shown in Figure 29A. The typical graphene 2D peak is visible around 2700 cm^{-1} and represents a double resonance process in which an electron is scattered from a K point in the graphene band structure to a K' point then back to a K point. The G peak visible at 1580 cm^{-1} corresponds to the optical vibration mode between two adjacent carbon atoms in a graphene layer. The third peak which commonly appears in the graphene Raman spectra is the D peak located at 1350 cm^{-1}. The D peak is a disorder induced band which is only present in defected areas of the graphene. The 2D:G ratio combined with the FWHM of the 2D peak can be used to assess the number of graphene layers. The observed spectrum for the as-is sample shown in Figure 29B shows a 2D:G ratio of >2:1 and a FWHM of 30 cm^{-1} indicating single layer graphene. The absence of the D peak at 1350 cm^{-1} is a clear indication that the graphene is of high quality. By observing the evolution of the

graphene Raman spectra with each cleaning process, the impact of the cleaning process on the graphene is determined.

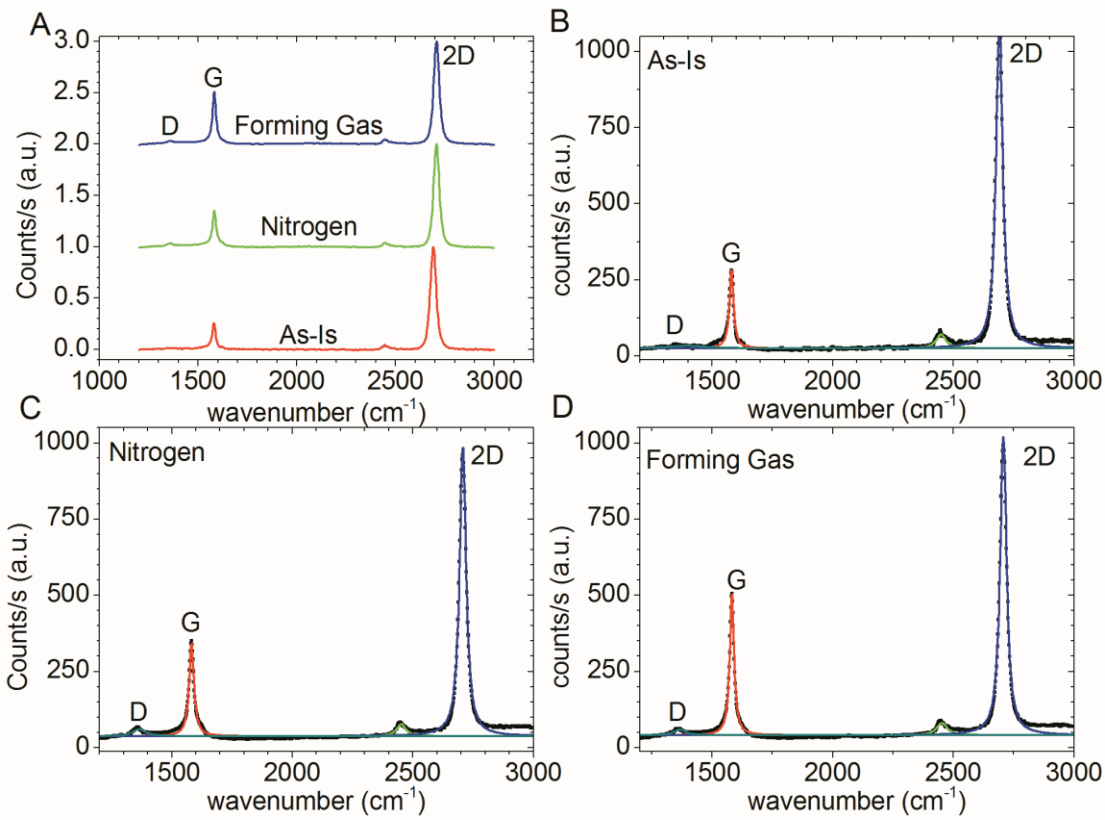

Figure 29 (A) Raman spectra of graphene before and after each cleaning condition. (B-D) Raman spectrum before cleaning, after nitrogen cleaning, and after forming gas cleaning respectively. Lorentzian peak fittings for the D, G, and 2D are superimposed.

The nitrogen sample Raman spectrum shows a marginal increase in the D peak at 1350 cm^{-1} as shown in Figure 29C indicating the heating process introduces a small amount of defects into the graphene structure. 2D peak shifts to 2707 cm^{-1}while the G peak shifts to 1582 cm^{-1} indicative of p doping from the cleaning process. The increased D peak and the shifting of the 2D and G indicate that nitrogen cleaning is not an acceptable cleaning method.

The forming gas sample Raman spectrum shown in Figure 29D shows a slight increase in the D peak intensity. The D peak intensity is 25% larger than the D peak introduced by heating under nitrogen suggesting the hydrogen can react with the graphene to create additional defects. The 2D peak and G peak are shifted to 2707 cm^{-1} and 1582 cm^{-1} respectively. The similar peak shifting observed between the forming gas and nitrogen annealing suggests the doping is most likely coming from an increased interaction with the substrate or ambient environment as a result of the heating as opposed to the environment the sample was heated in. Overall, the forming gas and nitrogen processes have a marginal impact on the graphene physical and electronic structure as observed by Raman spectroscopy.

The electronic properties of the graphene are further assessed by fabricating back gated FETs and performing I_D-V_G measurements (transfer measurements) of the graphene. Graphene intrinsically has equal conductance of electrons and holes. This is shown in the transfer curve by symmetry around the point of minimum conductance (Dirac point; V_{Dirac}) which is intrinsically at 0 V. The transfer curve of the as-is samples shows a shifting in the Dirac point to 18 V and a slight asymmetry in the hole and electron conductance. The method developed by Kim *et al* is used to extract the mobility, carrier concentration, and total contact resistance from the transfer curve in order to assess the impact of the cleaning procedures on the electrical performance of graphene FETs.[193] Shown in Figure 30B, the average Dirac point of the graphene shifts from 18 V to 14.4 V after heating in either forming gas or nitrogen. The reduced shifting of the Dirac point is indicative of a reduction in accidental doping of the graphene. The Dirac point is similar for the forming gas and nitrogen samples despite the disparity in polymer

contaminants on the graphene as evidenced by XPS and AFM. This suggests the doping of the graphene is either coming from the substrate or adsorbates from the environment and not the remaining polymer contaminant. The intrinsic carrier concentration, n_0, is a measure of the free carrier concentration at the Dirac point. The free carrier concentration of graphene is intrinsically 0 cm^{-2}. An increase in n_0 is indicative of an increase in charge at the graphene interfaces. As shown in Figure 30A, the as-is sample shows an average n_0 of $9x10^{11}$ cm^{-2} with a standard deviation of $4x10^{11}$ cm^{-2}. The forming gas sample shows an average n_0 of $1.05x10^{12}$ cm^{-2} with a standard deviation of $2x10^{11}$ cm^{-2}. The change in n_0 between the as-is sample and the forming gas sample falls within the error of the as-is sample indicating only a marginal change in n_0 when heating in an inert environment. The nitrogen sample shows an average n_0 of $1.2x10^{12}$ cm^{-2} with a standard deviation of $1x10^{11}$ cm^{-2}. The change of $3x10^{11}$ cm^{-2} of the nitrogen sample is indicative of a significant increase. The increase in n_0 is a result of more intimate contact between the substrate and graphene as a result of the heating. While this effect is also present in the forming gas sample, the hydrogen present during heating in forming gas passivates the silicon surface. A similar n_0 is measured between the as-is sample and the forming gas sample due to the offsetting of increased substrate influence due to a more intimate contact by a reduction in the surface charge due to hydrogen passivation at the SiO_2/graphene interface. As shown in Figure 30 C, a slight increase in contact resistance is seen for both heat treatments. Both heat treatments result in an increased mobility while forming gas treatment results in a slightly higher mobility as shown in Figure 30D.

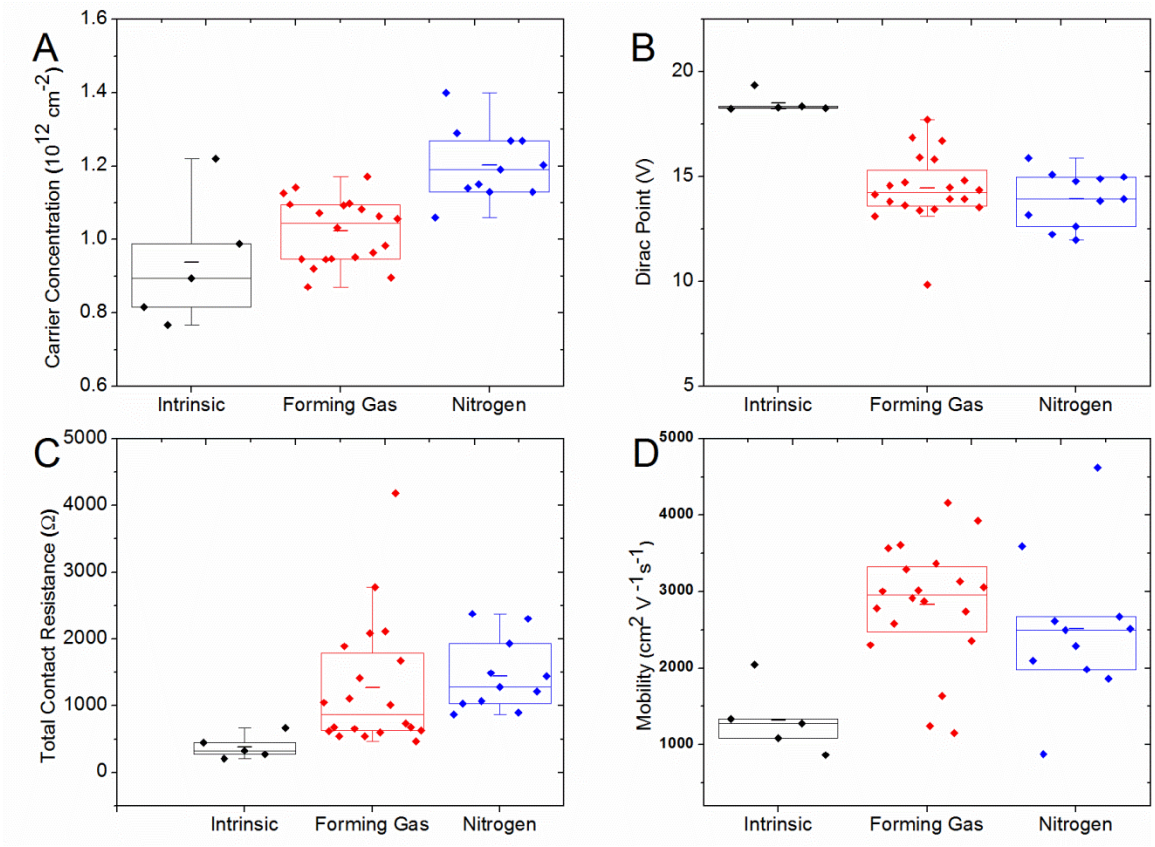

Figure 30 (A) Induced carrier concentration (n_0) before and after cleaning. (B) Dirac point of the graphene before and after cleaning. (C) Total contact resistance before and after cleaning. (D) Mobility before and after cleaning.

4.3 Titanium Cleaning

Back gated field effect transistors (FETs) were fabricated using conventional photolithography and e-beam evaporation for the deposition of Ni contacts capped with Au. Three sets of devices (15 devices per set) were fabricated using graphene from the same copper foil (i.e. graphene grown during the same run) and transferred to a substrate cleaved from the same Si/SiO_2 wafer to prevent run-to-run variations in the data. The first set of devices, labeled "as-is", did not receive any post fabrication treatments following device fabrication. The second set of devices, labeled "HF-cleaned", was

treated with a 200:1 DI:HF solution for thirty seconds. The third set of devices, labeled "Ti-cleaned", had 2 nm of Ti deposited via e-beam evaporation at a rate of 1 Å/s and was subsequently etched using a 200:1 DI:HF solution until the Ti was completely removed as evidenced by x-ray photoelectron spectroscopy (XPS). The thickness of 2 nm was chosen as the thickness was sufficient to provide complete coverage of the graphene and did not require a significant etch time to remove. Thicker depositions are not expected to impact the cleaning procedure other than increasing the etch time required to fully remove the Ti layer. The deposition rate was chosen due to system calibration settings and is not expected to significantly impact the cleaning procedure. All electrical measurements were carried out in a Lakeshore cryogenic probe station under vacuum ($5x10^{-6}$ Torr) following an overnight 80 °C *in situ* anneal in order to remove environmental adsorbates from the graphene channel.[132]

Figure 31 shows a summary of the electrical characterization of the prepared devices. The mobility, intrinsic or impurity carrier concentration, and minimum conductance point were extracted from the I_d-V_g curves using a method outlined elsewhere.[134, 250] The mobility, impurity carrier concentration, and minimum conductance point can give a clear indication in the amount of contamination on the graphene channel. Contamination on the graphene channel acts as scattering centers for the charge carriers, decreasing the mobility due to increased scattering. Contamination on the surface can also act as dopants, injecting additional charge carriers into the graphene channel resulting in a rise of the impurity carrier concentration. The minimum conductance point of the graphene can be impacted by the introduction of charge inhomogeneity from the contamination in the form of electron/hole puddles or charged contamination species.

Figure 31A shows the mobility of the devices. The as-is devices have an average mobility of 1142 $cm^2\ V^{-1}s^{-1}$. The HF-cleaned devices saw an increase in average mobility up to 1806 $cm^2V^{-1}s^{-1}$ suggesting partial removal of the contamination while the Ti-cleaned devices showed the largest average mobility of 2235 $cm^2V^{-1}s^{-1}$. From Figure 31B, the impurity carrier concentration is slightly reduced following the HF cleaning, but is not as effective as the Ti removal process which reduces the impurity carrier concentration from $9.41x10^{11}\ cm^{-2}$ to $4.98x10^{11}cm^{-2}$. Figure 31C shows the minimum conductance point of the graphene devices. The as-is samples have an average minimum conductance point of 7.09 V. The HF cleaned samples show an increase in the minimum conductance point to 14.4 V, suggesting an increase in charge inhomogeneity on the graphene surface possibly due to the addition of fluorine or hydrogen to the graphene or due to changes in the underlying substrate resulting from HF exposure. The Ti cleaning procedure results in the minimum conductance point moving to 2.48 V, closer to the intrinsic minimum conductance point of 0 V for graphene indicating a removal of contamination from the channel. Figure 31D shows the contact resistance showing a slight increase in contact resistance after the Ti cleaning procedure.

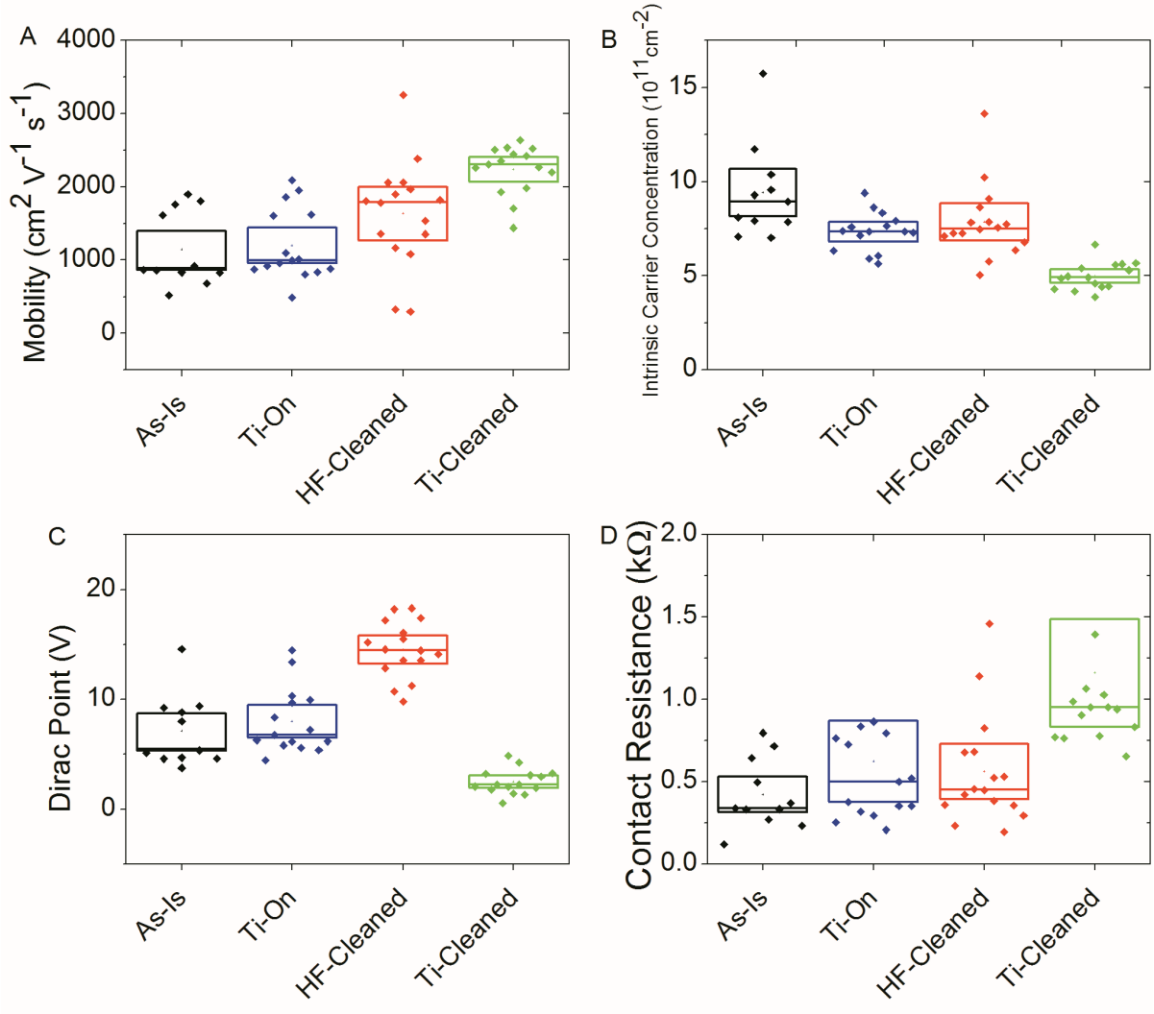

Figure 31 (A) Mobility measurements of the as-is, HF-cleaned, and Ti-cleaned devices. Ti cleaning results in the highest mobility. (B) Intrinsic or impurity carrier concentration measurements. The Ti cleaning results in a significant improvement. (C) Minimum conductance point measurements. The Ti-Clean devices shift towards the intrinsic point of graphene while the HF cleaning shifts away from the intrinsic point of 0 V. (D) Contact resistance measurements. A slight increase in contact resistance is only observed after the Ti cleaning procedure.

The impact of the cleaning procedures on the graphene was characterized using Raman spectroscopy. The Raman characterization was performed in a Thermo Scientific Nicolet Almega XR using an excitation wavelength of 488 nm. As can be seen in Figure 32A, the D-band is similar for graphene from all three processes, signifying that the e-

beam evaporation of Ti and the chemical etching process do not damage the graphene. The G band position shifts from 1582 cm^{-1} to 1572 cm^{-1} after Ti deposition as seen in Figure 32B, suggesting that the metal deposition causes doping in the channel.[183] Figure 32B also shows that following the removal of Ti from the channel, the G band position shifts to a value of 1580 cm^{-1}.[251] This indicates that the dopants associated with the Ti deposition do not remain after Ti removal and that Raman can be used as a simple and effective means to determine if all Ti has been removed. Interestingly, the Raman spectrum of the HF cleaned sample shows significant doping as seen in Figure 32B, and further indicates that HF alone is not an effective means to clean graphene as it introduces doping into the channel. This is not present in the Ti-cleaned sample despite over etching to ensure all Ti is removed.

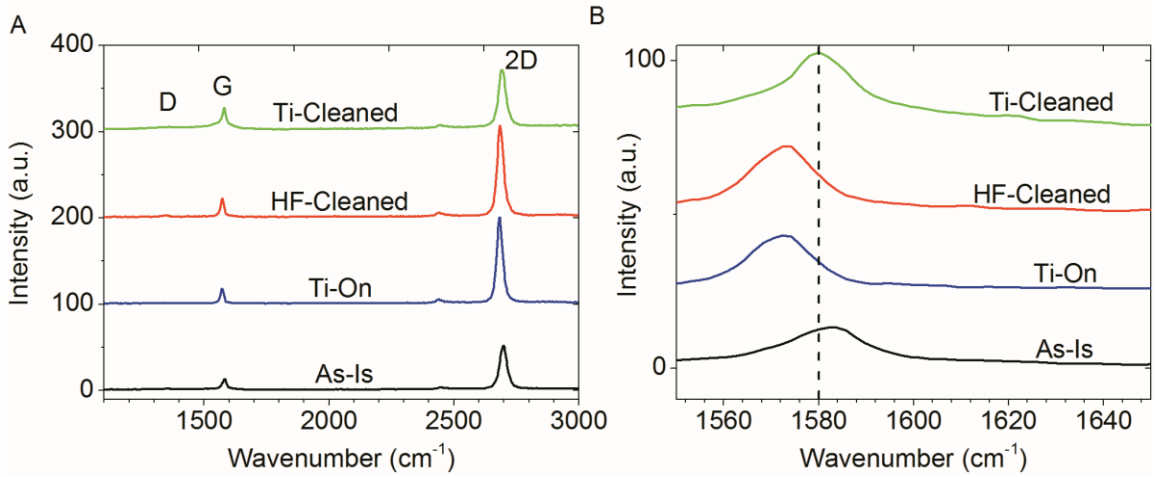

Figure 32 (A) The Raman spectra for the as-is, HF-cleaned, and Ti-Cleaned samples (Both before and after Ti removal). For all samples, the 2D/G ratio is greater than 2:1 indicating monolayer samples. The D peak is negligible in all four spectrums indicating no damage occurs to the graphene during the processing of the devices or during the cleaning procedure. The 2D, G, and D peak positions are labeled with their respective letter designations. (B) The G peak of the as-is, HF-cleaned, and Ti-cleaned samples. Shifting in the spectrum signifies doping, with Ti-cleaning being the closest to the intrinsic position of 1580 cm^{-1}.

Following the Raman and electrical characterization, the HF cleaning procedure was deemed to be inferior to the Ti cleaning process due to the apparent doping associated with the process and non-ideal electrical characterization. To further characterize the effectiveness of the Ti cleaning procedure, an XPS analysis was performed on the as-is and Ti-cleaned samples. The C1s XPS spectrum of PMMA has peaks at 289.03, 286.90, 285.68, 285.00 eV in a 1:1:1:2 ratio corresponding to the carbon-oxygen double bond, carbon-oxygen single bond, quaternary carbon bonds, and secondary/tertiary carbon bonds, respectively.[252] As can be seen in Figure 33, the as-is sample has an easily distinguishable peak located at 289 eV. This peak was used as a signature of the presence of PMMA due to the absence of such a peak in pristine graphene spectrums and because the peak is easily distinguishable from the main carbon peak at 285 eV.[167] The Ti deposited spectrum clearly shows a peak at 289 eV, indicating the PMMA is still present following the Ti deposition. Following the Ti removal, the peak at 289 eV is completely removed, indicating the complete removal of PMMA residues from the graphene channel. The Ti deposition results in Ti bonding with the oxygen sites in the oxygen rich PMMA residue as evidenced by the Ti 2p spectra (not shown) containing peaks at 458 and 464 eV, consistent with complete oxidation of the Ti layer, as well as the absence of the Ti-C peak at 282.7 eV in the C1s spectra. This bonding with the oxygen species in the PMMA assists in the breakdown of the PMMA residue, allowing the residues to be easily removed via HF removal of the Ti layer.

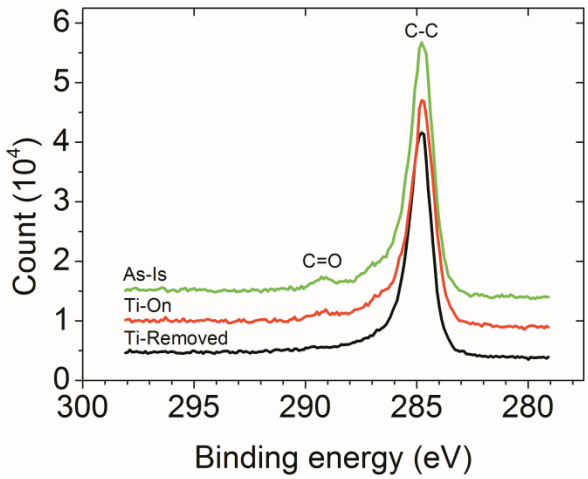

Figure 33 The C1s XPS spectra of the as-is, Ti-On, and Ti-removed samples (triangles, diamonds, and circles respectively). The C=O peak located at 289 eV is completely removed following the Ti etching indicating complete removal of the PMMA.

4.4 Conclusion

A variety of thermal and wet cleaning procedures were assessed for the removal of process contaminants following graphene device fabrication. The effectiveness of thermal cleaning was found to be dependent on the environment during heating. Heating an in inert environment was shown to result in the decomposition of PMMA, but not in the removal of the decomposition products from the surface. Heating under similar conditions in a hydrogen containing environment showed a drastic reduction in surface contaminants. The surface contaminants that remained following heating in a hydrogen environment were shown to be PMMA. While the complete removal of PMMA may be possible by increasing the length of the thermal exposure, Raman spectroscopy showed that both thermal procedures studied introduced defects into the graphene. Electrical characterization following the thermal procedures indicated an increased substrate/graphene interaction and only marginal improvements in impurity carrier concentration and Dirac point.

A wet chemical etching of a sacrificial Ti layer was shown to be a more effective cleaning procedure to the studied thermal cleaning procedures. The Ti process resulted in complete removal of the PMMA from the graphene surface and electrical properties consistent with intrinsic graphene. Additionally, the Raman spectrum of Ti cleaned graphene showed no D peak indicating no introduction of defects from the cleaning procedure. In comparison, direct exposure of the graphene to HF showed only marginal changes in the impurity carrier concentration and mobility as well as a large increase in the observed Dirac point.

CHAPTER 5: ALD BASED TUNNELING HETEROSTRUCTURES

5.1 Introduction

Tunnel FETs (TFET) are attractive for potentially replacing the traditional MOSFET for low power digital electronics due to the potential of reaching subthreshold swing values below the limit of 60 mV/decade for the conventional MOSFET.[156] The use of two-dimensional materials in tunneling based architectures is attractive due to the low effective mass and small quantum capacitance.[9] The graphene SymFET has been theoretically shown to exhibit negative differential resistance (NDR) in the tunneling characteristics due to resonance in tunneling when the Dirac points of the graphene layers are aligned.[50] Recently, gate-controlled tunneling in exfoliated graphene-hexagonal boron nitride (hBN)-graphene heterostructures have been experimentally demonstrated.[198] The observance of NDR has been theoretical predicted to be highly dependent on the disorder in the system. While an exfoliated structure allows for the observation of NDR, the scalability of such devices is limited. In this work, an integrated fabrication process utilizing large-area graphene synthesized by chemical vapor deposition and dielectrics deposited by atomic layer deposition are used in a CMOS compatible fabrication process.

5.2 Band Engineering

The traditional MOSFET utilizes thermionic current which limits the subthreshold swing of a traditional MOSFET to 60 mV/decade. The current in a TFET relies on band-to-band tunneling (BTBT) allowing the TFET to exhibit subthreshold swings of sub 60

mV/decade. The current through a graphene based TFET device can be modelled by an energy space formulation of the Bardeen Transfer Hamiltonian shown by equation 15.[253]

$$J_{tot} = \frac{e|M_{B0}|^2}{\hbar} \int_E \; g_B(E) g_T(E)(f_B - f_T) T(E) dE \qquad (15)$$

Where e is the electron charge, ħ is the reduced Planck's constant, $|M_{B0}|$ is a prefactor utilized as a fitting parameter, T(E) represents the overall transmission coefficient which accounts for direct tunneling, thermal emission, and Fowler Nordheim tunneling using the WKB approximation,[254] g_B and g_T are the density of states for the bottom and top graphene electrode respectively, and f_B and f_T are the Fermi levels for the bottom and top graphene electrode respectively.

The subthreshold swing, total device current, and on/off ratio of the TFET is ultimately determined by the barrier imposed by the dielectric tunnel barrier layer. The device behavior can therefore be controlled by engineering the tunneling barrier to give the desired current profile. In this study, band engineering for the graphene based TFET is experimentally shown using CVD synthesized graphene and various dielectric layers deposited by atomic layer deposition.

Graphene TFETs were fabricated on 7 nm thick SiO_2 grown by thermal oxidation on Si. CVD graphene was transferred onto the SiO_2/Si substrate using the wet transfer process. A 1-2 nm Ti metal layer was deposited by e-beam evaporation on the graphene and allowed to naturally oxidize under ambient conditions. The deposited TiO_x layer served as a seeding layer for the deposition of a variety of high-k tunneling barriers by atomic layer deposition at 250 °C. Four tunneling barriers were fabricated including (i) TiO_x (2 nm)/HfO_2 (5 nm) (ii) TiO_x (2 nm)/ Al_2O_3 (5 nm) (iii) TiO_x (2 nm)/TiO_2 (5 nm) and (iv) TiO_x (1 nm)/Al_2O_3 (1 nm)/TiO_2 (1 nm). Following the deposition of the

dielectric tunneling barrier, a second graphene layer was transferred on top of the stack by the wet transfer process. The graphene layers were each independently contacted by two Ni/Au contacts deposited by e-beam evaporation. Figure 34 shows a cross sectional schematic of the fabricated device.

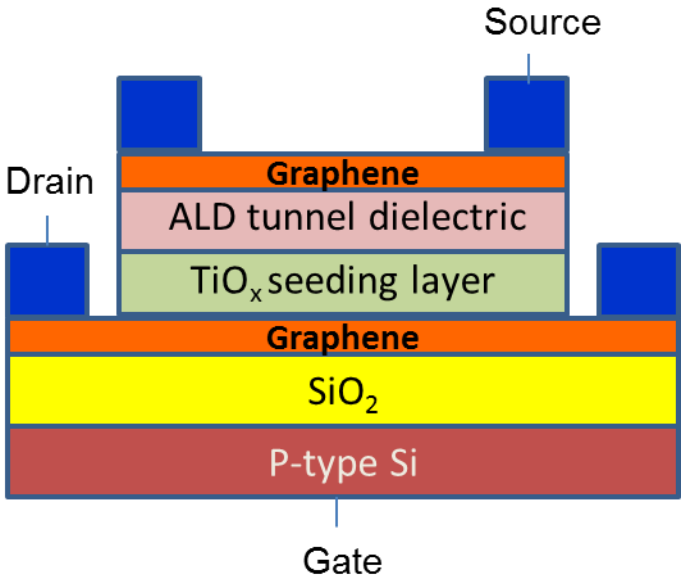

Figure 34 Cross sectional schematic of the fabricated graphene SymFET structure. Reprinted from Microelectronic Engineering, 109, T. Roy et al, Barrier Engineering for Double Layer CVD Graphene Tunnel FETs, 117-119, Copyright (2013), with permission from Elsevier.

The electrical characteristics of the fabricated devices were measured as a function of the applied gate bias as well as the applied drain bias. The devices were baked at 80 °C overnight at a pressure of ~5 x 10^{-6} Torr. The tunneling characteristics of the fabricated devices are shown in Figure 35. The subthreshold swing is calculated from the linear portion of the I_D-V_{GS} curve and ranges from 70 mV/decade for the TiO_x/TiO_2 stack to 120 mV/decade for the TiO_x/Al_2O_3 dielectric stack. The subthreshold swing of the

fabricated devices is limited by the capacitance of the gate oxide. Optimizing the design of the graphene TFET should allow for subthreshold swings less than 60 mV/decade.

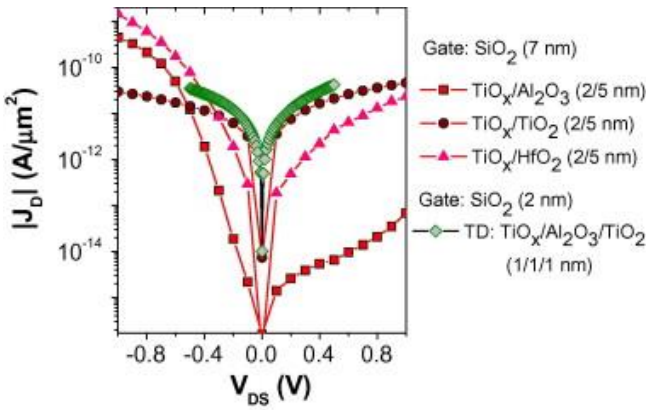

Figure 35 Tunneling current density of the fabricated graphene SymFET structures with a variety of tunneling barrier materials. Microelectronic Engineering, 109, T. Roy et al, Barrier Engineering for Double Layer CVD Graphene Tunnel FETs, 117-119, Copyright (2013), with permission from Elsevier.

The symmetry of the tunneling curve is another aspect of the graphene TFET that can be designed. As seen in Figure 35, the tunneling current is dependent on the thickness as well as the composition of the tunneling barrier. For a barrier consisting of TiO_x (2 nm)/Al_2O_3 (5 nm) the tunneling current is asymmetric due to the asymmetric barrier. The band diagram of the TiO_x/Al_2O_3 barrier is depicted in Figure 36. The electron affinity of the graphene is 4.57 eV. The electron affinity of the Al_2O_3 is 2.58 eV giving a conduction band offset of 1.99 eV. Al_2O_3 has a bandgap of 8.8 eV giving a valence band offset of 6.81 eV.[255] The electron affinity and bandgap of the TiO_x is 4.33 and 3.2 eV respectively.[256] The current due to the electron tunneling is inversely proportional to the area of the barrier above the pathway of the electron. When a positive bias is applied to the graphene electrode on the TiO_x side of the barrier, the electron sees the TiO_x and

Al_2O_3 barrier as shown. When applying a negative bias to the same electrode, the electron tunnels from the Al_2O_3 side of the barrier. The pathway from the Al_2O_3 side of the barrier sees a reduced section of the Al_2O_3 barrier compared to the electron tunneling from the TiO_x side of the barrier. The reduced effective tunneling barrier results in an increased current for negative bias voltages as seen in Figure 35.

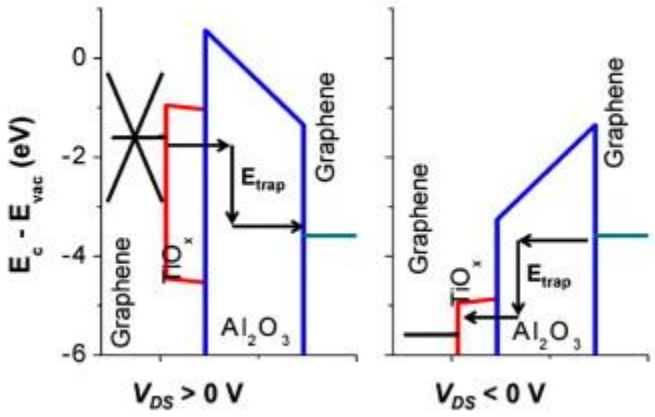

Figure 36 Energy band diagram of the TiO_x (1 nm)/Al_2O_3 (5 nm) tunneling barrier. Energy loss due to traps is not drawn to scale. Microelectronic Engineering, 109, T. Roy et al, Barrier Engineering for Double Layer CVD Graphene Tunnel FETs, 117-119, Copyright (2013), with permission from Elsevier.

At sufficiently large bias voltages, the electron will tunnel directly into the conduction band of the dielectric barrier as shown in Figure 37 for the TiO_x (2nm)/HfO_2 (5 nm) barrier. The direct tunneling into the conduction band of the barrier through the reduced effective barrier is known as Fowler-Nordheim (F-N) tunneling. The onset of F-N tunneling can be seen for the TiO_x (2 nm)/HfO_2 (5 nm) barrier at sufficiently large negative biases as shown in Figure 38.

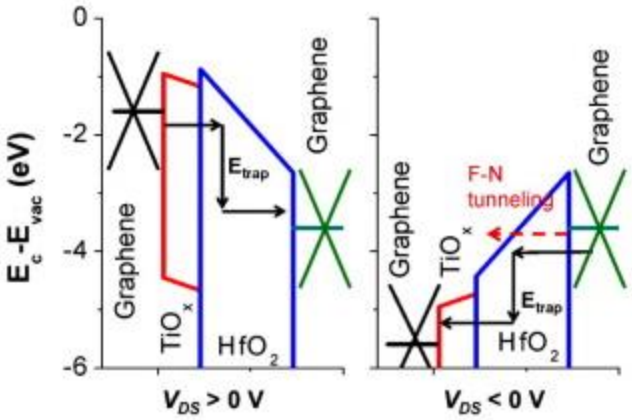

Figure 37 Energy band diagram of the TiO_x (2 nm)/HfO_2 (5 nm) barrier. At significantly large bias voltages, Fowler Nordheim tunneling is induced. Energy loss due to traps is not drawn to scale. Microelectronic Engineering, 109, T. Roy et al, Barrier Engineering for Double Layer CVD Graphene Tunnel FETs, 117-119, Copyright (2013), with permission from Elsevier.

The temperature dependence of the tunneling current was measured to determine whether the fabricated devices were dominated by trap assisted tunneling or direct tunneling. In the case of direct tunneling, the tunneling current is independent of the temperature while trap assisted tunneling is a thermally activated process. As shown in Figure 35 and Figure 38, the fabricated devices show a reduction in tunneling current as the temperature is decreased indicating trap assisted tunneling is the dominant mechanism. The trapping process could be indicative of traps at the graphene/dielectric interface, seeding layer/dielectric interface, or within the bulk of the dielectric. Oxygen vacancies have been previously shown to assist in trap-assisted tunneling for HfO_2 based barriers.

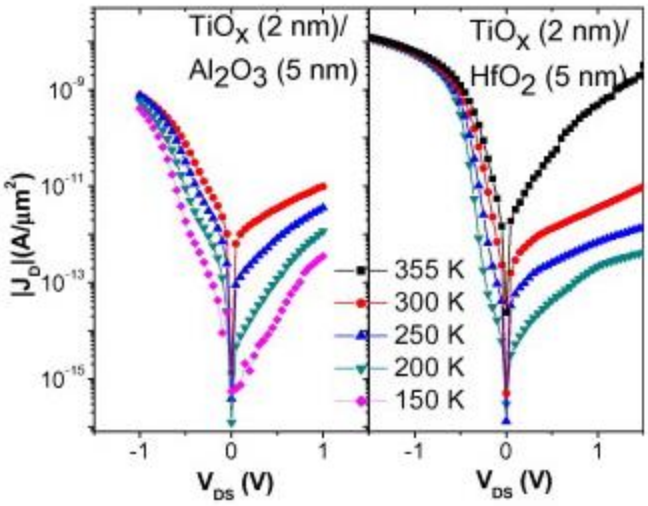

Figure 38 Tunneling current density for the TiOx (2nm)/Al_2O_3 (5 nm) tunneling barrier and the TiO_x (2 nm)/HfO_2 (5 nm) tunneling barrier. At high negative drain bias voltages the tunneling currents converge for all temperatures as Fowler Nordheim tunneling becomes dominant over trap assisted tunneling. Microelectronic Engineering, 109, T. Roy et al, Barrier Engineering for Double Layer CVD Graphene Tunnel FETs, 117-119, Copyright (2013), with permission from Elsevier.

5.3 Thickness Dependence

While the tunneling current can be controlled through band engineering in the previously fabricated tunneling barriers, the achieved current density and dominance of trap assisted tunneling are inadequate to make graphene TFETs a viable technology. Further scaling of the dielectric thickness to increase the overall current and achieve negative differential resistance is needed for this to be a viable technology. Negative differential resistance requires energy and momentum conservative tunneling. When the tunneling current is dominated by trap assisted tunneling the momentum conservative criteria cannot be met. The first criteria to achieve momentum conservative tunneling is for direct tunneling to be the dominant mechanism. As the dielectric barrier gets thinner, direct tunneling becomes more dominant.

In order to show that direct tunneling can be the dominant tunneling mechanism for a graphene TFET, graphene TFETs were fabricated with ultra-thin tunneling dielectrics. Two ultra-thin tunneling barriers were fabricated (i) a 1 nm Ti metal layer was deposited by e-beam evaporation and allowed to naturally oxidize and (ii) a TiO_x (1 nm)/Al_2O_3 (1 nm)/TiO_2 (1 nm) tunneling barrier. As shown in Figure 39, the temperature dependence of the tunneling current was measured from 77 K to 355 K with no measurable dependence on temperature for either sample set. The overall tunneling current is shown to be dependent on the dielectric barrier with a Ti seeding layer allowed to naturally oxidize being shown to be a sufficient tunneling barrier for a direct tunneling dominant graphene TFET.

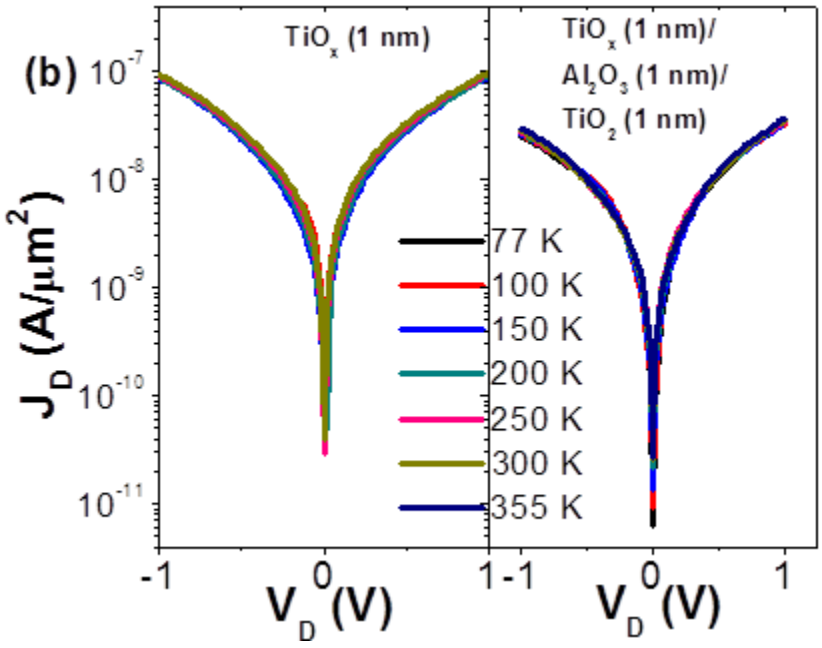

Figure 39 Tunneling current density for the TiO_x (1 nm) and TiO_x (1 nm)/Al_2O_3 (1 nm)/TiO_2 (1 nm) tunneling barriers. The temperature independent tunneling current indicates direct tunneling is the dominant tunneling mechanism.

While thinning the dielectric barrier results in direct tunneling being the dominant tunneling mechanism and a higher current density, further improvements are necessary to achieve NDR.

5.4 Grain Size Dependence

One potential source of disorder preventing negative differential resistance is the graphene. The main source of scattering in the graphene is the grain boundaries. In order to determine if the graphene itself is limiting the tunneling current in the graphene TFET, devices were fabricated with a 10 μm grain size and 200 μm grain size. The dimensions of the fabricated devices are 100 μm by 13 μm. The devices fabricated using the 200 μm grain size should have a minimal if any number of grain boundaries within the device.

The 10 μm grain size graphene was synthesized on copper foil by the standard CVD process. For the growth, no pre-treatments for the copper foil were done and a 10 minute anneal at 1000 °C was performed. Graphene from the same growth run used to fabricate devices was transferred to a silicon wafer and cleaned using a Ti sacrificial process. After cleaning, 2 nm of Al_2O_3 was deposited on the graphene using atomic layer deposition. The inert basal plane of the graphene does not react with the precursors while the grain boundaries and defect sites do. The preferential growth of the Al_2O_3 at the grain boundaries and defects allows measurement of the grain boundaries using atomic force microscopy.

Atomic force microscopy of the graphene sample after ALD is shown in Figure 40. The Al_2O_3 grows on the grain boundaries resulting in a height increase detectable by AFM. As seen in Figure 40, the grain size of the graphene measured by atomic force microscopy is ~10 μm. Several grain boundaries are highlighted in blue as a guide to the

eye. The larger grain size graphene was supplied by Professor Ruoff of UTA. Detailed characterization of the large grain size graphene and the synthesis process are discussed in detail elsewhere.[104]

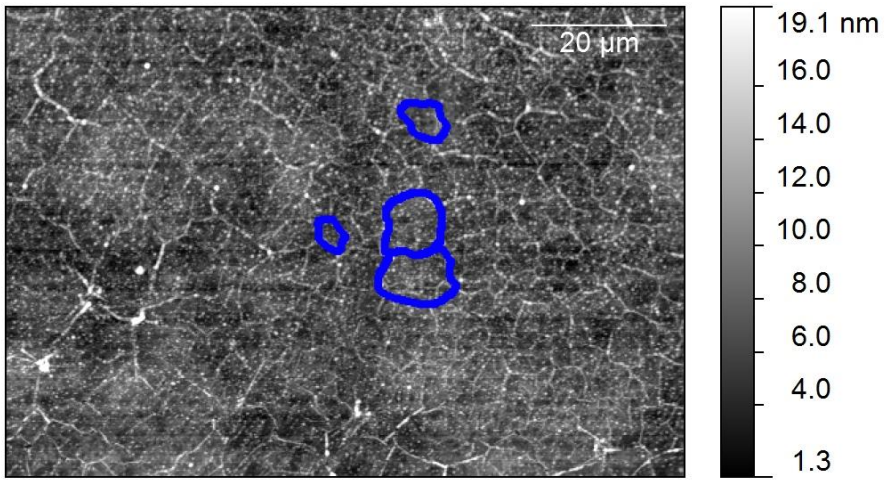

Figure 40 Atomic force microscopy image after deposition of Al_2O_3 on the graphene grain boundaries. Several graphene domains are outlined in blue as an aid to the eye. The graphene domains are of ~10 µm in size.

Graphene TFETs were fabricated from the two graphene samples with a TiO_x (1 nm)/Al_2O_3 (1 nm)/TiO_2 (1 nm) tunneling barrier. The tunneling characteristics of the graphene TFETs were measured under vacuum at ambient temperature after an 80 °C bake overnight to remove environmental adsorbates. The tunneling characteristics of the devices showed negligible dependence on the grain size of the graphene. Figure 41 shows the tunneling characteristics of the measured large grain and small grain graphene devices with the highest and lowest current density of their respective device set. As seen, the maximum current density is not dependent on the grain size of the graphene.

Furthermore, NDR is not present in any of the measured devices suggesting that the graphene is not the limiting mechanism for the graphene TFET operation.

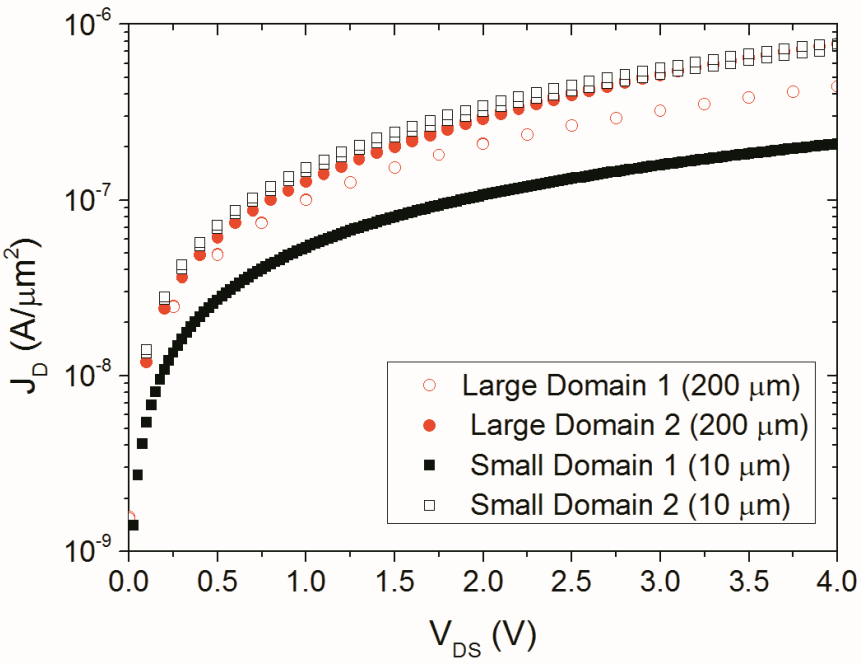

Figure 41 Tunneling current density of the large and small grain graphene. No significant difference in the maximum observed tunneling current is seen. The selected devices represent the highest and lowest observed tunneling current density in each device set.

5.5 Conclusion

Graphene TFETs based off of a variety of ALD dielectrics were fabricated and characterized. It was shown that the tunneling current of the graphene TFET can be engineered by engineering the tunneling barrier dielectric as demonstrated by the dependency of the symmetry of the tunneling current on the symmetry of the tunneling barrier. Thick tunneling barriers (> ~3 nm) result in trap assisted tunneling being the primary tunneling method for the graphene TFETs as evidenced by the temperature dependence of the tunneling current. By scaling the dielectric tunneling barrier thickness,

direct tunneling becomes the dominant tunneling mechanism for the graphene TFET. Despite direct tunneling being the dominant tunneling mechanism, NDR is not observed in the fabricated graphene TFETs. In order to determine if the graphene was limiting the tunneling current, graphene of small and large domain sizes (10 μm and 200 μm respectively) was used to fabricate the devices. No dependence on the graphene grain size was seen in the tunneling current suggesting the graphene is not limiting the tunneling characteristics. The substrate and dielectric barrier remain as two likely sources of disorder limiting the graphene TFET.

CHAPTER 6: GRAPHENE – MOLYBDENUM DISULFIDE – GRAPHENE HETEROJUNCTIONS

6.1 Introduction

Graphene grown by chemical vapor deposition (CVD) is a promising candidate for large-scale fabrication of a variety of electronic devices. However, the performance of graphene field effect transistors is limited by the high conductivity at the Dirac point (V_{Dirac}), which results in switching ratios less than ten at room temperature.[9, 257, 258] While a low switching ratio does not preclude the use of graphene-based electronics in high frequency and analog applications, applications such as logic require a higher switching ratio. Methods for achieving higher switching ratios by inducing a band gap in graphene have been demonstrated, such as the use of bilayer graphene, nanoribbons, and functionalization of the graphene.[147, 259, 260] An alternative approach to increasing the switching ratio of graphene-based devices is to utilize a tunneling based device architecture.[198]

2D heterostructures composed of graphene electrodes separated by a 2D tunneling barrier, such as hBN or MoS_2, have been recently reported.[198, 199, 261] The device is based off of the tunability of the density of states (DOS) in the graphene. A cross sectional view of the physical structure of the device is shown in Figure 42A. The device consists of two graphene sheets separated by a MoS_2 trilayer on a 300 nm thermal oxide grown on Si. The MoS_2 trilayer serves as a tunneling barrier and the SiO_2/Si substrate serves as the back gate. Applying a voltage between the top and bottom sheet (V_{DS} drives the current (I_d). The Si/SiO_2 serves as the back gate and a voltage applied to the Si (V_{bg}) modulates the Fermi level of the bottom layer graphene.

The operation of the device is depicted in the band diagram illustrated in Figure 42B. Applying a voltage to the back gate (V_{bg}) modulates the Fermi level of the bottom layer graphene due to the induced electric field (eV_{BOX}) across the bottom oxide. Applying a bias between the source and drain (V_{DS}) offsets the Fermi levels of the bottom and top graphene layer and induces an electric field across the interlayer (eV_{Int}). This opens a tunneling window due to the presence of available energy states in the opposing graphene sheet. The potential between the top and bottom graphene sheet drives the tunneling current. The magnitude of the current is controlled by the overlapping density of filled and available states in the bottom and top graphene layer respectively.

The barrier height between the graphene and tunneling barrier also influences the magnitude of the current and the switching ratio. The intrinsic barrier height for electrons (holes) can be calculated as the difference between the conduction (valence) band edge and the electron affinity (X_{Gr}) of the graphene. The intrinsic electron barrier height (Δ) for a graphene/MoS_2 system has been previously reported to be in the range of 0.29 eV to 0.44 eV dependent on the MoS_2 thickness.[262] Increasing the Fermi level of the graphene by application of a gate voltage will decrease (increase) the effective electron (hole) barrier height and vice versa. Increasing the Fermi level to levels approaching the conduction (valence) band edge can result in Fowler Nordheim tunneling and/or thermionic emission of electrons (holes) rather than direct tunneling as shown. The switching ratio for few layer h-BN ($\Delta \approx 1.5$ eV) has been shown to be ~50 while switching ratios as high as $\sim 10^4$ have been reported for few layer MoS_2.[198]

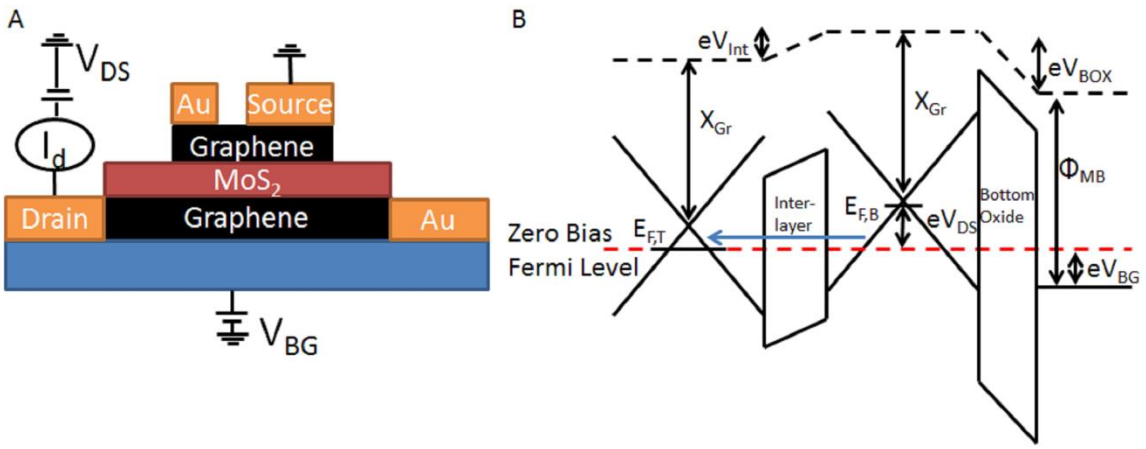

Figure 42 (A) Cross section of the Physical structure and circuit diagram of the tunneling heterostructure (not to scale). Current flows from one graphene sheet to the other across the MoS_2 tunneling barrier. The SiO_2/Si substrate serves as the back gate by applying a bias (V_{BG}) to the Si. (B) Band diagram depicting direct tunneling operation of the device. Depicted by the blue arrow, this results in tunneling from the bottom graphene layer to the top graphene layer. Φ_{MB} represents the work function of the Si back gate.

Most of the studies so far have focused on using exfoliated flakes for the graphene electrodes and 2D tunneling barrier [198, 199, 263]. For manufacturable electronics, it is required to have large-area materials that are compatible with photolithographic processes. While significant effort has been made on large-area synthesis of these materials [104, 264-267], there have been limited studies on the use of material synthesis techniques in an integrated heterostructure device fabrication process.

In addition to the possibility of a large on/off ratio for graphene based devices, recent reports for exfoliated vertical heterostructures have shown novel device properties including negative differential resistance (NDR).[268, 269] Theoretical models for these devices have shown the observance of NDR to be highly dependent on disorder within the system.[50, 253, 270, 271] Disorder can be induced by many factors including the quality of the materials, orientation of the layers, and contamination at the interfaces. The purpose

of this study is to understand the limitations of synthesized materials to achieving these device structures and associated tunneling characteristics.

Graphene-MoS_2-graphene vertical tunneling structures are fabricated using large-area synthesis techniques for all 2D materials. The MoS_2 tunneling barrier is either synthesized on a sacrificial substrate and transferred to the bottom-layer graphene or synthesized directly on CVD graphene. The impact of these fabrication processes on material structure is characterized using XPS and Raman. The transport properties of the individual graphene electrodes as well as the tunneling characteristics of the heterostructure are correlated to the physical measurements.

6.2 Materials Characterization

The device fabrication process is shown in Figure 43A-E; additional details are given in the Experimental section. Highly doped silicon wafers with 300 nm oxide formed by dry oxidation at 1000 °C were used as the device substrates. A monolayer of graphene grown by CVD on a copper foil was transferred to the Si/SiO_2 and subsequently patterned as the bottom electrode of the 2D heterostructure tunneling device shown in Figure 42A. Metal contacts were deposited onto the bottom layer graphene by e-beam evaporation and a lift-off process. The MoS_2 tunneling barrier was then either directly synthesized on the graphene bottom layer or transferred to the graphene bottom layer from a sacrificial growth substrate. To synthesize MoS_2, a Mo layer of 1 nm thickness was e-beam deposited onto the growth substrate and subsequently sulfurized resulting in trilayer MoS_2.[264, 272, 273] The direct synthesis of MoS_2 on graphene was performed at two different temperatures, 800 °C (low temp) and 1020 °C (high temp), to assess the impact of the synthesis temperature on the bottom layer graphene and MoS_2 quality. A second

layer of CVD grown graphene was transferred and subsequently patterned onto the tunneling barrier as the counter electrode of the tunneling structure and metal contacts were deposited onto the top layer graphene by e-beam evaporation and a lift-off process.

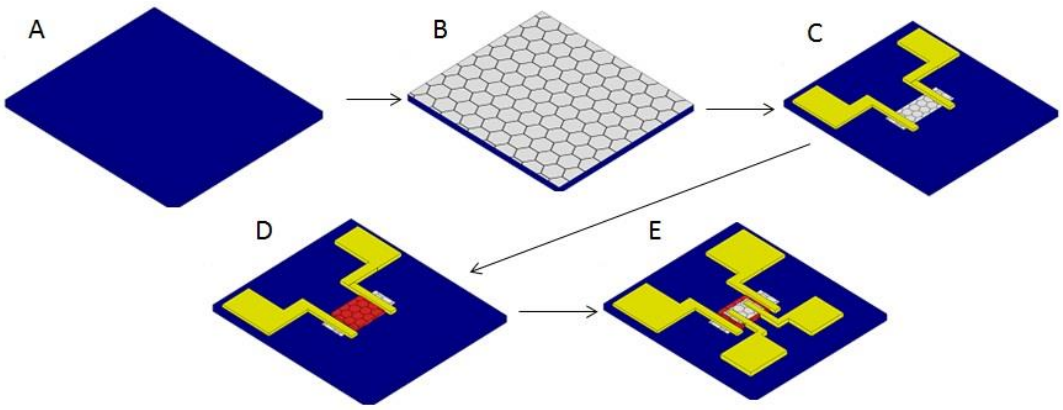

Figure 43 The fabrication sequence of the graphene-MoS_2-graphene devices (not to scale). (A) First a 300 nm thermal oxide is grown on Si. (B) Graphene is transferred to the SiO_2/Si substrate. (C) The graphene is patterned and metal contacts are deposited. (D) The MoS_2 interlayer is synthesized or transferred onto the graphene and patterned. (E) The second layer of graphene is transferred onto the interlayer, patterned, and metal contacts for the second layer are deposited.

In order to elucidate the impact of the direct synthesis of the tunneling barrier, XPS was used to assess the stoichiometry of the heterostructures, and Raman spectroscopy was used to evaluate the presence of defects in the bottom graphene layer. Figure 44A shows the Mo 3d and S 2s peaks and Figure 44B shows the S 2p peaks of the photoelectron spectra for MoS_2 synthesized on graphene at both low (Low Temp; black) and high (High Temp; red) temperatures as well as MoS_2 synthesized on SiO_2 and transferred to graphene. The S:Mo ratio was calculated using the normalized areas of the Mo 3d and S

2p peaks and found to be 2.06±0.02 for synthesis at 800 °C, 2.23±0.04 for synthesis at 1020 °C, and 1.98±0.04 for MoS_2 synthesized on SiO_2 and transferred to graphene. The stoichiometry of the transferred MoS_2 is consistent with previous studies on synthetic MoS_2 grown on SiO_2.[264, 274] The peak areas were normalized using an empirical sensitivity factor of 2.75 for the Mo 3d peak and 0.54 for the S 2p peak.[275] The Mo 3d peaks, S 2s, and S 2p peaks are consistent with the MoS_2 peak positions from the literature (Mo 3d 5/2 at 229.4 eV, Mo 3d 3/2 at 232.6 eV, S 2s at 226.6 eV, S 2p 3/2 at 162 eV, and S 2p 1/2 at 163.3 eV).[264] The larger ratio for MoS_2 synthesized on graphene could be due to either a higher sulfur content of the MoS_2 itself due to, for example, sulfur interstitials, or due to incorporation of sulfur into the underlying graphene.

The C 1s spectrum was analyzed to determine the cause of the increased S content. Figure 44C shows the C 1s spectra for intrinsic graphene before processing (Intrinsic; green), after synthesis of MoS_2 at low temperature (Low Temp; black), and high temperature (High Temp; red). Significant broadening of the C 1s spectrum is observed only in the high temperature synthesis of MoS_2. The C 1s spectrum for the bottom layer graphene after synthesis of MoS_2 at high temperature, shown in Figure 44D, shows clear broadening of the C 1s to the higher binding energy side of the C-C peak at 284.7 eV (C-C; red) when fit with Lorentzian line shapes of fixed position and a Shirley background. This is explained by the molybdenum metal acting as a catalyst to incorporate sulfur into the graphene giving rise to a C-S peak at 285.6 eV[276]

The C-S peak at 285.6 eV of the high temperature synthesis sample (Figure 44D) makes up 13% of the overall C 1s area and corresponds to a sulfur concentration of

$4.98x10^{14}$ cm^{-2}. This amount of sulfur incorporated into the graphene would account for the excess sulfur observed in the S:Mo stoichiometry. Based on a hexagonal lattice with a lattice constant of 3.12 Å [277], perfectly stoichiometric monolayer MoS_2 has a sulfur concentration of $1.58x10^{15}$ cm^{-2} (2 sulfur atoms per unit cell), meaning that stoichiometric trilayer MoS_2 would have a sulfur concentration of $4.74x10^{15}$ cm^{-2}. The calculated sulfur concentration from the C 1s spectrum is added to the expected sulfur concentration from a MoS_2 trilayer resulting in a total sulfur concentration of $5.24x10^{15}$ cm^{-2}. A calculated S:Mo ratio of 2.21:1 consistent with the S:Mo ratio of 2.23:1 calculated from the Mo 3d and S 2p XPS spectra is obtained. In summary, these results suggest that MoS_2 synthesized on graphene at 1020 °C has a stoichiometry ratio consistent with that synthesized on SiO_2 but with excess sulfur incorporated in the graphene. The C 1s spectra of the bottom layer graphene with MoS_2 synthesized at 800 °C (Figure 44C Low Temp; black) sample is comparable to bare (Figure 44C Intrinsic; green) graphene. This implies that any sulfur incorporation into the graphene at the reduced process temperature is below the detection limit of the XPS.

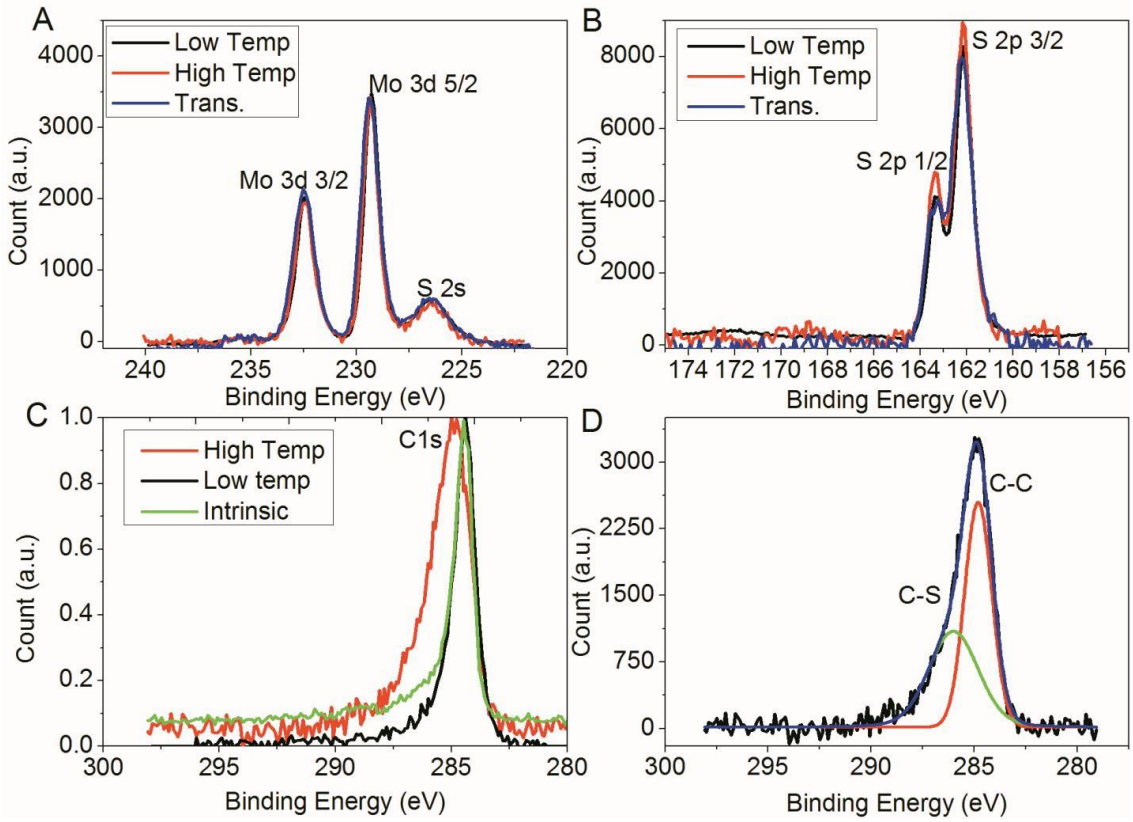

Figure 44 (A) The Mo 3d XPS spectra normalized to an empirical sensitivity factor of 2.75. (B) S 2p XPS spectra normalized to an empirical sensitivity factor of 0.54. The high temperature synthesis (High Temp; red) shows increased sulfur content.(C) The C 1s spectra normalized to the C 1s peak height. The C 1s spectrum of the high temperature sulfurization (High Temp; red) shows broadening on the high energy side of the C 1s spectra. (D) Deconvolution of the high temperature synthesis C 1s spectrum corrected with a Shirley background. The spectrum is consistent with a C-C component (red) at 284.7 eV and a C-S component (green) at 285.6 eV.

The MoS_2 Raman spectra for 3 different samples are shown in Figure 45A: the direct synthesis of MoS_2 on graphene, as synthesized on SiO_2, and transferred to graphene samples. The MoS_2 is extremely uniform and of similar quality for all conditions. The peak separation of the A_{1g} and E^1_{2g} peak is an ideal metric for determining the number of layers in the MoS_2.[278, 279] As more MoS_2 layers are added, the A_{1g} undergoes a blue-shift as result of suppressed atomic vibrations due to interlayer Van der Waals forces while the

E^1_{2g} undergoes a red-shift as a result of stacking induced structure changes or long-range Coulombic interlayer interactions.[278, 279] The combined shifting of the A_{1g} and E^1_{2g} peaks result in the peak separation of a monolayer of MoS_2 of 18.1 cm^{-1} increasing to a peak separation of 22.2 cm^{-1} and 23.3 cm^{-1} for bilayer and trilayer MoS_2 respectively.[278, 279] The as synthesized on SiO_2 spectra (Figure 45A On SiO_2; purple) shows a peak separation of 23.53 cm^{-1}, consistent with trilayer MoS_2.[264] After transferring the MoS_2 from the sacrificial SiO_2 substrate to the graphene (Figure 45A Transferred; blue), the peak separation increases to 25.67 cm^{-1}. The direct synthesis of MoS_2 on graphene (Figure 45A High Temp; black) shows a peak separation of 25.67 cm^{-1} as well, consistent with the transferred trilayer MoS_2 on graphene. The increased peak separation is caused by a suppression of the out of plane lattice vibrations due to the Van der Waal's interactions of the layers as well as strain introduced from the lattice mismatch of the graphene/MoS_2.[280] The similar peak separation of the transferred MoS_2 as well as the directly synthesized MoS_2 indicates no covalent bonding between the graphene and MoS_2 for both the transferred and synthesized MoS_2 conditions, consistent with the similar C 1s XPS spectra for the low temperature synthesis of MoS_2 and pristine graphene.

Figure 45B shows that the MoS_2 films in all cases are highly uniform, as measured by the Raman peak separation taken at 10 μm steps across a device channel from the transferred, high temperature, low temperature, and on SiO_2 samples. The average peak separation across all samples is 25.67±0.3 cm^{-1} when on graphene and 23.53 cm^{-1} when on SiO_2. A fluctuation of 1 monolayer of MoS_2 would result in a change of ~1 cm^{-1} in the peak separation suggesting the thickness uniformity of the MoS_2 is 3±0.3 layers across

the device channel. Assuming each monolayer to be ~0.66 nm, a conservative estimate of the thickness fluctuation of the MoS_2 is predicted to be ±0.22 nm.

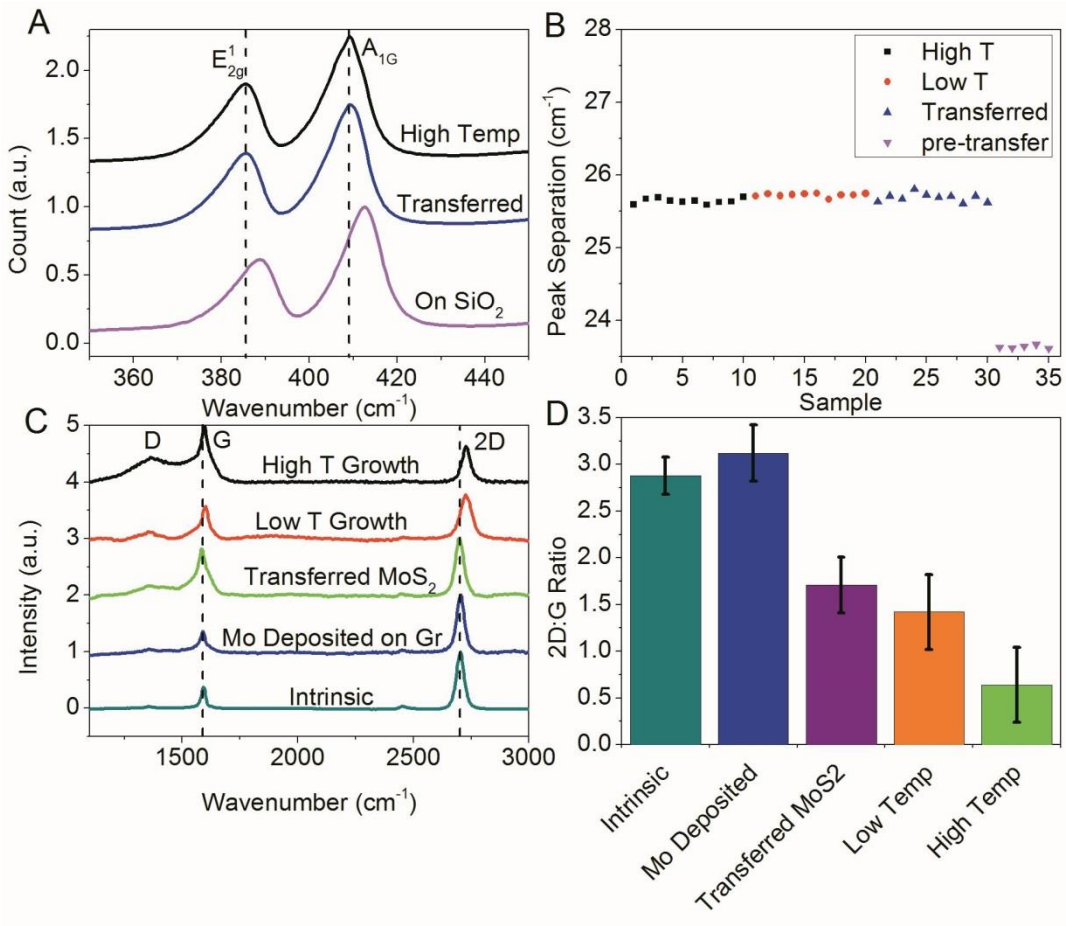

Figure 45 (A) Raman spectra of the A_{1g} and E^1_{2g} peaks of MoS_2 for each MoS_2 synthesis condition. The Raman spectra of the MoS_2 show a distinct shift in peak position of the A_{1g} and E^1_{2g} peaks when MoS_2 is on graphene. (B) Linear mapping of the MoS_2 at 10 μm steps. The MoS_2 is extremely uniform for all synthesis conditions as shown by the consistency in peak separation. (C) Graphene Raman spectra before and after each MoS_2 synthesis condition. The Raman spectra show high quality single layer graphene before processing. The graphene becomes more defective after MoS_2 synthesis. (D) The graphene 2D:G ratio for each condition in (C). The 2D:G ratio is greater than 2 before processing indicating single layer graphene. The reduced 2D:G ratio after MoS_2 synthesis indicates an increase in defect density.[281]

The graphene Raman spectra at selected process steps is shown in Figure 45C. For intrinsic graphene on SiO_2, the 2D:G peak ratio, shown in Figure 45D, is greater than 2:1 and no D peak at 1350 cm^{-1} is observed indicating high quality graphene prior to MoS_2 synthesis. After the sulfurization process, the graphene spectrum exhibits increased D peak intensity for both the low temperature and high temperature synthesis samples as well as a suppression of the 2D:G ratio which can be a result of large defect concentrations in the graphene.[281] A Van der Waal's interaction between the graphene and MoS_2 which suppresses the 2D:G ratio is also expected.[280] To account for this interaction, the Raman spectrum of MoS_2 transferred to graphene is used as a reference (Figure 45C-D Transferred MoS_2; green) and shows a 2D:G ratio of 1.51:1. The low temperature sulfurization (Figure 45C Low Temp; red) results in a 2D:G ratio of 1.44±0.3, with a value slightly suppressed compared to the transferred case, while the high temperature sulfurization (Figure 45C High Temp; black) results in a much smaller 2D:G ratio of 0.68±0.4. The larger suppression of the 2D:G ratio from the high temperature sulfurization is indicative of the introduction of a substantial defect concentration. The higher graphene defect concentration seen in the high temperature sulfurization is caused by the incorporation of excess sulfur into the graphene structure.

6.3 Electrical Performance

Electrical measurements were used to assess the quality of the individual graphene layers as well as the tunneling current of the fabricated tunneling junctions. The samples were baked within a vacuum probe station at 80 °C overnight to remove adsorbates from the atmosphere prior to measurement. Figure 46A shows the transfer curve of the individual graphene layers (drain current vs back gate voltage) at a fixed drain voltage of

0.02 V. The transfer curves were modelled using the constant mobility model developed by Kim et al.[193, 282]

Prior to the transfer/synthesis of the MoS_2 tunneling barrier, the graphene performance as determined by the extracted mobility (average of 2634±336 cm^2/V-s across 15 devices) is comparable to literature values for a single layer graphene field effect transistor on SiO_2 (GFET).[132, 193, 282, 283] The direct synthesis of MoS_2 on the graphene channel results in the Dirac point shifting to values well beyond the breakdown voltage of the device. The transfer of MoS_2 onto the graphene channel results in the Dirac point shifting to ~22 V, most likely caused by defects in the MoS_2 tunneling barrier.[284] The larger shifting of the Dirac point for devices with MoS_2 synthesized on graphene is most likely caused by additional defects associated with sulfur incorporation and catalytic etching of the graphene during the sulfurization process. The introduction of MoS_2 causes a reduction of the electron/hole mobility in the graphene. The current-voltage characteristic of the transferred MoS_2 shows a reduction in the hole mobility by a factor of 2 (average of 1215±127 cm^2/V-s across 15 devices) and electron transport is nearly entirely suppressed. The large suppression of the electron conductance in the graphene channel is consistent with previous reports of MoS_2 on graphene in which sulfur vacancies resulted in increased trapping of electrons.[285]

The devices with MoS_2 directly synthesized on graphene did not exhibit tunneling behavior (not shown) as a result of the large defect concentration and large shift of the Dirac point. The analysis here-in focuses on transferred MoS_2 interlayer devices which exhibit tunneling based behavior. A total of eight transferred devices exhibiting tunneling behavior were characterized. The following analysis is representative of the eight

devices. Figure 46B shows the exponential nature of the transfer curve on a linear scale, an indication that the current is tunneling based. Figure 46C shows the tunneling characteristic between the graphene layers at various back gate voltages. The current is observed to decrease with increasingly positive applied back gate voltages with a relatively weak (linear) dependence.

The tunneling behavior was modeled using an energy space formulation for the current density derived from the Bardeen Transfer Hamiltonian, the details of which were published previously.[253, 270] A p-type doping concentration of $1.6x10^{12}$ cm^{-2} and $3.6x10^{12}$ cm^{-2} for the top and bottom graphene sheets, respectively, was used to match the Dirac point observed in the single layer transfer characteristics. A MoS_2 interlayer thickness of 1.8 nm was used, consistent with three layers of MoS_2, resulting in an interlayer capacitance of $1.97x10^{-6}$ F/cm^2. The electron affinity of the MoS_2 was set to 4.2 with a tunneling effective mass of 0.4 for holes and electrons in the tunneling barrier.[262] The graphene layers were modeled with an electron affinity of 4.5.[262] The valence band offset of the MoS_2 and graphene was varied from 1 eV to 1.7 eV with the best fit occurring for an offset of 1.5 eV. A coherence length of 1 nm was used for the best fitting results.

The tunneling model does not directly take into account an additional density of states due to defects. The lateral transport measurements show that the electron conductance is highly suppressed due to defects. The best fit of the experimental results requires suppression of tunneling from the conduction bands of the top and bottom layer. The validity of the fit is determined by comparing the value of the prefactor of the tunneling equation, shown in the experimental section, to experimental values for similar structures.

Including the conduction band tunneling results in the prefactor of the model, M_{B0}, to be a non-physical value ($1x10^{-6}$). Suppressing the conduction band current results in a M_{B0} value (0.001) similar to experimental values from the literature, indicating a valid fit.[271] Similar to the suppressed lateral transport of electrons in the device structure seen in the transfer curve (Figure 46A Trans. MoS_2; black), the increased trapping of electrons due to sulfur vacancies results in a suppression of electrons tunneling from the conduction band. Furthermore, as depicted schematically in figure 42A and 43E, the device structure relies on lateral transport in the bottom graphene layer before reaching the active tunneling area of the device. The reduced electron mobility limits the lateral transport which further impedes electrons tunneling from the conduction band.

Figure 46D shows the tunneling behavior of the graphene-MoS_2-graphene heterojunctions and the theoretical fitting using the above parameters. As the applied back-gate voltage is swept to more positive values, the conduction band in the bottom graphene sheet becomes more populated. Due to the reduced electron conductance in the graphene channel, the tunneling of electrons from the conduction band of the bottom layer is suppressed. The more positive gate bias pushes the tunneling window further into the conduction band of the graphene sheets resulting in a lower current density due to the suppression of electron tunneling from the conduction band. A relatively weak dependence (linear) on the back gate is observed with a more positive gate bias resulting in reduced current densities. A maximum switching ratio of ~100 was observed between an applied gate bias of -30 V (on state) and 30 V (off state) at a fixed V_{DS} = 0.2 V. This result is much smaller than the observed switching ratio of ~10^4 for exfoliated structures using MoS_2 as the tunneling barrier.[198] The reduced switching ratio is most likely a

result of the high defect density in the graphene and increased defects in the MoS_2 layer. The theoretical simulations with the conduction band current suppressed agree well with the experimental results.

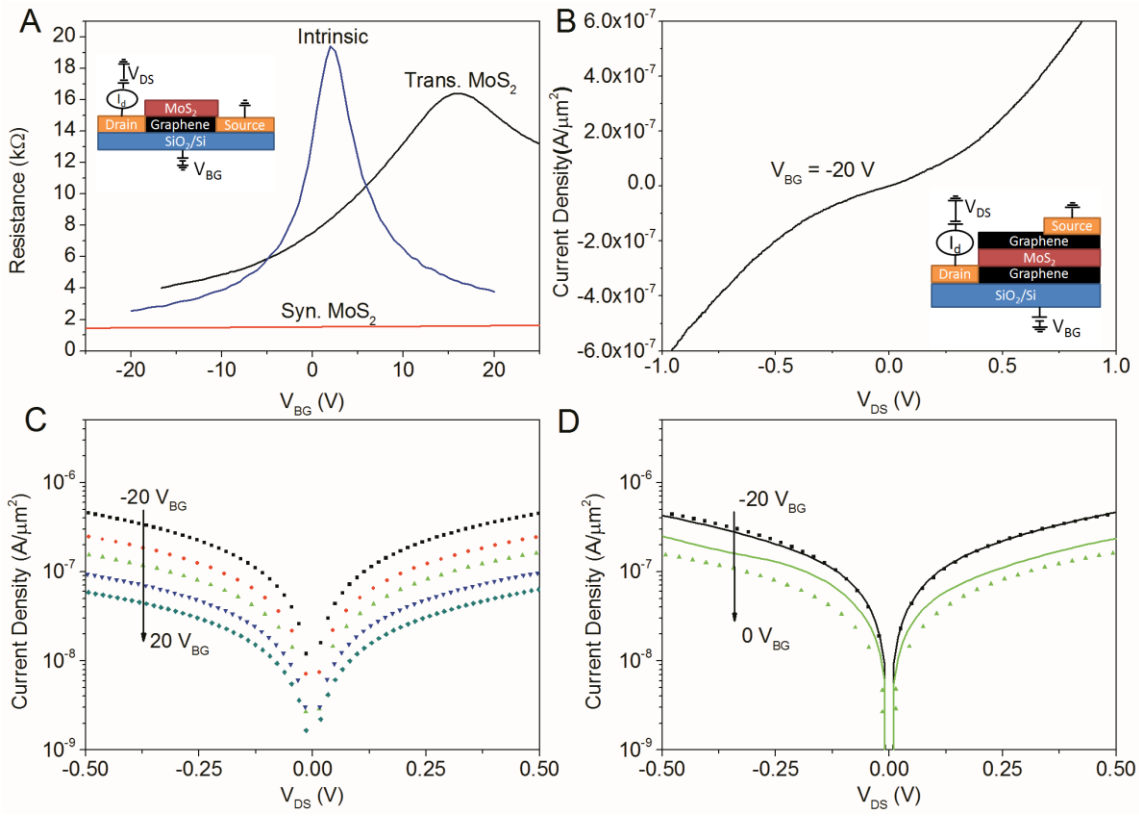

Figure 46 (A) Transfer characteristics of the bottom layer graphene at a constant drain bias (V_{DS}) of 0.02 V. The inset depicts a cross sectional view of the device and the measurement circuit. (B) The tunneling characteristics of a graphene-MoS_2-graphene device with an applied back gate voltage of -20 V on the linear scale. The inset depicts a cross sectional view of the device and the measurement circuit. (C) Experimental results for a device made from an MoS_2 interlayer transferred to graphene with an applied back gate of -20 V (top curve) to 20 V (bottom curve) in 10 V steps. (D) Simulations (solid lines) and experiment results (dotted lines) of an applied back gate voltage of -20 V (black) and 0 V (green). The theoretical results agree well with the shape and general behavior of the experimental results.

6.4 Conclusion

In conclusion, graphene-MoS_2-graphene tunneling junctions were fabricated using only large-area synthesized 2D materials. The MoS_2 tunneling barrier was shown to be a highly uniform trilayer (thickness of 1.8±0.22 nm) across the entire device area based off of the uniformity of the Raman compared to a known trilayer sample transferred to graphene. This indicates the graphene had no impact on the synthesis of MoS_2. The direct synthesis of MoS_2 on graphene at 1020 °C resulted in the incorporation of ~$5x10^{14}$ S atoms-cm^{-2} into the graphene lattice as evidenced by XPS. Raman spectroscopy was used to evaluate the relative disorder in the graphene structure and showed that MoS_2 synthesis at reduced temperatures was less detrimental to the underlying graphene. The presence of Mo on graphene increased the sulfur incorporation compared to bare graphene exposed to sulfur.

The conductance of the tunneling junctions based on transferred large-area MoS_2 was found to decrease as a more positive gate bias was applied reaching a maximum switching ratio of ~100. This value is much lower than the switching ratio of ~10^4 observed in exfoliated structures, but an order of magnitude greater than single layer graphene structures. The reduced tunneling current compared to exfoliated structures is a result of suppressed tunneling of electrons from the conduction band of the graphene sheets, as confirmed by theoretical simulations based on the Bardeen transfer Hamiltonian.[253, 270] The suppressed electron tunneling is a result of the reduced lateral electron transport of the graphene caused by trapping due to sulfur vacancies in the MoS_2. The direct formation of MoS_2 was also shown to negatively impact the underlying SiO_2 substrate as shown by the shifting of the graphene Dirac point to beyond the

breakdown voltage of the device as a result of defect formation due to the incorporation of sulfur. We have shown that the impact of the MoS_2 synthesis on the underlying graphene can be reduced by decreasing the synthesis temperature of the MoS_2, but further process improvements are required to fully eliminate the introduction of defects into the underlying device structure.

CHAPTER 7: HEXAGONAL BORON NITRIDE – GRAPHENE – HEXAGONAL BORON NITRIDE – GRAPHENE HETEROJUNCTIONS

7.1 Introduction

The carrier mobility of graphene is heavily dependent on the materials in contact with the graphene. The mobility of graphene can be limited by scattering introduced from charged surface states, impurities, substrate roughness, and phonon modes of the contacting materials.[132, 189] Charged impurities at the graphene-substrate interface can also induce doping of the graphene and cause a significant shift in the charge neutrality point of the graphene. Recently, the use of hexagonal boron nitride (hBN) has been shown to be an ideal substrate for improving the carrier mobility of graphene.[286]

An isomorph of graphene, hBN has a boron atom occupying the A sub lattice while a nitrogen atom occupies the B sub lattice of the graphene Bernal structure. With a large bandgap of 5.97 eV and a lattice mismatch of only 1.7% with graphene, hBN is an ideal insulating substrate for graphene.[287] The 2D nature of hBN further results in an inert surface free of dangling bonds, surface charge traps, and an atomically smooth surface which suppresses the rippling in graphene. With a permittivity of 4.2 and a breakdown voltage of 0.7 V nm^{-1}, hBN is comparable in dielectric quality to that of SiO_2. Furthermore, the large energy of hBN phonon modes results in less scattering in the graphene.[286, 287]

7.2 Physical Characterization of Materials

The fabricated devices were made from large area materials synthesis techniques and fabrication processes. Graphene monolayers were grown using a CVD synthesis process on a copper foil. The hBN multilayers were grown on a separate copper foil using a CVD synthesis process. The hBN multilayers were transferred to a thermally grown SiO_2/Si wafer (270 nm oxide thickness) to act as a buffer layer between the graphene and underlying SiO_2 substrate using the previously described wet transfer process. The underlying SiO_2/Si substrate serves as the back gate of the device. A graphene monolayer was transferred onto the hBN using the same wet transfer process. The graphene was patterned and Ni/Au (20/50 nm) contacts were deposited onto the graphene. A second hBN multilayer synthesized by CVD on copper foil was transferred using the wet transfer process on top of the graphene. The second hBN multilayer serves as the interlayer dielectric for the fabricated tunneling structures. A second graphene monolayer was transferred to the hBN/Gr/hBN stack to serve as the top electrode. Ni/Au (20/50 nm) contacts were deposited on to the second layer of graphene. A device similar to the device depicted in Figure 39A was fabricated with similar operating principles.

After transferring the hBN to the SiO_2/Si substrate, XPS was used to determine the quality of the CVD grown hBN. Shown in Figure 47, the synthesized hBN shows a B 1s peak at 191.6 eV and a N 1s peak at 398.2 eV.[288] The peak locations are consistent with reports of the hBN XPS spectra from the literature. The stoichiometry of the synthesized hBN was calculated from the normalized peak area ratios of the B 1s and N 1s peaks. The peaks were normalized with empirical sensitivity factors of 0.13 and 0.42 for the B 1s and N 1s peak respectively.[275] The calculated stoichiometry is 1.09±.02. The

stoichiometry was also calculated from Scofield relative sensitivity factors of .49 and 1.8 for the B 1s and N 1s respectively giving a stoichiometry of 0.96±.02.[289] The average stoichiometry from the two sets of sensitivity factors is 1.02±0.07. The near ideal stoichiometry of the hBN indicates high quality hBN with minimal interstitials or vacancies.

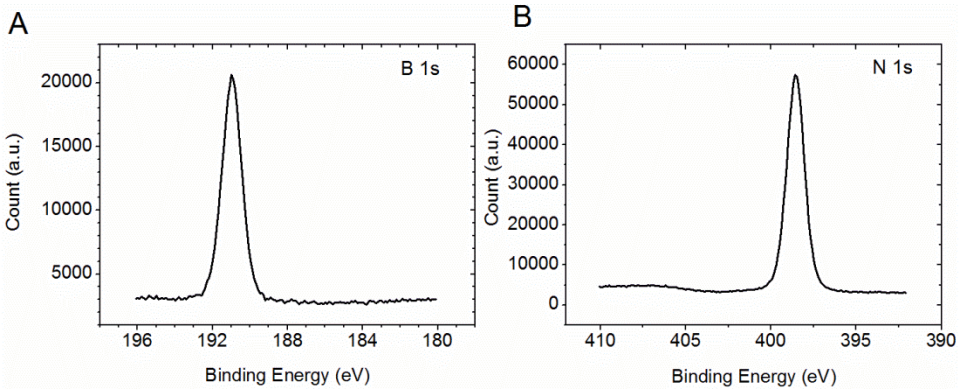

Figure 47 (A) XPS B 1s spectrum of the CVD hBN. (B) XPS N 1s spectrum of the CVD hBN

SKPM was used to compare the surface charge fluctuations of the hBN in comparison to the surface charge fluctuations of the underlying SiO_2 as shown in Figure 48. The surface charge fluctuations of the hBN (41 mV_{rms}) are reduced by a factor of ~3 compared to the surface charge fluctuations of the SiO_2 (144 mV_{rms}). The coherence length associated with the surface charge fluctuations is determined using the height to height correlation function.[290] The coherence length of the hBN is found to be 60 nm while the coherence length on the SiO_2 is determined to be 20 nm. This indicates that in the case of the surface charge fluctuation being the dominant scattering mechanism, the coherence length of the device will be limited by the substrate to either ~60 nm in the

case of hBN or ~20 nm in the case of SiO_2. Both substrates limit the coherence below the desired value of 100 nm. While CVD hBN is currently a drastic improvement over a SiO_2 substrate, improvements to the hBN quality are required for further device improvements.

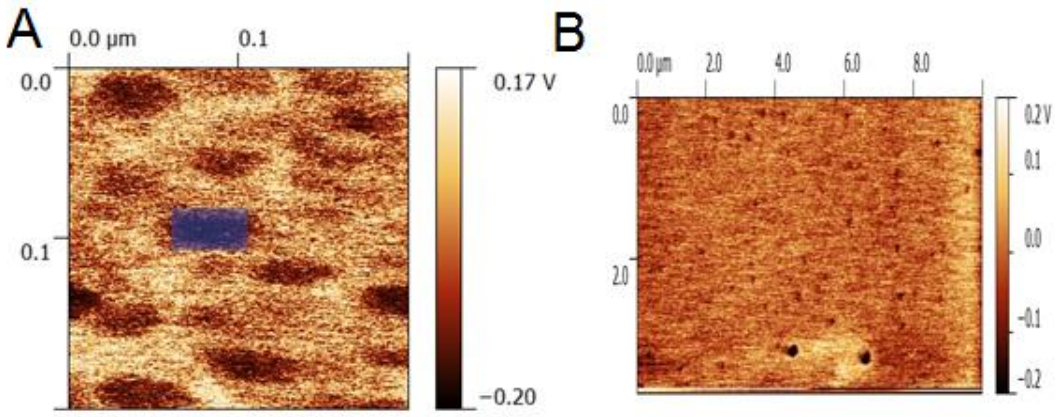

Figure 48 (A) SKPM measurement of the hBN surface. The V_{RMS} is 41 mV. The local V_{RMS} in the blue outlined region is 31 mV (B) SKPM measurement of the SiO_2 surface. The V_{RMS} is 144 mV.

The surface topography of the transferred hBN as measured by AFM is shown in Figure 49. The measured topography shows local fluctuations of 2-3 layers in the hBN thickness which correspond to the surface charge fluctuations of the hBN. This indicates the coherence length of the surface charge potential can be increased by improving the uniformity of the grown hBN. The surface charge fluctuations of the locally thicker hBN is 31 mV_{RMS} compared to the fluctuation of 41 mV_{RMS} indicating a thicker and more uniform hBN would provide a better buffer layer for graphene. In comparison, the surface of the SiO_2 is highly uniform indicating the measured surface charge potential of the SiO_2 is intrinsic to the dielectric and improvements to the processing conditions are unlikely to result in the SiO_2 being a suitable substrate to achieve NDR.

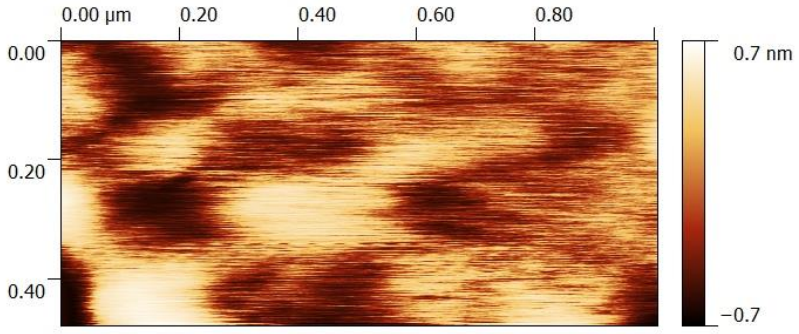

Figure 49 AFM topography image of the hexagonal boron nitride surface. Local fluctuations of ~2-3 layers are observed and correspond to the large charge fluctuations observed in the SKPM measurement.

7.3 Graphene on hexagonal boron nitride

Electrical measurements of the graphene were performed to assess the evolution of the graphene performance at each processing step. After transferring the graphene onto the hBN substrate, a maximum mobility of 7680 $cm^2V^{-1}s^{-1}$ was achieved. This is a significant improvement over the typical mobility of ~2000-3000 on SiO_2. The improved mobility is a direct result of the reduced scattering due to the higher energy phonon modes of the hBN and reduced surface potential fluctuation.

While an overall improvement is seen, fluctuations in the thickness of the hBN buffer layer are seen to greatly impact the device performance. Thickness fluctuations of up to 12 layers (~4 nm) are observed on the macroscopic scale for the transferred hBN. Graphene devices can either straddle multiple patches of hBN as shown in Figure 50A or fall within a single hBN patch shown in Figure 50B. The Raman spectra of the devices shown in Figure 48A-B are shown in Figure 50C. The Raman spectrum of the device straddling multiple hBN patches exhibits 2D and G peak widths of 46 and 36 cm^{-1} and peak positions of 2705 and 1590 cm^{-1} respectively. In comparison, the graphene device

which falls in a single hBN patch has peak widths of 33 and 16 cm^{-1} with positions of 2704 and 1593 cm^{-1} for the 2D and G peak respectively. The increased peak widths for the device straddling multiple hBN patches is an indication of increased strain in the graphene layer.[291]

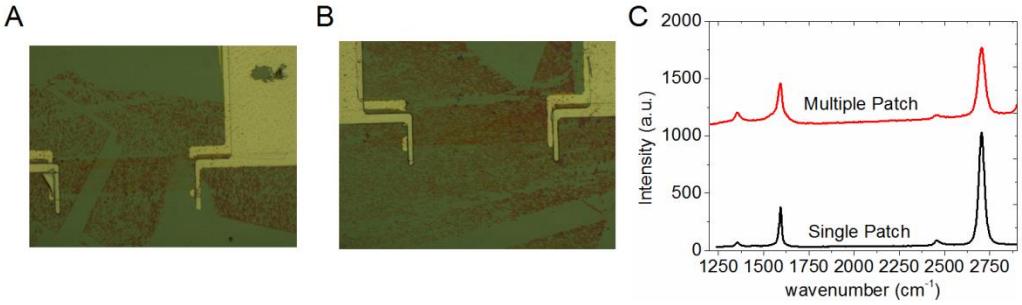

Figure 50 (A) Fabricated device which straddles multiple hBN patches. (B) Fabricated device which is in a single hBN patch. (C) Raman spectrum of A (Multiple Patch) and B (Single Patch).

A comparison of the electrical performance of these two devices is shown in Figure 51A. The graphene device which falls within a single hBN patch has a mobility of 7680 $cm^2\ V^{-1}s^{-1}$ while the graphene device which straddles multiple patches has a mobility of 1764 $cm^2\ V^{-1}s^{-1}$. As shown in Figure 51B, a device which straddles two hBN patches has a mobility of 3676 $cm^2\ V^{-1}s^{-1}$. The mobility of 10 measured devices is shown in Figure 51C. The mobility of these 10 devices as a function of the number of hBN patches straddled by the device is shown in Figure 51D. The devices which straddle a single hBN patch are shown to have significantly higher mobilities of 5663±1804 cm^2/Vs. Devices which straddle two hBN patches have reduced mobilities of 3918±575 cm^2/Vs compared to the single patch devices. Devices which straddle three or more patches show negligible

improvement over devices on SiO_2 with mobilities of 2353±832 cm^2/Vs compared to 2235±336 cm^2/Vs for graphene devices on SiO_2.

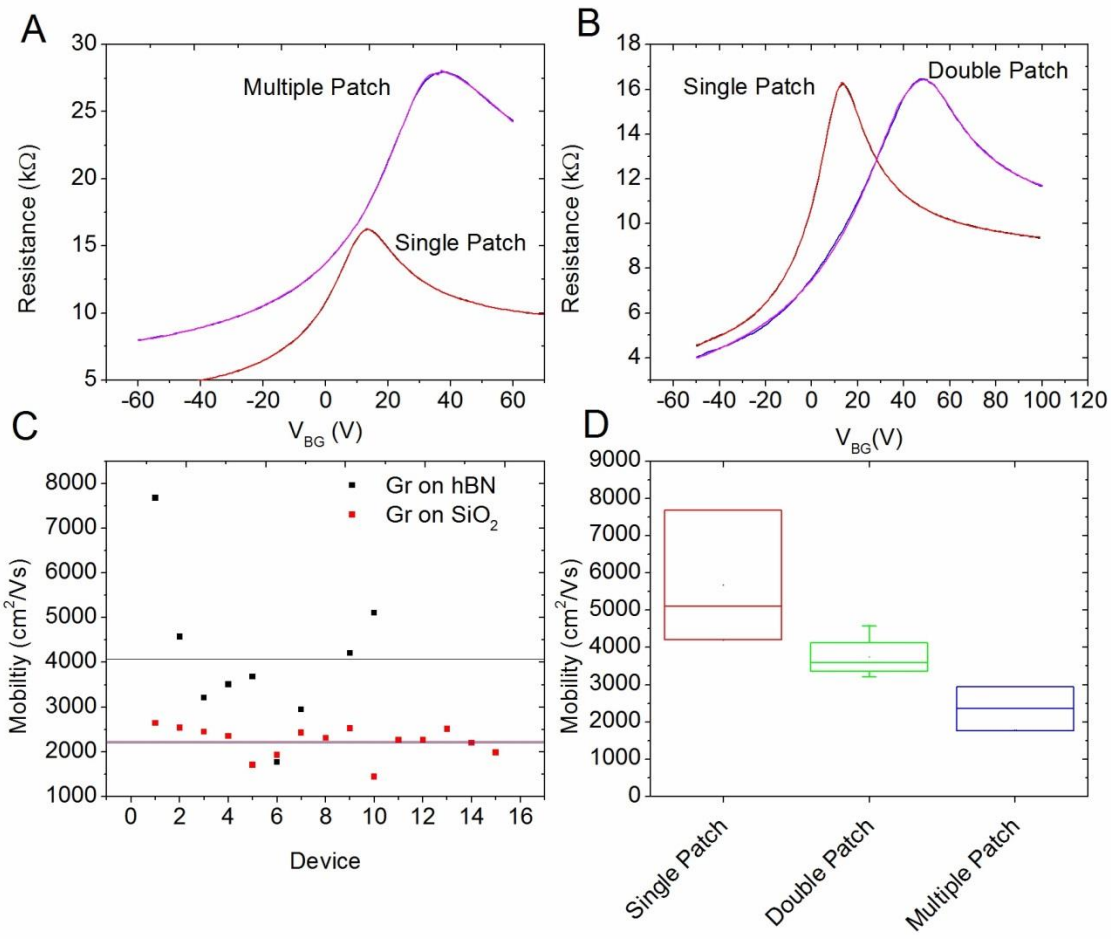

Figure 51 (A) Transfer curve comparison between a graphene device on a single patch of hBN to a device that straddles three separate patches. (B) Transfer curve comparison between a graphene device on a single patch of hBN to a device that straddles two patches. (C) Mobility of 10 measured graphene on hBN devices compared to graphene on SiO_2. (D) Mobility comparison between graphene on a single patch of hBN (single patch), graphene straddling two patches (double patch), and graphene straddling three or more patches (multiple patch).

After the addition of the hBN interlayer on top of the graphene, the mobility of the graphene is reduced. In the case of the device shown in Figure 7.3.1, the mobility is

reduced to 4200 cm^2 $V^{-1}s^{-1}$ from 7680 cm^2 $V^{-1}s^{-1}$. The reduction in mobility is caused by the additional disorder introduced by the hBN interlayer. The local thickness fluctuations as well as the surface charge fluctuations of the hBN interlayer impact the graphene similar to the impact seen from the hBN buffer layer under the graphene.

After characterizing the bottom layer of graphene, a second layer of graphene was transferred to the device stack and tunneling measurements were performed. The tunneling performance of the devices is shown in Figure 52. The tunneling performance of the devices with an hBN buffer layer is compared to similar devices directly on SiO_2. No significant change in the tunneling characteristics of the devices is seen suggesting the quality of the hBN is insufficient to noticeably impact the tunneling characteristics of the device. Also plotted in Figure 52 are the current-voltage characteristics of exfoliated Gr-hBN-Gr devices from the literature.[198] The results show gate-controlled tunneling comparable to previously reported exfoliated structures in the limit of no momentum conservation.

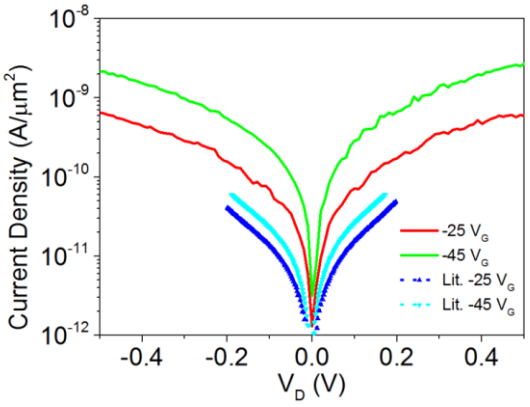

Figure 52 Tunneling current density on the log scale for the fabricated tunneling junctions compared to similar literature tunneling junctions utilizing exfoliated materials.[198]

7.4 Conclusions

Graphene tunneling junctions with an hBN buffer layer were fabricated and compared to results from the literature. XPS showed B 1s and N 1s peaks to be consistent with hBN from the literature. The normalized area ratio of the B 1s and N 1s peaks was used to show the hBN buffer layer was stoichiometric. The hBN buffer layer was shown to reduce the surface potential fluctuations compared to the traditional SiO_2 substrate by SKPM. The use of the CVD synthesized hBN buffer layer was shown to significantly increase the mobility of the graphene layers when the underlying hBN buffer layer was uniform. Thickness fluctuations of the hBN buffer layer were shown to lower the mobility of the graphene layers and in the extreme case diminish the mobility below that of graphene on SiO_2. Despite the improved transport within the graphene layer, the tunneling characteristics of the fabricated tunneling junctions were found to be comparable to literature values at the limit of no momentum conservation. Further improvements to the hBN synthesis process to reduce thickness fluctuations will be necessary to further improve the graphene tunneling junction's performance.

CHAPTER 8: FUTURE WORK

The major focus of this work was the development of an integrated materials synthesis and fabrication process for fabricating graphene SymFET structures. The impact of the fabrication process and materials based disorder on the performance of the graphene SymFET was investigated. Future work to further improve the performance of the graphene SymFET could include the following:

- CVD Graphene rivaling the performance of exfoliated graphene has been synthesized. CVD synthesized hBN was shown to have significant thickness fluctuations which negatively impact the graphene performance. The quality of CVD synthesized graphene is sufficient. The complimentary materials to the graphene are currently limiting the SymFET performance. The development of complimentary materials to graphene (hBN, MoS_2, WSe_2, etc.) are necessary to further improve the SymFET device performance.

- The wet transfer process of the tunneling barrier and top graphene layer introduce contamination to the device structure. Water trapped between the layers due to the wet transfer process is one potential source of disorder which was not investigated in this study. To eliminate this potential source of disorder, the development of an in situ synthesis technique of the interlayer dielectric and top graphene layer directly onto the bottom graphene layer would be ideal. One pathway for the direct synthesis of MoS_2 on graphene has been explored and the development of a lower processing temperature for

MoS_2 synthesis with increased grain sizes may allow MoS_2 to be a viable tunneling barrier for the SymFET structure.

- The orientation between the graphene layers has been theoretically and experimentally shown to impact the tunneling characteristics of the SymFET structure. A method using Raman spectroscopy to determine the misorientation between two graphene layers has been proposed. An evaluation of whether or not the misorientation of two graphene layers separated by a thin dielectric can be determined by Raman spectroscopy is needed.

CHAPTER 9: CONCLUSIONS

The goals of the work presented in this dissertation were (i) to develop a materials processing and integration scheme for large-area two dimensional materials (ii) determine the impact of contamination and disorder on vertical and horizontal electrical transport in graphene based vertical heterostructures (iii) elucidate the role of material synthesis/processing on the introduction of disorder in the vertical heterostructure and how this disorder impacts electrical transport.

Process flows for fabricating the graphene SymFET structure from large scale highly uniform 2D materials were developed. The developed processes include patterning techniques, metal depositions, dielectric depositions, wet etches, plasma etches, and process contamination removal techniques. The developed fabrication process was used to fabricate the SymFET structure and the materials based disorder in the structure was investigated.

Graphene SymFET structures with ALD based tunneling barriers were fabricated and the tunneling characteristics were characterized. The tunneling current of the fabricated structures was shown to be controlled by the designed band structure of the interlayer dielectric. Trap assisted tunneling was found to dominate the tunneling characteristics at large tunneling barriers while direct tunneling was shown to be dominant for dielectric barriers below 3 nm in thickness. Despite the dominance of direct tunneling, NDR was not observed and the graphene was investigated as a potential limiting source. No dependence of the tunneling characteristics on the graphene grain size was observed suggesting the limiting factor was likely to be the dielectric or substrate.

ALD based dielectrics suffer from the need of seeding layers for deposition on graphene and are a potential source for increased disorder in the SymFET structure. MoS_2 was investigated as a potential replacement for the ALD based dielectrics. The direct synthesis of MoS_2 on graphene was shown to be highly detrimental to the graphene. The graphene was shown to have no impact on the synthesis of the MoS_2. Temperature dependence was found on the disorder introduced by the MoS_2 synthesis process suggesting a reduced temperature synthesis process for MoS_2 is needed. The tunneling characteristics of a MoS_2 interlayer transferred to the graphene SymFET structure were investigated. The transferred MoS_2 film was shown to introduce significant charge trapping to the structure which reduced the tunneling current density. The most likely source of defects attributing to the trapping is the grain boundaries of the MoS_2. Larger domain size MoS_2 should be synthesized for future studies.

The impact of the substrate on the SymFET structure was investigated by introducing an hBN buffer layer between the bottom graphene sheet and the underlying SiO_2 substrate. The hBN buffer layer was shown to improve the graphene electrical characteristics in more uniform hBN areas. The improved characteristics are due to the reduced potential fluctuations on the surface of the hBN compared to the surface of the SiO_2 and the higher energy phonon modes of the hBN not introducing as much scattering as the lower energy SiO_2 phonon modes. When large thickness fluctuations were present under the graphene film, the graphene electrical characteristics were shown to be similar and in some cases inferior to graphene on SiO_2. An hBN tunneling barrier was then transferred to the graphene and the SymFET structure was fabricated. The hBN was shown to be of insufficient quality to realize NDR. The tunneling current densities of the

large-area material fabricated structures were shown to be of comparable quality to exfoliated materials in the limit of no momentum conservation. The quality of the materials complimentary to the graphene was found to be the limiting variable of the SymFET performance.

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