A COMPACT SWITCHING MODE CLASS-F POWER AMPLFIER DESIGN

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A COMPACT SWITCHING MODE CLASS-F POWER AMPLFIER DESIGN

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LIST OF SYMBOLS AND ABBREVIATIONS

η	Efficiency
θ	Angle in Radians
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
JFET	Junction Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MESFET	Metal Semiconductor Field Effect Transistor
pHEMT	pseudomorphic High Electron Mobility Transistor
PAE	Power Added Efficiency
HFSS	High Frequency Structural Simulator
Balun	Balanced Unbalanced

SUMMARY

Even though there had been extensive research in Switching Mode Power Amplifier design their applications at industry level are quite limited. This is because a Fully-Integrated Switching Mode Power Amplifier using conventional active devices such as Bipolar Junction Transistors (BJT) or Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is challenging due to the inherent design challenges in the Switching Power Amplifier design.

A Fully-Integrated Differential Class-$F_{2,3}$ Power Amplifier design is explored for this Thesis research. This Power Amplifier has a maximum theoretical efficiency of 90.7% but this value is reduced because of the switching nature of the active device, parasitic effects associated with layout and the quality factor of the passive components used. Waveform shaping required for a Class-F Power Amplifier is done using the stray inductances within a non-ideal transformer instead of individual inductors. This techniques effective reduces the foot prints of two inductors for the tuning network design and make a Fully-Integrated solution more practical.

Ideally, the harmonic tuning network must provide open termination at 3rd harmonic and short at 2nd harmonic, but the quality factor of the passive components used would cause certain amount of mismatch in the harmonic tuning network. The topology of the tuning network that makes use of the stray inductance also considers some approximations for the harmonic tuning which results in a loss of efficiency. However, this loss in efficiency can be an acceptable trade-off for the reduced inductor footprint.

Harmonic Tuning Network simulations were run on Agilent's Advanced Design System and Cadence Virtuoso Analog Design Environment (ADE). Layout of the active

devices and capacitors were done using Cadence Virtuoso Layout suite and passive components including inductors and transformers were designed using Ansys High Frequency Structural Simulator (HFSS) Electromagnetics Suite 16.1.

In conclusion, a maximum output power of 24.5dBm was measured with 62% efficiency at 5GHz operating frequency. The loss in efficiency from theoretical value of 90.7% was expected because of the losses associated with design but a Full-Integrated Class-F Power Amplifier solution is made possible.

CHAPTER 1

INTRODUCTION

1.1.Power Amplifier Applications

Power Amplifiers have been the integral part of RF/Wireless Communication Systems ever since their inception. The distance over which an RF signal can be transmitted is directly proportional to the power of the transmitted signal, which necessitates the use of Power Amplifiers in RF Systems. A Power Amplifier basically converts DC Power into RF Power based on the input driving signal [1]. As they consume DC Power inorder to provide the required amplification they are the most power hungry blocks in the entire RF system (Receiver included).

Over the past decade we have seen an explosive growth in hand held devices that use complex modulation schemes for data transmission and have limited battery life. Power Amplifier design for such devices is more challenging as the amplifier has to be linear enough to handle the complex modulation schemes and also has to be efficient because of limited battery life of the devices. Providing a single amplifier solution for all the wireless applications is a daunting task because of the trade-offs involved with Power Amplifier design and 50 years of research in this area have shown such solutions are not cost efficient and impractical at industry level especially for the applications discussed above.

1.2.Performance Metrics in Power Amplifier Design

Ideally a Power Amplifier must have a very large gain, large output power, consume minimum amount of DC power and has to be highly linear. A Power Amplifier converts DC Power into RF Power, as such it is necessary for the Amplifier to be efficient enough to convert maximum amount of DC Power into RF Power. Efficiency of a Power Amplifier is the ratio of RF Power generated to the DC Power consumed [1], η =

P_{out}/P_{DC}. Power Added Efficiency which is defined as the PAE = $(P_{out} - P_{in})/P_{DC}$ [1], also takes input power consumed into consideration and thus quantifying both Gain and DC Power consumed by the Amplifier.

The output response of a generic Power Amplifier is non-linear that can be modelled with n^{th} order polynomial and leads to effects such as Gain Compression and Inter Modulation. Saturated Power is the maximum power a Power Amplifier can generate (P_{sat}) for a fixed supply voltage and load impedance. 1-dB Compression Point ($P_{1dB)}$ is defined as the Power at which Gain reduces by 1 dB and is used to quantify the Gain Compression [2]. Third Order Intercept Point IIP3 is the point where power of the fundamental component is equal to the power of third order inter modulation products [2]. These performance metrics are used as Figure of Merits in Power Amplifier design.

1.3.Power Amplifier – Classes

In low power applications Efficiency becomes the critical performance metric and in applications using complex modulation schemes Power Amplifier must be highly linear and in case of High Frequency applications (mm-wave) Gain becomes a critical performance metric. Several Amplifier Classes have been proposed and each Class has its own set of merits and drawbacks to cater the needs of different applications. A particular Amplifier Class is chosen based upon the type of application the Power Amplifier is being used for.

However different the amplifiers performance may be, all the Amplifier Classes have a similar topology as shown in the Figure 1, with a Supply Voltage that is the source of DC Power which is converted to RF Power by the active device via a DC Feed Inductor which acts as a RF choke between Supply Voltage and the active device. BJTs and MOSFETs are most commonly used active devices in industry because of their low cost and availability. But because of their drawback active devices such as JFETs, MESFETs, pHEMTs are finding their way into Power Amplifier design. The active

device is driven by a input signal that determines the frequency of operation and the output power is transferred to an output load typically 50Ωs via an Output Tuning Network. The output tuning network serves multiple purposes based on the amplifier class, some of them include filtering fundamental frequency if any harmonics are generated, converting the output load resistance to a required optimum resistance for maximum power transfer and waveform shaping in case of switching mode power amplifiers.

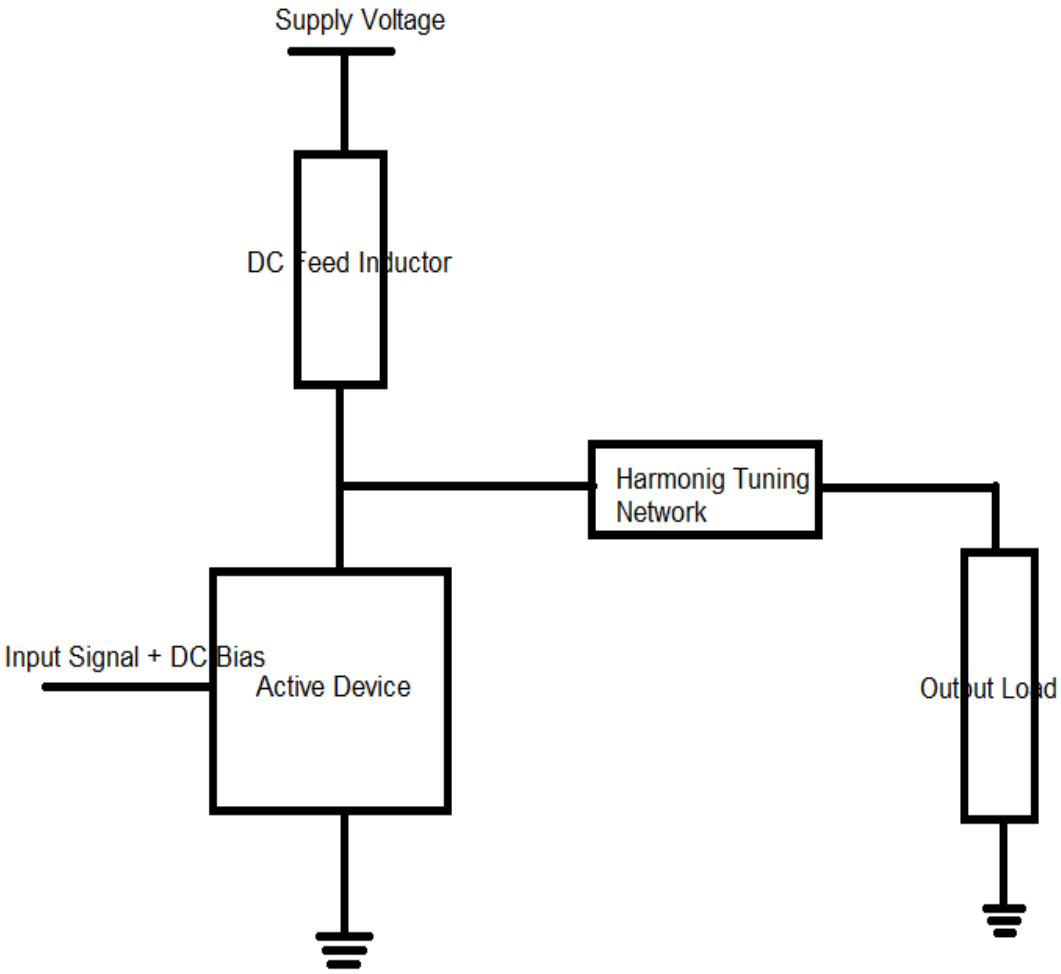

Figure 1: General Block Diagram of Power Amplifier.

Amplifiers can be broadly classified into Linear Mode Power Amplifiers (Class A/AB/B/C) and Switching Mode Power Amplifiers (Class D/E/F/F-1).

1.3.1. Linear Mode Power Amplifiers

Linear Mode Power Amplifiers are categorized into different classes based on the conduction angle (θ). Conduction angle is the fraction of the input signal duty cycle the active device is ON multiplied by 2π [3]. The conduction angle is changed by changing DC bias level to the active device. In a Class-A Power Amplifier conduction angle is 2π, i.e., the active device is ON for the entire duration of the duty cycle. The drain/collector voltage and current waveforms are always sinusoidal which makes it very linear however as the active device consumes half of the DC power that is converted to RF power leading loss in efficiency. The maximum efficiency a Class-A Power Amplifier can achieve is 50% [3].

In Class-B Power Amplifier the active device is turned ON only for half the duration of the duty cycle making the conduction angle π. DC Bias to the active device is set to threshold voltage of the device which makes the Drain/Collector current to be a half wave rectified sine wave. This will reduce the DC current consumed by the active device increasing the efficiency of the amplifier. Maximum efficiency achieved by a Class-B Amplifier is 78.6% [3], however this increase in efficiency comes at loss in Gain and linearity.

It must be noted that the maximum efficiencies discussed above are achieved only when maximum voltage and maximum current are delivered to the load and at this point the output power starts saturating for both amplifier classes. Any back-off from maximum output power will reduce efficiency. In case of Class-A Power Amplifier efficiency decreases in proportion to the drop Output Power delivered i.e, for a 3dB loss from maximum output power efficiency decreases to 25%. In case of Class-B Power Amplifier efficiency is independent to current and drop only in proportion to drop in

output voltage. In application using complex modulation schemes like QAM, OFDM the Peak-to-Average Power Ratio (PAPR) of signal is generally high and the Power Amplifier must operate in backed-off region to ensure linearity thereby reducing the efficiency.

In a Class-AB power amplifier conduction angle is in between π - 2π. A Class AB amplifier is more linear than a Class-B amplifier and is more efficient than a Class-A Power Amplifier. In a Class-C Power Amplifier conduction angle is less than π and has higher efficiency than a Class-B Amplifier but with reduced Gain. The equation below shows the relationship between conduction angle and efficiency assuming maximum output power is transferred –

$$\eta = \frac{1}{4}.\frac{\theta - sin\theta}{sin\left(\frac{\theta}{2}\right) - \left(\frac{\theta}{2}\right).cos\left(\frac{\theta}{2}\right)}$$

As the conduction angle decrease efficiency may increase but at the loss of PA Gain. A Class C Power Amplifier can achieve an efficiency of 100% but the active device will be switched OFF giving zero output power and so in practice a Class-C Power Amplifier has an efficiency around 85% [3]. In order to achieve higher efficiency with reasonable Power Amplifier Gain Switching Mode Power Amplifiers were developed which use waveform shaping techniques to achieve higher efficiency.

1.3.2. Switching Mode Power Amplifiers

It can be observed that loss in DC power in a Linear Mode Power Amplifier is because of the power consumed by the active or in other words the overlap between Drain/Collector Voltage and Current. In Switching Mode Power Amplifiers the active device is driven much harder so that they act as switches and aim at reducing or entirely eliminating the overlap between voltage and current at Drain/Collector. Since the active device is acting as a switch the amplifiers are not linear enough to support linear modulation scheme applications and use modulation schemes such as Pulse Width Modulation (PWM).

A Voltage-Mode Class-D Amplifiers employs a Push-Pull approach by driving each transistor 180^0, so that there will be no overlap between Voltage and Current. A series LC resonator is used to filter the Fundamental Frequency to the output load. In a Current Mode Class-D amplifier current and voltage wave forms are interchanged to reduce the effect of parasitic capacitance on efficiency requirements. A Current Mode Class-D Amplifier with high efficiencies were implemented in [4] at GHz frequencies.

A Class-E Power Amplifier achieves 100% efficiency by defining Zero Voltage Switching and Zeros Current Switching condition [5]. The output tuning network is designed in such a way that when the transistor is turned ON voltage at drain/collector is zero and this called Zero Voltage Switching (ZVS) condition and when the transistor is switched OFF current at drain is zero which is the Zero Current Switching (ZCS) condition. If both the above conditions are satisfied there will be no overlap between Current and Voltage and efficiency will be 100%. A Class-E Power amplifier will also consider the effect of transistor parasitic capacitance when achieving ZVS and ZCS, however while achieving these conditions Drain/Collector voltage can go as high as 3 times Supply Voltage causing reliability concerns. It is very hard to find devices that can tolerate such high drain/collector voltages and as the operating frequency increases the effect of parasitic capacitance will become more dominant.

A Class-F Power Amplifier uses harmonic resonators to shape the voltage and current waveforms so that there is no overlap between them. All Switching Mode Power Amplifiers can achieve a theoretical efficiency of 100% but this efficiency is limited by the switching nature of the active device, loss in the passive devices used in the tuning networks. The Table 1 summarizes the performance characteristics of different Power Amplifier Classes.

Table 1: Characteristics of Different Power Amplifier Classes

Class	Class A	Class B	Class C	Class D	Class E	Class F	Class F^{-1}
Linear	Yes	Yes	No	No	No	No	No
Efficiency	50%	78.6%	~85%	100	100	100	100

CHAPTER 2

CLASS F POWER AMPLIFIER - DESIGN

2.1.Waveform Engineering

Waveform Engineering forms the basis of a Class-F/F^{-1} Power Amplifier design and provides insight into converting a sinusoidal signal to a maximally flat waveforms. The figure below shows the effect of adding in-phase third harmonic $V_3.\cos 3\theta$ to a sinusoid $V_1.\cos\theta$. ($V = V_1\cos\theta - V_3.\cos 3\theta$) –

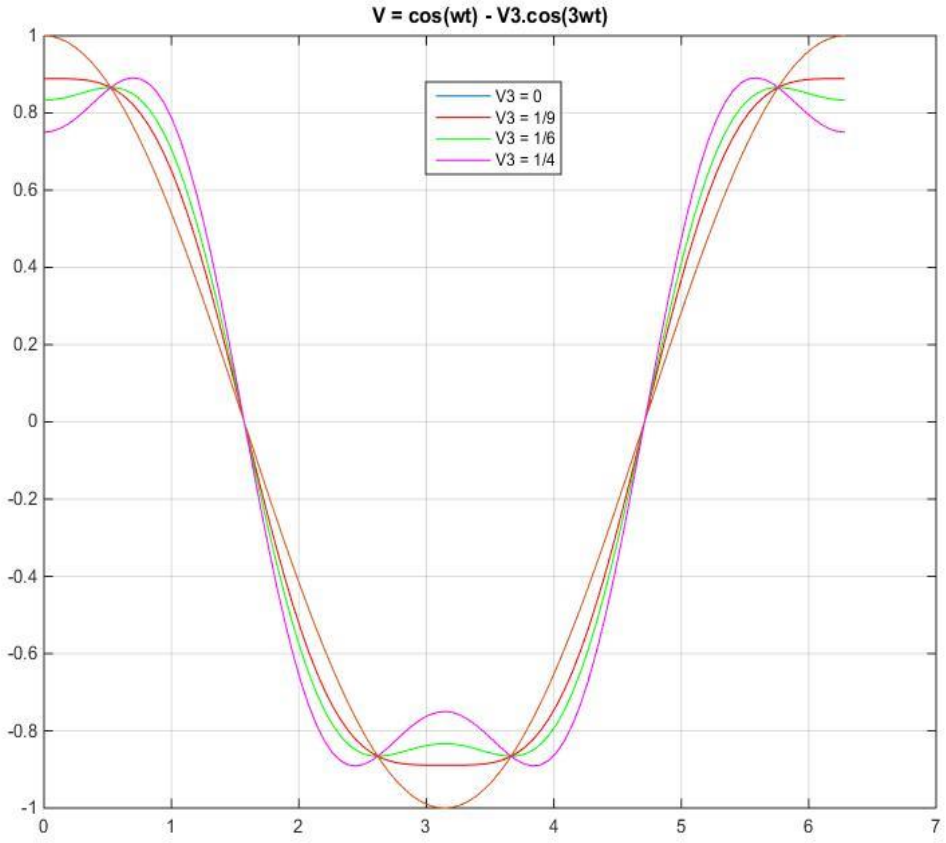

Figure 2: Waveform Shaping using Third Harmonic content.

By adding the third harmonic it is clear that peak value of the waveform decreases as long as there is only a single peak. It can be easily proven that for $V_3/V_1 < 1/9$ there will only be single peak with magnitude $V_{pk} = (V_3-V_1)$ and for higher V_3 values the waveforms starts to overshoot and we can calculate the global minimum of V_{pk} and will be $\frac{\sqrt{3}}{2}.V_1$, when $V_3/V_1 = 1/6$.

Assuming the maximum acceptable voltage at Drain/Collector of an amplifier is V_{max}, we can increase the fundamental component voltage by a factor of *k* by adding some in phase third harmonic to the sinusoid and the maximum value of *k* is $\frac{2}{\sqrt{3}}$. In an optimum case where the fundamental current, DC Voltage and Currents are unaffected this increase in fundamental component voltage directly translates into increase in efficiency. In case of a Class-B Power Amplifier efficiency increases to $\frac{\pi}{4}.\frac{2}{\sqrt{3}}$ or 90.7%.

For a maximally flat case where $V_3/V_1 = 1/9$, $k = 9/8$ which corresponds to an efficiency increase to 88.4%. In this case where the voltage is a maximally flat waveform and current is half wave rectified sine wave is termed as a Class-F Power Amplifier [1]. The voltage waveform can be made into a square wave by adding infinite odd harmonics to the sinusoid. A waveform having *m* number of odd harmonics has the general form –

$$\frac{V(\theta)}{Vdc} = 1 - \sum_{q=0}^{m} V(2q-1).sin(2q-1)\theta,$$

The complexity in solving the above equation is finding the values of the coefficient and θ which maximize the fundamental component for a given V_{max}. A generalized solution was proposed by Rhodes [6] for the above waveform and constraint V(θ) >0. The set of θ that give maximum value for the fundamental are

$$\theta_r = \frac{r\pi}{m+1}, \text{ for } r = 1 \text{ to } m$$

After further solving the above equation we can calculate the maximum value of V(1) when introducing a fifth harmonic is

$$V_1 = \frac{1+\sqrt{2}}{2}.V_{max},$$

The efficiency of a Class-B amplifier by adding 3rd and 5th harmonic content increases from 78.6% to $\frac{\pi}{4}.\frac{1+\sqrt{2}}{2}$ or 94.8% [7]. The figure below shows the increase in efficiency by increasing the number of odd harmonics to the drain/collector voltage waveform

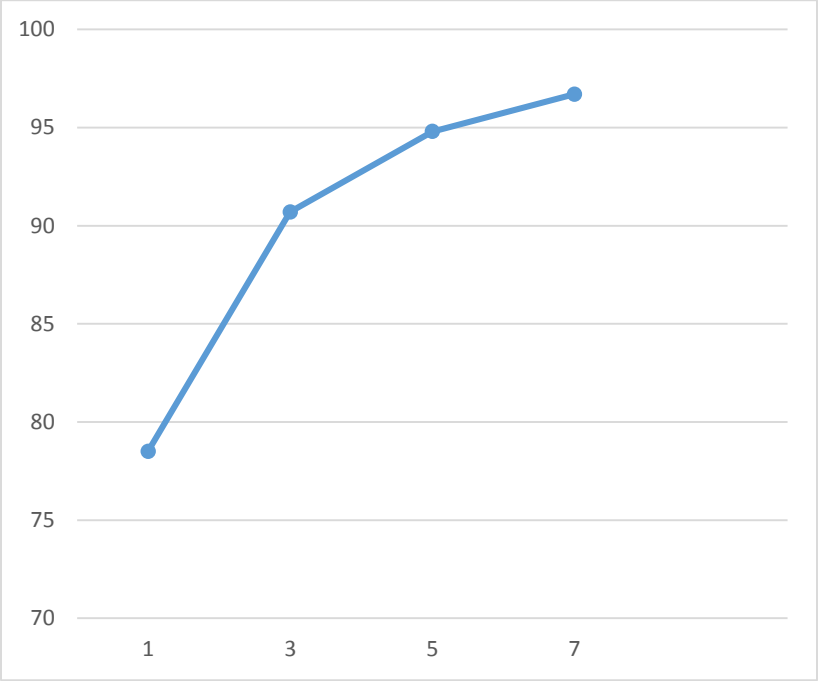

Figure 3: Plot of Efficiency vs. Number of Odd Harmonics added to fundamental.

As the number of odd harmonics added increases infinite the waveform will become a perfect square wave with fundamental component becoming $\frac{4}{\pi}.V_{max}$ and efficiency will be 100%. A similar analysis can be done by replacing the voltage waveform with current waveform in case of Class-F^{-1} Power Amplifier.

A Class-F/F^{-1} Power Amplifier can be described as overdriven Class-B Power Amplifier that can achieve a theoretical efficiency of 100% by using waveform engineering. This is achieved by shaping either current or voltage waveform into a Square Wave and the other into a half wave rectified sine wave. In a Class-F Power Amplifier, Voltage waveform is shaped into a square wave by adding odd harmonic

voltages into the Drain/Collector Voltage and shorting the even harmonic voltages. This will in turn create a half wave rectified sine wave Current 180^0 out of phase with Voltage. The waveform shaping is achieved by placing parallel LC resonators blocking odd harmonics and series LC resonators to ground shorting even harmonics [8]. Theoretically, this will give an efficiency of 100%, i.e., when infinite odd harmonics are blocked and even harmonics are grounded and active device behaves as an ideal switch.

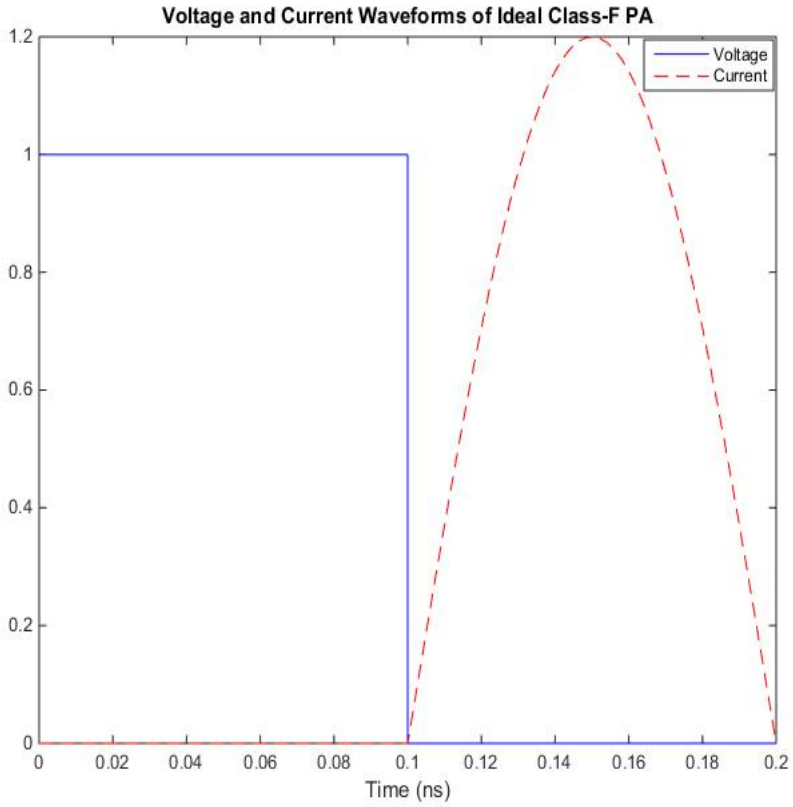

Figure 4: Voltage and Current waveforms at Drain/Collector of a theoretical Class-F Power Amplifier.

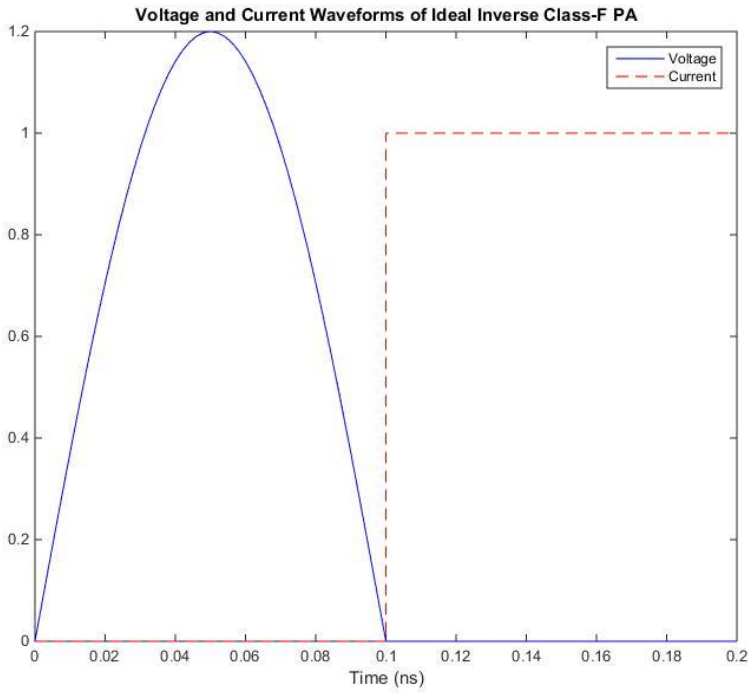

Figure 5: Voltage and Current waveforms at Drain/Collector of a theoretical Class-F^{-1} Power Amplifier.

2.2.Class-F Power Amplifier in Practice

One of the main drawbacks of using Switching Mode Power Amplifiers at High GHz frequency is the switching speed of the active device is too slow and the active device will not be able to sweep through its linear region as an ideal switch. The On-Resistance of the active device will degrade the efficiency as there will be an overlap between Current and Voltage at the Drain/Collector. Most importantly, either Voltage or the Current cannot be fully shaped as Square wave as we cannot use infinite LC resonators to block the odd harmonics and short the even harmonics. The number of odd and even harmonic content tuned define the order of the Class-F Power Amplifier. A Class-$F_{2,3}$ Power Amplifier, where 3^{rd} harmonic is added to fundamental and 2^{nd} harmonic is shorted, is designed for this Thesis study.

The maximum theoretical efficiency of 90.7% for a 3rd order Class-F Power Amplifier is not practical to achieve because of losses associated with active device which include ON resistance of the active device, knee voltage. The quality factor of the inductors and capacitors used in the tuning network not only increase power dissipated but also affect the waveform shaping. The ratio of third harmonic content added to the fundamental should be 1/6 inorder to achieve maximum efficiency and so all the above impairments must be considered when designing harmonic tuning network.

Despite these drawbacks, Switching Mode Power Amplifiers find their way into several applications because of the high efficiency and output power they can deliver. Among the Switching Mode Power Amplifiers Class-E Power Amplifiers more prominent (at low GHz frequencies) because of the complexity in the design of Class-F Power Amplifiers output resonators, but Class-E Power Amplifiers generate a drain voltage which will be typically 3 times the supply voltage [5]. A similar problem is seen in Class-F^{-1} as we convert current to a square wave and voltage to half rectified sine wave. So, a solution to such problem would be to simplify the output harmonic network of a Class-F Power Amplifier, which is the basic aim of this thesis study.

2.3.Harmonic Tuning Network

The order of the Class-F Power Amplifier determines the number of in-phase odd harmonics content added to the fundamental component at Drain/Collector and increases the complexity of the output harmonic tuning network. This is because for each odd harmonic content added a LC resonator is required. Apart from adding odd harmonic component the tuning network must also provide optimum load at fundamental for maximum power transfer.

Inductors have a large footprint and occupy maximum area in a Fully Integrated circuit which is why Class-F Power Amplifier designs often employ off-chip harmonic tuning. In recent years research was done on the reuse of inductors within a non-ideal

Transformer used for differential to single ended conversion. If we can incorporate such design technique into Class-F output harmonic tuning we can reduce the number of inductors used for the network. Consider an ideal transformer shown in the figure below –

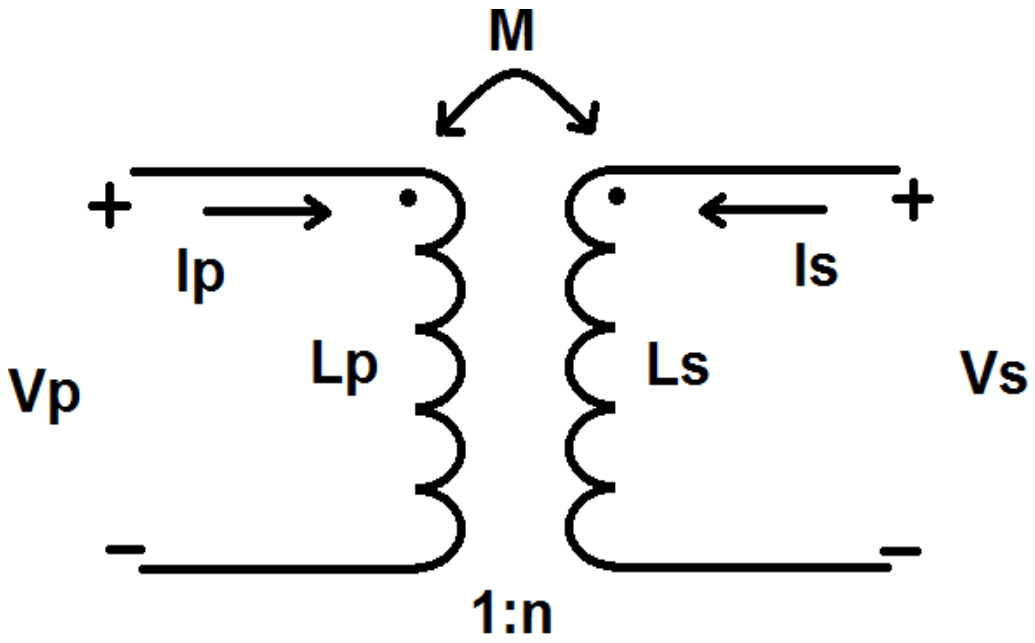

Figure 6: Ideal Transformer Model.

Lp and Ls are the self-inductance of primary and secondary coil respectively and M is the Mutual inductance. Voltages Vp and Vs can be derived from Ip and Is using the below equations –

$$Vp = j\omega Lp.Ip + j\omega M.Is$$

$$Vs = j\omega M.Ip + j\omega Ls.Is$$

and

$$\frac{Vp}{Vs} = \frac{Is}{Ip} = \frac{Np}{Ns} = \sqrt{\frac{Lp}{Ls}} = n,$$

Coupling Coefficient, $k = \frac{M}{\sqrt{LpLs}}$

The above identity holds only if power transfer is lossless and magnetic flux is confined to the magnetic core [9]. However, in reality stray inductances were observed in a non-ideal transformer as shown in the figure below –

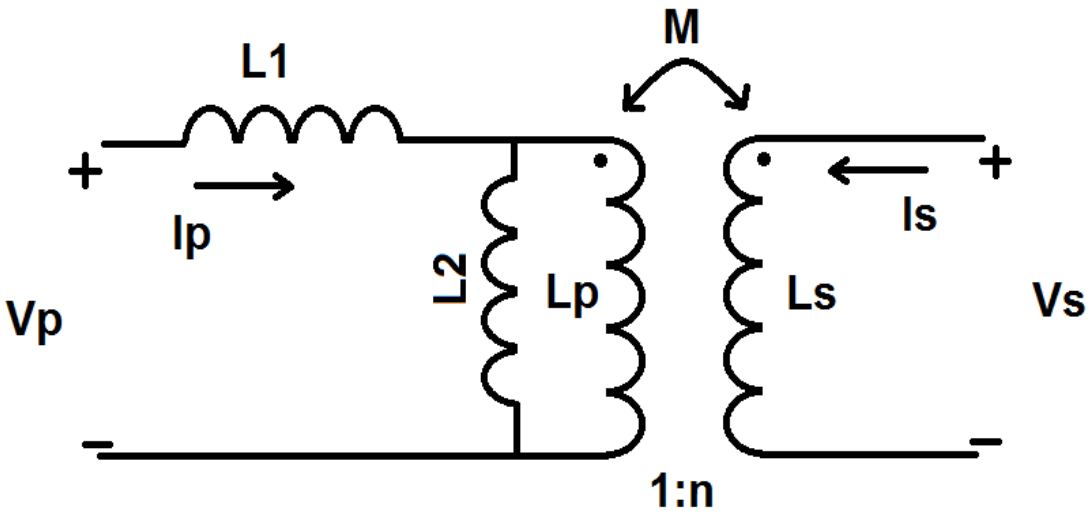

Figure 7: Non-Ideal Transformer Model.

In case of a non-ideal transformer

$$L1 = (1-k^2).Lp$$

$$L2 = k^2.Lp$$

In [10] these stray inductances were reused to achieve a Broadband harmonic tuning for a Class AB Power Amplifier design. Using similar technique stray inductances L1 and L2 can be used as a part of harmonic tuning network for the Class-F Power Amplifier. Using this technique we can effectively eliminate the footprint of two inductors by replacing them with the stray inductances. However, the series-shunt topology of inductors L1 and L2 must restrict the harmonic tuning network design. This may lead to some amount of mistune but the advantage of reducing inductor footprint overweighs the mismatch in

harmonic tuning. That is why this technique is employed in the harmonic tuning network for Class-F Power Amplifier design in this Thesis research.

CHAPTER 3

CLASS F POWER AMPLIFIER - IMPLEMENTATION

The table below shows the Target Specifications for the Class-F Power Amplifier design –

Table 2: Class-F Power Amplifier Design Specifications. Amplifier design.

Supply Voltage (V_{supp})	2.2V
Output Power (P_{out})	25dBm/0.316W
Operating Frequency	5GHz
Gain	15 dB
Power Added Efficiency (PAE)	>50%

3.1.Optimum Load Calculations

Assuming an ideal Square wave for voltage and a half wave rectified sine wave for current at drain/collector the following is the Fourier series expansion of voltage –

$$v(t) = \frac{Vmax}{2} + \frac{4}{\pi} Vmax \sum_{n=1}^{\infty} \frac{\sin((2n-1)\omega t)}{2n-1},$$

where V_{max} is maximum voltage or the amplitude of the square wave and is equal to twice supply voltage as DC Feed inductor is used.

$$v(t) = V_{DC} + V_1.\sin(2\pi f_1.t) + V_3.\sin(2\pi f_3.t) + V_5.\sin(2\pi f_5.t) + \ldots..$$

$$V_1 = \frac{4}{\pi} V_{max}\ ;\ V_{max} = 2*V_{DC}$$

$$V_1 = \frac{8}{\pi} V_{DC}$$

$$P_{out} = V_1.V_1/2*R_{opt}$$

However, the voltage waveform cannot be assumed to be ideal square wave as only third harmonic content is added and the peak value fundamental can reach when only an in-phase third harmonic is added is $\frac{2}{\sqrt{3}}$. This implies –

$$V_1 = \frac{2}{\sqrt{3}}.V_{max} = \frac{4}{\sqrt{3}}.V_{DC}$$

Solving the above equation with V_{DC} = 2.2V; Pout = 25dBm = 0.316Watts

$$R_{opt} = 40.84\Omega$$

The figures below shows the harmonic tuning network and smith chart representation of the impedances of the tuning network –

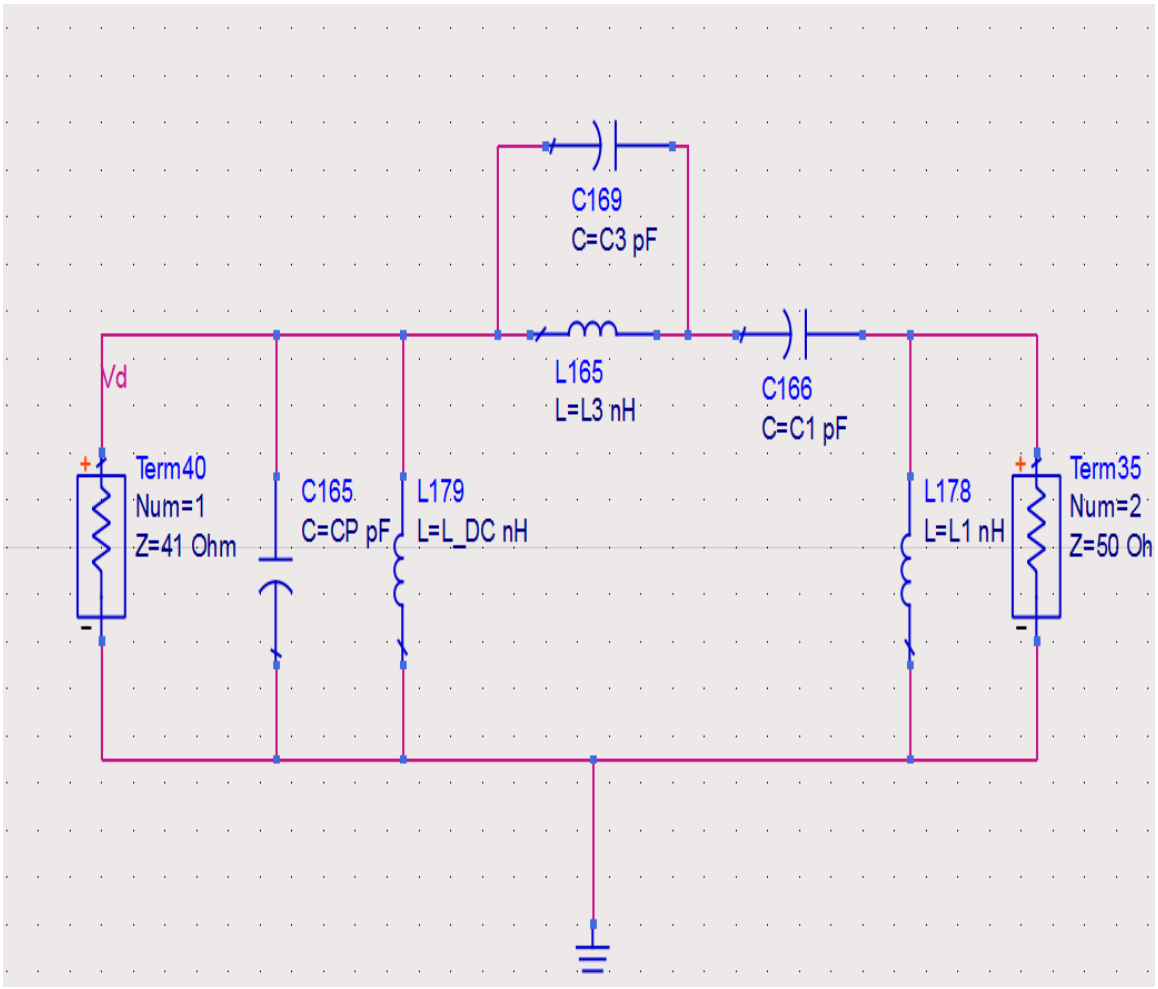

Figure 8: Harmonic Tuning Network Design with LC Resonators.

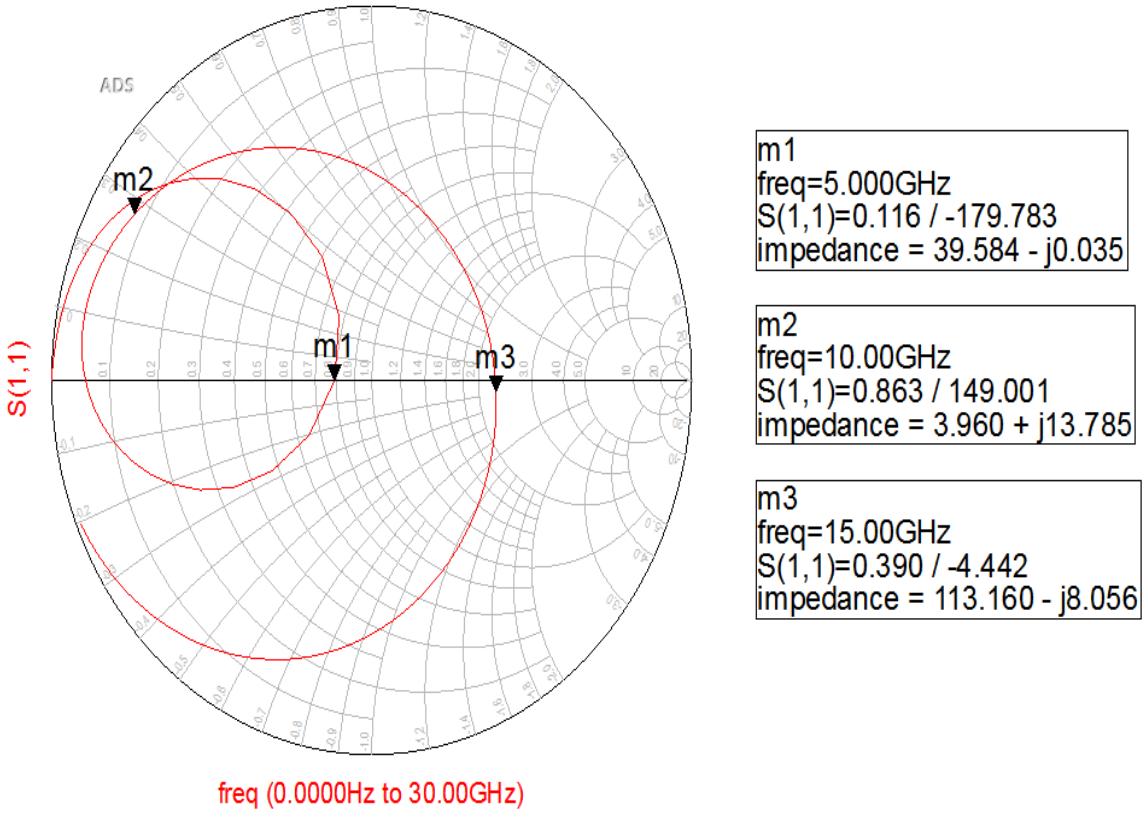

Figure 9: Smith Chart representation of Impedances across frequency.

Inorder to design the class F Power Amplifier we need a parallel LC Tank to block 3rd Harmonic voltage at drain at 15GHz and short 2nd harmonic at 10GHz. However, using such topology would not allow us to reuse the inductors within the transformer and also we cannot make the 3rd harmonic impedance seen from drain to be infinite. So after considering some reasonable approximations, we designed the harmonic tuning network shown in figure 10.

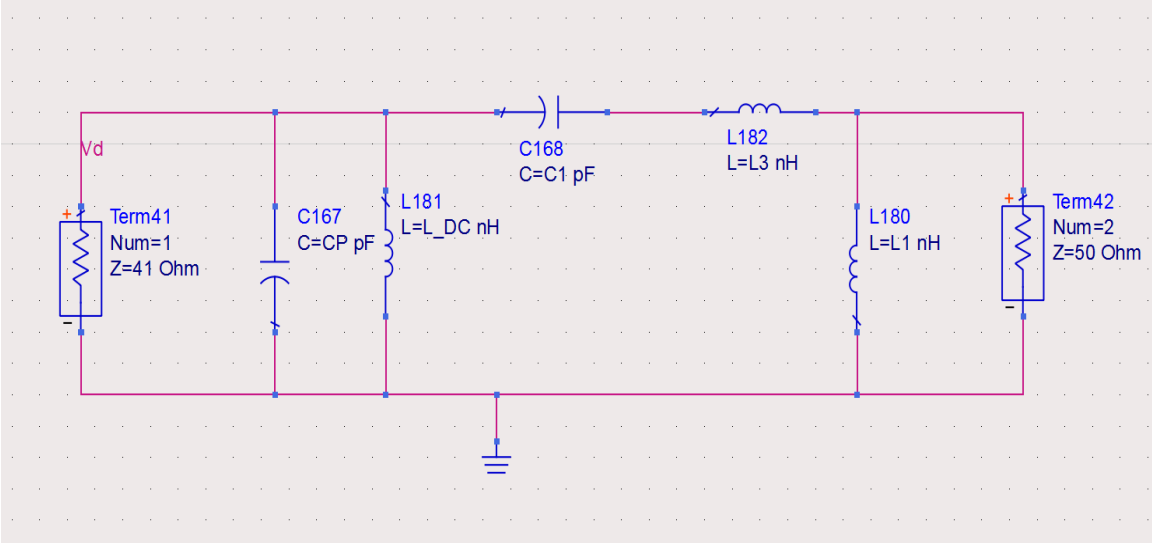

Figure 10: Schematic of the proposed Output Harmonic Tuning Network.

The figure below shows the smith chart representation of the impedances across frequency of the tuning network –

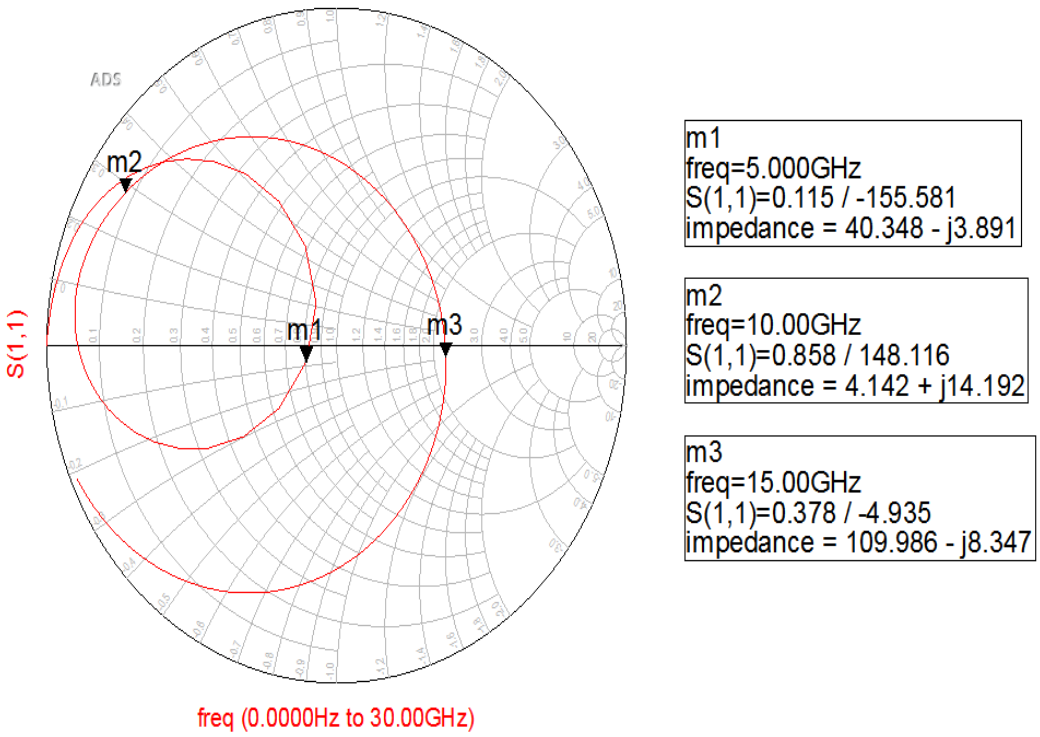

Figure 11: Smith Chart Representation of Impedances across frequency.

The above results show a single-ended realization of the harmonic tuning network, which is same as the Differential/Odd Mode impedance that apply to only 1st and 3rd harmonics (odd harmonics). Common/Even Mode impedance characterizes the impedance of 2nd harmonic and so differential mode analysis using ideal transformer is done. The R_{opt} value calculated for single ended analysis changes to $R_{opt,diff} = R_{opt}/n^2$, where n is the turn ratio of the transformer. A 1A AC current source is connected across the terminals of the harmonic tuning network and voltage is measured across them, using the following equations Odd-Mode and Even-Mode impedances are calculated –

$$Z_{odd} = (V_p - V_n)$$

$$Z_{even} = (V_p + V_n)/2$$

The figures below shows the schematic of the Test Bench used to perform Differential Mode analysis and plots of Even Mode and Odd Mode Impedances across frequency–

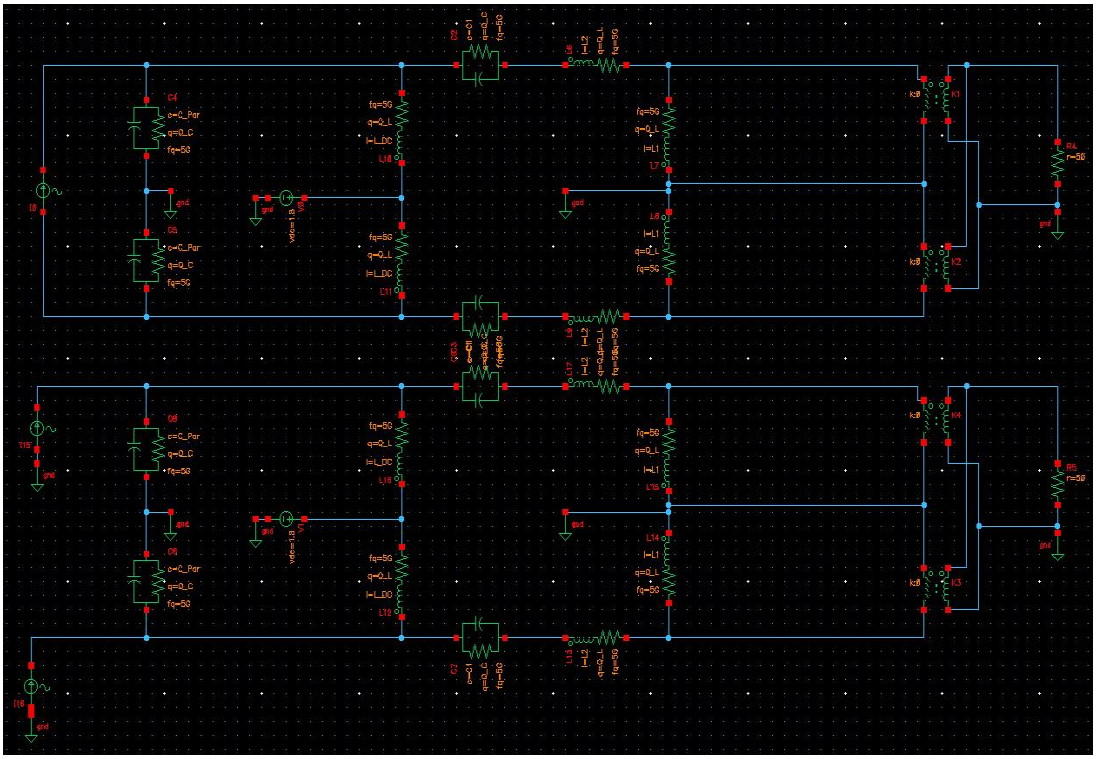

Figure 12: Differential Mode Analysis test bench.

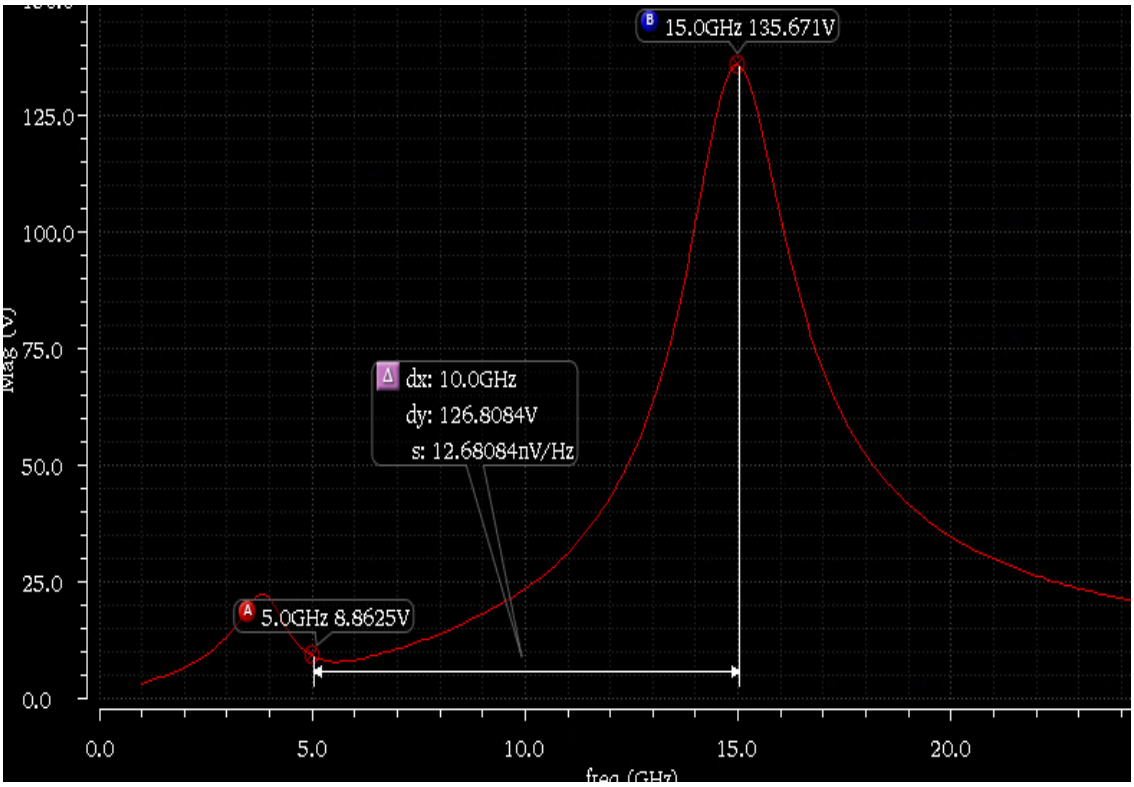

Figure 13: Odd Mode Impedance across Frequency.

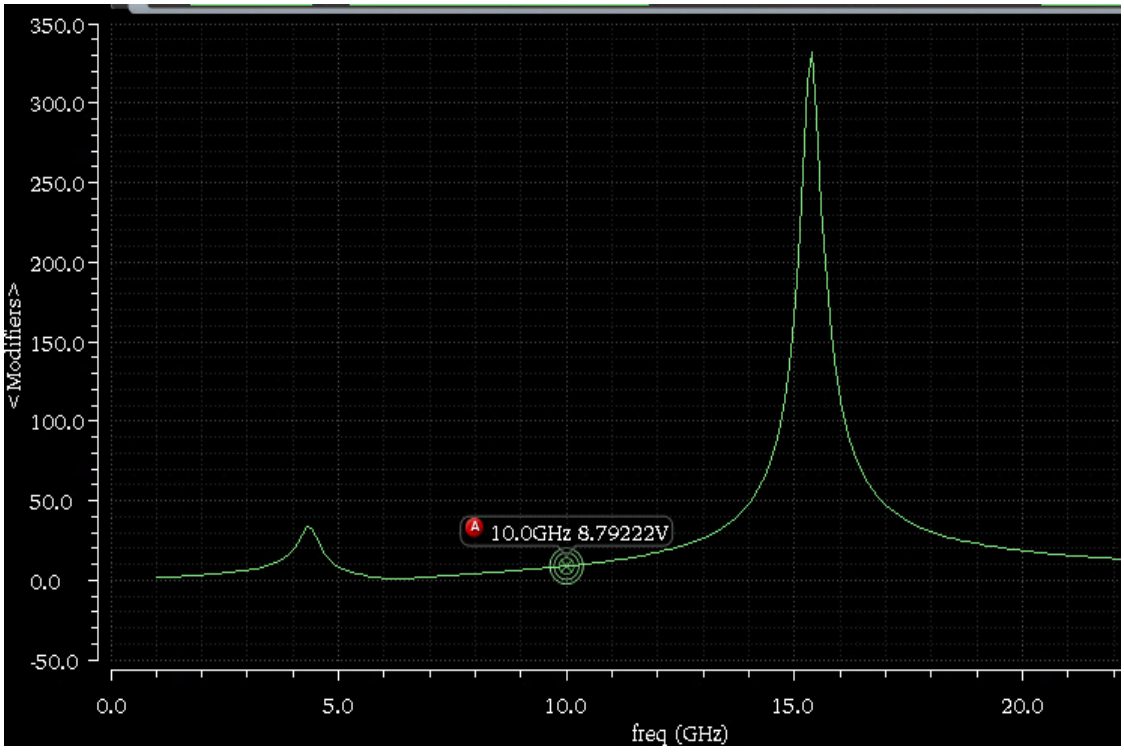

Figure 14: Even Mode Impedance across Frequency.

The impedances seen change when active device is introduced because of the effect of non-linear capacitance at the input and the output of the device. The capacitance introduces distortion at 2nd and 3rd harmonics which hinder the waveforms shaping required for Class-F operation [11]. A 2-stage Differential Power Amplifier is designed to reach required specifications. The figure below shows a single branch of the 2-stage Power Amplifier along with the harmonic tuning network –

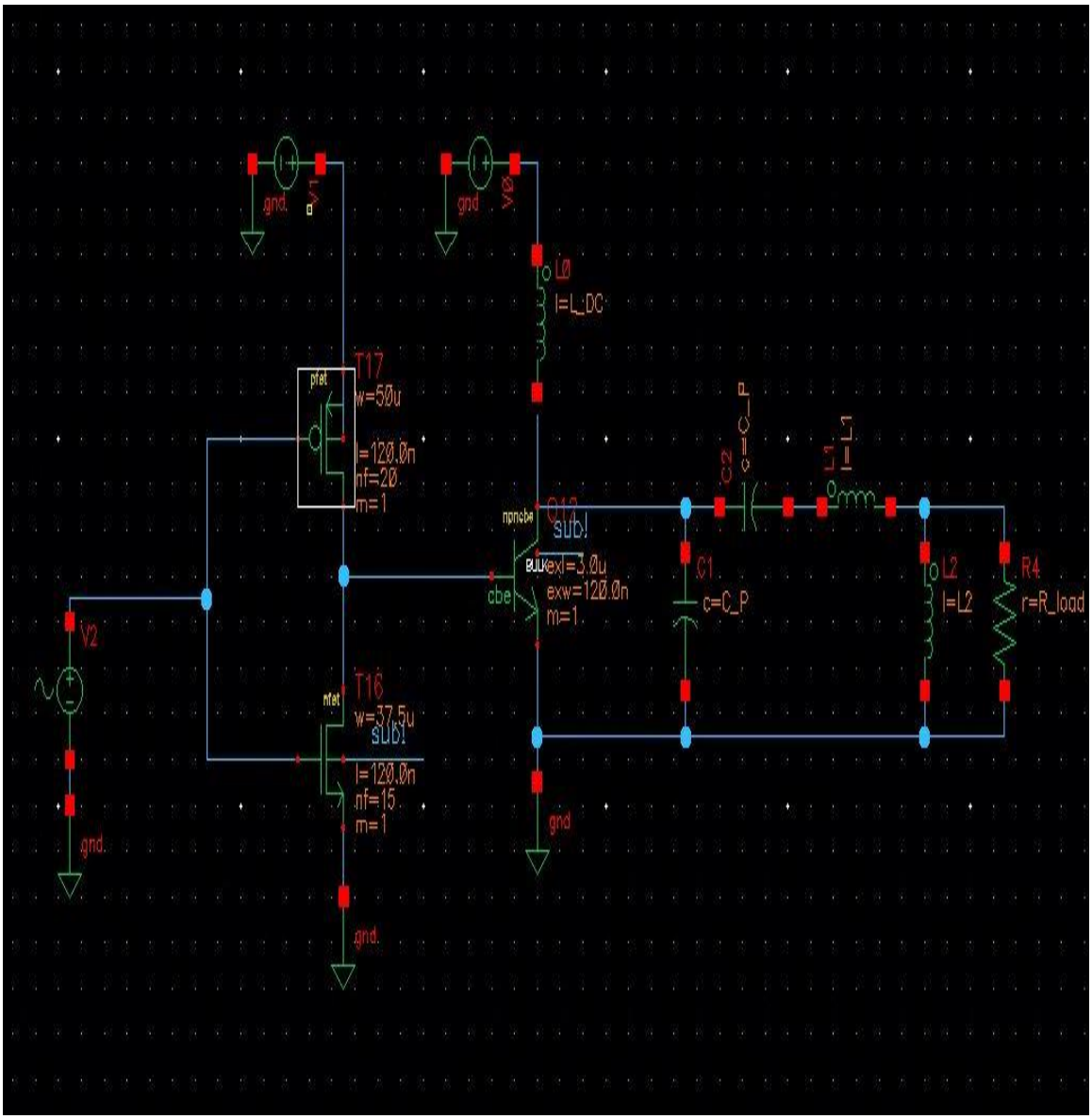

Figure 15: Schematic of 2-Stage Class-F Power Amplifier.

3.2.CMOS Inverter to drive Power Amplifier

In order to achieve the Gain specification I used a CMOS inverter to drive the Class-F Power Amplifier. The supply voltage used to for the inverter defines the rail to rail voltage of the inverter and thereby the input signal of the Power Amplifier. In order to achieve the required efficiency and gain the supply voltage was fixed at Vsupp_Inv = 1.6V. The inverter also consumes a certain amount of DC Power which increases the overall DC power consumption of the system and decreases the efficiency, however the DC power consumed by the inverter is relatively small when compared with DC power consumed by the amplifier itself. DC Bias value to the inverter is also optimized for better Gain and Efficiency. Below is the schematic diagram and the layout of the CMOS inverter designed to drive the amplifier –

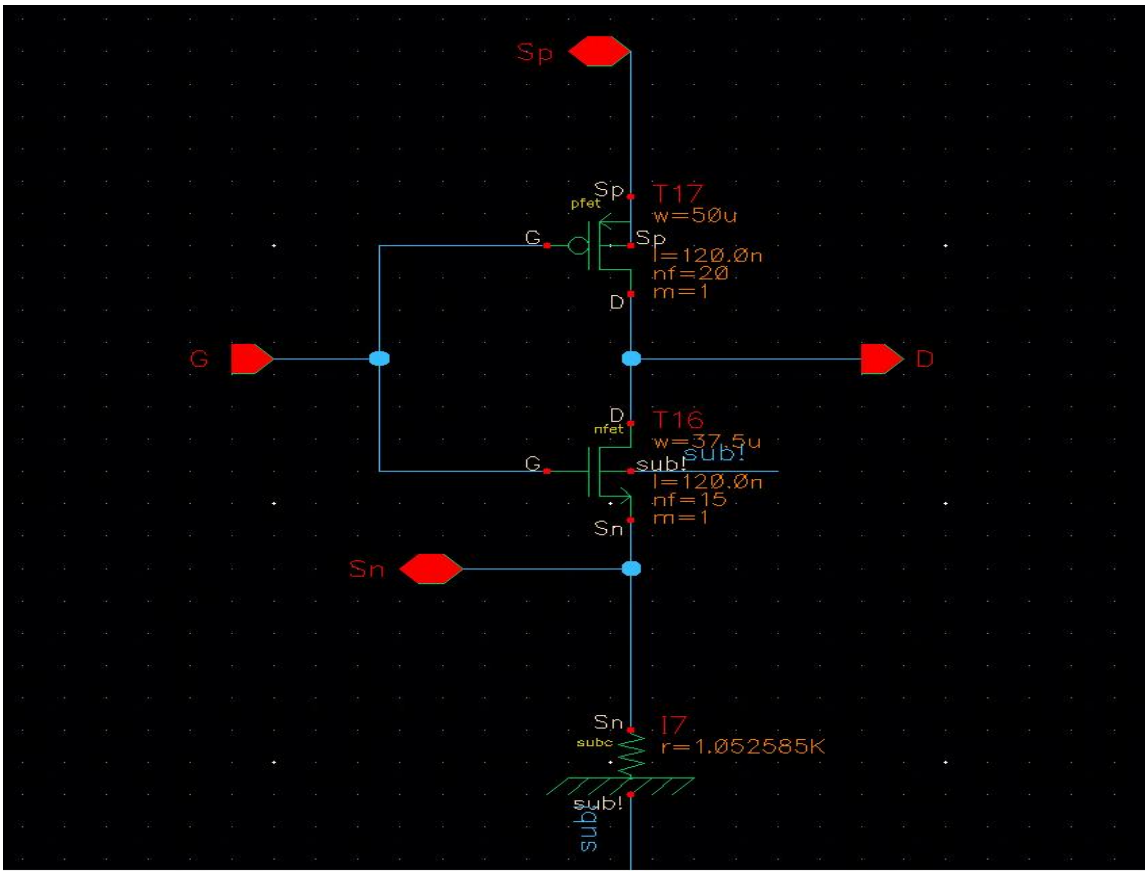

Figure 16: CMOS Inverter Schematic.

3.3.Passive Structure Design

Passive Structures play a significant role in determining the performance of the Class-F Power Amplifier because of their usage in the waveform shaping of the collector voltage and current. In this particular design we need an input transformer to convert a single ended input to a differential input to the CMOS invertor, a DC feed inductor and an output transformer to convert differential output to single ended. All the above mentioned passive structures were designed using ANSYS High Frequency Structural Simulator Electromagnetics Suite 16.1 with IBM BICMOS 8HP design kit metal layer stack.

3.3.1. Inductor Design

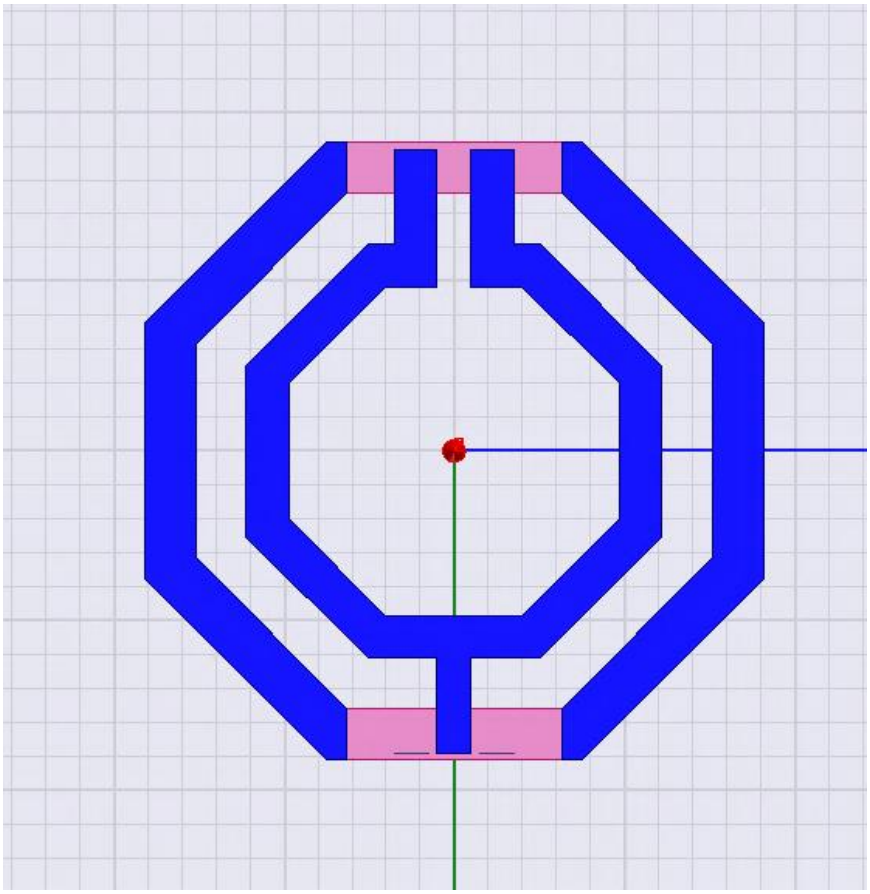

Figure 17. Inductor Design using HFSS EM simulator.

The figure shows the inductor design with octagon shape to have better quality factor and also occupying less space at the same time. The output matching network for the Power Amplifier is optimized by reusing the stray inductance of the non-ideal output transformer. But a DC Feed Inductor is still used between the supply voltage and the active device (BJT in this case).

3.3.2. Input Balun:

Input Balun is used to convert a single ended input to differential input for the inverter. For the Input Balun, I designed a 1-to-1 transformer using IBM BICMOS 8HP metal layer stack. Below figure shows the transformer designed for the Input Balun –

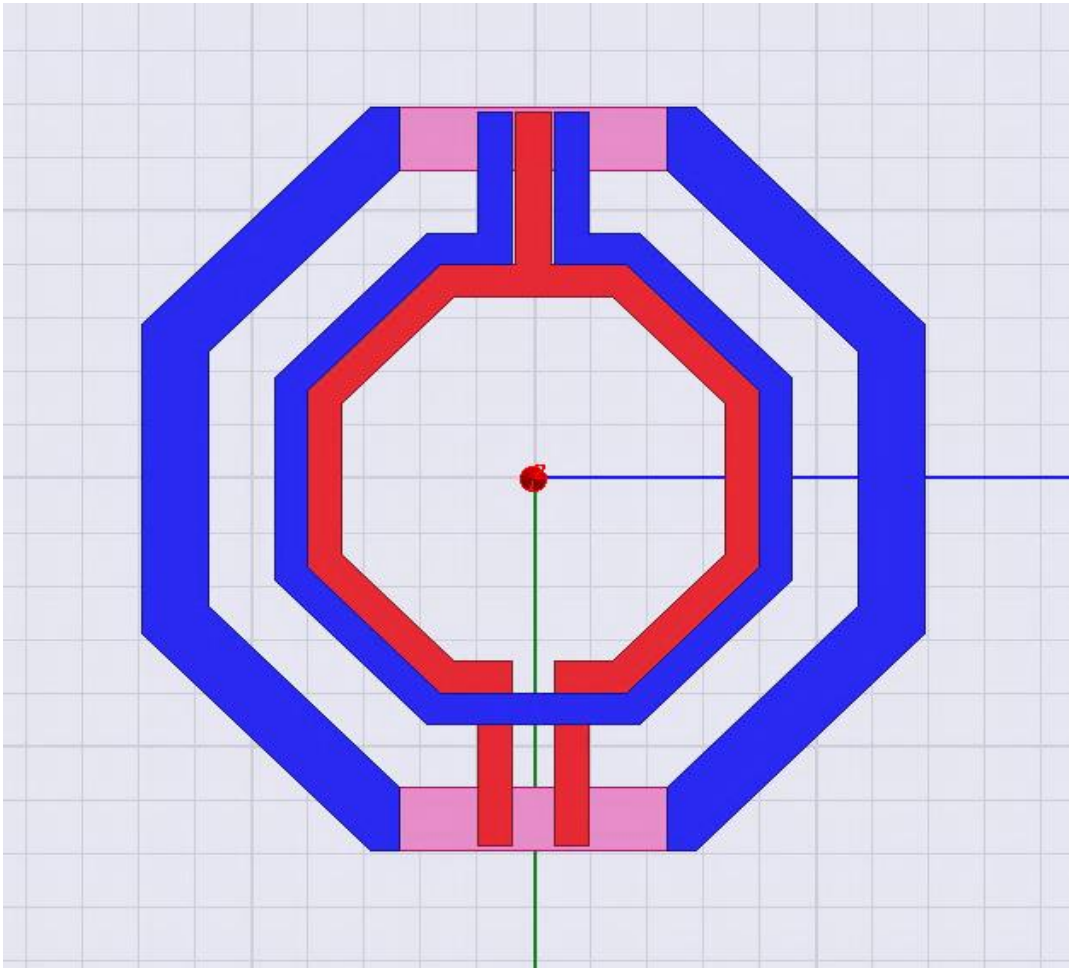

Figure 18. 1-to-1 Transformer designed for Input Balun.

The Outer Ring is made using Metal Layer MA and Inner Ring is made using Metal Layer E1. The Outer Ring makes up the single ended side of the transformer and the Inner Ring is the differential side of the transformer.

3.3.3. Output Balun:

The design of Output Balun is critical for the Power Amplifier performance as the stray inductance of the Transformer are to be used in the Output Matching Network of the Power Amplifier. A 1-to-2 Transformer is used as the Output Balun for this design. The figure below shows the 1-to-2 center-tap transformer structure –

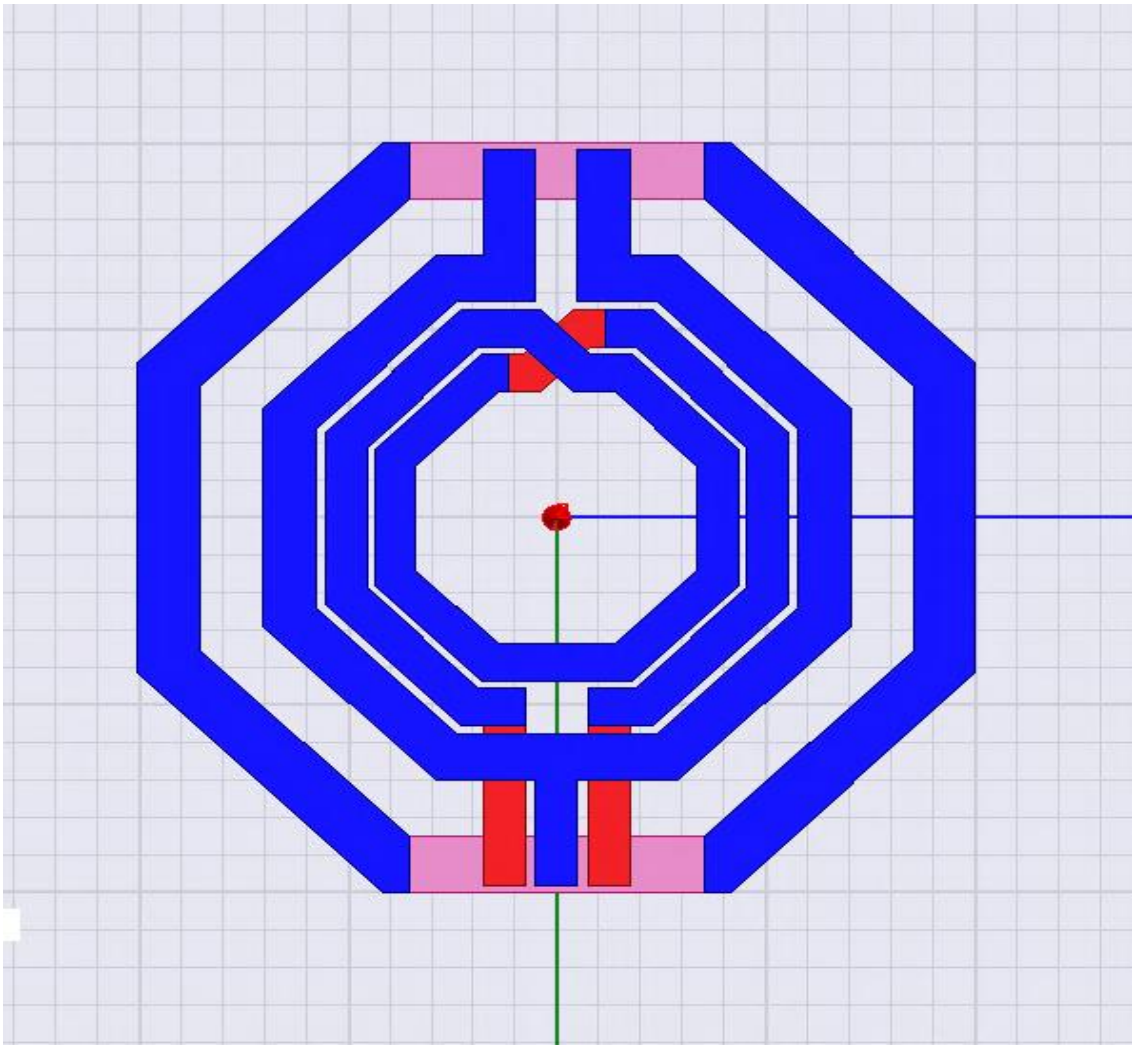

Figure 19. 1-to-2 Transformer designed for Output Balun.

The outer ring made up Metal Layer MA forms the differential side of the Blaun with center tap connected to the ground. The inner ring with 2-turns for s the single ended side of the Balun.and is made up of Metal layer E1 and for better conductivity metal layer MA is stacked over layer E1 using via.

The Metal Insulator Metal (MIM) capcitors from BICMOS8HP IBM Design Kit are used in the harmonic tuning network. Two capacitors were designed one with a Capacitance of 20fF to be used for capacitors of the order of 100fF and other with capacitance of 135fF to be used for capacitors of the order of 1pF.

CHAPTER 4

SIMULATION RESULTS

Ideally, Class-F Power Amplifier designed with 3rd order harmonic terminations should be able to achieve efficiency of 90.4%. However, this efficiency is limited by the switching nature of BJT, parasitic effects that come up with layout design and also the quality factor of the components used. This value is further degraded because of the compact nature of Output Tuning Network. The figure below shows the top level schematic of the 2-stage power amplifier with extracted view of the inverter and Power Amplifier blocks, along with 5-port block and 3-port block with s-parameter files extracted from the Output Balun and DC-Feed Inductor using Ansys HFSS EM suite.

The figure below shows the Top Level schematic used to test the performance of the Class-F Power Amplifier with 5-port with s-parameter file extracted from Input Balun design –

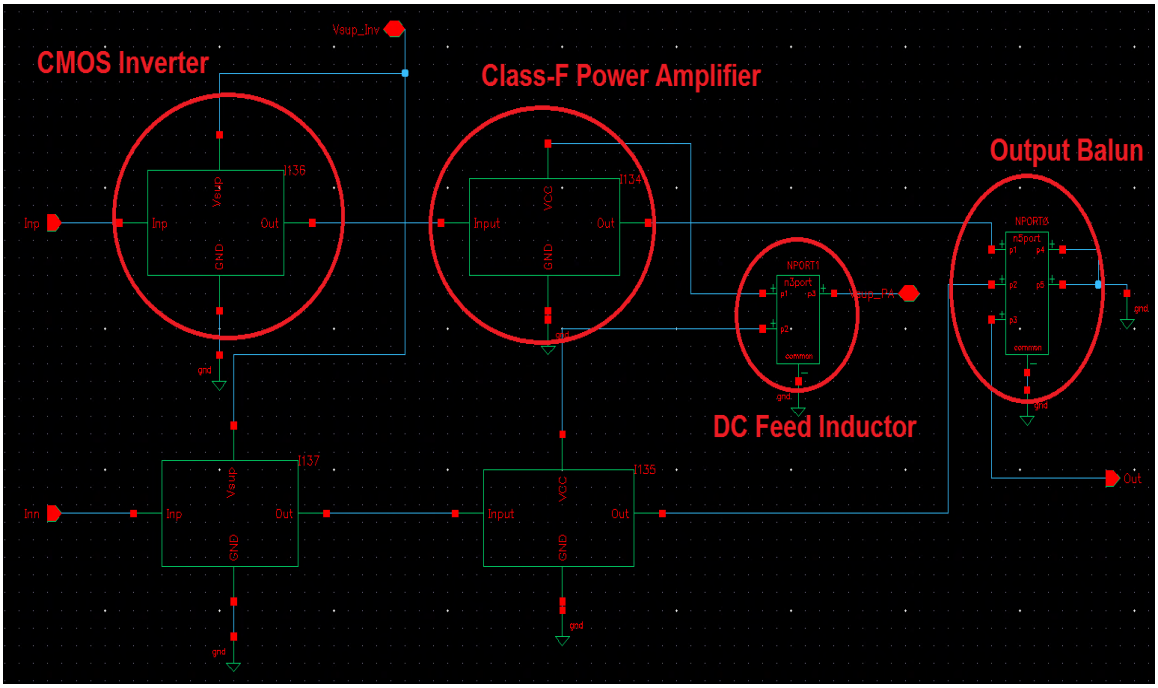

Figure 20: Top Level Schematic of 2-stage Class-F Power Amplifier.

4.1.Top Level Simulations

4.1.1. Input S11:

The Input Balun designed for Single Ended to Differential conversion cannot be assumed to be an ideal transformer and has some stray inductance that result in loss of Power at frequency of Operation and thereby reduce the Gain. After tuning out the stray inductance S11<-15dB is observed at 5GHz the frequency of operation. The plot below shows S11 across frequency measured at the input of the Balun for a 50Ω source resistance –

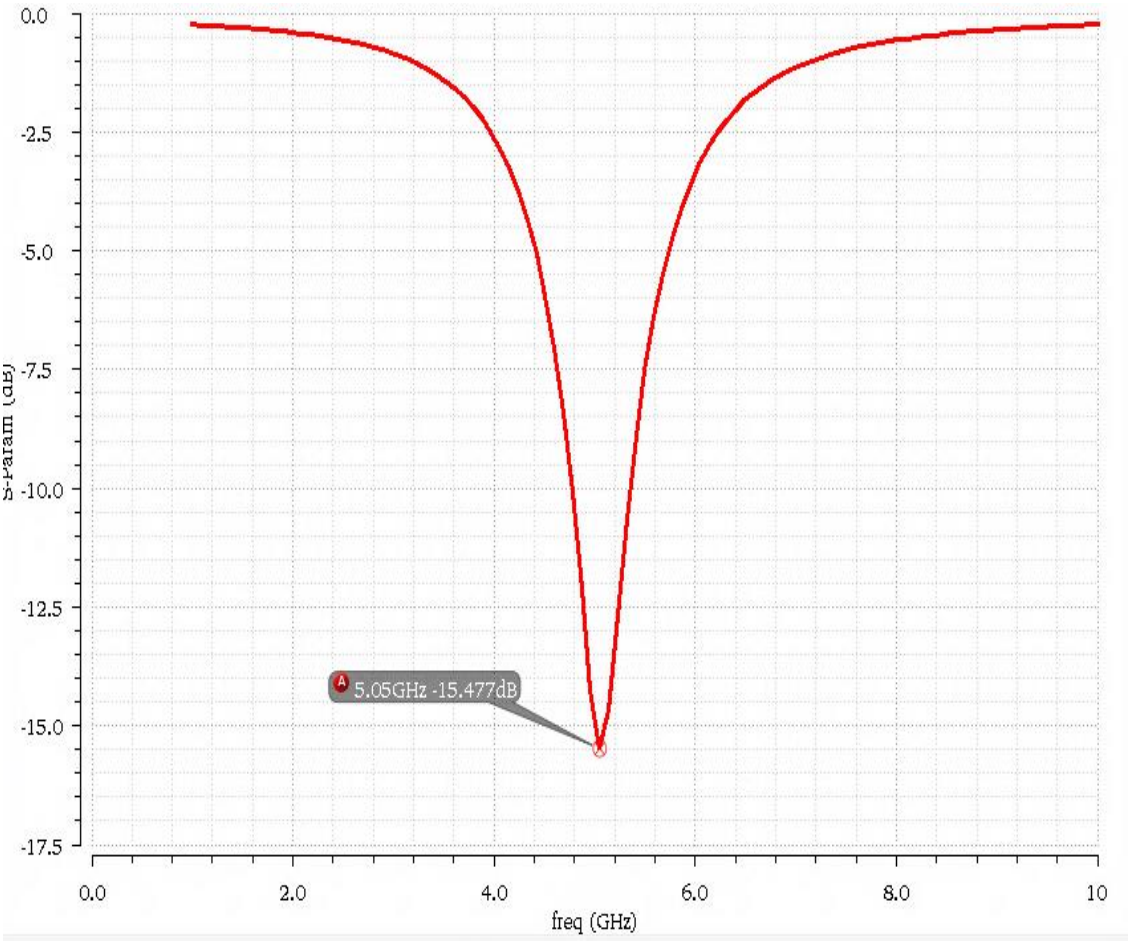

Figure 21: Plot of S11 across frequency

4.1.2. AM-AM Simulations:

Input Power is swept from -10dBm to 12dBm and output power is measured to analyze the AM-AM performance of the Power Amplifier. Using the measured output power Efficiency (η) and Power Added Efficiency (PAE) were also measured.

The figure below shows the plot of Output Power Vs Input Power along with Efficiency and Power Added Efficiency performance –

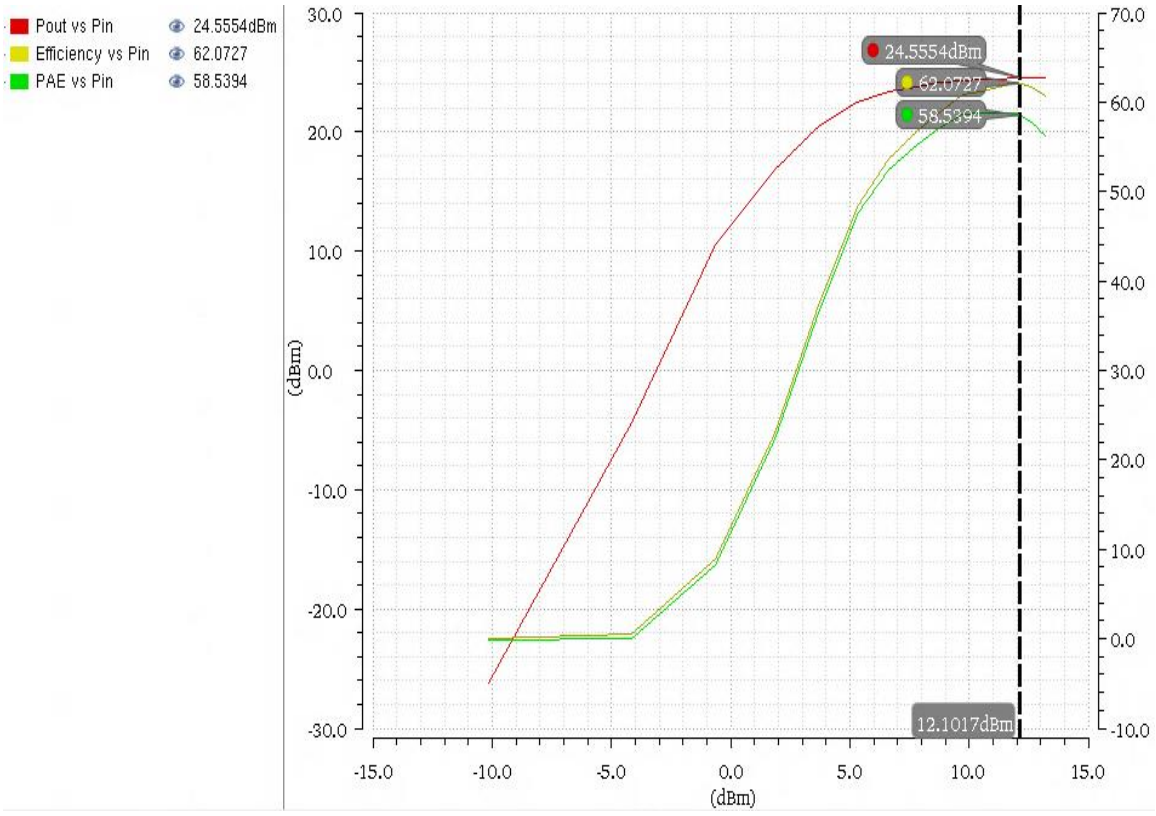

Figure 22. Output Power, Efficiency and PAE Vs. Input Power.

Output Power of the amplifier increases linearly with Input Power and starts saturating. Peak Efficiency reaches to 62% at 24.55dBm Output Power, however Gain drops by more than 3dB. At P1dB Output Power is 23.7dBm, Efficiency is 56.27% and PAE is 54.9%. The figure below shows the magnitude of voltage at each harmonic –

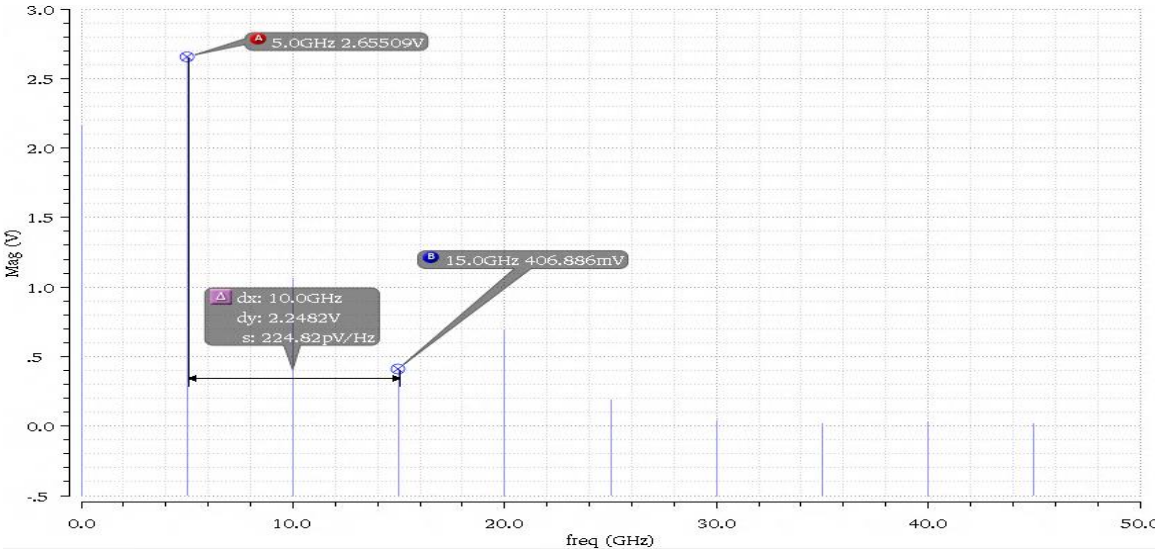

Figure 23. Voltage Magnitude at different harmonics.

The magnitude of voltage at first harmonic is V_1 = 2.65V and at third harmonic is V_3 = 0.406V, making the ratio of V_3/V_1=1/6.52, which is near to ratio of 1/6 that gives out maximum fundamental voltage for a given peak voltage. However, because of the second harmonic content generated by the parasitic capacitance and knee voltage of the active device waveform is distorted. Figure 24 shows the Collector Voltage and Current Waveforms.

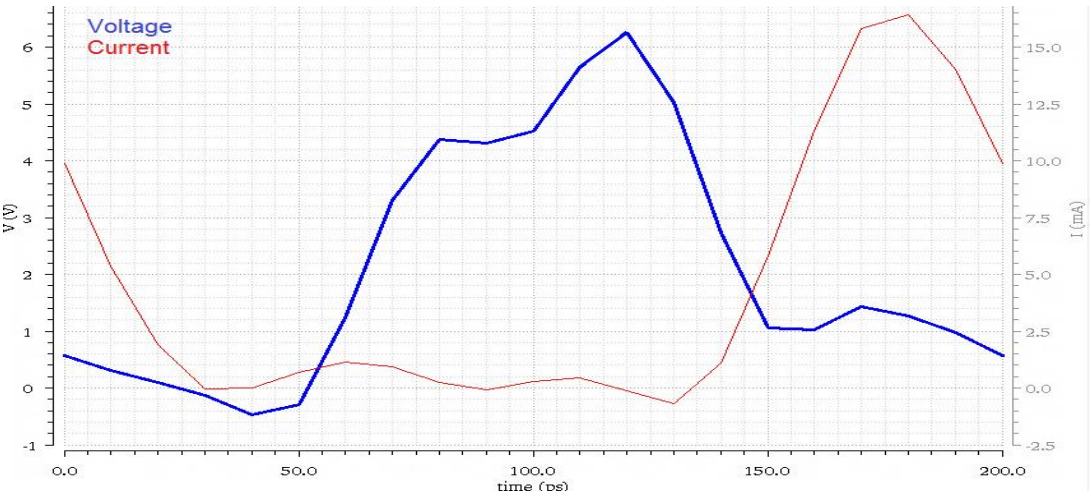

Figure 24: Collector Voltage and Current Waveforms.

CHAPTER 5

CONCLUSIONS

In conclusion, a Class-F Power Amplifier is designed by using Bipolar Junction Transistors as an active device. A saturated output power of 24.5dBm was measured with 62% efficiency. At P1dB this efficiency decreases to 56.2%, however because of a high gain of 15dB the PAE is measured at 54.9%. The complexity of Output Harmonic tuning network was reduced by reusing the stray inductances and Fully Integrated Power Amplifier solution has been proposed and implemented.

However, several approximations were considered during the Harmonic Tuning Network design which reduced the efficiency of the Power Amplifier. A more careful approach while designing the tuning network which considers the parasitic effects of the passive components, the effects of parasitic capacitance of the active device that introduces harmonic distortions will lead to better performance.

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