HIGH-FREQUENCY SILICON-GERMANIUM RECONFIGURABLE CIRCUITS FOR RADAR, COMMUNICATION, AND RADIOMETRY APPLICATIONS

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2015

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ACKNOWLEDGEMENTS

I wish to thank my advisor Dr. Cressler for his constant support and guidance. He allowed me the time and opportunity to explore, fail, and learn. As a result, I think I have grown both personally and professionally. I have found Dr. Cressler to be an excellent mentor, as well as a role model in how to achieve good balance between personal and professional life. I think the lessons I have learned from him will benefit me greatly as I move forward into the working world.

I would like to thank my reading committee members Dr. Papapolymerou and Dr. Durgin. Both of which also served as reading committee members for my masters thesis and have provided excellent insight and feedback on my work. I would also like to thank Dr. De Heer and Dr. Ulusoy for being on my defense committee. They are all busy Georgia Tech researchers and I am extremely grateful for the time they have invested in my dissertation work. I would also like to thank the members of the ECE and TSRB staff, especially Lisa, Roosevelt, and Daniela.

I would like to acknowledge the members of the Air Force Research Laboratory who have guided me in my research and helped me learn firsthand during summer internships. The feedback from Tony Quach, Aji Mattamana, Vipul Patel, Kari Grooves, and Len Pompei has been greatly appreciated. I would also like to thank the Georgia Tech Research Institute, TowerJazz Semiconductor, and IBM, who played roles in the projects and hardware fabrication that supported this work.

I would also like to thank the members of the SiGe Circuits and Devices group at Georgia Tech. I would especially like to thank my early mentors Laleh, Tushar, and Duane for having the patience to guide me as I was just beginning to learn the complexities of our field. I would also like to thank Richie who was there banging

his head against the wall with me as we began graduate school. I owe a great deal of my success to Peter, Chris, and Cagri for helping me decide which new ideas were worthwhile to pursue. I don't think I can emphasize how significant of a role Cagri has played in helping our group design working millimeter-wave circuits. Finally, I would like to thank the device experts in our group, especially Stan and Uppili, for explaining the underlying physics of the SiGe HBT and what would happen when I used the transistor in strange ways.

Finally, I would also like to thank my family for their constant encouragement. There is no doubt in my mind that I would not be where I am today without your support. Thank you for putting up with the things I have taken apart and "put back together." I promise it will continue in the years to come.

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SUMMARY

The objective of this research is to develop new reconfigurable circuits that enable significant benefits to RF and millimeter-wave systems. The ability to reconfigure RF systems can enable capabilities such as meeting multiple requirements, adapting to different environment and processing conditions, calibrating system performance, and monitoring system health. This work provides several examples of novel circuit designs that create reconfigurable RF capabilities in silicon-germanium platforms. The design and characterization of reconfigurable X-band LNAs is presented. In addition, several reconfigurable circuits and systems are developed at W-band. The following is a summary of the contributions of this work:

1. A comparison of the RF performance of current state-of-the-art transistors in advanced CMOS and SiGe BiCMOS platforms. This analysis has been submitted to the IEEE Transaction on Electron Devices (TED) © 2014 [1] and extends work from the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) © 2014 [2]

2. The design of reconfigurable X-band LNAs demonstrating frequency agility, linearity improvements, and gain control. This work has been published in BCTM © 2014 [3], © 2012 [4] and the Government Microcircuit and Applications and Critical Technology Conference (GOMAC) 2013 [5].

3. The development of innovative reverse-saturated SiGe HBT millimeter-wave switches. These switches have been analyzed in detail and published in the IEEE Microwave and Wireless Components Letters (MWCL) © 2014 [6], the

IEEE Transactions on Microwave Theory and Techniques (TMTT) © 2014 [7], and extend earlier ideas published in the the IEEE Topical Meeting on Silicon Monolithic Integrate Circuits in RF Systems (SiRF) © 2012 [8] and BCTM © 2013 [9].

4. The design and characterization of a front-end built-in-self-test system at 94 GHz. This work will be submitted to the the IEEE International Microwave Symposium (IMS) 2015.

5. The development of a highly-integrated radiometer with an ambient and active hot temperature references. This system will be submitted to IMS or the IEEE Radio Frequency Integrated Circuits Symposium (RFIC) 2015.

Copyright Statement

CHAPTER 1

INTRODUCTION

1.1 Origin and History of the Problem

The market for radio frequency (RF) systems has long evolved under a paradigm where once a system is built, it cannot be changed. This has resulted in vicious design cycles which quickly outdate previous chipsets. It has been recognized that building flexibility into RF systems and providing mechanisms to reconfigure the RF system can enable significant benefits, including: the ability to support multiple modulation schemes and standards with the same design, the reduction of product size and overdesign, the ability to adapt to environmental conditions such as temperature and spectral interference, the improvement of spectrum utilization, and the ability to calibrate, characterize, and monitor system health.

Creating reconfigurable radar or communication systems has been researched in both the digital and RF domains. Most of the research in the digital domain has focused on the idea of a software defined radio, which pushes as much of the RF functionality into digital domain where the functionality can be reconfigured using software. An ideal software defined radio uses a digital-to-analog converter (DAC) as a transmitter and an analog-to-digital converter (ADC) as a receiver and connects them directly to a circulator and antenna [10]. However, the ideal software defined radio is not feasible because of the limitations of DACs and ADCs in terms of sampling rate, resolution [11], noise figure [12], and power consumption [13]. As a result, there must be RF components such as filters, switches, amplifiers, and mixers that condition the signal between the antenna and the digital domain. Thus, flexible RF components are essential to create a reconfigurable system and are the focus of this research.

1.2 Silicon-based Transistor Technologies

The RF performance of silicon-based transistor technologies has improved at a remarkable rate over the past several decades. Both the n-type field effect transistor (nFET) and the silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) now report a unity gain frequency (f_T) and a maximum oscillation frequency (f_{max}) at or above 300 GHz [14, 15]. The RF performance of nFETs has improved with aggressive scaling and the subsequent reduction in the minimum feature size, along with innovations such as silicon-on-insulator, high-k dielectrics, and strained active regions. While maintaining more conservative (larger) minimum feature sizes, the RF performance of SiGe HBTs has also increased due to a reduction in both the vertical and lateral profile, and aggressive doping and bandgap engineering.

These improvements in the core transistor technologies have enabled silicon-based circuit designs and systems well above 100 GHz. In addition to high performance RF transistors, the ability to integrate dense digital back-end functionality on the same silicon die provides the potential to develop highly complex integrated circuits for short-range high-resolution radar [16], multi-gigabit/second data wireless transmission [17], and high resolution passive imaging [18] at millimeter-wave and even sub-THz frequencies.

Traditionally, the RF performance of complimentary metal-oxide-semiconductor (CMOS) and SiGe HBT transistors has been benchmarked directly at the input and output of the transistor. However, the interconnect from the bottom metal layer, where the transistor is connected, to the top metal layer, where it connects to the rest of the circuit, has a substantial impact on the usable RF performance of the transistor. This is critical since most RF circuits require the transistors to connect to the top metal layer where lower loss transmission lines and matching networks can be designed.

An old rule-of-thumb comparing SiGe HBTs and nFETs was that a SiGe HBT

could achieve similar RF performance to an nFET that was two technology nodes more aggressively scaled than the SiGe HBT [19]. This technology trend was based on the core transistor performance and did not consider the impact of the interconnect from the transistor to the top metal. As technology has continued to improve, the parasitics associated with the interconnect have played an increasingly large role in the overall RF performance at the top metal layer.

Figure 1.1 and Figure 1.2 show the measured results of the two main RF figure-of-merit (FoM), peak f_T and f_{max}, of several nFET and SiGe HBT technologies at the bottom and top metal layers, respectively. It is clear from Figure 1.1 and Figure 1.2 that very different technology trends are occurring at the bottom and top metal layer reference planes. In Figure 1.2, aggressive CMOS scaling has achieved comparable or superior f_T and f_{max} values in comparison to SiGe HBT technology at the bottom metal layer. However, Figure 1.2 shows SiGe HBT technologies achieve comparable f_T and significantly higher f_{max} values at the top metal layer in comparison to more advanced CMOS technology nodes. The FoMs reported at the top metal layer give a better indication of the usable RF performance of a technology since they are more representative of how the transistors will be utilized in circuit designs. In addition, FoMs reported at the bottom metal layer often use slightly different de-embedding techniques and reference planes, which make precise comparisons between technology nodes difficult. These results suggest that SiGe HBTs can provide superior RF performance for emerging millimeter-wave applications. This work leverages the benefits of SiGe HBTs in reconfigurable microwave and millimeter-wave circuits.

1.3 Current State-of-the-art Reconfigurable Techniques

The challenge of developing reconfigurable RF systems is to enable extra desired capabilities, while minimizing the impact the reconfigurable circuitry has on the core system performance. Reconfigurable capabilities can be developed at both the system

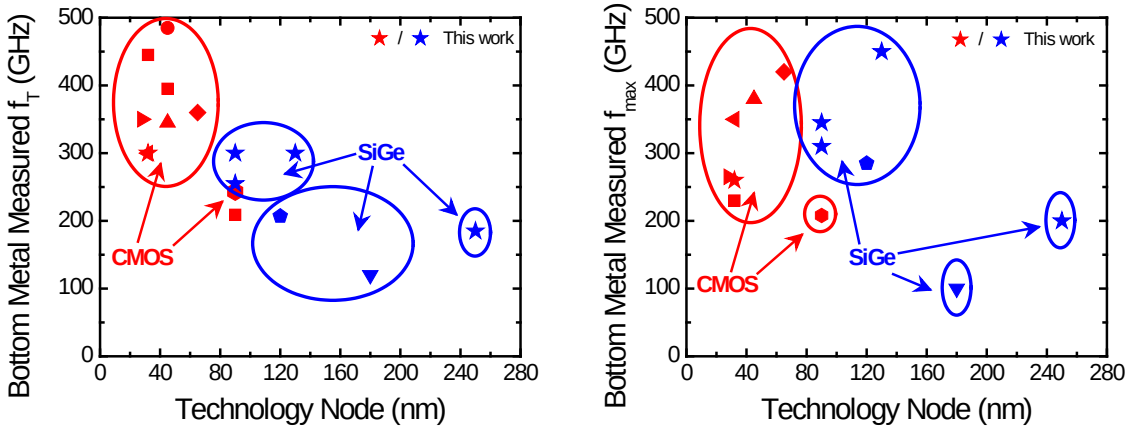

Figure 1.1: Measured f_T and f_{max} at the bottom metal layer for different technology nodes in SiGe HBT and CMOS technologies. Data points taken from this work have a star symbol. Other data points are taken from [15, 20–27] © 2014 IEEE [1].

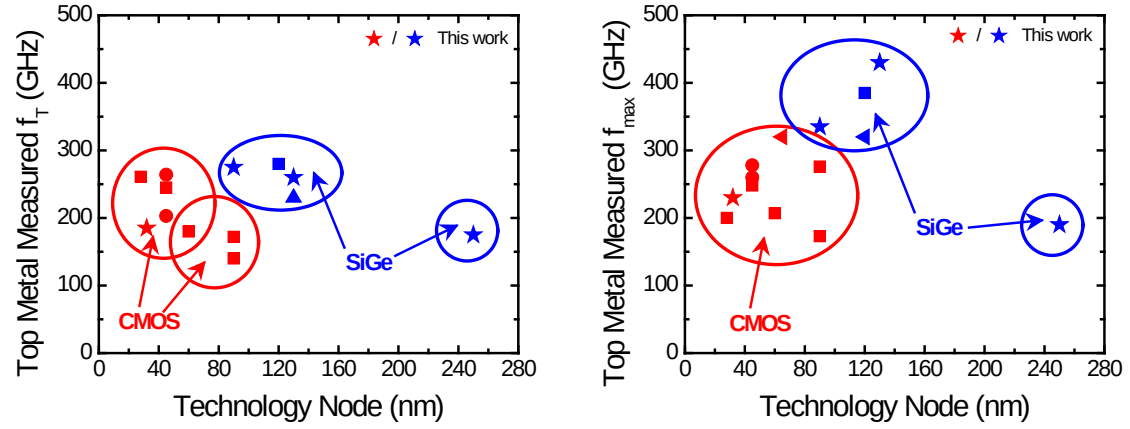

Figure 1.2: Measured f_T and f_{max} at the top metal layer for different technology nodes in SiGe HBT and CMOS technologies. Data points taken from this work have a star symbol. Other data points are taken from [28–31] © 2014 IEEE [1].

and local levels, as shown for a receiver in Figure 1.3.

At the system level, a single transceiver can be designed to operate in multiple modes with different performances by having switches that change between completely separate RF signal paths [32,33]. System reconfigurability is often used in cell phone products with dedicated channels for different communication standards [34]. To further enhance system reconfigurability, defense advanced research projects agency (DARPA) is now leading research to develop systems that operate similar to field-programmable gate array (FPGA)s, but for RF applications. The RF FPGA contain several banks of filters, amplifiers, and mixers with a matrix of switches to define the desired RF signal path [35,36]. However, system reconfigurability increases the system size and power dissipation dramatically since each mode of operation requires its own set of core RF components. Local reconfigurability modifies the RF performance within circuit blocks and reuses them in multiple modes of operation. This work focuses on creating local reconfigurability within X-band low-noise amplifier (LNA)s without increasing the circuit footprint and also explores novel reconfigurable W-band topologies.

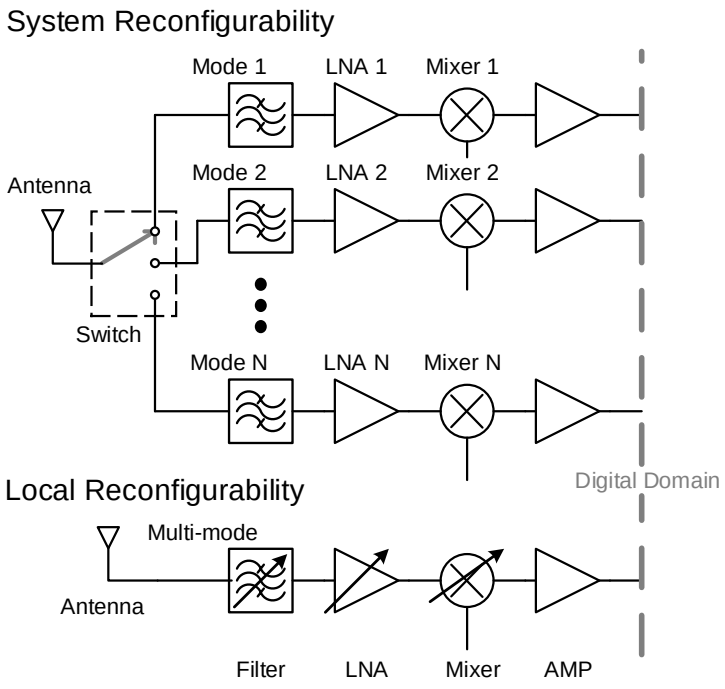

Figure 1.3: Conceptual comparison of system and local reconfigurability in a receiver.

1.3.1 Reconfigurable Low-noise Amplifiers

The LNA is the key circuit block in the receiver path. The LNA is crucial for amplifying the received signal to detectable power levels and providing sufficient gain to reduce the overall noise contribution of subsequent circuitry. Substantial research has focused on creating reconfigurable or multi-function LNAs to meet multiple cellular standards. The development of these reconfigurable LNAs can be divided into two main strategies. The first strategy develops wideband LNAs [37–39] and then uses mixers with variable local oscillator (LO) frequencies to achieve frequency agility. However, wideband LNAs suffer from higher noise figure, and they amplify a wide range of signals, both desired and undesired. Wideband amplification creates large interfering signals at the output of the LNA and can create serious linearity problems for circuits following the LNA.

An alternative approach is to create tunable narrowband LNAs. Tunable narrowband LNAs reduce the amplitude of out of band interfering signals, but require methods to modify the matching networks. Multi-mode matching networks have been achieved by using multi-tap transformers [37] or creating switchable matching networks [40–42]. Unfortunately, these networks require large passive components that increase the circuit size. This work investigates the idea of changing amplifier performance by activating additional transistor area in the amplifier core. Specifically X-band frequencies are targeted to support a large number of military communication and radar applications.

1.3.2 W-band Switches

A fundamental component to creating reconfigurable RF systems is a low-loss RF switch. Front-end switches are used in transceivers to reconfigure between transmit and receive modes of operation [43–45]. The front-end switch allows the system to use a single antenna, thereby reducing the overall footprint of the system. In addition, a front-end switch is used in passive imaging systems that use a Dicke radiometer topology to remove low-frequency gain variations from the system output [46–48]. Front-end switches are also used in digital beam forming networks to connect multiple antennas to the same RF electronics [49, 50].

Typically, millimeter-wave switches use CMOS transistors in silicon technologies [43, 46, 47] for low power consumption, but the performance of CMOS switches is significantly limited by the conductive silicon substrate. More costly III-V technologies, such as gallium arsenide (GaAs) or indium phosphide (InP), are used in applications demanding higher performance [44, 51, 52]. Previous to this work, few publications have examined the potential of SiGe HBTs in high-frequency switches [45, 48]. In [48], the performance of the high-frequency SiGe switch was similar to that of the CMOS switch, but the design did not appear to be properly optimized for the SiGe

HBT.

1.3.3 W-band Reconfigurable Systems

Providing multi-function and reconfigurable capabilities becomes difficult at millimeterwave frequencies. At millimeter-wave frequencies, greater atmospheric losses, higher noise figure sub-components, and degradation from parasitics make it difficult to achieve high dynamic range systems. As a result, the losses introduced by adding any reconfigurable capabilities must be kept to an absolute minimum. However, there is significant interest in creating built-in-self-test (BIST) capabilities for silicon-based systems. The advantage of silicon-based systems is that a large quantity of transceiver modules can be produced at a low cost and combined into a large array. Unfortunately, the measurement and verification of all the chips combined in a large array significantly increases the cost of the system. Verification is especially costly at millimeter-wave frequencies where equipment is expensive and measurements are time intensive. Thus, the ability to characterize the performance of a millimeter-wave system on die, without any expensive millimeter-wave equipment has the potential to dramatically reduce the cost of production.

One topology proposed in literature to enable BIST capabilities at W-band is shown in Figure 1.4. In this topology, a low-power reference signal is injected into the input of the receiver chain through capacitive couplers. Each channel can be activated one at a time to allow the low-power signal to propagate through the receive path to the intermediate frequency (IF) outputs. The I and Q outputs can be used to determine the amplitude and phase of the signal. Thus, the channel can be characterized in terms of gain and phase [53]. Similarly, capacitive couplers have been used at the output to of the PA to characterize the transmit path [54, 55]. This is an exciting concept that can significantly reduce measurement cost and time. However, this topology has several weaknesses. The topology only allows relative gain and

phase measurements and still must be normalized to a reference measurement with millimeter-wave equipment. The design also requires complex lossy routing such that the signal injected at channels far from the reference source are below the noise floor and cannot be characterized. In addition, the performance of the capacitive couplers changes depending on the impedance at the antenna port.

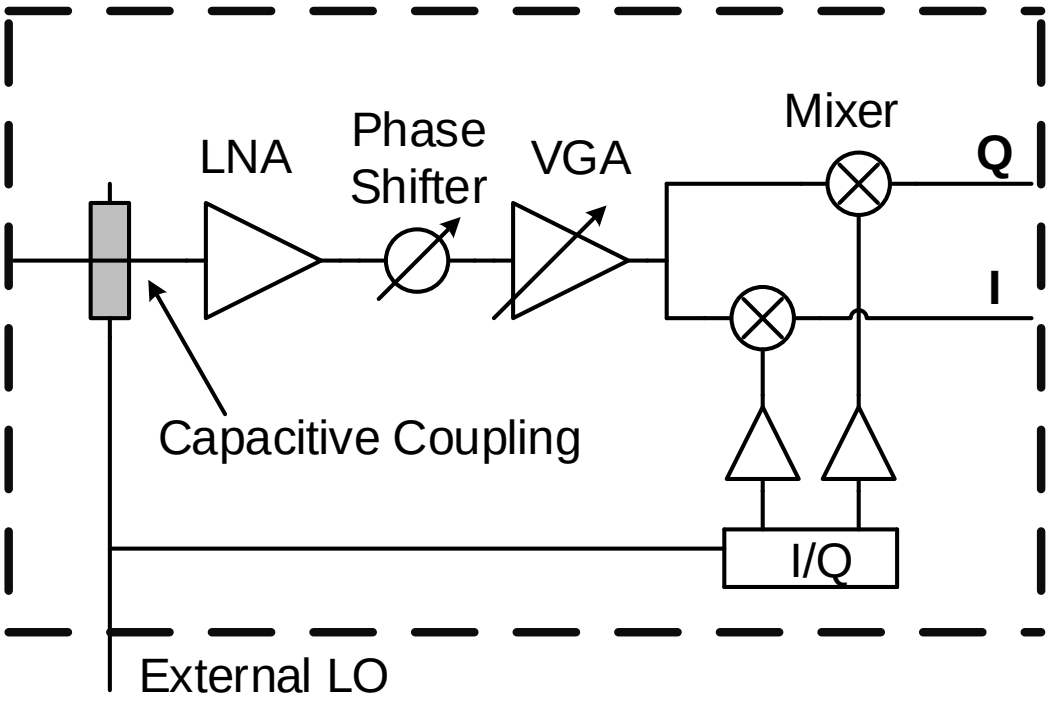

Figure 1.4: BIST topology using a low-power injection technique, after [55].

An alternative design that has been recently investigated uses a single antenna connected to a hybrid coupler. The hybrid coupler architecture allows both the transmitter and receiver to interface with antenna, as shown in Figure 1.5 [16]. The coupler allows a small portion of transmit signal to loop back into the receive path through the isolated port of the coupler. The loop back signal enables the relative gain and phase of the receiver channel to be determined [56]. The drawback to this topology is the coupler degrades the dynamic range of the system. The thru port of the coupler normally achieves about 2 dB of loss, and the coupled port has about

5-10 dB loss. If the coupled port is connected to the transmitter, the output power is reduced significantly [56]. On the other hand, if the coupled port is connected to the receiver, the noise figure of the system suffers drastically [16]. In this work, a new type of BIST architecture, which overcomes many of these challenges and can provide on chip measurements of absolute gain, and the 1-dB compression point (P1dB) is proposed.

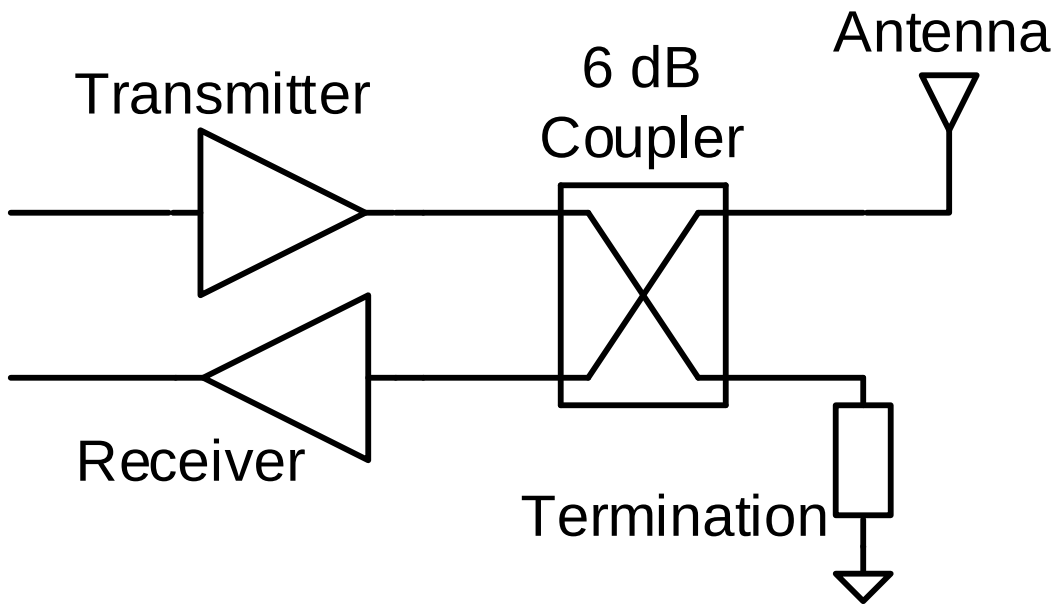

Figure 1.5: BIST topology using a hybrid coupler loop back test, after [16].

Another topic of interest for silicon-based millimeter-wave systems is radiometry and passive imaging. The goal of passive imaging systems is to measure the background thermal noise emitted by objects. Historically, radiometers have used several bulky discrete components implemented in III-V technologies and connected with waveguide interconnects [57, 58]. Due to the improvements in silicon transistor technology, there is now great interest in highly-integrated, small-footprint millimeter-wave radiometer solutions.

The calibration of radiometers is extremely critical and is often as important as the radiometer design itself [59]. The output voltage of the radiometer is related to

the received antenna noise temperature, T_A, according to Equation (1.1), where G is the gain, c is a constant related to the bandwidth of the system and responsivity of the power detector, and T_N is the noise temperature of the receiver [60].

$$V_{out} = c * (T_A + T_N) * G \tag{1.1}$$

Ideally, V_{out} would only change with a corresponding change in the received antenna noise temperature. However, as a result of the 1/f noise of active components and variations in LNA gain, G can vary over time [61]. To overcome system variations, passive imaging systems often use a Dicke switch topology in which the receiver periodically connects to a reference noise source, as shown in Figure 1.6. The Dicke radiometer topology takes the difference between T_A and a known reference noise temperature, T_R, to adjust the output voltage, as shown in Equation (1.2). The Dicke radiometer removes the impact of any variations in the receiver noise figure. In addition, when T_R is selected near T_A, the impact of gain variations is reduced.

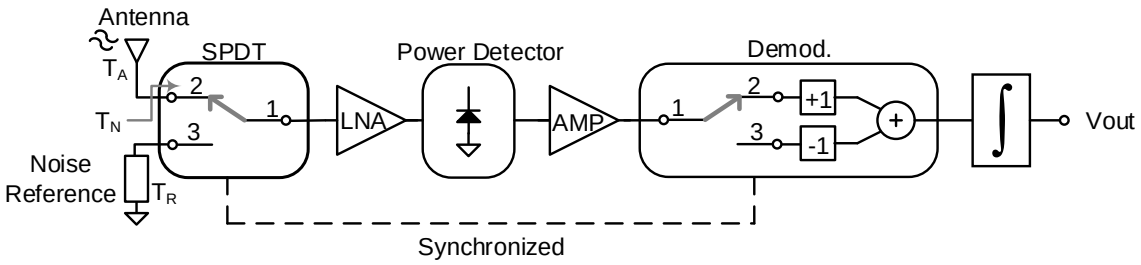

Figure 1.6: Basic Dicke radiometer topology (after [47]).

$$\Delta\ V_{out} = c * (T_A - T_R) * G \tag{1.2}$$

Unfortunately, semiconductor-based noise sources suffer from long-term drift [59, 62], and some systems require additional periodic calibration to external known reference temperatures [59, 60]. In this work, a highly-integrated Dicke radiometer is

developed with a new 4-way switch topology.

1.4 Organization

The goal of this work is to demonstrate the ability of SiGe BiCMOS processes to develop novel reconfigurable circuits and systems. Several examples are provided, which indicate that SiGe BiCMOS processes can be utilized to achieve beneficial reconfigurable capabilities. Chapter II further discusses important technology trends in the RF performance of silicon transistor technologies and indicates the future potential of SiGe HBTs in RF systems is very promising. Chapter III demonstrates multiple X-band LNA designs with local reconfigurability. Chapter IV describes the theory and development of record setting low-loss W-band single-pole double-throw (SPDT) switches utilizing SiGe HBTs. Chapter V discusses a novel W-Band BIST circuit, which reconfigures the transceiver to provide feedback on system performance. Finally, Chapter VI describes a highly integrated W-band radiometer with an innovative switch design.

CHAPTER 2

SILICON TECHNOLOGY RF PERFORMANCE TRENDS

The underlying RF transistor performance in both CMOS and SiGe HBT technology has improved tremendously over the past decade. However, as transistors begin to approach dimensions on the order of 10 nm, the impact of this scaling on RF performance must be reevaluated. The rapid scaling of CMOS technology has been driven by dense digital and memory circuitry and does not focus on optimizing RF performance. The extreme scaling of advanced CMOS nodes has a significant impact on the usable RF performance of these technologies that was not initially anticipated. To demonstrate and further analyze this impact the RF performance of state-of-the-art 32 nm silicon-on-insulator (SOI) CMOS and a half-terahertz SiGe HBT technology are analyzed in this section. The results of this comparison have significant implications for the future of high performance RF silicon circuit designs.

2.1 32 nm nFET Transistor Layout Optimization

In this section the performance of several different possible transistor layouts are compared for the 32 nm SOI nFET. Figure 2.1 shows the different transistor layouts including: (a) a single-sided gate contact (SS), (b) a double-sided gate contact (DS), and (c) a double-sided relaxed-pitch gate contact (DSRP).

The different layout configurations are compared at a bias point of $V_{DD} = 0.9$ V and $V_G = 0.6$ V for a 20 finger 32 nm x 1.0 μm high threshold voltage nFET, which has been optimized in simulation and measurement. S-parameters were measured on an Agilent E8361C PNA up to 67 GHz. A calibration to the probe tips was made using LRRM, followed by de-embedding using open and short test structures at a top metal layer reference plane. While on-die TRL has been shown to be a more accurate

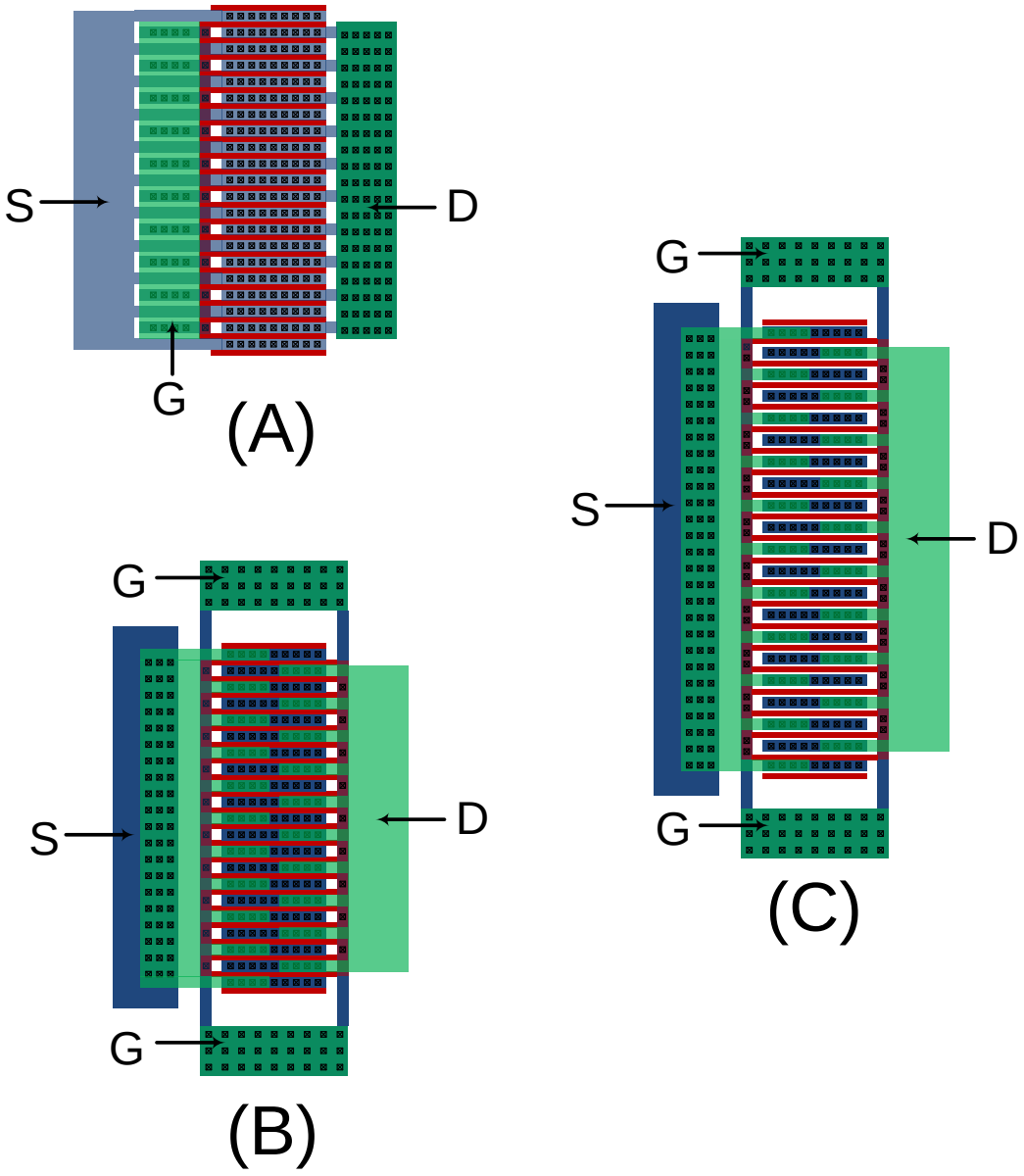

Figure 2.1: Different layout configurations for the (a) single-sided gate contact, (b) double-sided gate contact, and (c) double-sided relaxed-pitch gate contact © 2014 IEEE [1].

method to de-embed the test structure pads and feed lines [63], in this case the 100 μm feed transmission lines are below $\lambda/20$ at 67 GHz and can be approximated as the lumped element model assumed in open-short de-embedding [31].

While the SS layout is the simplest configuration, it suffers from high gate resistance. For large width transistors, the resistance of the long, relatively low conductivity polysilicon gate can degrade the overall performance of the transistor. In addition, with the SS configuration, the number of vias from the bottom metal layer to the polysilicon gate is limited. At advanced technology nodes such as 32 nm, the vias between the bottom metal layer and the polysilicon layer are more than 50 Ω per via. In a 20 finger x 32 nm x 1.0 μm nFET using the SS layout, there are only 10 vias between the polysilicon gate and the bottom metal layer. Thus, the connection between the gate and bottom metal layer immediately introduces more than 5 Ω of parasitic resistance, which reduces the f_{max} of the transistor.

The DS topology reduces the parasitic resistance by reducing the length of the current path along the polysilicon gate and by doubling the number of vias between the polysilicon and bottom metal layer. Based on the simple small-signal nFET model in Figure 2.2, the small-signal parameters related to f_T and f_{max} can be extracted from the measured Y-parameters using Equations (2.1)-(2.4) [28]. Figure 2.3 shows these small-signal parameters for the different layout configurations using measured S-parameters referenced to the top metal. The DS topology reduces the gate resistance from the SS layout an average of 45% from 20-50 GHz.

$$R_g = \frac{Re\left(Y_{11}\right)}{Im\left(Y_{11}\right)^2} \tag{2.1}$$

$$g_m = Re\left(Y_{21}\right) \tag{2.2}$$

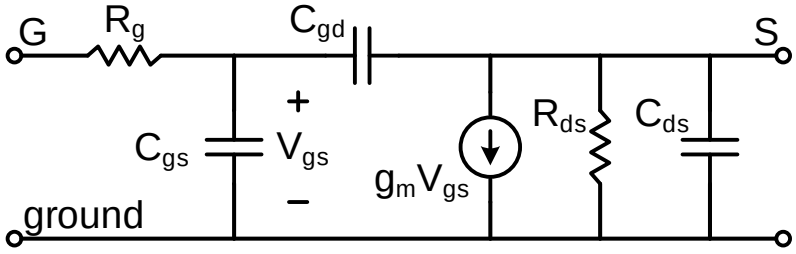

Figure 2.2: The small-signal model for the nFETs.

$$C_{gs} = \frac{Imag\,(Y_{11} + Y_{12})}{2\pi f} \tag{2.3}$$

$$C_{ds} = \frac{Imag\,(Y_{22} + Y_{21})}{2\pi f} \tag{2.4}$$

To further improve f_T and f_{max}, a DSRP layout is used to increase the transconductance (g_m) of the transistor through stress-induced mobility improvements [64] and reduce the gate to source/drain contact capacitance [15]. This option in the design kit increases the pitch between adjacent gates from 90 nm to 220 nm. The transconductance extracted from the measured Y-parameters using Equation(2.2) [28] is shown in Figure 2.3. The DSRP layout increases the transconductance an additional 7% compared to the normal pitch transistor and reduces C_{gd}, resulting in higher f_T and f_{max}.

Figure 2.4 shows the measured H_{21} and Mason's unilateral gain (MUG) of the DS configuration with the extrapolated f_T and f_{max}. While H_{21} and MUG appear to fall at the expected -20 dB/dec rate from 20-50 GHz, plotting the f_T and f_{max} across the extrapolation frequency provides a better indication of the quality of the extrapolation and the variation of the measurement. Figure 2.5 and Figure 2.6 show the measured f_T and f_{max} for the different layout configurations plotted against extrapolation frequency, respectively. Between the extrapolation frequencies of 20 and

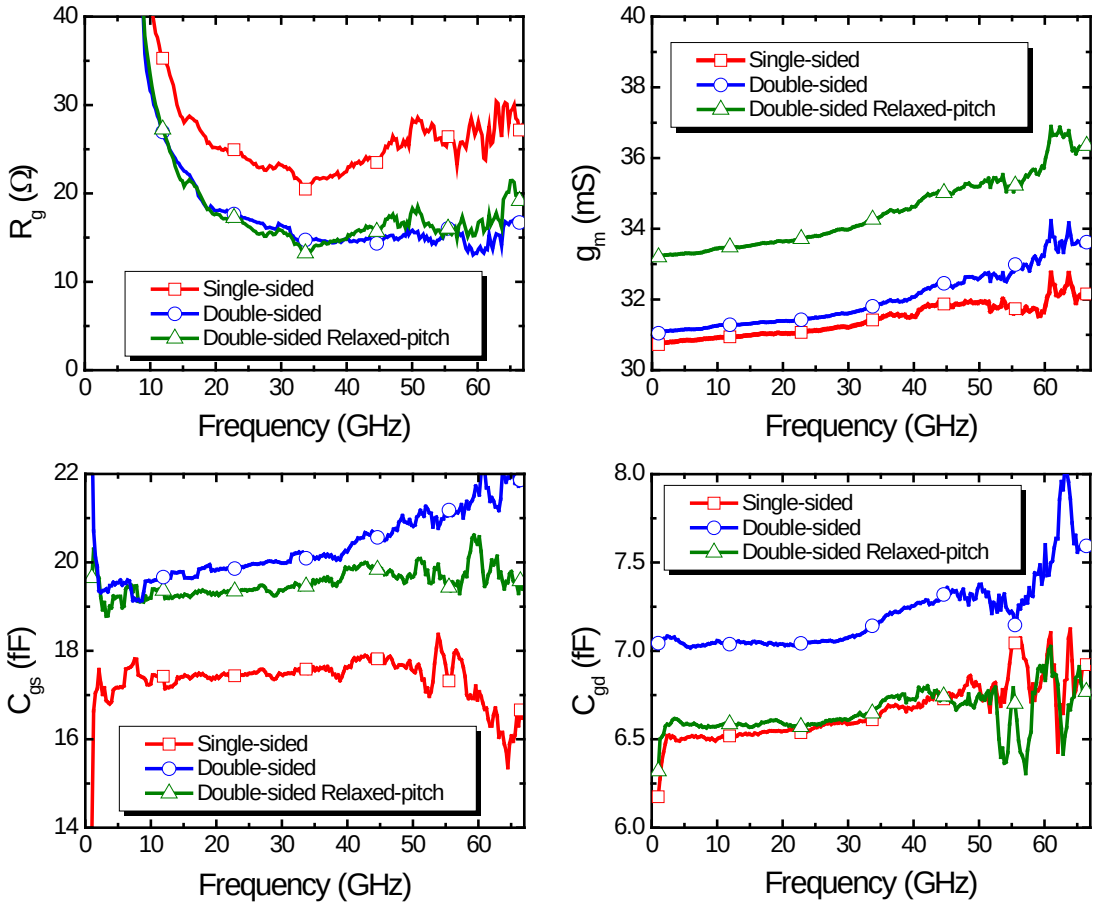

Figure 2.3: The small-signal parameters for different layout configurations extracted from measured S-parameters, including gate-resistance, transconductance, C_{gs}, and C_{gd}.

50 GHz, the variations in f_T and f_{max} are less than 4% and 15%, respectively. The post-layout parasitic extracted simulation result is also plotted for the SS layout.

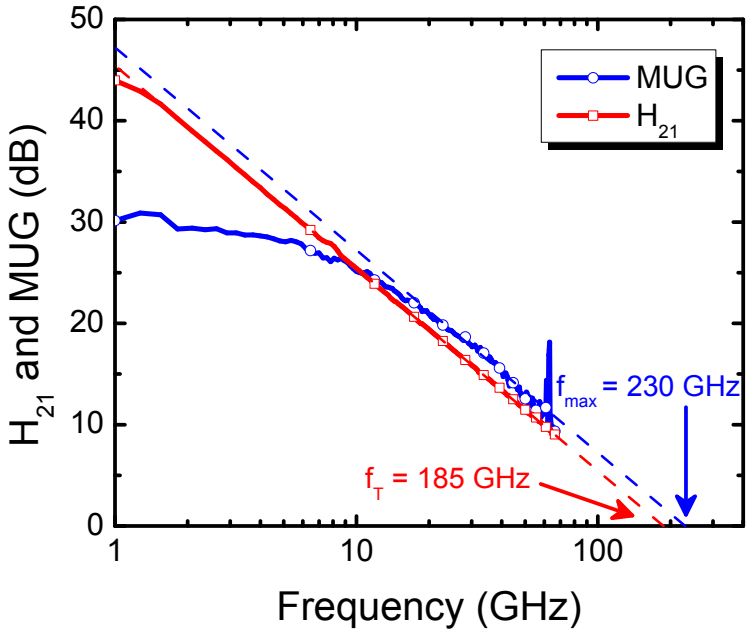

Figure 2.4: Measured H_{21} and MUG of the DS configuration © 2014 IEEE [1].

The DSRP configuration achieves the best f_T and f_{max}, with an average extrapolated f_T and f_{max} of 210 and 245 GHz, respectively, for extrapolation frequencies between 20 GHz and 50 GHz. The DSRP achieves more than a 25% improvement in the f_{max} in comparison to the SS layout result of 195 GHz. If a -20 dB/dec slope of MUG is assumed, it can be calculated from Equation (2.5) that the DSRP layout has a fixed increase in MUG across all frequencies in comparison to the SS configuration of nearly 2 dB.

$$\Delta MUG\,(dB) = 20 * log\left(\frac{f_{max1}}{f_{max2}}\right) \tag{2.5}$$

$$\Delta H_{21}\,(dB) = 20 * log\left(\frac{f_{T1}}{f_{T2}}\right) \tag{2.6}$$

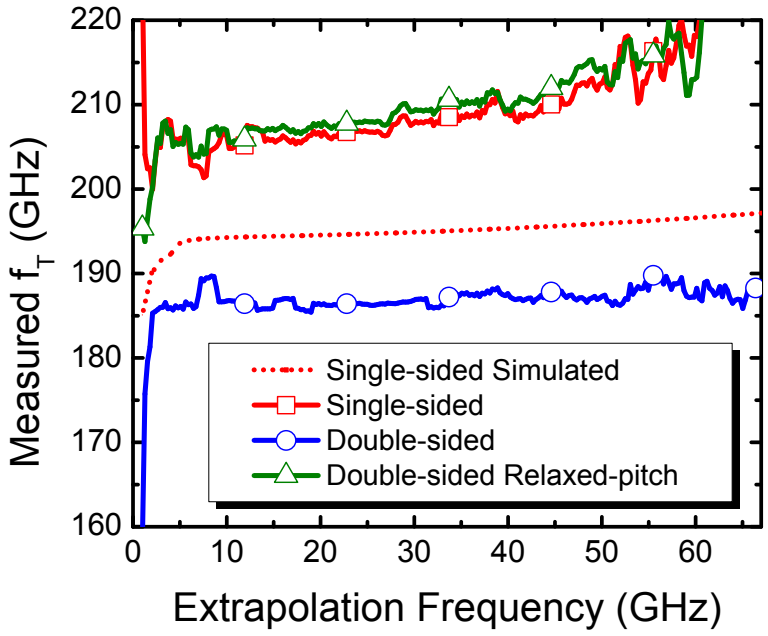

Figure 2.5: Measured f_T at the top metal for the different layout configurations plotted against the -20dB/dec extrapolation frequency © 2014 IEEE [1].

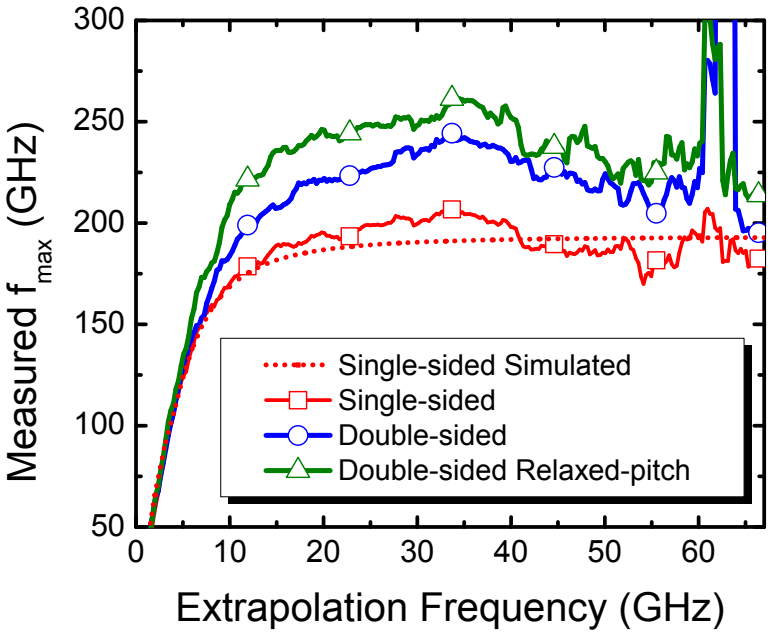

Figure 2.6: Measured f_{max} at the top metal for the different layout configurations plotted against the -20dB/dec extrapolation frequency © 2014 IEEE [1].

Additional open and short test structures were fabricated which included the interconnects to the bottom metal layer. Figure 2.7 shows the f_T and f_{max} for the DS layout referenced to the bottom and top metal layers. As seen in Fig. 8, the f_T reduces 38%, from 300 GHz at the bottom metal layer to 185 GHz at the top metal layer. In addition, f_{max} reduces 12% from 260 GHz at the bottom metal layer to 230 GHz at the top metal layer. Using Equation (2.6) and (2.5), this decrease in f_T and f_{max} from the bottom to top metal layer indicates a 4.2 dB and 1.1 dB reduction in H_{21} and MUG, respectively, across all frequencies.

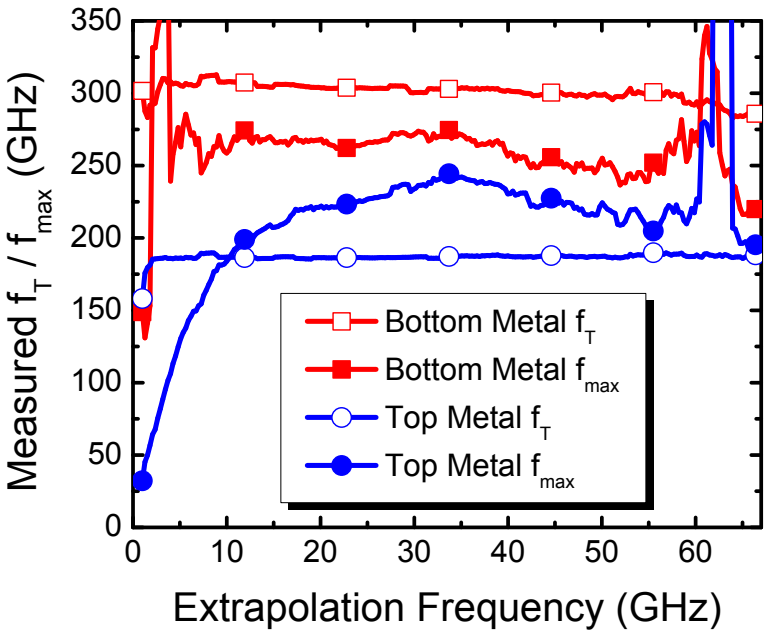

Figure 2.7: Comparison of the measure f_T and f_{max} at the bottom and top metal layers plotted across the -20dB/dec extrapolation frequency © 2014 IEEE [1].

2.2 Measured 120 nm SiGe HBT Performance

Transistor test structures from the innovations for high performance (IHP) state-of-the-art 0.5 THz SG13G2 (G2) technology were used to analyze the impact of interconnects on SiGe HBT performance [2]. The interconnect was optimized to achieve high f_{max} at the top metal layer.

Figure 2.8 presents the simulated peak f_T and f_{max} for a 4-finger 3.6 μm emitter area G2 SiGe HBT for varying numbers of via rows connecting to the device. The G2 technology provides seven metallization layers. In these simulations, the number of metal-1 (M1) to metal-5 (M5) layer vias is swept by increasing the number of via rows, with each row having 15 vias. The top metal vias are kept constant in each case, as they have relatively low resistance in the G2 technology and do not impact RF performance. In Figure 2.8, the effects of the vias are determined by post-layout parasitic extraction. As can be seen, for the worst case of a single row of vias, the f_{max} of the device degrades 18%, from 460 GHz to 380 GHz. As the number of via rows is increased, the post-layout extracted f_{max} approaches the schematic simulated value, as the total series loss is reduced by the parallel connection of vias. On the other hand, f_T begins to decline for increasing numbers of vias due to the increased parasitic capacitance. Finally, in order to account for the distributed nature of the interconnect parasitics, a full-wave electromagnetic (EM) simulation was performed to model the device interconnects for the 16-row case.

A measurement procedure similar to that used to characterize the nFETs was used to characterize the SiGe HBTs. The Agilent E8361C was calibrated to the probe tips and then the pads and feed lines were de-embedded using open and short test structures. The SiGe HBT was biased through external bias-tees with V_{be} = 0.92 V and V_c = 1.5 V for peak f_{max}. The measured f_T and f_{max} of the G2 SiGe HBT at the bottom and top metal layers are shown plotted against the extrapolation frequency in Figure 2.9. The plot shows an average reduction of less than 5% in f_{max} and 15% in f_T.

Additional measurements were conducted to determine the impact of interconnects in a wide variety of SiGe HBT processes including IBM 9HP (9HP) [65], Tower Jazz SBC18-H4 (H4), and IHP SG25-H1 (H1) [66]. The results from these measurements are summarized in Table 2.1, with the 9HP measurements also shown in Figure 2.10.

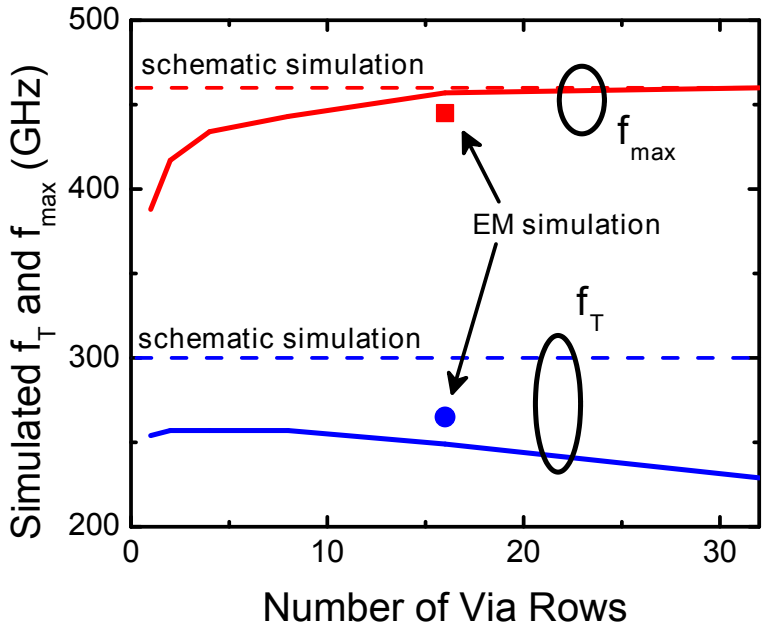

Figure 2.8: Simulation of the peak f_T and f_{max} as a function of the number of M1-M5 via rows using post-layout parasitic extraction © 2014 IEEE [1].

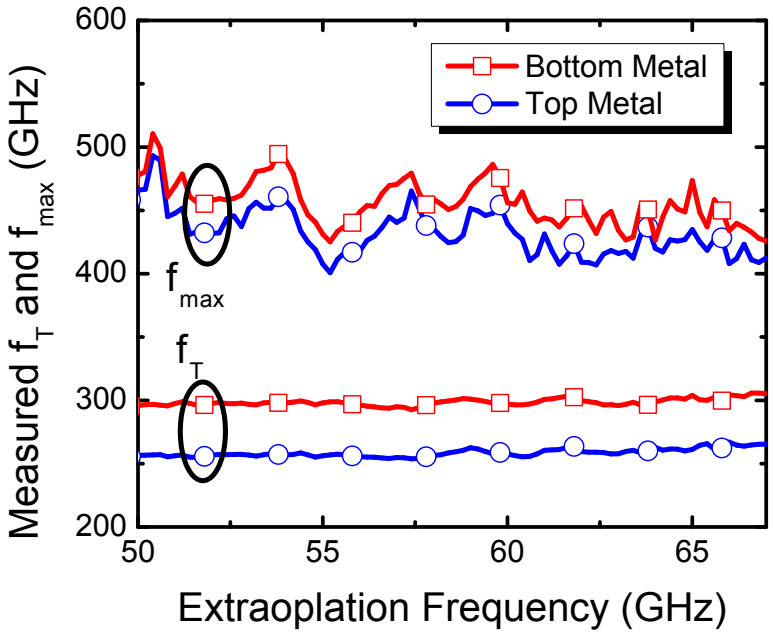

Figure 2.9: Extracted f_T and f_{max} for the top metal and bottom metal layer de-embedding planes of a 4-finger 3.6 μm emitter area G2 SiGe HBT plotted against the extrapolation frequency © 2014 IEEE [1].

All SiGe HBT technologies show a bottom to top metal layer degradation of f_T and f_{max} of less than 15% and 5%, respectively.

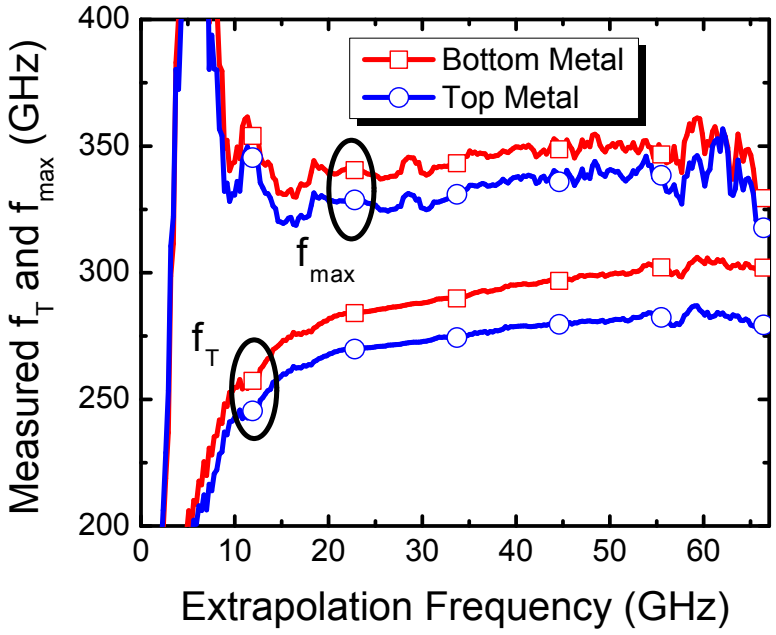

Figure 2.10: Extracted f_T and f_{max} for the top metal and bottom metal layer de-embedding planes of a 9HP 0.09 μm x 6 μm SiGe HBT plotted against the extrapolation frequency © 2014 IEEE [1].

Table 2.1: The Impact of the Device Interconnect on SiGe HBT Performance © 2014 IEEE [1]

Technology	G2	9HP	H4	H1
Emitter Width (nm)	120	90	90	250
f_T Bottom Metal (GHz)	300	300	250	185
f_{max} Bottom Metal (GHz)	450	345	310	200
f_T Top Metal (GHz)	260	280	240	175
f_{max} Top Metal (GHz)	430	335	300	190
f_T % Difference (%)	13.3	6.7	4.2	5.4
f_{max} % Difference (%)	4.4	2.9	3.2	5.0

2.3 Comparison of the Interconnect Impact on Device Performance

It has been estimated from simulations that the f_T of 45 nm SOI nFETs can

drop up to 35% from the bottom to top metal layer [67] and this work shows a 38% reduction in f_T from the bottom to top metal layer for 32 nm SOI nFETs. However, SiGe HBTs show less than a 15% reduction in f_T from the bottom to top metal layer.

The 32 nm SOI nFET has a bottom metal layer measured C_{gs} of 11 fF and C_{gd} of 6 fF. With a g_m of 32 mS, the f_T can be approximated from Equation(2.7) to be about 300 GHz. In comparison, the 4-finger G2 SiGe HBT has a measured base-emitter capacitance (C_{be}) of 28 fF and base-collector capacitance (C_{bc}) of 6 fF. The g_m is 65 mS resulting in a similar estimated f_T from Equation (2.8) of nearly 300 GHz.

$$f_{T\_nFET} = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{2.7}$$

$$f_{T\_SiGe} = \frac{g_m}{2\pi\left(C_{be} + C_{bc}\right)} \tag{2.8}$$

However, the small parasitic capacitances that are added through the interconnecting via stack have a larger impact on the overall capacitance in the 32 nm SOI CMOS process than in the G2 SiGe HBT process. In 32 nm SOI CMOS, the parasitic capacitance can contribute a significant portion of the overall capacitance and thus reduce the ratio in Equation (2.7).

While larger CMOS devices could be used with larger g_m and C_{gs}, longer gate length nFETs have increased gate resistance, and the increased resistance and capacitance associated with a bigger feed network connecting to a larger multi-finger transistor would eventually limit the benefits of this approach. However, the device size can have a significant impact on how much the parasitic interconnect capacitance degrades the f_T. This is one reason why very different f_T values can be achieved for the same advanced CMOS technology node.

It is important to note that f_T gives the RF current gain with a short circuit at

the output. This metric is relevant for circuits which drive the transistor hard at fast speeds, such as mixers or class-E power amplifier (PA)s, but it does not give a good indication of performance for small-signal amplifiers. MUG and f_{max}, on the other hand, give an indication of the maximum transistor performance invariant to any external lossless matching and are therefore more relevant performance metrics for most RF amplifier designs. An external parasitic capacitance by itself can be absorbed into the matching network and has no impact on f_{max}. However, in a more realistic case where there is parasitic capacitance at the bottom metal layer followed by a small via resistance, both the parasitic resistance and capacitance values impact f_{max}. Due to the extreme dimensional scaling in 32 nm SOI CMOS, the vias are highly resistive and the separation between metal layers is very small. As a result, the parasitic interconnect resistances and capacitances of 32 nm SOI CMOS are larger than in the G2 process. Thus, the reduction in f_{max} of 32 nm SOI CMOS is slightly higher (12%) than SiGe HBT technologies (5%).

While this work found a 12% reduction in f_{max} from the bottom to top metal layer for 32 nm SOI CMOS, it appears from Figure 1.1 and Figure 1.2 that typically advanced CMOS technology nodes have a much more significant reduction in f_{max}. One possible explanation for this is the variety of de-embedding methods and reference planes used when reporting the device level RF performance. As shown in [68], a large variety of f_{max} values can be reported for a single technology node depending on the de-embedding method used. Many of the methods report an intrinsic f_{max} that removes some of the parasitics present at the bottom metal layer. For RF designers, the top metal layer f_{max} is far more relevant than the intrinsic and bottom metal layer measurements.

Referring to Figure 1.2, the top metal f_{max} of advanced SiGe HBTs is now substantially higher than that of all currently reported CMOS technologies. Furthermore, it appears likely that the top metal layer f_{max} has peaked for CMOS technologies at

the 45-65 nm technology nodes due to increasing gate resistance [29].

2.4 Summary

This work has analyzed the current technology trends of the RF performance in both CMOS and SiGe HBT technologies. Due to the extreme dimensional scaling, the interconnect from the bottom to top metal layer is having a large impact on the usable transistor performance. It is clear the additional parasitic capacitance of the interconnect has a significant effect on the f_T of advanced node CMOS technologies where the input capacitance is low. The f_T of 32 nm SOI CMOS was reduced 38% from the bottom to top metal layer. Measured data across many SiGe HBT platforms has shown a reduction in f_T from the bottom to top metal layer of only $5-15\%$. The degradation in top metal layer f_{max} was found to be 12% in 32 nm SOI CMOS and 5% in SiGe HBT technologies. There are now multiple SiGe HBT platforms in which the top metal layer f_{max} exceeds those of all reported CMOS technology nodes. This has important implications for RF designers and indicates SiGe HBTs can provide more gain in comparison to advanced node nFETs.

CHAPTER 3

X-BAND RECONFIGURABLE LOW NOISE AMPLIFIERS

3.1 Motivation

Today's radar systems are exposed to a variety of dynamic surroundings. Changes in temperature, weather, and spectral environment all have a significant impact on radar performance. In addition, radar systems have become light-weight and mobile, making it even more important to have high performance across all environmental conditions. The US Frequency Allocation Chart in Figure 3.1 shows that the X-band (8-12 GHz) segment of the electromagnetic spectrum is very crowded [69]. X-band is a popular frequency range because the small wave length at these frequencies allows for high resolution, but the relatively low atmospheric attenuation enables longer range systems. In this congested X-band region, receivers can be subjected to high power signals that can damage amplifiers, as well as low power interfering signals.

To maintain reliable performance, multiple radar systems may be utilized in combination. For example, aircraft radar typically uses both C-band (4-8 GHz) and X or Ku-band (12-18 GHz). The C-band system is crucial because it is less susceptible to signal degradation caused by rain and fog. The X or Ku-band radar has better resolution and is used for air-traffic control radar. While having multiple radar systems can help prevent disruptions in a changing environment, it comes at a high cost. Clearly, if a single radar system could reconfigure to its environment, there would be tremendous benefits in terms of size, cost, and reliability.

Most RF systems have addressed reconfigurability at a system level by introducing banks of filters and amplifiers that can be selected to change the RF path. One example of this is an RF FPGA system being developed by DARPA and Northrop

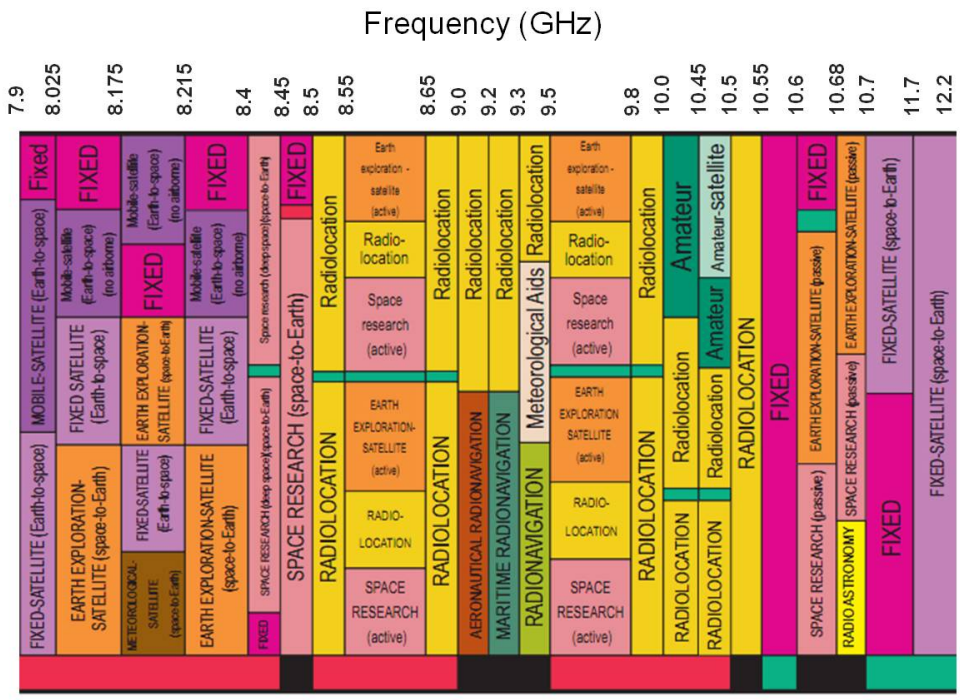

Figure 3.1: United States X-band frequency allocation chart [69]

Grumman shown conceptually in Figure 3.2. The goal of this system is to create powerful reprogrammable RF transceiver chips. By creating a RF transceiver that can reprogram performance to operate at different frequencies, power levels, and other performance metrics, a single chip can be used to meet the requirements of a large number of applications and projects, as well as adapt to different environments. Thus, the RF FPGA has the potential to significantly reduce non-reoccurring engineering and fabrications costs, as well as decrease product development time.

However, system reconfigurability has significant disadvantages. Products using system reconfigurability are usually very large in size. In addition, in order to achieve the low-loss switches required in a large switch matrix, the signals must be routed up to a separate, expensive super-strate where phase change switches can be created. There are significant benefits in terms of product size and power dissipation that can be achieved with local reconfigurability. This chapter focuses on the design of locally reconfigurable LNAs since the LNA sets many of the key FoMs for the receiver.

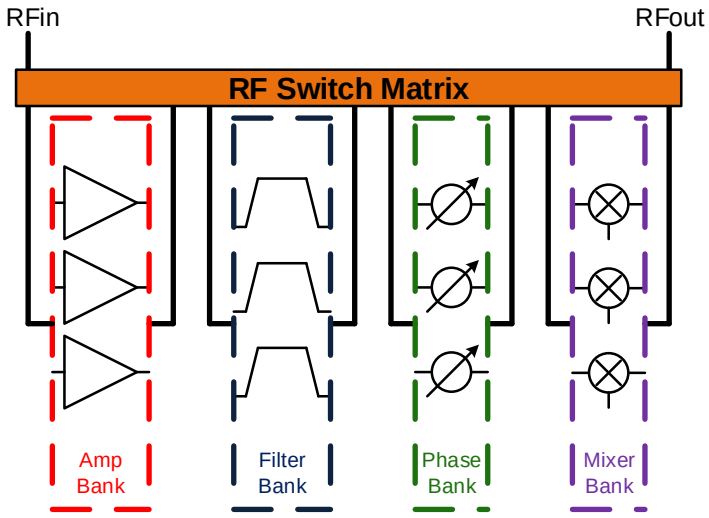

Figure 3.2: Conceptual diagram of the DARPA and Northop Grumman RF FPGA receiver chip, after [35].

In addition, having a dynamic reconfigurable LNA can relax the requirements of subsequent blocks in the receiver chain. Figure 3.3 shows a simple transmit-receive module (TRM) topology. If the phase shifter is the linearity bottleneck in the receiver, adding the capability to decrease the gain of the low noise amplifier can reduce the power of the signal going into the phase shifter and mitigate the linearity problem.

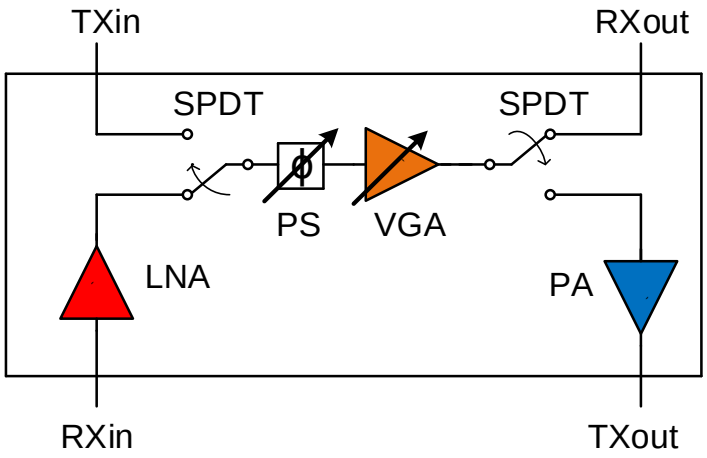

Figure 3.3: Transmit-receive module system block diagram.

3.2 Activating Additional Transistor Area

A common design approach for a reconfigurable LNA is to have switchable matching networks or varactors which allow the circuit to change to different frequencies or noise matches [70, 71]. These designs are normally large in size because the switchable networks add a significant number of passive components. In addition, this type of design is limited in its ability to reconfigure to improve linearity. An alternative approach is to activate additional transistors. Figure 3.4 shows the basic concept of having a switchable transistor core in an amplifier. The switches have been optimized with nFETs for low loss and isolation as discussed in [72] and can be used to control the state of the additional transistors.

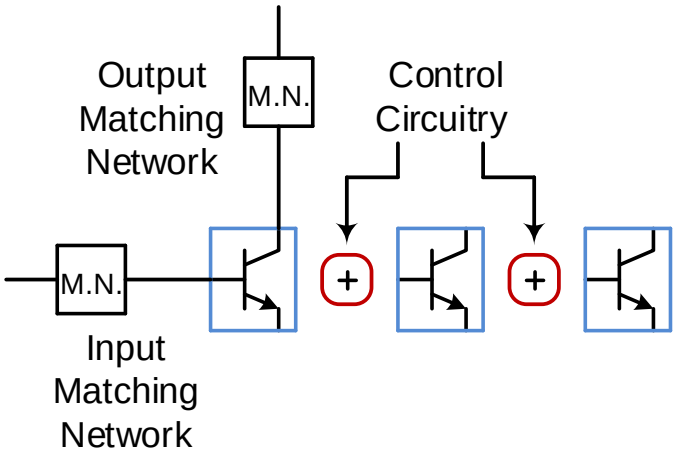

Figure 3.4: Conceptual diagram of activating additional transistor area in an amplifier.

For a single transistor LNA design, a simultaneous noise and power match can be achieved with inductors at the base and emitter. The bias point, transistor size, and emitter inductor are chosen such that $\frac{g_m}{C_{be}} L_e = 50\,\Omega$. The base inductance is then chosen to resonate out the capacitive load at the operating frequency. Figure 3.5 shows the schematic and small-signal diagram of the LNA. The input impedance of the LNA is given in Equation (3.1).

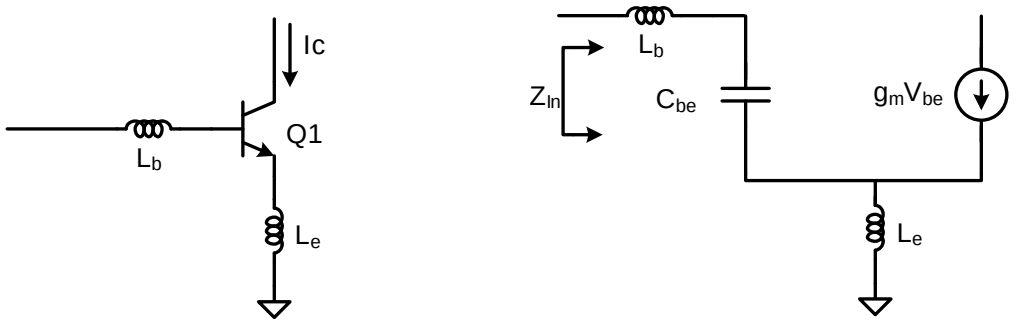

Figure 3.5: Simplified schematic and small-signal diagram of a single transistor LNA.

$$Z_{in} = \frac{g_m}{C_{be}} L_e + j\left[\omega\left(L_e + L_b\right) - \frac{1}{\omega C_{be}}\right] \tag{3.1}$$

This same approach can be used for a multiple transistor design as seen in Figure 3.6. To simplify the results, the impedance of the switch in between the two transistors is assumed to be relatively small, such that $V_{be1} = V_{be2}$. If both transistors are biased at the same current density, then the $\frac{g_m}{C_{be}}$ ratio remains the same when the second transistor is turned on and off. Looking at Equation (3.2), if the $\frac{g_m}{C_{be}}$ ratio remains constant ($\frac{g_{m1}}{C_{be1}} = \frac{g_{m2}}{C_{be2}} = \frac{g_{m1}+g_{m2}}{C_{be1}+C_{be2}}$), then the real part of the input impedance does not change when additional transistors are switched in to operation. With the switch turned on, the imaginary part of the input impedance becomes more inductive as a result of the extra base-emitter capacitance. Equation (3.3), shows the imaginary part of the input impedance resonates out at a lower frequency when the second transistor is turned on. In this way, adding transistor cores can provide frequency tuning [73].

$$Z_{in} = \frac{g_{m1} + g_{m2}}{C_{be1} + C_{be2}} L_e + j\left[\omega\left(L_e + L_b\right) - \frac{1}{\omega\left(C_{be1} + C_{be2}\right)}\right] \tag{3.2}$$

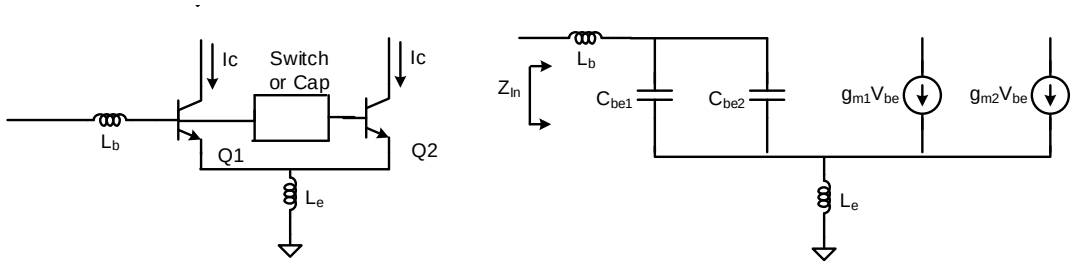

Figure 3.6: Small-signal diagram of a switchable transistor LNA.

$$\omega_0 = \sqrt{\frac{1}{(C_{be1} + C_{be2})(L_e + L_b)}} \tag{3.3}$$

This is an encouraging theoretical result, but the assumption that the switch impedance is small enough to ignore is not always accurate and is heavily dependent on how the switch is implemented. Fundamentally, there are three ways to operate this switch. One option is for the switch to turn on and off both the AC and DC current. Alternatively, the DC current could always be present and the switch could just turn on or off the AC current flow. The advantage to this topology is that the switch could include blocking capacitors at the input and output. This would allow the source-bulk and drain-bulk junctions to be reverse biased to decrease the lossy parasitic capacitances. Finally, a third option is the AC current flow could always be present, but the DC biasing could turn on or off the additional transistors.

In order to implement either the only AC or only DC switch, separate paths for the DC and AC current must be created to decouple their operation. In simulation, it was determined that the DC switch significantly outperformed the AC switch in terms of noise figure when implemented in an amplifier. The topologies shown in Figure 3.7 were selected to be further explored. The first base-switch topology uses a switch that conduct both AC and DC current. The second topology resistively biased topology uses a capacitor to separate the DC current between the two transistors while allowing the AC current to pass. In this topology, the additional transistor can be turned on

through the second resistive current mirror.

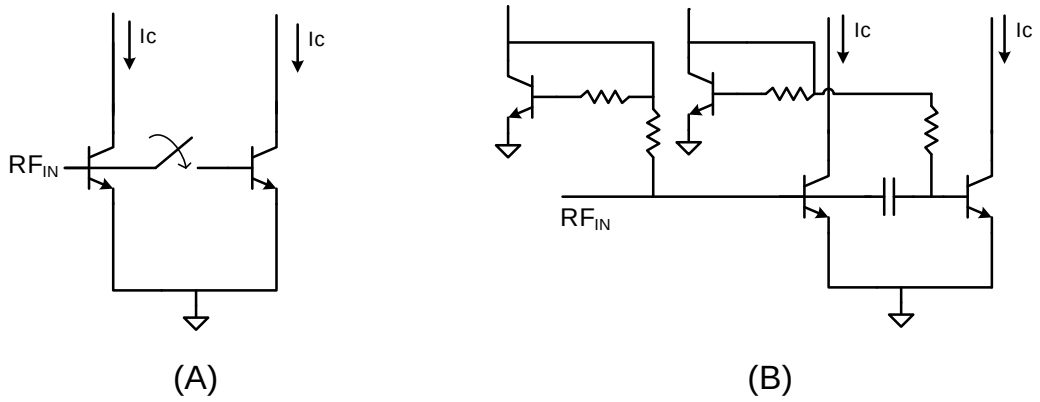

Figure 3.7: Switchable core topologies: (a) Base-switch (b) Resistive base bias.

3.3 Reconfigurable Base-switch Low-noise Amplifier

The reconfigurable base-switch LNA design uses a cascode topology, as shown in Figure 3.8. The cascode architecture is selected for several reasons. First, the common emitter stage provides a large gain and good noise figure. As a result of the large gain, the effect of the noise added by the second common base transistor is small. In addition, the low impedance looking into the emitter of the upper transistor limits the impact of the miller capacitance on the common emitter stage [74]. This increases the amplifier performance at high frequencies. The upper transistor also helps to isolate the input from output. This is especially useful in reconfigurable circuits because any changes in the input matching network have little effect on the output impedance.

The bias point, transistor size, and inductor values were chosen to achieve a simultaneous noise and power match, as described in [74]. As discussed in the previous section, by activating the additional transistor area, the input match is tuned to a different center frequency. In addition, a varactor is included at the output to modify the output matching. The bias network at the upper base node includes decoupling capacitors and small resistors to reduce the quality factor on the cascode node, which

has the potential for instability [4]. The die photograph of the reconfigurable base-switch LNA is shown in Figure 3.9. The LNA is 700 μm by 1000 μm and the added base switch functionality does not add substantially to the overall size of the amplifier.

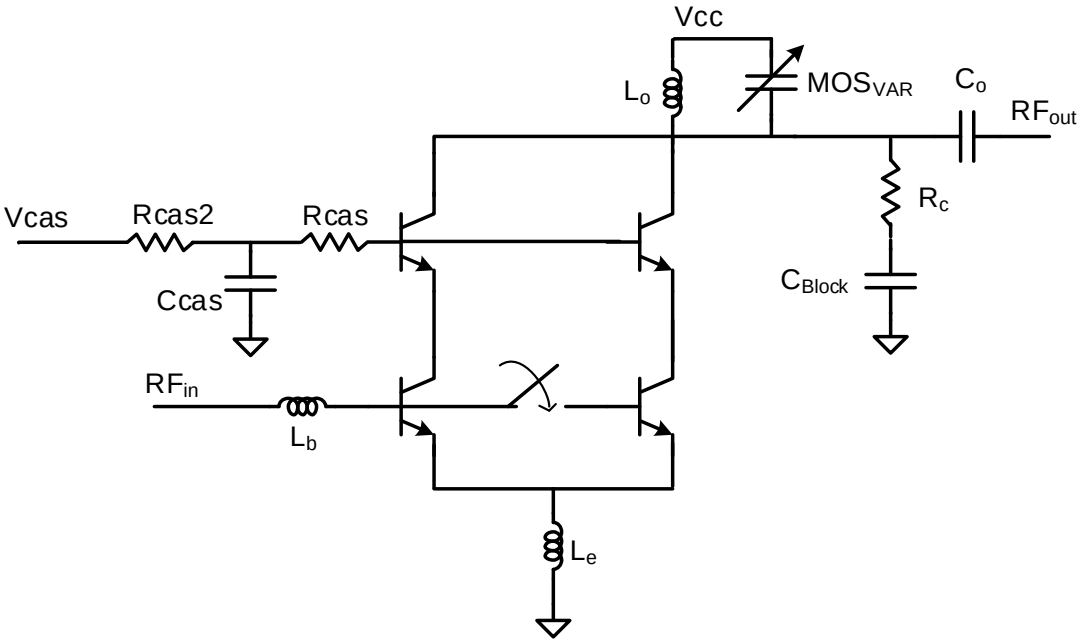

Figure 3.8: Schematic diagram of the reconfigurable base-switch LNA.

Frequency agility is achieved at the input using the base switch, as shown in Figure 3.10 and at the output using the varactor, as shown in Figure 3.11. The center frequency can be changed from 9.7 GHz to 8.2 GHz with a gain of 13-15 dB. This LNA provides a powerful set of control knobs to adjust performance in crowded spectral environments where there maybe interfering signals. Furthermore, the device sizes and matching networks can easily be redesigned to target different frequencies of operation.

The reconfigurable base-switch LNA also demonstrates that activating additional transistor area can improve the linearity of the amplifier. The IIP3 increases from -0.5 dBm to 1 dBm when the additional transistor periphery is activated, as shown in Figure 3.12. Thus, the reconfigurable base-switch LNA offers a dual solution to

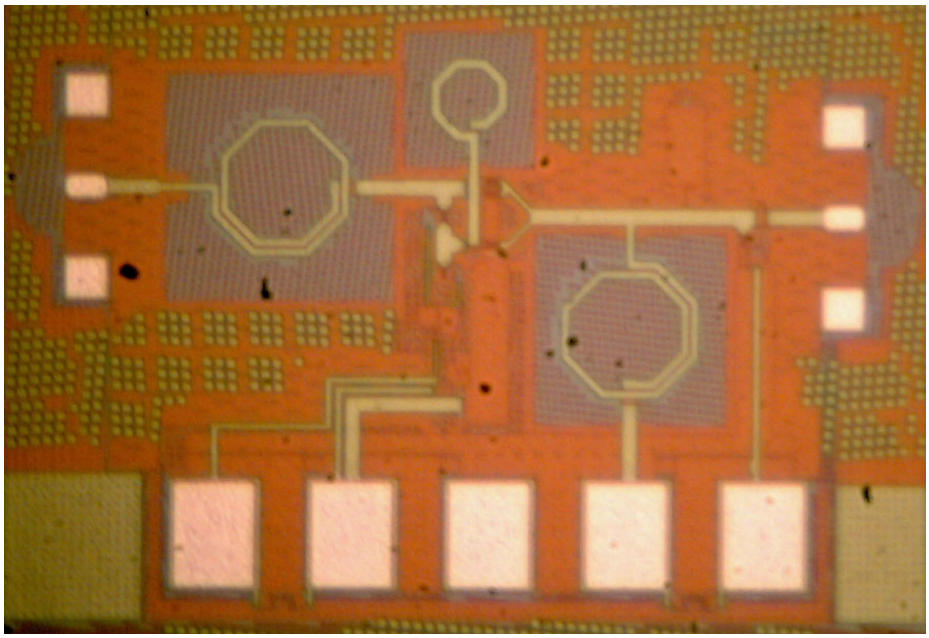

Figure 3.9: Die photograph of the reconfigurable base-switch LNA.

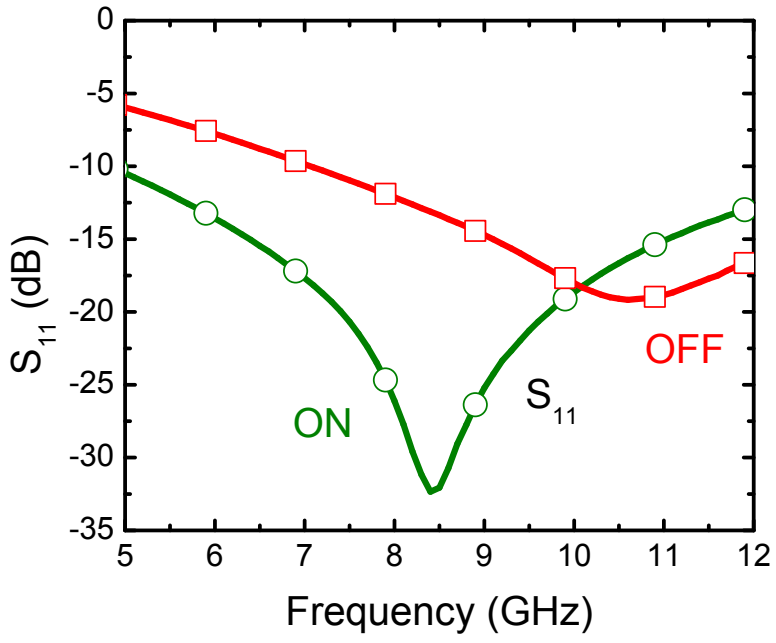

Figure 3.10: Measured S_{11} of the reconfigurable base-switch LNA in the on- an off-states.

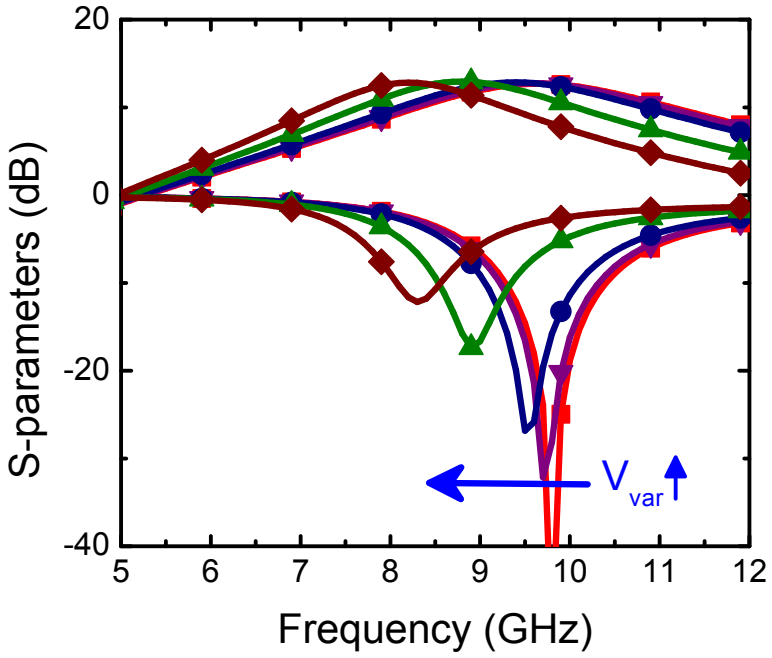

Figure 3.11: Measured S_{21} and S_{22} of the reconfigurable base-switch as a function of the varactor voltage.

interfering signals. The LNA can both change operating frequencies and improve the linearity performance. Activating additional transistor area does come at the cost of increasing the power consumption from 10 mW to 15 mW.

One problem with the reconfigurable base-switch topology is that a lossy switch element has been placed in the amplification path. When the switch is turned on, the loss of the switch is amplified to the output and degrades the noise figure of the amplifier. The noise figure of the LNA is 2.6 dB at 9.7 GHz in the off-state and 3.3 dB at 8.2 GHz in the on-state, as shown in Figure 3.13. However, this design uses a relatively unaggressive technology with a SiGe HBT f_T/f_{max} of 150/180 GHz. The noise performance will improve significantly if a more advanced SiGe HBT technology is used. In addition, as will be shown in the next section, modifications to the topology may enable reconfigurable capabilities without compromising noise figure.

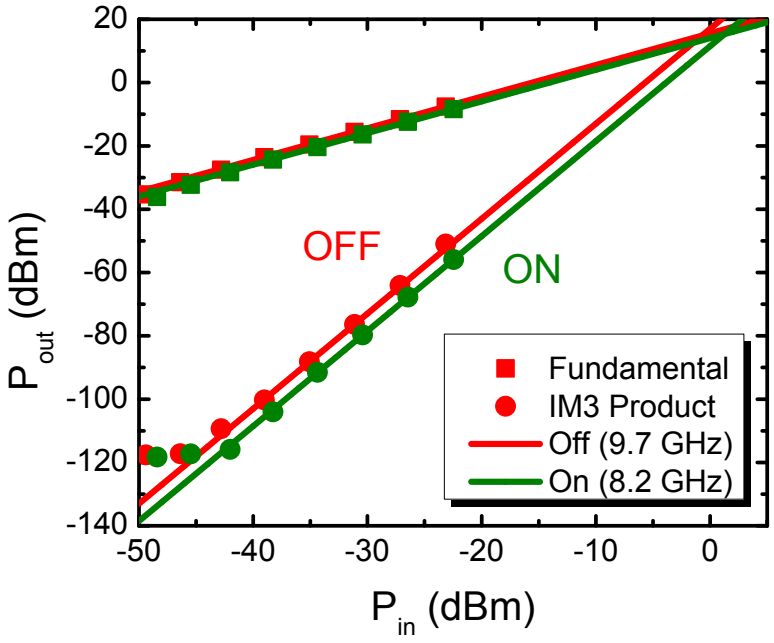

Figure 3.12: Measured two-tone linearity of the reconfigurable base-switch LNA in the on- and off-states.

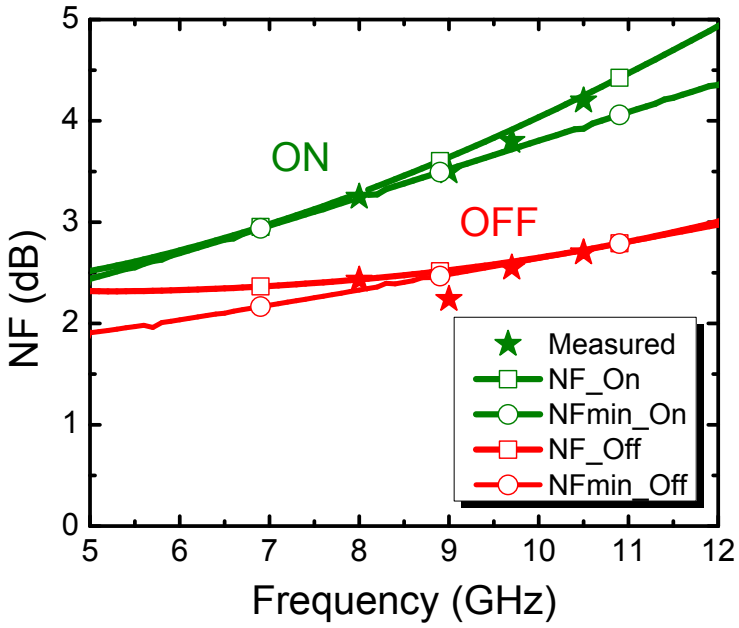

Figure 3.13: Measured noise figure of the reconfigurable base-switch LNA in the on- and off-states.

3.4 Reconfigurable Resistively Biased Low-noise Amplifier

To reduce the noise figure of the reconfigurable base-switch LNA, the lossy switch must be eliminated. An alternative method to activate transistor area is shown in Figure 3.14, where multiple current mirrors are used to separately activate different transistor cores.

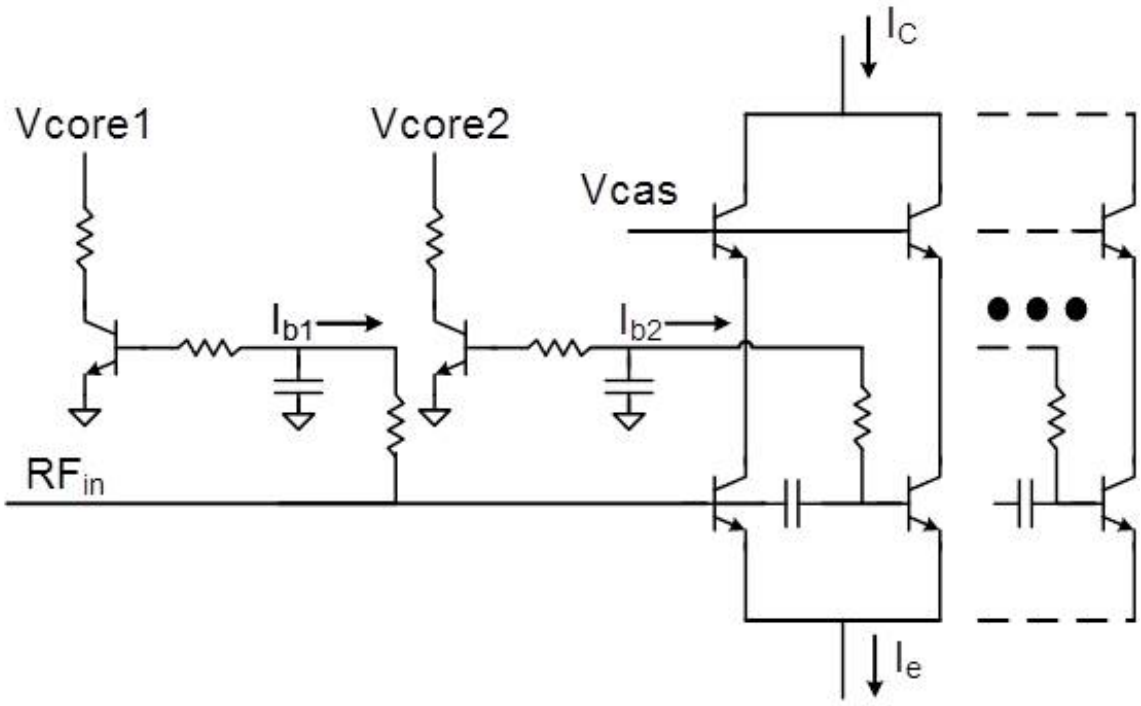

Figure 3.14: Schematic diagram of a cascode core with separate resistive current mirrors for digital activation © 2014 IEEE [3].

In Figure 3.14, the DC voltage at the base node of each transistor core is separated by using blocking capacitors. The blocking capacitors are made large in size to reduce the phase difference between amplifier cores. The resistive current mirrors enable each transistor core to be activated with a 1.0 V bias. Each core can be deactivated with 0 V bias, which prevents current from flowing through the cascode pair. Large resistors are used in the current mirrors to present a high impedance to the RF path and reduce the impact of the current mirrors on the RF matching.

A cascode structure is utilized to provide high gain and high isolation. The high

isolation between input and output is particularly beneficial for maintaining a good output match while changing the active transistor area at the input. The open-circuit voltage gain of a cascode amplifier can be derived as given in Equation (3.4)[75], where g_{m1} is the transconductance of the input transistor, $r_{\pi 2}$ is the input resistance of the cascode transistor, g_{m2} is the transconductance of the cascode device, and r_{o2} is the output resistance of the cascode transistor.

$$A_{vo} = -g_{m1} r_{\pi 2} g_{m2} r_{o2} \tag{3.4}$$

When the active transistor area is changed using the current mirrors in Figure 3.14, the effective transconductance of the common-emitter device (g_{m1}) is changed, allowing the gain of the amplifier to be controlled.

This design uses a Tower Jazz SBC18-H3 technology, which features SiGe HBTs with a selectively shrunk 130 nm emitter and an f_T/f_{max} of 240/260 GHz [76]. This aggressive SiGe HBT technology significantly decreases the base resistance of the HBTs and reduces the noise figure of LNAs. The digitally-controlled transistor core was incorporated into an X-band variable gain low noise amplifier (VGLNA). The VGLNA has three amplifier cores that are binary weighted in size with one, two, and four 6 μm emitter length SiGe HBTs, providing seven different states of operation. The transistor core blocking capacitors, C_{block}, are chosen to be 550 fF to balance the tradeoff between the phase delay and physical size of the capacitor. The current mirrors use 5 kΩ resistors, R_b, to inject the base current into the amplifying SiGe HBTs.

The schematic of the seven-state X-band VGLNA is shown in Figure 3.15. The size of the transistor core is chosen to move the optimum noise impedance toward 50 Ω. The degeneration inductor, L_e, is chosen to balance the tradeoff between achieving a good input match and providing a high gain. The output network is matched at 10

GHz using a 500 Ω resistor, 625 pH inductor and 165 fF capacitor.

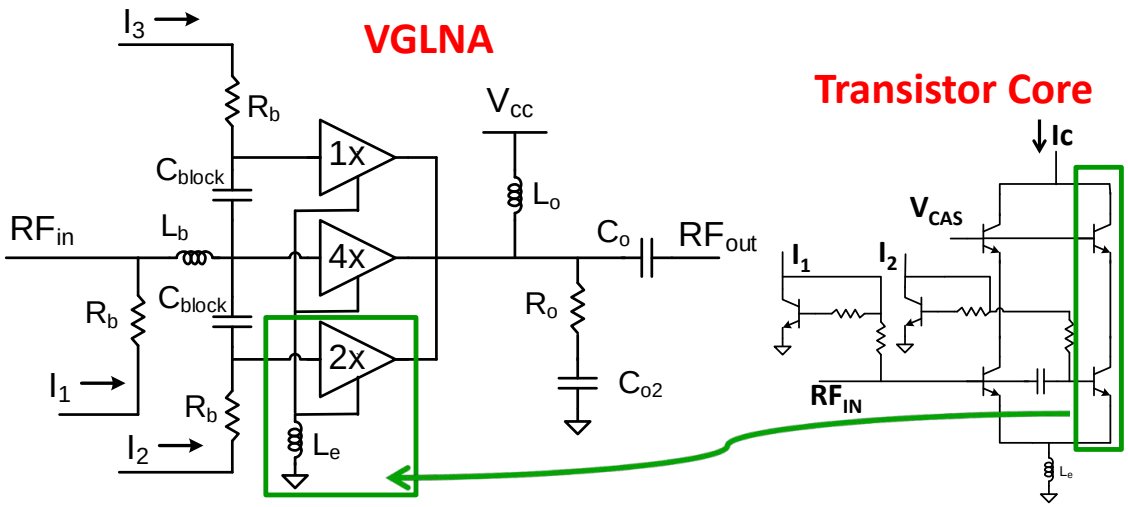

Figure 3.15: Schematic diagram of the seven-state VGLNA. Each amplifier core represents a cascode pair.

The input impedance of a degenerated LNA is given in Equation (3.5). When extra transistor area is activated, the effective transconductance g_{m1} of the amplifier increases. As a result, the real part of the input impedance increases as additional transistor area is activated, while the imaginary part remains roughly the same. This characteristic may be used to adjust the amplifier to account for process variations or changes in the antenna impedance. Figure 3.16 shows the simulated S_{11} and optimum noise impedance, Γ_{opt}, of the VGLNA at 10 GHz as the active transistor area is increased. In this case, the S_{11} has been partially compromised to achieve good noise matching.

It is interesting to note that the while the imaginary part of the input impedance changed with the base-switch LNA topology, the imaginary part of the input impedance stays relatively constant for the resistive base bias topology used in the VGLNA. This happens for a combination of reasons. In the base-switch topology, the RF switch effectively isolates the capacitive load of the second transistor core from the RF input path when the switch is turned off. However, for the resistive base bias topology

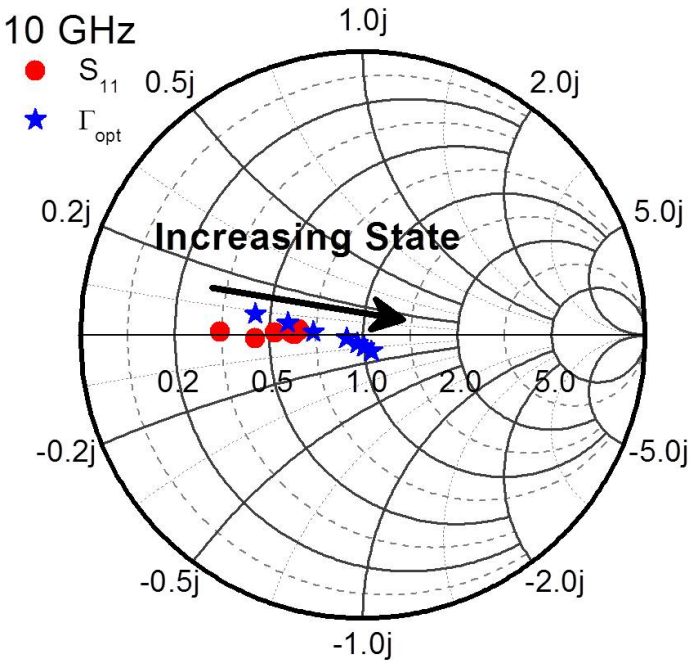

Figure 3.16: Simulated S_{11} and Γ_{opt} normalized impedances at 10 GHz as a function of the state of the transistor core © 2014 IEEE [3].

the on and off transistor cores are only separated by a DC blocking capacitor. As a result the input impedance includes the shunt base-emitter depletion capacitances of the transistor cores that are turned off. When the transistor cores are activated, the relative increase in capacitance is not as large in comparison to the base-switch topology. In addition, the parasitic resistance of the emitter inductor degenerates this increase in capacitance. Equation (3.5) shows the input impedance of the small signal model in Figure 3.5 when the parasitic resistance of the emitter inductor, R_{Le} is included.

$$Z_{in} = \frac{g_m}{C_{be}} L_e + j\left[\omega\left(L_e + L_b\right) - \frac{1 + g_m R_{Le}}{\omega C_{be}}\right] \tag{3.5}$$

As the equivalent base-emitter capacitance increases with more active transistor area, the effective transconductance and $(1 + g_m R_{Le})$ also increases and reduces the change in the imaginary part of the input impedance.

The layout of the seven-state VGLNA is shown in Figure 3.17. The final circuit is 800 μm by 950 μm including pads and 500 μm by 700 μm without pads. The digitally-controlled SiGe HBT core is only 80 μm by 80 μm. It is clear from the die photo that the added functionality of the digitally-controlled transistor core does not increase the overall size of the circuit.

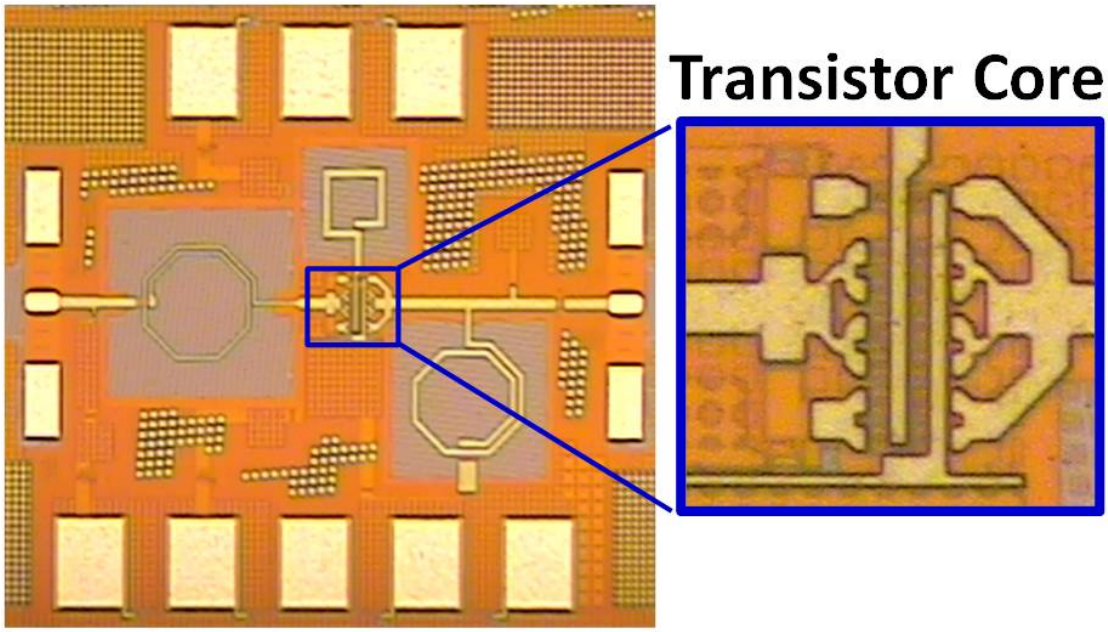

Figure 3.17: Die photograph of the seven-state VGLNA with a zoomed in picture of the transistor core © 2014 IEEE [3].

The S-parameters of the seven-state VGLNA were measured on an Agilent E8351A PNA from 1-40 GHz. The gain of the VGLNA can be digitally controlled from 9.5 to 16.5 dB, as shown in Figure 3.18. In Figure 3.19, the output return loss remains the same between different states, but the input return loss degrades for small transistor areas due to the small g_{m1}, as expected from Equation 3.5. In future designs, the input match could be improved at the cost of a slightly higher noise figure by modifying the device size and degeneration inductance. However, the input return loss is still better than 10 dB at 10 GHz for four of the seven states.

The noise figure and linearity of the seven-state VGLNA was measured using a custom-built integrated S-parameter, noise figure, and load-pull probing station

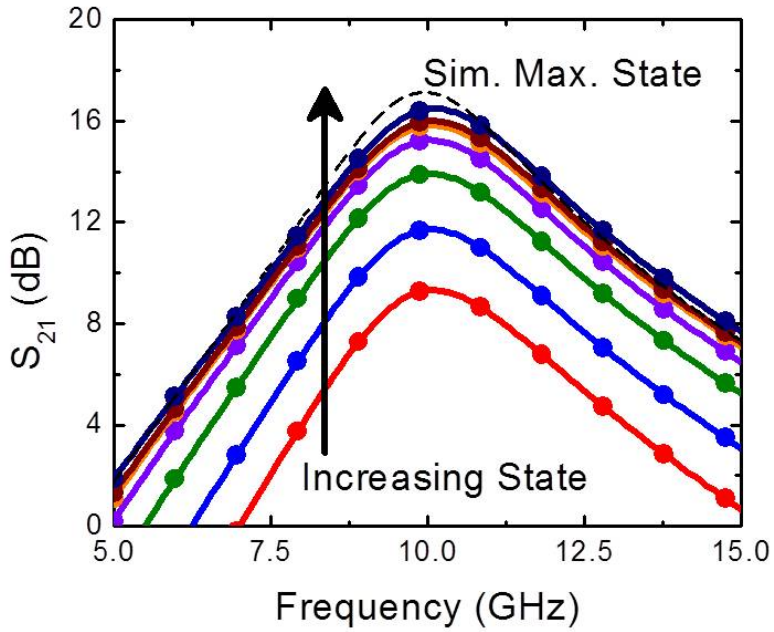

Figure 3.18: Measured gain of the seven-state VGLNA as a function of the state of the transistor core © 2014 IEEE [3].

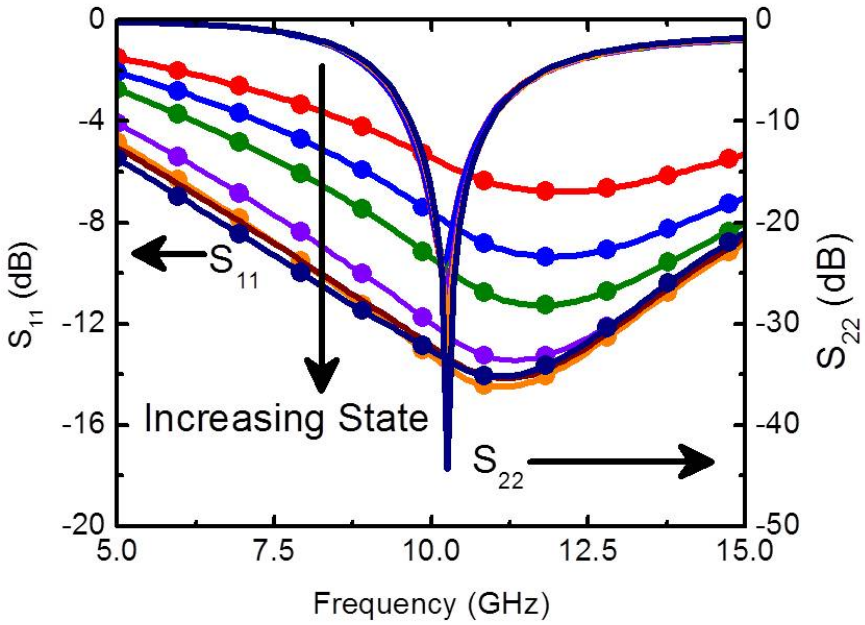

Figure 3.19: Measured S_{11} and S_{22} of the seven-state VGLNA as a function of the state of the transistor core © 2014 IEEE [3].

which provides RF switching between the network analyzer, the signal sources, and the spectrum analyzer.

Figure 3.20 compares the two-tone linearity of the amplifier with the smallest and largest transistor area activated, demonstrating the additional transistor area can also provide benefits in terms of linearity. The output referred third harmonic intercept point (OIP3) improves from 5.5 dBm in the smallest area state to 18.5 dBm in the maximum area state.

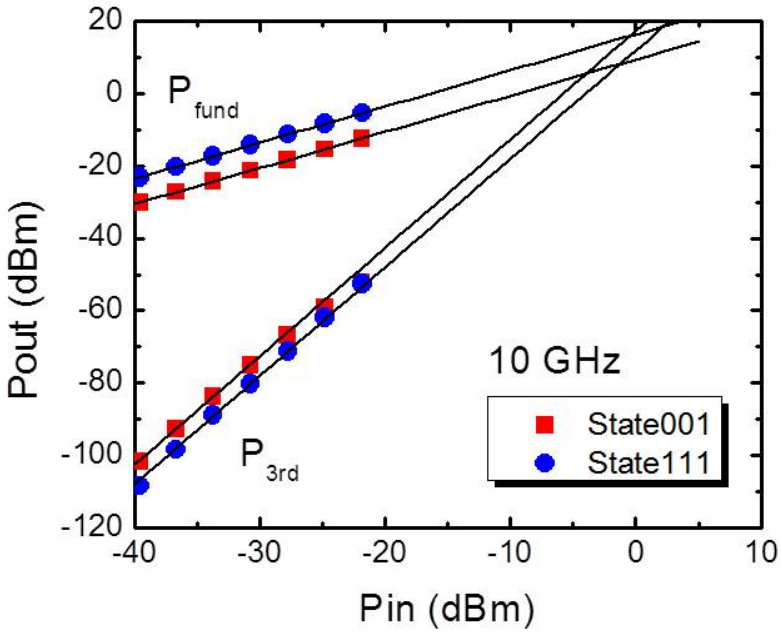

Figure 3.20: A comparison of the measured two-tone linearity of the VGLNA in the maximum and minimum transistor area states © 2014 IEEE [3].

The digitally-controlled SiGe transistor cores enable the transconductance of the amplifier to be changed by activating additional transistor area. However, the transconductance can also be increased by maintaining the same transistor area, and increasing the bias point of the amplifier in an analog fashion. To compare these two techniques, the performance of the VGLNA across the seven states is compared to the LNA with all transistors activated and the bias voltage modified to achieve the same current density as the digitally-controlled VGLNA.

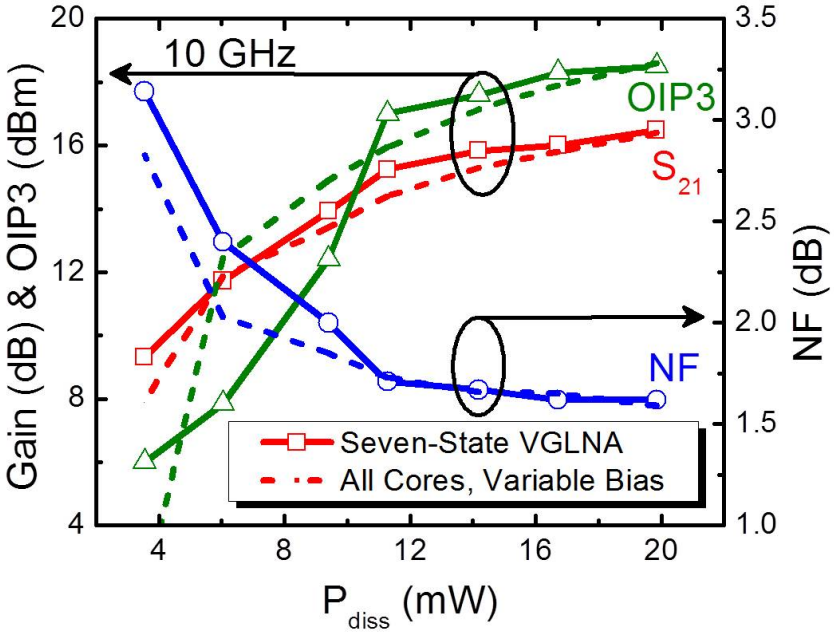

Figure 3.21: Measured gain, two-tone linearity, and noise figure for the seven-state VGLNA. The performance of the VGLNA using the digitally-controlled transistor core (solid lines) is compared to having all transistors turned on and adjusting the bias for the same current consumption (dashed lines) © 2014 IEEE [3].

The digitally-controlled VGLNA and variable bias LNA show similar performance, as seen in Figure 3.21. However, there are several benefits to the digitally-controlled VGLNA topology. First, in highly-integrated systems that require reconfigurable RF circuitry or self-healing capabilities, the variable bias LNA will be controlled by some digital logic and require a DAC. In addition, the digitally-controlled SiGe HBT transistor core offers improved reliability. Since each transistor core is biased separately, the amplifier can still function even if one of the transistor cores is damaged from radiation, breakdown, or fabrication failures.

The seven-state VGLNA also achieves excellent noise figure, with a noise figure of 1.6 dB when all transistor cores are activated and less than 2 dB noise figure for five of the seven states. This demonstrates that using resistive current mirrors in a digitally-controlled transistor core can provide lower noise figure than topologies which use switches to activate transistor area [5, 73, 77]. A clear tradeoff between the VGLNA performance and power dissipation is also shown in Figure 3.21. Based on this tradeoff, a state can be selected to meet the receiver requirements while minimizing power consumption.

A logical extension of this work is to use the VGLNA as a high performance variable gain amplifier (VGA). With good gain control and excellent noise performance, using the VGLNA as the VGA may improve transceiver performance. It also may be possible in some TRM topologies to combine the LNA and VGA to save power and reduce product size. While this is possible, it does increase the complexity of TRMs in a phased-array system. Normally in phased-array systems, it is desirable for the VGA to have low phase variation and the phase shifter to have low gain variation. This allows the control of the gain in the VGA and the control of the phase in the phase shifter to be decoupled from each other and simplifies the algorithms required for phased-array beam steering.

In this case, the VGLNA does show phase variation at the different gain states,

as shown in Figure 3.22. This is due to the extra capacitance and different trace lengths in the different transistor cores. As a result, a phased-array system using this VGLNA as a VGA would need to compensate for the phase variation in the VGLNA. Intelligent phase shifting could be utilized with a look up table to achieve specific gains and phases accounting for the phase variation. Alternatively, a second stage could be added to the VGLNA with the opposite phase variation trend [78].

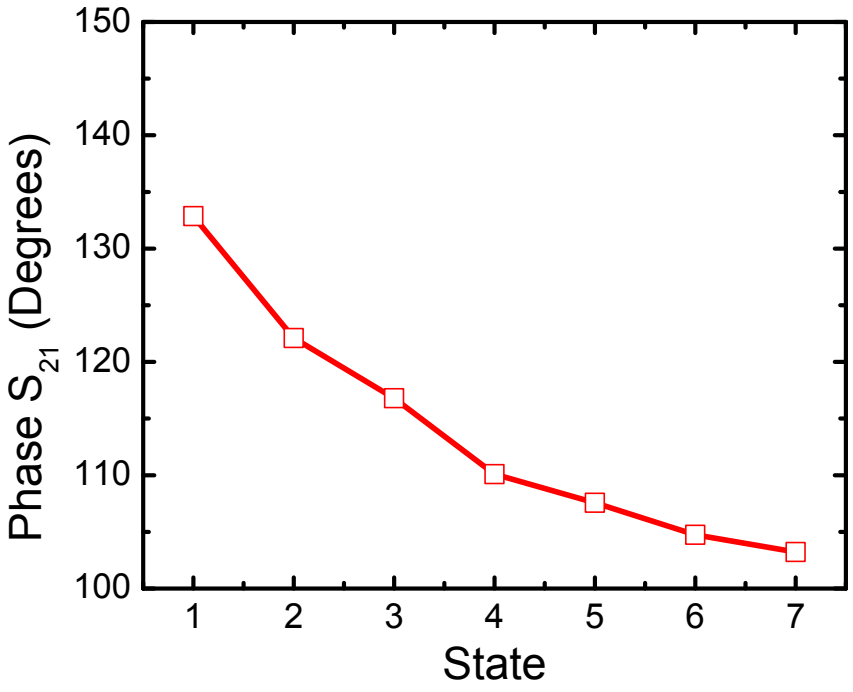

Figure 3.22: The phase shift across the input to output of the VGLNA at the different states of the amplifier

Table 3.1 summarizes the performance of published state-of-the-art VGLNAs at microwave frequencies. The digital core VGLNA presented in this work shows excellent noise figure in comparison to other publications. In addition, the power consumption is reduced in comparison to the current steering designs.

3.5 Summary

In this chapter, the ability to locally reconfigure X-band LNAs without increasing the amplifier footprint was demonstrated by activating additional transistor area.

Table 3.1: Comparison of RF Variable Gain LNAs © 2014 IEEE [3]

Ref.	Techn.	Topology	Freq. (GHz)	Gain (dB)	NF (dB)	OIP3 (dBm)	Pdiss (mW)	Area (mm^2)
This	130 nm SiGe	Digital Core	9.3-11.0	9.5-16.5	3.3-1.6	5.5-18.5	3.5-19.9	0.76
[79]	120 nm SiGe	Digital Current Steering	32.0-34.0	9.0-20.0	4.3-3.4	-10.0-1.0	26.3	0.13
[80]	180 nm SiGe	Analog Current Steering	8.0-16.0	7.5-15.0	8.1-4.5	2.0-16.0	36.0	1.17
[81]	250 nm SiGe	Analog Bias Control	1.0-12.0	-17.0-18.0	12.0-2.2	-	2.5-55.0	0.99
[75]	130 nm CMOS	Switchable Core	2.4-5.4	12.0-24.0	5.0-2.2	0.0-8.0	4.6	0.49

The base-switch LNA provided a dual solution to interfering signals with the ability to both improve linearity and change frequency of operation from 9.7 GHz to 8.2 GHz. The resistive base bias VGLNA was able to digitally control the gain, while maintaining an excellent noise figure. The VGLNA has a gain control of 7 dB, and 5 of the 7 states achieved a noise figure less than 2 dB. By introducing this gain control early in the receiver chain, the VGLNA can be used to reduce linearity limitations in subsequent circuit blocks in the receiver chain. In addition, this topology shows the potential to combine the LNA and VGA blocks in a phased-array system to reduce size and power consumption.

CHAPTER 4

W-BAND SATURATED SIGE HBT SWITCHES

Millimeter-wave electronics are rapidly becoming a ubiquitous part of everyday life. While applications at these high frequencies were once limited to specialized and expensive military and scientific systems, millimeter-wave systems are increasingly utilized in applications such as automotive radar [49,82] airport security scanners [83, 84], wideband point-to-point communication [85], and multi-Ggigabit/second wireless transceivers [17, 86].

There is a great opportunity for low-cost platforms, such as silicon and SiGe, to play a role in these potentially large volume markets. With the top metal f_T/f_{max} of 45 nm SOI CMOS reaching 265/280 GHz [28] and 130 nm SiGe achieving a top metal f_T/f_{max} of 260/430 GHz [2], silicon-based technology can now provide sufficient performance at millimeter-wave frequencies while enabling low-cost, large-scale production. Advanced W-band radar [87] and phased-array [54] systems have now been demonstrated utilizing SiGe technology.

In many applications requiring transceivers, it is often desirable to use a front-end switch so that the transmitter and receiver can share a single antenna [43–45]. Using a single antenna increases integration, and reduces array size. A front-end switch is also important for passive detection systems which use a Dicke radiometer topology to remove low frequency gain variations [46–48].

In these applications, the performance of the front-end switch is extremely critical. In a transceiver, the switch loss directly reduces the maximum output power of the transmitter. In receive mode, the switch loss is added to the signal before any amplification and directly contributes to the overall noise figure of the system. In

addition, switches need high power handling capabilities to support the large signal output of the PA. RF switches are typically implemented in CMOS [43,46,47] to minimize cost and power consumption, or in more expensive III-V technologies [44,51,52] when performance is essential. However, it has been shown that using SiGe HBTs in a novel reverse-saturated configuration can significantly improve millimeter-wave silicon-based switches and approach the performance of III-V technologies [6].

The present work demonstrates multiple new high-performance saturated SiGe HBT switch designs, which are implemented in the IBM 90 nm SiGe BiCMOS 9HP technology platform. The challenges of designing millimeter-wave switches are examined and different technology solutions are compared. A design procedure to optimize millimeter-wave switches based on theory and design equations is described. Next, the measured results of both the forward- and reverse-saturated 94 GHz SPDT switches designed using this optimization procedure is presented. The reverse-saturated SPDT achieves a state-of-the-art insertion loss of 1.05 dB with 22 dB of isolation at 94 GHz. The switching speed and power handling capabilities of the switches are examined. In addition, initial RF stress measurements show no significant performance degradation over a 48 hour stress period. Finally, an alternative switch using a transformer to minimize the circuit footprint is presented.

4.1 Millimeter-wave Silicon Switches

At microwave frequencies, most switches employ a series-shunt topology [88–90]. A typical FoM to compare the switch performance of different technologies is $1/(R_{on} * C_{off})$. This FoM is intuitive since the on-resistance determines the ability of the transistor to pass RF energy in the on-state and the off-state capacitance limits how much RF energy is blocked in the off-state. Thus, $1/(R_{on} * C_{off})$ gives a good first-order indication of a given technology′s switch capabilities.

At millimeter-wave frequencies, however, it becomes difficult to use series devices

because they add loss to the on-state and suffer from capacitive feed through in the off-state [91]. For this reason, most millimeter-wave switches only use shunt transistors. The most common topology for millimeter-wave switches above 60 GHz is the quarter-wave shunt switch topology, as shown in Figure 4.1.

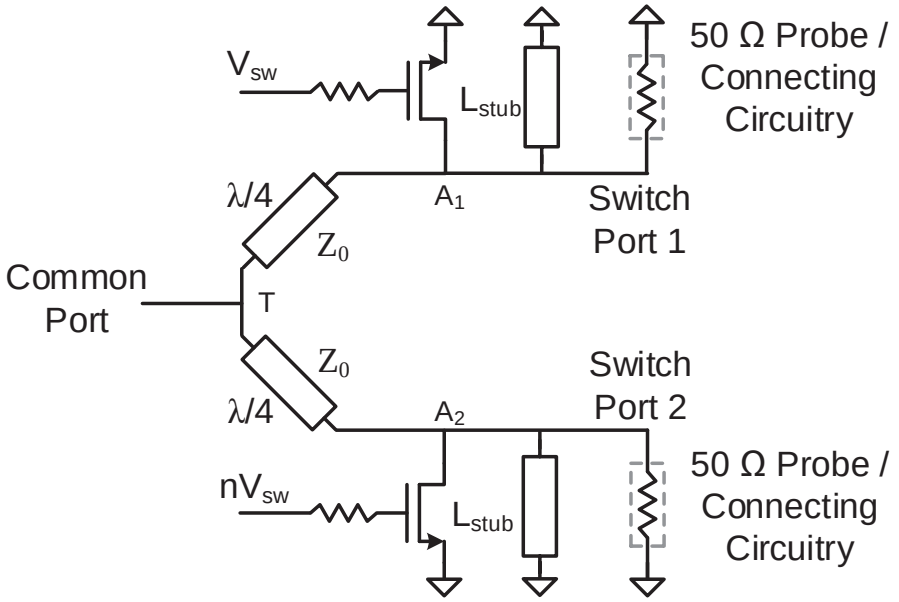

Figure 4.1: The schematic of a quarter-wave shunt switch using nFET devices © 2014 IEEE [7].

In this topology, when the upper device is turned on with a high voltage at V_{SW}, it creates a low impedance at point A1. The quarter-wave transmission line transforms the low impedance at A1 into approximately an open circuit at point T. The open circuit presented by the upper half of the switch blocks the RF energy at the Common Port from flowing towards Switch Port 1. The second device is turned off with a zero bias applied to nV_{SW}, presenting a high impedance at point A2. As a result, a low loss path is created between the Common Port and Switch Port 2. In a similar fashion, a low loss path between the Common Port and Switch Port 1 can be created by applying a low voltage to V_{SW} and high voltage to nV_{SW}. Typically, an inductive shunt stub (L_{stub}) is included with each transistor in order to resonate

out the capacitance of the shunt device at the intended frequency of operation. The insertion loss is primarily determined by how large a resistance the off-state transistor can present to the transmission line, and the isolation is determined by how small an impedance the on-state transistor can achieve.

4.1.1 Analysis of Shunt Devices

Additional insight can be gained by analyzing the small-signal switch model of a FET, as shown in Figure 4.2, where R_{ch} is the channel resistance, C_{ch} is the channel capacitance, C_{sb} is the source-bulk capacitance, C_{db} is the drain-bulk capacitance and R_b is the resistance to the substrate. For simplicity, separate substrate resistances are used for the source and drain nodes. In actuality, there is additional capacitive feed-through from drain to source through the substrate. This effect can be included by connecting the substrate nodes, but the added complexity only adds secondary effects to the equations derived in this section. For an nFET in the shunt configuration shown in Figure 4.2, the equivalent shunt resistance and capacitance are given in Equations (4.1) and (4.2).

$$R_{eq\_FET} = \frac{R_{ch}[(1 + (\omega R_b C_{sb})^2]}{1 + (\omega R_b C_{sb})^2 \left(1 + \frac{R_{ch}}{R_b}\right)} \tag{4.1}$$

$$C_{eq\_FET} = C_{ch} + \frac{C_{sb}}{1 + (\omega R_b C_{sb})^2} \tag{4.2}$$

Equation (4.1) can be simplified for both the on- and off-states of the transistor. In the on-state, when $R_{ch} \ll R_b$, the equivalent on-state resistance (R_{eq_on}) is dominated by the channel resistance, as shown in Equation (4.3).

$$R_{eq\_on} \approx \frac{R_{ch}[(1 + (\omega R_b C_{sb})^2]}{1 + (\omega R_b C_{sb})^2} \approx R_{ch} \tag{4.3}$$

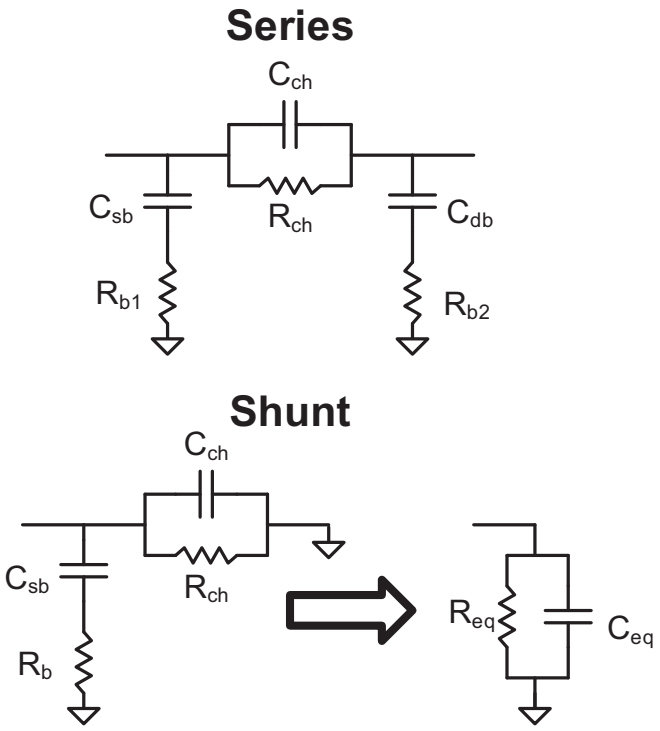

Figure 4.2: Small-signal switch model of nFET transistors © 2014 IEEE [7].

Since the off-state capacitance is normally resonated out with an inductive shunt stub, it is the equivalent off-state resistance which limits the performance of the off-state device. In the off-state, when $R_{ch} \gg R_b$, the equivalent off-state resistance (R_{eq_off}) can be derived, and is given in Equation (4.4).

$$R_{eq\_off} \approx \frac{1 + (\omega R_b C_{sb})^2}{\omega^2 R_b C_{sb}^2} \approx R_b + \frac{1}{\omega^2 R_b C_{sb}^2} \tag{4.4}$$

This theoretical result derived from the simple small-signal switch model can be compared to the results given by the design kit nFET model. The shunt R_{eq} and C_{eq} can be extracted from the simulated admittance parameters (Y-parameters) using Equations (4.5) and (4.6), where f is the desired frequency of operation.

$$R_{eq} = \frac{1}{Re\,(Y_{11})} \tag{4.5}$$

$$C_{eq} = \frac{imag\,(Y_{11})}{2\pi f} \tag{4.6}$$

R_{eq_off} has a fixed component due to the substrate resistance, and a frequency-dependent term that decreases with the square of the frequency, as shown in Figure 4.3. While at low frequencies the second term of Equation (4.4) dominates the equivalent resistance, at high frequencies the equivalent resistance can begin to approach that of the substrate resistance. Equation (4.4) indicates that the equivalent off-state resistance is maximized when R_b is either very large or very small. Unfortunately, due to the size of the transistors required to achieve high isolation, the resistance to the substrate of the transistors in most silicon switches is on the order of a couple hundred ohms and results in a relatively low R_{eq_off}. This is shown in Figure 4.4, where R_{eq_off} and R_{eq_on} are plotted as a function of a substrate resistance multiplier for a 10 finger, 8.5 μm gate width 90 nm nFET. In Figure 4.4, the substrate resistance is normalized to the value estimated by the design kit for the RF nFET layout cell. The plot indicates that unless the substrate resistance can be reduced by more than 50%, R_{eq_off} will not increase by reducing the substrate resistance. R_{eq_on}, on the other hand, shows little dependence on the substrate resistance, as predicted by Equation (4.3).

Thus, it is often more practical to increase the substrate resistance to improve R_{eq_off}. To increase the off-state resistance, techniques such as reducing substrate contact area [46], and utilizing SOI [92, 93] or triplewell technology [47, 48] are often applied in high frequency switch design to increase the substrate resistance or to decrease the coupling to the substrate. Figure 4.3 shows the simulated improvement in the equivalent off-state resistance for a triple-well device in comparison to a regular nFET.

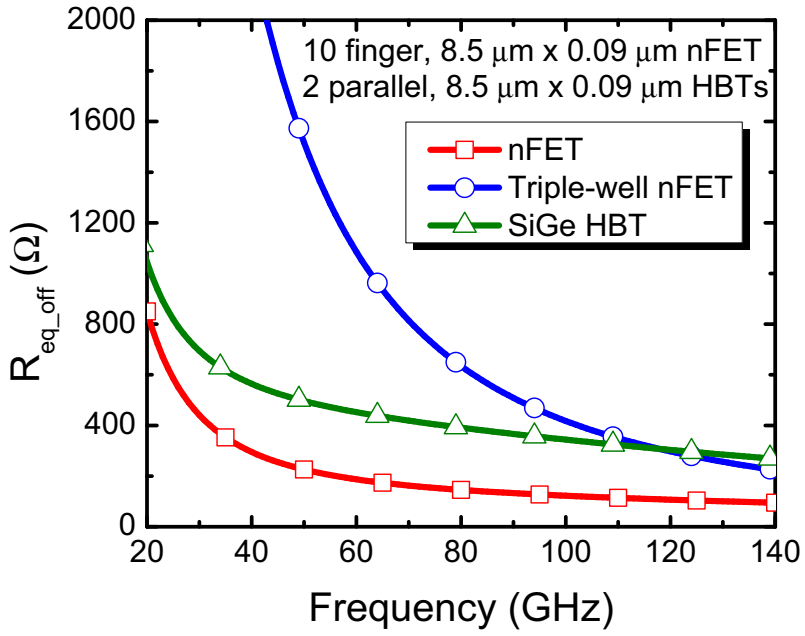

Figure 4.3: Simulated R_{eq_off} plotted over frequency for a 10 finger, 8.5 μm gate width 90 nm nFET, triple-well nFET, and 2 parallel, 8.5 μm emitter length 90 nm SiGe HBTs © 2014 IEEE [7].

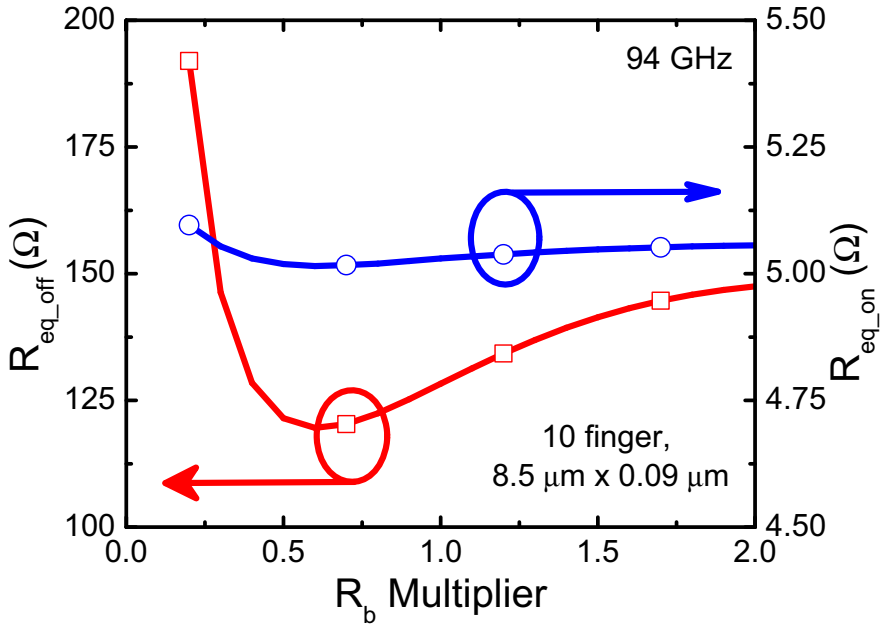

Figure 4.4: Simulated R_{eq_off} and R_{eq_on} as a function of substrate resistance for a 10 finger, 8.5 μm gate width 90 nm nFET at 94 GHz © 2014 IEEE [7].

4.1.2 Technology Comparison

SiGe HBTs can replace the nFETs in Figure 4.1, oriented such that the emitter is grounded and collector is connected to the RF node. Since the collector is also dc grounded by the shunt stub, both pn junctions of the SiGe HBT are forward-biased when a base voltage is applied and the SiGe HBT is forced into saturation. This configuration can be modeled to first order using the small signal model in Figure 4.5, where R_{cb} is the diffusion resistance of the collector-base junction, and C_{cb} is junction and diffusion capacitance of the collector-base junction. R_{be} and C_{be} are the resistance and capacitance of the base-emitter junction, C_{cs} is the collector-substrate capacitance, and R_s is the substrate resistance. If it is assumed $R_{cb} \approx R_{be}$ and $C_{cb} \approx C_{be}$ then the shunt SiGe HBT model takes a similar form to the shunt FET model and the equivalent shunt impedance equations simplify to Equations (4.7) and (4.8).

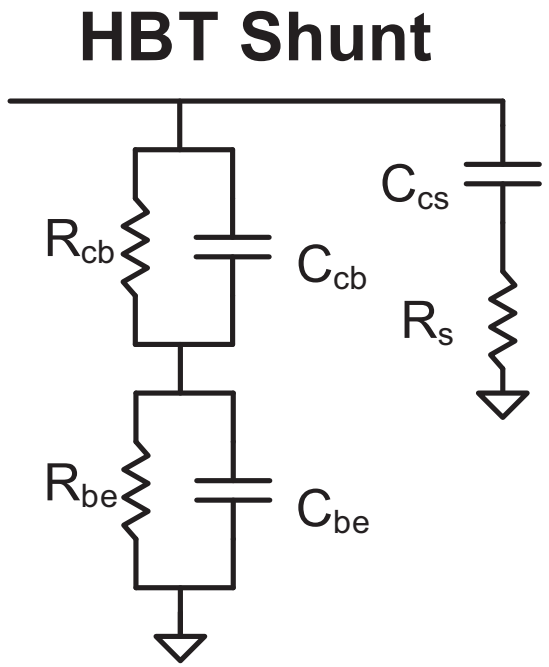

Figure 4.5: Small-signal model of the shunt SiGe HBT © 2014 IEEE [7].

$$R_{eq\_HBT} = \frac{2R_{be}[(1+(\omega R_s C_{cs})^2]}{1+(\omega R_s C_{cs})^2\left(1+\frac{2R_{be}}{R_s}\right)} \tag{4.7}$$

$$C_{eq\_HBT} = \frac{C_{be}}{2} + \frac{C_{cs}}{1+(\omega R_s C_{cs})^2} \tag{4.8}$$

The equivalent on- and off-state resistances for the SiGe HBT simplify to Equations (4.3) and (4.4), respectively, with an exchange of variables ($2R_{be} \Leftrightarrow R_{ch}$, $R_s \Leftrightarrow R_b$, and $C_{cs} \Leftrightarrow C_{sb}$). Figure 4.3 shows the equivalent off-state resistance of the shunt SiGe HBT has a similar frequency response to that of the nFET and agrees well with Equation (4.4).

It was determined that the SiGe HBT can also be flipped as shown in Figure 4.6, with the collector grounded and the emitter at the RF node, in order to create a new configuration termed reverse-saturation [6]. The equivalent off-state resistance of the reverse-saturated (reverse sat.) configuration is significantly increased in comparison to the forward-saturated (forward sat.) mode, due to improved isolation from the emitter to the conductive silicon substrate.

Figure 4.7 shows a scanning electron microscope (SEM) cross section of the 9HP SiGe HBT [65]. While the n+ subcollector comes in contact with the p- substrate and creates a parasitic junction which contributes capacitance, the emitter is physically well-isolated from the substrate. In the reverse-saturated configuration, the parasitic RC network associated with the substrate in Figure 4.5 is not present at the emitter and the off-state resistance is limited by the pn junctions and not the substrate network.

In addition, carriers in the emitter face a higher potential barrier to flow through the transistor in the off-state. The energy band diagram of a SiGe HBT with zero potential at all nodes is shown in Figure 4.8. The emitter doping is typically above

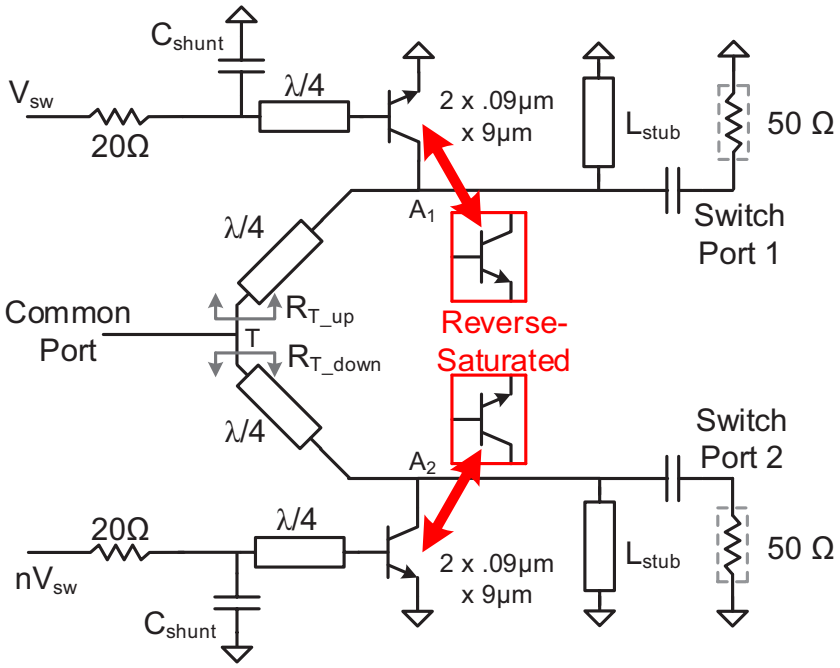

Figure 4.6: Schematic of the forward-saturated quarter-wave shunt SPDT switch. By flipping the SiGe HBT, the transistor is placed in the reverse-saturated configuration © 2014 IEEE [7].

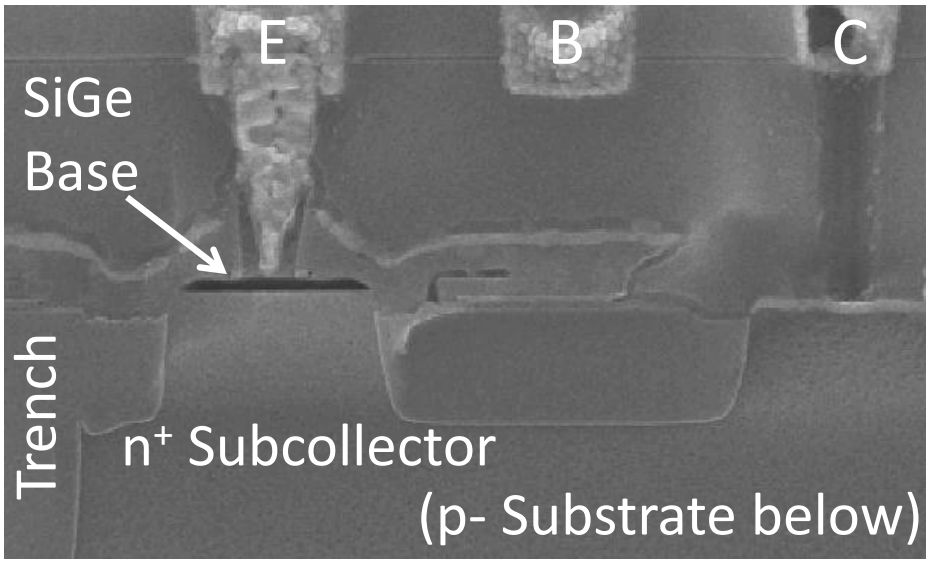

Figure 4.7: SEM cross section of IBMs 9HP SiGe HBT [65].

10^{20} cm^{-3}, whereas the collector doping is only above 10^{17} cm^{-3}. As a result, the conduction band potential barrier is higher from emitter to base (ΔE_{CE}) than from collector to base (ΔE_{CC}). The germanium (Ge) profile also has an impact on the potential barriers [94]. The higher Ge content at the collector-base junction reduces the band gap and further shrinks the collector-base potential barrier. Thus, carriers in the emitter of the reverse-saturated configuration are less likely to leak through the off-state transistor.

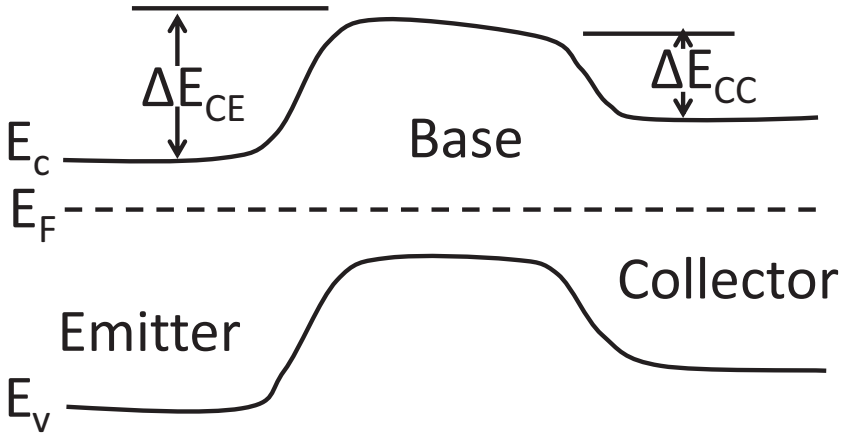

Figure 4.8: Equilibrium energy band diagram of a SiGe HBT in the off-state © 2014 IEEE [7].

Figure 4.9 compares the simulated equivalent shunt resistances, R_{eq_on} and R_{eq_off}, for the different device configurations available in IBMs 9HP technology, at 94 GHz. The R_{eq_on} and R_{eq_off} values are plotted as the device size is swept, indicating the resistance values attainable for a given technology. The nFET and triple-well devices are swept from 1-20 μm with 10 fingers and a 1.5 V gate bias. The SiGe HBTs are swept from 1-10 μm (the valid range of the RF model), with three transistors connected in parallel and a 0.875 V base bias. For each gate width or emitter length, the pair of R_{eq_off} and R_{eq_on} values is plotted in Figure 4.9.

The results in Figure 4.9 indicate that for a given R_{eq_on} value (fixed x-axis value), the reverse-saturated SiGe HBT achieves a R_{eq_off} about eight times larger than the

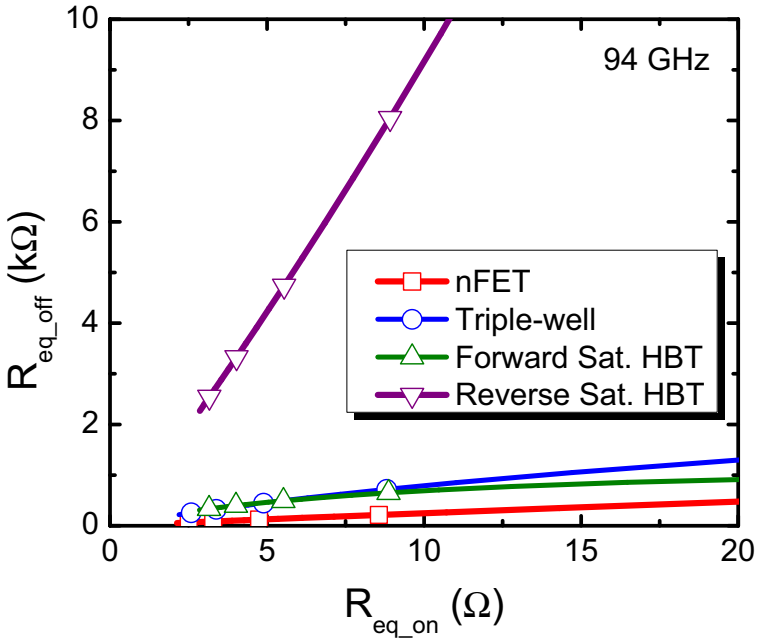

Figure 4.9: R_{eq_off} vs. R_{eq_on} for the available 9HP device configurations at 94 GHz © 2014 IEEE [7].

other configurations. In the quarter-wave shunt switch topology, the larger R_{eq_off} value prevents RF energy from leaking to ground and reduces the insertion loss. Since R_{eq_on} and R_{eq_off} both scale with the inverse of the device size, it reasonable to form a FoM for high frequency quarter-wave shunt switches, where $FoM_1 = R_{eq\_off}/R_{eq\_on}$. The R_{eq_off}*size product, R_{eq_on}*size product, and FoM_1 are listed for the different device configurations in Table 4.1.

Table 4.1: Comparison of Switch Figure-of-Merit at 94 GHz © 2014 IEEE [7]

Technology	nFET	Triple-well nFET	Forward Sat.	Reverse Sat.
R_{eq_off}*size (Ω*μm)	11,000	44,000	9,500	68,000
R_{eq_on}*size (Ω*μm)	428	440	85	85
FOM_1	26	100	112	800

4.2 Quarter-wave Shunt SPDT Optimization

To facilitate rapid design and quick approximations of technology performance, a methodology was created to optimize the quarter-wave shunt SPDT. This approach

was beneficial in reducing design iterations and providing intuitive insight into existing design tradeoffs. The following section demonstrates how this process was used to design the quarter-wave shunt SPDT with reverse-saturated SiGe HBTs.

4.2.1 Device Sizing

The primary challenge in quarter-wave shunt switch design is choosing the optimal device size. In order to compare the performance at different device sizes, the inductive stubs must be changed for each size in order to resonate out the device capacitance. To avoid an excessively iterative loop, the assumption can be made that for all devices sizes, the shunt stubs will be designed to resonate out with the equivalent shunt capacitance. In this case, R_{eq_on} and R_{eq_off} can be extracted from the Y-parameters of a shunt device and then, referring to Figure 4.6, the insertion loss (IL) and isolation (Iso) can be calculated empirically using Equations (4.9)-(4.13).

$$R_{T\_Up} = \frac{(Z_0)^2}{R_{eq\_on} \parallel Z_0} \tag{4.9}$$

$$R_{T\_Down} = \frac{(Z_0)^2}{R_{eq\_off} \parallel Z_0} \tag{4.10}$$

$$\Gamma_{in} = \frac{R_{T\_Up} \parallel R_{T\_Down} - Z_0}{R_{T\_Up} \parallel R_{T\_Down} + Z_0} \tag{4.11}$$

$$IL\,(mag) = \sqrt{\left(1 - (\Gamma_{in})^2\right)\left(\frac{R_{T\_Up}}{R_{T\_Up} + R_{T\_Down}}\right)\left(\frac{R_{eq\_off}}{R_{eq\_off} + Z_0}\right)} \tag{4.12}$$

$$Iso\,(mag) = \sqrt{\left(1-(\Gamma_{in})^2\right)\left(\frac{R_{T\_Down}}{R_{T\_Up}+R_{T\_Down}}\right)\left(\frac{R_{eq\_on}}{R_{eq\_on}+Z_0}\right)} \tag{4.13}$$

The device size can now easily be selected. R_{eq_on} and R_{eq_off} can be extracted for different sized SiGe HBTs and inserted in Equations (4.12) and (4.13) to determine the insertion loss and isolation. Figure 4.10 shows the calculated SPDT insertion loss and isolation versus emitter length for the reverse- and forward-saturated configurations. Initial simulations showed multiple HBTs were required to achieve the desired isolation. Thus, in Figure 4.10 two shunt SiGe HBTs have been connected in parallel and the EM simulations of the base and collector contacts have been included to improve the accuracy of this analysis.

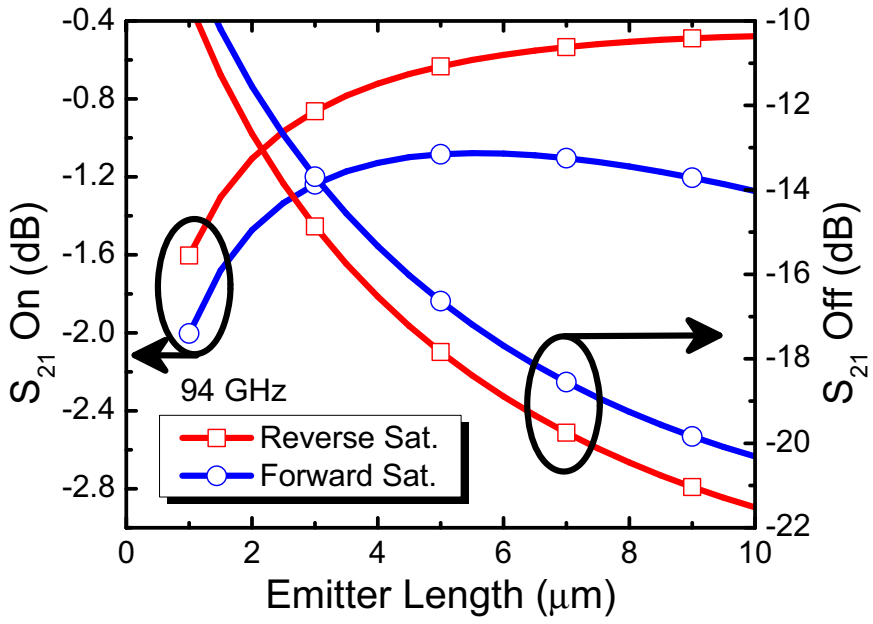

Figure 4.10: Calculated SPDT insertion loss (-1*S21 On) and isolation (-1*S21 Off) for two parallel SiGe HBTs in reverse- and forward-saturation © 2014 IEEE [7].

As the device size increases, the isolation increases, since the larger device reduces

the impedance when the device is turned on. The insertion loss initially decreases with increasing size. This is because the on-state impedance of a small SiGe HBT is not an ideal short, and as result, the impedance it presents after the quarter-wave transmission line at the T-junction is not very high. This causes power to leak towards the wrong Switch Port, increasing loss. Eventually, increasing the transistor size further reduces the equivalent off-state resistance and degrades the insertion loss due to increased capacitance and reduced substrate resistance.

It is expected that Equations (4.12) and (4.13) slightly underestimate the switch loss because ideal loss-less quarter-wave transmission lines are assumed. However, Equations (4.12) and (4.13) provide an excellent approximation for selecting the optimal device size. In this case, a SiGe HBT emitter length of 9 μm was selected for both the forward- and reverse-saturated configurations to balance insertion loss and isolation and provide a fair comparison between the two configurations.

4.2.2 Matching Networks

After selecting the device size, the inductive matching stubs can be designed. The stubs should resonate out with the equivalent shunt capacitance at the desired center frequency, according to Equation (4.14).

$$L_{stub} = \frac{1}{(2\pi f)^2 C_{eq\_off}} \tag{4.14}$$

For nFET switches, the equivalent on- and off-state capacitances are nearly the same. However, this is not true for bipolar switches, since the capacitance of a bipolar device is heavily dependent on the bias current [94]. The stubs should be designed to resonate with the off-state capacitance and not the on-state capacitance. For the quarter-wave shunt switch topology in Figure 4.6, it is the Switch Port with the off-state transistor that creates the low-loss path to the Common Port. Thus,

in order to have a high return loss at the Switch Ports, the capacitance of the off-state device must be resonated out. In addition, when the shunt device is turned on, the inductive stub is in parallel with a low impedance and has little impact on the combined equivalent shunt impedance. That network still presents a large RF impedance at the T-junction, even if the reactance is not completely resonated out.

The inductive stubs and transmission lines were implemented using microstrip lines. The back-end-of-the-line (BEOL) in IBM 9HP features 9 copper metal layers and a top aluminum layer. The microstrip lines utilized the top aluminum metal and a combination of metal 3 and metal 2 for a ground plane. Metal 1 was reserved for dc routing below the ground plane. The cross-section of the microstrip line is shown in Figure 4.11. The transmission line has an EM simulated loss of 0.38 dB/mm at 100 GHz.

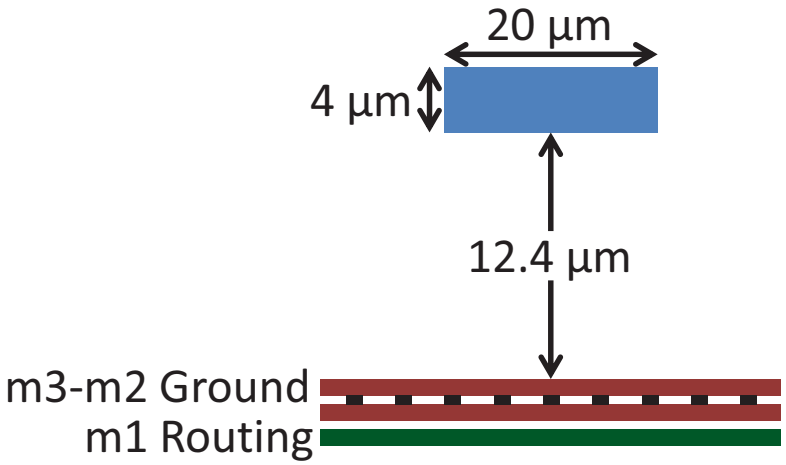

Figure 4.11: The cross section of the microstrip lines with a characteristic impedance of 50 Ω © 2014 IEEE [7].

Creating a high-quality ground plane while meeting process required metal density rules can be challenging. To simplify the ground plane, a mesh of metal 2 and metal 3 was created, as shown in the inset of Figure 4.12. The metal 2 ground uses 6.5 μm x 6.5 μm squares connected together by 2 μm strips of metal. Metal 3 is created in a plus shape to cover all areas where metal 2 is not present. In the regions where

metal 2 and metal 3 overlap, they are connected with vias. This mesh completely covers the substrate and meets all density requirements. Furthermore, it can easily be placed throughout the entire circuit, creating an excellent ground plane with only a few discontinuities for connecting to transistors. Since the vertical distance between metal 2 and metal 3 is small in comparison to the dielectric height of the microstrip line, the mesh ground plane has little impact on the characteristic impedance of microstrip lines. Figure 4.12 compares the EM simulation of a 180 μm x 20 μm shorted stub using the mesh ground plane to the EM simulation of the shorted stub with a simplified ground plane of only metal 3. Since there is little difference between the stub inductance and Q of the different types of ground planes, the mesh ground plane can be simplified to just metal 3 in EM simulations to reduce simulation time while maintaining accuracy. The 90 pH short stubs used in the reverse-saturated SiGe HBT SPDT achieve a simulated Q-factor of 28 at 100 GHz (not shown).

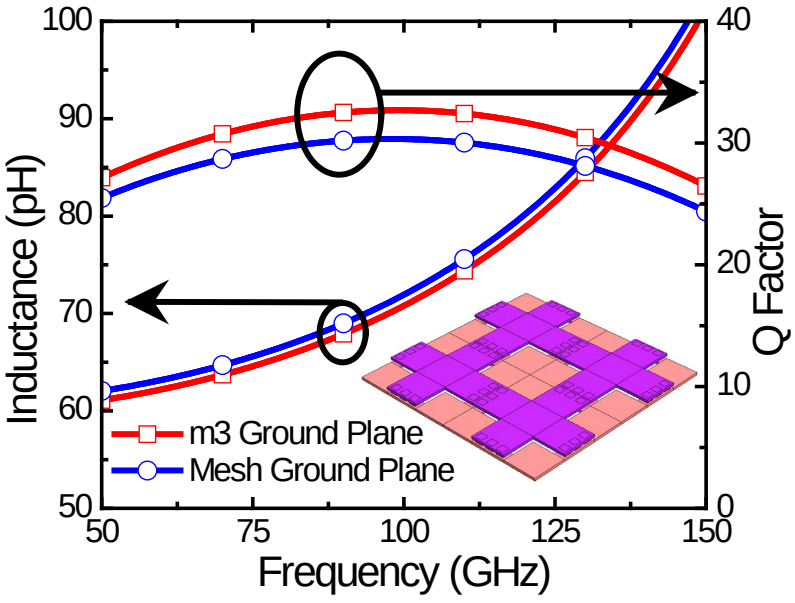

Figure 4.12: Comparison of the inductance and quality factor of a 180 μm x 20 μm shorted stub using a solid metal 3 (m3) ground plane and the metal 3-metal 2 mesh ground plane.

4.3 Forward- and Reverse-Saturated SPDT Results

The quarter-wave shunt SPDT switches were designed using the described procedure, with shunt devices in both the forward- and reverse-saturated configurations. Referring to Figure 4.6, both designs used shunt devices with two SiGe HBTs of 9 μm emitter length for comparison. The inductive stub was designed to be 65 pH for the forward-saturated SPDT and 90 pH for reverse-saturated SPDT to properly resonate with the device capacitance. At the base node of the SiGe HBT, the dc bias line must present a high impedance to prevent RF leakage to ground. However, the saturated SiGe HBTs can draw a substantial amount of current in the on-state. In order to provide this current and a high RF impedance, the base of the SiGe HBT is biased with a quarter-wave transmission line. The RF loss of these quarter-wave lines is not critical to the overall switch performance, and the bias lines can be created with thin, high-impedance lines which are tightly meandered to reduce size.

In order to facilitate simple two-port measurements, one of the Switch Ports was terminated on-die with a tantalum nitride (TaN) metal resistor available within the BEOL. Due to the symmetry of the RF circuitry, the insertion loss and isolation should be the same for both Switch Ports. A TaN resistor was used instead of a substrate resistor to minimize the parasitic reactance of the on-die 50 Ω termination. The additional 20 Ω resistors in the bias networks of V_{sw} and nV_{sw} have an impact on the transient response, which is discussed in the next section. The die photograph of the reverse-saturated SiGe HBT quarter-wave shunt SPDT is shown in Figure 4.13.

A value of 1.1 V was used for V_{sw} in order to limit the switch power dissipation (Pdiss) to be less than 6 mW. Separate open and short test structures were used to de-embed the loss of the pads and contact resistance up to the reference plane, as shown in Figure 4.13. Due to the small size of the RF pads used in layout, de-embedding only reduced the total insertion loss by 0.30 dB at 94 GHz.

The measured and simulated insertion loss and isolation of the forward- and

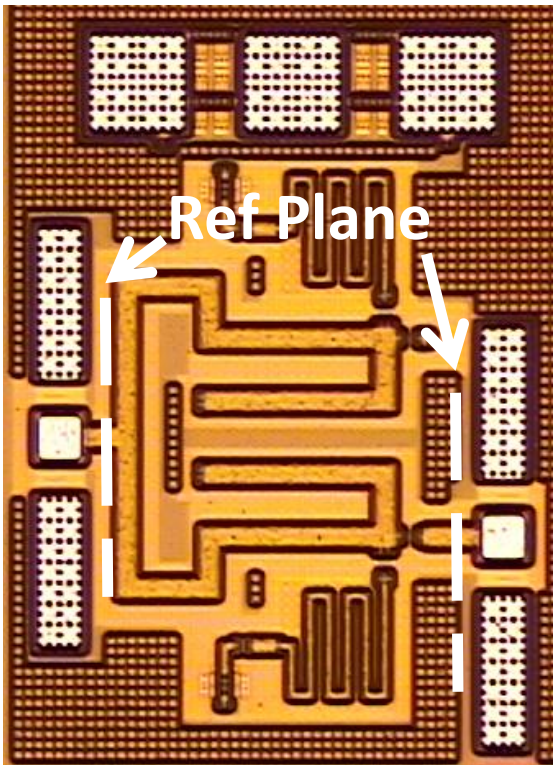

Figure 4.13: Die photograph of the reverse-saturated SiGe HBT SPDT switch. The switch is 680 μm x 480 μm with pads and 580 μm x 380 μm without pads © 2014 IEEE [7].

reverse-saturated SiGe HBT SPDTs are shown in Figure 4.14. At 94 GHz, the forward-saturated switch achieves an insertion loss of 1.30 dB, with the reverse-saturated design reducing the loss to 1.05 dB. The measured reverse-saturated SPDT is slightly degraded compared to simulation, but the forward-saturated measurements are better than simulated. The difference between simulations and measurement are reasonable considering that the deeply-saturated mode of operation is typically not considered during compact model development.

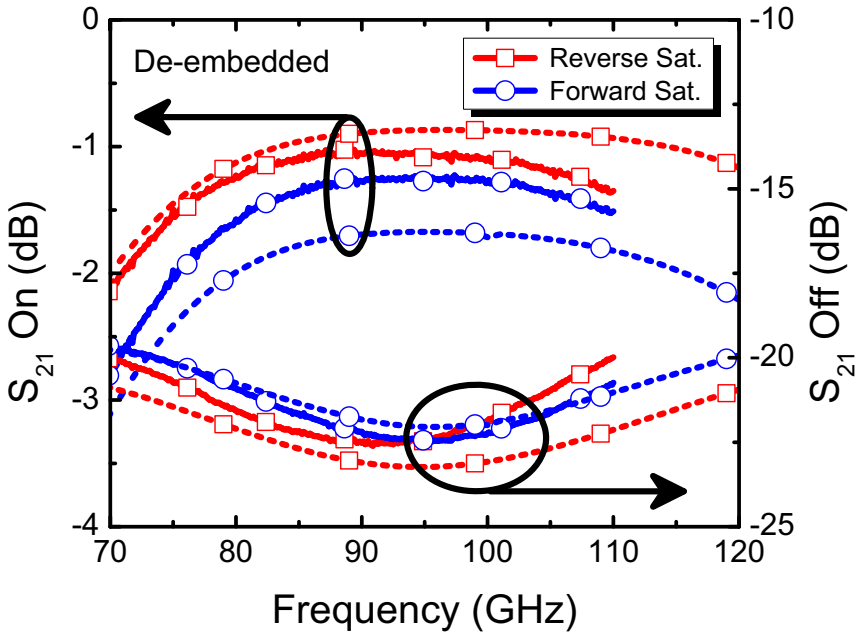

Figure 4.14: Measured (solid) and simulated (dashed) insertion loss and isolation of the forward- and reverse-saturated SiGe HBT quarter-wave shunt SPDTs © 2014 IEEE [7].

The improvement in switch loss in the reverse-saturated SPDT is less than initially would be expected from the results in Figure 4.9 because at very high off resistances, the impedance presented by the parallel LC network and the impedance presented by the opposite side of the switch also contribute considerably to the switch loss. With higher Q passive elements the difference in insertion loss between the forward- and reverse-saturated SPDTs would be larger. The results shown in Figure 4.14

demonstrate further improvement in comparison to initial W-band SiGe HBT SPDT designs that were developed earlier in a H4 process using a similar optimization procedure [6]. The H4 technology features a 180 nm SiGe BiCMOS process with a selectively shrunk 90 nm emitter. The insertion loss and isolation of the H4 forward- and reverse-saturated SiGe HBT SPDTs are repeated here and shown in Figure 4.15. In comparison to the H4 process, the full 90 nm IBM 9HP process further reduces the parasitic capacitances and results in a higher R_{eq_off}. This improvement reduces the overall insertion loss of the switch.

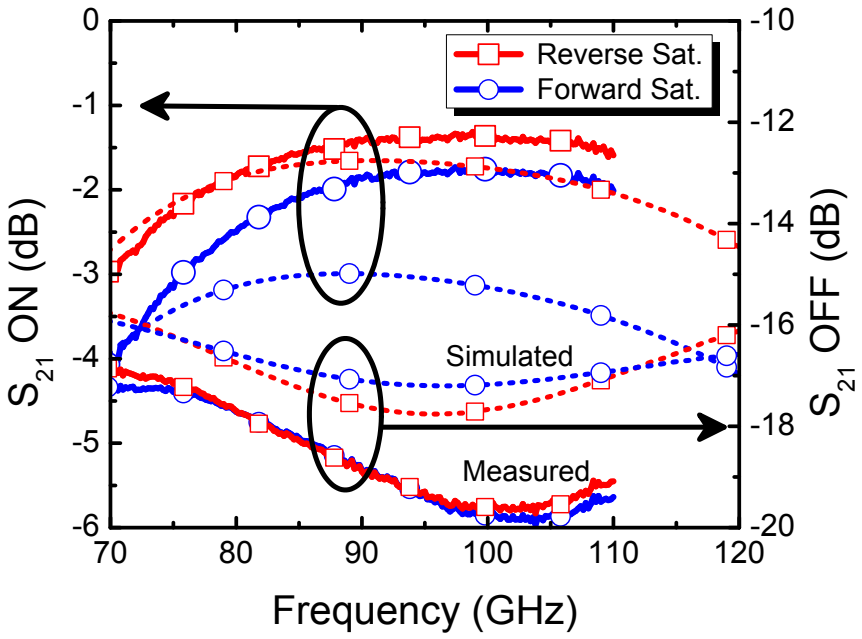

Figure 4.15: Measured (solid) and simulated (dashed) insertion loss and isolation for the forward- and reverse-saturated SiGe HBT SPDTs fabricated on Tower Jazz SBC18-H4 © 2014 IEEE [6].

The bandwidth of the quarter-wave shunt switches is driven by the input and output return losses of the switch. Figure 4.16 shows both switches to have greater than 10 dB input and output return losses from 78 to 110+ GHz and have a simulated fractional bandwidth of more than 50%. The frequency dependence of the input and output match is due to the resonance of the equivalent shunt capacitance and

the inductive stub. It is well known that for parallel LC resonant filters, a lower capacitance and higher inductance creates a wider filter bandwidth [95]. Thus, while increasing the size of the shunt device improves the isolation, it will also increase the off-state capacitance and reduce the switch bandwidth [47]. The bandwidth can be incorporated into the device size optimization procedure shown in Figure 4.10, but in most cases the switch bandwidth is more than sufficient and will not limit the overall transceiver performance.

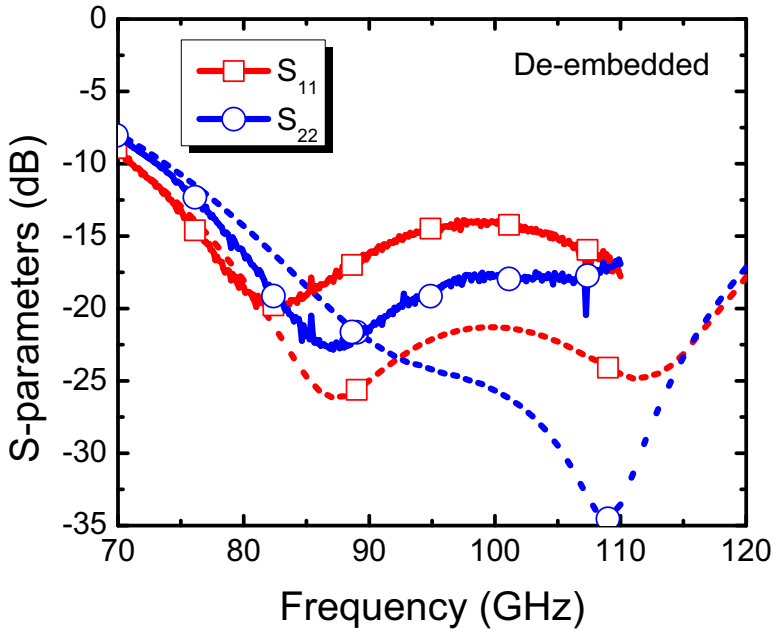

Figure 4.16: Measured (solid) and simulated (dashed) return losses of the reverse-saturated quarter-wave shunt SiGe HBT SPDT © 2014 [7].

Finally, since the matching networks are designed based on the off-state impedance of the transistor, a bias point can be selected at the end of the design process to balance performance and power dissipation. The measured insertion loss and isolation of the forward- and reverse-saturated quarter-wave shunt SPDTs are shown in Figure 4.17 as a function of the bias voltage and current. Even when the switch operates at a reduced bias point to consume less than 1 mW of power, the reverse-saturated SPDT still achieves 1.4 dB insertion loss and greater than 20 dB of isolation at 94

GHz before de-embedding pad losses.

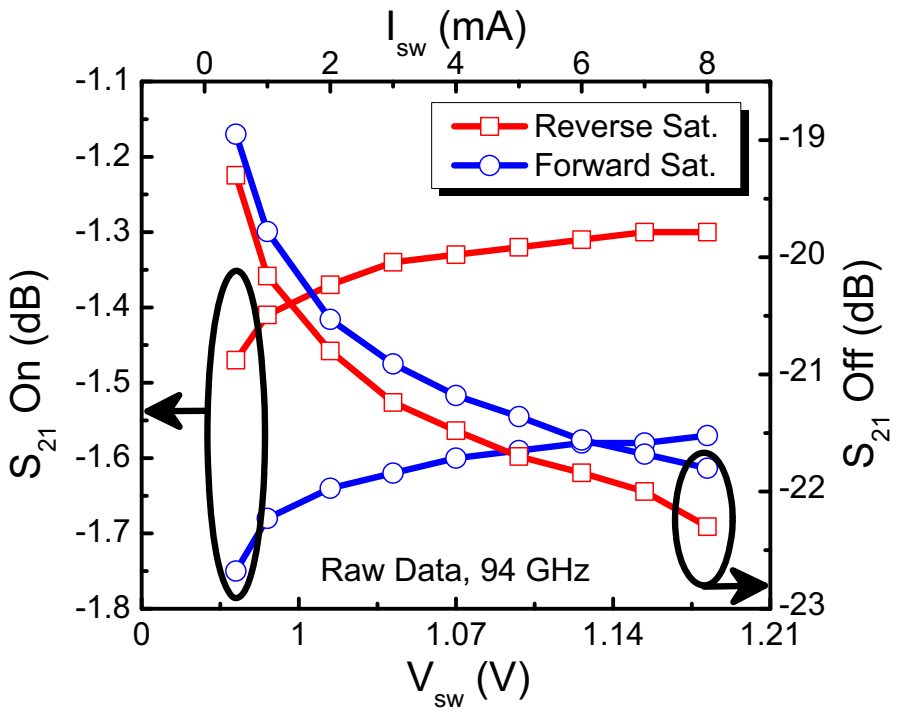

Figure 4.17: Insertion loss and isolation of the forward- and reverse-saturated SiGe HBT quarter-wave shunt SPDTs plotted over bias voltage and current before de-embedding, at 94 GHz © 2014 IEEE [7].

4.4 Switching Speed

The ability to switch rapidly is especially important when the switch is used to change between transmit and receive modes of operation. For mid- to short-range radar applications, obtaining a switching speed of less than a couple nanoseconds is important [96] and correlates to detecting objects beyond a minimum range of 1 meter.

When placed in a deeply-saturated bias configuration, a substantial amount of minority carriers build up on the base node of the SiGe HBT due to the forward-basing of both junctions. This excess charge in the base can slow the transistor down, and as a result, most RF circuits avoid saturation. Specifically for switches, when the device is turned off, the minority carriers must discharge or recombine before

the SiGe HBT is completely turned off [97].

However, there is an important distinction between typical nFET switches and the SiGe HBT quarter-wave shunt switches presented in this work. In the nFET schematic in Figure 4.1, the gate is biased with a large resistor. As a result, any charge that builds up on the gate has a large time constant for discharging to ground. It has been shown that reducing the size of this resistor can decrease the switching time, but this also reduces the isolation between the gate and ground and degrades the insertion loss of the switch [92]. In a SiGe HBT switch, the removal of the minority carriers from the base node is limited by the reverse current from the base through the bias network. In the SiGe HBT switch in Figure 4.6, the quarter-wave bias line presents a large impedance at W-band, but a low impedance at lower frequencies. As a result, the reverse current can be quite large and is only restricted by the 20 Ω limiting resistor placed after C_{shunt} (Figure 4.6). Essentially, the quarter-wave bias line allows the isolation from the base to ground and the switching speed to be decoupled into independent problems.

Unfortunately, the switching speed of W-band SPDTs is difficult to measure due to frequency limitations of oscilloscopes. Figure 4.18 shows the transient simulation of the reverse-saturated SiGe HBT quarter-wave shunt SPDT with changes in the switch state at 2.5 and 7.5 ns. Figure 4.18 indicates that the turn-on and turn-off times of the switch are both less than 200 ps. This is similar to the simulated switching speed of millimeter-wave nFET switches, which have been reported on the order of 300 ps [92]. While there is some concern that the deeply saturated mode of operation has not been considered in compact model development and could impact the transient simulations, it is anticipated the low impedance presented by the quarter-wave bias line will allow the minority carriers in the base to discharge quickly. Most likely the switching speed will be limited by the driver circuitry and not the switch core itself. Thus, using a quarter-wave transmission line to bias the base of the SiGe HBT is an

effective method to address the minority charge that builds up on the base node of the deeply-saturated SiGe HBT.

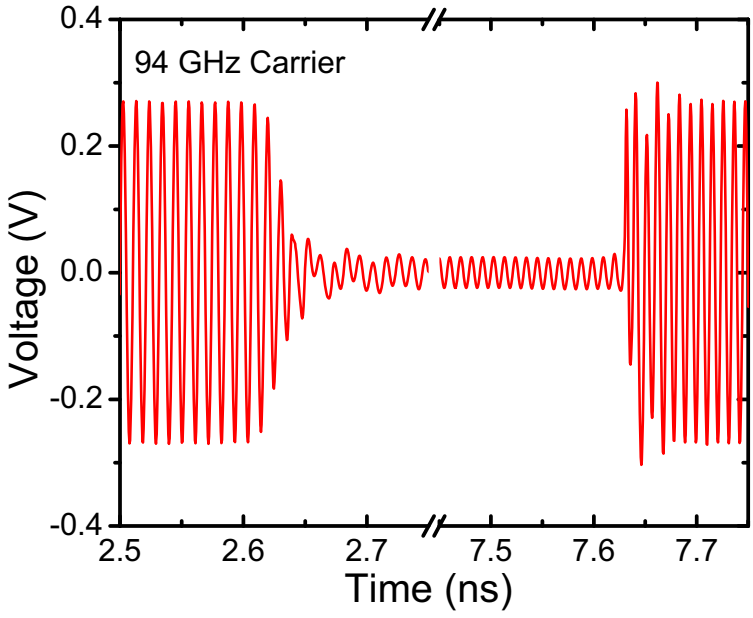

Figure 4.18: Simulated transient response of the reverse-saturated SiGe HBT quarter-wave shunt SPDT © 2014 IEEE [7].

4.5 Power Handling

In transceiver applications, the RF switch must be able to handle the high output power generated by the PA. The main limitation on the power handling capability of the quarter-wave shunt switch occurs at the Switch Port, with a large voltage swing across the off-state SiGe HBT, as pictured in Figure 4.19. Due to the collector-base and base-emitter capacitances, the voltage at the Switch Port capacitively divides to the base terminal. When the voltage at the base becomes large enough, the base-collector and base-emitter diodes begin to turn-on and provide a leakage path for the RF power.

As a result, the power handling of a quarter-wave shunt switch is heavily dependent on the turn-on voltage of the transistor. Similarly, for nFET-based quarter-wave shunt

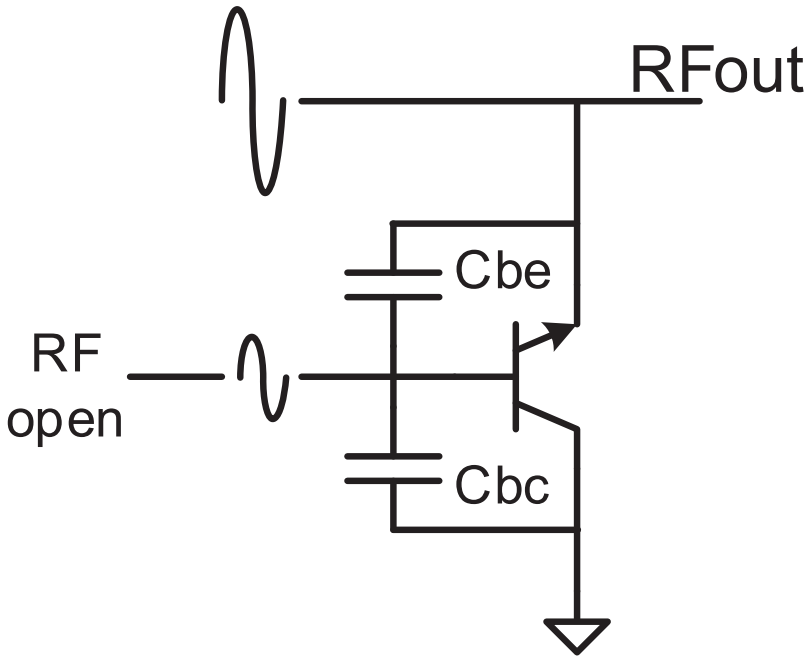

Figure 4.19: Schematic showing how capacitive coupling induces an RF voltage on the base of the off-state transistor © 2014 IEEE [7].

switches, the capacitive voltage division due to C_{gd} and C_{gs} induces a voltage on the gate. Thus, SiGe-based shunt switches have significantly improved power handling capabilities in comparison to nFETs, where the threshold voltage is much smaller [98]. Table 4.2 shows the calculated minimum input-referred 1-dB compression point ($P1dB_{min}$) for various SiGe HBT and nFET technologies when the Switch Port is terminated with a 50 Ω load. This value indicates the RF power level at which the base or gate node of the off-state device reaches the turn-on or threshold voltage (V_{th}) according to Equation (4.15).

$$P1dB_{min} = \left(\frac{2V_{th}}{\sqrt{2}}\right)^2 * \frac{1}{50} = \frac{(V_{th})^2}{25} \tag{4.15}$$

For SiGe HBTs, this equation assumes that $C_{be} \approx C_{bc}$ and thus the $P1dB_{min}$ is approximately the same for forward- and reverse-saturated modes. Since the off-state

Table 4.2: Shunt Switch Power Handling © 2014 IEEE [7]

Technology	180 nm nFET	90 nm nFET	65 nm nFET	90 nm SiGe
$V_{th}/V_{turn-on}$ (V)	0.43	0.36	0.24	0.72
$P1dB_{min}$(dBm)	8.7	7.1	3.6	13.2

device must be turned-on for a significant portion of the RF swing before contributing 1 dB of loss, the actual P1dB is typically several dB higher than the $P1dB_{min}$ value. However, Table II shows an important trend that the relatively large turn-on voltage of SiGe HBTs enable significantly higher power handling capabilities than scaled nFET switches. In order to achieve high power handling with scaled nFET switches, additional techniques such as using stacked nFETs in an SOI process will need to be investigated for millimeter-wave frequencies.

Initial power measurements were made using the setup shown in Figure 4.20. A low frequency signal generator feeds into an Oleson Microwave Labs (OML) 6x multiplier W-band source module. The W-band signal connects to a Millitech voltage-controlled attenuator (VCA) and then Millitech MCA-12-130133 PA. The PA features a P1dB above 22 dBm and includes a -20 dB coupled port to monitor the output power. The input and output power levels were calibrated to the probe tips. Since the difference in power from the input probe tip to the coupled port of the PA is fixed, both the input and output power levels can be measured simultaneously. This setup provides a DUT input power range from -0.4 to 18.7 dBm.

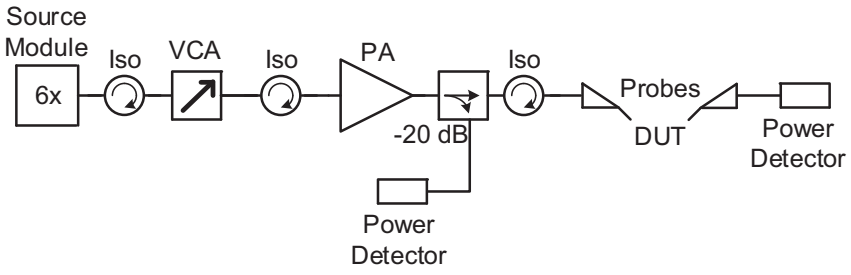

Figure 4.20: Power measurement setup at 88 GHz © 2014 IEEE [7].

For the power handling capabilities of a switch, it is important to distinguish

between the P1dB when RF power is injected at the Common Port and when RF power is injected at the Switch Port. P1dB is typically specified by injecting power at the Common port, but this can be deceptive. In transmit-receive switches, the antenna is connected at the Common Port and the Switch Ports are connected to the PA and LNA. In this case, the high RF power will be injected at the Switch Port connected to the PA.

Since the non-linearity of the switch arises from the off-state transistor at the Switch Port, injecting power at the Switch Port directly applies more RF power to the non-linear device. As a result, the P1dB when power is injected at the Switch Port is lower than the P1dB when power is injected at the Common Port. Figure 4.21 compares the measured P1dB when power is injected at the Common Port and Switch Port for the reverse-saturated SiGe HBT quarter-wave shunt SPDT at 88 GHz.

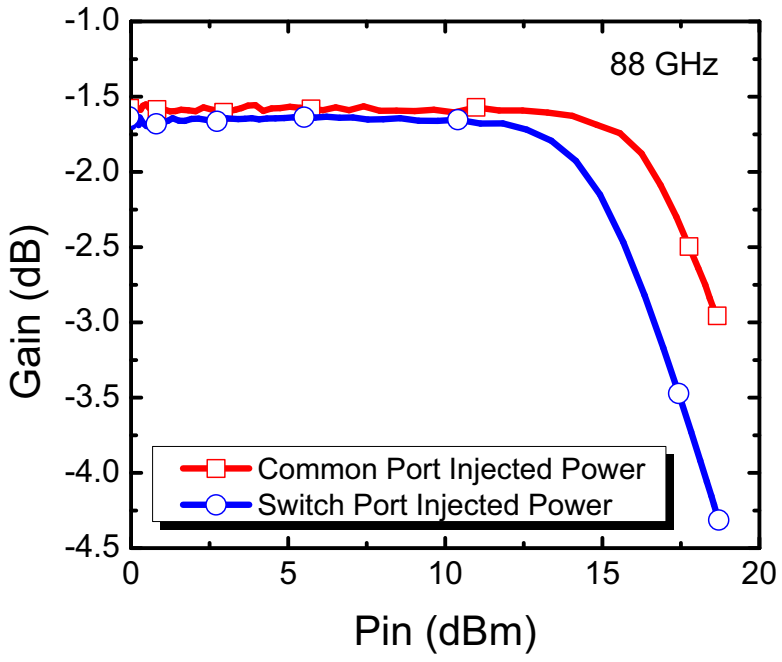

Figure 4.21: Comparison of the measured P1dB when power is injected at the Common Port and Switch Port for the reverse-saturated SiGe HBT quarter-wave shunt SPDT © 2014 IEEE [7].

Since the non-linearity arises when a portion of the RF swing adds to the dc bias

to turn-on the shunt device, it is reasonable to expect that the P1dB will increase if a negative dc bias is applied to the off-state transistor. With a negative bias at the base, the device has a similar off-state impedance, but it takes a larger RF swing for the base to reach the turn-on voltage of the SiGe HBT. To investigate this effect, the switch was measured at 94 GHz at different biases on a separate high power millimeter-wave setup. The measurement setup consisted of a Millitech 6x multiplier, Millitech mechanical step attenuator, a Quinstar 90-96 GHz power amplifier, Maury WR-10 tuners, a fixed 10 dB attenuator, a HP WR-10 power sensor, and WR-10 probes.

Figure 4.22 shows the power sweep of the reverse-saturated SiGe HBT quarter-wave shunt SPDT for different biases applied to the base of the off-state transistor. Once again, RF power was injected at the Switch Port to apply more RF power to the non-linear device. Figure 4.22 indicates that P1dB improves by 5 dB with a bias of -0.8 V, up to 22 dBm. The negative bias is limited not by the SiGe HBT, but by the n-tiedown diodes used to protect the dielectric layer of the metal-insulator-metal (MIM) capacitors during fabrication. The n-tiedowns could be replaced by large resistors to enable larger negative bias voltages. While negative voltage supplies are difficult to implement on-die in many systems, the improvement in power handling capabilities is significant. In applications requiring high output power, negative charge pump circuits could be designed to provide the needed negative voltages on-die [99].

4.6 RF Stress

In order to establish saturated SiGe HBT switches as a viable alternative for millimeter-wave systems, it is important to demonstrate that this relatively unexplored mode of operation does not quickly accumulate damage and degrade performance. In [100], drastic degradation of a diode-tied SiGe HBT single-pole single-throw (SPST) switch was demonstrated at extremely high RF powers at X-band

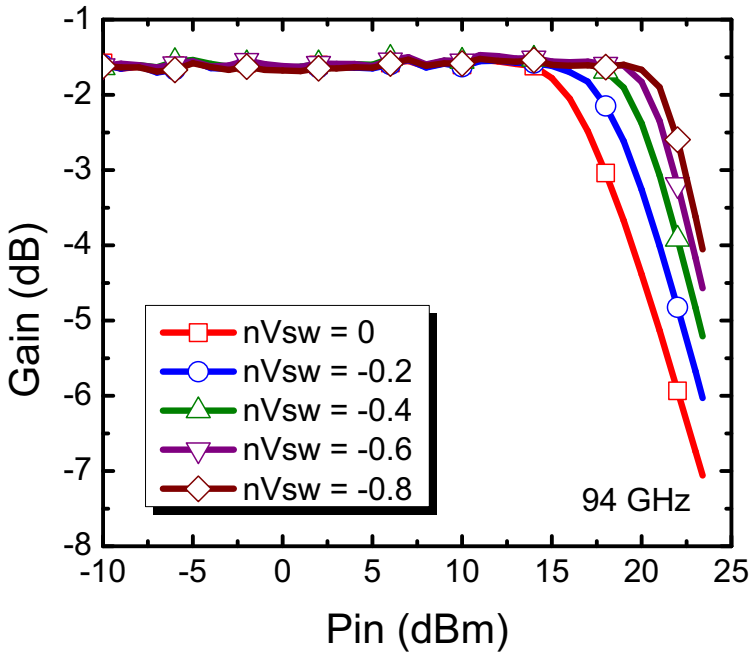

Figure 4.22: Power sweep of the reverse-saturated quarter-wave shunt SPDT using negative voltages at the base of the off-state transistor © 2014 IEEE [7].

frequencies. However, that work only analyzed an on-state series SiGe HBT.

Using the setup in Figure 4.20, a feedback loop between the input power detector and the VCA was used to provide a constant 17 dBm input power at the Switch Port of the reverse-saturated SiGe HBT quarter-wave shunt SPDT. Power was injected at the Switch Port for 24 hours in the on-state and 24 hours in the off-state. The performance of the switch over time is shown in Figure 4.23. There is little to no degradation in the switch performance over the cumulative 48 hour measurement period. Additional lifetime testing may investigate this mode of operation further, but the initial results are very promising.

4.7 Transformer-based SPDT

While the quarter-wave shunt switch topology achieves excellent performance at

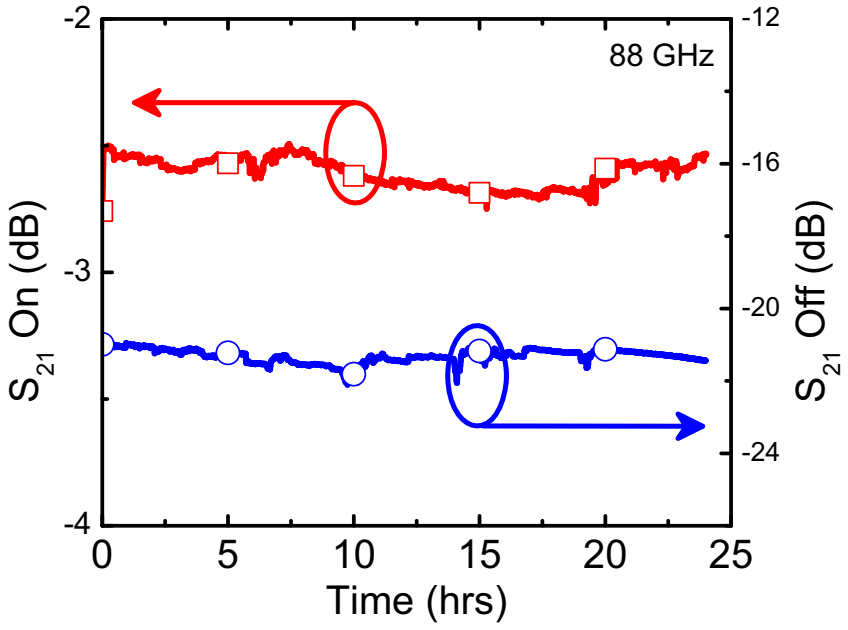

Figure 4.23: Insertion loss and isolation over time for the reverse-saturated SiGe HBT quarter-wave shunt SPDT © 2014 IEEE [7].

W-band, quarter-wave transmission lines are still quite large at 94 GHz. One technique to reduce the size of the switch is to replace the quarter-wave transmission lines with a transformer [9, 91], as shown in Figure 4.24. The transformer switch is only 140 μm x 140 μm without pads, as shown in Figure 4.25. The small size of the switch enables it to be used in applications where die constraints do not permit the quarter-wave shunt switch topology. For example, a transformer switch could be used in a direct conversion architecture to enable both on- and off-chip local oscillator (LO) generation. In this case, two transformer switches would be required since the LO port of the mixer is normally differential. The switches would increase the ability to characterize the performance of the transceiver without separate breakout circuits, while also reducing risk of failure. The transformer switch could also be placed in other locations throughout the transceiver to provide additional functionality, while maintaining nearly the same overall footprint.

In the schematic shown in Figure 4.24, the on-state device provides an approximate

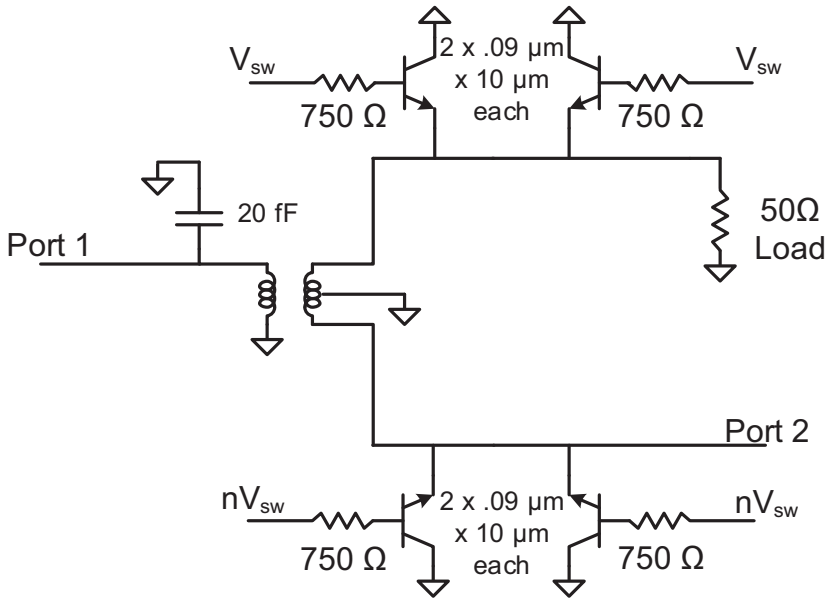

Figure 4.24: The final schematic of the reverse-saturated SiGe HBT transformer SPDT © 2014 IEEE [7].

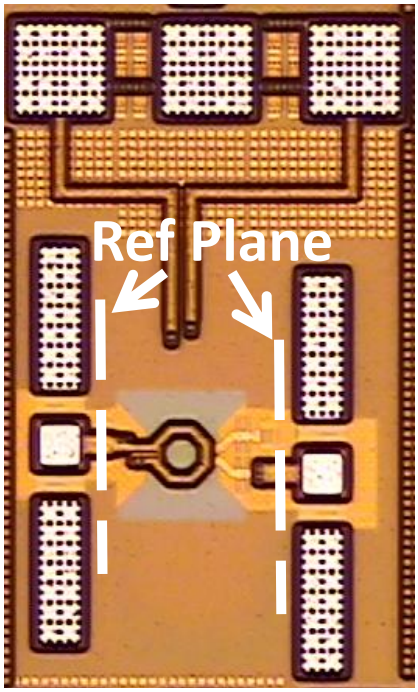

Figure 4.25: Die photograph of the reverse-saturated SiGe HBT transformer SPDT. The switch size is 640 μm x 320 μm with pads and only 140 μm x 140 μm without pads © 2014 IEEE [7].

short circuit to one transformer output, forcing most the RF energy to flow to the other output of the transformer. The device size and transformer are co-designed so the equivalent off-state shunt capacitance resonates with the transformer inductance. This eliminates the need for the shunt stubs and reduces the size of the switch.

To reduce the size of the switch further, the quarter-wave dc bias line connected to the base of the SiGe HBT can be eliminated. Figure 4.17 shows that the bias point of the SiGe HBT can be reduced to a lower current while still achieving excellent insertion loss and isolation. The low current operation allows the base to be biased with a large resistor rather than a quarter-wave transmission line. Thus, in this design the on-state device operates at a reduced bias point, which compromises isolation, but enables a smaller foot print. To address the reduction of isolation and to enable a resonance between the device capacitance and transformer inductance at W-band, the shunt device size was increased to include four 10 μm emitter length reverse-saturated SiGe HBTs.

The measured and simulated insertion loss and isolation are shown in Figure 4.26. The switch achieves better than 2.05 dB insertion loss and 23 dB isolation at 94 GHz, with a minimum insertion loss of 1.4 dB achieved at 75 GHz. Figure 4.27 shows the input and output return losses are greater than 10 dB from 65-110+ GHz. There is a noticeable shift to lower frequencies in the measured S-parameters. This shift may be due to the SiGe HBT placement in layout. In order to save space, the deep trench of adjacent SiGe HBTs was shared. The complete impact of this layout configuration on device performance is still under investigation.

4.8 Summary

Silicon-based millimeter-wave systems have great potential to create low-cost, high-volume products that have previously been impractical due to the high cost and low-integration associated with III-V technologies. In particular, SiGe-based systems

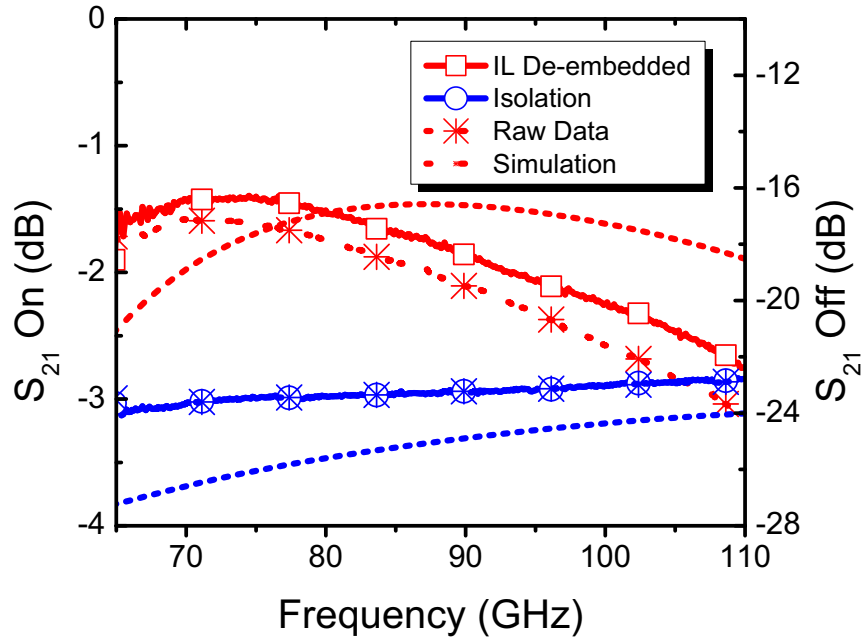

Figure 4.26: Measured and simulated insertion loss and isolation of the reverse-saturation SiGe HBT transformer SPDT © 2014 IEEE [7].

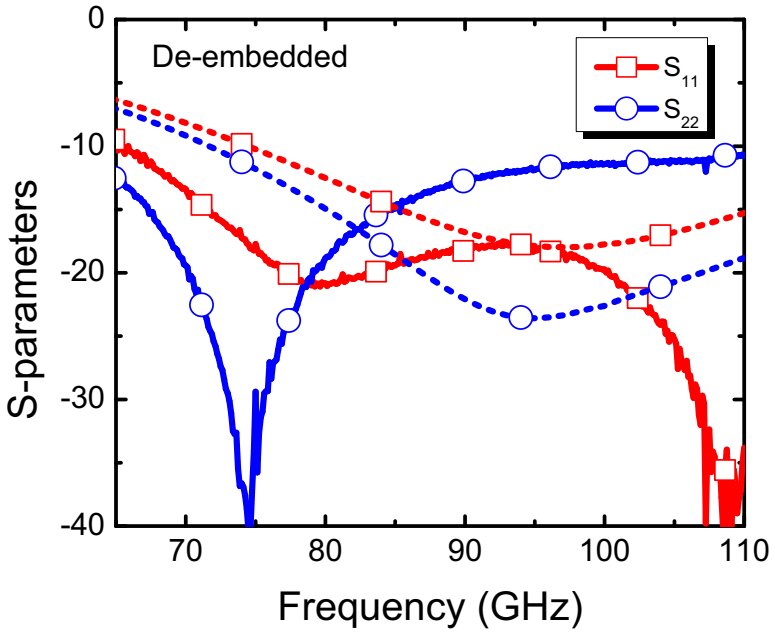

Figure 4.27: Measured (solid) and simulated (dashed) return losses of the reverse-saturated SiGe HBT transformer SPDT © 2014 IEEE [7].

have generated great interest due to the ability to achieve high performance LNAs and PAs at high frequencies [101]. However, in most current BiCMOS millimeter-wave systems, the front-end switch utilizes nFETs, with only a few exceptions exploring the use of SiGe HBTs in [6, 45, 48].

This work demonstrates that there are significant benefits to using SiGe HBTs in the front-end switch. The novel reverse-saturated topology leverages the higher off-state resistance at the emitter to improve switch performance. Figure 4.28 compares the insertion loss and isolation of 94 GHz SPDTs for different technologies. Table 4.3 summarizes the performance of the designed switches and compares this work to other state-of-the-art millimeter-wave SPDTs. The reverse-saturated SiGe HBT switches achieve nearly a 50% reduction in insertion loss in comparison to the best nFET SPDTs, and are competitive with III-V solutions. While the switching speed of saturated SiGe HBTs is of potential concern, initial transient simulations using current compact transistor models show promising results.

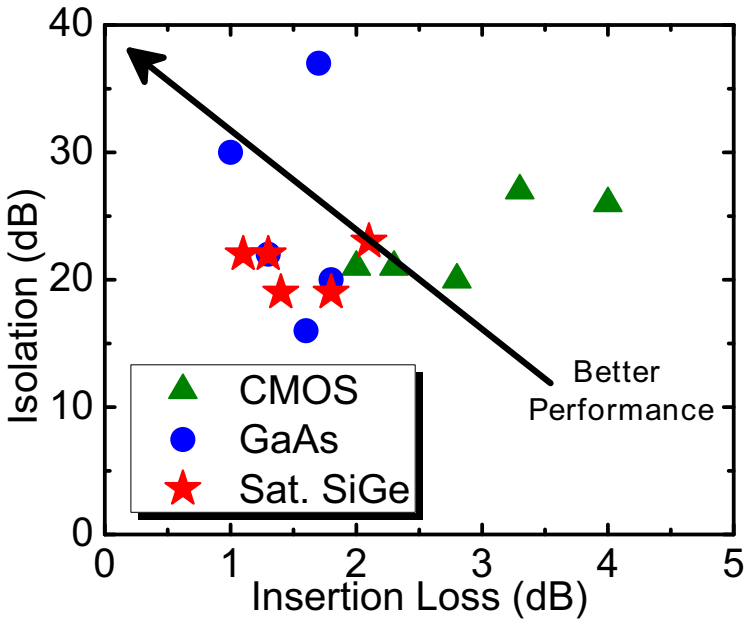

Figure 4.28: Comparison of the measured insertion loss and isolation of current state-of-the-art SPDTs at 94 GHz © 2014 IEEE [7].

The only performance disadvantage of SiGe switches in comparison to nFET switches is that SiGe-based switches consume power. However, it was demonstrated that the bias voltage can be reduced so the switch consumes less than 1 mW while still achieving excellent performance. In most applications, the system benefits of higher output power and reduced noise figure enabled by the low-loss SiGe switch more than outweigh the small power consumption it requires. Based on these results, saturated SiGe HBT switches may enable significant improvements to future silicon-based millimeter-wave systems.

Table 4.3: Comparison of State-of-the-art Millimeter-wave SPDTs © 2014 IEEE [7]

Ref.	Technology	Freq (GHz)	IL (dB)	Iso. (dB)	P1dB (dBm)	Area (mm2)	Pdiss (mW)
This	90 nm Rev. Sat. SiGe	73-110+	1.05	22	17	0.213	5.0
This	90 nm Sat. SiGe	78-110+	1.30	22	17	0.213	5.0
This	90 nm SiGe Transformer	65-110+	2.1	23	16	0.020	5.5
This	Selective 90 nm SiGe	77-110+	1.4	19	19	0.140	8
[46]	180 nm CMOS	75-110	2.8	>20	-	-	0.0
[47]	120 nm Trip-well CMOS	85-105	2.3	21	-	0.048	0.0
[43]	120 nm CMOS	80-110	2.0	21	-	-	0.0
[102]	90 nm CMOS	50-94	<3.3	>27	15	0.294	0.0
[103]	65 nm CMOS	60-94+	4.0	26	-	0.06	0.0
[93]	45 nm SOI CMOS	140-220	3.0	>20	8	0.248	0.0
[104]	130 nm SiGe PIN	50-78	2.0	25	-	0.11	28
[44]	50 nm InAlGaAs HEMT	77-120	1.8	20	>19	0.750	0.0
[51]	GaAs PIN Diode	94	1.3	22	-	0.938	-
[52]	GaAs PIN Diode	93-94	<1.0	>30	-	1.92	-
[105]	GaAs PIN Diode	75-110	<1.6	>16	-	1	-

CHAPTER 5

W-BAND BUILT-IN-SELF-TEST CIRCUITRY

5.1 Motivation

An important area of research currently in development for silicon transceivers is built-in-self-test (BIST) capabilities. The significance of BIST circuitry has grown as the complexity of RF systems has increased. There are now examples of SiGe millimeter-wave security imaging systems with over 6,000 RF channels [106]. In addition, wafer-scaled phased-array systems are currently in development, which may provide several thousand phased-array elements fabricated on a single silicon substrate in the near future [107].

These highly complex, numerous element systems are an area where CMOS and SiGe technology hold a distinct advantage over competing III-V technologies. The ability to integrate analog, digital, and RF circuitry all on a silicon substrate can provide a complete single chip transceiver. However, creating systems with a large number of elements comes at a high cost. The measurement and verification of each element in the array can be extremely costly and time consuming, especially in arrays of several thousand elements. The problem is exacerbated further at millimeter-wave frequencies where measurement systems are more expensive and time intensive. To address this growing limitation on low-cost transceiver development, BIST capabilities strive to provide some means to assess the functionality of the transceiver without the normal time-intensive millimeter-wave measurements.

While some research has investigated millimeter-wave built-in-self-test (BIST) capabilities, the previous approaches are sensitive to the antenna impedance, require several reference measurements, introduce significant losses or are not scalable to

large array designs. This work uses a novel type of loop-back testing to provide BIST capabilities.

Transceivers with loop-back testing use the signal at the output of the transmitter and feed it back into the receiver to verify the system functionality. There are several challenges associated with loop-back testing. First, the transmitter normally provides an output power much higher than the power level the receiver is designed to handle. Thus, the power of the transmitter must be significantly backed-off to the small-signal level or an attenuator must be placed between the transmitter and receiver. The first option means the loop-back test is not testing the transmitter with the conditions that it will actually operate in. A transmitter operating at low input power has significantly different matching, power consumption, and stability issues in comparison to large signal operation.

The second option to attenuate the signal between the transmitter and receiver is promising and the isolated path of the front-end switch can be used to attenuate the transmitter output signal [108]. However, most milimeter-wave switches are reflective and will present either the transmitter or the receiver with close to a short circuit. In this case, once again the loop-back test does not provide the same conditions as when the transceiver is in the normal transmit-receive (T/R) operation mode. Furthermore, presenting a near short circuit to the PA or LNA has the potential to create instabilities since most of the energy is reflected back into the amplifiers. Absorptive switches can be developed such that the transmitter and receiver are connected to 50 Ω impedances in all transceiver and loop-back states. However, this comes at a significant cost to both circuit size and performance. The circuit in this work presents 50 Ω impedances in all states of operation, while also minimizing the cost in terms of loss and size.

A conceptual diagram of the proposed system is shown in Figure 5.1. The switch in Figure 5.1 has both a normal T/R mode of operation and a BIST mode. In T/R

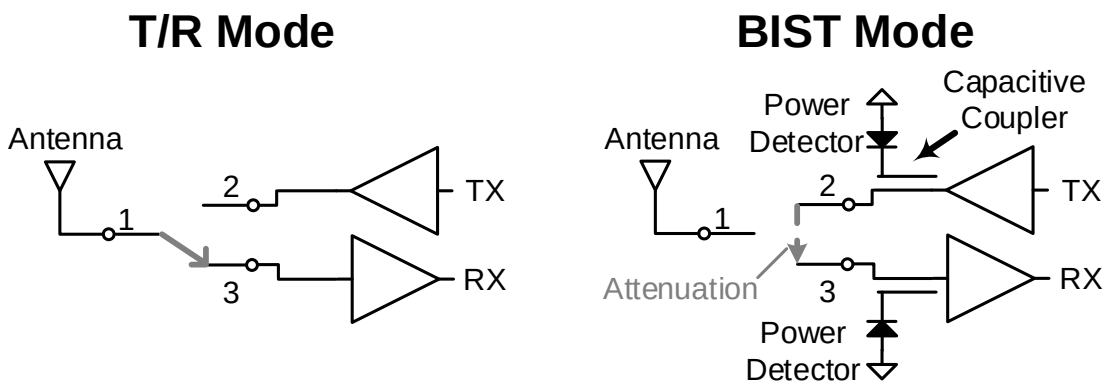

Figure 5.1: Conceptual diagram of a front-end switch being used for both transmit-receive operation and built-in-self-testing.

mode, the control voltages can easily switch between transmit and receive modes of operation. In the BIST mode, the attenuation path allows a portion of the transmit signal to be injected back into the receiver for on-die characterization. In addition, capacitive couplers are used to sense the RF power at the transmitter and receiver nodes. If the transceiver includes up and down conversion mixers, test signals can be injected and measured at the IF. Utilizing the power detectors, the transmitter and receiver gain can be determined on die based on the output voltage of the power detectors. In addition, if the receiver has the functionality to determine the in-phase and quadrature components of the signal, the change in gain and phase of VGAs and phase shifters can be characterized on die as well. The BIST mode of operation is designed with the transmitter and receiver connected to 50 Ω loads so that the matching is the same as the T/R mode of operation.

5.2 Front-End BIST Switch Design

The T/R and BIST modes of operation conceptually seem very different, but they can actually be designed using a lot of the same components and incorporated into the same front-end switch. The schematic of the front-end BIST switch is shown in Figure 5.2. Normal T/R operation is achieved by turning on Q4 and Q5 and turning

off Q1. The low impedances at Q4 and Q5 are transformed to open circuits at the RF outputs after the quarter-wave transmission lines. The off-state capacitance of Q1 resonates with the inudctive shunt stub and allows the antenna port to connect to the transmitter or to the receiver using Q3 and Q2. In BIST mode, Q1 is turned on and all other transistors are turned off. Q1 presents close to an open circuit at the RF output nodes due to the quarter-wave transmission lines. This isolates the transmitter and receiver from the antenna and provides a lossy attenuation path between the transmitter and receiver. This attenuation is important since the transmitter operates at a power level much higher than the P1dB of the receiver. With Q4 and Q5 turned off, the device capacitance resonates with the inductive shunt stubs. The quarterwave transmission lines in the Q4 and Q5 networks have a characteristic impedance of about 75 Ω to transform the 115 Ω load to 50 Ω at the Tx and Rx ports. In this state, the power level at the output of the transmitter and at the input of the receiver can be measured using the power detectors.

The front-end BIST switch leverages the excellent performance of the reverse-saturated SiGe HBT switches to provide BIST capabilities without significantly degrading insertion loss. The T/R control transistors, Q2 and Q3, are biased with quarterwave transmission lines to provide high current for good isolation and quick switching speeds. The BIST control transistors Q1, Q4, and Q5 are less critical to the switch insertion loss and isolation and are biased with 750 Ω resistors to reduce the circuit size. A 115 Ω termination is used in the BIST networks of Q4 and Q5. An impedance of larger than 50 Ω is chosen to limit the current flow across the resistor in the BIST mode. This is especially important for the transmitter where high power could heat the on-die termination and change its impedance.

The capacitive couplers used at the transmitter and receiver nodes are optimized for the expected power levels at the output of the PA and the input of the LNA. The capacitive couplers extract a small portion of the energy traveling along the

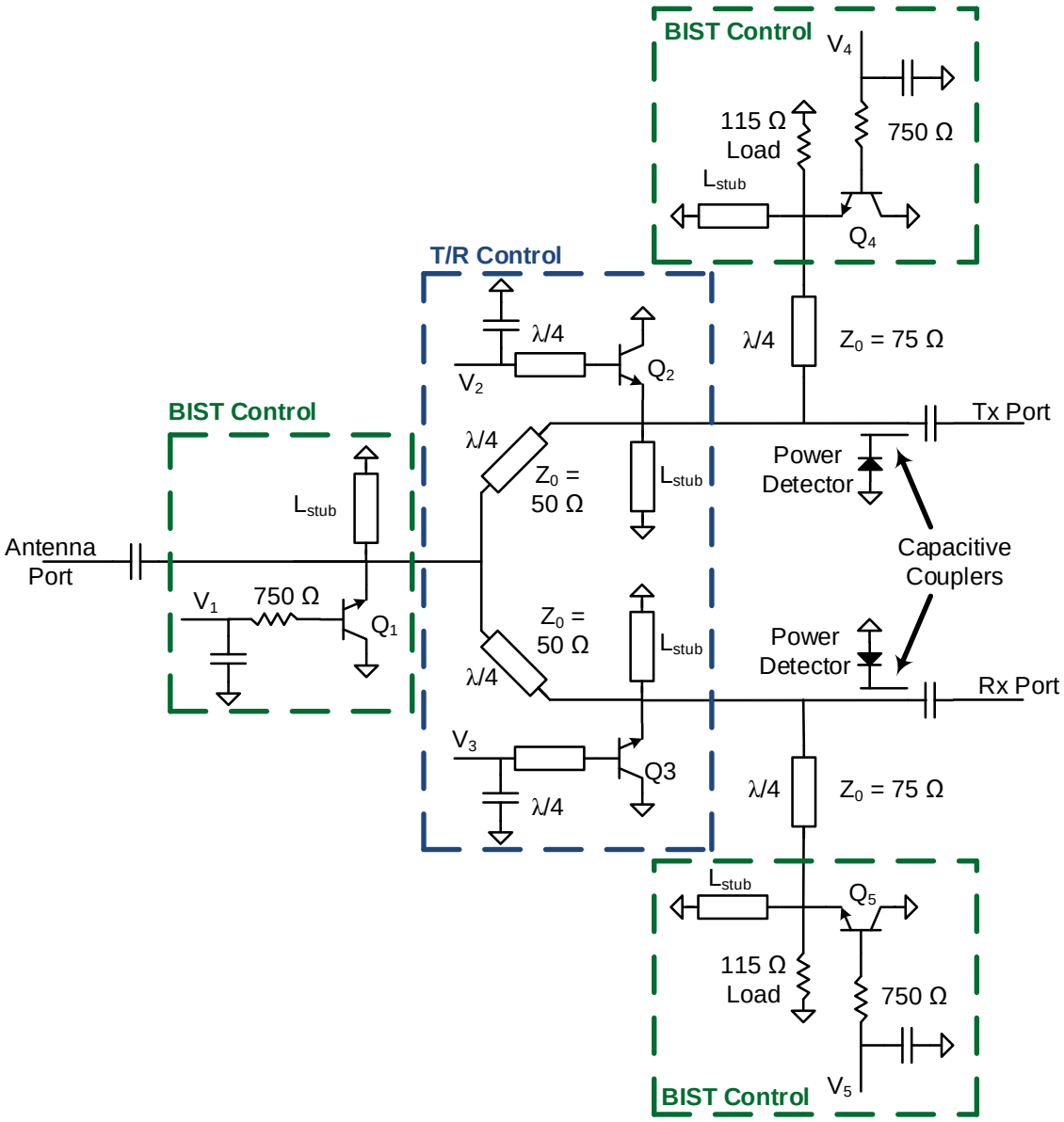

Figure 5.2: Schematic of the front-end BIST switch.

transmission lines. Figure 5.3 shows a 3D image of the transmitter and receiver couplers. The transmitter coupler is between metals 4 and 5 of the BEOL, with an overlapping area of 4 μm x 4 μm and a separation of 0.4 μm. Since the anticipated power at the receiver is much lower, the coupler at the receiver is designed with a higher coupling coefficient to ensure the signal reaching the power detecor is within the detectable range. The receiver coupler is between metals 3 and 4, with an overlapping area of 10 μm x 10 μm and a separation of 0.25 μm.

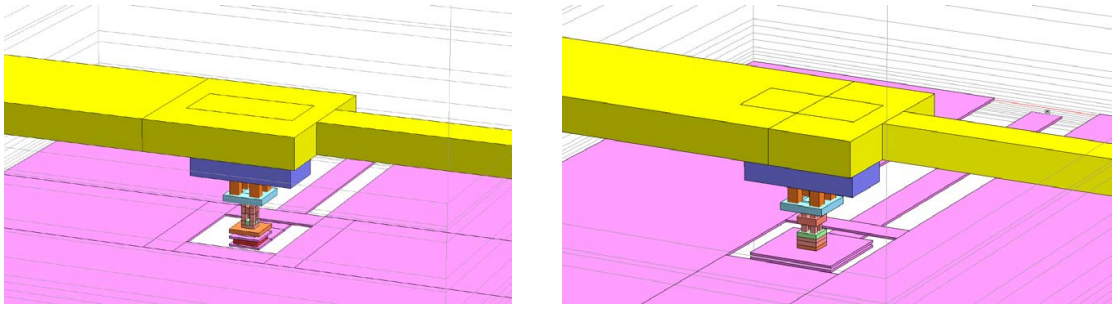

Figure 5.3: 3D image of the transmitter and receiver capacitive couplers.

The schematic of the power detector used in the front-end BIST switch is shown in Figure 5.4. There are several examples of using SiGe HBTs as a power detector [18, 109–113]. However, in most of these examples the main goal is high responsivity [18,111,113,114]. For the power detectors in this work, rather than designing for high responsivity, it is important to achieve a wide range of an accurate linear response. The power detectors are biased similar to a class B PA, right near the turn-on voltage of the transistor, so that it is very sensitive to small input powers.

The change in power detector output voltage from the DC bias point for the power detector in Figure 5.4 can be written as in Equation (5.1), where V_{be} is the DC base-emitter voltage, V_T is the thermal voltage, R_C is the collector resistance, I_S is the reverse-saturation current, and V_{RF} is the RF voltage swing at the base of the power detector. By using the Taylor Series expansion in Equation (5.2) and integrating over a single period in Equation (5.3), Equation (5.1) can be approximated as in Equation

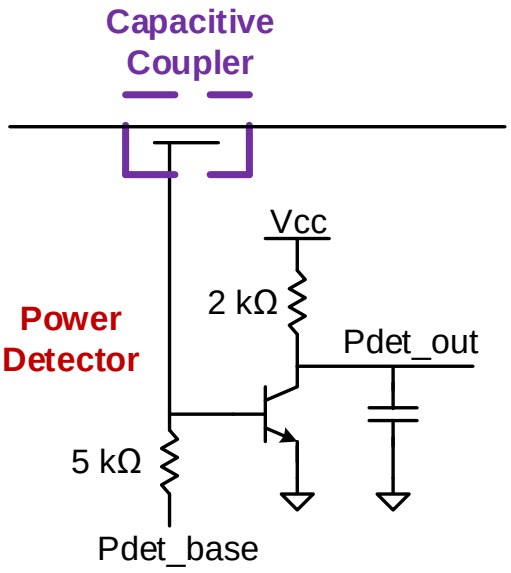

Figure 5.4: Schematic of the BIST power detector.

(5.4). The responsivity is defined as the change in output voltage due to the RF input power and can be calculated for the power detector topology as in Equation (5.5), where α is a constant relating the input power, P_{in}, to V_{RF}^2 based on the input impedance and mismatch [115].

$$\Delta\, V_{out} = R_C I_s e^{V_{be}/V_T}\left(e^{V_{RF}cos(2\pi t)/V_T} - 1\right) = R_C I_C\left(e^{V_{RF}cos(2\pi t)/V_T} - 1\right) \tag{5.1}$$

$$e^{V_{RF}cos(2\pi t)/V_T} \approx 1 + \frac{V_{RF}cos\,(2\pi ft)}{V_T} + \frac{V_{RF}^2 cos^2\,(2\pi ft)}{V_T^2} \tag{5.2}$$

$$f\int_0^{1/f} e^{V_{RF}cos(2\pi t)/V_T} dt \approx 1 + \frac{V_{RF}^2}{4V_T^2} \tag{5.3}$$

$$\Delta\, V_{out} \cong R_C I_{DC}\frac{V_{RF}^2}{4V_T^2} \tag{5.4}$$

$$\Re = \frac{\Delta V_{out}}{P_{in}} \approxeq R_C I_{DC} \frac{\alpha}{4V_T^2} \tag{5.5}$$

As shown in Equation (5.5), the responsivity is linearly related to the DC collector current and the collector resistor. However in this case, if the responsivity it too high, it will cause a large change in voltage at the output of the collector for small RF power levels. The collector current will increase, reducing the collector voltage and start to push the SiGe HBT into saturation, resulting in a lower responsivity. Thus in order to design a power detector intended for higher input powers, the responsivity must be intentionally reduced to prevent the compression of the responsivity. A collector resistor of 2 KΩ is selected and collector currents biases of 170 μA and 225 μA are used for the receiver and transmitter power detectors respectively.

While many power detectors use a notch filter at the collector of the SiGe HBT to reduce the RF feed through from the base to collector [112–114], the benefits of this additional passive network are small. Using a simple decoupling capacitor is sufficient to suppress RF feed through at 94 GHz and significantly reduces the footprint of the power detector.

In future work, a differential power detector would be preferred, in which one end of the differential power detector is grounded. This simplifies the processing of the power detector output voltage. In the single ended case, the power detector output voltage must be compared to the DC bias voltage to determine the RF power. However, turning off all RF power in a system is not always possible for BIST applications. It is important to note that using a differential power detector topology will not make the power detector insensitive to temperature changes, as claimed in [110]. The responsivity is inherently exponentially dependent on the thermal voltage as indicated in Equation (5.1). The responsivity is sensitive to temperature regardless of whether the topology is single ended or differential. Temperature compensation

must be handled in a different manner.

Figure 5.5 shows the die photograph of the front-end-BIST switch. The total area of the switch is 1100 μm x 700 μm. Each power detector is only 50 μm by 80 μm and does not substantially increase the size of the circuit. This indicates that similar power detectors could be placed at other locations in the transceiver to provide additional information on individual circuit block performances. In addition, without DC pads, the front-end BIST switch is only 700 μm wide and is easily small enough to allow for antenna elements to be spaced $\lambda/2$ apart at 94 GHz.

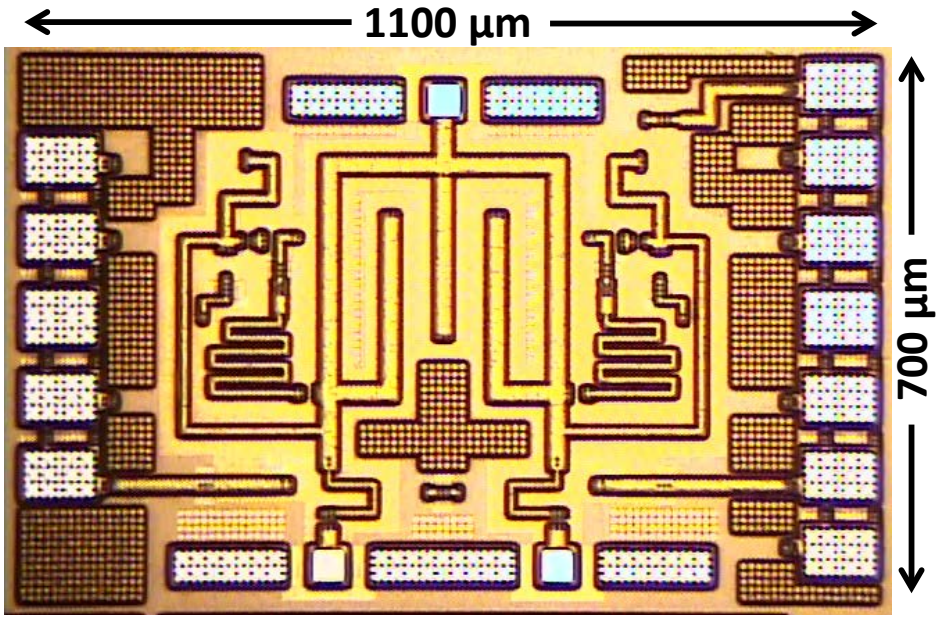

Figure 5.5: Die photograph of the front-end BIST switch. The switch is 1100 μm x 700 μm and only 700 μm x 700 μm without DC pads.

5.3 Measured S-parameters

The S-parameters were measured on an Anritsu 3738A Lightning system with millimeter-wave test heads. Figures 5.6 and 5.7 show the measured and simulated insertion loss and isolation of the BIST front-end switch from the antenna to transmitter and the antenna to the receiver ports respectively. The insertion loss is about 0.5 dB higher than simulation. However, this is expected considering the difference

between simulation and measurement was about 0.2 dB for the normal reverse saturated SPDT switch. This most likely indicates the compact model of the SiGe HBTs overestimates the off-state impedance of the transistor in the reverse-saturated configuration. Since the front-end BIST switch has more shunt off-state SiGe HBTs in the circuit, the difference between simulation and measurement is greater than for the SPDT switch.

Figure 5.6 shows the transmitter to antenna port path is able to achieve 2.15 dB insertion loss and 19.8 dB isolation at 94 GHz. The receiver to antenna port shows similar results with an insertion loss of 2.35 dB and an isolation of 19.5 dB at 94 GHz. Open and short test structures were used to deembed the pad capacitance and contact resistance. However, due to the small RF pads used in layout, deembedding reduced the insertion loss less than 0.2 dB. The loss in the receiver path is slightly higher than the transmitter path since the power detector on the receiver side requires a coupler with a high coupling ratio.

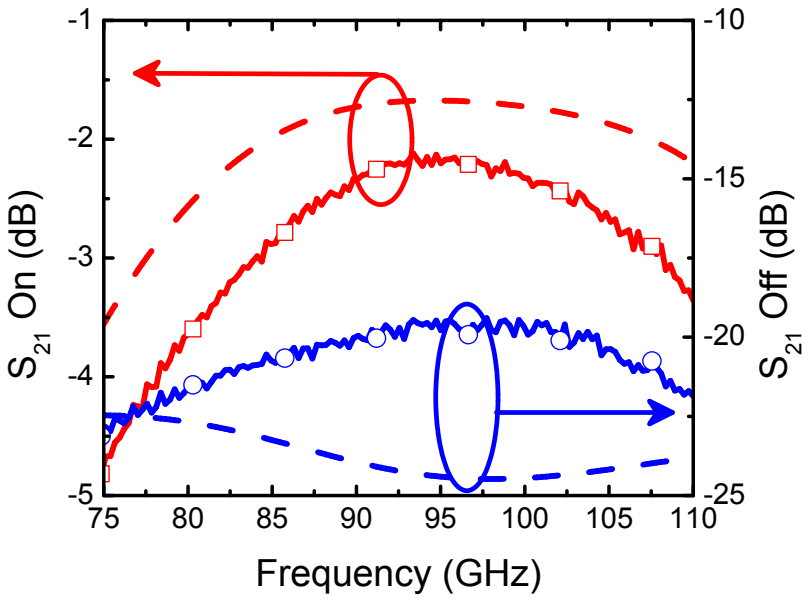

Figure 5.6: Measured (solid) and simulated (dashed) insertion loss and isolation of the BIST front-end switch from the antenna port to the transmitter.

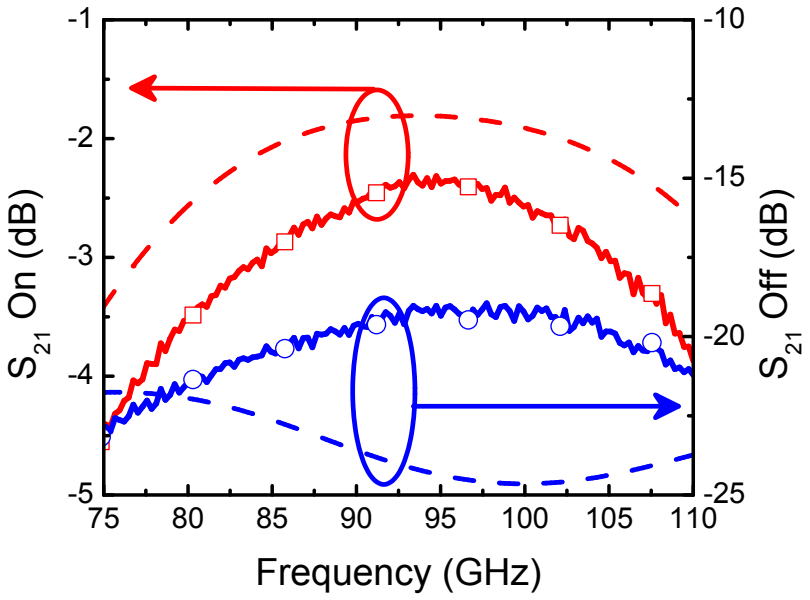

Figure 5.7: Measured (solid) and simulated (dashed) insertion loss and isolation of the BIST front-end switch from the antenna port to the receiver.

One goal of the front-end BIST topology was to achieve a similar impedance at the transmitter and receiver nodes in T/R and BIST mode. Figure 5.8 shows the impedance at the transmitter and receiver nodes in both normal T/R and BIST modes of operation. The stars symbols at 94 GHz indicate that very similar matching has been achieved for the two modes of operation. Thus the BIST mode captures the performance of the T/R mode very accurately.

5.4 Power Measurements

Extensive power measurements were completed to assess the capabilities of the front-end BIST switch concept. Test structures for the receiver and transmitter coupled power detectors were fabricated. These structures were first tested to analyze the chip-to-chip variability in the power detector response. Then using the responsivity measured on the test structures, the output power present on the receiver and transmitter nodes of the full front-end BIST switch was predicted based on the output

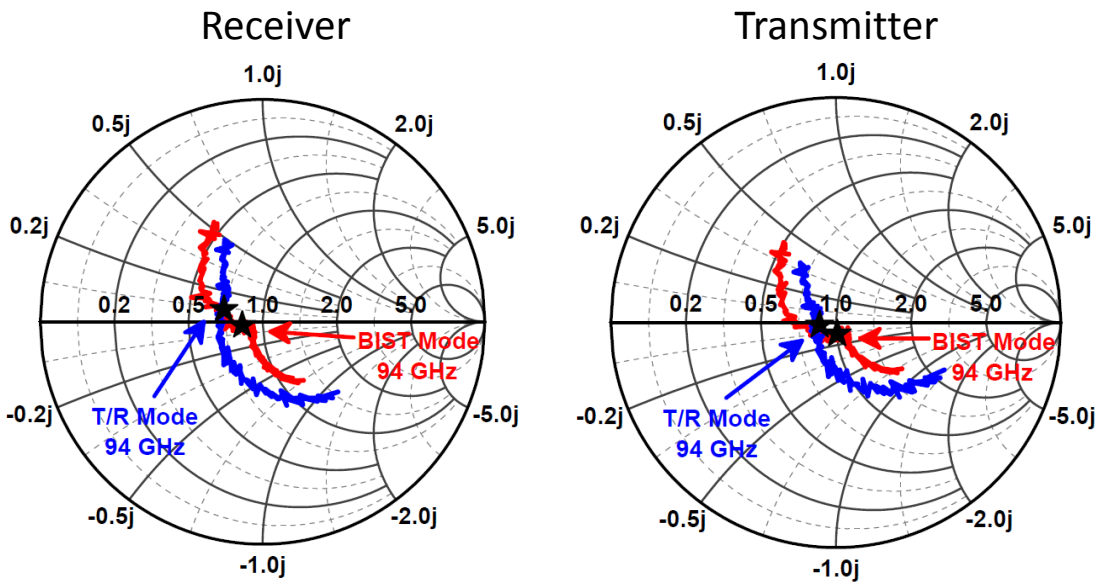

Figure 5.8: Comparison of the impedances seen at the transmitter and receiver nodes in the T/R mode and BIST mode. The stars indicate the impedance at 94 GHz.

voltage of the power detectors. The accuracy of this approach was analyzed by comparing the predicted output power to the actual power at the receiver and transmitter nodes determined by a two step power calibration. Achieving a low error between the predicted and actual power levels indicates that for a large system, the test structures could be used to determine the responsivity of the power detectors. Then, the power at the receiver and tramsmitter nodes of all the elements of a phased-array system could easily be predicted by the output voltage of the power detector. As a result, the measurement and verification time of a system would be significantly reduced.

Figure 5.9 shows the schematic of the transmitter power detector test structure. The test structure should resemble the front-end BIST switch as close as possible to accurately predict the power in the front-end BIST switch. As seen in Figure 5.9, the transmitter test structure repeats the transmit half of the front-end BIST switch, but removes the receiver and antenna path to reduce area. The connection of the transmitter test structure to the rest of the front-end BIST switch is left as an open.

In BIST mode, Q1 of Figure 5.2 is turned on creating close to a short. After the quarterwave transmission line this presents a very large impedance to the transmitter half of the circuit. Thus, leaving the connection as an open is a reasonable approximation of the impedance the front-end BIST switch presents to the transmitter half BIST mode. However, the difference between the open circuit of the test structure and the actual impedance the front-end BIST switch presents to the transmitter half of the circuit may cause a small error in estimating the responsivity of the power detectors.

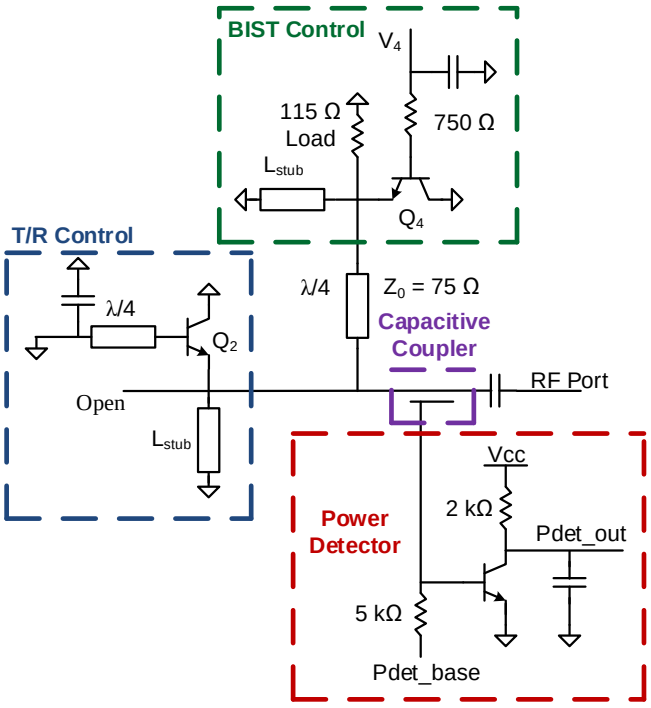

Figure 5.9: Schematic of the BIST transmitter power detector test structure.

Figure 5.10 shows a die photograph of the transmitter and receiver power detector test structures. The receiver power detector test structure uses the same layout at the transmitter power detector structure, but with a different coupler and power detector bias point. Each test structure is 600 μm x 600 μm.

5.4.1 Receiver Measurements

Figure 5.11 shows the W-band power measurement setup for the receiver power

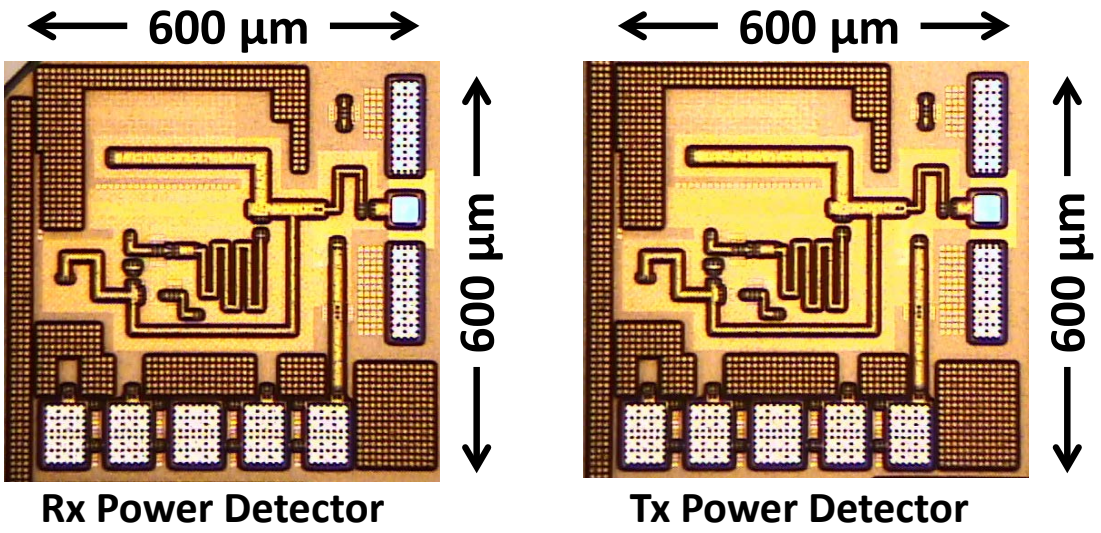

Figure 5.10: Die photograph of the receiver and transmitter power detector test structures.

detector. A low frequency signal generator feeds into an Oleson Microwave Labs (OML) 6x multiplier W-band source module. The W-band signal connects to a Millitech voltage controlled attenuator (VCA). A coupler and an Agilent W8486A W-band power detector are used to accurately determine the power at the waveguide level. For the receiver power setup, the power detector is placed at the thru port of the coupler since the power levels are low and the W8486A is limited to a -30 dBm to 20 dBm range. A W-band to 1 mm coax adapter and a 1 mm coax cable is used to connect to the 110 GHz GSG probe. Since there are only passive elements between the W8486A and the probe tip, this offset is independent of power level and can be accurately calibrated out of the measurement setup for each measurement frequency.

Figure 5.12 shows the steps required for the power calibration. In the first step, two power detectors are used at the thru and coupled port of the coupler. The bias of the VCA is swept the from 0-10 V to determine the difference in power levels between the thru and coupled ports over a 20 dB power range. The variation in the difference between the two power detectors is on the order of 0.1 dB and an average power offset value is assumed between the two coupler ports. As a result, the power at the coupled

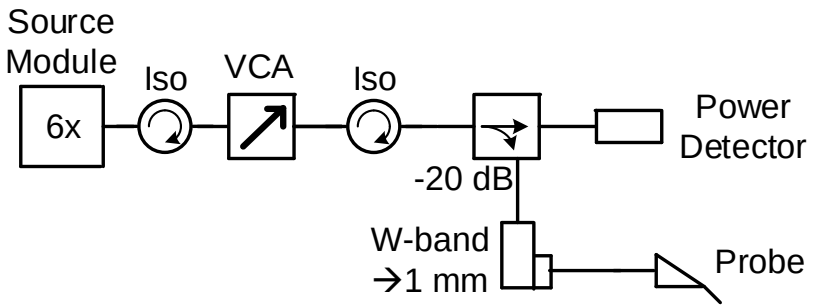

Figure 5.11: Block diagram of the setup used for the receiver power measurements.

port can be determined by the power measured at the thru port. This procedure is carried out at each frequency of interest. In the second step, two sets of W-band to 1 mm coax adapters, 1 mm coax cables, and 110 GHz probes are added in between the coupled port and the second power detector, as shown in Figure 5.12. Next, the power levels are measured while probed on a thru calibration structure. The additional loss measured in step two is the loss of the two additional adapters, cables, and probes. Due to the symmetry of the setup the loss of a single adapter, cable, and probe can be estimated by dividing this additional loss by two. The single-sided loss can be added to the difference in the coupled ports to determine the power at the probe tip as in Equation (5.6). This setup provides probe tip input powers from -23 dBm to -7 dBm.

$$P_{probe\_tip} = P_{coupler\_thru\_port} + P_{coupler\_offset} + P_{adapter,cable,probe\_loss} \tag{5.6}$$

Using the described measurement setup, the change in the receiver power detector output voltage was measured over input power as shown in Figure 5.13. As predicted by Equation (5.4), the change in output voltage increases linearly with input power. While Figure 5.13 uses a logarithmic scale for the change in output voltage, the input power is also using a logarithmic scale since the units are in dBm. There is a linear

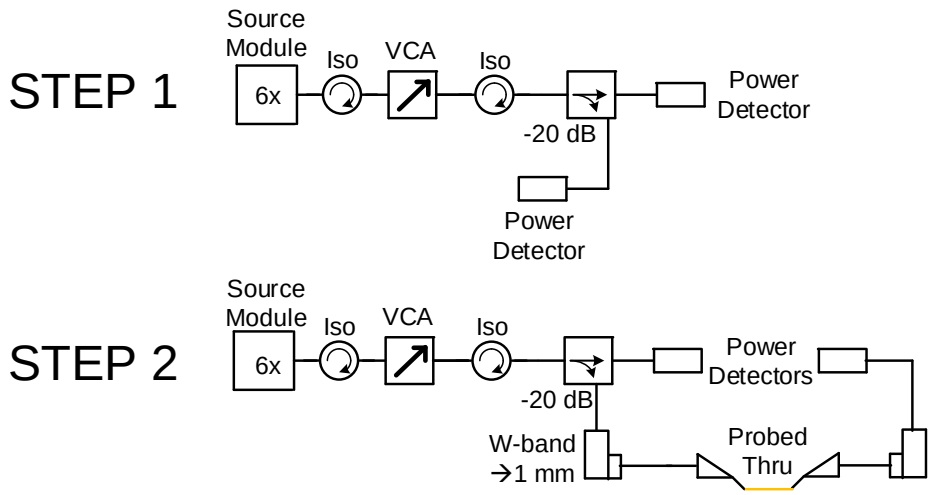

Figure 5.12: Required steps to determine the power level at the probe tip.

relationship between the change in power detector voltage and the input power in Watts. The slope of this line is the responsivity and can be used to predict the power level based on Equation (5.7).

$$P_{predict} = \frac{\Delta V}{\Re} \tag{5.7}$$

Figure 5.14 shows the measured responsivity of the receiever power detector test structure over input power for several die. The low die-to-die variation and constant response over input power indicate that a single responsivity value can be used with reasonable accuracy to predict the power level based on the change in power detector output voltage. Based on Figure 5.14, the receiver responsivity is estimated to be 400 V/W.

To demonstrate the feasibility of the front-end BIST switch approach, the responsivity measured on the power detector test structure is used to predict the power at the receiver node based on the change in output voltage and Equation (5.7). The predicted power is compared to the actual probe tip power level dtermined from the power calibration. Figure 5.15 shows the error between the predicted and actual

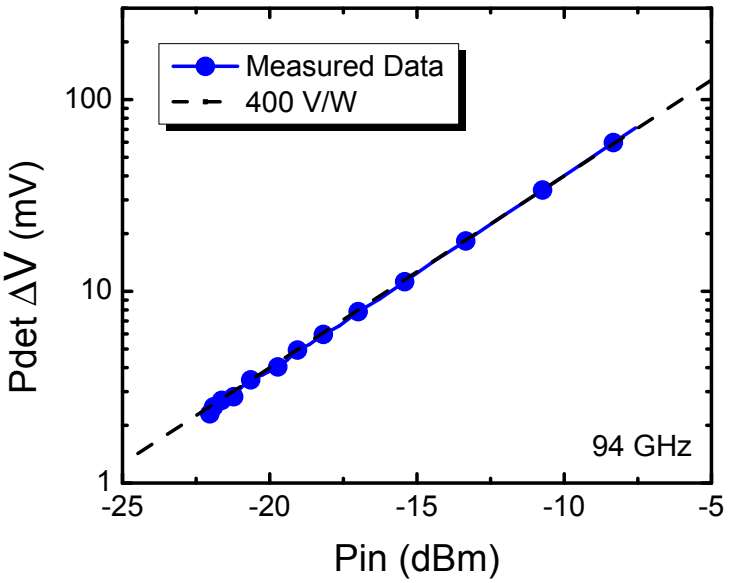

Figure 5.13: The measured change in the output voltage of the receiver power detector as a function of the RF input power.

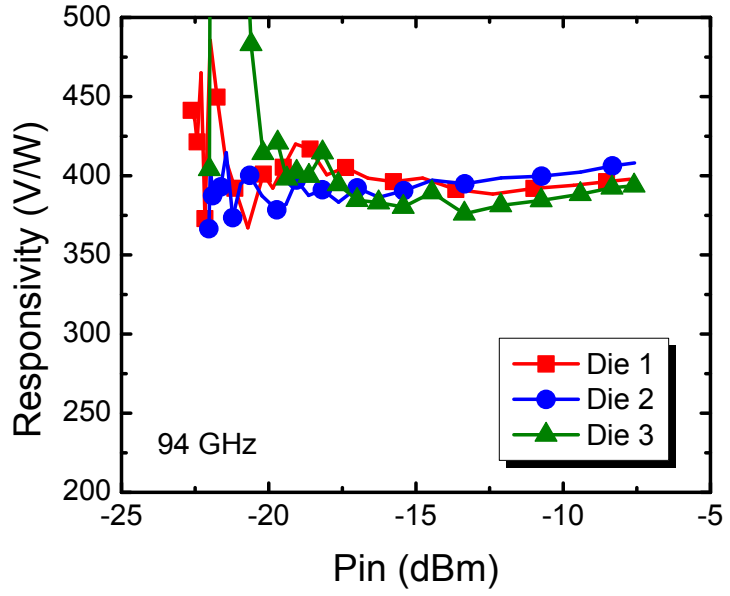

Figure 5.14: The measured responsivity of the receiver power detector test structure at 94 GHz plotted over input power for 3 different die.

power for four different die. The error is less than 0.5 dB for -20 dBm to -7 dBm.

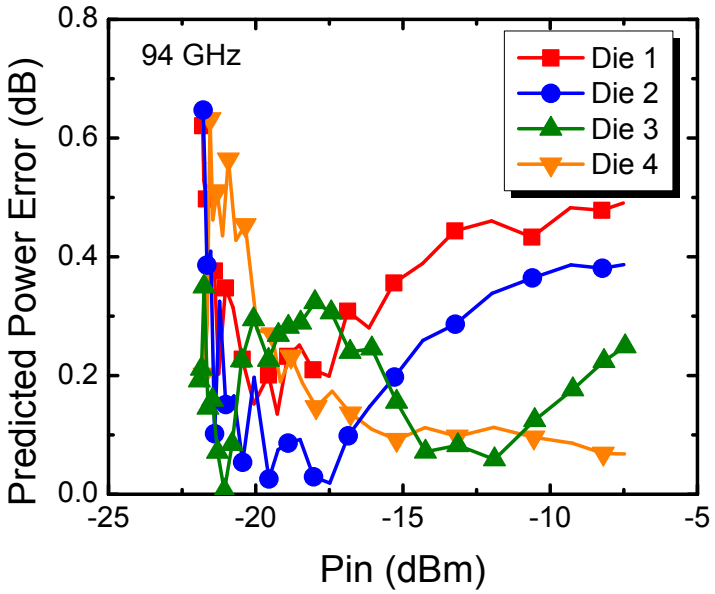

Figure 5.15: The error in predicted receiver power at 94 GHz for multiple die assuming a responsivity of 400 V/W.

To further establish this approach, the error in the predicted power is measured over the collector bias of the power detector. This is important since there will be some system drift in the bias point over time. If the power detector responsivity is extremely sensitive to the bias point then large errors in the predicted power will occur as the system drifts from the initial bias point. Figure 5.16 shows the variation in the responsivity and predicted power error assuming a responsivity of 400 V/W over the collector bias current for Die 4. As expected from Equation (5.5), the responsivity increases with the collector bias. However, the predicted power error is less than 0.5 dB from 160-200 uA. This demonstrates that even with moderate system drift, the power can still be predicted with reasonable accuracy.

In addition, the front-end BIST switch is measured over frequency. Figure 5.17 shows the responsivity of the power detector over frequency. Due to the relatively flat response of the responsivity over frequency, the power at the receiver node can be

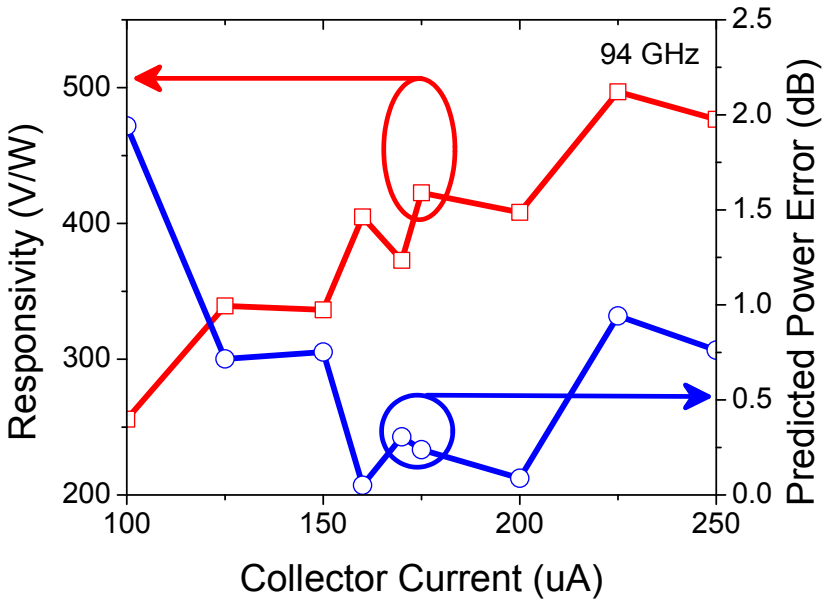

Figure 5.16: The measured responsivity of the receiver power detector and the error in the predicted power level at 94 GHz plotted over the power detector collector bias current.

predicted over frequency using a single responsivity value. This indicates, the front-end BIST switch could be used to predict the gain of the receiver over frequency without additional power detector test structure measurements.

5.4.2 Transmitter Measurements

Similar measurements were carried out for the transmitter power detector test structure and full front-end BIST switch. To achieve the appropriate power levels expected from the power amplifier, a 25 dBm Millitech PA was added to the measurement setup and the coupler was reoriented, as shown in Figure 5.18. This setup provides probe tip input powers from 0 dBm 13 dBm.

Figure 5.19 shows the change in the power detector output voltage as the input power is swept. Once again a nice linear response occurs between the input power and change in power detector output voltage. In comparison to the receiver power detector, the responsivity of the transmitter power detector is much lower. This

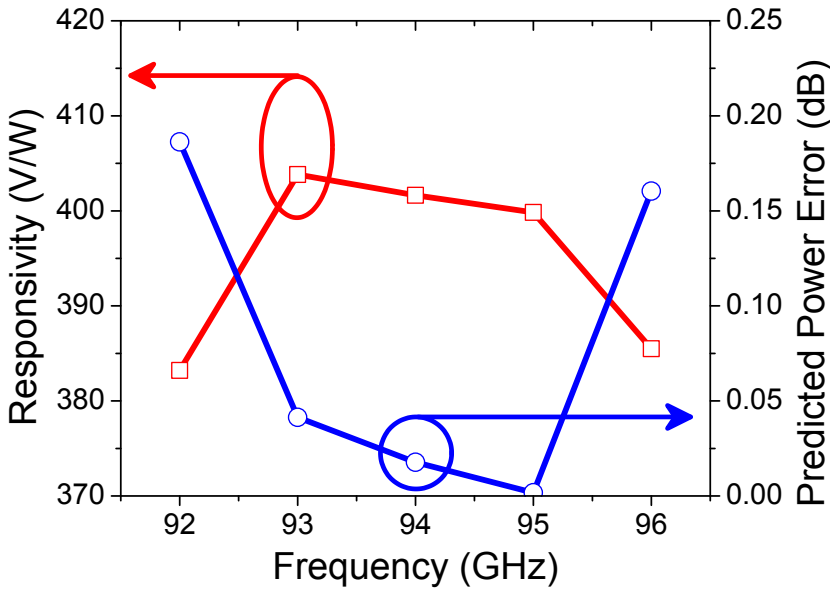

Figure 5.17: The measured responsivity of the receiver power detector and the error in the predicted power level plotted over frequency.

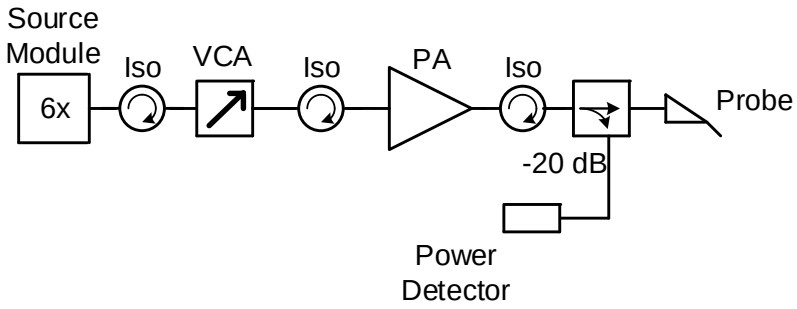

Figure 5.18: Block diagram of the setup used for the transmitter power measurements.

because the capacitive coupler has been designed for a lower coupling ratio so the compression of the transmitter power detector responsivity doesn't occur until higher power levels.

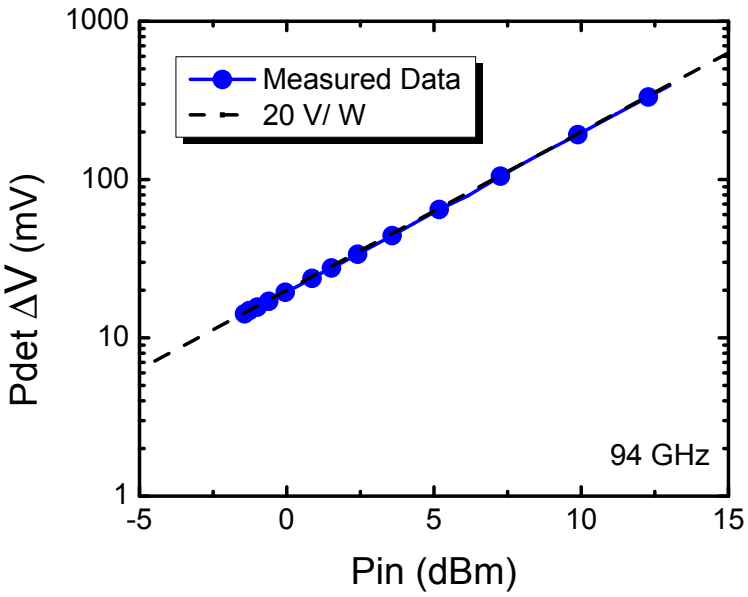

Figure 5.19: The measured change in transmitter power detector output voltage at 94 GHz plotted over input power.

Figure 5.20 shows the responsivity over input power for three different die. Good consistency is seen between die and the transmitter power detector is estimated to have a responsivity of about 20 V/W.

Assuming a 20 V/W responsivity for the transmitter power detector, the predicted power error is plotted for several die while measuring the full front-end BIST switch in BIST mode. As can be seen in Figure 5.21, the error for the transmitter power detector is higher than that of the receiver power detector. While the variation between die is fairly low, there is a consistent offset between the front-end BIST measurement and the test structure measurement. The responsivity of the power detector within the front-end BIST switch is approximately 17 V/W, instead of 20 V/W as measured on the test structure. This disparity may be due to the different

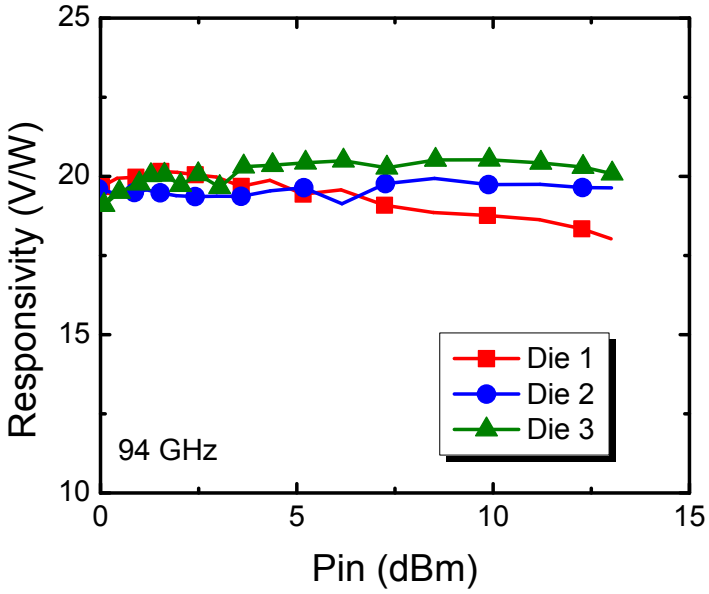

Figure 5.20: The measured responsivity of the transmitter power detector test structure plotted over input power for 3 different die.

impedance presented to the transmitter half of the circuit in the test structure and full front-end BIST switch.

In multi-element phased-array systems, it may be more appropriate to use the full front-end BIST switch as the test structure to determine the responsivity to the power detectors embedded in the phased-array. In this case, the matching conditions of the power detectors are exactly the same as the matching conditions of the power detectors in the full phased-array. Thus, it should minimize any offset between the responsivity of the test structure and the responsivity of the actual system. Almost no additional area is required to use the full front-end BIST structure as the test structure for determining the responsivity. Using separate tansmitter and receiver power detector test structures requires two 600 μm x 600 μm circuits and the front-end BIST switch is 1100 μm x 700 μm. Adjusting the responsivity to 17 V/W reduces the predicted power error as shown in Figure 5.22. The error reduces to less than 0.5 dB from 0-13 dBm for all die.

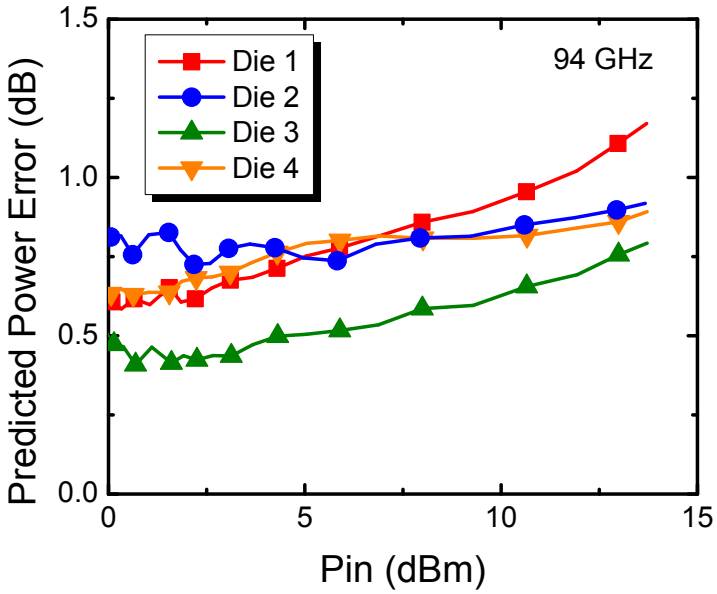

Figure 5.21: The error in predicted transmitter power for multiple die assuming a responsivity of 20 V/W.

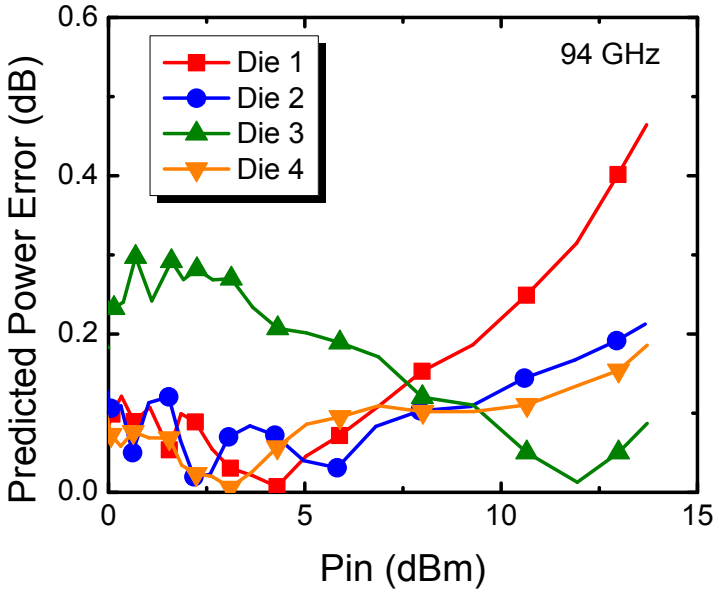

Figure 5.22: The error in predicted transmitter power at 94 GHz for multiple die assuming a responsivity of 17 V/W.

The transmitter power detector is also checked to determine the sensitivity to system drift and bias changes. Figure 5.23 shows less than 0.5 dB predicted power error from 200 μA to 270 μA when the adjust responsivity of 17 V/W is used to predicted the output power. This indicates the change in output voltage should remain almost the same despite small bias changes.

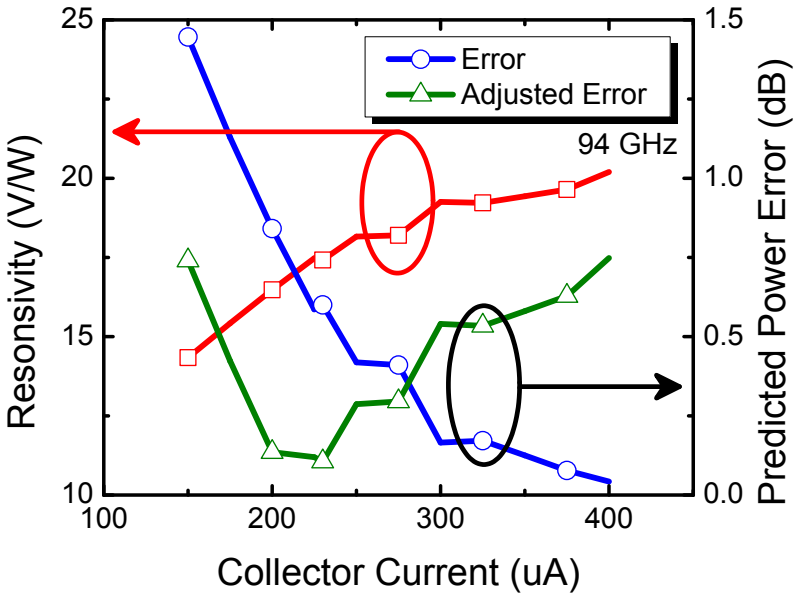

Figure 5.23: The measured responsivity and error in predicted power of the transmitter power detector in the full front-end BIST switch at 94 GHz plotted over the collector current. The first predicted power uses a responsivity of 20 V/W. The adjusted predicted power uses a responsivity of 17 V/W.

Figure 5.24 shows the variation in the responsivity of the transmitter power detector in the full front-end BIST switch over frequency and the resulting predicted power error. The adjusted predicted power error is less than 0.5 dB from 92-96 GHz.

The front-end BIST switch has been designed to be incorporated into a 94 GHz T/R module designed at Georgia Institute of Technology. The maximum output power of the PA in the T/R module is 10 dBm The LNA has a input P1dB of -10 dBm. The front-end BIST switch has been designed to accommodate these power levels. The transmitter power detector has demonstrated it can provide 0.5 dB accuracy

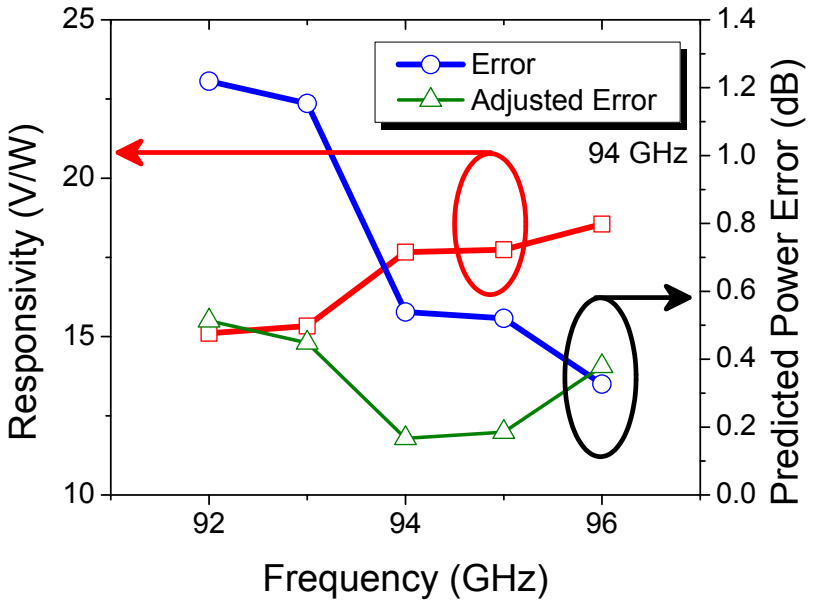

Figure 5.24: The responsivity and error in predicted power of the transmitter power detector in the full front-end BIST switch plotted over frequency. The first predicted power uses a responsivity of 20 V/W. The adjusted predicted power uses a responsivity of 17 V/W.

from 0-13 dBm. In BIST mode, Q1 in Figure 5.2 is turned on attenuating the signal between the transmitter and receiver. The attenuation was measured to be 23 dB between the transmitter and receiver using the power setup in Figure 5.18. As a result, the power injected to the receiver in BIST mode is approximately -13 dBm and is below the compression point of the LNA.

5.5 Summary

The front-end BIST switch demonstrates the ability to predict the power at the transmitter and receiver nodes based on the DC output voltage of the on-die power detectors. This is an exciting innovation for large scale arrays where the cost of measurement and verification can often dominate the overall cost of development.

A chip containing up- and down-conversion mixers with the front-end BIST switch could quickly be checked for basic functionality by using the loop-back testing. With

only DC bias and IF signals the attenuated transmit signal would be fed back into the receiver in the BIST mode. To further verify the system functionality, the on-die power detectors could be used to measure the power at the transmitter and receiver nodes. Depending on the required accuracy of the verification, the power levels could be estimated based off the simulated responsivity of the power detectors or for better accuracy, based off the measured responsivity of power detector test structures. Combining these power levels with the signal power at IF would provide the transmitter and receiver gain without millimeter-wave equipment. The gain variation of VGAs in the system could also be characterized. Since the power detectors are inherently large signal sensors, the P1dB of the transmitter and receiver could also be determined. In addition, since the antenna port is isolated from the transmitter and receiver while in BIST mode, changes in the antenna impedance will have little impact on the BIST mode of operation. This makes the front-end BIST switch well suited to monitor the system health over time.

The front-end BIST switch is currently being packaged and characterized in a single channel T/R module. The T/R module includes the front-end BIST switch, LNA, PA, and up- and down-conversion mixers, as shown in Figure 5.25. The results will further explore the ability of the front-end BIST switch to provide self-testing capabilities.

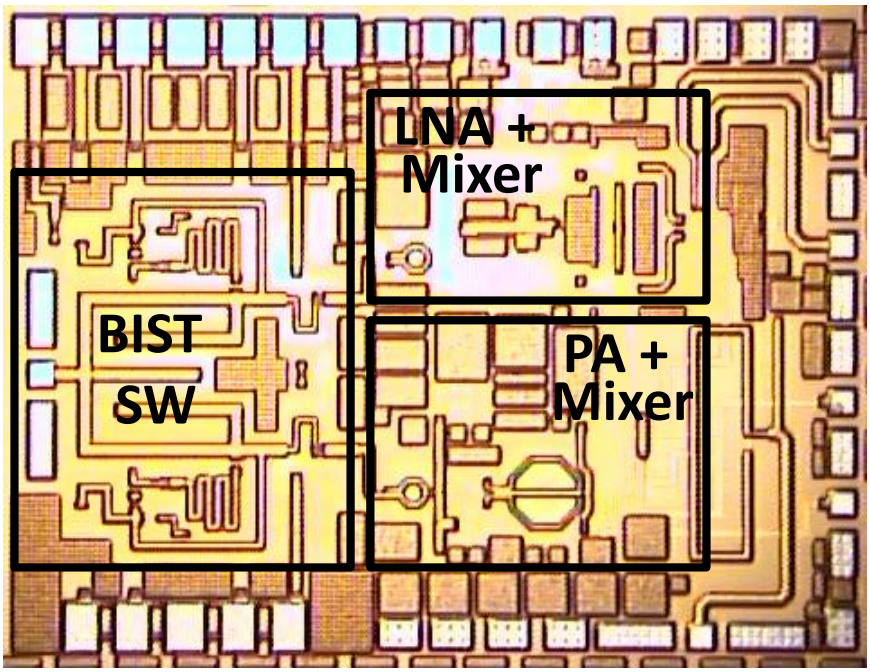

Figure 5.25: Die photograph of the front-end BIST switch integrated in a T/R module.

CHAPTER 6

HIGHLY INTEGRATED SIGE HBT W-BAND RADIOMETER

In order to detect small noise temperatures, the incoming signal must be amplified before reaching the power detector using an LNA. This is the basic topology of a total power radiometer. However, the gain variations and 1/f noise of the LNA is a concern and can change the responsivity of the system over time. As discussed in the introduction, a Dicke switch topology is commonly utilized to overcome these issues by periodically calibrating to a known temperature reference.

The sensitivity (ΔT) of a radiometer is the minimum change in temperature the system can detect. Equation (6.1) shows the sensitivity of a total power radiometer, where T_A is the antenna temperature, T_N is the noise temperature of the receiver, β is the system bandwidth, τ is the integration time, G is the LNA gain, and ΔG is the change in gain over time. In a total power radiometer, it is impossible for the system to distinguish between changes in the LNA gain and changes in the noise emitted by the targeted object. Often the (ΔG/G) term is the main limitation in the minimum sensitivity. In a Dicke radiometer topology, switching between the antenna and a known temperature reference at a speed faster than the 1/f noise corner of the receiver minimizes the impact of gain variations. However, for a Dicke radiometer, there is a factor of two penalty in the sensitivity, as shown in Equation (6.2), because half of the integration time is spent connected to the reference temperature.

$$\Delta T_{TotalPower} = (T_A + T_N)\sqrt{\frac{1}{\beta\ \tau} + \left(\frac{\Delta\ G}{G}\right)^2} \tag{6.1}$$

$$\Delta T_{Dicke} = 2 * \frac{T_A + T_N}{\sqrt{\beta\ \tau}} \tag{6.2}$$

In addition, the Dicke switch topology also degrades the radiometer because the switch loss increases the noise temperature of the receiver. As a result, the loss of the switch must be kept to an absolute minimum. However, the calibration of radiometers is often as critical as the design of the radiometer itself and using switches to connect to multiple noise source can be used for accurate calibration. For example, in earth science instruments, multiple noise references are often used to provide more accurate noise measurements and to prevent problems caused by the drift of individual noise sources. The NASA Jason Microwave Radiometer project, which was used until 2013 to determine atmospheric water vapor content, contains six different noise reference diodes [59]. This work leverages the excellent performance of the reverse-saturated switch design to create a high performance, highly-integrated radiometer.

A system diagram of the W-band radiometer is shown in Figure 6.1. The system consists of a 4-way switch with an integrated hot temperature reference and an ambient temperature reference. The 4-way switch features a unique design in which any two of the four ports may be connected with a low-loss path, while isolating that path from the other ports. The switch is followed by a high gain W-band LNA [116] to amplify the noise received at the antenna to detectable levels. Finally, this signal is fed into a power detector, which converts the W-band RF signal into a DC voltage. The radiometer was designed in the IBM 9HP 90 nm SiGe HBT technology.

Figure 6.2 shows a die photograph of the full radiometer. The radiometer is 1750 μm x 900 μm including pads. The small footprint of the radiometer indicates the potential to create highly-integrated miniature radiometers on SiGe BiCMOS platforms. In the future, other key circuit blocks such as low frequency amplifiers, integrators, ADCs, and switch drivers could be integrated to create a single-chip

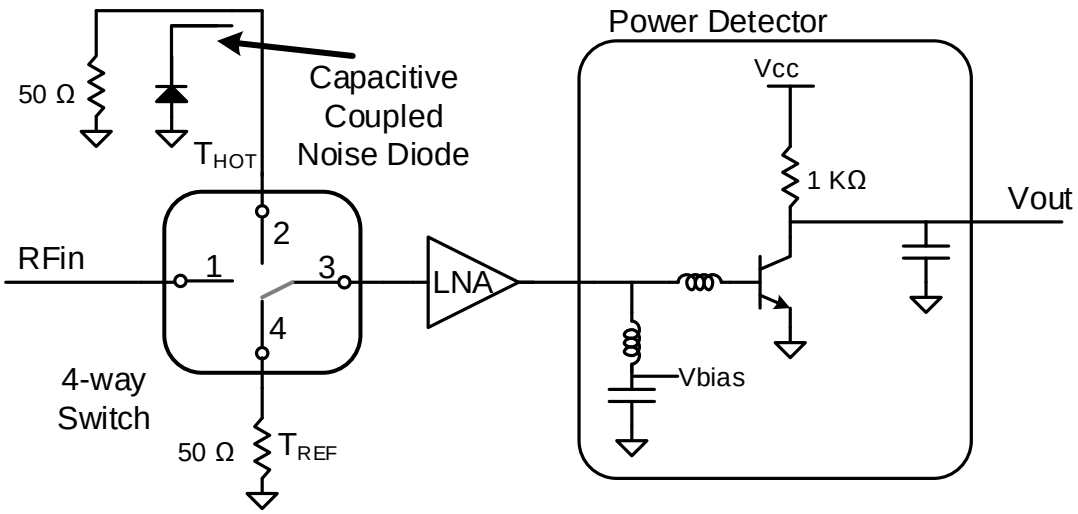

Figure 6.1: Block diagram of the highly-integrated W-band radiometer.

radiometer.

6.1 Radiometer Circuit Block Designs

6.1.1 4-way Switch

The 4-way RF switch with the hot and ambient temperature references can be achieved by adding two more quarter-wave shunt sections in to the typical SPDT topology. The schematic of the reverse-saturated 4-way switch is shown in Figure 6.3. In this topology, the RF energy is block from the isolated ports by applying a high voltage to the shunt device at the corresponding ports. The low impedance of the on-state SiGe HBT is transformed to an open impedance at the cross junction. This allows most of the RF energy to flow between the other two ports, where the shunt devices are turned off. Since the circuit is symmetric with respect to the cross junction, any two ports can be connected while isolating that transmission path from the other two ports. Furthermore, as a result of the symmetry of the circuit, the insertion loss and isolation are nearly the same in all states. This technique can be extended to include additional on-die noise references for improved accuracy and reliability.

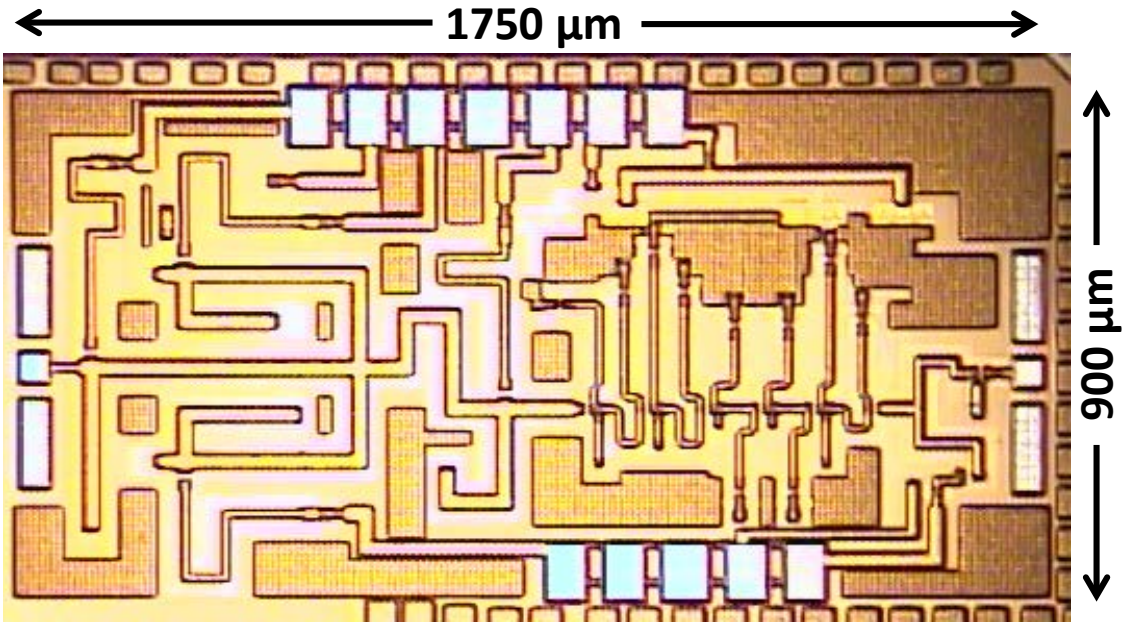

Figure 6.2: Die photograph of the full W-band radiometer system.

The symmetry also means that measuring the noise source at the input port is an accurate characterization of the noise source when it is connected to the receiver. This property is under investigation to determine if it provides benefits in simplifying calibration or monitoring the drift of the temperature references.

The ambient temperature reference is implemented with a 50 Ω load connected at the end of one of the quarterwave shunt switch sections. It is well known and common practice to use a matched 50 Ω load to produce a noise temperature equal to the ambient temperature of the system [59]. The hot temperature reference is implemented using a diode-tied SiGe HBT with the base and emitter shorted together. The collector-base junction of the SiGe HBT is reverse-biased near the breakdown of the pn junction. At this bias, the SiGe HBT is at the onset of avalanche multiplication and produces significant noise [117]. This noise is coupled into the system using a capacitive coupler. In order to remain well matched to 50 Ω, the quarterwave shunt section of the hot temperature reference is also terminated in a 50 Ω load. The capacitive coupler provides roughly -9 dB loss. As a result, the change in impedance

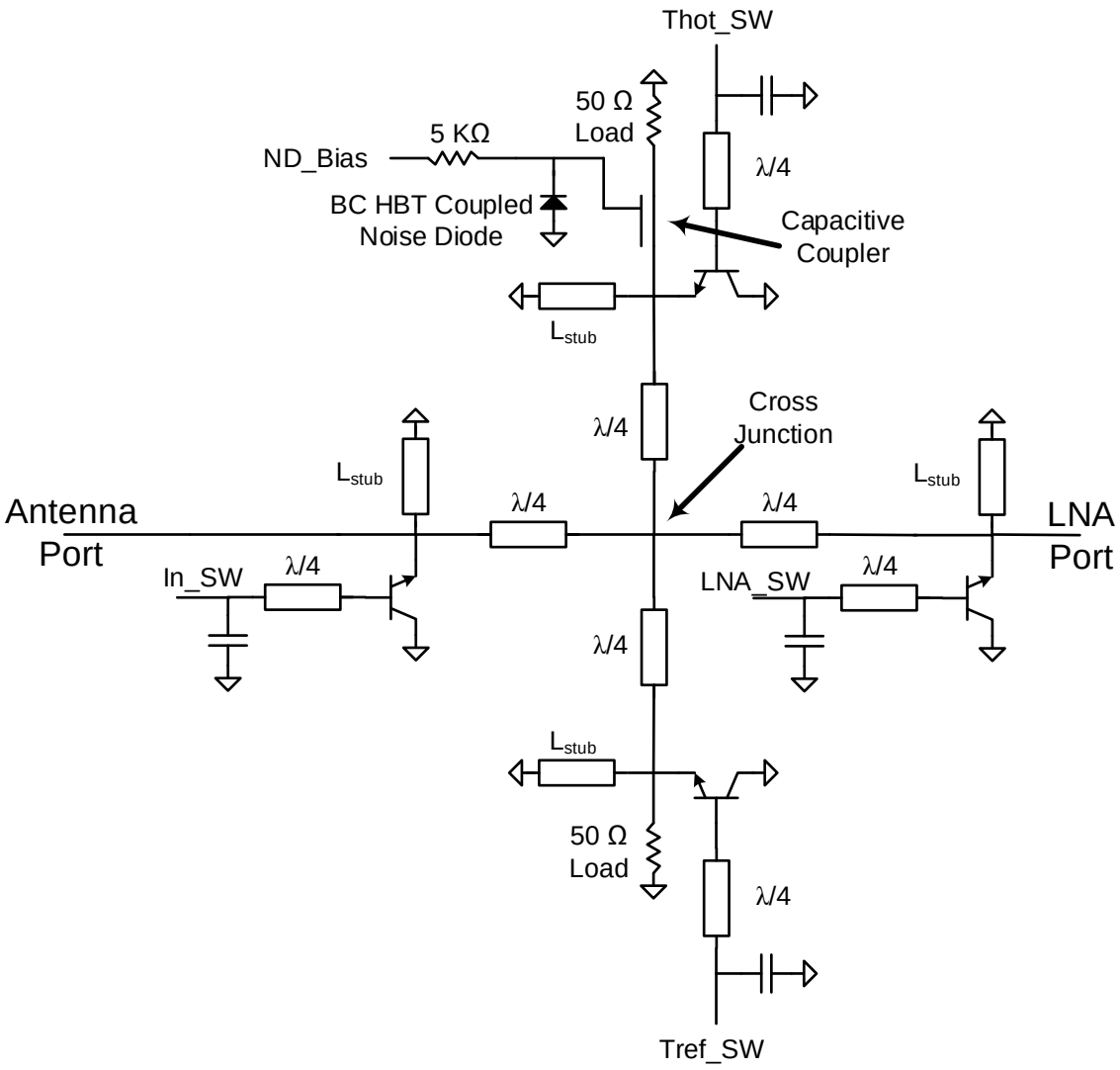

Figure 6.3: Schematic of the 4-way switch connected to the hot and ambient temperature references.

of the collector-base diode does not significantly change the matching when it is reverse-biased near breakdown. In the future, the hot and ambient temperature references could be implemented with a single switch leg by turning off the diode in the ambient state and activating it in the hot state.

The 5 KΩ resistor in the hot temperature reference also plays an important role in creating a feasible hot temperature reference. The breakdown of the collector-base junction is very rapid due to avalanche multiplication around 5.3 V. Biasing the junction above 5.3 V causes permanent damage to the device. As a result, it is very difficult to bias the diode near avalanche to produce high noise, without damaging the device. Using a 5 KΩ biasing resistor limits the current through the diode and prevents rapid breakdown. Figure 6.4 shows the measured diode IV curves with and without the 5KΩ bias resistor. Post IV measurements showed the diode without the 5 KΩ resistor was permanently damaged, whereas the 5 KΩ resistor was able to protect the diode.

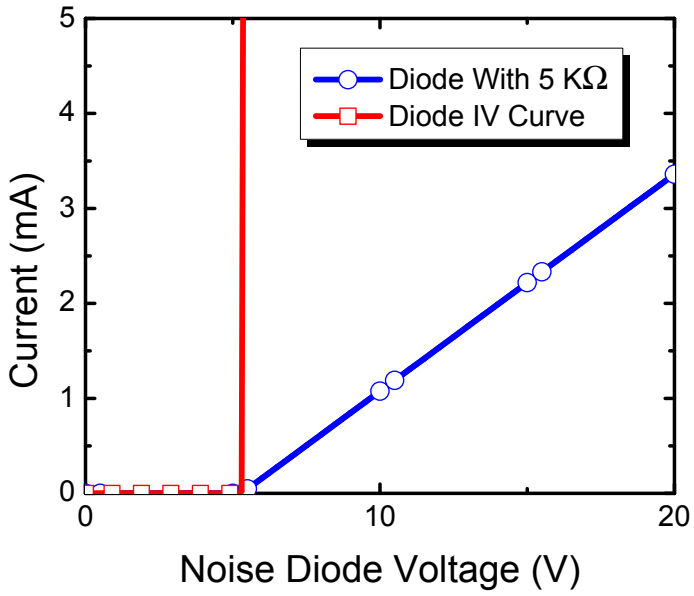

Figure 6.4: Comparison of the SiGe HBT collector-base diode IV curves with and without the 5 KΩ biasing resistor.

A test structure circuit was fabricated to determine the performance of the 4-way switch, as shown in Figure 6.5. The test structure is 1000 μm x 900 μm. Unfortunately, it was not possible to measure the S-parameters of the 4-way switch due to equipment failures. However, using a power measurement setup similar to Figure 5.18, it was possible to determine the difference in power levels in the on- and off-states. Figure 6.6 shows the estimated insertion loss and isolation from 92-96 GHz using the power measurement setup. The insertion loss and isolation are approximately 2.5 dB and 21 dB respectively. It is anticipated that this is a conservative estimation of the insertion loss. Due to additional reflections and pad losses, the insertion loss of the switch is estimated to be about 2 dB. The simulated insertion loss was 1.7 dB, but it is expected that the loss will be slightly higher than simulation since the model has been shown to overestimate the off-state impedance of the reverse-saturated SiGe HBT in the SPDT and the front-end BIST switch. The S-parameters of the 4-way switch will be measured when W-band PNA is fixed.

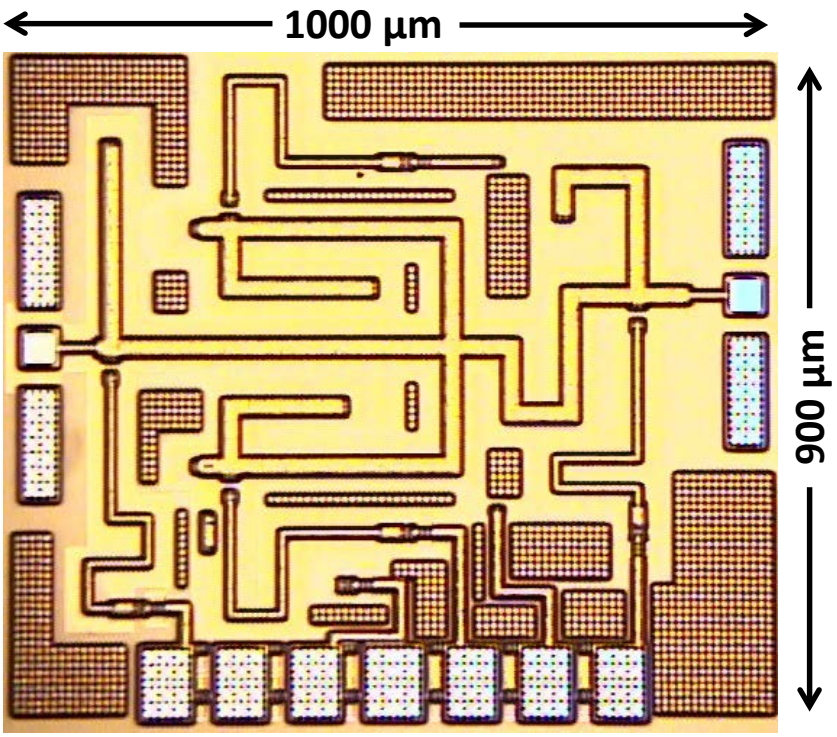

Figure 6.5: Die photograph of the 4-way switch test structure.

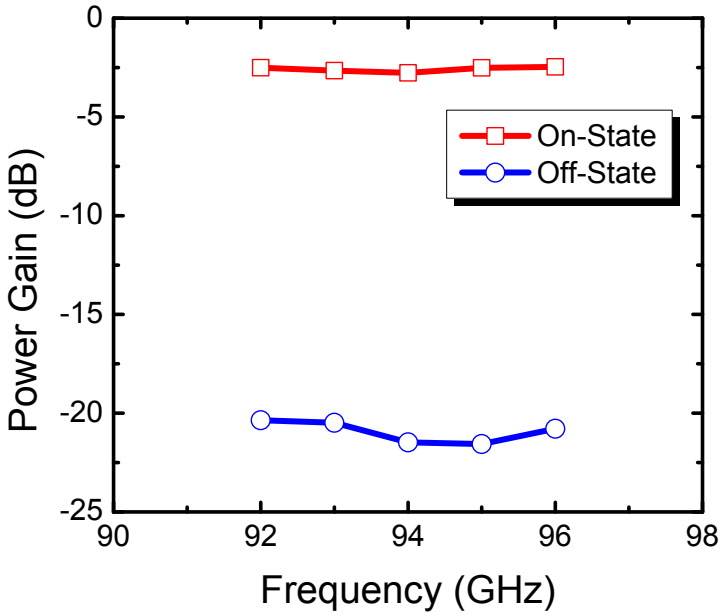

Figure 6.6: Measured insertion loss and isolation using large-signal power measurements.

The unique capability of the 4-way switch to connect any two ports, while isolating the others means the switch has six different distinct states. This may be useful in a wide variety of applications. One straight forward example is to us the 4-way switch to connect a single transmitter and receiver to two antennas of vertical and horizontal polarizations. Using multiple polarizations enables more information to be extracted about a target object in radar and imaging applications and can improve the reliability of signal detection [118]. Previously to achieve systems with multiple polarizations, multiple transmitters or receivers had to be placed within the same system [45]. Using the 4-way switch would significantly reduce the footprint and complexity of these systems.

6.1.2 W-band Low-noise Amplifier

The W-band LNA has been previously published in collaboration with another student [116]. It features a maximum measured gain of 35 dB at 81 GHz and a

minimum measured noise figure of 3.5 dB at 80 GHz. A gain of 25 dB and noise figure of less than 4.5 dB is achieved over the entire 75-110 GHz W-band. This is state-of-the-art LNA performance and it is the first SiGe based W-band LNA to demonstrate less than 4 dB noise figure. The large gain and low noise are critical for radiometer applications. The high gain increases the responsivity of the radiometer, allowing it to amplify small noise temperatures to measurable values. The low noise figure reduces the noise temperature of the radiometer and enables a smaller sensitivity.

6.1.3 W-band Power Detector

Similar to the power detectors in the front-end BIST switch, the power detector in the radiometer makes use of the linear relationship between input power and change in output voltage at low bias currents. However, while the power detectors in the front-end BIST switch were purposefully mismatched at the input to decrease the responsivity, the radiometer requires high responsivity. Figure 6.7 shows the schematic of the power detector. A shunt-series transmission line network is utilized to match the input to 50 Ω at 94 GHz while also providing a means to bias the base of the transistor. At the output, the power detector is connected externally to a Stanford Research Systems, SRS-552 amplifier. This amplifier has a minimum noise figure at a 1 KΩ input impedance. As a result the power detector has been designed to have an output impedance of 1 KΩ. While many W-band power detectors include a shunt L-C notch filter at the output to reduce the RF feed through from the input to the output, this has little benefit over a simple shunt capacitor at 94 GHz. In this design, it was decided to only include a shunt capacitor at the output to reduce the circuit foot print.

The power detector test structure is shown in Figure 6.8. The test structure is only 350 μm x 700 μm and mostly dominated by the size of the pads. The power detector DC output voltage has been routed to RF pads so that the RF feed through

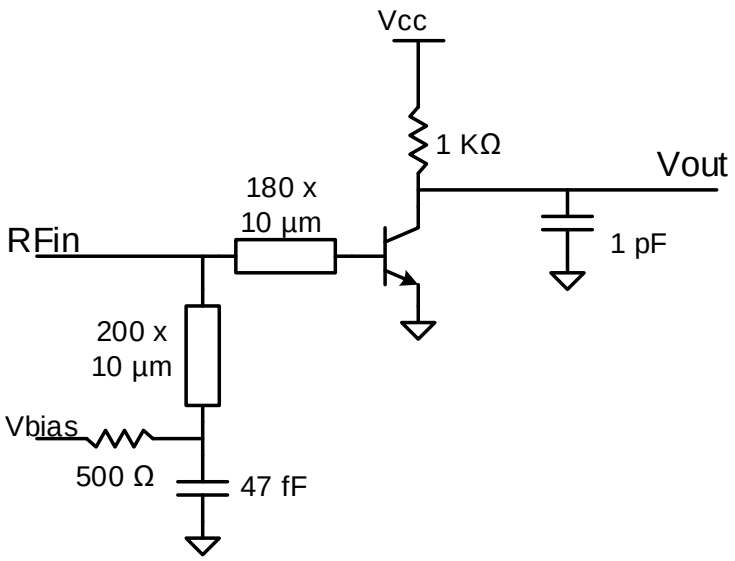

Figure 6.7: Schematic of the W-band power detector block in the highly-integrated radiometer.

can be measured with a PNA.

Unfortunately, due to equipment failures, the S-parameters of the power detector could not be measured to analyze the input matching and the RF feed through. However, the operation of the power detector was demonstrated with large signal measurements. Figure 6.9 shows the measured responsivity at 94 GHz plotted over the collector current bias of the power detector. As expected, the responsivity increases with the bias current. However, with a 1 KΩ resistor in the bias network, the SiGe HBT begins to push into saturation at high bias currents, reducing the responsivity.

$$NEP = \frac{V_n}{\Re} \tag{6.3}$$

A common FoM for detectors if the Noise Equivalent Power (NEP), which is given by the output noise voltage divided by the resposnivity, as shown in Equation (6.3). Since the noise of the power detector increases with the collector current, the bias point for minimum NEP is on the left side of the peak responsivity bias [47], shown

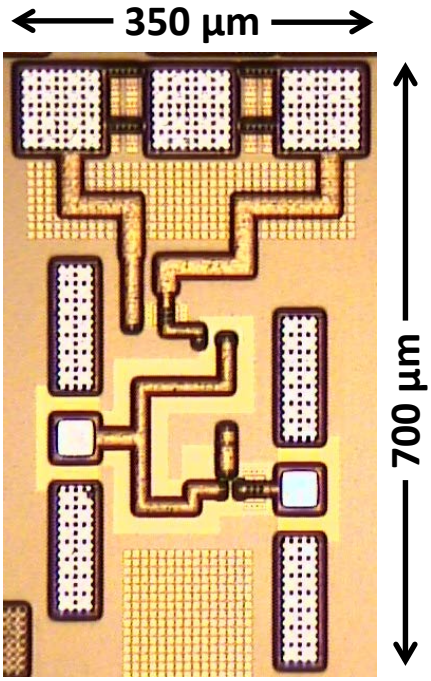

Figure 6.8: Die photograph of the power detector test structure.

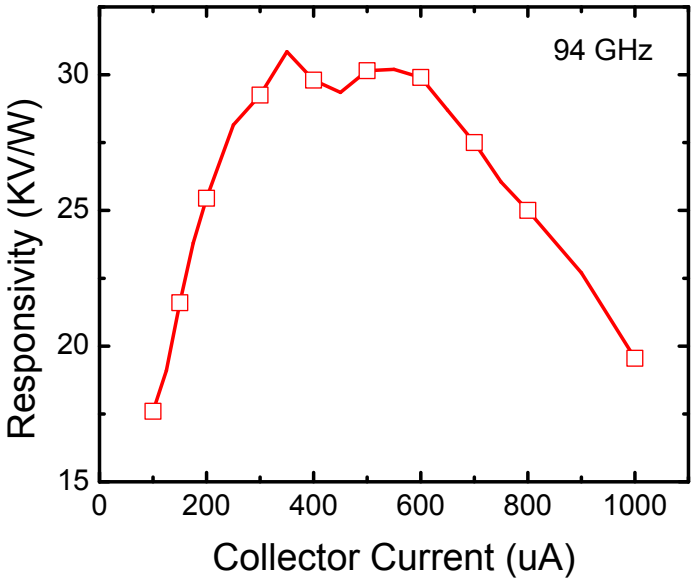

Figure 6.9: Measured responsivity of the power detector test structure at 94 GHz.

in Figure 6.9. Here, the nominal bias point is 170 uA, with a responsivity of roughly 22 KV/W.

Figure 6.10 shows the responsivity measured from 90-100 GHz at 170 uA and 250 uA. The plot shows the responsivity is larger than 20 kV/W over the entire 90-100 GHz range. Wideband radiometers are highly desirable since the sensitivity reduces with the bandwidth of the system.

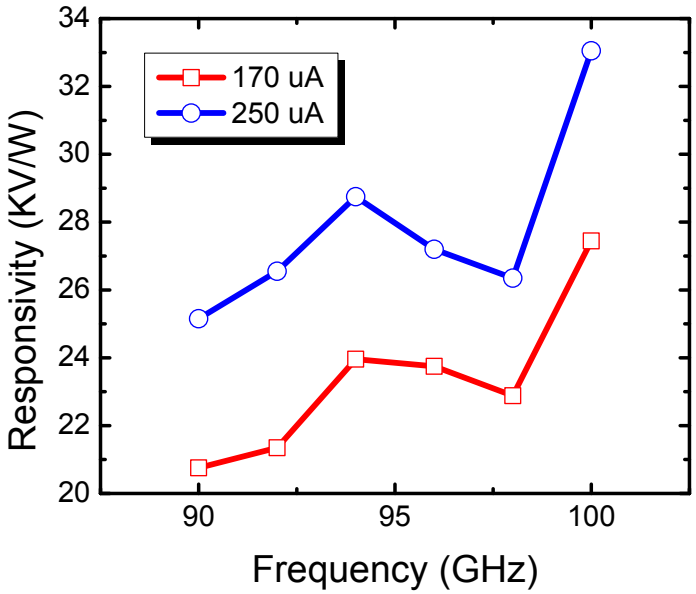

Figure 6.10: Measured responsivity of the power detector test structure over frequency.

6.2 W-band Radiometer Measurements

The responsivity of the radiometer was measured using a setup similar Figure 5.11. Figure 6.11 shows the change in the radiometer output voltage and responsivity as a function of the input power. As desired, the radiometer is sensitive to even very small input powers. The responsivity begins to compress at -40 dBm.

The responsivity of the entire radiometer system can be estimated from the circuit block performance assuming a perfect match between blocks according to Equation (6.4). If the switch loss is estimated to be 2 dB, the LNA gain is 30 dB, and the

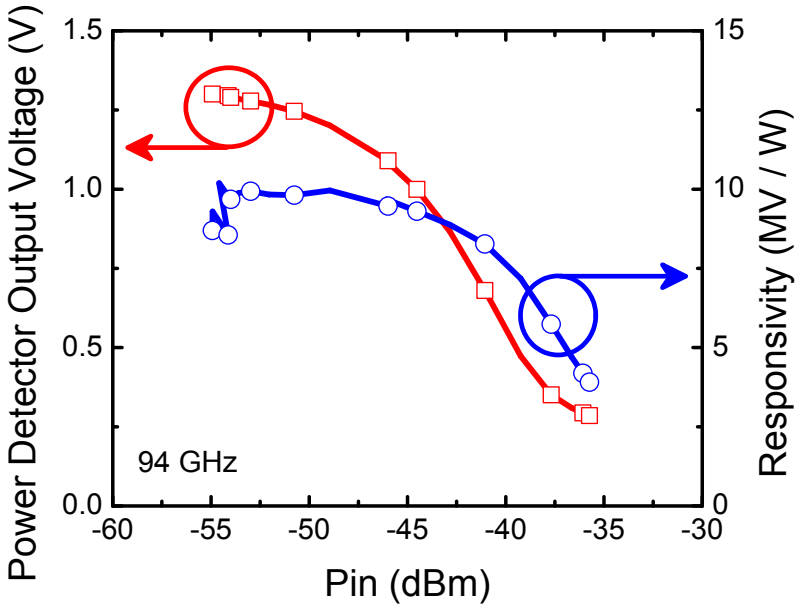

Figure 6.11: Measured radiometer output voltage and responsivity as a function of the input power.

responsivity of the power detector is 22 KV/W, then the estimated responsivity of the whole radiometer is 13 MV/W. It is expected this will be an over estimate since there will be losses due to mismatch, but it gives a reasonable estimation to verify correct functionality of the overall system.

$$\Re_{radiometer} = \left(10^{-IL/10}\right) * \left(10^{LNA\_S21/10}\right) * \Re_{power\_detector} \tag{6.4}$$

Figure 6.12 shows the responsivity of the radiometer over the collector current bias of the power detector. As expected the responsivity is slightly less than that estimated from Equation (6.4). The radiometer shows a similar responsivity result over bias current in comparison to the power detector test structure but is roughly three orders of magnitude larger. The nominal bias point of 170 uA is chosen to balance the increase in responsivity at high bias currents with the larger noise.

The responsivity of the radiometer is also characterized over frequency from 90-100 GHz, as shown in Figure 6.13. The responsivity is greater than 4 MV/W for

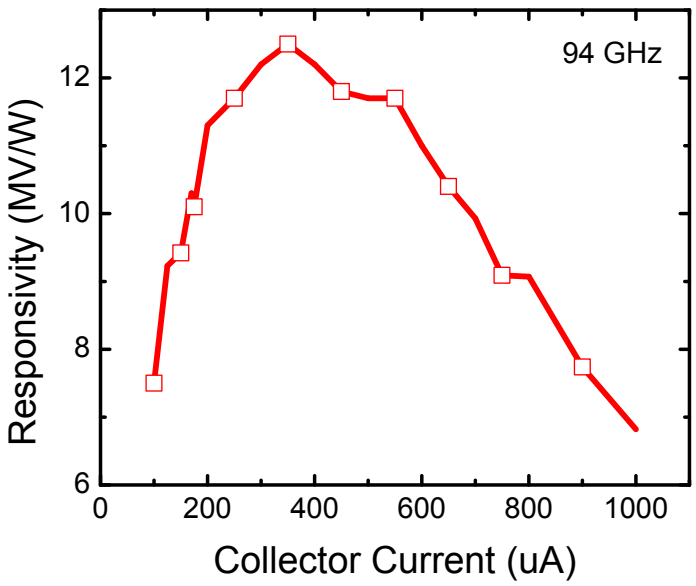

Figure 6.12: Measured responsivity of the radiometer at 94 GHz plotted over collector bias current of the power detector.

the entire range. In comparison to the power detector test structure in which the responsivity was reasonably flat over frequency, the full radiometer shows a clear trend of decreasing responsivity with frequency. This is due to the response of the LNA, where the gain decreases from 35 dB to 25 dB from 80 GHz to 100 GHz [116]. Future measurements will characterize the responsivity over a wider bandwidth to determine the full -3dB bandwidth of the system.

An exciting result of the highly-integrated SiGe radiometer was that it demonstrated the ability to use a coupled noise diode as an active hot temperature reference on-die. Previous to this work, very few publications have demonstrated an active hot temperature reference on silicon. To analyze the active hot temperature reference, the radiometer was biased with a high voltage on In_ SW and Tref_ SW (Figure 6.3). LNA_ SW and Thot_ SW were grounded to create a low-loss path from the coupled noise source to the LNA. The radiometer output voltage was measured while sweeping the bias voltage of the collector-base noise diode from 0-15 V and then back down

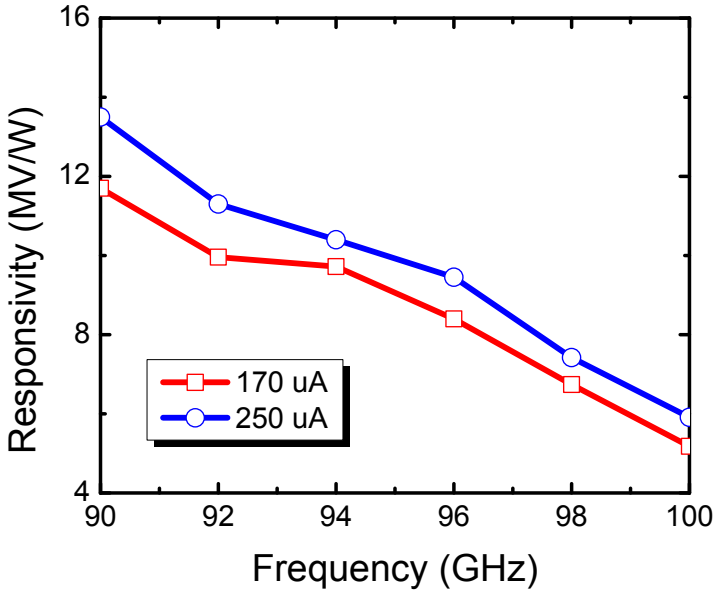

Figure 6.13: Measured responsivity of the radiometer over frequency.

from 15-0 V to ensure the results were not due to system drift. Figure 6.14 shows the output voltage of radiometer changes over 10 mV at a 15 V bias.

The radiometer output voltage was also measured while the 4-way switch had a low-loss path between the ambient temperature reference and the LNA. The noise diode bias voltage was swept from 0-15 V and back down from 15-0 V. As shown in Figure 6.14, the resulting change in radiometer output voltage is about an order of magnitude lower. This result is expected because the isolation of the switch is finite and some of the noise generated by the noise diode will leak into the Tref to LNA transmission path.

The noise measurements of the radiometer are currently in progress. However, the simulated noise spectrum is shown in Figure 6.15. The 1/f noise corner occurs at about 10 kHz and the noise above the 1/f noise corner is about 100 $nV/Hz^{1/2}$. The sensitivity can be estimated for a Dicke radiometer using Equation (6.5), where k is Boltzmann's constant. Estimating the performance of the radiometer at 8 MV/W for a bandwidth of 20 GHz, and using a integration time of 30 ms for video imaging,

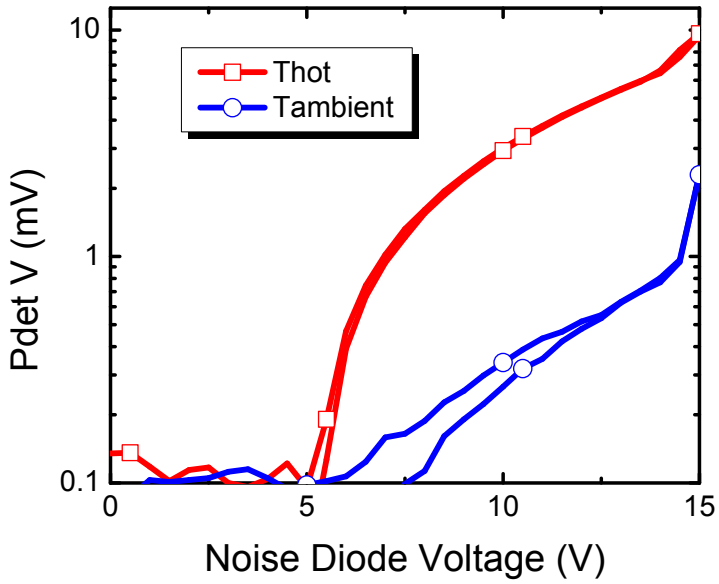

Figure 6.14: Measured change in the radiometer output voltage as a function of the noise diode bias, while the LNA is connected to the hot and ambient temperature references.

the sensitivity is calculated to be 0.37 K. This is very comparable to other literature on silicon, as shown in Table 6.1. However, this radiometer also has additional functionality and can switch to multiple temperature references. This is capability is beneficial since it is desirable to have the reference temperature near the temperature of the target object.

$$\Delta T = 2\frac{NEP}{kB\sqrt{2\tau}} \tag{6.5}$$

6.3 Summary

A highly-integrated W-band radiometer was developed with multiple on-die temperature references. A coupled noise diode was used to create an active hot temperature reference. A 50 Ω termination was utilized as the ambient temperature reference. The 4-way switch has an estimated insertion loss of 2 dB. The LNA has roughly 30

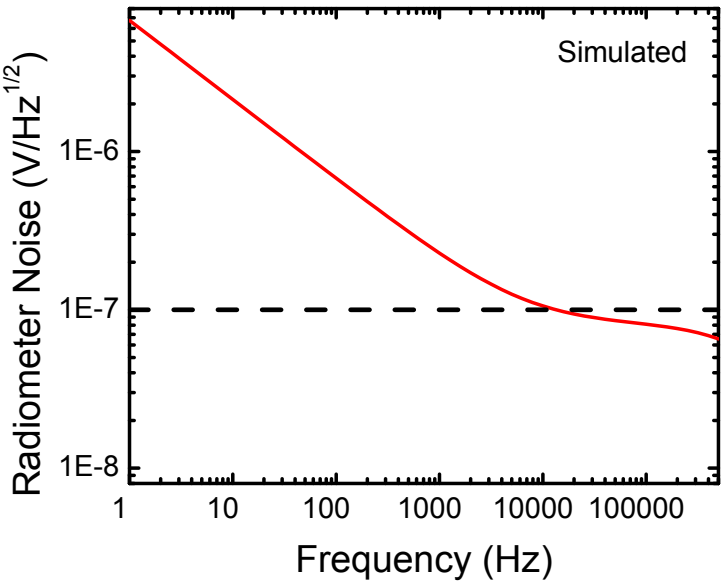

Figure 6.15: Simulated noise spectrum of the radiometer.

Table 6.1: Comparison of State-of-the-art Millimeter-wave Radiometers

Ref.	Tech.	Topology	$\Re$ (MV/W)	Integration (ms)	NEP ($fW/Hz^{1/2}$)	ΔT (K)
This	90 nm SiGe	SW + LNA + Pdet	8	30	12	0.37
[47]	130 nm SiGe	SW + LNA + Pdet	4	30	14	0.69
[119]	165 nm SiGe	LNA + Pdet	28	3.1	18	0.35
[103]	65 nm CMOS	SW + LNA + Pdet	0.09	30	200	10
[115]	180 nm SiGe	SW + LNA + Pdet + IF AMP	45	30	10	0.4
[120]	InP HEMT	LNA + Pdet	0.5	3.1	–	0.45

dB of gain and a 4 dB noise figure. The power detector achieved a responsivity of over 20 KV/W. The full radiometer responsivity was measured over 10 MV/W. The noise measurements are currently in progress, but it is anticipated based on previous designs, that the radiometer will achieve state-of-the-art sensitivity levels. In the future, further integration with low frequency amplifiers, integrators, switch drivers and ADCs could create an impressive single-chip radiometer solution.

CHAPTER 7

CONCLUSION

7.1 Summary of Contributions

This work explores novel techniques to reconfigure RF and millimeter-wave circuits and systems. The ability to reconfigure a system can provide several benefits including: meeting multiple standards or project requirements, adapting to environmental conditions, adjusting to process variations, calibrating a system, providing built-in-self-test capabilities, and monitoring system health. These benefits are especially well suited for highly-integrated silicon-based systems, which can support digital logic, analog circuitry, RF circuitry, and memory blocks with high yield. The specific contributions of this work include:

1. The analysis of current trends of transistor RF performances in CMOS and SiGe BiCMOS processes. The top metal layer f_T/f_{max} of a 120 nm SiGe HBT process was demonstrated to be 260/430 GHz in comparison to a top metal layer f_T/f_{max} of 210/245 GHz for 32 nm SOI CMOS.

2. The design of a frequency-agile low noise amplifier using a transistor core base-switch. The frequency-agile LNA can be tuned from 8.2 to 9.7 GHz at both the input and output, and has a measured noise figure of 2.6-3.3 dB.

3. The design of a digitally controlled seven state variable-gain LNA at 10 GHz. The digital control bits set the gain between 9.5 and 16.5 dB. The noise figure of 5 of the 7 states was less than 2 dB.

4. The development of a novel reverse-saturated SiGe HBT configuration for millimeter-wave switches. This configuration was analyzed in detailed and has demonstrated record setting insertion loss for silicon-based millimeter-wave switches.

5. The design of a novel front-end switch with a built-in-self-test system. This system allows the power levels at the transmitter and receiver nodes to be determined on-die with minimal millimeter-wave measurements. This is an exciting innovation that enables quick system verification and system health monitoring over time.

6. The development of a highly integrated radiometer with an ambient temperature reference and active hot temperature reference. The radiometer has state-of-the-art responsivity of over 10 MV/W.

7. The design of a novel 4-way switch, which allows any two ports to be connected with a low-loss path, while isolating the transmission path from the other ports.

7.2 Future Work

There are several extensions of this research that are exciting research topics.

1. Based on the technology trends research, bench mark circuits such as amplifiers and mixers can be designed to further compare the performance of SiGe HBT and advanced node CMOS technologies.

2. At X-band, sensors can be incorporated into transceivers to determine information about the environment such as the temperature and spectral power levels. This information can be fed back into the control knobs of the LNA and other circuit blocks to dynamically optimize performance to the environment.

3. The techniques used to create control knobs for the LNA can also be explored for PA design.

4. The reverse-saturated switch can be used in other switch variants to increase the off-state impedance of millimeter-wave switches.

5. The BIST switch capabilities can be incorporated into larger systems. Incorporating a differential power detector would make the measurements of the power levels less sensitive to system drift.

6. There are significant research opportunities for silicon-based radiometers. This field has been dominated by III-Vs but the ability to integrate multiple noise references, RF amplifiers, power detectors, low frequency amplifiers, and ADCs all on a single die is very attractive solution for small footprint radiometers.

7. Characterizing the radiometer not only in terms of NEP, but also in terms of the noise temperature of the noise sources is an important next step in creating a full radiometer system.

8. There are also significant research opportunities for the optimization of millimeter-wave power detectors. The power detector is a heavily non-linear circuit and there is still room for improvement in the understanding of how to design current state-of-the-art power detectors.

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