DESIGN OF A LOW-POWER INTERFACE CIRCUITRY FOR A VESTIBULAR PROSTHESIS SYSTEM

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DESIGN OF A LOW-POWER INTERFACE CIRCUITRY FOR A VESTIBULAR PROSTHESIS SYSTEM

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SUMMARY

The objective of this research is to design and validate a signal processing interface circuitry for a vestibular prosthesis (VP) system.

The human vestibular system is responsible for maintaining balance and orientation, and stabilizing gaze during head motion. Head motion is sensed by vestibular sensors and encoded via the firing rate of vestibular neurons. Vestibular disorders can result in dizziness, imbalance, and disequilibrium. Currently there are no therapeutic options for individuals suffering from bilateral vestibular dysfunction. A potential solution is a vestibular prosthesis (VP). This device serves to replace peripheral vestibular organs by sensing angular motion, detected by semicircular canals (SCCs), and linear head motion, detected by the otolith, and selectively stimulating the corresponding vestibular afferents. An ideal VP will not only mimic the patient-dependent vestibular neural dynamics, but also consume low power.

In this study, three energy-efficient ways to implement the motion encoding function required in a vestibular prosthesis are presented: (1) signal processing circuit implementation on an experimental field-programmable analog array (FPAA), (2) a fully-custom design of signal processing circuitry that extensively makes use of subthreshold analog signal processing techniques, and (3) signal processing functions implementation on an ultra-low power microcontroller. This way, both analog and digital signal processing techniques to implement the vestibular signal processing functions are investigated.

CHAPTER 1

INTRODUCTION

In human body, the vestibular system is responsible for helping the body to keep balance, to have a perception of orientation, and to stabilize the vision during head movements [1]. Using motion sensors that constitute the peripheral vestibular organs, the vestibular system detects angular velocities and linear accelerations. Vestibular afferents provide the detected motion information to the vestibular nuclear (VN) complex where not only vestibular but also related information such as visual or somatosensory information are gathered. The vestibular and vestibular related information are processed at the VN to give rise to vestibuloocular (VOR) or vestibulospinal reflex pathways as well as pathways to the central nervous system (CNS). The VOR causes the eyes to move in a direction opposite to the direction of head motion, which stabilizes images on the retina. The vestibulospinal reflex provides information to the limb and head muscles to maintain the posture and balance. The CNS uses cues from the VN to interpret the body orientation.

The motion sensors of the body are located inside the inner ear and the information from the sensors is transmitted to the VN along the cochleovestibular nerve. The vestibular sensors, which are a series of tubes and sacs, form the membranous vestibular labyrinth. The angular rotations are sensed by the semicircular canals (SCCs). In each ear, there are three SCCs that are located (almost) orthogonal to each other. The transducer cells located in the SCCs encode the angular velocity information into the firing rate of the vestibular neurons. The linear accelerations are sensed by the otolith organs, namely the saccule and the utricle. While the saccule is sensitive to up and down movements, the utricle is sensitive to horizontal movements. In both the SCCs and the otolith organs, conversion of motion to vestibular neuron firing is done by the transducer cells, namely the hair cells.

Disorders that affect the vestibular labyrinth result in dizziness, imbalance, and disequilibrium. Research based on data collected from more than 5000 individuals between

the years 2001 and 2004 reveals that 35.4% of the participants aged 40 and older had vestibular dysfunction, which corresponds to 69 million Americans [2]. In patients over the age of 65 years, these problems often result in falls which may cause fatal or non-fatal injuries. When the vestibular dysfunction is in one ear (unilateral), vestibular rehabilitation therapy can help a patient reduce imbalance and dizziness [3]. However, for bilateral vestibular dysfunction, there are not any therapeutic options. Bilateral vestibular dysfunction may occur primarily due to ototoxic drugs, trauma, or infection that inhibits the functioning of the peripheral vestibular organs. It is estimated that there are 50,000 individuals in the U.S. that would benefit from bilateral vestibular dysfunction treatment [4].

A treatment option that would increase the quality of life for individuals suffering from bilateral vestibular dysfunction is an implantable prosthesis. Such a device would replace the functions of the peripheral vestibular organs by sensing angular and linear head motions and selectively stimulating the corresponding vestibular afferents. In this dissertation I describe my doctoral research toward building a state-of-the-art signal processing circuitry for a VP system that can be used in vestibular studies on animals and for ultimate use in human patients having bilateral vestibular dysfunction.

This document begins by describing the biological properties of the peripheral vestibular organs, namely the SCCs and the otolith organs. Then, a VP that would replace the functions of the peripheral vestibular organs is presented from a system-level perspective. Chapter 1 is concluded by a review of the state-of-the-art VP systems to summarize the efforts and highlight the major challenges towards building a VP. The necessity for building a state-of-the-art signal processing circuitry for a VP is justified at the end of Chapter 1. Different signal-processing implementations that make use of analog and digital domains are presented in the following sections. In Chapter 2, a Field-Programmable Analog Array (FPAA) implementation of a neural stimulator and part of the signal processing functions that process signals in the analog domain is presented. In

Chapter 3, a full-custom design VP signal processing circuit that utilize energy-efficient analog-signal processing techniques is presented. In Chapter 4, a digital domain implementation of the VP signal processing functions on an existing commercial solution is presented. Lastly, in Chapter 5, conclusion of the study and the future directions are discussed.

1.1 Peripheral Vestibular Organs

The vestibular organs are grouped into two categories based on the types of motions they detect; the SCCs and the otolith organs. Angular motions are sensed by the three SCCs, namely horizontal, posterior, and anterior canals. Linear motions are sensed by the two otolith organs, namely the saccule and the utricle. Macromechanics; the transducer cell (hair cell) properties; neuron types, dynamics, and firing rate encodings; and directional properties corresponding to the SCCs and the otoliths are presented below.

1.1.1 SCCs

In a human body, inside each ear, there are three SCCs positioned (almost) mutually orthagonal to each other as shown in Figure 1(a). SCCs in one ear work complementarily with those in the other ear forming a pair of SCCs. This way, the common mode rejection ratio of the sensory information increases.

1.1.1.1. Canal Macromechanics

An SCC is essentially a circular canal that is filled with a fluid called endolymph. The three SCCs have curvature radii of 3.17±0.21 mm, and the lumen of the canal has an elliptic cross section [5]. The region of the canal where the cross section widens to a bulb shape is called the ampulla (Figure 1(b)). A jelly-like structure called the cupula, which resides at the ampulla, divides the circular canal into two sections. When the SCC rotates, the endolymph moves at a slower speed relative to the canal walls causing the cupula to experience a deflection in the opposite direction of rotation. In fact, studies of the cupula

suggest that for the mid-range frequency band that defines the normal head movements, the cupula is attached along the ampullary wall at its entire perimeter and deforms like a diaphragm [6].

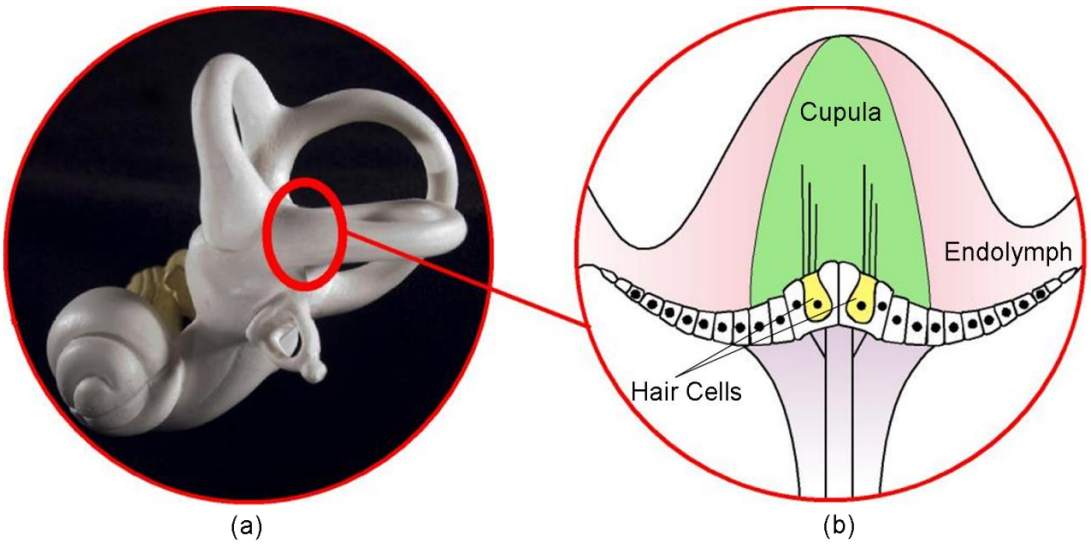


Figure 1. Semicircular Canal (SCC) Structure (a) Three SCCs are (almost) orthogonal to each other. (b) Cross sectional view of the ampulla. The hair cell hairs are embedded inside a jelly-like structure, namely the cupula. The cupula occludes the canal which is filled with a fluid, endolymph.

1.1.1.2. Canal Hair Cell and Afferent Properties

The end of the cupula that is fixed at the ampulla is populated with sensory cells, namely hair cells. The hair cells are the transducer cells of the vestibular organs. A series of biochemical reactions inside the hair cells cause the innervating afferents to fire. If hair cell cilia are deflected, depending on the direction and the magnitude of inclination, the chemical reaction rate increases or decreases. Hair cell cilia are embedded inside the cupula. Thus, the cilia of a hair cell deflect in response to motion, modulating the afferent firing rate. It is known that under no motion vestibular neurons fire at a constant rate, namely baseline rate, which is ~60 spikes/s. Increasing angular velocity, depending on its direction of rotation, increases (excitatory rotation) or decreases (inhibitory rotation) the neuron firing rate. Because the dynamic range for firing rate in response to inhibitory

stimuli (from ~15 spike.s^{-1} to ~60 spike.s^{-1}) is smaller compared to that in response to excitatory stimuli (from ~60 spike.s^{-1} to ~350 spike.s^{-1}), there is an asymmetry between the excitatory and inhibitory responses. Furthermore, although the gain remains almost constant for a range of excitatory input angular velocities, when the angular velocity is increased further, the gain decreases, causing saturation of the angular velocity-firing rate curve for large excitatory and inhibitory angular velocities. The asymmetry and the saturation effects result in an asymmetric sigmoid firing rate-angular velocity relationship. Rough representations of the firing rate vs. head velocity relationships observed in chinchillas for various gain values have been shown in Figure 2 [7].

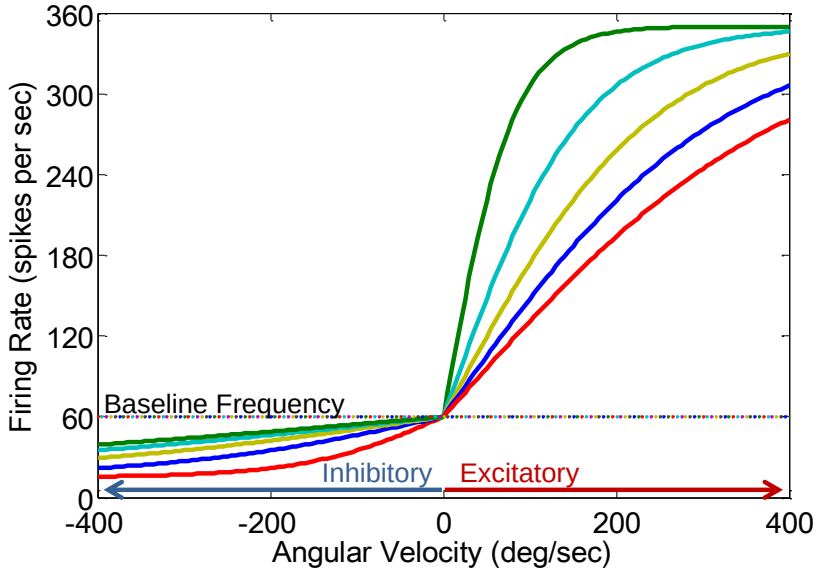


Figure 2. SCC afferents firing rate-angular velocity. Curves having different gains are plotted.

The afferent SCC dynamics are best described by the following transfer function [7]:

$$H_{SCC}(s) = A_V \left(\frac{\tau_1 s}{(1+\tau_1 s)(1+\tau_2 s)} \right) \left(\frac{\tau_A s}{1+\tau_A s} \right), \qquad (1)$$

where τ_1 and τ_2 are the long and the short time constants associated with the band-pass characteristics of the SCC mechanical model, respectively. In (1), A_v is the gain in spike.s^{-1}/deg.s^{-1} at a mid-band frequency of 0.2 Hz and τ_A is the time constant associated with the adaptation of the afferents for small frequency inputs.[1] The gain plot corresponding to (1) is shown in Figure 3.

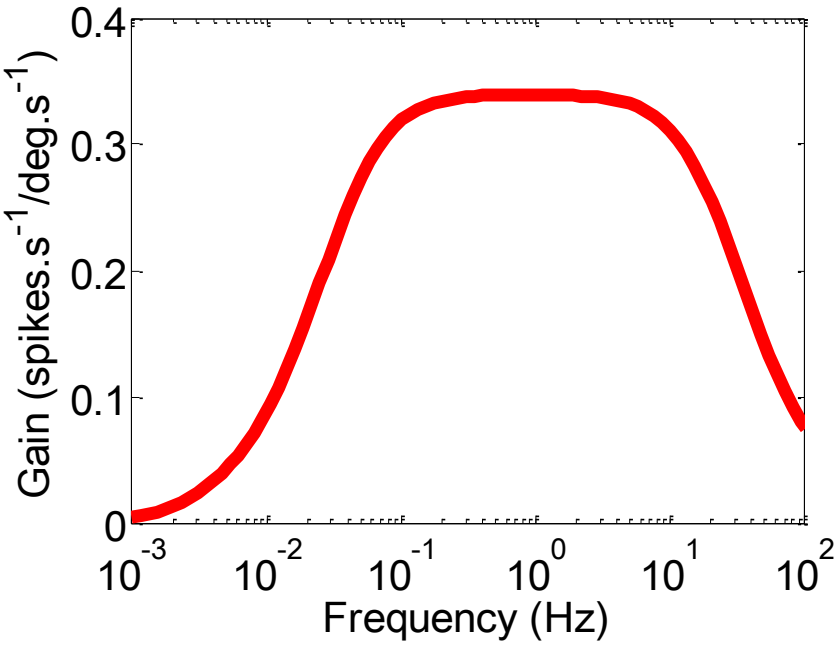


Figure 3. Frequency response of SCC afferents. The plot is drawn based on (1). Typical values of A_V, τ_1, τ_2, τ_A are 0.34 spikes.s^{-1}/deg.s^{-1}, 4.37 s, 7 ms, and 80 s, respectively.

1.1.1.3. Canal Directional Properties

Historically, it has been assumed that 3D angular movements are resolved into three separate vector components and each component is carried to the VN by the afferents of one SCC. Thus, rotation about one of these three vector components is expected to excite afferents of a single canal. However, more recent studies to predict the directions about

[1] Adaptation is defined as the reduction in neuron firing rates during prolonged stimulation [1].

which the vestibular labyrinth resolves 3D angular movements into separate vector components, have revealed that the rotations about the directions normal to the anatomical planes of the canals do not give maximum responses [8],[9]. This is partly because the cross-section area of the canal is not fixed everywhere on the canal, and partly because of the interdependence of canal responses due to the same single mass fluid flowing inside all three-canals. These directions about which maximum responses occur are called the maximum response directions. Since rotations about the maximum response directions also result in afferent activation in the other canals, the maximum response directions cannot be the separate vector components that 3D angular movements are resolved into. Thus, a set of different directions, namely prime directions, were suggested to represent the canal orientations. Figure 4 shows the three prime directions ($\mathbf{n_H}$, $\mathbf{n_A}$, and $\mathbf{n_P}$) corresponding to each of the three SCCs. Prime direction for one canal is obtained by intersecting the maximum response planes of the other two canals. Thus, rotation about the prime direction of one canal results in zero responses in the other two canals.

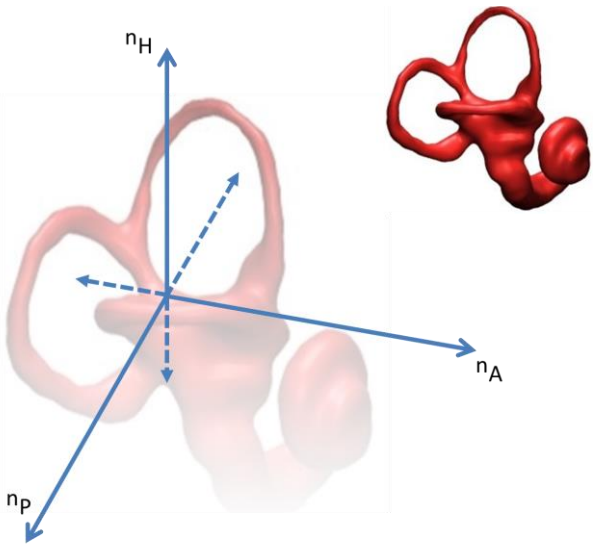


Figure 4. The prime directions ($\mathbf{n_H}$, $\mathbf{n_A}$, and $\mathbf{n_P}$) corresponding to the horizontal, anterior, and posterior canals. The labyrinth image is adapted from [10].

1.1.2. Otolith Organs

There are two otolith organs that sense linear accelerations in the vestibular labyrinth, namely the saccule and the utricle. The saccule and the utricle senses vertical and horizontal accelerations, respectively.

1.1.2.1. Otolith Mechanics

The otoconial membrane is a flat jelly-like structure that covers the neural tissue of the otolith organs. Three layers constitute the otoconial membrane: the otoconial layer, the gelatinous layer, and the columnar layer (Figure 5) [1].

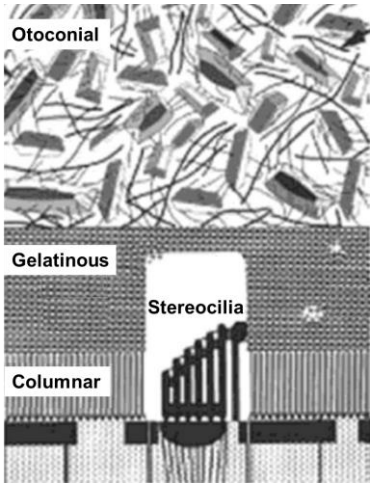


Figure 5. The otoconial membrane [1].

The otoconial layer is occupied with calcium carbonate crystals in the form of a loose fiber network. Beneath the otoconial layer is the gelatinous layer, which is a dense and cross-linked filamentous network. Linear forces, which displace the otoconial layer, are coupled to the columnar layer by the gelatinous layer. Shearing displacements of the columnar layer result in displacements in the stereocilia of the hair cells.

1.1.2.2. Otolith Hair Cell and Afferent Properties

The anisotropic structure of the columnar layer causes the cilia of the hair cells bend in response to shear motion only. Similar to the hair cell operation in SCCs, bending of the cilia controls the rate of a series of biochemical reactions inside the cell that cause firing of the innervating afferents. Depending on the bending of the cilia, the rate of the chemical reactions increase or decrease, which in turn modulates the firing rate of the action potential train carried to the vestibular nucleus (VN) by the afferents. Similar to the canal afferents, the firing rate-acceleration dependence of the otolith afferents is a sigmoid function. Figure 6 shows firing rate-linear acceleration relationships of six otolith afferent neurons. Each plot illustrates a different kind of variation observed among afferents, namely the position on the horizontal axis (a), dynamic range of the discharge rate (b), and linear-region gains (c).

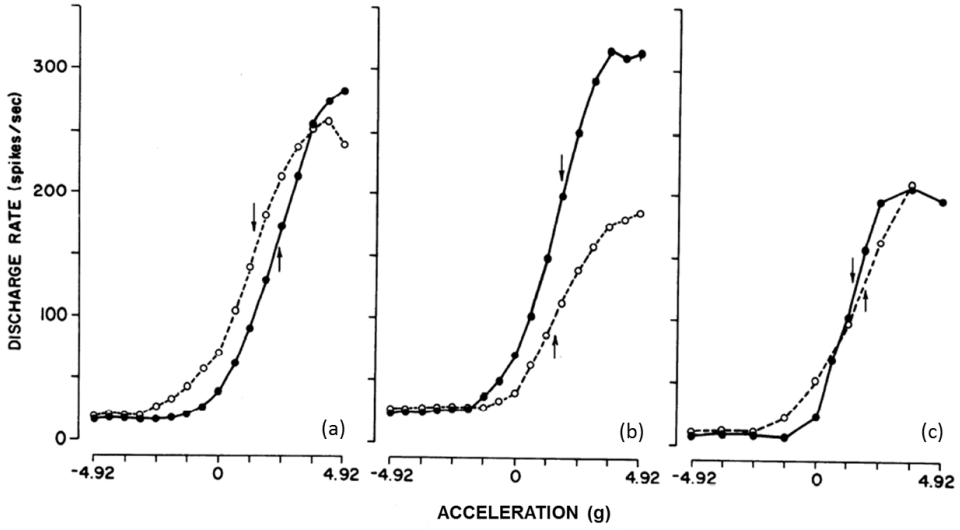


Figure 6. Otolith afferents firing rate-linear acceleration ([11]). The input acceleration is in units of *g*, the gravitational acceleration. Each pair of curves in each plot are used to signify the variation of different curve properties seen in the otolith afferent. These properties are (a) the location of the curve along the x-axis, (b) the dynamic range of the discharge rate, and (c) the gain in the linear region.

The otolith afferent dynamics are best described by the following transfer function [12]:

$$H_{oto}(s) = A_v\left(\frac{1+k_A\tau_A s}{1+\tau_A s}\right)\left(\frac{1}{1+\tau_M s}\right), \quad (2)$$

where τ_A and τ_M are the adaptation and mechanical related time constants, respectively. In (2), A_v is the gain in spike.s^{-1}/g at a mid-band frequency of 0.2 Hz, where g is the gravitational acceleration. The gain plot corresponding to (2) is shown in Figure 7.

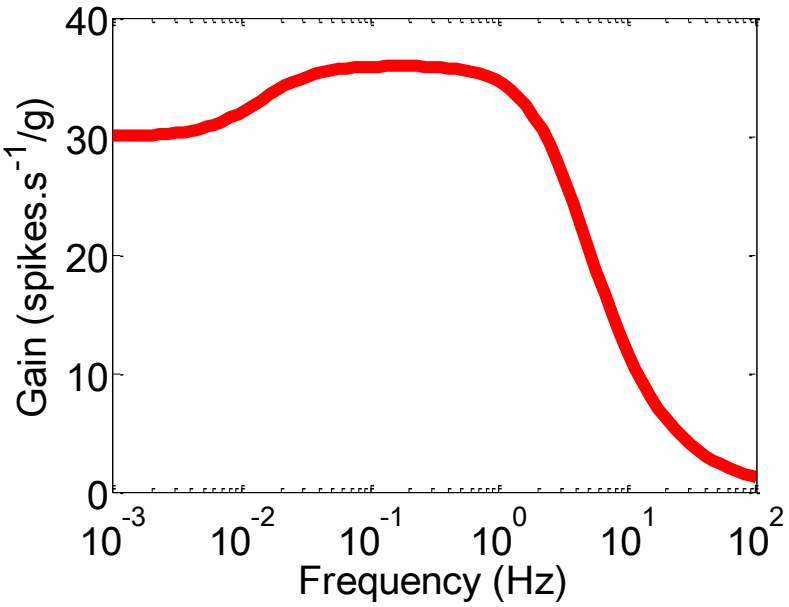


Figure 7. Frequency response of otolith afferents. The plots are drawn based on (2). Typical values for A_V, κ_A, τ_A, and τ_M are 30 spike.s^{-1}/g, 1.2, 11 s, and 46 ms, respectively.

1.1.2.3. Otolith Directional Properties

Each hair cell in the otolith organs has a polarization direction. While deflections in the polarization direction increases the afferent discharge rate, those in the opposite of the polarization direction decreases the discharge rate. The otolith directional properties were determined by understanding both how the otoconial membrane of each otolith organ is oriented in the head and how the polarization directions of the hair cells inside an otolith organ are distributed. Studies reveal that while the utricle provides a two-dimensional

representation of linear accelerations in the horizontal plane, the saccule provides the vertical acceleration information.

Below, the functions of a VP that could replace the aforementioned vestibular organ functions is described. Then an overview of the state-of-the-art VP systems is presented.

1.2 A System-Level Description of a VP

In designing a VP, it is aimed to replace the functions of the peripheral vestibular organs. Therefore, the VP needs to sense angular and linear head motions and selectively stimulate the corresponding vestibular neurons. An analogy between the natural vestibular system and the VP is illustrated in Figure 8.

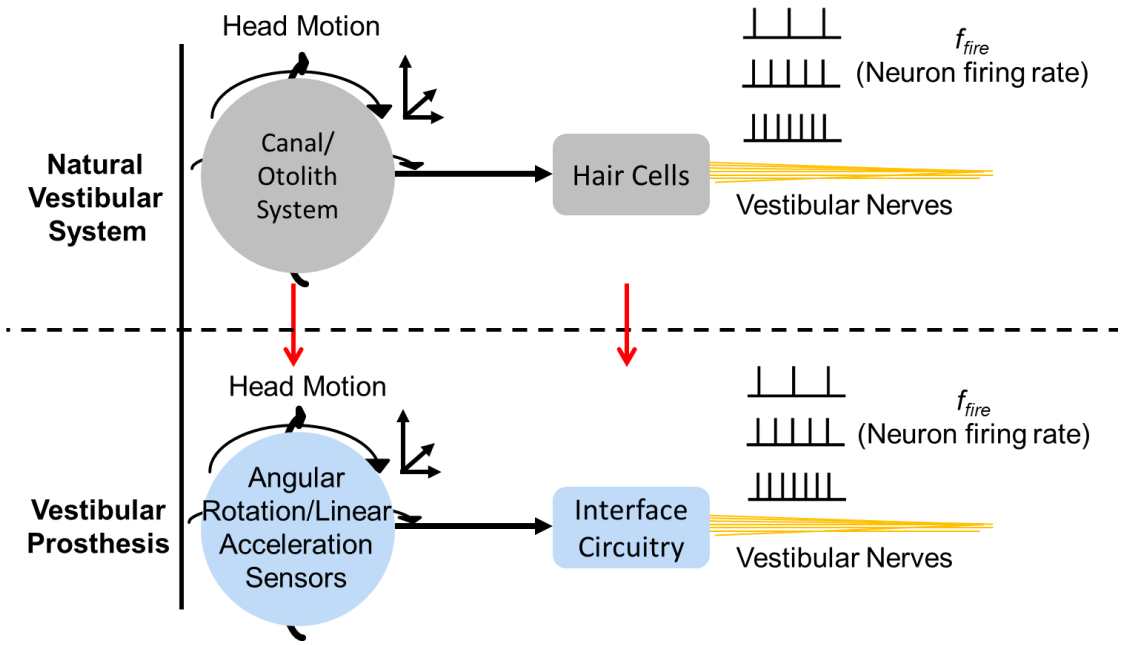


Figure 8. A vestibular prosthesis needs to replace the vestibular organ functions. Canal/otolith system and the hair cells are replaced with rate sensors and an interface circuitry, respectively.

3D angular and linear head motions need to be sensed by rate sensors. Interface circuitry is needed to encode head motion information measured by the sensors into current

pulse rates and stimulate the vestibular neurons. A block diagram of the interface circuitry is shown in Figure 9.

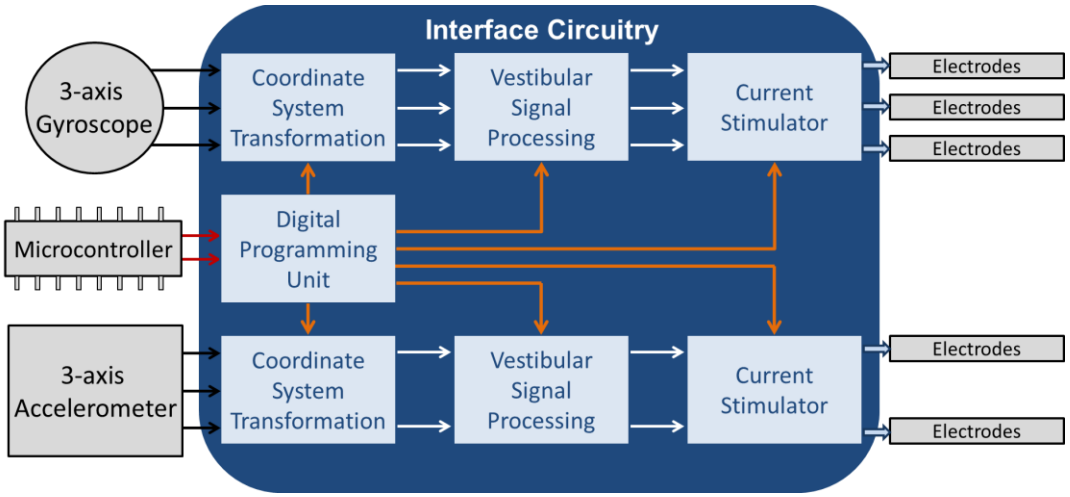


Figure 9. The interface circuitry block diagram.

The interface circuitry needs to perform a coordinate system transformation for two reasons. One is to align the primary axes of angular and linear rate sensors with the SCC and otolith alignments. This way, the implantation operation time is reduced thereby reducing the risks and the costs of the operation. The other reason is related to current spread at the stimulation sites. Small distances between adjacent canals/otolith organs (~ 6 μm) cause stimulation current targeted for a particular canal/otolith to excite another canal/otolith, thereby creating erroneous representation of head motion. The coordinate system transformation can be used to implement a precompensation strategy to reduce erroneous representation of head motion due to current spread.

The vestibular signal processing block is needed to implement the canal/otolith dynamics as well as the firing rate encoding observed at the vestibular neurons.

Lastly, the interface circuitry needs to stimulate the vestibular neurons. Based on clinical studies, current stimulation is proven to be successful for a VP [1]. The charge accumulation at the tissue site during electrical stimulation is harmful for the tissue in the long-term [13]. To prevent long-term harms in the tissue, electrical neuro-stimulators use

biphasic waveforms to initiate action potential at the neurons (Figure 10(a)). The first (cathodic) phase initiates the action potential, and the second (anodic) phase takes back the charge delivered to the tissue during the cathodic phase.

An H-bridge circuitry can be used to generate biphasic current pulses (Figure 10(b)) [14]. The current through a stimulation electrode is controlled by four switches that are controlled by two clocks in pairs. This way, the current flow direction across the electrode is switched. Pulse widths of the clocks Φ_1 and Φ_2 determine the phase durations of the biphasic waveform. The phase difference between the clocks determine the interphase gap, IPG, of the two phases.

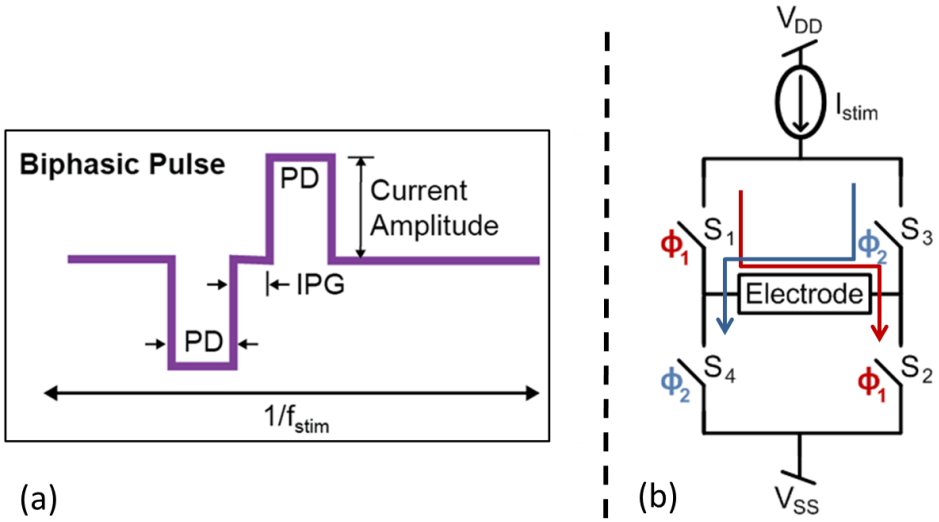


Figure 10. Biphasic waveform is used to in electrical stimulators to prevent harmful electrochemical processes at the tissue sites. (a) Biphasic current pulse. The cathodic phase is followed by an anodic phase. The two phases are separated by an interphase gap (IPG) to ensure the neuron firing. (b) Biphasic current pulses can be generated across an electrode by an H-bridge circuit. Four switches are operated in pairs to switch the flow direction of the stimulation current across the electrode.

Most parameters of the aforementioned functions are patient-dependent. For instance, the general characteristics of the neural dynamics presented in Figures 3 and 7 are fixed. However, the exact locations of the poles/zeros not only vary from neuron to neuron but also from patient to patient. Similarly, firing rate values as well as current phase-widths are needed to be set to optimum values that create the stimuli that best represent the head motions in a particular patient.

To quantify the efficiency of the stimuli, the vestibular system provides an easily accessible and reliable path, namely vestibuloocular reflex (VOR). When the head is moved in one direction, the VOR moves the eye pupils in the opposite direction at the same speed to obtain a stable vision. Therefore in clinical studies, the efficiency of the stimuli delivered to vestibular neurons is assessed by monitoring the motions of the eye pupils of the subject. One of the methods that monitors eye pupil motions uses a camera to track markers that are affixed to the eyes of the subject [15]. The patient-dependent parameter values that move the eye pupils in the right directions at the correct magnitudes are the optimal values for that particular patient. After the implantation operation, the characterization of the implanted VP can be performed by monitoring the eye pupil motions in response to a series of stimuli. Based on the matrix that relates the stimuli to responses, a new matrix that would correct the sensor orientations as well as minimize the erroneous stimuli due to current spread could be obtained [16]. In practice this could be accomplished via a programming unit whereby all needed patient-dependent parameters can be programmed onto the interface circuitry.

A representation of an implanted VP system is shown in Figure 11. Besides the blocks shown in Figure 9, the complete system needs to have a wireless link to perform data and power transfer between the external and the implanted units.

1.3 State-of-the-art VP Systems

To formulate a baseline for existing VP systems, I investigated the four research groups/projects building VP systems; which are the Johns Hopkins University Group, University of Cyprus-Imperial College Group, Closed-Loop Neural Prosthesis for Vestibular Disorders (CLONS) Project, and the UC Irvine Group. In Table 1, the state-of-the-art VP systems are summarized. In the following subsections each VP system is assessed with respect to technology, function, physical dimensions and power consumption.

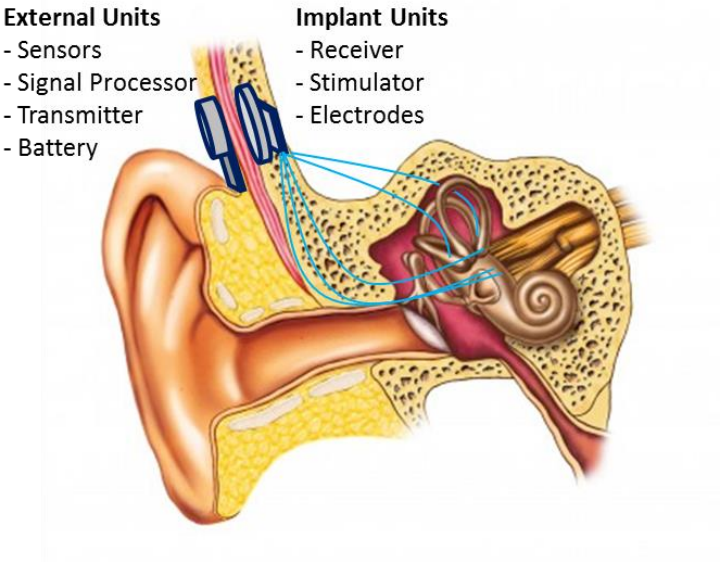


Figure 11. A representation of an implanted VP system.

Table 1. State-of-the-art Vestibular Prostheses Circuitry

Group/Project	Technology	Functions			Area	Power
Johns Hopkins University	PCB with off-the-shelf components	3 Canals Multipolar	Coordinate System Transformation	8 current sources	841 mm^2	Circuitry: ~5 mW (estimated)
University of Cyprus/ Imperial College	ASIC (AMS 0.35µm)	3 Canals+ 2 Otolith Bipolar	NO Coordinate System Transformation	3 current sources	6 mm^2	Circuitry: ~120 µW
CLONS	ASIC (X-Fab 0.6 µm HV CMOS)	3 Canals Bipolar	Coordinate System Transformation	3 current sources	2.27 mm^2	Circuitry: 1.1 mW
Data for the CLONS Project correspond to per one canal stimulator. The signal processor of the CLONS Project has not been reported yet.						

1.3.1 The Johns Hopkins University Group

The VP system developed by this group restores SCC functions to create a normal 3D angular-VOR (aVOR) [17]. The device includes gyroscopes to detect angular velocities and MEMS linear accelerometers to detect linear accelerations. Yet, this system has been reported to process only the outputs of the gyroscopes. For electrical stimulation, the device contains four pairs of current sources that can be used as current sinks and sources. Thus, it allows implementation of simultaneous multipolar neural stimulation techniques. These

techniques are usually used to perform focused stimulation of afferents when different types of afferents are located within a small region as in the case of the vestibular afferents. The inputs from the three gyroscopes are also processed to reduce the misalignment caused by current spread at the stimulation sites. Use of a microcontroller as the signal processing unit provides the device with the capability of implementing different signal processing schemes to the sensor output signals. To do *in-vivo* measurements of electrode impedances, the system also includes an instrumentation amplifier that takes as inputs the potentials of any electrode pairs, amplifies the differential voltage, and outputs to the microelectrode. Through the microcontroller, the device interfaces with an external computer for data analysis.

Despite its capabilities, this VP system is simply integration of off-the-shelf components on a PCB. Thus, in terms of device size (29 mm x 29 mm x 5 mm) the device requires significant scaling and integration to approach the space needed for implantation. Furthermore, although low-power microcontroller and sensors have been used in the system, the power consumption is significantly high for a battery-powered implant. It was reported that the sensor power consumption (~45 mW for triaxial sensing) dominates the total power consumption of the system. Thus, this device is more suitable for animal studies rather than use as an implant.

1.3.2 University of Cyprus-Imperial College Group

Similar to the Johns Hopkins Group, the system developed by this group also aims to sense angular and linear motions, process the signals from the sensors, and provide artificial stimulus to the afferents of three SCCs and two otolith organs [14], [18-20]. MEMS sensors are used in the system to sense motion in six degrees of freedom (three angular, three linear). Unlike the Johns Hopkins system, the signal processor and the stimulation circuitry have been developed as an application-specific integrated circuit (ASIC). The circuitry interfaces to either a custom-design or an off-the-shelf

accelerometer. However, it can only interface to an off-the-shelf gyroscope. The sensor outputs are fed to the otolith and the SCC processors, which are implemented as inherently tunable switched capacitor filters. The current stimulator has five current sources, which can only be used in bipolar stimulation configuration [14]. The current magnitudes and the pulse widths of each of the five sources can be controlled independently. Patient-dependent parameters that vary the filter cut-off frequencies are programmed onto the device using a microcontroller. Of the circuit blocks constituting this VP system, only the tilt-processing circuitry that is used to estimate the tilt angle using an accelerometer [18] and the current stimulator circuitry [14] have been fabricated and tested separately.

This system meets the minimum requirements expected from a VP such as sensing 3D motion, processing the signals from the sensors to match the afferent dynamics, and stimulating the afferents. The reported power consumption values are 48.84 µW, 4.963 µW, and ~65.6 µW for the SCC signal processor, the Tilt-processing unit, and (static power consumption of) the Current Stimulator, respectively. The footprint of the system is 3mm x 2mm. Yet, there are two deficiencies of this system that affect the performance of the device as an implant. One of them is that the system does not allow reduction of axis misalignment due to current spread. The other is that the system does not allow correction of discrepancies between the orientations of the implanted sensors and the SCCs after the implantation process.

1.3.3 Closed-Loop Neural Prosthesis for Vestibular Disorders (CLONS) Project

This project, which is conducted by a consortium of eight partners, is based upon the early work of a major partner, D. Merfeld, the inventor of the first VP [21]. Unlike the first VP device, the CLONS project aims to restore vestibular information by electrically stimulating all three SCC afferents. The research steps of this project have been explained in various papers [22-26]. These steps include designing implanted and external components, building systems performing control algorithms, anatomical modeling, and

animal/human experiments. The external components are the gyroscopes and the internal components are the stimulation electrodes [24]. Control algorithms of the system are reported to perform angular velocity-to-firing rate encoding and gyroscope-SCC orientation transformation [23]. The current version of the system built under CLONS project uses an off-the-shelf three-axis gyroscope to sense 3D angular velocity. The stimulator circuitry consists of a management unit and an output stage. The management unit receives command frames from the external signal processor unit and manages the output stage, which is a current DAC. The stimulator can deliver currents to electrodes in bipolar configuration [22]. Since it has been reported that an ASIC is going to be designed, the dimension of the system is expected to be small. On the other hand, a signal processor circuitry has not been designed yet. Thus, it cannot be estimated how close the system will mimic the natural vestibular afferent dynamics.

1.3.4 The UC Irvine Group

The focus of this group was to demonstrate a single-axis gyroscope customized for a vestibular prosthesis [27]. In summary, all the blocks of the system; namely the sensing unit; the signal processing unit, which consists of transfer-function and voltage-to-frequency converter units; and the current stimulation unit are implemented on a PCB. Being an off-the-shelf demonstration, the device was not designed as an implant device. Because off-the-shelf resistors, capacitors, and potentiometers are used, this system does not allow precise tuning of transfer-function or current-pulse related parameters, making the device inconvenient for animal studies. Given the rudimentary nature of the VP interface circuitry, we do not include the UC Irvine Group as state-of-the-art.

As mentioned in the Introduction, a vestibular prosthesis (VP) can be a therapeutic option for those having bilateral vestibular dysfunction. Although there have been four research groups that have built a VP system at different complexities and properties, none of those systems have been implanted in a human patient yet. However, there are two

prosthetic devices that have been implanted in human subjects [28],[29]. Both of these devices are revised versions of commercial cochlear implants. While, the first device is operated by the patient to reduce the deleterious effects of dizziness caused by the Meniere's disease, the second device was used in a case study to see the feasibility of a vestibular implant for humans. Thus, neither of the devices aimed to replace malfunctioning peripheral vestibular organs.

The motivation behind my PhD research is to improve the energy-efficiency of a VP interface circuit. Considering the VP interface circuitry blocks presented in Figure 9, the lower limit for the current stimulator power consumption is limited by the stimulation current and stimulation electrode headroom voltage limitations that are imposed by the vestibular clinical studies. Therefore, the focus in this work is given to designing coordinate system transformation and vestibular signal processing blocks that make use of energy-efficient signal processing techniques. To explore those techniques, part of the vestibular signal processing functions for one SCC were implemented on an experimental field-programmable analog array (FPAA) platform, which is explained in Chapter 2. To investigate the limits of the FPAA as a VP interface circuit platform, a current stimulation circuit on an FPAA is also presented in Chapter 2. Then a custom design solution that meets the small area and the energy-efficiency requirements of an implantable VP system is presented in Chapter 3. The custom design includes coordinate system transformation blocks for three SCCs and two otoliths and vestibular signal processing blocks for two SCCs and one otolith. To compare the custom-design with an existing low-power signal processing system and a promising state-of-the-art VP system developed by the Johns Hopkins Group, a Texas Instruments MSP430 series ultra-low power microcontroller implementation of the VP functions is explained in Section 4.

CHAPTER 2

VESTIBULAR PROSTHESIS SIGNAL PROCESSING ON A FIELD-PROGRAMMABLE ANALOG ARRAY (FPAA) DEVELOPMENT PLATFORM

As mentioned in previous sections, *in-vivo* studies indicate a pressing need for optimizing current stimulation paradigms as well as reducing spurious stimulation. Thus, refining and optimizing encoding of angular velocity, and processing of angular velocity signals, is an essential step to achieving the clinical efficacy of a vestibular prosthesis. To investigate a potential reconfigurable, low-power option for angular velocity encoding, we explored an experimental Field Programmable Analog Array (FPAA) development platform [30].

Accomplished completely in the analog domain, the signal processing circuitry generates a non-linear signal that codes angular velocity into a pulse rate for a single SCC (Figure 12).

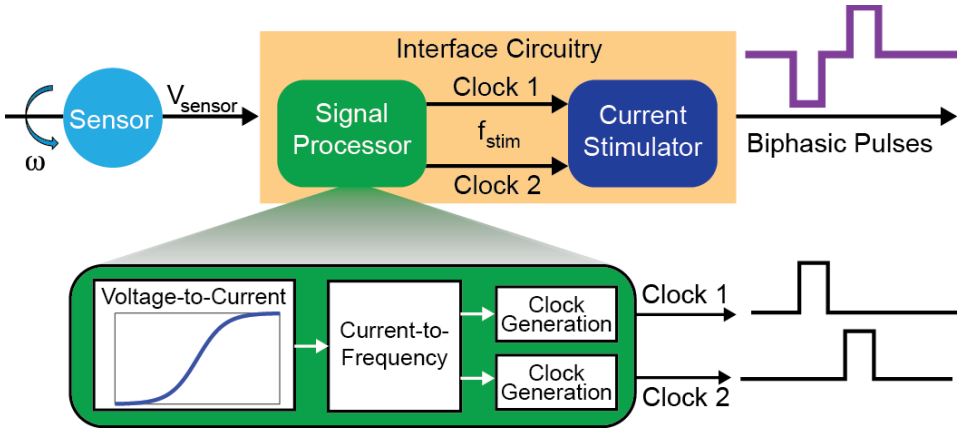


Figure 12. Single Canal Vestibular Prosthesis System Diagram.

Producing two out-of-phase clocks, the circuit can control all of the timing features of a biphasic pulse and ultimately drive a current stimulator for targeted activation of vestibular nerve fibers.

Below, a brief description of the FPAA and the procedure for realizing circuitry on the FPAA is presented.

2.1. FPAA Architecture

The FPAA used is an experimental chip; the Reconfigurable Analog Signal Processor (RASP) 2.8 designed by the Integrated Computational Electronics Laboratory, Georgia Institute of Technology [30]. Although a commercial FPAA could also serve as a development platform [31], we chose the RASP 2.8 since its floating gate architecture provides greater functionality through the ability to program the switches with variable impedance. In addition, by operating the circuitry in weak inversion, considerable power saving can potentially be realized.

Fabricated with the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm 2P3M CMOS process and operating with a 2.4 V power supply, the RASP 2.8 is comprised of computational analog blocks (CABs) and an interconnect network (Figure 13(a)). A total of 32 CABs (CAB1 or CAB2) consist of circuit elements and blocks at different levels of complexity. Circuit elements/blocks such as transconductance amplifiers (OTAs), multi-input floating gates, nFET/pFET transistors, floating capacitors, Gilbert Multipliers, and floating-gate current mirrors are distributed among CAB1 and CAB2 (Figure 13(b)). The role of the interconnect network, which consists of switches (floating-gate pFETs) and interconnect lines, is to sensitize connections between CAB elements/blocks. In addition, global interconnect lines are also connected to input/output pins for voltage/current measurements.

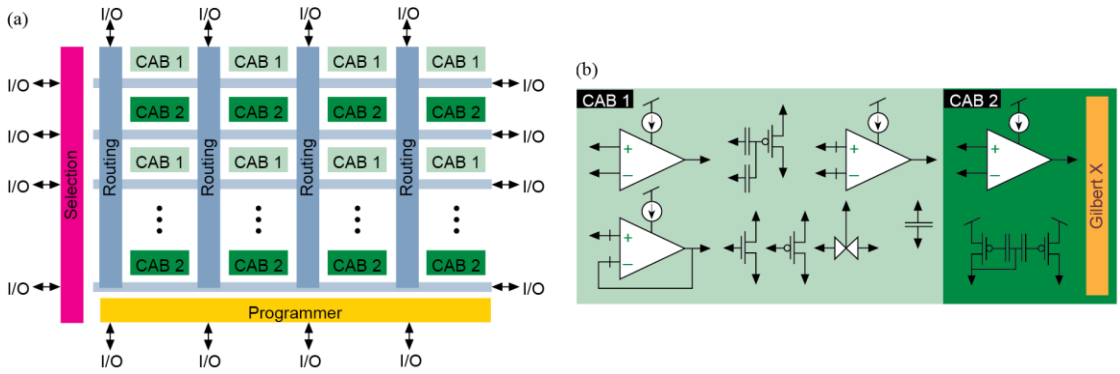


Figure 13. Floating-gate FPAA architecture. (a) The FPAA consists of an 8 x 4 matrix of Computational Analog Blocks (CABs) interconnected through crossbar networks. (b) Circuit elements/blocks are distributed among CAB1 and CAB2.

To implement a particular circuit on the FPAA, connections are made by programming the necessary switches in the interconnect network. An automated placement and routing tool, the Generic Reconfigurable Array Specification and Programming Environment (GRASPER), determines which switches to activate. GRASPER converts a user-generated SPICE netlist describing the circuit into a netlist of switches [30]. To program a floating-gate pFET, negative charge is injected onto the floating-gate of the transistor. The amount of the charge trapped at the floating-gate affects the effective gate potential of the transistor and thus directly controls the conductance of the device. Briefly, the charge injection mechanism is accomplished by applying a high potential difference (~15 V) between the drain and the source terminals. As a result, a programming current, I_{prog}, passes across the two terminals. I_{prog} can be varied between 1 nA-32 µA, with higher I_{prog} causing more negative charge to be trapped at the floating-gate. The communication between the PC and the FPAA is achieved through a microprocessor-based board.

2.1.1. Signal Processor

For each SCC, the encoding of angular velocity into a pulse rate is based on a relationship validated in animal models [32]. This non-linear relationship between the angular velocity and the firing rate is represented as (Figure 10):

$$f_{stim} = 200 + 150 \tanh\left(\frac{\omega}{500/3}\right), \tag{3}$$

where ω is the angular velocity in °/sec, and f_{stim} is the pulse rate in pulses per second (pps). The offset value in the equation conveys a baseline pulse rate corresponding to zero angular velocity.

A biphasic current scheme (Figure 14) is generated to prevent any charge accumulation at the tissue site that can cause long-term adverse effects [33]. The amplitude and pulse duration (PD) of the cathodic pulse determines how much charge is delivered to the neural tissue. Similarly, the PD and the amplitude of the anodic pulse determine how much charge is returned from the tissue. The interphase gap (IPG) separates the two pulse periods to ensure the firing of the neuron. This control is essential for optimizing stimulus waveforms to reduce threshold, improve spatial selectivity, and reduce spurious stimulation.

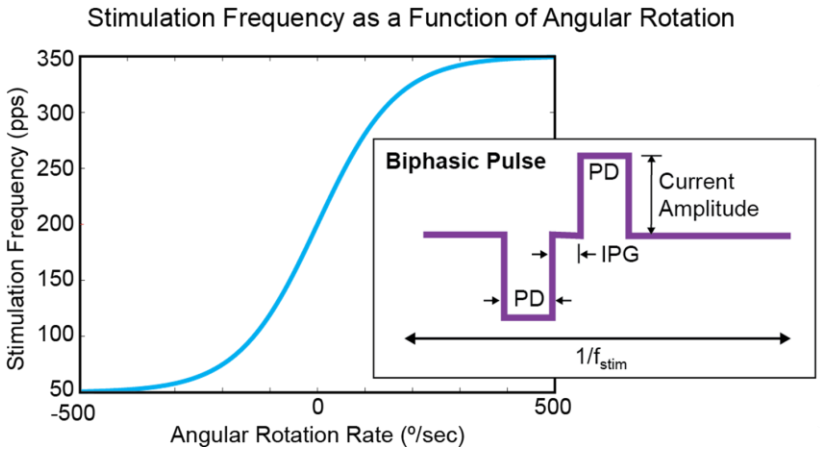


Figure 14. Non-linear relationship between the angular velocity and the firing rate. A representative biphasic pulse is shown inside the graph.

The signal processor provides the user with the freedom to control all timing features of a biphasic current pulse. The signal processor senses an analog voltage output from an inertial sensor, $V_{gyro,out}$, and converts this voltage into two out-of-phase clocks (Clock 1 and Clock 2) each with a frequency of f_{stim}. In turn, Clock 1 and Clock 2 serve as control signals for a stimulator. The respective pulse duration of the two clocks determine

the cathodic and the anodic PD of the biphasic current waveform. The phase difference between Clock 1 and Clock 2, less the PD, determines an IPG. The three blocks constituting the signal processor are the voltage-to-current converter block, the current-to-frequency converter block, and the clock generation block (Figure 15). Each block is described in detail below.

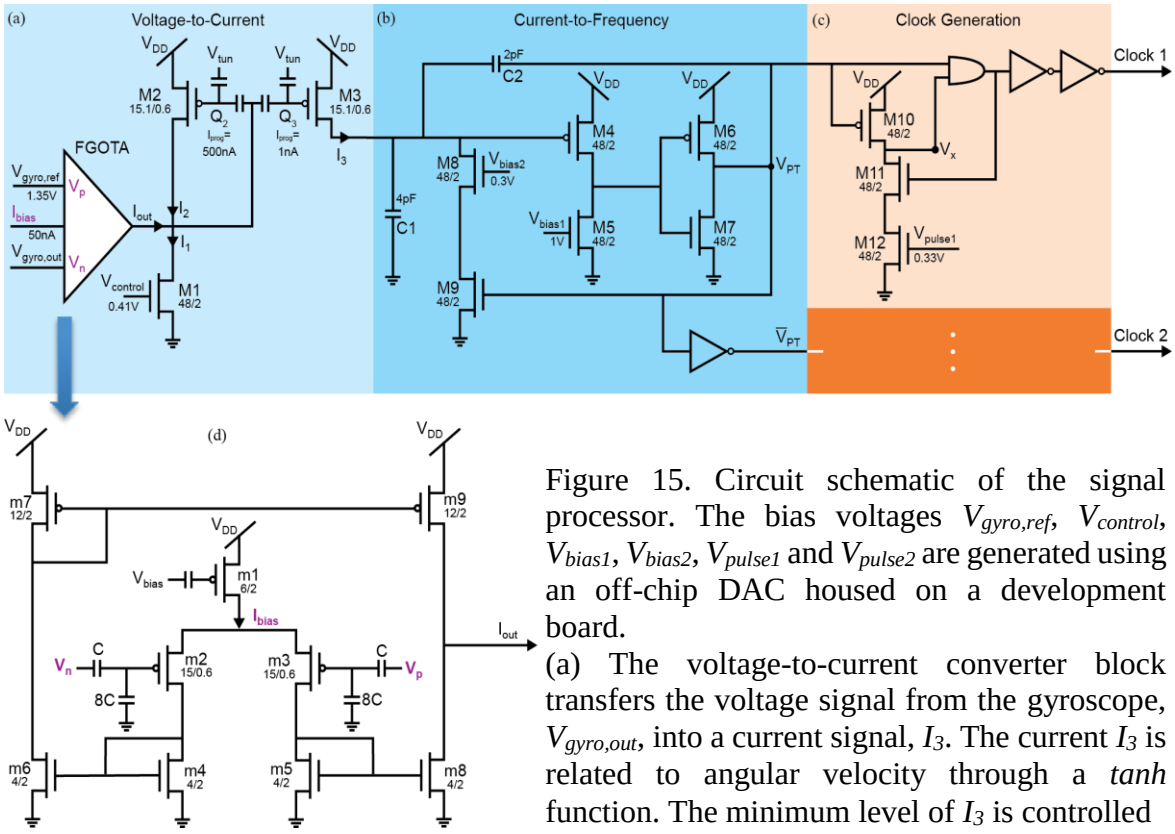


Figure 15. Circuit schematic of the signal processor. The bias voltages $V_{gyro,ref}$, $V_{control}$, V_{bias1}, V_{bias2}, V_{pulse1} and V_{pulse2} are generated using an off-chip DAC housed on a development board.

(a) The voltage-to-current converter block transfers the voltage signal from the gyroscope, $V_{gyro,out}$, into a current signal, I_3. The current I_3 is related to angular velocity through a *tanh* function. The minimum level of I_3 is controlled by $V_{control}$. By adjusting $V_{gyro,ref}$ an offset can be added to $V_{gyro,out}$. This serves to translate the I_3 along the x-axis of the I_3 vs. $V_{gyro,out}$ curve.

(b) The current-to-frequency converter block converts the current signal, I_3, into the pulse train output V_{PT}. Linearly related to I_3, the frequency of V_{PT} determines f_{stim}.

(c) Two similar fully digital Clock Generation stages create Clock 1 and Clock 2. The pulse width of Clock 1 is controlled by V_{pulse1} and a similar relationship exists for Clock 2.

(d) The FGOTA is the core of the voltage-to-current converter block. In the sub-threshold region, the output current, I_{out}, of the FGOTA is related to its differential input voltage, V_p-V_n, through a *tanh* function. I_{bias} is the bias current which determines the region of operation and is set up during the programming stage by V_{bias}.

2.1.1.1. Voltage-to-Current Converter Block

The first block of the Signal Processor transfers the analog voltage output from an inertial sensor, gyroscope, into a current signal (Figure 15(a)). As indicated in (3), the stimulation frequency is related to angular velocity through a hyperbolic tangent function. In the spirit of biomorphic circuit design, we followed an integrate-and-fire neuron scheme utilizing a floating-gate OTA (FGOTA) [34]. In the sub-threshold region, the output current, I_{out}, of the FGOTA is related to its differential input voltage, V_p-V_n, through a *tanh* function:

$$I_{out} = I_{bias} \tanh\left(\frac{\kappa\alpha\left(V_p - V_n\right)}{2U_T} \right), \tag{4}$$

where κ is a constant relating the surface potential of a transistor to its gate voltage, α is the attenuation factor due to the capacitive divider at the input differential pair, I_{bias} is the bias current which determines the region of operation of the transistors, and U_T is the thermal voltage. Thus, an FGOTA is at the core of the voltage-to-current converter block.

In our implementation, $V_{gyro,out}$, the output of the gyroscope, is connected to V_n input of the FGOTA. V_p is tied to $V_{gyro,ref}$, the reference voltage for the gyroscope. To ensure that I_{out} is positive, M1, drawing I_1 from the output node of the FGOTA, adds a DC offset. The current I_1 is controlled by $V_{control}$ and I_2 is the DC shifted version of -I_{out}. To ensure that I_2 maintains f_{stim} within the 50-350 Hz interval, I_2 is scaled and mirrored using a mismatched current mirror circuit. The mirror circuit is formed by two floating-gate pFETs, M2 and M3, thereby creating I_3. Since device sizes are fixed in the FPAA, the mismatch between M2 and M3 is controlled by programming varying amounts of charges (Q2 and Q3) onto their respective floating gates. For the I_{prog} values of M2 and M3 shown in Figure 15, the I_2/I_3 ratio is measured to be ~80. The minimum level of I_3 is controlled by $V_{control}$. By adjusting $V_{gyro,ref}$ an offset can be added to $V_{gyro,out.}$ This serves to translate the I_3 along the x-axis of the I_3 vs. $V_{gyro,out}$ curve.

2.1.1.2. Current-to-Frequency Converter and Clock Generator Blocks

Since these two blocks function in an integrated fashion to provide control signals for a current stimulator, we begin by describing the main signals of interest followed by a detailed description of each block. The main output of the current-to-frequency converter block is V_{PT}, a frequency modulated pulse train with an adjustable pulse-width. Figure 16 depicts the duration that V_{PT} is high and low, t_{high} and t_{low} respectively.

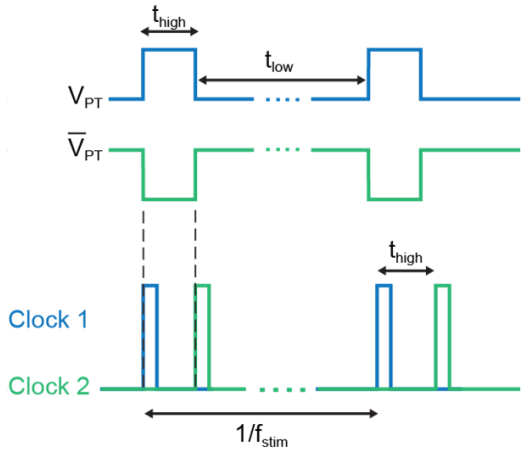


Figure 16. Pulse timing control. The signal V_{PT} is output from the current-to-frequency converter block with a pulse rate of f_{stim}. The rising edge of V_{PT} triggers Clock 1 in the clock generation block. The clock generation block also controls the PD, the duration of each clock. The delay between the clocks, t_{high}, less the PD is the IPG.

The rising edge V_{PT} triggers Clock 1 in the subsequent clock generation block. Similarly, the rising edge of $\bar{V}_{PT}$ triggers Clock 2. As a result, the frequency of V_{PT} determines the pulse rate, f_{stim}. The pulse duration (PD) of the target biphasic pulse is controlled in the clock generation block. The interphase gap (IPG) is determined by the delay between Clock 1 and Clock 2, t_{high}, less the pulse duration (PD).

Current-to-Frequency Converter

The circuit is a modified version of a self-resetting neuron circuit [35] where the main signal of interest is V_{PT}. The bias voltage V_{bias2} controls the discharge current I_8 through M8 and M9 when M9 is on. As a result, V_{bias2} controls t_{high}. Alternatively, t_{low} is affected by I_3 since it controls how fast *C1* (4 pF) and *C2* (2 pF) are charged up. Another

parameter affecting t_{low} is V_{bias1}, as it determines how fast V_{PT} makes the low to high transition. The relationship between f_{stim} and I_3 is:

$$f_{stim} = \frac{1}{t_{high} + t_{low}} = \left(\frac{I_3}{C_2 V_{DD}} \right) \left(1 - \frac{I_3}{I_8} \right). \quad (5)$$

For $t_{low} >> t_{high}$, it can be shown that:

$$f_{stim} \approx \frac{1}{t_{low}} = \left(\frac{I_3}{C_2 V_{DD}} \right). \quad (6)$$

The linear relationship between f_{stim} and I_3 enables I_3 to have the same dependence on angular velocity as f_{stim} expressed in (3). When examining (5) it appears that at high pulse rates the linear assumption may be inaccurate. Consider an f_{stim} of 450 pps and t_{low} = 10(t_{high}). Thus, 200 µs may be dedicated to the PD and IPG of a biphasic pulse. Given that most PDs are 100 – 200 µs and that the IPG does not affect response to electrical stimulation of vestibular nerve fibers [36], it is reasonable to assume that the linearity assumption would not be grossly violated. However if necessary, V_{bias2} may be dynamically controlled through a feedback circuit to maintain a small I_3/I_8 rending the term negligible. As a result the needed linearity can be realized.

Clock Generator Block

Two fully digital clock generation circuits constitute this block generating Clock 1 and Clock 2, each with a frequency of $f_{stim.}$ The goal of each circuit is to create a pulse at the rising edge of its respective input and set the duration of each pulse [37]. To give the two clocks a phase difference, Clock 1 is generated directly from the pulse train obtained at the previous block, V_{PT}. Clock 2 is generated from the inverse of that pulse train, $\bar{V}_{PT}$. When V_{PT} is low, Clock 1 is also low. During that period, M10 keeps V_X high. When V_{PT} makes a low-to-high transition, because M11 allows current flow, a discharge path is created that decreases V_X. During that phase, Clock 1 is at high. When V_X reaches the low value for the AND gate, Clock 1 also goes down to low. At that instant, M11 turns off,

disconnecting the discharge path. The pulse-width of Clock 1 is related to how fast V_X goes down to zero, which is effectively controlled by V_{pulse1}. The circuit for Clock 2 operates similarly and the pulse duration is controlled by V_{pulse2}.

2.1.2 Measurement Results

To observe the pulse rate as a function of angular velocity, the signal processor was driven by a commercial gyroscope. Rotated about its z-axis, the gyroscope exhibited a sensitivity of 2 mV/º/s over a full-scale range of ±500 º/s, with a reference voltage of 1.35 V (InvenSense Inc., Sunnyvale, CA). Using a single-axis rate table (Ideal Aerosmith LLC, Pittsburgh, PA), the gyroscope was subjected to 33 sinusoidal rotations with angular velocity magnitudes that varied between 0 º/sec and 500 º/sec in 15 º/sec increments. Pulse rate data was captured from an oscilloscope and processed using MATLAB software (The MathWorks Inc., Natick, MA) running on a PC. Discrete angular velocities were required since we were limited by the data transfer rate between the oscilloscope and the PC. Approximately 75 data points were obtained for each rotation. To find the pulse rate in the positive direction, the three maximum frequency values were averaged. Similarly, to find the pulse rate in the negative direction, the three minimum frequency values were averaged.

Figure 17 compares the target and experimental f_{stim} vs angular velocity. To better understand the difference between the two curves we consider the three aspects of the curve relating pulse rate to angular velocity; the steepness, the baseline frequency (the frequency corresponding to zero angular velocity in the plane of measurement), and the frequency range.

The steepness of the output curve is controlled by the transconductance of the FGOTA (voltage-to-current converter). To characterize the linearity and the transconductance of the FGOTA, we varied V_{out} from 0–2.4 V. For a bias current of, I_{bias} = 3 nA, the measured linear range for 5% degradation in transconductance of the FGOTA is between 0.31 V and 0.37 V, when V_{out} ranges between 0.27 V and 2.13 V. The data reveals

that the transconductance of the FGOTA is only slightly dependent on V_{out} and is ~3 nS. The transconductance of the FGOTA is mainly dependent on the κ_{eff} (κ*α term in (4)). This is verified by a series of curves illustrating f_{stim} vs angular velocity for a range of κ_{eff} from 0.05 to 0.15 (Figure 17). As expected from (4), the steepness of the curve increases with κ_{eff}. At κ_{eff} = 0.05 the expected curve closely matches the experimental curve. Yet, the κ_{eff} corresponding to the target curve is around 3 times larger than that (~0.15). There are two reasons why the κ_{eff} is bound to small values. First, the κ of a transistor, in the FGOTA, in the weak inversion region is smaller than when in the strong inversion region. Second, the capacitive divider at the floating gates of the FGOTA reduces α to significantly low values, slightly lower than 1/9 considering the gate capacitances of M2 and M3.

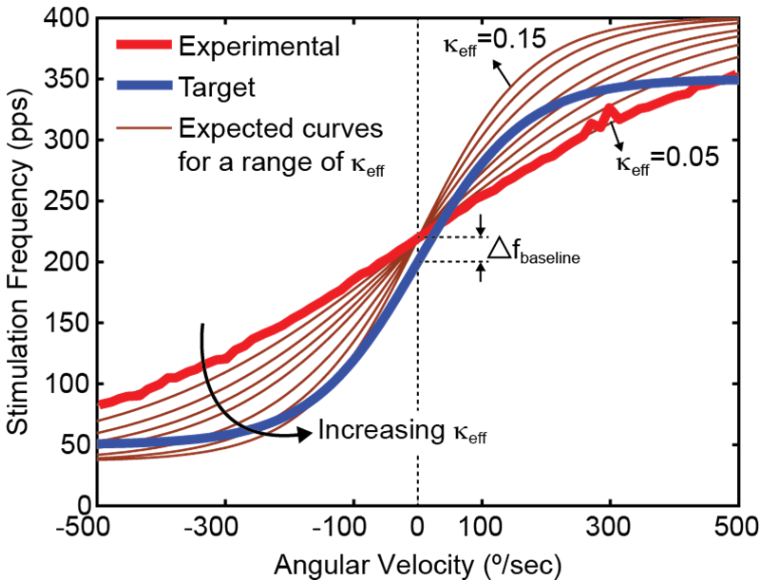


Figure 17. Stimulation frequency vs. angular velocity. The experimental stimulation frequency (pulse rate) as a function of angular velocity is shown. Superimposed on the plot is a a series of curves illustrating f_{stim} vs angular velocity for κ_{eff} (0.05–0.15). The steepness of the curve is controlled by the κ_{eff} of the FGOTA The baseline frequency difference between the experimental and the target curves, $\Delta f_{baseline}$, can be adjusted by decreasing I_1 (controlled by $V_{control}$). To control the stimulation frequency range, the following values can be adjusted: the bias current of the FGOTA, I_{bias} in (4), and the current ratio of the mismatched current mirror, I_3/I_2, and the capacitance $C2$ in (6).

The second aspect is the baseline frequency, $f_{baseline}$. This frequency is effectively controlled by the DC value, I_1, added to I_{out} in Figure 15(a). By changing I_1 (controlled by $V_{control}$), the difference between the baseline frequencies of the two curves ($\Delta f_{baseline}$ = 19.5 pps in Figure 17) can be adjusted.

The last aspect we consider is the frequency range. This is controlled by three factors: the capacitance *C2* in (5), the bias current of the FGOTA, I_{bias}, and the current ratio of the mismatched current mirror, I_3/I_2. By varying any of these, the experimental curve can be adjusted to maintain within the desired stimulation frequency range.

Figure 18 summarizes critical outputs from the signal processor blocks. Figure 18(a) illustrates the non-linear I_3 response to $V_{gyro,out}$ generated by the voltage-to-current converter block. In Figure 18(b) a linear f_{stim} vs. I_3 response is exhibited by the current-to-frequency converter block. And finally, in Figure 18(c) the triggering of Clock 1 by the rising edge of V_{PT} is shown.

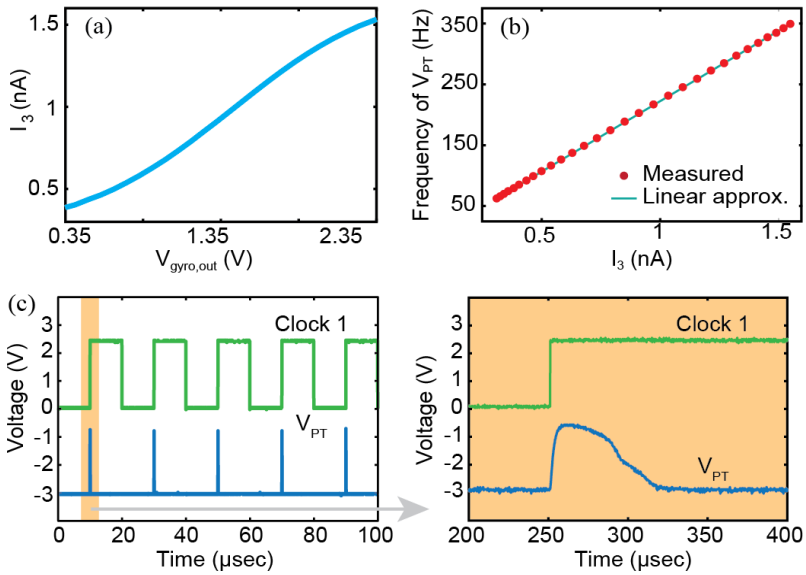


Figure 18. Summary of signal processor block level outputs. (a) Non-linear response to $V_{gyro,out}$ generated by the voltage-to-current conversion block. (b) Linear f_{stim} vs. I_3 response is exhibited by the current-to-frequency conversion block with t_{high} = 200 µs. (c) Triggering of Clock 1 by the rising edge of V_{PT}. Note that a long (10ms) clock pulse was created in the clock generation block to illustrate the relationship between the rising edge of V_{PT} and Clock 1. In practice the pulse duration of Clock 1 would be less than the duration of V_{PT}.

To demonstrate biphasic pulse control a 1 kΩ resistive load was placed across an H-bridge circuit. (Figure 19). Although this is voltage-based stimulation, it served to illustrate the ability of the signal processor to accurately control biphasic pulses ultimately generated by a current stimulator. When connected to a 2.4 V supply, a current level of 100 µA was obtained. Pulse durations of anodic and cathodic phases between 25 – 400 µs, and an interphase gap between 25 – 250 µs were observed. Hence all timing segments of a biphasic pulse can be controlled well within the necessary ranges.

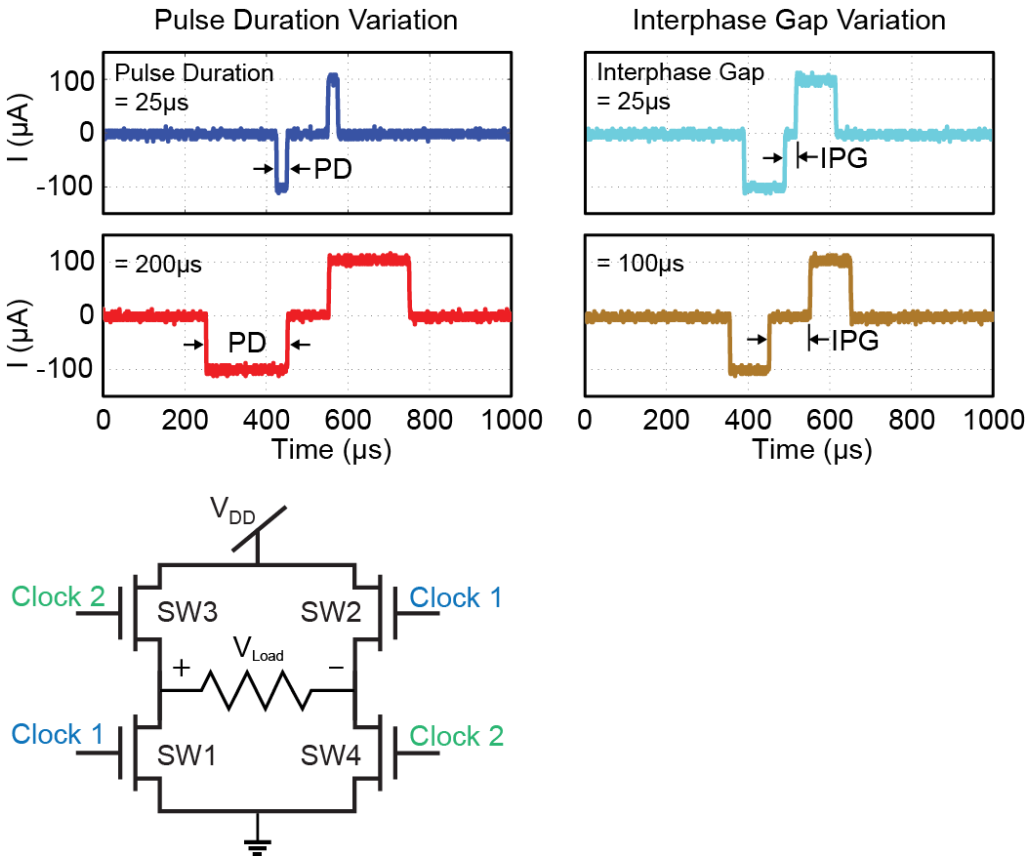


Figure 19. Biphasic pulse control. Using a 1 kΩ resistive load placed across an H-bridge circuit, Clock 1 and Clock 2 serve to control a cathodic-first, symmetric, biphasic pulse. Representative values of the PD and IPG are demonstrated.

To appreciate the power demands of the signal processor circuitry, estimates are reported for a 350 Hz pulse rate with a 100 µsec PD. The voltage-to-current converter block consumes 0.48 µW. The combined dynamic power consumption of the current-to-

frequency converter and the clock generator blocks is ~44 nW when any short circuit or leakage currents is ignored and a line capacitance of 2 pF is assumed [30]. Based on simulations the static power consumption of the current-to-frequency block is estimated as 45 µW. The necessary switch circuitry consumes an additional 16.8 µW resulting in 62 µW. The use of a 14-bit AD5380 DAC (Analog Devices, Inc., Norwood, MA) for setting the six bias voltages consumes 12 mW max. Although the off-chip DAC facilitated circuit prototyping, in practice such bias voltages would be generated on the FPAA. Schlottmann and Hasler illustrate a method for creating voltage references through trapping different amount of charges at the floating gates of a FGOTA [38]. Precisely controllable (<±1 mV) bias voltages from rail-to-rail (0 - 2.4V) can be generated and will consume very little power, on the order of µW.

2.1.3 Neural Stimulator

A stimulator circuit is implemented to explore voltage/current limits of the FPAA for a VP application. In review, the stimulator specifications were based on ongoing experiments in animal models revealing currents ranging from 10-500 µA in amplitude, 100-200 µsec per phase, and 50-250 Hz in rate [36],[39]. Although the lower bound on current resolution has yet to be determined, cochlear stimulators were used as the gold standard where levels are programmable in increments of two percent.

To implement the current sources, a core current source circuit using a bootstrap voltage reference circuit was designed and tested (Figure 20). This topology was selected for its insensitivity to temperature changes and other environmental effects [40].

Two matched nFETs, M3 and M4, form a current mirror. The current passing through M1 and M2 are equal. Unlike a conventional bootstrap circuit where V_{ref} is generated by setting the size of M1 larger than M2, programming the gates of M1 and M2 at different charge levels, Q1 and Q2, generates V_{ref}. Assuming a perfect match between M1 and M2, V_{ref} is directly proportional to the charge difference $\Delta Q=Q_1-Q_2$. Additional

floating-gate pFETs connected to the circuit (Mcur1-McurN in Figure 20(a)) reflect the current generated inside the core circuit to an outside pin. The charge level (Q_3) programmed onto the gates of Mcur1-McurN changes the respective effective gate voltages, thus I_1 is dependent on Q_3. In summary, the current I_1 is dependent on both DQ and Q_3. Multiple current branches can boost the current level with N copies. A total of two CABs are required to realize the core circuit.

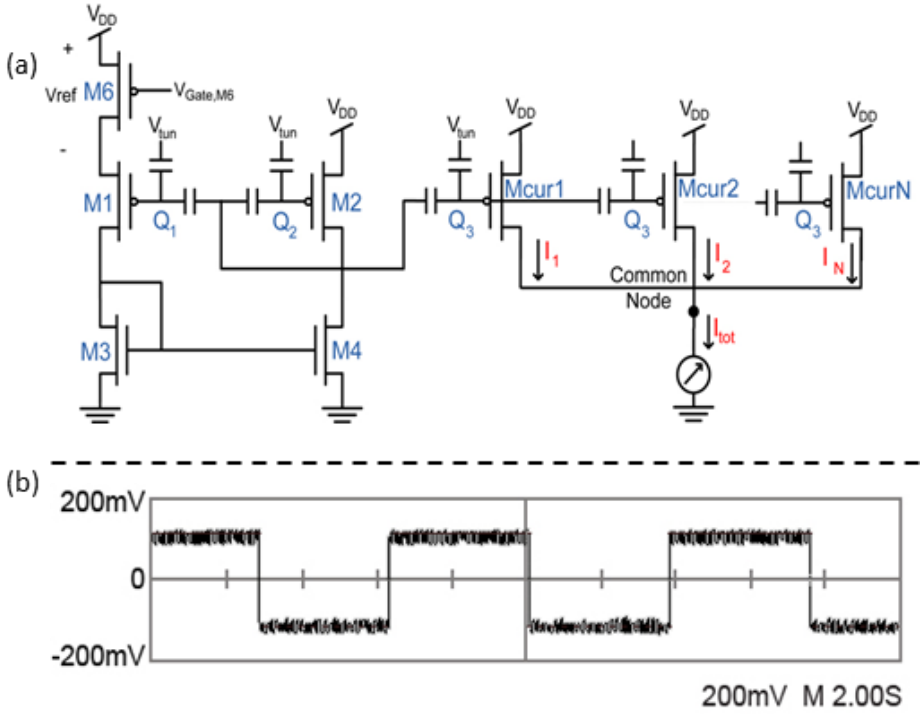


Figure 20. Current Source Circuit. (a) Two matched nFETs, M3 and M4, form a current mirror (gate voltage of M6 at zero). Equal currents pass through M1 and M2. Unlike a conventional bootstrap circuit where V_{ref} is generated by setting the size of M1 larger than M2, programming the gates of M1 and M2 at different charge levels, Q1 and Q2, generates V_{ref}. Assuming perfect matching of M1 and M2, V_{ref} is directly proportional to the charge difference Q_1-Q_2. Floating-gate pFETs, Mcur1-McurN, reflects the current generated inside the core circuit to an outside pin. The charge level (Q_3) programmed onto the gates of Mcur1-McurN changes the respective effective gate voltages, thus I_1 is dependent on Q_3. Multiple current branches can boost the current level with N copies. To linearly span a range of currents M6 is controlled to act as a variable resistor thereby providing current increments of 2%. (b) The oscilloscope trace illustrates an 116 µA biphasic charge-balanced pulse output across a1kW load resistor in parallel with a 10 nF capacitor.

Table 2 illustrates the charging scheme necessary to achieve the current levels on a single output line and ranges from 10.5 µA to 56.5 µA. The table also illustrates the ability to copy the current on parallel paths by connecting the core reference to *N* copy branches. Finally, Table 2 illustrates the ability to span a current range by using M6 as a variable resistor. This demonstrates two percent current increment capability. To further validate the current drive capability of the RASP 2.8, a representative 116 µA biphasic charge balanced stimulating current was generated and driven across a 1 kΩ load resistor in parallel with a 10nF capacitor used to model the input impedance of an electrode (Figure 20(b)).

Table 2. FPAA Current Stimulator Outputs

$V_{Gate, M6}$ (V)	N Branches	Charging Scheme (nA)			Current Level (µA)
		Q_1	Q_2	Q_3	
0.00	1	32000	1	1000	10.5
0.00	1	32000	1	5000	21.6
0.00	1	32000	1	32000	56.5
1.99	4	32000	1	32000	160.0
0.00	4	32000	1	32000	275.0
2.12	8	32000	1	32000	400.0
0.00	8	32000	1	32000	530.0

2.1.4 Analysis of Results from the FPAA Implementation

An FPAA-based vestibular signal processor for a single-canal system in which a voltage output from a rotated gyroscope was encoded into frequency modulated control signals for a current stimulator has been demonstrated. Also an FPAA implementation of a bootstrap current reference circuitry generating stimulation currents is presented. Although the current values that are sufficiently large to stimulate the vestibular neurons could be generated, the electrode voltage headroom was limited to the supply voltage of the FPAA, which is 3.3. V. The signal processing implementation demonstrated the power advantage of processing signals in the analog domain. Yet, because the number of circuit elements in an FPAA is limited, the signal processing and the current generation circuitry

were implemented on separate FPAA chips. Furthermore, only a single-canal signal processing circuitry could be implemented on the FPAA chip that has the signal processing circuitry. Another limitation of an FPAA implementation of the vestibular signal processing circuitry is related to its configurability. Although floating-gate pFETs provide an FPAA configurability, not all parameters of the signal processing block can be controlled by varying the charge trapped in floating-gate pFETs. For instance, to vary the steepness of the *tanh* expression in (4), the capacitance divider ratio at the inputs of the FGOTA needs to be changed. The last important limitation of the FPAA that renders it less suitable for a VP application is the large foot-print of the chip. Because of these limitations of the FPAA, a full-custom VP signal processing circuitry is designed as an Application-Specific Integrated Circuit (ASIC).

CHAPTER 3

A VP SIGNAL PROCESSING ASIC

The signal processing circuitry implemented on the FPAA was capable of converting inertial sensor outputs into firing rates in an energy-efficient manner. For a single SCC, the maximum/minimum values as well as the DC value of the *tanh* function that relates the firing rate to the gyroscope output could be well controlled. However control over the remaining parameters of the *tanh* function was not possible with the FPAA implementation. For instance the slope of the *tanh* function was fixed because of the fixed capacitance divider networks at the FGOTA inputs. Also the asymmetry observed at the neuron firing rates between the excitatory and the inhibitory movements as well as the neural dynamics filters and the coordinate system transformation circuitry were not implemented because of the limited number of elements. In summary, the energy-efficiency of signal processing in the analog domain was verified on an FPAA. However, due to the limited number of devices and the large footprint of the FPAA, a full-custom design approach is essential to meet space restrictions for an implantable low-power VP. For energy-efficiency, the design extensively makes use of low-power analog signal processing techniques that utilize MOS devices in subthreshold region.

In review there are three necessary signal processing functions for a VP; matrix-multiplication, filtering, and firing rate encoding. A matrix multiplication serves to align the primary axes of implanted rate sensors with the natural vestibular sense organs and to implement a precompensation strategy that reduces the erroneous representations of head motions because of current spread at the stimulation sites. Filtering these signals enables mimicking vestibular neural dynamics. And finally, firing rate encoding converts the head motion information into signals that neurons can transmit.

All of those functions can be performed purely in digital or analog domains. When selecting the domain, power and area that maintain the natural system's signal-to-noise

ratio (SNR), are the main concerns. In [41] it is shown that for small to mid-range SNR values (SNR<60 dB), subthreshold analog signal processing techniques are more advantageous over digital in terms of power and area. The SNR values corresponding to SCC and otolith signal processing circuitry can be approximated by finding the ratios of maximum angular velocity/linear acceleration values of normal head motions to the minimum sensation levels of the SCCs and otoliths, respectively. Biological data reveal that angular velocity and linear acceleration ranges of head motions are ±500 º/sec and ± 4 g, respectively, where g is the gravitational acceleration [1]. The detection thresholds are 2 º/sec and 15 mg for SCCs and otolith organs, respectively [42], [43]. Based on those values, the SNRs are estimated as ~48 dB for both SCCs and otoliths. Therefore, the custom-design extensively makes use of subthreshold signal processing techniques.

In the next sections, the blocks that are designed to implement the aforementioned VP functions are presented in detail.

3.1. Vector-Matrix Multiplier

A Vector-Matrix Multiplier (VMM) block is an essential component of the VP system that improves the efficacy of stimulation. In the natural human system, neurons of semicircular canals (SCCs) carry a three-component representation of 3D angular head movements and each SCC is associated with one-component [8]. In an analogous fashion, 3D linear movements are resolved into two separate vector components by the otolith organs. A VMM block serves to align the primary axes of implanted angular and linear rate sensors with the natural alignment of natural vestibular sense organs (Figure 21(a)); hence, the VMM performs coordinate system transformation. Additionally, the VMM block mitigates false representations of motion caused by undesired current spread. Resulting from the close proximity of vestibular neurons from adjacent canals/otolith organs (approx. 6 μm), stimulation current targeted for a given canal/otolith organ may excite neural tissue

for an adjacent canal/otolith organ (Figure 21(b)). A VMM can mitigate this effect with a precompensation strategy [16].

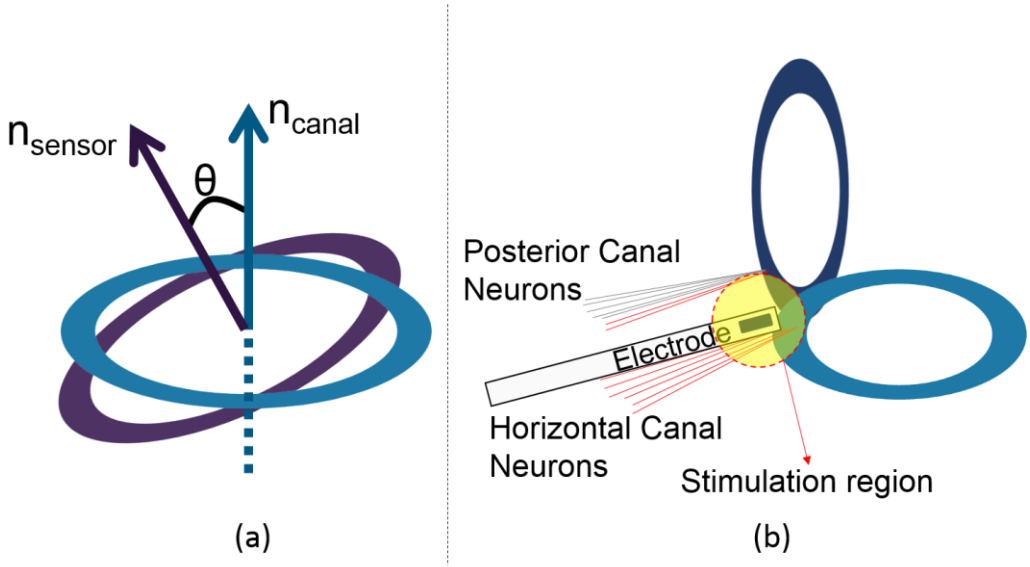


Figure 21. Vector Matrix Multiplication (VMM). For simplicity, the necessity for the VMM block is explained for the canals only. (a) To align the primary axes of implanted sensors and peripheral vestibular sense organs, a VMM can perform a coordinate system transformation between the implanted sensors and natural organs. (b) When an electrode is placed to stimulate only horizontal canal neurons, a portion of posterior canal neurons can be stimulated erroneously. To eliminate false representations of motion due to current spread a VMM can precompensate, or adjust, for the effect.

Functionally, the VMM block operates on the triplet from the angular velocity and linear acceleration sensors into appropriate modulation signals by use of a 3-by-3 and a 3-by-2 transformation matrix, respectively. These matrices can be characterized by analyzing the eye movements in response to stimuli and selecting transformation weights that maximize the response [16].

3.1.1. Design Considerations

In designing the VMM, four main parameters have been taken into account. Those are: (1) input and output voltage ranges, (2) bandwidth, (3) energy-efficiency, and (4) noise.

(1) Serving as the front end of the VP signal processing system, the VMM input voltage range needs to match with the output voltage range of the rate sensors of the VP. To figure output voltage ranges of the rate sensors, results from clinical studies and specifications of commercial rate sensors are used. Biological data reveals that angular velocity and linear acceleration ranges of head motions are ±500 º/sec and ± 4 g, respectively, where g is the gravitational acceleration [1]. Commercially available gyroscopes and accelerometers that operate within those ranges, have sensitivities varying between 0.1 mV/ º/sec – 2 mV/ º/sec and 10 mV/g - 400 mV/g, respectively. Therefore, the smallest input voltage ranges allowed for the VMM are ±50 mV and ±40 mV when interfacing with gyroscopes and accelerometers, respectively.

    The output voltage range of the VMM block is related to the following stage, namely the neural dynamics filters. The VMM output signals have to be within the linear range of the filters.

(2) The frequency range for normal head motions is f<20 Hz. Therefore, the VMM needs to have flat frequency response characteristics for signal frequencies less than 20 Hz.

(3) The energy-efficiency, in general, is very critical in designing systems for prosthetic applications to increase the amount of time the system battery lasts before it needs a replacement. In particular, for a VP to provide a sustained therapeutic benefit, continuous stimuli to vestibular neurons is essential [44].

(4) The noise performance of the VMM is important to not degrade the minimum sensation levels observed in SCCs and otoliths. Clinical studies reveal that detection threshold values for SCCs and otolith organs are 2 º/sec and 15 mg, respectively [42], [43]. Therefore, if a gyroscope having a sensitivity of 2 mV/ º/sec is used to detect the signal voltage corresponding to 2 º/sec, the VMM input noise power needs to be lower than 16 μV^2. Clearly, to interface the VMM with

sensors having smaller sensitivities, the noise performance of the VMM needs to be better.

The aforementioned design parameters are considered in selecting the signal processing domain in which VMM operation is performed. The selection procedure is detailed in the next subsection.

3.1.2. The VMM Architecture

Analog VMM architectures in the literature use either regular or floating-gate MOS devices [45],[46]. Because the latter needs relatively more complex peripheral circuitry to program charges onto the gates of MOS devices, the design makes use of regular MOS devices. The design explained here performs a 3-by-3 VMM operation for the SCCs. The design of the 3-by-2 VMM for the otoliths is the similar but with a slight difference which is presented in Section 3.1.3.6.

The general block diagram of the VMM is shown in Figure 22(a). For the nine multiplications needed for a 3-by-3 matrix multiplication a single multiplier is utilized, but the signals are time-division multiplexed (TDM). This is advantageous since power consumption is reduced and calculation errors due to device mismatches are minimized with a single multipler. It should be noted that the computation time, T_{VMM} needs to be much less than one period of the maximum frequency of the normal head motions (f_{max}=20 Hz), i.e. T_{VMM}<<50 msec.

Timing of the VMM is presented in Figure 22(b). The sensor output and the weight voltages ($w_{j,i}$) are fed to the multiplier periodically. A transimpedance amplifier (TIA) converts current output of the multiplier into voltage. This voltage is demultiplexed periodically in groups of three. In each group, three voltages are added together to generate discrete-time corrected signals for each SCC. A voltage averaging circuitry performs the addition. A second demultiplexer periodically feeds the voltage averaging output to three low-pass reconstruction filters to generate continuous-time corrected signals. A Clock

Generation Block (CGB) generates the necessary clocks. In the following sub-section, operation of each block is explained in detail.

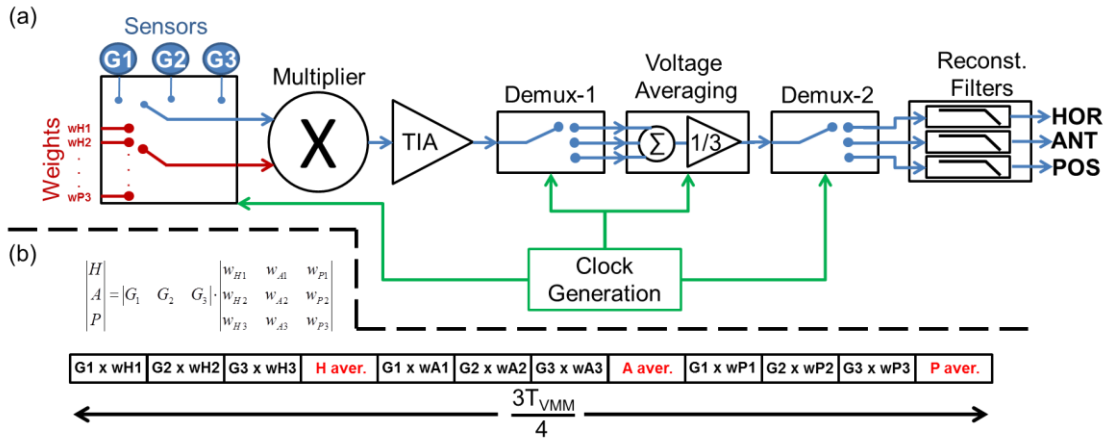


Figure 22. VMM operation. (a) Block Diagram. (b) The time sequence of each arithmetic operation, where T_{VMM} is the VMM cycle time. *HOR*, *ANT*, and *POS* are the corrected signals for the horizontal, anterior, and posterior canals, respectively. G_1, G_2, and G_3 denote the output signals from the gyroscopes and $w_{j,i}$ denotes the weight voltage corresponding to the canal j, and the gyroscope number i.

3.1.3. Design Details

3.1.3.1. Sensor and Weight Voltages Multiplexing

One period of the VMM cycle, T_{VMM}, is divided into 16 equal time intervals. The first 12 intervals are used for multiplication and voltage averaging (Fig. 22(b)). During each of these intervals sensor voltages and weight voltages are fed to the inputs of the multiplier sequentially. To reduce charge injection and clock feedthrough, multiplexing is done over a series of small-sized complementary switches controlled by the CGB. The VMM is idle for the last 4 intervals. The additional circuitry to reset the counter after 12 intervals would consume power and was therefore omitted retaining a 16-interval cycle.

This stage is essentially consisting of sample-and-hold circuits sampling three sensor and nine weight voltage signals. Each sample-and-hold circuit can be considered as an RC network when the corresponding switch is ON. During that period, R is the switch

ON resistance and *C* is the load capacitance, which is the gate capacitance of the multiplier input transistor. Thermal noise introduced by *R* is sampled onto the capacitor and therefore during switch OFF period, it remains at the output. The total output voltage noise power, in the Nyquist bandwidth is found as *kT*/*C* [47]; where *k*, *T*, and *C* are the Boltzmann constant, temperature in *K*, and total capacitance seen at the multiplier input, respectively. Using large multiplier input transistors, the load capacitance of the sample-and-hold circuits is increased, thereby improving the noise performance of this stage.

3.1.3.2. Multiplier

A transconductance multiplier generates current outputs proportional to the product of its voltage inputs; namely, a gyroscope output and a stored weight voltage. The multiplier is a four-quadrant, wide-output-range Gilbert multiplier (Figure 23) [35].

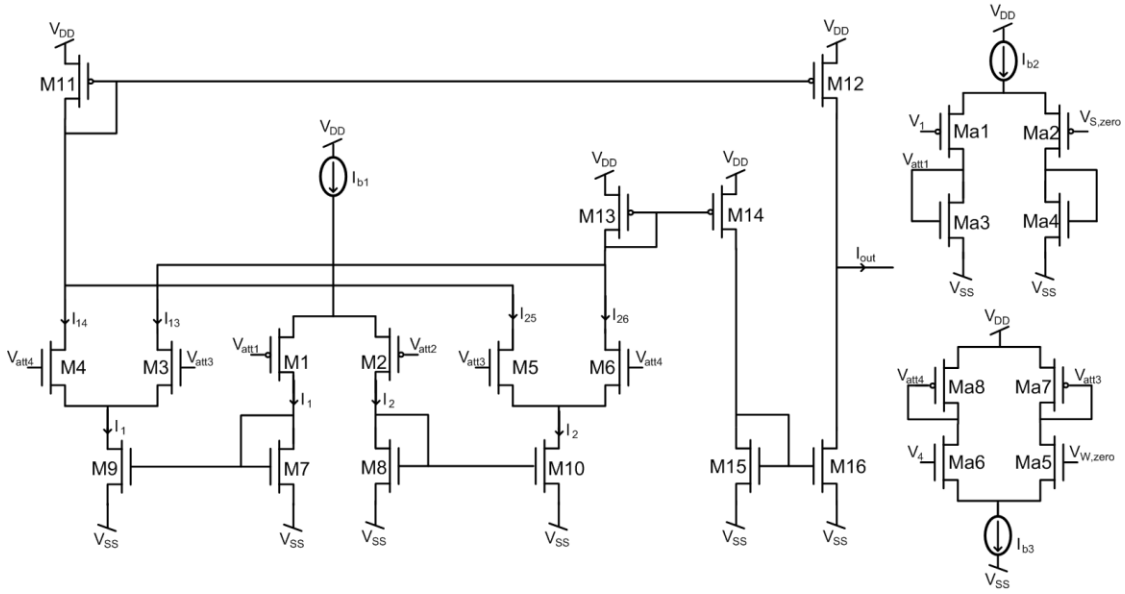


Figure 23. Multiplier schematics. Attenuation stages are used to increase the linear range.

The multiplier is operated in the subthreshold region with a current characteristic of a MOS in saturation:

$$|I_{DS}| = I_0 \left(\frac{W}{L}\right) e^{\frac{\kappa|V_{GB}|-|V_{SB}|}{U_T}}, \quad (7)$$

where I_0 is the zero-bias current, κ the constant relating the surface potential of the MOS to its gate voltage, V_{GB} the gate-to-bulk potential, V_{SB} the source-to-bulk potential, and U_T the thermal voltage [10]. After a series of calculations the multiplier output current, I_{out} is:

$$I_{out} = I_{b1} tanh\left(\frac{\kappa(V_{att1} - V_{att2})}{2U_T}\right) tanh\left(\frac{\kappa(V_{att3} - V_{att4})}{2U_T}\right). \quad (8)$$

To increase the small linear range due to subthreshold operation, input voltages are attenuated at two attenuation stages (Figure 23) [48]. Each attenuation stage consists of a differential pair in above-threshold region with a diode-connected load in subthreshold region, thereby creating an attenuation factor:

$$\alpha = -\frac{2U_T}{\kappa}\sqrt{\frac{K(W/L)}{I_{b,att}}}, \quad (9)$$

where K is the transconductance parameter, which is a function of mobility and unit gate-oxide capacitance; and $I_{b,att}$ is the bias current of the attenuation stage [48]. The bias currents I_{b1}, I_{b2}, and I_{b3} are generated by an off-chip reference circuitry.

The effective noise sources of the multiplier are presented in Figure 24.

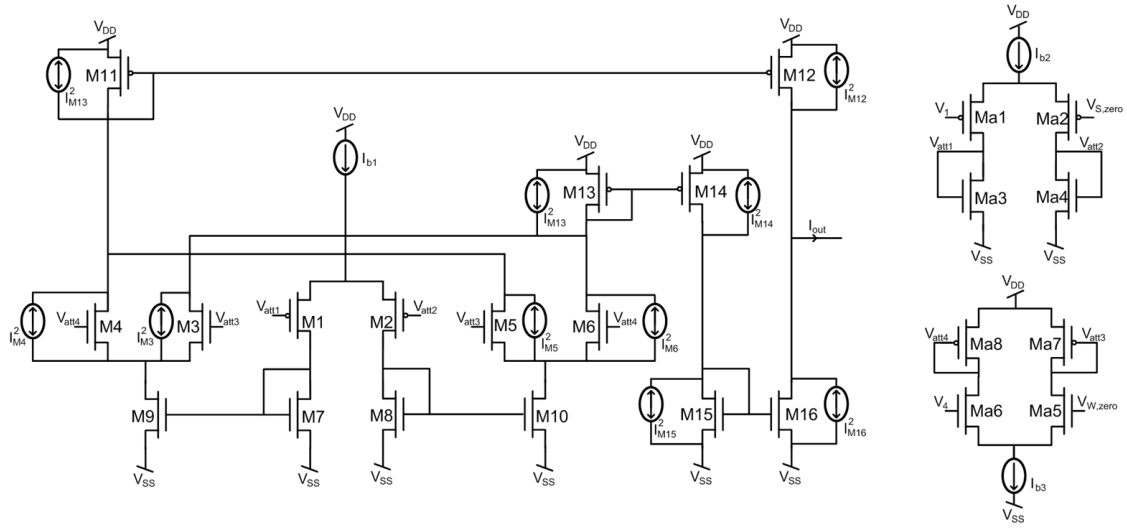


Figure 24. Multiplier noise model.

Ideally, noise contributions from the transistors M1-M2, M7-M10, Ma1-Ma8, and the current sources I_{b1}-I_{b3} cancel each other because of the current subtraction at the output

node. Therefore, they are not included in the following noise expression. Assuming noises of same size and same type transistors are the same, the input-referred noise PSD:

$$\hat{v}_{in,Mult}^2 = \frac{A\cdot\left(4\hat{i}_{M3}^2 + 3\hat{i}_{M11}^2 + \hat{i}_{M15}^2\right) + \left(\hat{i}_{M12}^2 + \hat{i}_{M16}^2\right)}{G_{id}^2}, \tag{10}$$

where the coefficient A is the unitless size ratio of M12 to M11 and G_{id} is the small-signal differential transconductance gain of the multiplier, which is given by $G_{id} = g_{m1}g_{mA1}/g_{mA3}$. Considering the white noise, the output voltage noise power is found as:

$$v_{out}^2 = \int_0^\infty \frac{v_{in,Mult}^2 df}{1+(2\pi f\tau)^2} = \frac{M}{(g_{mA1}/g_{mA3})^2}\left(\frac{kT}{C}\right) = \frac{M}{\alpha^2}\left(\frac{kT}{C}\right), \tag{11}$$

where M is a constant related to κ, C the output capacitance of the multiplier, τ the time constant associated with the high impedance output node of the multiplier, and α the attenuation factor. Based on (9) and (11), decreasing the bias currents through the attenuation stages improve the noise performance of the multiplier.

3.1.3.3. Transimpedance Amplifier

The current output of the multiplier is converted into voltage by a transimpedance amplifier (TIA). It should be noted that, a linear relationship between the input current and the output voltage is desired at this stage. Therefore, a linear TIA topology is selected over a logarithmic TIA [49]. The TIA utilizes an operational transconductance amplifier (OTA) in resistive feedback configuration (Figure 25). This configuration keeps the input node potential, which is at the same time the output node of the multiplier, at virtual ground, thereby reducing variations in multiplier output current because of changes in the output voltage.

The transfer function of the TIA is found as:

$$\frac{V_{out,TIA}(s)}{I_{mult}(s)} = -R\left[\frac{1-(1/RG)}{1+\frac{sC_L}{G}}\right], \tag{12}$$

where G is the OTA transconductance and C_L is the load capacitance. Based on (12), it is suggested that if RG term is sufficiently large, the DC gain would be equal to -R V/A. The input impedance of the TIA is found as:

$$Z_{in}(s) = \frac{1+sRC_L}{G+sC_L}. \tag{13}$$

It should be noted that, for small frequencies, Z_{in} is approximately equal to $Z_{in} \cong 1/G$. To keep power consumption small while obtaining a sufficiently small Z_{in} such that the multiplier output can source current to the TIA, bias current $I_{b,TIA}$, which is related to G through $G=I_{b,TIA}/2U_T$, is set as $I_{b,TIA}$=300 nA, thereby setting $Z_{in} \cong 173\ k\Omega$, which is sufficiently small compared to the high output impedance of the multiplier in the GΩ range. The R value is set by the input current and output voltage range requirements of the TIA. The TIA is the last amplification stage of the VMM. Therefore, the output voltage range of the TIA needs to be identical to the VMM's output voltage range, which is set by the input voltage range requirement of the neural dynamics filters stage (~100 mV). Justification of that requirement is explained in Section 3.2.2., where the Neural Dynamics Filter architecture is discussed. To obtain an output voltage range of ±50 mV from the

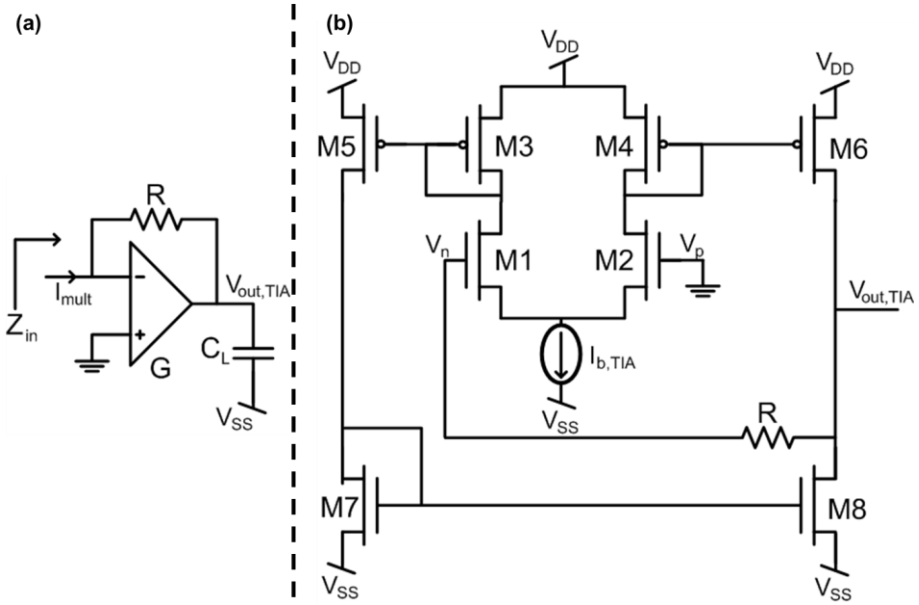


Figure 25. TIA schematics. (a) A linear TIA topology has been selected. (b) The TIA utilizes and OTA in subthreshold region.

multiplier output current that has a range of ±50 nA, *R* is selected as *R*=1 MΩ. The voltage output of the TIA is connected to the voltage averaging and demultiplexing stage.

To investigate the noise performance of the TIA, the noise model in Figure 26 is used.

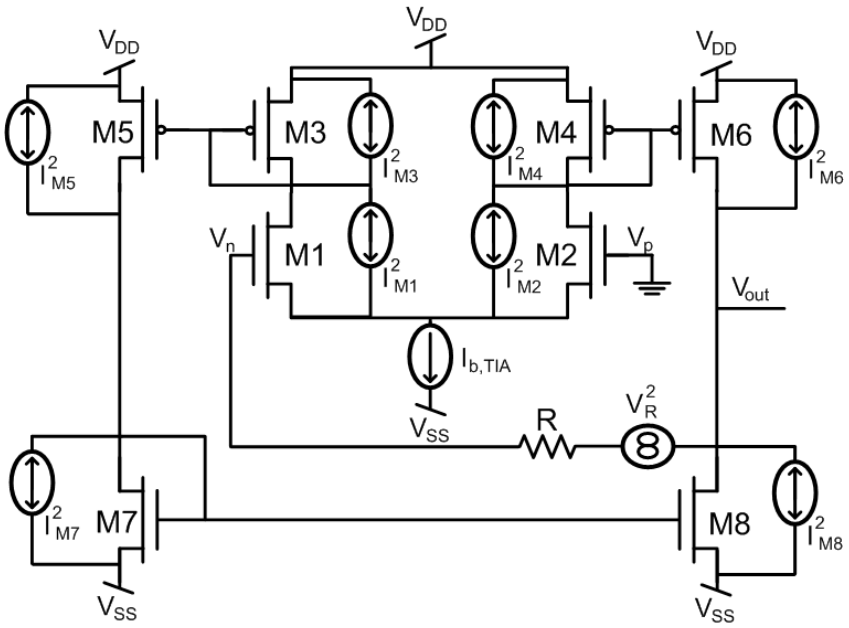


Figure 26. TIA Noise Model.

Input-referred current noise PSD is found as:

$$i_{in}^2 = \frac{(2i_{M1}^2+4i_{M3}^2+2i_{M7}^2)(r_{o6}//r_{o8})^2}{R^2} + \frac{4kT}{R}, \tag{14}$$

To find the total output voltage noise power, input-referred current noise PSD is multiplied by the square of the transfer function of the TIA, and then integrated over all frequencies. If only white noise is considered, the total output voltage noise power expression is found as:

$$v_{out}^2 = \int_0^\infty \frac{i_{in}^2 R^2 df}{1+(2\pi f\tau)^2} = \frac{i_{in}^2 R^2}{4\tau} = \frac{(2i_{M1}^2+4i_{M3}^2+2i_{M7}^2)(r_{o6}//r_{o8})^2+4kTR}{4C_L/G}, \tag{15}$$

Based on (15), the noise performance degrades with increasing *R* and the drain currents of the devices, which are directly related to the $I_{b,TIA}$, and decreasing C_L.

3.1.3.4. Voltage Averaging and Demultiplexing

The TIA output is demultiplexed to generate three voltages that are arithmetically averaged at voltage averaging circuitry (Figure 27).

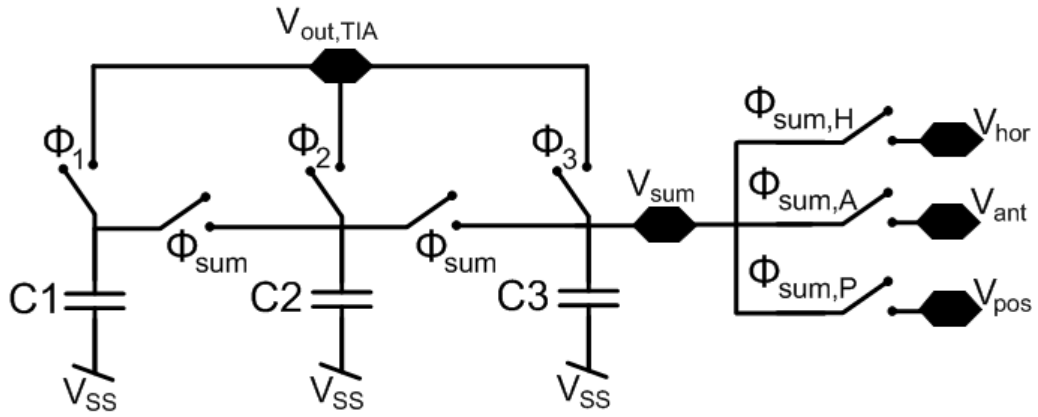


Figure 27. Voltage averaging and demultiplexing schematics.

For energy-efficiency, the voltage averaging circuitry is designed as a passive averager that uses charge-sharing principle. At Φ_1, Φ_2, and Φ_3; TIA output is sampled into equal sized sampling capacitors; *C1*, *C2*, and *C3*, respectively. At Φ_{sum}, the sampling capacitors are connected in parallel to generate a voltage, V_{SUM}, which is ideally equal to one third of the sum of the voltages stored at the capacitors. However, because of charge leakage during hold periods, the voltage levels at sampling capacitors reduce. The sampling capacitance is set at 5 pF, which is large enough to create negligible error because of charge leakage. Capacitor mismatches also create error. Both leakage and mismatch errors can be compensated by the weight voltages. V_{SUM} is demultiplexed to generate the discrete-time corrected signals corresponding to the three canals, namely V_{hor}, V_{ant}, and V_{pos}.

Switched-capacitor operation of this stage results in kT/C noise power at the output per each canal. It should be noted that, increasing the sampling capacitor values not only improves the noise performance of the voltage average and demultiplexer stage, but also that of the TIA based on (15).

3.1.3.5. Reconstruction Filters

High-frequency components of the output signals of the voltage averaging and demultiplexing stage are removed by the reconstruction filter stage, which consists of three cascaded 1st order low-pass filters per each canal. For their high power efficiency, Gm-C filter topology is selected over other active filter topologies, namely opamp-C, MOS-C, and switched-capacitor filters (Figure 28).

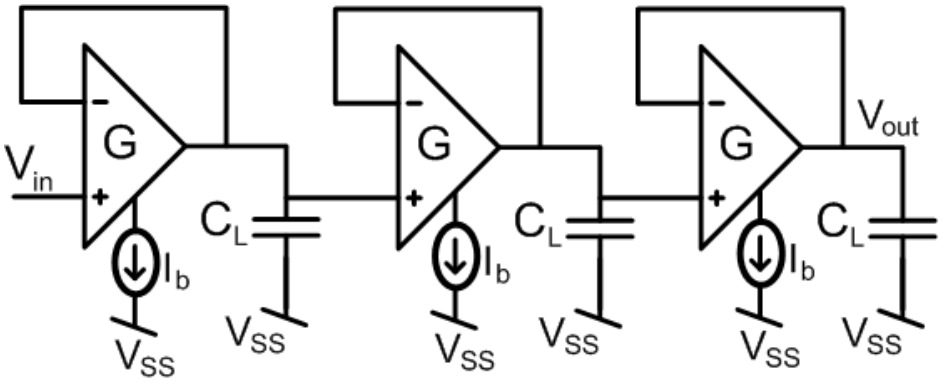


Figure 28. Reconstruction filter schematics.

OTAs, which can be built with small number of devices, function as the transconductance elements. The bias currents of the stages are set to 1 nA to keep power consumption low. The -3 dB frequency of stages is determined by considering the amount of degradation in signals corresponding to the maximum head motion frequency of 20 Hz. Simulations show that by setting -3 dB frequency to 1 kHz, 20 Hz signals degrade only by 800 ppm. For the selected bias current of 1 nA, f_{-3dB}= 1 kHz when load capacitances are C_L=10 pF. Reconstruction filter stage not only removes the unwanted high frequency components of the signals, but also improves the noise performance of the overall VMM block by narrowing down the bandwidth of the system.

3.1.3.6. Clock Generation Block

The clocks necessary for a 3-by-3 VMM circuitry are generated by a Clock Generation Block (CGB), which consists of D-Flip Flops and various logic gates. The input

to the CGB is an external clock. Its period, $T_{in,}$ must guarantee complete charging/discharging of the voltage averaging capacitors. This is accomplished by the multiplier output current. For typical values (I_{b1}=50 nA, sampling capacitor of 5 pF, maximum potential change of 100 mV) the gyroscope output and weight voltage sampling interval must exceed 10 µs (100 kHz max. input clock frequency). The upper bound for T_{in} is determined by the bandwidth requirement of the system. Signals sampled non-ideally with a clock pulse duration of τ, are low-pass filtered in the frequency domain by the $sinc(\pi*f*\tau)$ function [50]. Similarly, the sample-and-hold operation of our system reduces the magnitudes of the sensor signals. The multiplexer samples the sensor signals with a duration of $\tau=T_{in}$ and at a frequency of $f_s=0.25/T_{in}$. The magnitude of the frequency response of the sampling is shown in Figure 29.

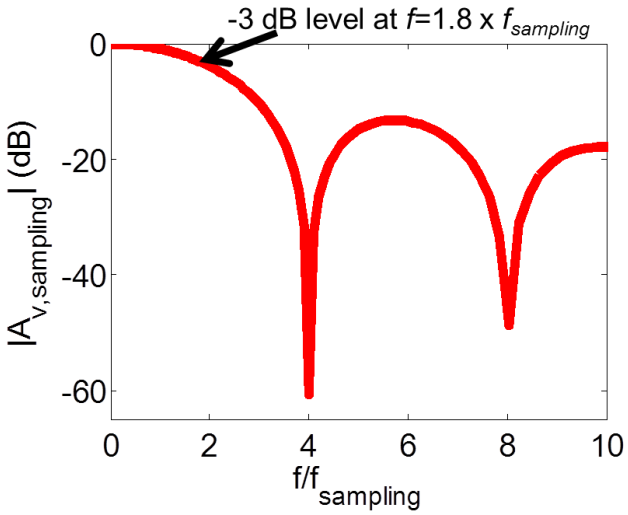


Figure 29. Sampling of the signals at the multiplexing stage reduces the magnitudes of the sensor signals by means of a *sinc* function, which limits the minimum allowable input clock frequency.

The -3 dB frequency is $f_{-3dB}=1.8f_s=0.45/T_{in}$. For signal frequencies less than 20 Hz, to limit the magnitude reduction to 1000 ppm, -3 dB frequency is to be set to f_{-3dB}=360 Hz, implying an upper bound of T_{in}=1.3 ms (800 Hz minimum input clock frequency). It should be noted that this upper bound is impractical because of charge leakage at the sampling capacitors of the voltage averaging stage. Thus, the optimum clock

frequency is determined when testing the devices. One period of VMM operation, namely T_{VMM} is T_{VMM}=16*T_{in}. The schematics of the clock generation block is shown in Figure 30.

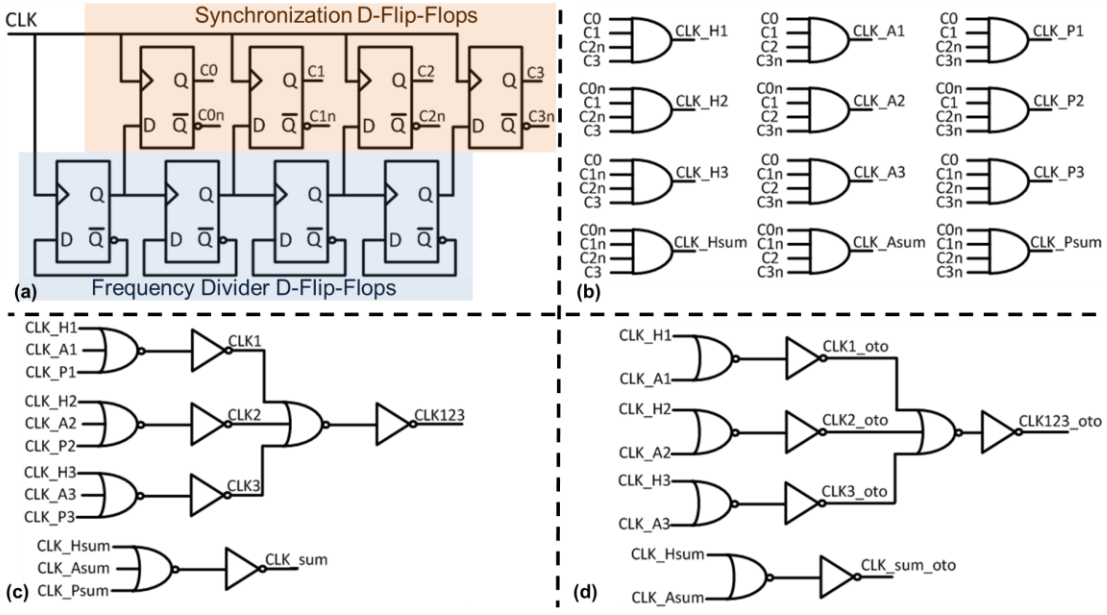


Figure 30. Clock Generation Block Circuitry. (a) Frequency of the input clock, CLK, is divided into 2/4/8/16. The resulting clocks are then synchronized. (b) Clocks of the sensor and weight multiplexing stage for both 3-by-3 and 3-by-2 VMM operations. (c) Demultiplexer clocks of 3-by-3 VMM operation (SCC). (d) Demultiplexer clocks of 3-by-2 VMM operation (otolith).

It should be noted that both VMMs complete the calculation in 16 clock cycles. However, because of less number of calculations, the 3-by-2 VMM is idle for the last 8 intervals instead of 4 intervals as is the case in the 3-by-3 VMM. Therefore, instead of NOR3 gates, NOR2 gates are used in the multiplexer clock generation circuitry of the 3-by-2 VMM.

3.1.4. Measurement Results

The VMM has been fabricated with TSMC 0.35-µm 4P2M n-well and TI LBC7 0.35-µm 3P2M n-well CMOS processes. In Figure 31, optical images and floor plans of the VMMs are shown. The TSMC VMM performs a 3-by-2 multiplication and the footprint is 1.523 mm x 1.548 mm. However, the effective area covered is less than a quarter of the

total footprint. TI VMM performs a 3-by-3 multiplication and the footprint is 1 mm x 0.73 mm.

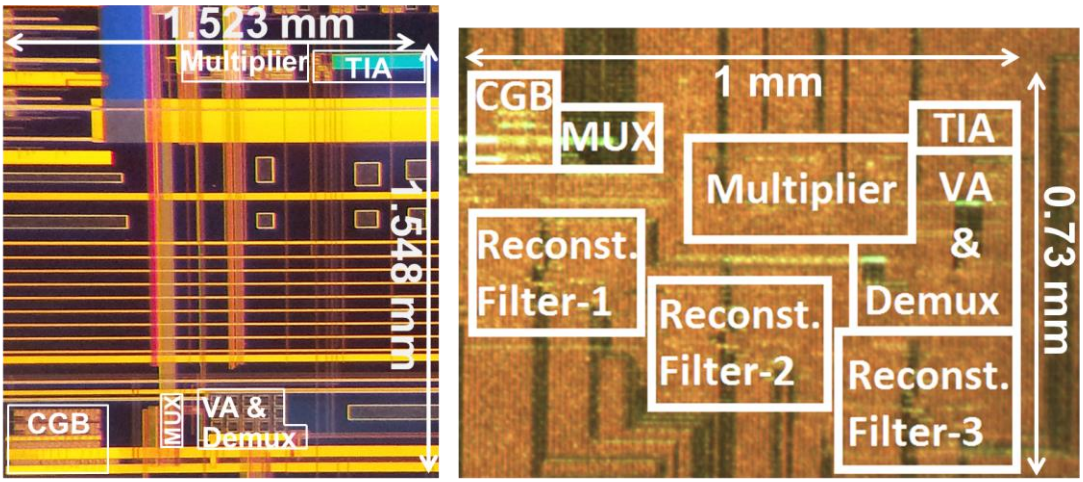


Figure 31. VMM Floor Plans. The abbreviation VA refers to the voltage averaging block. (a) 3-by-2 VMM fabricated with TSMC 0.35-µm 4P2M n-well CMOS process. (b) 3-by-3 VMM fabricated with TI LBC7 0.35-µm 3P2M n-well CMOS process.

3.1.4.1. Testing Procedure

The VMM test-bench schematic is shown in Figure 32. It should be noted that the schematic is drawn based on the 3-by-3 VMM chip. The test-bench for the 3-by-2 VMM is the same with the exception that the number of bias currents, weight voltages, and output signals are fewer. The VMM operates with dual power supplies, ±1.6 V. To eliminate the power supply noise, bypass capacitors of 100 nF are connected between the rail voltages and the ground terminals of the power supplies, namely PS-1 and PS-2 (for simplicity not shown in the schematics).

Input clock for the CGB is generated using an off-the-shelf MSP430 microcontroller from Texas Instruments (Dallas, TX). One single channel Hewlett Packard 33120A (Palo Alto, CA) and one dual channel Tektronix AFG 3022B (Beaverton, OR) function generator and two dual channel Keithley 2636A (Cleveland, OH) sourcemeters supply sensor input signals and weight voltages, respectively. The output signals are

observed on a Tektronix DPO 3014 scope. The total output voltage noise power measurement has been performed using an HP 35665A signal analyzer. All bias currents have been generated using off-the-shelf components. Below, after the describing the off-chip bias current generation circuitry, measurement results are presented.

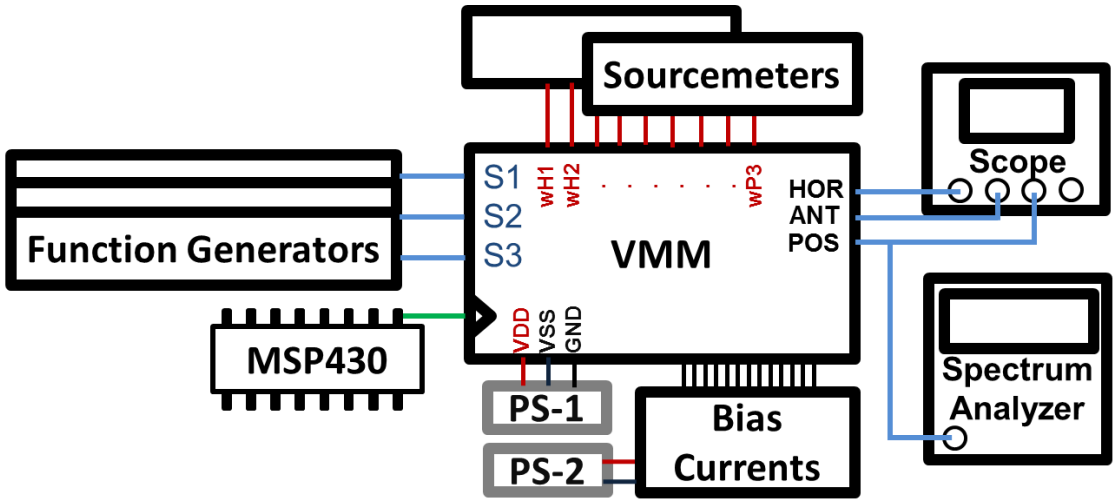


Figure 32. VMM Test-bench schematics.

3.1.4.2. Bias Generation Circuitry

Off-the-shelf current reference and OPAMP chips have been used to generate the bias currents of the VMM block. In total, 13 bias currents (source/sink) have been generated using the schematics in Figure 33.

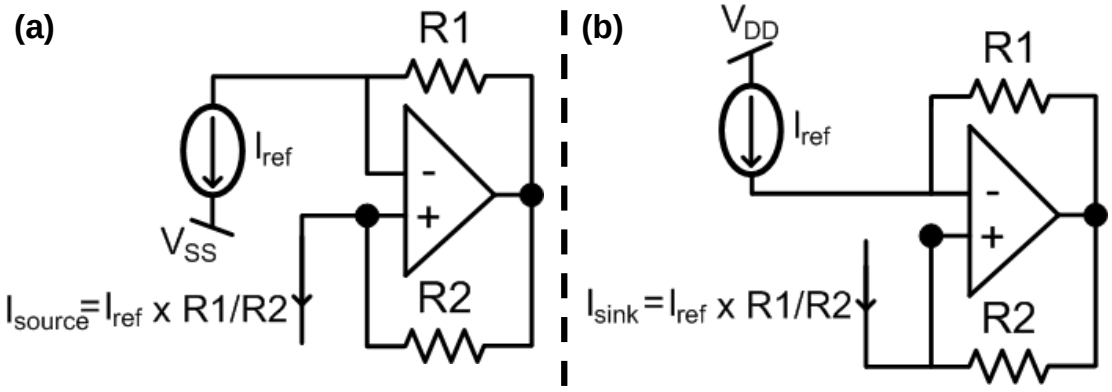


Figure 33. Off-chip bias current generation circuitry. (a) Source. (b) Sink.

The reference current, namely I_{bias}, has been generated using a TI REF 200 dual current source/sink chip. Because, bias currents of the VMM are less than 1 µA, an ultra-low bias current TI OPA129 has been used as the OPAMP stage. R1 and R2 are discrete components and their values for all bias currents generated are summarized in Table 3. In the following subsections, measurement results from both TSMC and TI VMM chips are presented in parallel.

Table 3. Bias Current Generation Circuitry Resistance Values for VMM

Bias Name	Value	R1	R2
Multiplier main (source)	51 nA	510 Ω	1 MΩ
Multiplier attenuation (source and sink)	360 nA	3.6 kΩ	1 MΩ
TIA (sink)	300 nA	3 kΩ	1 MΩ
Reconstruction filter (sink)	1 nA	10 Ω	1 MΩ

3.1.4.3. Linearity

To validate linearity, a sinusoidal signal representing gyroscope output is input to the VMM. This sensor input is multiplied with a range of weight voltages between -427 mV and 323 mV for the 3-by-2 TSMC chip and between -200 mV and 200 mV for the 3-

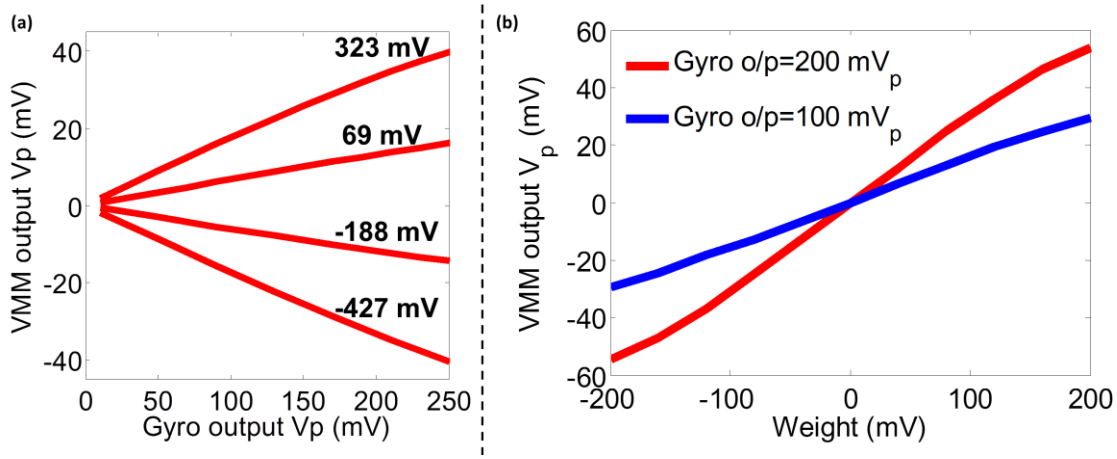


Figure 34. Linear dependence of the VMM output (y-axis) with respect to the input signal magnitudes (x-axis). (a) The results from the TSMC 3-by-2 VMM chip are parameterized by weight voltage (-427 mV to 323 mV, equal weighting applied to all gyro outputs). (b) The results from the TI 3-by-3 VMM chip are parameterized by gyroscope output voltages (200 mV_p and 100 mV_p).

by-3 TI chip. For a fixed weight voltage, the output signal magnitude varies linearly with the magnitude of the sinusoidal input (Figure 34).

Figure 35 illustrates the outputs of the 3-by-2 and 3-by-3 VMM chips, when 10 Hz and 3.5 Hz sinusoidal signals are fed to all three sensor inputs; *G1*, *G2*, and *G3*; and multiplied by the weight elements $W_{3-by-2} = \begin{vmatrix} 0.2 & -0.44 \\ 0.2 & -0.44 \\ 0.2 & -0.44 \end{vmatrix}$ and $W_{3-by-3} = \begin{vmatrix} 1 & -1 & 1 \\ 1 & -1 & 0 \\ 1 & -1 & -1 \end{vmatrix}$, respectively.

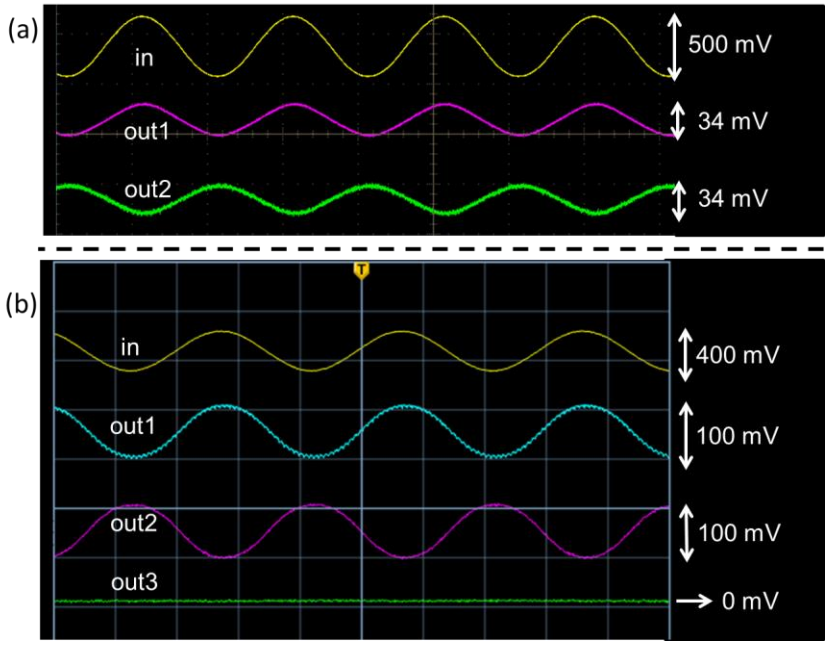


Figure 35. The output waveforms. (a) TSMC 3-by-2 VMM measurements. Out1-out2 are obtained when the input voltage is multiplied by the weight matrix $W_{3-by-2} = \begin{vmatrix} 0.2 & -0.44 \\ 0.2 & -0.44 \\ 0.2 & -0.44 \end{vmatrix}$ (b) TI 3-by-3 VMM measurements. Out1-out3 are obtained when the input voltage is multiplied by the weight matrix $W_{3-by-3} = \begin{vmatrix} 1 & -1 & 1 \\ 1 & -1 & 0 \\ 1 & -1 & -1 \end{vmatrix}$.

3.1.4.4. Bandwidth

Because of the high input clock frequencies, bandwidths of both VMMs are dominated by the reconstruction filter stage rather than the low-pass filtering behavior of

the non-ideal sampling. The measured -3 dB frequencies of the 3-by-2 and 3-by-3 VMM systems are $f_{-3dB,VMM}$=~500 Hz for both VMM chips, which is equal to -3 dB frequency of the cascaded reconstruction filter stage.

3.1.4.5. Noise

As reported in Section 3.1.4.3. the bandwidths of the VMM stages are ~500 Hz. However, the next stage, namely the neural dynamics stage, narrow downs the -3 dB bandwidth to ~23 Hz. Therefore noise analysis is performed for a bandwidth of 20 Hz<BW<500 Hz. The output voltage noise PSD of the 3-by-3 VMM is measured for f<50 Hz on the spectrum analyzer, when all sensor and weight voltage inputs are shorted to ground. The data is transferred to a PC and plotted with MATLAB (Figure 36).

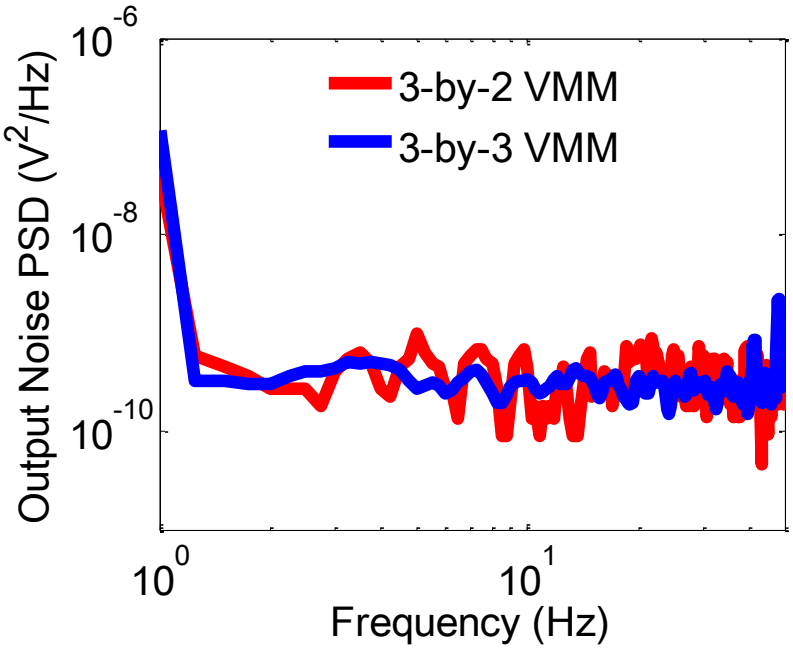


Figure 36. Output noise voltage PSDs of the 3-by-2 and 3-by-3 VMMs.

Integrating the output noise PSDs, the total output noise power is calculated as $v_{n,out,3-by-3}^2 = 16.76\, nV^2$ and $v_{n,out,3-by-2}^2 = 18.04\, nV^2$. To find the minimum detectable signal, the total output noise power is reflected to input. The gains of the 3-by-2 and 3-by-3 VMMs are 0.16 V/V and 0.25 V/V, respectively. Therefore, input-referred

noise power is found as $v_{n,in,3-by-3}^2 = 16v_{n,out}^2 = 268.1\, nV^2$ and $v_{n,in,3-by-2}^2 = 39v_{n,out}^2 = 704.7\, nV^2$, from which minimum detectable signal of the VMM is found as $v_{mds,3-by-3} = \sqrt{v_{n,in}^2} = 517.7\, \mu V$ and $v_{mds,3-by-2} = \sqrt{v_{n,in}^2} = 839\, \mu V$.

3.1.4.6. Power

Under normal bias conditions of I_{b1}=50 nA, I_{b2}=I_{b3}=350 nA, and $I_{b,TIA}$=300 nA, the power consumptions of the multiplier and the transimpedance amplifier stages of the 3-by-2 VMM are calculated as 2.72 µW and 1.92 µW, respectively. With the assumption that the parasitic capacitance values at the outputs of each gate are as large as 500 fF, the clock generation circuitry power consumption is calculated as 730 nW. Ideally the voltage averaging circuitry consumes power only during the time instances when the TIA output is sampled on the load capacitors of 5 pF. For each capacitor the sampling frequency is approximately equal to one quarter of the input clock frequency. Also, the voltage output of the TIA varies between ±50 mV. To estimate the worst-case power consumption value, during each sampling period it is assumed that the sampling capacitance voltage value varies by 50 mV. Using the dynamic power consumption formula for a digital gate, the power consumption of the voltage averaging stage is calculated as ~ 1 nW. Therefore, the total power consumption of the 3-by-2 VMM is calculated as 5.37 µW. The 3-by-3 VMM chip power consumption is measured as 5.1 µW, indicating 8.16 nJ of energy consumption per 3-by-3 VMM operation.

3.1.5. Discussion

A 3-by-2 and a 3-by-3 VMM circuitry for a VP is presented. The performance parameters of both 3-by-2 and 3-by-3 VMMs are summarized in Table 4.

The VMMs can be interfaced with accelerometers and gyroscopes having sensitivities up to 62.5 mV/g and 0.4 mV/˚/sec, respectively. The output voltage ranges of the VMMs match with the linear ranges of the neural dynamics filters stage (±50 mV). The

bandwidths of the VMMs are sufficiently large, thereby ensuring no attenuation of the sensor signals limited to normal head motion bandwidth of 20 Hz. The power values verify the energy-efficiency of the designs.

Table 4. Summary of Performance Parameters of the 3-by-2 and the 3-by-3 VMMs

Property	**3-by-2 VMM**	**3-by-3 VMM**
Power	5.37 µW (calculated)	5.1 µW
Input/output voltage range	±250 mV / ±40 mV	±200 mV / ±50 mV
Noise ($v_{n,in}$)	839 μV_{rms}	517.7 μV_{rms}
Minimum detectable acceleration/angular velocity	19 mg	1.83 deg/sec
SNR	46.47 dB	48.73 dB
Bandwidth	500 Hz	500 Hz
Clock Frequency	22 kHz	10 kHz
Calculation Time	728 µs	1.6 ms
MAC/µW	1720	1103
Dimensions	1.5 mm x 1.5 mm	1 mm x 0.73 mm

The 3-by-3 VMM noise performance satisfies the design criteria of the SCC sensation threshold value (2 deg/sec). In the future versions of the designs, the noise performance can be further improved by performing the following. Since the noise expressions are in *kT/C* form, increasing the sampling capacitances can improve the noise performance but at the expense of increased area. Additionally, the dimensions of the input MOS devices can be increased. As a result, the load capacitances of the demultiplexing and the multiplier stages would be increased, thereby reducing the *kT/C* noise. Increasing the input MOS device sizes would also reduce the flicker noise. Another method to reduce the flicker noise is to change the TIA and the OTA architectures from nMOS-input to pMOS-input. As an effort to reduce the thermal noise contribution of the resistor, the value of the TIA feedback resistor can be reduced. The reduction in the transimpedance gain can be compensated by increasing the multiplier bias current, at the expense of increased power

consumption. However, because the power consumption of the multiplier is dominated by the attenuation stages, increase in the multiplier bias current is tolerable.

Matrix multiplication is performed in two of the state-of-the-art VP systems [16-17],[51]. In [16] an ultra-low power microcontroller and in [51] a real time controller is used. In neither of the systems, power consumption values specific to the matrix multiplication operation are reported. In [17] the microcontroller is reported to consume 12 mW of power when performing all VP signal processing functions. To estimate the power consumption due only to the matrix multiplication, an analog input/output VMM is implemented on an MSP430 microcontroller. For an A/D sampling frequency of 220 Hz, the measured power consumption is 6 mW. It should be noted that to make a more realistic comparison between the VMMs presented and the microcontroller, supporting blocks; namely memory, reference, and DAC; need to be designed. However, with careful design of those blocks, current consumption of the custom chip could still be kept in the sub-mW range.

3.2. Neural Dynamics Filters

Research on animals show that firing rate of the vestibular neurons is frequency dependent [7],[12]. To fully replicate the vestibular neural behavior, the VP needs to implement the vestibular neural dynamics. The frequency-dependence stems from both the mechanical properties of the vestibular organs and the adaptation of neurons [7],[12]. By utilizing rate sensors that mimic the natural angular-velocity and linear-acceleration sensing mechanisms in SCCs and otoliths, mechanical-property-related dynamics could be implemented in a VP. Although research is in progress on developing such a sensor for sensing angular-velocity, there is not any commercial gyroscopes or accelerometers available in the market that mimics the sensing mechanisms of the natural vestibular organs

[52],[53][2]. As the signal processing circuitry is designed to interface with commercial rate sensors, both mechanical and adaptation-related frequency characteristics need to be implemented. Research on animals show that the semicircular and otolith neural dynamics have bandpass and lowpass characteristics, respectively (Figure 37 [7],[12].

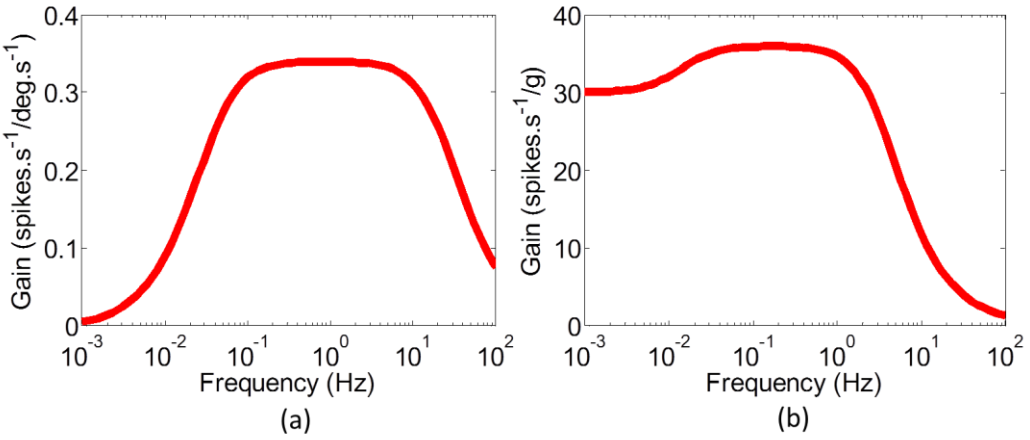


Figure 37. Neural dynamics of peripheral vestibular organs. (a) SCC neural dynamics. (b) Otolith neural dynamics.

In the next subsection, design goals when implementing these transfer-functions for a VP, are presented.

3.2.1. Design Considerations

Designing the neural-dynamics filters, five major parameters have been considered; namely (1) achieving very long and tunable time-constants, (2) energy-efficiency, (3) area, (4) input and output voltage ranges, and (5) noise.

(1) The time constants associated with the vestibular neural dynamics can be very long (up to 80s). The general shape of the neural transfer-function characteristics presented in Figure 37, and it is roughly the same within all

[2] Finite element analysis simulations corresponding to an angular velocity sensing mechanism that mimics the SCCs are presented in Appendix A.

members of a species. However, animal studies show that, the time-constants measured from a single neuron is not the same as in other neurons [7],[12]. Similarly, time constants vary from patient to patient. Therefore, the VP needs to allow the user to tune the time-constants, to best mimic the natural behavior of the vestibular neurons of a particular patient. The design needs to overcome the challenge of achieving long time constants while keeping the total area reasonably small.

(2) It is desired to achieve long battery life in a prosthesis, thereby reducing the frequency of surgical operations needed to replace the battery. Therefore, energy-efficiency is the paramount design criteria in designing the filters.

(3) Very long time constants usually require very large capacitors, which is not desired as the area is an important concern for prosthetic applications.

(4) The filter stage functions as the intermediate stage between the VMM and the voltage-to-frequency conversion block. Therefore, input and output voltage ranges of the filter stage needs to match with the output voltage range of the VMM and input voltage range of the voltage-to-frequency conversion block, respectively.

(5) To achieve the minimum sensation levels observed in SCCs and otoliths, the noise performance of the filters is an important design criterion.

In the next subsection an overview of possible circuit architectures are presented. Then, justification of the selected architecture and a brief description of its operation are addressed.

3.2.2. Selection of the Filter Architecture

The analog signals from the VMM block can be filtered either using only passive circuit components; namely resistors, capacitors, and inductors; or using both active and

passive components as in OPAMP-RC, OPAMP-MOSFET-C, switched-capacitor OPAMP, and OTA-C filter topologies [54-57].

3.2.2.1. Time Constants

It should be noted that the time-constants of the neural dynamics are very long (in the order of tens of seconds). Therefore, a passive filter topology is not practical since long time constants would require very large on-chip resistors and capacitors. When considering energy-efficiency, OTAs are advantageous over OPAMPs since they require relatively less number of MOS devices [49].

3.2.2.2. Energy Efficiency

The power consumed by an OTA-C stage decreases with decreasing bandwidth [49]. Therefore, OTA-C filter is very desirable for the vestibular application as -3 dB bandwidths of the SCC and otolith transfer functions are very small; ~23 Hz and ~3.5 Hz, respectively. To keep power consumption small, the OTA of an OTA-C filter can be operated in subthreshold region. Operation in subthreshold is also advantageous since it can achieve the long time-constants of the vestibular neural dynamics through its very low transconductance values.

3.2.2.3. Area

To appreciate the area limitation, a 1st order OTA-C stage is considered (Figure 38(a)). Even the OTA is biased with a very small current value of 1 nA, to obtain a time-constant of 80 s, the capacitance value needs to be C= 1.54 µF. Using the poly-poly capacitors of the TI 0.35 µm technology, the C layout would cover an area of 1.6 mm x 1.6 mm. To overcome this issue, a switch that limits the effective output current of the OTA is used (Figure 38(b)) [58].

The switch is periodically turned on/off thereby limiting the output current, I_{OTA}, and creating an effective current of $I_{OTA,eff}=\gamma \cdot I_{OTA}$, where γ is the duty cycle of Φ, the clock

that controls the switch. As a result, very long time constants can be achieved. By varying γ, the pole-zero locations associated with that particular OTA-C element are controlled. This enables individual control over all pole/zero locations of the neural dynamics filters needed to fit patient-dependent parameters.

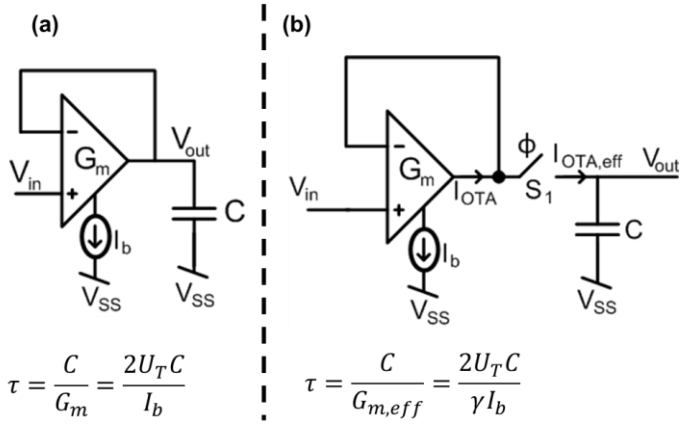


Figure 38. First order OTA-C filters. (a) Regular configuration. (b) A switch at the output limits the OTA current, thereby reducing the effective transconductance [58].

In actual design, besides the original OTA, there are two additional OTA stages employed in negative feedback. One of them serves as a buffer between two stages and the other serves as a path for I_{OTA} when the switch is off (Figure 39).

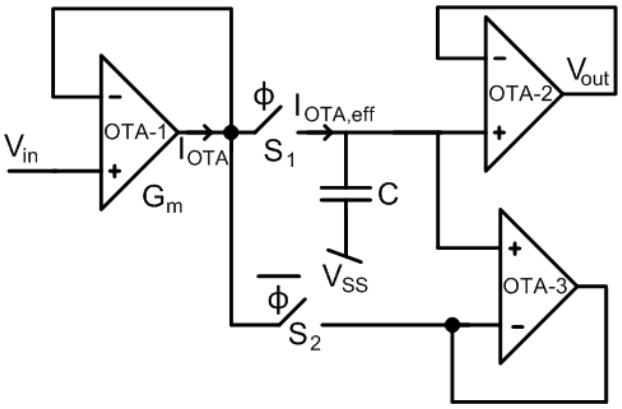


Figure 39. Actual implementation of the 1st order clocked transconductor OTA-C integrator.

The switches S_1 and S_2 are implemented as nMOS and pMOS devices, respectively. This way, the need for additional digital circuitry to synchronize the clock Φ and its inverse, namely $\overline{\Phi}$, is eliminated.

3.2.2.4. Input/Output Voltage Range

As transconductance elements, the filters utilize wide-range OTA architecture for its small number of elements as well as wide output range (Figure 40).

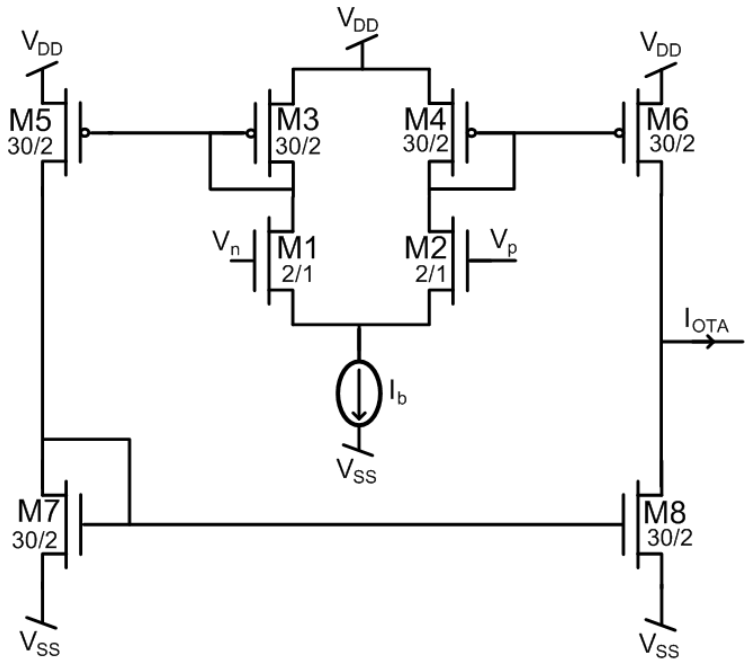


Figure 40. Wide-range OTA schematic. All OTAs of the filters are designed as wide-range OTAs. To improve the output impedance, current mirrors are cascode MOS devices.

Operating in the subthreshold region, OTA output current, I_{OTA}, is found as:

$$I_{OTA} = I_b \cdot tanh\left(\frac{\kappa(V_p - V_n)}{2U_T}\right), \quad (16)$$

where κ is the constant relating the gate voltage to channel potential for the input transistors M1 and M2; U_T, the thermal voltage; and $V_{in}=V_p-V_n$, the input differential voltage. To estimate the linear range value using (16), κ parameter for an nMOS fabricated with the 0.35 µm TI LBC7 process in subthreshold saturation region is extracted by performing a gate voltage sweep simulation (Figure 41).

With the estimated κ value of κ=0.66, the linear range, V_L, is found as V_L=±82 mV. Therefore, the output signal range of ±50 mV of the previous stage, namely the VMM, is within the limits of the V_L of the OTA.

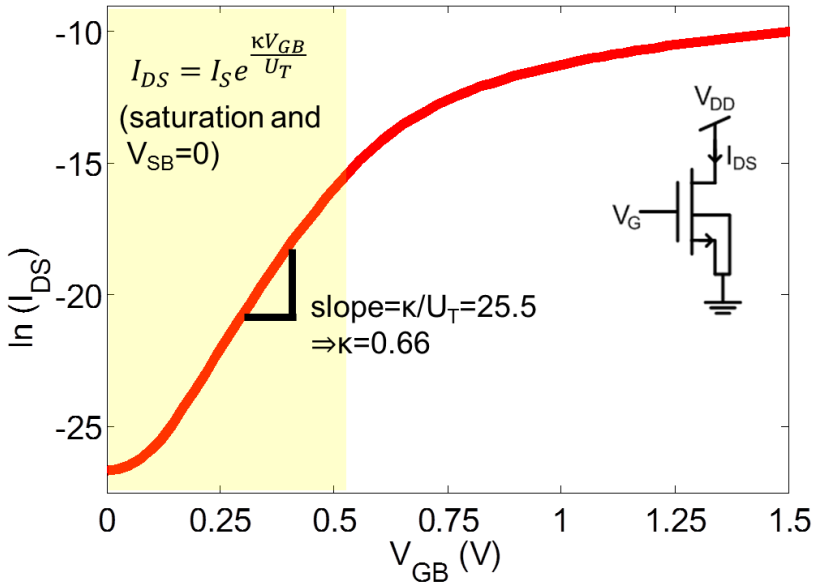


Figure 41. V_{GB} sweep simulation for an nMOS in 0.35 µm TI LBC7 process. *ln(I_{DS})* vs V_{GB} plot is used to extract the process-dependent κ value.

The output signal of the filter stage is amplified at an amplification stage to meet the input voltage range requirement of the next stage, namely the V-to-F. The amplification stage functions as a signal conditioning stage for the V-to-F and is explained in Section 3.3.3.5.

3.2.2.5. Noise

The noise of the filters affect the minimum detectable signal of the VMM, which in turn affects the sensation level thresholds of vestibular organs. To investigate the noise performance of the clocked OTA-C, a 1st order integrator noise performance is discussed below. It should be noted that, sampling of the switch results in aliasing, which increases the noise PSD at lower frequencies. However, sampling does not change the total noise power [59]. Therefore, an expression for the output noise power of a 1st order clocked

OTA-C integrator when the switch is ON obtained using the schematics in Figure 42, is valid when the noise is sampled by the switch. It is also noteworthy to mention that only devices along the signal path contribute to the signal noise power. Therefore, noise sources of S2 and OTA-3 in Figure 39 are not included in Figure 42.

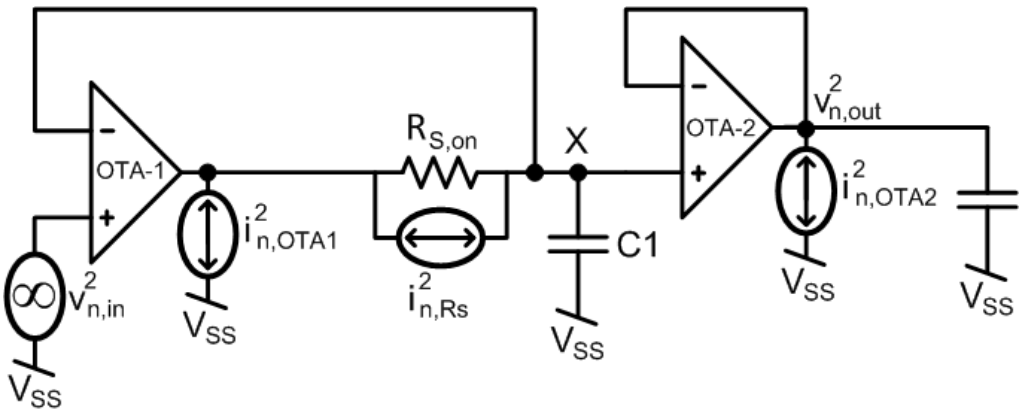


Figure 42. The LPF noise sources during the sampling phase.

To obtain an expression for the output voltage noise power, the following steps have been taken:

1. Output current noise PSD of OTA-1 and thermal noise current PSD of the switch resistance are reflected to the input of the OTA-1.

$$v_{n,in}^2 = \frac{i_{n,OTA1}^2 + i_{n,Rs}^2}{g_m^2}, \tag{17}$$

2. The noise power at the node X, namely $V_{n,X}^2$, is found by integrating the product of input-referred noise PSD found in step 1 and the transfer function from the input to the output node, over all frequencies. It should be noted that C_L is the gate capacitance of the following OTA stage. Because $C_1 >> C_L$, the dominant pole of the transfer function from the input to the output node is set by the time constant $C_1/g_{m,1}$:

$$v_{n,out1}^2 = \int_0^\infty \frac{v_{n,in}^2 df}{\left[1+\left(\frac{2\pi f C_1}{g_{m,1}}\right)^2\right]} = \frac{i_{n,OTA1}^2 + i_{n,Rs}^2}{4C_1 g_{m,1}}. \quad (18)$$

To calculate the integral in (18):

- MOS devices are assumed to contribute frequency-independent white noise only, which is a valid assumption based on [49]. To support the validity of that assumption, mirror transistors are sized as large MOS devices, which reduces their flicker noise.
- The output current noise PSD of the OTA in Figure 40 is the sum of current noise PSDs of all eight MOS devices. In subthreshold region, MOS white noise PSD is given as $i_n^2 = 2qI_{ds}$. Therefore, $i_{n,OTA1}^2 = 8\left(2qI_{b,1}/2\right) = 8qI_{b,1}$.
- Thermal current noise PSD of the resistor is $i_{n,Rs}^2 = 4kT/R_{S,on}$.

Therefore, an expression for $v_{n,out1}^2$ is obtained as:

$$v_{n,out1}^2 = \left(\frac{4}{\kappa} + \frac{8U_T}{\kappa I_{b,1} R_{S,on}}\right)\left(\frac{kT}{C_1}\right) \quad (19)$$

3. Output current noise PSD of the OTA-2 is reflected to its input node, namely the node X.

$$v_{n,X-OTA4}^2 = \frac{i_{n,OTA2}^2}{g_{m,2}^2} = \frac{8qI_{b,2}}{g_{m,2}^2}, \quad (20)$$

4. The voltage PSDs found in (17) is multiplied by the square of the transfer function from node X to the output node. The product is integrated over all frequencies to obtain an expression for the output noise power contribution of the OTA-2:

$$v_{n,out2}^2 = \int_0^\infty \frac{v_{n,X-OTA2}^2 df}{\left[1+\left(\frac{2\pi f C_L}{g_{m,2}}\right)^2\right]} = \frac{4}{\kappa}\left(\frac{kT}{C_L}\right) \quad (21)$$

5. The total output noise voltage power expression is equal to the sum of noise powers found in (19) and (21):

$$v_{n,out}^2 = \left(\frac{4}{\kappa} + \frac{8U_T}{\kappa I_{b,1} R}\right)\left(\frac{kT}{C_1}\right) + \frac{4}{\kappa}\left(\frac{kT}{C_L}\right) \quad (22)$$

From (22), it can be concluded that the noise performance of the switched OTA-C filter architecture improves as capacitance values are increased. Therefore, use of large capacitances to achieve long time-constants of the vestibular neural dynamics filters, and at the same, time improves the noise performance.

The aforementioned analyses show that with the selected filter architecture, the design criteria for implementing vestibular neural dynamics can be met. The design of the filters is explained in detail in the following subsection.

3.2.3. Design of the Vestibular Neural Dynamics Filters

To implement the higher-order neural dynamics transfer functions, 1st order OTA-C filters are cascaded. The high-frequency components of the signals associated with clocked operation, are removed at a three-cascaded 1st order low-pass filter stage, which is presented in Section 3.1.3.5.

Filter clocks are generated using the architecture presented in the Clock Generation Block explained in Section 2.1.1.2, which generates a pulse at the rising-edge of the input clock [60]. To reduce the total area, devices are sized smaller than the FPAA implementation. The schematic is redrawn in Figure 43(a) for convenience. The operation of the circuit is as follows. It is assumed that the initial condition for input and output is low. In that case the output is low and M1 acts as an ON switch, thereby making the node X high. When the input makes a low-to-high transition, the node Y goes high, thereby turning on the discharge path created by M2 and M3, as well as resulting in a low-to-high transition at the output. The potential of node X reduces proportionally to a speed set by the bias voltage, $V_{b,pw}$. When X becomes sufficiently low, the node Y makes a high-to-low transition, thereby turning off the discharge path, as well as resulting in a high-to-low transition at the output. The circuit enables precise control over the pulse-width (PW) of the output clock. For a range of $V_{b,pw}$ between $V_{b,pw}$=-90 mV and $V_{b,pw}$=-900 mV, the simulated pulses are shown in Figure 43(b). Based on simulations, PWs as short as 800 ps

can be generated. It should be noted that, increase in PW is achieved by increasing the time the discharge path remains on, which in turn increases the power consumption of the circuit. For instance, based on simulations, to generate pulse-widths of PW=2.6 µs and PW=86 µs, the circuit consumes 0.5 µW and 16.4 µW, respectively.

Below details of implementation of the transfer functions of the SCC and otolith neural dynamics are presented.

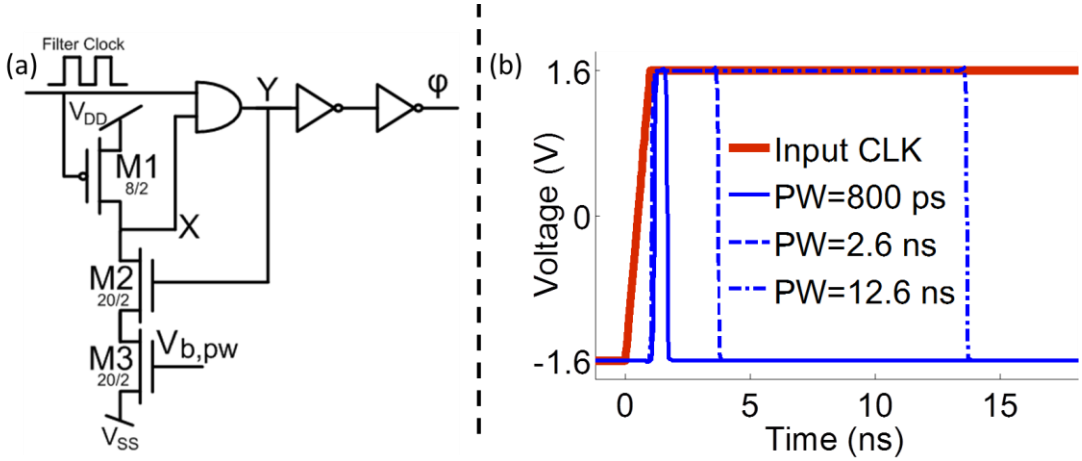


Figure 43. Clock generation circuitry. (a) Schematics. (b) PW control based on simulation results. PW=800 ps is obtained when $V_{b,pw}$=-90 mV.

3.2.3.1. SCC Filter

Based on animal studies, the transfer function associated with the SCC neural dynamics was given as (1) in the Section 1.1.1.2. The transfer function is decomposed into three 1st order filters; one low-pass (LPF) and two high-pass filters (HPF) as:

$$H_{SCC}(s) = (A_V \tau_1 \tau_A) \frac{1}{(1+\tau_2 s)} \frac{s}{(1+\tau_1 s)} \frac{s}{(1+\tau_A s)}. \quad (23)$$

In (23), typical values for the time constants are τ_1=4.37 s, τ_2=7 ms, and τ_A=80 s. It should be noted that (23) is derived from firing rate data obtained from animal vestibular neurons. However, the signals filtered here are not firing rate but rather rate sensor signals from the rate sensors, magnitudes of angular velocity or linear acceleration information. Therefore, the gain term in (23), namely A_V, is ignored when implementing the filters. The firing rate

gain is controlled at the block following the filters, namely the Voltage-to-Frequency block.

The first stage is the LPF. This way, LPF flicker noise is filtered at the following HPF stages. The continuous-time versions of the implemented OTA-C filters and their respective s-domain transfer functions are shown in Figure 44(a). In the actual implementation, the circuit in Figure 38(a) is modified to include buffer stages as well as the switches to control the output currents of OTA-1, OTA-2, and OTA-3. The schematic of the filter together with the high-frequency removal stage (HF-removal) at the output is shown in Figure 44(b).

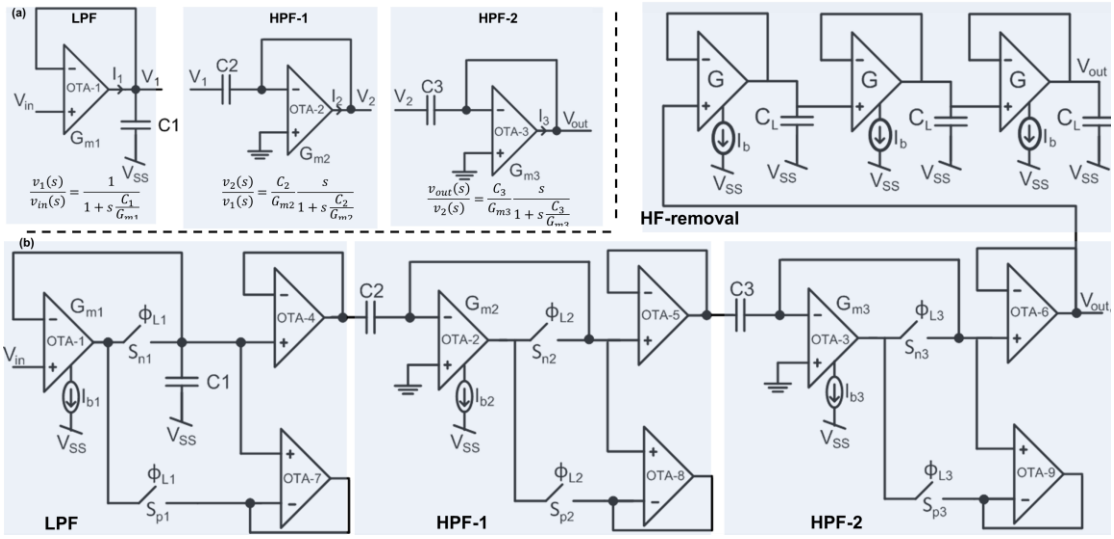


Figure 44. SCC neural dynamics filter schematics. (a) The simple OTA-C implementation of the SCC transfer function shown in (23). (b) The implementation of the SCC transfer function filter using clocked OTAs. The design includes switches and buffer stages.

Capacitance values are selected such that varying the pulse-width of the associated clock, a range of time-constants including the typical values from the biological experiments can be obtained for a reasonablsy low bias current value of 100 pA. It should be noted that, apart from the fact that the design area needs to be small, there is another reason why capacitances cannot be arbitrarily large; it is desired to keep the pulse-widths of the clocks small. This way, clock generation block power consumption is limited. The

capacitance values are presented in Table 5. For the case when the clock duty-cycle is varied between 0.5% and 30%, the calculated time constant ranges corresponding to the LPF, HPF1, and HPF2 are also presented in Table 5.

OTA-4 through OTA-9 are biased with relatively large currents (35 nA) to ensure a flat frequency response characteristics at the buffer stages. The parameters of the circuit are summarized in Table 5.

Table 5. SCC Filter Circuit Parameters and Time Constant Ranges

C1	10 pF
C2	250 pF
C3	1 nF
I_{b1}, I_{b2}, I_{b3}	1 nA, 100 pA, 100 pA
I_{b4}-I_{b9}	35 nA
$(W/L)_{Sn1-Sp3}$	0.9 µm / 0.4 µm
C_L	10 pF
I_b	1 nA
τ_{LPF}	1.7 ms – 104 ms
τ_{HPF1}	0.43 s – 26 s
τ_{HPF2}	1.7 s – 104 s

3.2.3.2. Otolith Filter

Based on animal studies, the transfer function associated with the otolith neural dynamics was given as (2) in the Section 1.1.2.2. The transfer function is decomposed into two stages; a pole-zero doublet and a LPF stage:

$$H_{oto}(s) = A_V \frac{1+k_A\tau_A s}{(1+\tau_A s)} \frac{1}{(1+\tau_M s)}. \quad (24)$$

In (24), typical values for the time constants are $k_A\tau_A$=13.2 s, τ_A=11 s, and τ_M=46 ms. The continuous-time versions of the implemented OTA-C filters and their respective s-domain transfer functions are shown in Figure 45(a). In the actual implementation, buffer stages as well as the switches to control the output currents of the OTA-1, OTA-2, and OTA-3 are added to the circuit. The schematic of the filter together with the high-frequency removal stage (HF-removal) at the output is shown in Figure 45(b).

Capacitance values, which are presented in Table 6, are selected following the same line of reasoning explained in the SCC filters section. For the case when the clock duty-cycle is varied between 1% and 10%, the calculated time constant ranges corresponding to the pole-zero doublet and the LPF are also presented in Table 6. All bias currents, capacitances, and the switch dimensions are presented in Table 6. The clocks Φ_1, Φ_2, and Φ_3 are generated externally. By varying the pulse width of each clock, locations of both poles and the zero are controlled.

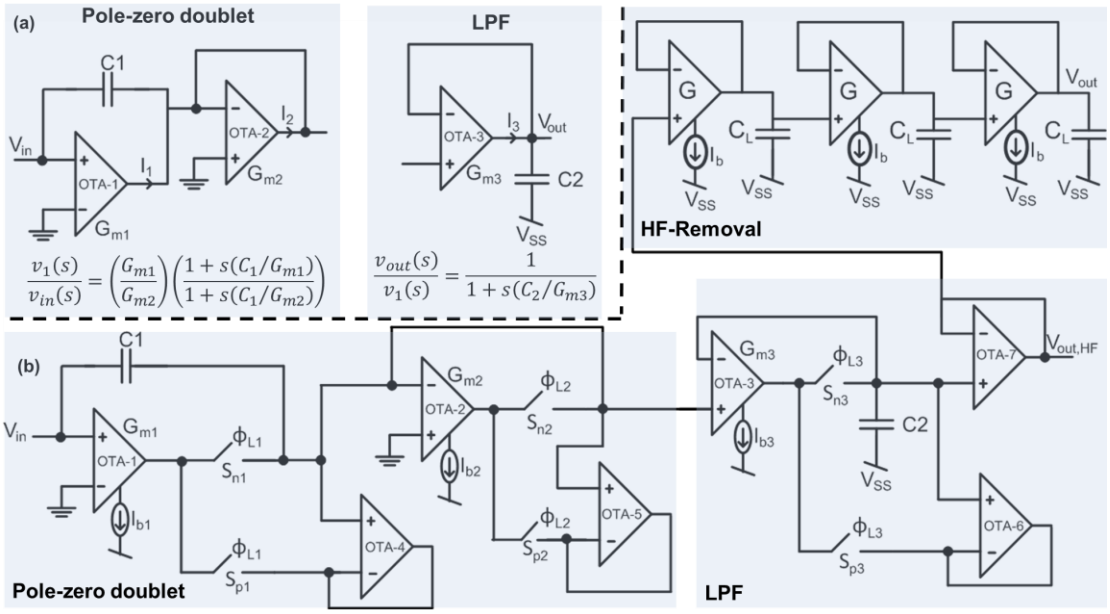


Figure 45. Otolith neural dynamics filter schematics. (a) The simple Gm-C implementation of the otolith transfer function shown in (20). (b) Actual implementation of the SCC transfer function filter using clocked OTAs.

Table 6. Otolith Filter Circuit Parameters and Time Constant Ranges

C1	800 pF
C2	20 pF
I_{b1}, I_{b2}, I_{b3}	100 pA, 100 pA, 1 nA
I_{b4}-I_{b7}	35 nA
$(W/L)_{Sn1-Sp3}$	0.9 µm / 0.4 µm
C_{HFrm}	10 pF
$I_{b,HFrm}$	1 nA
τ_A - $k_A\tau_A$	4.16 s – 41.6 s
τ_{LPF}	10.4 ms – 104 ms

In the next subsection, the measurement results of the filters are presented.

3.2.4. Measurement Results

The filter stage is fabricated with the TI 0.35-µm 3P2M n-well CMOS process. Two versions of the SCC filter is designed, namely SCC-v1 and SCC-v2. Designed for characterization purposes, SCC-v1 is fed with externally generated clock sources. The clocks of the SCC-v2 are generated internally by the clock generation block, based on their respective bias voltages. The otolith filter is fed with externally generated clocks. In Figure 46, the optical images and the floor plans of the filters are shown. The footprints of the SCC-v1, SCC-v2, and otolith filters are 1.3 mm x 1.14 mm, 1.42 mm x 1.14 mm, and 1.34 mm x 1 mm, respectively.

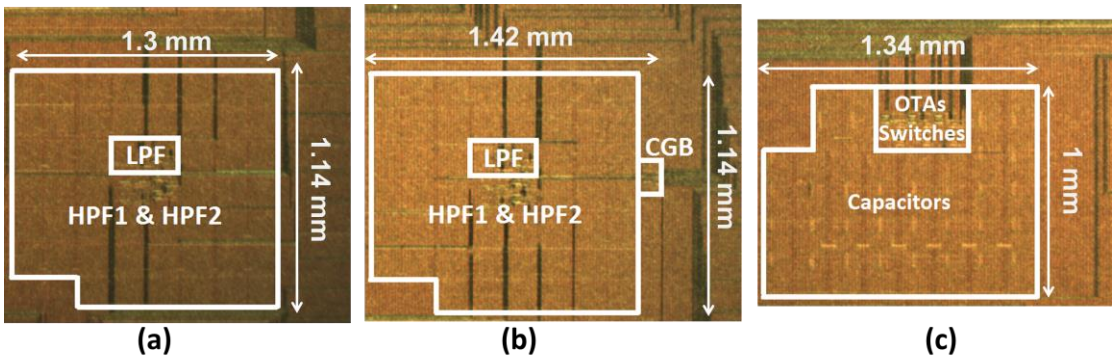


Figure 46. Filter floor plans. (a) SCC-v1. (b) SCC-v2. (c) Otolith.

3.2.4.1. Testing Procedure

The test-bench schematic is shown in Figure 47. All bias currents are generated externally using the bias generation circuitry explained in Section 3.1.4.1.

The functionality tests of each stage of the filters are performed on the SCC-v1 and the Otolith Filter dies. Each stage of the filters is supplied with a 100 mV_{pp} sinusoidal signal representing the VMM output signal. Then, the output signal magnitude of each stage is measured. To obtain the gain plot corresponding to a stage, the frequency of the input signal is swept over a frequency range where the pole/zero lies within. The number of sweep

points is ~10 for each sweep measurement. To observe the pole/zero location control, the sweep measurements are repeated for different clock pulse-widths (PW).

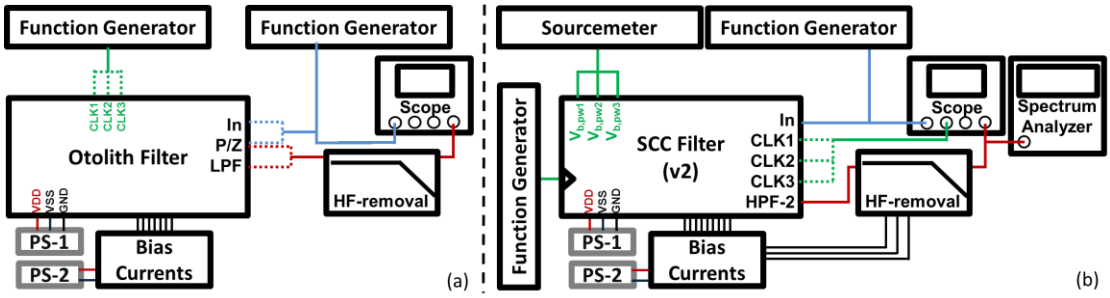


Figure 47. Filter Test-bench Schematics. (a) For ease of characterization, SCC-v1 and otolith filter use externally generated clocks. For simplicity, the schematics is drawn for the case only the otolith filter is under test. (b) Clocks are generated internally at SCC-v2.

From the tests of each stage of the SCC-v1, the clock pulse-widths that match the poles of the SCC filter with the values obtained by the clinical studies are found. Then on the SCC-v2 die, the clock generation circuitry bias voltages that generate the corresponding pulse widths are found by observing the CLK1-CLK2-CLK3 on the scope. The SCC-v2 is supplied with corresponding bias voltages and the gain plot of the complete filter is obtained when the frequency is swept from 0.6 mHz to 80 Hz using 18 data points. The gain plot of the complete Otolith Filter is performed on the Otolith Filter die by performing a frequency sweep from 1 mHz to 20 Hz using 13 points.

SCC-v2 represents a complete filter stage. Therefore, noise measurements are performed only on the SCC-v2 filter. To investigate the minimum detectable signal at the input, total output voltage noise power, namely $v_{n,tot}^2$, is measured at the output of the HF-removal filter when the input is grounded. The filter has a bandwidth less than 100 Hz. Therefore, $v_{n,tot}^2$ is measured using PSD for frequencies less than 100 Hz. The minimum detectable signal, $v_{mds}(f)$, is then found by calculating the signal magnitude that gives a signal-to-noise ratio of 1 at the output [49]. Therefore, at a certain frequency f, $v_{mds}(f)$ is calculated as:

$$v_{mds}(f) = \sqrt{\frac{v_{n,tot}^2}{A_V^2(f)}}, \tag{25}$$

where $A_V^2(f)$ is the gain of the filter at that particular frequency f. The v_{mds} calculation is made for frequencies within the pass band, where most normal head motions lie.

3.2.4.2. Functionality

SCC Filter

SCC-v1 is supplied with externally generated clocks to verify adjustability of pole locations. The gain plots of the LPF, HPF-1, and HPF-2 are shown in Figure 48(a), (b), and (c). The -3dB pole locations and their corresponding PW values are presented within the plots.

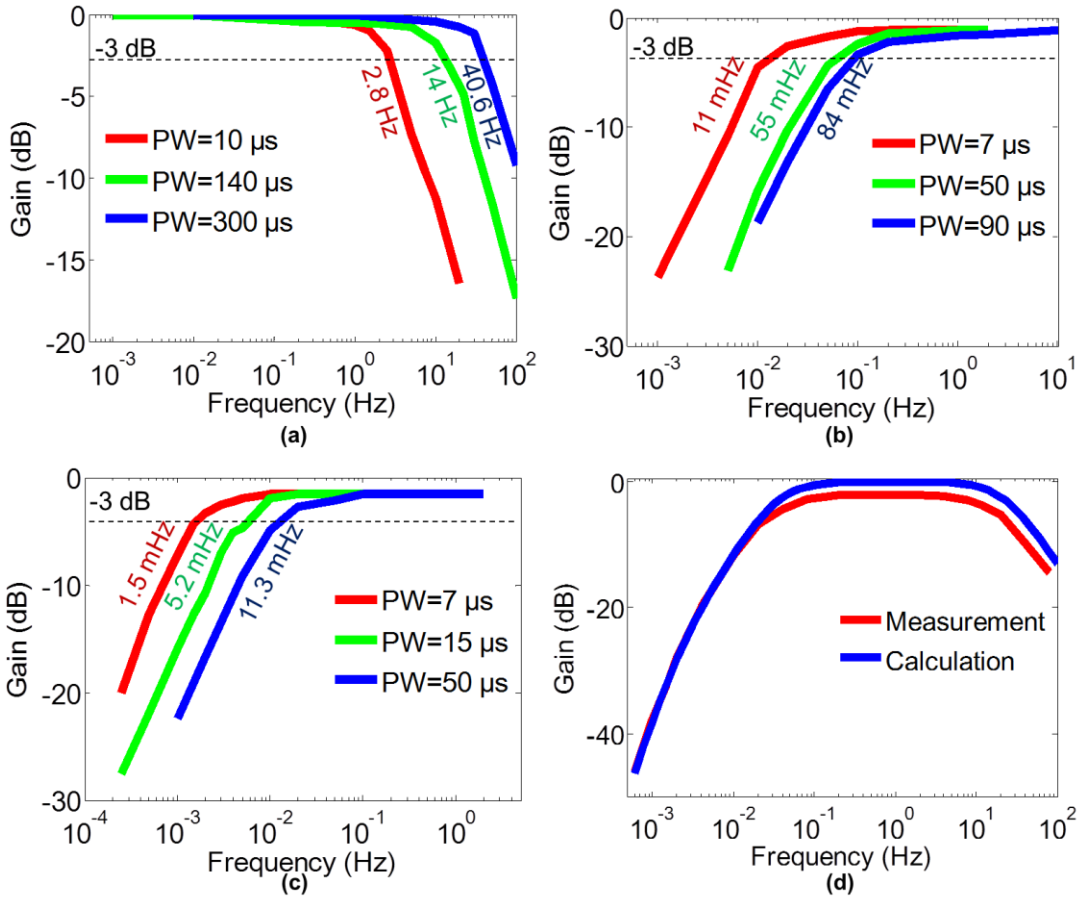


Figure 48. SCC neural dynamics filter measurements. (a) LPF measurements (b) HPF-1 measurements (c) HPF-2 measurements. (d) The complete transfer function measurements.

The functionality of the whole filter is verified by generating the clocks internally on SCC-v2. For the bias current values in the Table 5 and clock PWs of $PW_{\Phi 1}$=20 µs and $PW_{\Phi 2}$= $PW_{\Phi 3}$=10 µs, the poles match closely with the SCC transfer function calculated using typical τ_A, τ_1, and τ_2 values (Figure 48(d)). The clock generation circuitry bias voltages corresponding to $PW_{\Phi 1}$ and $PW_{\Phi 2}$= $PW_{\Phi 3}$ are $V_{b,pw1}$=-1.34 V and $V_{b,pw2\text{-}3}$=-1.23 V, respectively.

Otolith Filter

The otolith filter is supplied with external clocks. Varying the PWs of clocks, pole/zero locations are controlled. The gain plots of the pole-zero doublet and LPF stages are shown in Figure 49(a) and (b). The PW values and the corresponding time constants are presented within the plots. The transfer function observed at the otolith organs is obtained when $PW_{\Phi 1}$=40 µs, $PW_{\Phi 2}$=43 µs, and $PW_{\Phi 3}$=75 µs (Figure 49(c)).

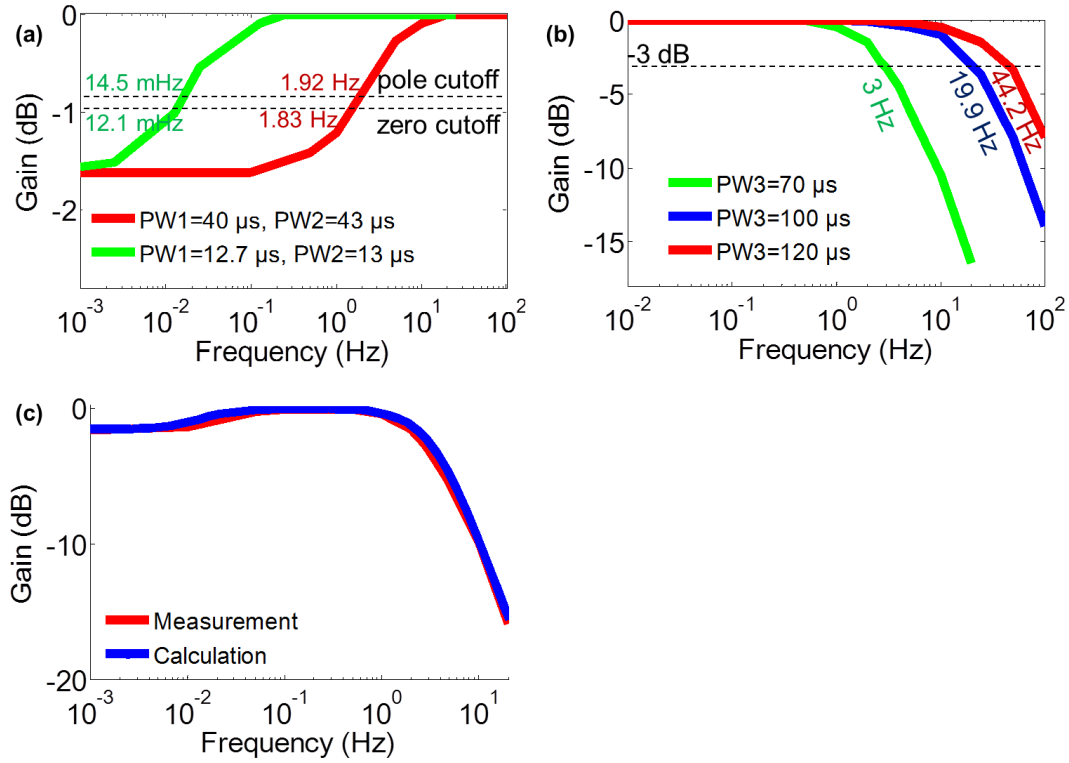


Figure 49. Otolith neural dynamics filter measurements. (a) Pole-zero doublet stage measurements. (b) LPF measurements. (c) The complete transfer function measurements.

3.2.4.3. Noise

The PSD of the output voltage noise for the frequency range of interest (f<100 Hz) is shown in Figure 50. From the PSD, total output voltage noise power is found as, $v_n^2 = 4.7 \cdot 10^{-8}$ V^2/Hz. From (25), for signals within the bandpass frequencies of the filter, where the gain is ~0.78 V/V, the minimum detectable signal is found as $v_{mds} = 279\ \mu V$.

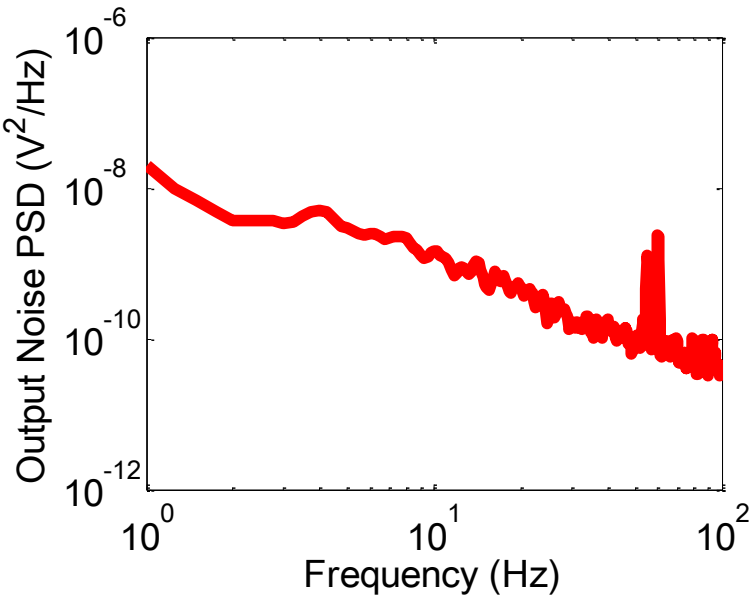


Figure 50. Output voltage noise PSD of the SCC filter.

3.2.4.4. Power

The total power consumptions of the SCC-v2 and the otolith filters are measured as 6.96 µW and 1.2 µW for the bias current values presented in Tables III and IV, respectively. Power consumption is more in the SCC-v2, which is attributed to the internal clock generation circuitry as well as the larger number of OTAs.

3.2.5. Discussion

Low-power filters implementing the SCC and the otolith neural dynamics are presented and the performance parameters are summarized in Table 7. In the literature, three VP prototypes implement the neural dynamics. In [21] and [27], the implementations

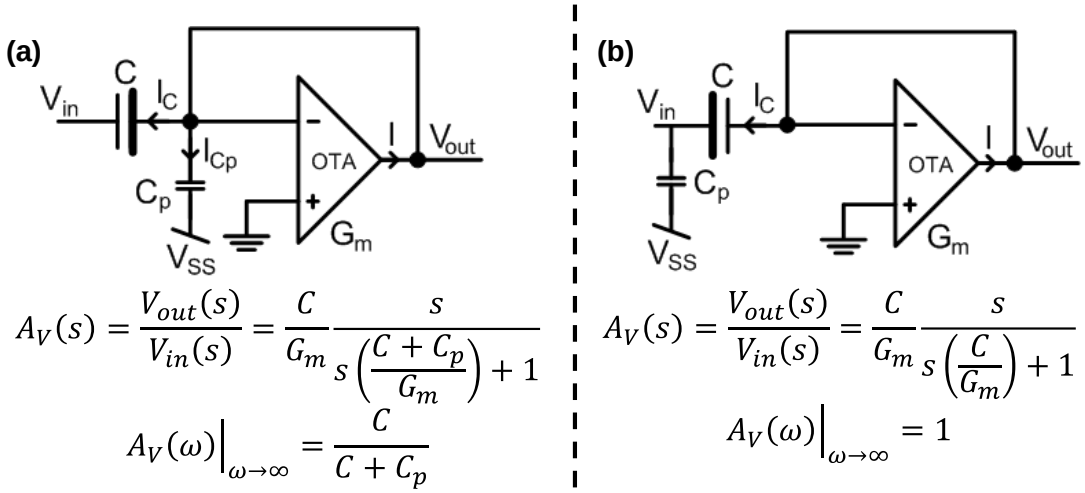
Table 7. Summary of Performance Parameters of the Neural Dynamics Filters

Property	**This Work (SCC)**	**This Work (Otolith)**	**2008 [20]**
Technology	0.35 µm CMOS	0.35 µm CMOS	0.35 µm CMOS
Functions	Single SCC	Single Otolith	Single SCC
Power	6.96 µW	1.2 µW	<48.84 µW (simulated)
Input/output voltage range	±50 mV / ±39 mV	±50 mV / ±50 mV	N/A
Time Constant Range	3.92 ms - 106 s	3.6 ms – 13.2 s	N/A
Noise ($v_{n,in}$)	279 μV_{rms}	N/A	N/A
Minimum detectable acceleration/angular velocity	3.95 deg/sec	N/A	N/A
SNR	42 dB	N/A	N/A
Clock Frequency	1 kHz	1 kHz	10 kHz
Area	~2.4 mm^2	~1.35 mm^2	<~1 mm^2

are performed in digital domain using microprocessors, whereas in [20], an ASIC that makes use of switched-capacitor filters to implement the neural dynamics. To make a meaningful comparison, the filters presented in this work are compared with only the ASIC presented in [20]. The comparison is presented in Table 7. It should be noted that, the circuit in [20] performs capacitor-to-voltage and voltage-to-current conversions besides implementing the neural dynamics. Therefore, the dimension and the simulated power values in [20] reflect upper-bounds.

The filters presented offer a wide range of tunable time constants while consuming less than 7 µW of power. Based on the area of single SCC and otolith filters, the total area for three SCCs and two otoliths is estimated as 9.9 mm^2.

It should be noted that, high frequency gains of the HPFs of the SCC filter are less than 0 dB (-2.16 dB). The reduction in gain is contributed to the parasitic capacitance between the bottom plate of the capacitors and the p-substrate, which is connected to V_{SS}. To see the effect of parasitic capacitance on gain, the schematics of a simple Gm-C implementation of the HPF stage with bottom plate of the capacitance C is connected to V_{out} is shown in Figure 51(a). At the output node, the parasitic capacitance C_p creates a current path to V_{SS}, thereby reducing the gain. The reduction in the gain is compensated up to a certain point at the signal-conditioning amplifier stage of the V-to-F Block. In the future version of the design to eliminate the attenuation due to the parasitic capacitance, the bottom plate of the capacitor can be connected to the input node as shown in Figure 51(b).



$$A_V(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{C}{G_m} \frac{s}{s\left(\frac{C + C_p}{G_m}\right) + 1}$$

$$A_V(\omega)\Big|_{\omega \to \infty} = \frac{C}{C + C_p}$$

$$A_V(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{C}{G_m} \frac{s}{s\left(\frac{C}{G_m}\right) + 1}$$

$$A_V(\omega)\Big|_{\omega \to \infty} = 1$$

Figure 51. The effect of bottom-plate parasitic capacitance, C_p, on the gain of the HPF stage. (a) Because the bottom-plate (thick plate on the schematics) is connected to V_{out}, the maximum gain is less than 1. (b) To eliminate the effect of C_p, the bottom plate should be connected to V_{in}.

To reduce the minimum detectable signal angular velocity, the noise performance of the filters can be improved by increasing the input MOS device sizes of the OTAs, thereby reducing the flicker noise. To reduce the flicker noise further, the OTA architecture can be changed from nMOS-input to pMOS-input.

3.3. Voltage-to-Frequency Block

Neurons carry information by means of pulses. Research on the vestibular system shows that SCC and otolith neurons encode angular velocity and linear acceleration information into pulse rates, respectively. Earlier in this work, it was discussed that the relationship between the head motion (either angular or linear) and the vestibular neurons' firing rate has an asymmetric sigmoid relationship. In Figure 52 firing-rate data obtained from SCC and otolith neurons are plotted (Redrawn from [61],[11]). It should be noted that among different neurons, the values of the parameters that define the sigmoid firing rate-head motion relationship vary, which is illustrated by presenting data obtained from three different otolith neurons in Figure 52(b)[11]. The VP signal processing circuitry needs to perform the transformation from head motions to firing rate frequencies based on biological data. Given that the output signals of the Neural Dynamics Filters stage is voltage, a voltage-to-frequency block (V-to-F) is designed. The rate-modulated pulses generated by the V-to-F can be used to drive an H-Bridge current stimulator that generates biphasic current pulses to stimulate the vestibular neurons.

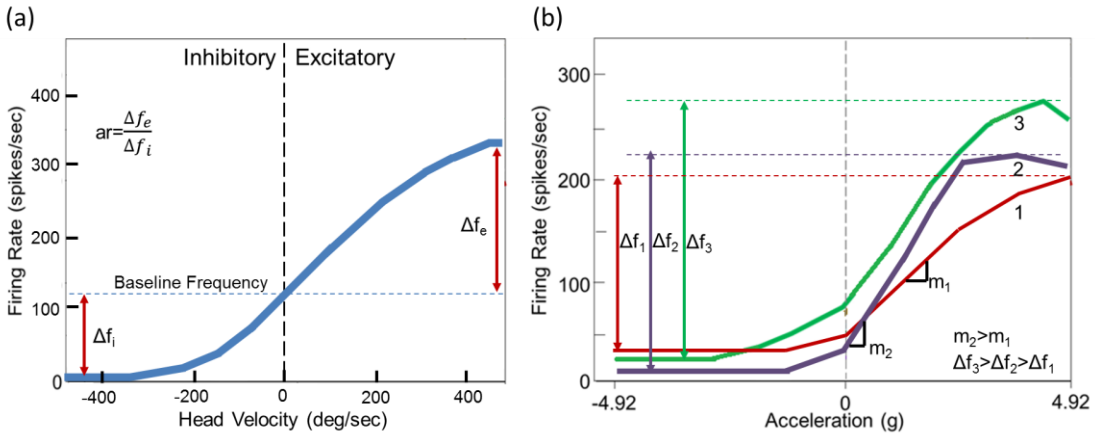


Figure 52. Firing rate angular velocity/linear acceleration relationship. (a) Data from an SCC neuron (Redrawn from [56]) Baseline frequency is the neuron firing rate when there is no head motion. The asymmetry ratio, *ar*, is defined as the ratio of firing rate spans of excitatory and inhibitory head motions. (b) Data from otolith neurons (redrawn from [11]). Three plots correspond to different otolith neurons. The firing rate ranges, *Δf*, and the gains, *m*, of the curves are different.

As shown in Figure 52, four parameters define the curves; namely the baseline frequency, the firing rate range, the asymmetry ratio, and the gain. Values of those parameters vary from neuron to neuron and thus patient to patient. Therefore, the V-to-F needs to enable tuning of them, which is one of the design parameters of this block. All design parameters of the V-to-F are presented in the following subsection.

3.3.1. Design Considerations

Three design criteria have been considered when designing the V-to-F. These include (1) achieving sigmoid frequency vs. voltage relationship with tunable parameters in an energy-efficient manner, (2) input voltage range, and (3) noise. Below details of why those parameters are important for the V-to-F is presented.

(1) The variation in the values of the four parameters; namely the baseline frequency, firing rate range, asymmetry ratio, and the gain; that define the sigmoid curves among different vestibular neurons was mentioned above. Values of them differ from patient to patient as well. Therefore, a V-to-F that enables control over those parameters could be employed to best mimic the vestibular firing rate characteristics of that particular patient. Additionally, the V-to-F needs to be energy-efficient as it is designed for an implant system.

(2) The input voltage range of the V-to-F needs to match with the output voltage range of the Neural Dynamics Filters Block.

(3) Noise performance of the V-to-F affects the minimum detectable angular velocity/linear acceleration values of the VP. Essentially the V-to-F is an oscillator and the noise of an oscillator causes variation in the phase of the output clock, which results in fluctuations in the frequency.

Considering the aforementioned design considerations the blocks constituting the V-to-F has been determined from a system-level perspective. The procedure is discussed in the following subsection.

3.3.2. System-Level Design of the V-to-F

3.3.2.1. Achieving Sigmoid Frequency vs. Voltage Relationship with Tunable Parameters in an Energy-Efficient Manner

Based on the biological data presented above, the first function that the V-to-F needs to implement is introduction of a sigmoid function. The sigmoid function needs to be asymmetric about the x-axis and the degree of asymmetry as well as the linear region gain, max/min values, and dc offset values of the sigmoid function are to be tuned.

It should be noted that a sigmoid function can be implemented in an energy-efficient way. By utilizing an OTA in subthreshold region, its output current is related to the input voltage through a *tanh* function. The bias current of the OTA sets the maximum/minimum values of the output current, which are also the asymptotic maximum/minimum values of the *tanh* function. If a linear-range control circuit that is complementary to the OTA is designed, the linear-region gain of the OTA, and therefore that of the *tanh* function can be tuned.

To introduce asymmetry to the sigmoid function, as well as to control the DC offset and degree of asymmetry, additional analog signal processing circuitry is designed. It should be noted that, there are two reasons why a current-mode signal processing is desired to implement those functions; one is that the OTA already generates a current signal and the other is that doing the signal processing in the current mode is natural when implementing remaining functions is considered. For instance, current-mode addition, which is used to add DC offset, does not require any complex circuitry as it is implemented simply by forming a node with all current carrying lines to be added. Similarly, introducing asymmetry to the sigmoid function is a straightforward process in current-mode signal processing; it only requires addition of currents that are weighed with different constants at non-identical current mirrors.

The second function that the V-to-F implements is frequency modulation. A current-controlled oscillator is designed to convert the current output from the previous stage into frequency. For its linear frequency-current relationship and ability to generate the frequencies of interest (f_{out}<~600 Hz) with current values in the order of nA, an integrate and fire circuit, which was first presented in [35], is selected as the current-controlled oscillator architecture.

The V-to-F is designed to control the switches of an H-Bridge circuit that generates biphasic current pulses to stimulate neurons. A pair of out-of-phase clocks are generated to control an H-Bridge. These clocks are generated by cascading three glitch circuits. The output generates a pulse at the falling-edge of the input clock.

3.3.2.2. Input Voltage Range

The input signal of the V-to-F is the Neural Dynamics Filter output voltage, which has an output voltage range of ±50 mV. That voltage range is not large enough to meet the input voltage range requirement of the linear-range control circuitry assisted OTA. Therefore, a variable-gain amplifier is designed to serve as the signal conditioning stage for the V-to-F.

3.3.2.3. Noise

The noise performance of the V-to-F is contingent upon how the transistors and other circuit elements are sized. By making use of current-mode signal processing techniques, the number of active elements that contribute to noise is reduced. This way, power consumption is also lowered.

In the next subsection, the details of the blocks constituting the V-to-F are described.

3.3.3. Design Details of the V-to-F

The sub-blocks constituting the voltage-to-frequency stage are shown in Figure 53.

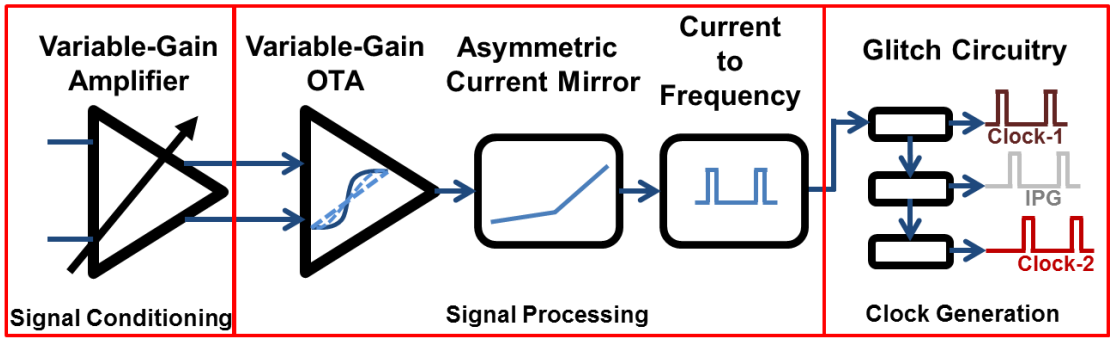


Figure 53. Voltage-to-Frequency Block Diagram.

The design details are presented in the following order: First, the Signal Processing and the Clock Generation Blocks are explained. Then, the variable-gain amplifier (VGA) is presented, which is designed based on the design requirements of the Signal Processing Blocks.

3.3.3.1. Variable-Gain OTA

An OTA in subthreshold region has an output current-differential input voltage relationship described by a *tanh* function [35]. For the wide-range OTA shown in Figure 53, the output current, I_{out}, is related to input differential voltage, V_{in} through:

$$I_{out} = I_b \cdot tanh\left(\frac{\kappa(V_2 - V_1)}{2U_T}\right), \tag{26}$$

where I_b is the bias current controlled by the bias voltage, V_b. In (26), linear region transconductance gain is fixed and set by; κ, the constant relating the gate voltage to channel potential for the input transistors M1 and M2; U_T, the thermal voltage; and $V_{in}=V_2-V_1$, the input differential voltage. The linear range of the OTA, V_L, is fixed and found as $V_L=\pm 82$ mV in Section 3.2.2. For a fixed bias current, I_b, the linear-region gain is also fixed:

$$G_m = \frac{\kappa I_b}{2U_T}, \tag{27}$$

The need for obtaining variable-gain sigmoid curves is mentioned in Section 3.3.1. To control the gain of the *tanh* curves, V_{in} is attenuated at an attenuation stage, which consists of a differential pair in deep inversion region with a diode-connected load in subthreshold region (Figure 54) [48].

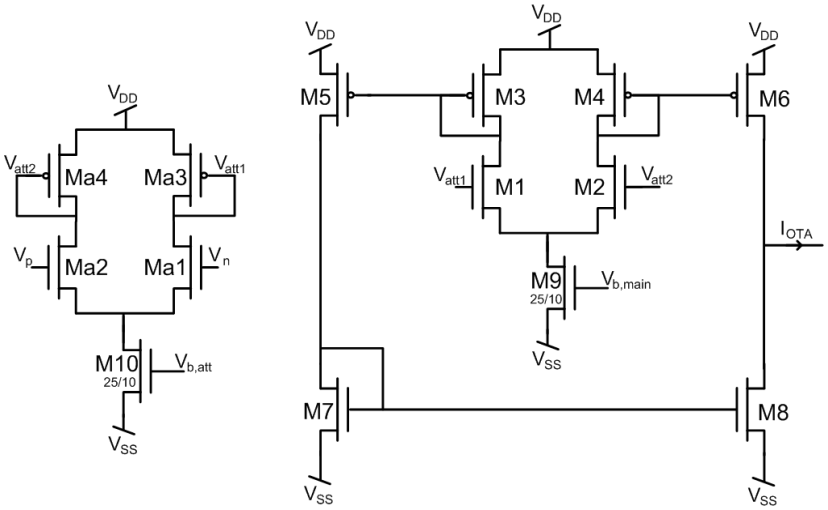


Figure 54. Variable-gain OTA.

The attenuation stage functions as a small-signal voltage divider. The difference between the transconductances of a MOS in subthreshold and deep inversion regions creates a bias-current-dependent attenuation factor. This way, I_{out}-V_{in} relationship in (26) becomes:

$$I_{out} = I_b \cdot tanh\left(\frac{\alpha\kappa(V_2 - V_1)}{2U_T}\right). \tag{28}$$

The gain expression for the variable-gain OTA is found by multiplying wide-range OTA gain that is given in (27) by the attenuation factor in (28), α, that is dependent on the bias current of the attenuation stage, $I_{b,att}$, as:

$$G_{m,att} = \alpha \cdot G_m = \left[-\frac{2U_T}{\kappa}\sqrt{\frac{K(W/L)_{Ma1}}{I_{b,att}}}\right] \cdot \left(\frac{\kappa I_b}{2U_T}\right), \tag{29}$$

where K is the transconductance parameter, which is a function of mobility and unit gate-oxide capacitance, and $(W/L)_{Ma1}$ is the aspect ratio of transistor Ma1.

It should be reemphasized that, (29) is valid only when Ma1-Ma2 and Ma3-M4 are in deep inversion and subthreshold regions, respectively. This condition limits the values $I_{b,att}$ can take, which creates a lower and an upper bound for α. As the variable-gain OTA input voltage range corresponds to angular velocity/linear acceleration range of normal head motions, the boundary values of α are particularly important in determining the input voltage range of the variable-gain OTA. The input voltage range needs to ensure that the *tanh* curves obtained with the possible values of α are steep enough to match well with the sigmoid curves obtained based on the biological data. To calculate an input voltage range satisfying that criterion, following steps are taken:

1. The α range; which is set by the $I_{b,att}$ range that keeps Ma1-Ma2 and Ma3-M4 in deep inversion and subthreshold regions, respectively; is determined based on the inversion boundary assumptions [62]:

$$I_{D,Ma1} > 10\, I_S \Rightarrow \text{deep inversion}$$
$$I_{D,Ma3} < 0.1\, I_S \Rightarrow \text{weak inversion,} \tag{30}$$

where $I_{D,Ma1}$ and $I_{D,Ma3}$ are the drain currents of transistors Ma1 and Ma3, respectively; and I_S is the moderate inversion characteristic current:

$$I_S = \frac{2KU_T^2}{\kappa} \cdot \frac{W}{L}. \tag{31}$$

Based on the assumption that $I_{b,att} \cong 2xI_{D,Ma3}$ and $I_{b,atts} \cong 2xI_{D,Ma1}$, and substituting (31) and the α term in (29) into (30), the range for α is found as:

$$\frac{\sqrt{10}}{\sqrt{\kappa}} \sqrt{\frac{(W/L)_{Ma1}}{(W/L)_{Ma3}}} < |\alpha| < \left|\frac{1}{\sqrt{10\kappa}}\right|$$
$$4\sqrt{\frac{(W/L)_{Ma1}}{(W/L)_{Ma3}}} < |\alpha| < 0.4, \tag{32}$$

which suggests α cannot exceed 0.4. The minimum value for α is a function of the aspect ratio of Ma1 to Ma3, $(W/L)_{Ma1}/(W/L)_{Ma3}$.

2. The linear range of the variable gain OTA for α=0.4 is found as, V_L=±197 mV. Similarly, the linear range of a sigmoid curve from biological data is found. The

curve used as the biological data is the mathematical expression presented in [63], which is an approximation of the sigmoid curves obtained from biological experiments. It should be noted that only linear region gain of the curve is important in calculating the OTA input range. Therefore, the parameters that model the asymmetry in the original expression in [63] are removed and the magnitude is normalized to 1. The expression is further modified to change its input variable from 12-bit digitized angular velocity to angular velocity, ω. Therefore the expression of the curve from biological experiments becomes:

$$f = tanh\left(2\left(\frac{\omega}{493}\right)\right). \tag{33}$$

The linear range of the curve in (33) is, $V_{L,bio}$=±246.5 deg/sec. For the curves from OTA and biology to overlap, the input range of the OTA is calculated as ±400 mV. To enable the possibility of obtaining steeper curves than the sigmoid curve of the (33), input range of the OTA is increased to ±500 mV. To visualize the results, the OTA I_{out} vs V_{in} curve corresponding to α=0.4 and the curve from biology in (33) are plotted as shown in Figure 55.

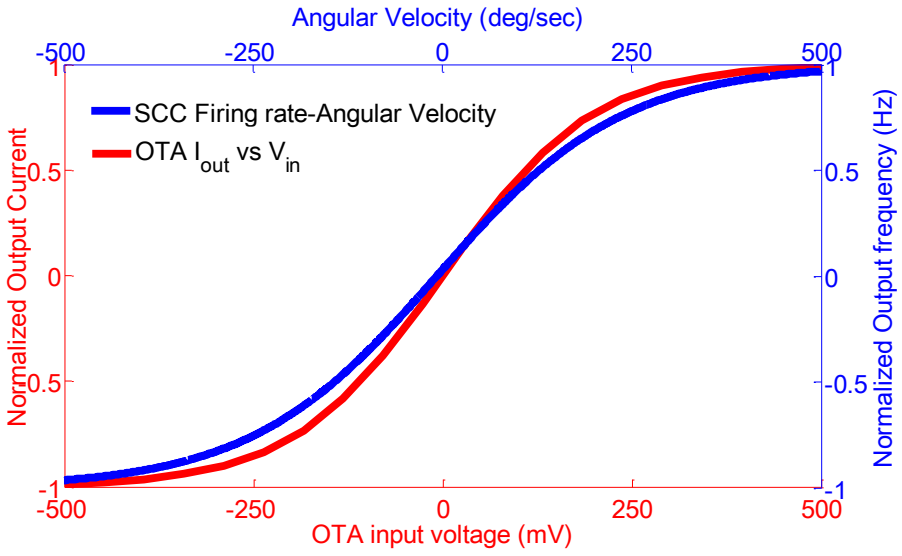


Figure 55. The sigmoid firing rate-head angular velocity relationship based on (33) and the *tanh* curve calculated based on (28) for the maximum attenuation factor of α=0.4, when the input voltage range is ±500 mV.

The devices are sized as follows: (1) To allow a wide-range of attenuation factor, the ratio of the sizes of Ma1 (=Ma2) to Ma3 (=Ma4) is kept very small ($(W/L)_{Ma1} = 1/100$ and $(W/L)_{Ma3} = 200/1$), thereby setting the lower bound for the attenuation factor at α=~0.03 based on (32). (2) To ensure subthreshold operation of M1 and M2 for a wide range of bias currents (I_b<~3 µA), M1 and M2 aspect ratio is large, $(W/L)_{M1,M2} = 20/3$. Large gate area of M1 and M2 reduces their flicker noise contributions. (3) To reduce the effect of channel-length-modulation when operating in moderate or deep inversion, M9 and M10 are sized as long devices; $(W/L)_{M9,M10} = 25/10$. (4) Lastly, current mirrors are cascoded structures with large device sizes to reduce the mirroring errors and flicker noise, $(W/L)_{M3-M8} = 30/2$.

When the design is simulated for V_b =-1.32 V and $V_{b,att}$ varying between -1.15 V and -1.4 V, the control of gain for a fixed bias current is verified. It should be noted that, even the input voltage range is reduced from ±500 mV to ±300 mV, it is possible to obtain curves steeper than the curve based on biological data (Figure 56). In fact, the attenuation factor of the steepest curve in Figure (56) is found as α=1.125 based on (28), which is higher than the calculated value of 0.4 in (32). Therefore it is concluded that, based on simulations, Ma1 and Ma2 are concluded to remain in deep inversion region for $I_{D,Ma1} > 1.2\, I_S$. Because the simulator makes use of process dependent estimates of the inversion boundaries as opposed to the generic estimates presented in (30), input voltage range is reduced to ±300 mV based on simulation results.

The bandwidth of the variable-gain OTA is limited by the dominant-pole at the output node. It should be noted that, the output of the OTA is connected to the gate of a series of pMOS current mirrors and the drain of an nMOS device of the Asymmetric Current Mirror Block (Figure 57 (a)). The frequency response is found as:

$$\frac{v_X(s)}{v_{in}(s)} = \frac{G_{OTA}/g_{Ma}}{1+sC_{out}/g_{Ma}}, \tag{34}$$

where $G_{OTA} = \alpha\kappa I_{b,main}/2U_T$ and $g_{Ma} = \kappa I_1/U_T$. From (34), -3 dB frequency is $f_{-3dB} = g_{ma}/(2\pi C_{out})$. Based on simulations, $f_{-3dB} = \sim 4\,kHz$, thereby ensuring a flat characteristics for frequencies of interest (<20 Hz) (Figure 57(b)).

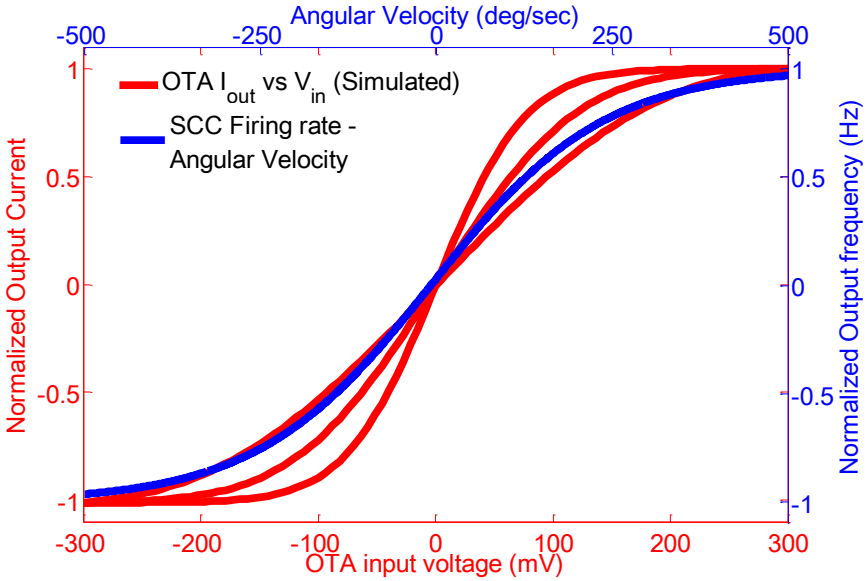


Figure 56. The sigmoid firing rate-head angular velocity relationship based on [6] and the *tanh* curves based on simulation results of the variable gain OTA designed.

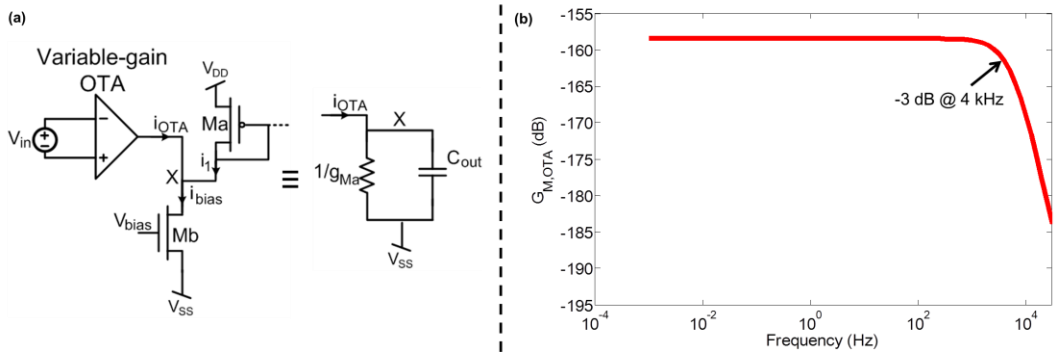


Figure 57. Variable-gain OTA frequency response. (a) The schematic showing the connections at the output node of the OTA and its small signal equivalent. (b) Simulation result.

To find an expression for the total output voltage noise power, first the output current noise PSD, $i_{n,OTA}^2$, is reflected to input to find the input-referred voltage noise PSD:

$$v_{n,in}^2 = \frac{i_{n,OTA}^2}{G_{OTA}^2}. \tag{35}$$

Then, the input-referred voltage noise PSD is multiplied by the square of the transfer function gain and integrated over all frequencies:

$$v_{n,out1}^2 = \int_0^\infty (G_{OTA}/g_{Ma})^2 \frac{v_{n,in}^2 df}{\left[1+\left(\frac{2\pi f C_{out}}{g_{ma}}\right)^2\right]} = \frac{i_{n,OTA1}^2}{4g_{ma}C_{out}} = \frac{2I_{b,main}}{\kappa I_1}\left(\frac{kT}{C_{out}}\right), \quad (36)$$

where $i_{n,OTA}^2 = 8i_{M1}^2 = 8qI_{b,main}$[49]. Based on (36), the noise performance degrades with increasing $I_{b,main}$ and improves with increasing I_1 and C_{out}.

The power consumption of the variable-gain OTA is found as:

$$Power = (V_{DD} - V_{SS}) \times \left(I_{b,att} + 2I_{b,main}\right). \quad (37)$$

3.3.3.2. Asymmetric Current Mirror

An asymmetric current mirror stage consisting of a series of current mirrors is designed to reflect the asymmetry in the firing rate-head motion relationship corresponding to excitatory and inhibitory head motions (Figure 51(a)). The circuit essentially combines two separate lines to generate a piecewise linear function [64]. Also the baseline frequency, which corresponds to firing rate when there is no head motion, is controlled at this stage. The circuit schematic is presented in Figure 58(a).

First, the output current of the variable-gain OTA is subtracted from an offset current, namely I_{OS}. The resultant current, i_1, is replicated twice to generate i_2 and i_3:

$$i_1 = i_2 = i_3 = I_{OS} - i_{OTA}. \quad (38)$$

Each replica is fed to one of the two current mirror pairs formed by M4-M7 and M8-M11 to generate i_A and i_B. Because M6-M7 pair is a sink-input current mirror, i_A is non-zero only when $i_{OTA}<0$. Similarly, M10-M11 is a source-input current mirror, thereby creating a non-zero i_B only if $i_{OTA}>0$:

$$i_A = \begin{cases} m \cdot (i_2 - I_{OS}) = -m \cdot i_{OTA} & , i_2 - I_{OS} > 0 \therefore i_{OTA} < 0 \\ 0 & , i_2 - I_{OS} < 0 \therefore i_{OTA} > 0 \end{cases}$$

$$i_B = \begin{cases} n \cdot (i_{OS} - I_3) = n \cdot i_{OTA} & , I_{OS} - i_3 > 0 \therefore i_{OTA} > 0 \\ 0 & , I_{OS} - i_3 < 0 \therefore i_{OTA} < 0 \end{cases}, \quad (39)$$

where $m = (W/L)_{M7}/(W/L)_{M6}$ and $n = (W/L)_{M11}/(W/L)_{M10}$ and m≠n. Therefore; the output of the asymmetric current mirror; i_{out}, which is obtained by summation of I_{OS}, i_A,

and $-i_B$ at the output node; is asymmetric across the horizontal I_{OS} line. The exact expression of i_{out} is as follows:

$$i_{out} = I_{OS} + i_A - i_B = \begin{cases} I_{OS} - m \cdot i_{OTA} & , i_{OTA} < 0 \\ I_{OS} - n \cdot i_{OTA} & , i_{OTA} > 0 \end{cases}. \tag{40}$$

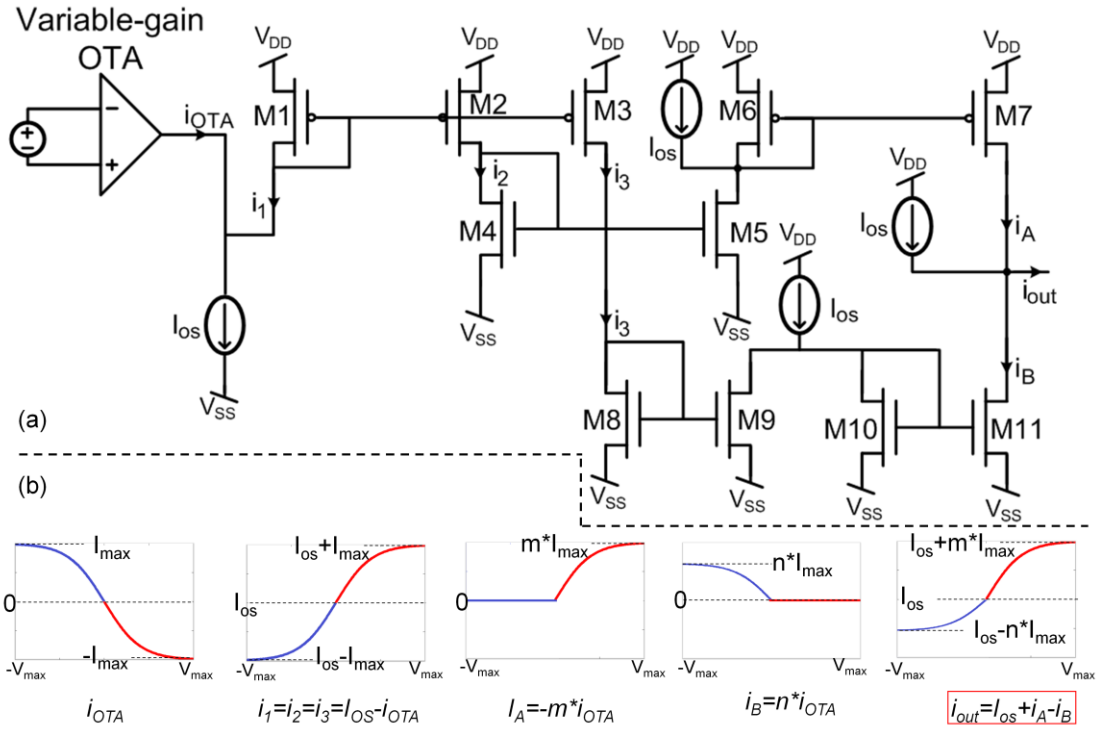


Figure 58. Asymmetric current mirror. (a) Schematic. The input to the block is the current output of the Variable-gain OTA, i_{OTA}. The offset current, I_{OS}, is generated as the drain current of a long-channel nMOS, gate voltage of which is controlled by a bias voltage. The I_{OS} is replicated by a series of pMOS current mirrors. For simplicity, the nMOS and the current mirrors are not shown in the figure. (b) Variations of currents with respect to input voltage of the variable-gain OTA are illustrated by the plots at the bottom.

All current mirrors are designed as cascode structures to reduce mirroring errors. The current mirrors formed by M1-M3, M4-M5, and M8-M9 have unity current-gains. To match the asymmetry of 1/4 as observed in neurons in Figure 51, the mirror M6-M7 has a current-gain of m=4. To provide the system with one more degree of freedom, four M11's with different sizes are designed. Therefore, at the mirror M10-M11, current-gain can be n=1, 1.3, 1.6, or 2, resulting in a range of degree of asymmetry, m/n, between 2 and 4. Selection of M11 is done by means of a 1-to-4 line demultiplexer connecting the gates of

M10 and M11. The demultiplexer is designed using minimum-size transmission-gates. To generate the offset current, I_{OS}, an nMOS, gate voltage of which is controlled by a bias-voltage, is used. To reduce the effect of channel-length modulation on I_{OS}, the nMOS is sized as a long-channel device with (W/L)=25 µm / 10 µm.

The bandwidth of the system is limited by the dominant pole at the output node. Therefore transfer function is:

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{G_{acm}}{1+sC_{out}r_{out}}, \tag{41}$$

where G_{acm} is the DC gain. It should be noted that, the asymmetric current mirror drives the Current-to-Frequency Block, which has large capacitors connected at its input, thereby reducing the bandwidth. However, for frequencies below 20 Hz, the asymmetric current mirror has a flat frequency response characteristics based on simulations (Figure 59).

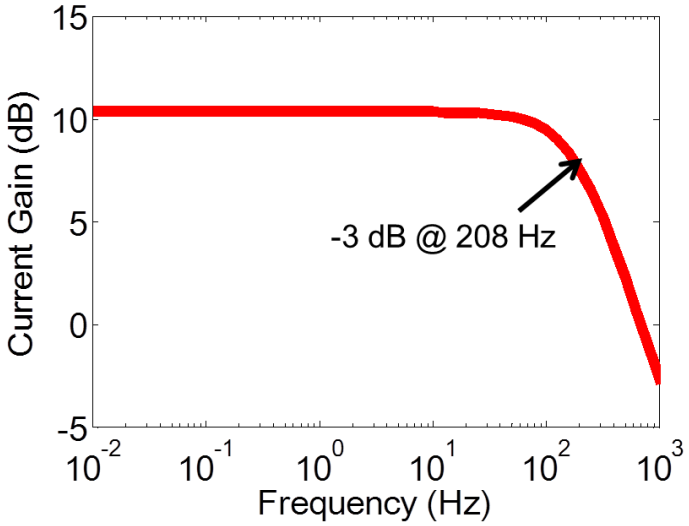


Figure 59. Frequency response of the asymmetric current mirror based on simulations.

The total output current noise power is found by first multiplying the output current noise PSD by the square of the transfer function divided by the dc gain. Then, the product is integrated over all frequencies to obtain the total power:

$$i_{n,out}^2 = \int_0^\infty \frac{i_{n,acm}^2 df}{[1+(2\pi f C_{out}r_{out})^2]} = \frac{i_{n,acm}^2}{4r_{out}C_{out}}, \tag{42}$$

where $i_{n,acm}^2$ is:

$$i_{n,acm}^2 = (m^2 + n^2) \cdot (4i_{M2}^2 + i_{OS}^2) + [i_{M7}^2 + i_{M11}^2 + i_{OS}^2] + \left[\frac{(m-n)^2}{4}(i_{M1}^2 + i_{OTA}^2 + i_{OS}^2)\right]. \quad (43)$$

As (42) and (43) suggest, the total current noise power increases with the current. Increasing the output capacitance improves the noise. It should be mentioned that, utilizing large current mirror devices, M1-M3 gate capacitances are increased and therefore the noise performance of the previous stage is improved. Because of non-identical current gains at the current mirrors formed by M6-M7 and M10-M11 (m≠n), noise contribution from the OTA and M1 appears in (43).

The power consumption expression is found as:

$$Power = (V_{DD}) \times (-5i_{OTA}+6i_{OS}) + (V_{SS}) \times (5i_{OS} - 2i_{OTA}) \quad (44)$$

3.3.3.3. Current-to-Frequency Block

The current output from the Asymmetric Current Mirror stage is fed to a current-to-frequency converter circuitry to generate a master clock. The current-to-frequency converter circuitry is a modified version of a self-resetting neuron circuit explained in Section 2.1.1.2. For convenience, the schematic is redrawn in Figure 60.

Transistors M1-M4 are sized as the same as the transistors similar to the FPAA design. Transistors M5 and M6 are sized as large devices to reduce the effect of flicker noise. Besides, M5 is a long-channel device to reduce the dependency of the current through it with respect to variations in the input node potential. The device sizes are shown in Figure 60. Setting the capacitance C2=10 pF, the frequency output of the circuit meets the normal firing-rate range observed at the vestibular neurons (f_{fire}<600 Hz) for small input current range (i_{in}<20 nA). Increasing the C1 value, the output current noise power of the previous stage can be improved based on Equation 42. However, for correct operation of the circuit, at times when low-to-high and high-to-low transitions occur at the output, potential changes at the input node, which is connected to the output through the capacitive

divider formed by C1 and C2 and given by C2/(C1+C2), needs to be sufficiently large. Therefore C1 cannot be an arbitrarily large value. Given those considerations C1 is set as 60 pF.

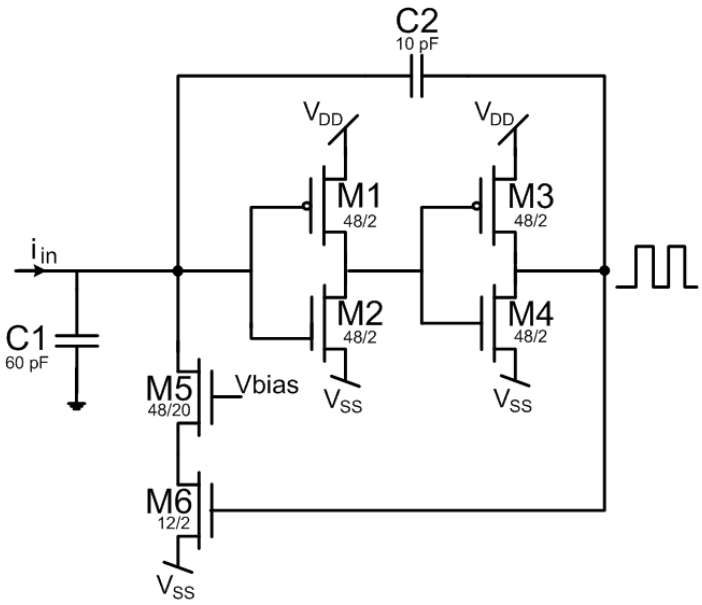


Figure 60. Current to frequency conversion block schematics.

3.3.3.4. Clock Generation Block

Two clocks (CLK1 and CLK2) are generated out of the master clock generated at the Current-to-Frequency Block. CLK1 and CLK2 are out of phase by a certain amount of time, namely the interphase gap (IPG). A three-stage clock-generation-circuit is designed to generate the pulses. Pulse-widths of both clocks as well as the interphase gap are adjustable. The circuit principle is similar to that of the positive-edge clock generation circuitry that generates the clocks of the Neural Dynamics Filters in Section 3.2.3. It should be noted that, obtaining a linear frequency-current relationship at the Current-to-Frequency Block is possible only if the duty-cycle of the master clock is very small. At a positive-edge triggered clock generation circuitry, the output clock pulse-width is limited by the input clock pulse-width. Therefore, the filter clock circuitry is modified to trigger at the falling-edges of the input clock, namely the master clock. The circuit schematic is shown

in Figure 61(a). When CLK_{in} is high, CLK_{out} and the node X are low. When CLK_{in} makes a high-to-low transition, the output node makes a low-to-high transition and the node Y makes a high-to-low transition. As a result, the potential at node X increases because of the drain current of M1 that is set by $V_{b,clk}$. During the time the X potential increases, the output remains at high. The X potential increases until it is sufficiently large to create a high-to-low transition at the output of the NOR gate. When that happens, the output goes back to low. Cascading three stages, CLK1 and CLK2, which are apart from each other by an IPG amount, can be obtained as shown in Figure 61(b). The pulse-widths of CLK1 and CLK2, as well as the IPG are set by the bias voltage, $V_{b,clk}$, of each one of the three-cascaded clock-generation-circuitry.

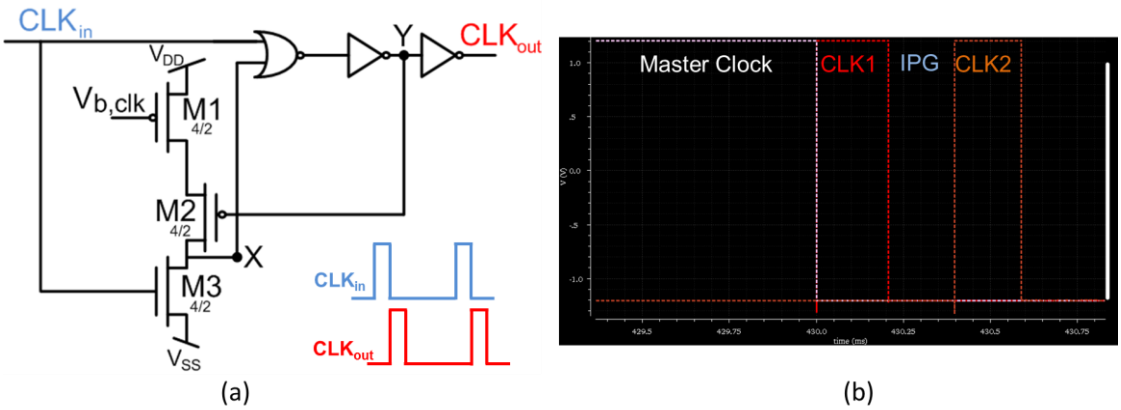


Figure 61. Clock-generation-circuitry (a) Schematics. $V_{b,clk}$ controls the pulse width of the CLK_{out}. CLK_{out} is generated at the falling edge of CLK_{in}. (b) Three clock-generation circuitry are cascaded to generate CLK1 and CLK2 with an interphase gap (IPG). Simulated waveforms of CLK1 and CLK2 generated from a Master Clock.

3.3.3.5. Variable-Gain Amplifier

Serving as a signal conditioning block, the primary function of the VGA is to amplify the output signals of the neural dynamics filters (<100 mV_{pp}), to meet the input voltage range requirement of the variable-gain OTA (600 mV_{pp}).

Designed as a basic differential pair with resistive loads, the VGA inherently offers high output swing, high linearity, high power supply noise rejection, and simple biasing (Figure 62) [65].

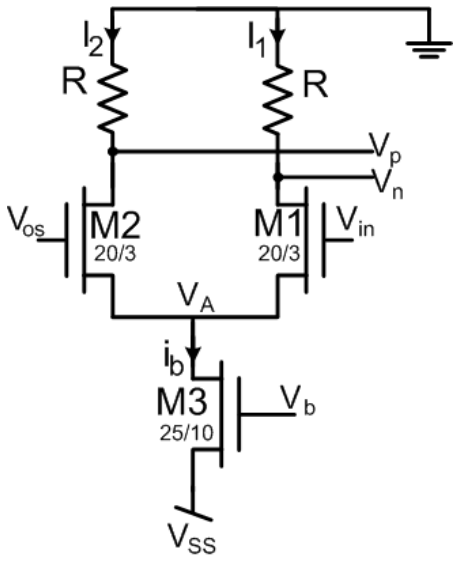


Figure 62. Variable-gain amplifier schematics.

Transistor M3, which is used as a current source, is sized as a long device (W/L=25 µm /10 µm) to obtain an almost constant bias current, I_b, regardless of the variations at the potential, V_A. Transistors M1 and M2 are sized as large devices to reduce 1/f noise. To reduce the power consumption, the transistors are biased in subthreshold region. The sum of the currents through M1 and M2, namely I_1 and I_2, is equal to I_b. Therefore, the output differential voltage is found as:

$$V_p - V_n = R \times (I_1 - I_2) = I_b \frac{e^{\left(\frac{\kappa V_{in}}{U_T}\right)} - e^{\left(\frac{\kappa V_{os}}{U_T}\right)}}{e^{\left(\frac{\kappa V_{in}}{U_T}\right)} + e^{\left(\frac{\kappa V_{os}}{U_T}\right)}} = R \times I_b \tanh\left[\frac{\kappa(V_{in} - V_{os})}{2U_T}\right]. \qquad (45)$$

The linear range and the input common mode range of the VGA determine what the input signal magnitude should be for correct operation. The linear range is limited by the parameters of the argument of the *tanh* function in (45). From (45) and (26), the linear range of the VGA is equal to that of the wide-range OTA, which is V_L=±82 mV. The gain of the VGA is found as:

$$A_{VGA} = \frac{\partial(V_p - V_n)}{\partial(V_{in} - V_{os})} = \frac{R \times \kappa}{2U_T} \times I_b. \quad (46)$$

Because of the exponential I_b-V_b dependence of M3, the gain is exponentially related to the bias voltage, V_b. It should be noted that; to lower the output common-mode voltage to a value within the input common-mode range of the next stage, namely the variable-gain OTA; the positive rail of the circuit is grounded instead of connecting to V_{DD}. Based on simulations, the maximum gain of the circuit is ~6.5, which is obtained when when I_b= 630 nA from (46). Therefore, the maximum potential drop across the resistors, R, is ~315 mV, thereby reducing the common-mode potential to -315 mV, which ensures operation of the variable-gain OTA.

The input common mode range (ICMR) of the VGA is particularly important to ensure matching with the output common-mode range of the Neural Dynamics Filter. The ICMR is determined by investigating the conditions keeping all transistors in saturation. In subthreshold region, an nMOS is in saturation as long as $V_{DS} \geq V_{DS,SAT} = 4U_T \approx 100$ mV. When both inputs are connected to the negative supply, i.e. $V_{in} = V_{os} = V_{CM} = -1.2$ V, M1 and M2 are off, pulling V_p and V_n to the higher rail voltage, i.e. $V_p = V_n = 0$. As V_{CM} is increased, neglecting any mismatch between M1 and M2, each starts conducting a current equal to the half of I_b. For M3 to act as a current source, the saturation condition must be satisfied, implying $V_A \geq V_{SS} + V_{DS,SAT}$. With the assumption of $I_1 = I_2 = I_b/2$, a lower bound for V_{CM} is found as:

$$V_{CM,low} = V_{SS} + V_{DS,SAT} + V_{GS,M1}. \quad (47)$$

As long as M1 and M2 remain in saturation, $I_1 = I_2 = I_b/2$ condition holds. Therefore, as V_{CM} is increased, V_A tracks V_{CM}. However, if V_{CM} is increased further, M1 and M2 exit saturation region when $V_p - V_A = V_n - V_A < V_{DS,SAT}$. The upper limit of V_{CM} is equal to the voltage making M1 and M2 exit saturation, which occurs when

$$V_{CM,up} = -\left(R\frac{I_b}{2}\right) - V_{DS,SAT} + V_{GS,M1}. \quad (48)$$

The first term in (48) is set by the small-signal gain requirement of the VGA and therefore fixed. The second term is also fixed to ~100 mV. The last term is determined by the input transistor dimensions for a given bias current, I_b. Therefore, to increase $V_{CM,up}$, M1 and M2 dimensions need to be reduced. However, from (47), increasing $V_{GS,M1}$ increases $V_{CM,low}$. For I_b=250 nA, based on simulations the ICMR is larger than 0.6 V with $V_{CM,low}$≈-0.6 V and $V_{CM,up}$>0 V. Therefore, it is concluded that the ICMR of the VGA is wide enough considering the output common-mode voltage of ~0 V of the Neural Dynamics Filter.

The dominant pole of the VGA is at its output. The output impedance can be approximated as $R_D//r_{o1}$≈R_D=1 MΩ. The load of the VGA output is the input transistor of the variable-gain OTA, which is an nMOS with (W/L)=1 µm /100 µm. Based on simulations, the load capacitance value is estimated as C_L=190 fF. Therefore, -3 dB frequency is estimated to be at f_{-3dB}=~840 kHz. Therefore, a flat gain characteristics is obtained for the frequency range of interest (f<20 Hz) based on simulations.

The total output voltage noise power is found as:

$$v_{ntot,out}^2 = \int_0^\infty \frac{v_{n,in}^2\left(\frac{R_D I_b \kappa}{2U_T}\right)^2 df}{[1+(2\pi f C_L R_D)^2]} = \frac{v_{n,out}^2}{R_D^2 g_m^2}\frac{R_D \kappa^2 I_b^2}{16U_T^2 C_L} = \frac{2kT}{C_L} + \frac{I_b R_D q}{2C_L}, \quad (49)$$

where $v_{n,out}^2 = 2qI_bR_D^2 + 8kTR_D$. Based on (49), increasing I_b degrades the noise performance.

The power consumption of the VGA is:

$$P_{VGA} = -V_{SS}I_b. \quad (50)$$

3.3.4. Measurement Results

The V-to-F has been fabricated with TI 0.35-µm 3P2M n-well CMOS process. In Figure 63, optical image and floor plan of the V-to-F are shown. The footprint is 0.47 mm x 0.65 mm.

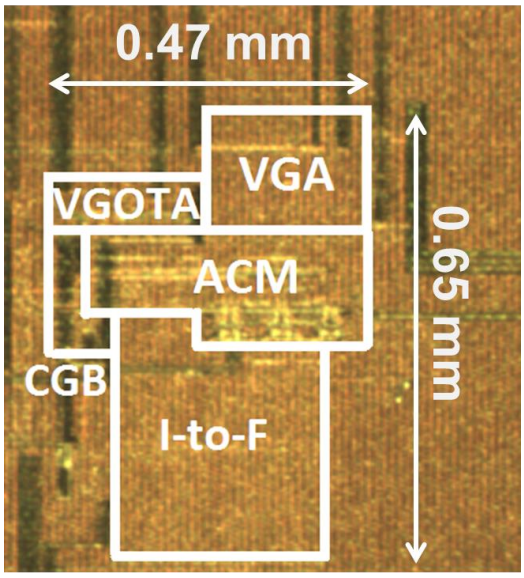


Figure 63. V-to-F Floor plan. The abbreviations ACM and VGOTA refer to the Asymmetric Current Mirror and the Variable-gain OTA blocks.

3.3.4.1. Testing Procedure

The schematic of the test-bench for measurements is shown in Figure 64. All bias voltages are generated by sourcemeters and a triple output HP E3631A power supply. The input to the V-to-F is generated from a function generator. For testing the Asymmetric Current Mirror and the Current-to-Frequency Blocks, sourcemeters are used to supply currents in the order of nA. All current measurements are performed using the sourcemeters. To perform frequency measurements, the scope is connected to a PC. The data acquisition is performed using the NI LabVIEW SignalExpress software (National Instruments, Austin, TX). The frequency measurements are made for 11 data points spanning the input voltage range of ±300 mV. For each data point ~10 frequency measurements is performed, which are averaged using MATLAB. In the following subsections, measurement results pertaining to each sub-block of the V-to-F are presented.

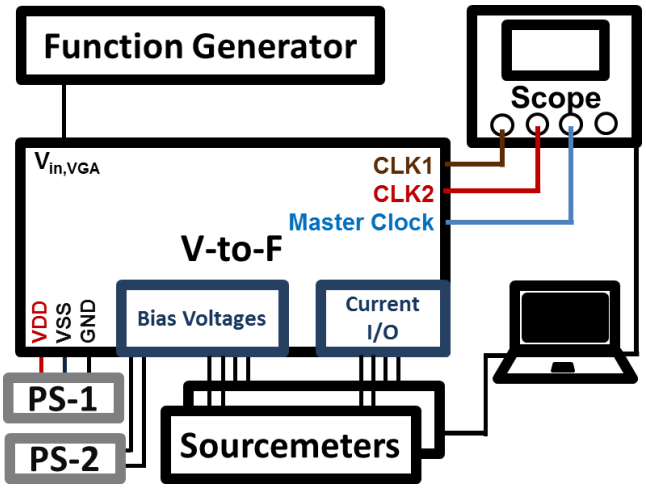


Figure 64. V-to-F Test-Bench Schematics.

3.3.4.2. Functionality

The functionality of the V-to-F is verified for each sub-block. Below, measurement results from each sub-block is presented.

Variable-Gain OTA

The slope control of the OTA for a constant output current and the gain control for a constant slope are shown in Figure 65.

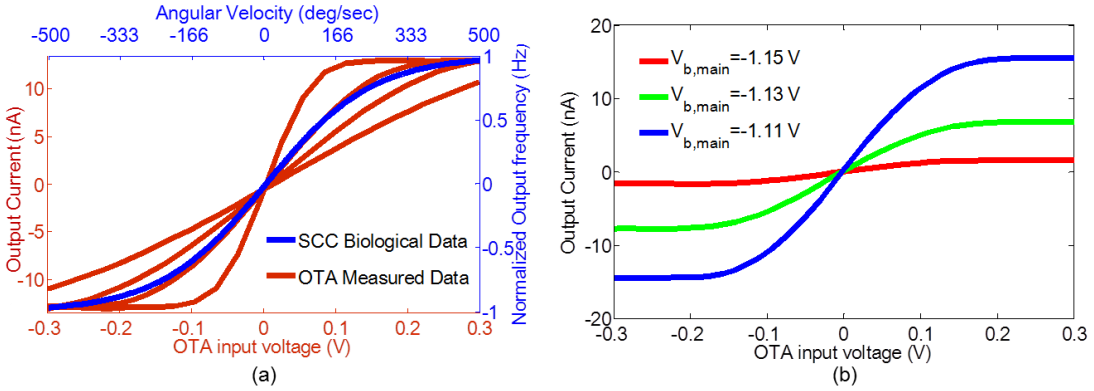


Figure 65. Variable-gain OTA measured data. (a) Slope control and SCC neuron firing rate from [58]. (b) Current range control.

For a constant $V_{b,main}$, varying $V_{b,att}$ within a range of ~60 mV, the slope of the *tanh* curve is controlled (Figure 65(a)). In Figure 65(b), the output current range control of the OTA for a constant $V_{b,att}$, is shown.

Asymmetric Current Mirror

The asymmetry about the zero input current is verified as shown in Figure 61. The four different orders of asymmetry, selected by the select bits of the demultiplexer, are shown in Figure 66(a). The output current, when variable-gain OTA output feeds the asymmetric current mirror, is shown in Figure 66(b).

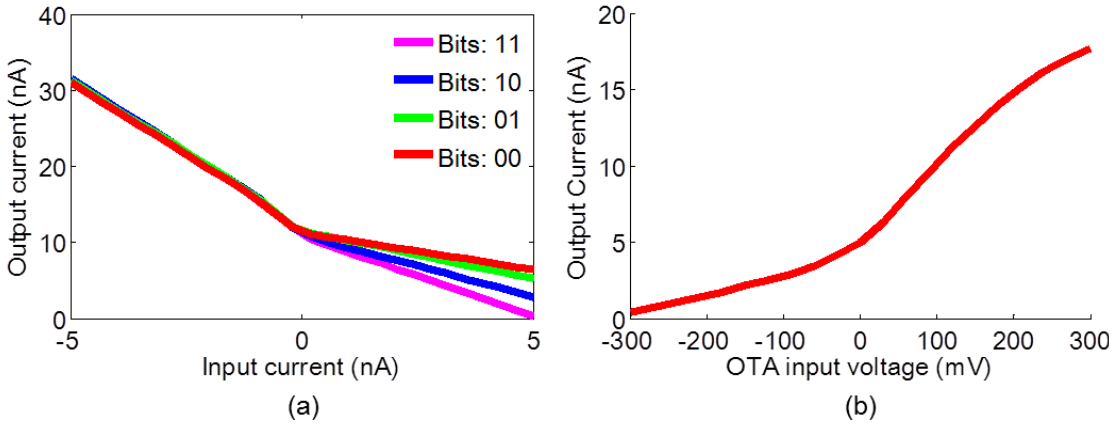


Figure 66. Asymmetric current mirror measurement results. (a) The order of asymmetry control. (b) Output current when variable-gain OTA feeds the asymmetric current mirror.

Current-to-Frequency

The output frequency vs. input current relationship is shown in Figure 67. The pulse-width of the output clock is set to a value of 10 µs, which is significantly smaller than the period of the maximum measured frequency of 540 Hz. Therefore, a linear frequency-current dependence is obtained. The sensitivity is measured as 18 Hz/nA.

Variable-Gain OTA – Asymmetric Current Mirror – Current-to-Frequency

Measurement results from the signal processing blocks together are shown in Figure 68. For a fixed $V_{b,main}$ of the variable-gain OTA, $V_{b,main}$=-1.1 V, varying the $V_{b,att}$ from -1.14 V to -1.2 V, the slope control of the frequency-input voltage is shown in Figure 68(a). The linear ranges for the excitatory inputs vary from 176 deg/sec to 500 deg/sec,

which includes the excitatory linear range of $V_{L,bio,exc}$=246.5 deg/sec obtained from biology based on (33).

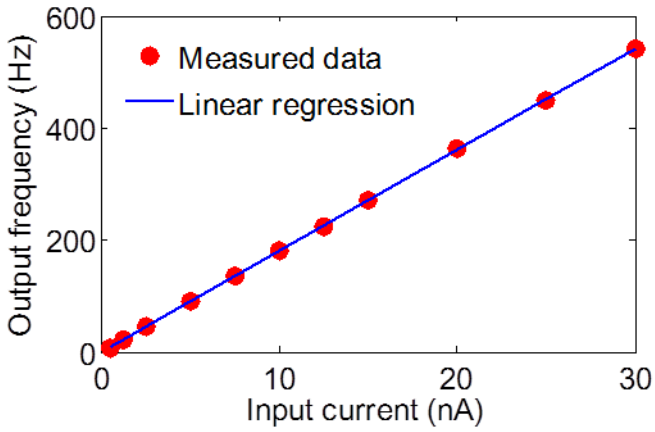


Figure 67. Measurement results of the current to frequency conversion block.

For a fixed $V_{b,att}$, varying $V_{b,main}$, the range of the output frequency is controlled as shown in Figure 68(b). It should be noted that, increasing the baseline frequency, a larger frequency range can be obtained.

The order of asymmetry is controlled between 2 and 4, by varying the select bits as shown in Figure 68(c).

The baseline frequency is controlled by varying the offset voltage bias, namely V_{OS}, of the Asymmetric Current Mirror, which controls the I_{OS} in Figure 58(a). Based on measurements, 5 mV of change in the V_{OS} results in 56 Hz of difference.

Clock Generation Block

The clock waveforms, CLK1 and CLK2, are shown in Figure 69. The pulse-duration (PD) of each clock as well as the IPG is controlled from less than 1 µs to the maximum duration possible for that particular clock frequency. For PD=IPG, varying $V_{b,clk}$ from ~1.184 V to ~1.354 V, resultant PDs vary from 5 µs to 630 µs as shown in Figure 69.

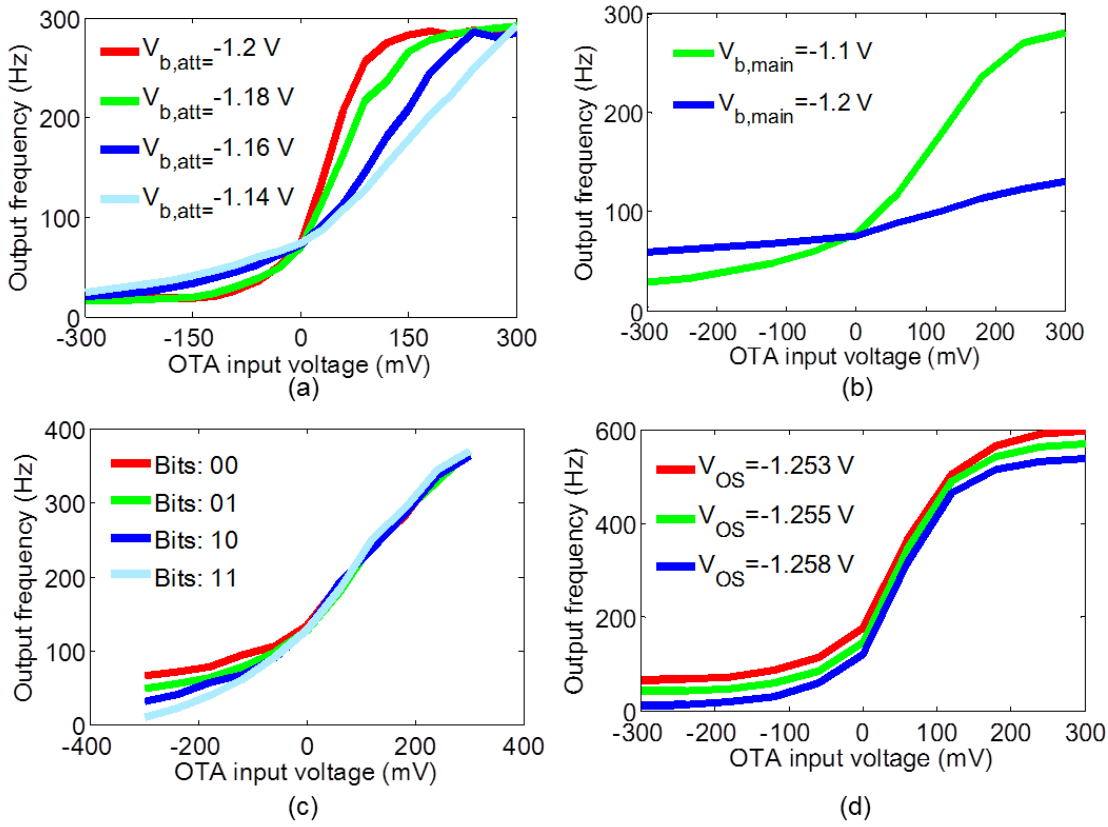


Figure 68. Measurement results of the current to frequency conversion block. (a) Slope control. (b) Frequency range control. (c) The order of asymmetry control. (d) Baseline frequency control.

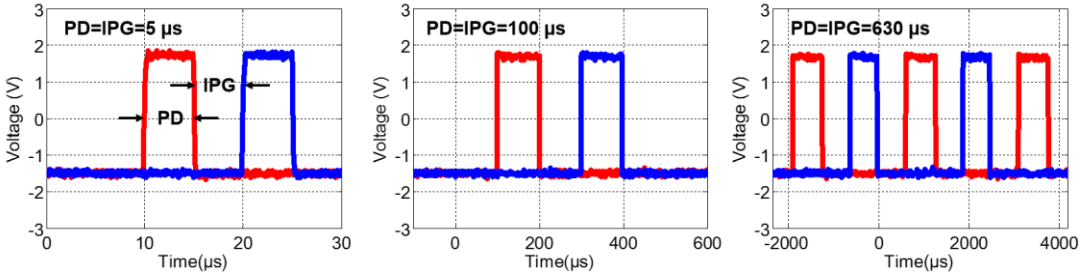


Figure 69. Measured CLK1 and CLK2 waveforms. The pulse duration (PD) and the interphase gap (IPG) can be varied from <1 µs to the maximum possible value for that particular frequency (630 µs when PD=IPG and clock frequency is 400 Hz). For PD=5 µs, 100 µs, and 630 µs, $V_{b,clk}$ values are ~1.184 V, ~1.287 V, and ~1.354 V, respectively.

Variable-Gain Amplifier

The exponential dependence of the VGA gain to its bias voltage is verified with the measurements as shown in Figure 70. For V_b=-1.1 V, the gain is at its maximum value,

A_{VGA}=6.48 V/V. Therefore, to output a signal that meets the ±300 mV of input voltage range requirement of the variable-gain OTA, the input voltage range of the signal to be amplified at the VGA, namely the output of the neural dynamics filter, needs to be larger than ±46.3 mV.

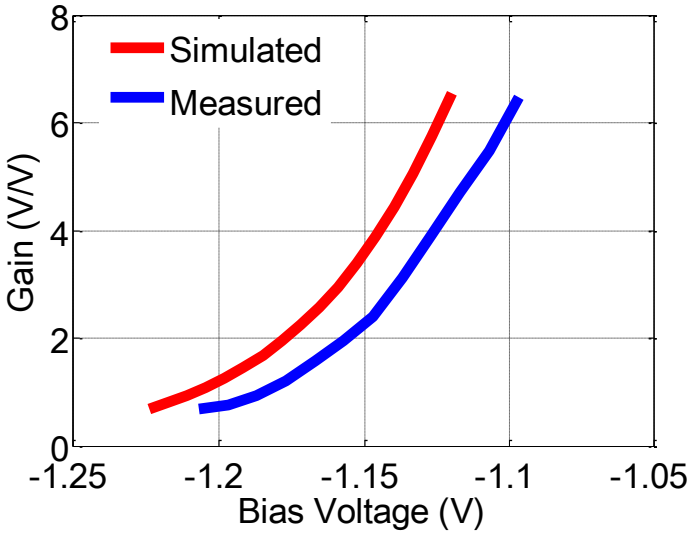


Figure 70. VGA gain variation with the bias voltage V_b.

3.3.4.3. Noise

Essentially the V-to-F is a voltage controlled oscillator that has a DC gain of:

$$A_{V-to-F} = A_{VGA}A_{VG-OTA}A_{ACM}A_{I-to-F}, \quad (51)$$

where A_{VGA}, A_{VG-OTA}, A_{ACM}, and A_{I-to-F} are the DC gains of the VGA, variable-gain OTA, asymmetric current mirror, and the Current-to-Frequency sub-blocks, respectively. Noise of the V-to-F is observed as jitter in the time-domain (Figure 71).

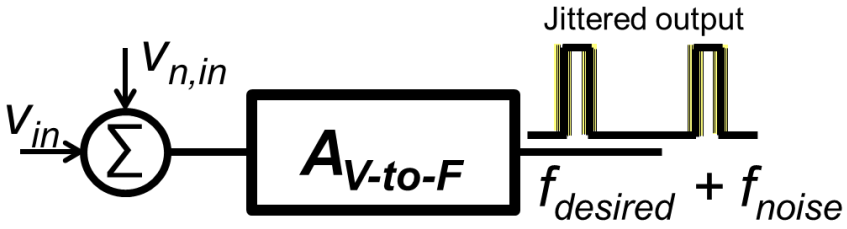


Figure 71. Noise of the V-to-F is observed as jitter at the output in the time domain.

In Figure 71, v_{in}, $v_{n,in}$, $f_{desired}$, and f_{noise} denote the input signal voltage, input-referred voltage noise of the V-to-F, desired output frequency, and the shift in the frequency due to noise. To measure the input-referred voltage noise, the output frequency noise power is measured from the frequency distribution that is obtained out of 512 frequency measurements. The variance of the frequency distribution is equal to the noise power [66]. Then using the gain in (51), first input-referred noise power and then voltage were calculated. Vestibular sensation threshold refers to the minimum angular/linear motion that causes a perception of the motion when in a steady position. Therefore, the noise power measurements were performed for a baseline frequency of ~70 Hz. The measured frequency values are shown in Figure 72.

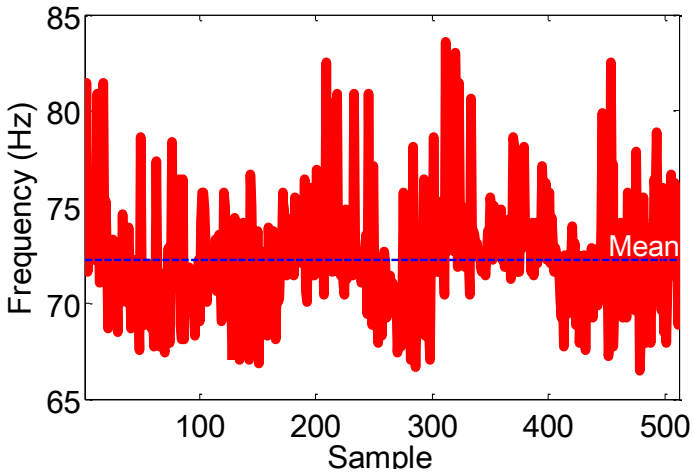


Figure 72. Noise of the V-to-F is observed as jitter at the output in the time domain.

The variance is calculated as 8.37 Hz^2, which is equal to the output frequency noise power, namely $f_{n,out}^2$. For a maximum output frequency of 300 Hz, 50 mV of input voltage creates ~230 Hz of increase in the output frequency. Therefore, the DC gain of the V-to-F is approximated as 230 Hz / 50 mV. Referring the output frequency noise power to input and taking the square root of the result, input voltage noise is found as

$$v_{n,in} = \sqrt{\frac{f_{n,out}^2}{A_{V-to-F}^2}} = 630\ \mu V_{rms}. \quad (52)$$

3.3.4.4. Power

The power measurements are made for the case when the output frequency is at a typical maximum value of 300 Hz, the variable-gain OTA attenuation stage draws a maximum current of ~350 nA, and the gain of the VGA is at its maximum value of ~6.5 V/V. Under those conditions, the total power consumption is measured as 405 µW. The power breakdown is shown in Figure 73.

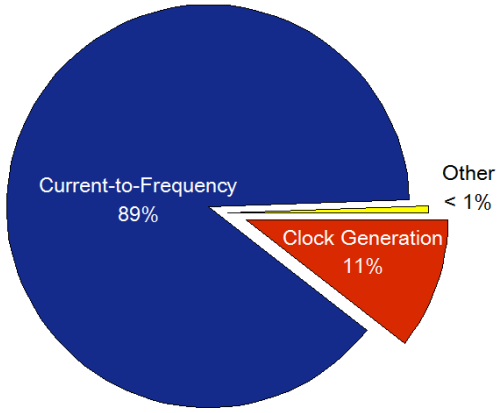


Figure 73. Power breakdown of the V-to-F.

3.3.5. Discussion

A voltage-to-frequency converter block (V-to-F) that implements the asymmetric-sigmoid-shaped firing rate-head motion relationship observed at the vestibular neurons is presented. All parameters that describe the sigmoid curves can be controlled. The performance parameters of the V-to-F is summarized in Table 8.

Table 8. Summary of Performance Parameters of the V-to-F

Property	**V-to-F**
Input voltage	>±46.3 mV
Noise ($v_{n,in}$)	630 μV_{rms}
Minimum detectable angular velocity - acceleration	8.9 ˚/sec – 71 mg
SNR	35 dB
Maximum Output Frequency	> 1 kHz
Asymmetry Ratio Range ($\Delta f_{exc}/\Delta f_{inh}$)	2 - 4
Output Clocks Pulse-Width & IPG Range	> ~1 µs
Dimensions	773 µm x 715 µm
Power	405 µW

The baseline frequency, the firing rate range, the asymmetry ratio, and the gain parameters are tunable.

As shown in Figure 73 the total power consumption is dominated by the Current-to-Frequency and the Clock Generation Blocks. It should be noted that the power of the inverter stages of the Current-to-Frequency Block is decomposed into three components; dynamic, short-circuit, and static power. For an inverter whose input voltage switches between the two rail voltages, power consumption would be dominated by the dynamic and short-circuit power components. However, the input node of the current-to-frequency block is at a potential between V_{SS} and V_{DD}, thereby resulting in significant static power consumption of the inverters. Sizing M1-M4 smaller, the total power consumption could be significantly improved. In fact, by reducing the aspect ratio of the transistors by 99.8%, the power consumption could be improved by also 99.8% based on simulation results (Figure 74). It is noteworthy to mention that the measured supply current value of 112.5 µA is close to the simulated average supply current value of 89.6 µA for the case when $(W/L)_{M1\text{-}M4}$=48/2 in Figure 74.

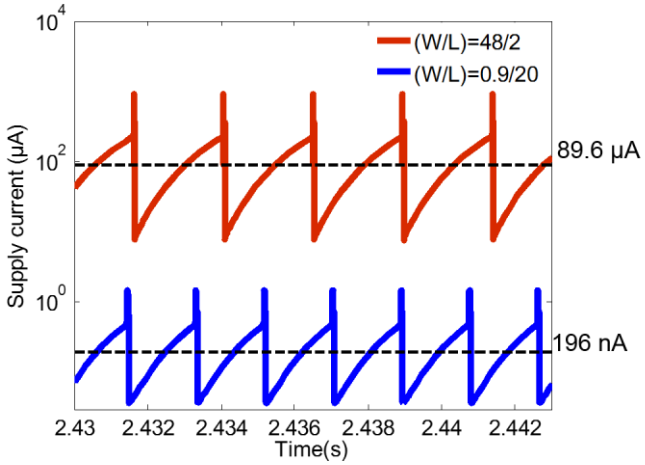


Figure 74. Current to frequency conversion block static power consumption simulations.

The noise performance is affected by the test setup. For characterization purposes, the sub-blocks of the V-to-F are connected on a breadboard, which is a noisy platform. To

improve the noise performance, the sub-block connections can be made on-chip. Furthermore, a PCB and package specifically designed for the die can improve the noise performance of the V-to-F. To further improve the noise performance, the flicker noise contributions of the VGA and the Variable-gain OTA can be reduced by employing large pMOS transistors at the inputs instead of nMOS transistors.

CHAPTER 4

VESTIBULAR PROSTHESIS SIGNAL PROCESSING ON AN ULTRA LOW-POWER MICROCONTROLLER

Because of its inherent repeatability, consistency, and insensitivity to environment; today, signal processing is more commonly performed in digital domain than in analog domain [67]. To implement digital signal processing algorithms the two most popular platforms are microprocessors, and digital signal processors. Digital signal processors (DSPs) are essentially microcontrollers specialized for performing arithmetic operations quickly. The computational power advantages of DSPs; however, render DSP platforms more power-hungry when contrasted with microcontrollers. Therefore, for applications where power consumption is a primary concern and limited computational power is sufficient, microcontrollers are preferred over DSPs. Considering low-frequency content of normal head-motions, signal processing functions of a vestibular prosthesis, which is a battery-powered device, are implemented on an ultra-low-power microcontroller. Of all ultra-low-power microcontrollers available in the market, TI MSP430 series microcontrollers are claimed to be one of the most power-efficient platforms, in both sleep and active modes [68]. Furthermore, using an MSP430 device, it is possible to compare the custom-design presented in Chapter 3 with one of the most promising state-of-the-art vestibular prosthesis devices, which is being developed using an MSP430 series microcontroller [17].

The block diagram of the MSP430 implementation of the vestibular signal processing functions is shown in Figure 75. Digitized input signals from the rate sensors are applied a coordinate system transformation operation, filtered with IIR filters reflecting neural dynamics, and lastly converted to pulses to control a current stimulation circuitry. Using MSP430 IAR C Compiler, a C code implementing the aforementioned functions is

compiled and programmed on an MSP-430FG4619 microprocessor, which sits on an MSP-FET430UIF development board. Below, details on each block is presented.

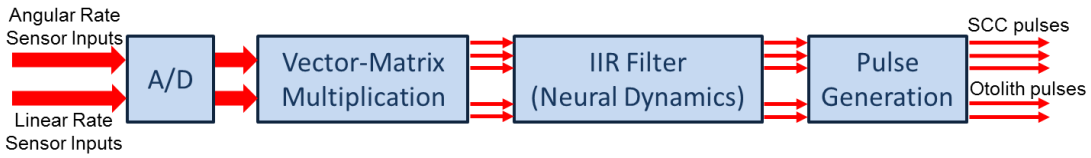


Figure 75. Block diagram of the vestibular signal processing functions implemented on a TI MSP430 microcontroller.

4.1. A/D Conversion

The 12-bit ADC unit of the MSP430 is used to sequentially digitize six rate sensor outputs (three angular, three linear). For the presumed physiological angular velocity and linear acceleration ranges (i.e <±500 deg/sec and <±4 g [11],[12]), output voltages of most commercial gyroscopes/accelerometers are below 2.5 V. The built-in voltage reference of 2.5 V is selected as the reference voltage, thereby eliminating the need for an external signal conditioning circuitry. The ADC sampling rate directly affects the coefficients of the IIR filters, which are to be selected such that the effect of rounding errors can be minimized. When the sampling rate is increased, the corresponding IIR filter coefficient values get closer, which is not desired as 32-bit addition/multiplication operations of IIR calculations result in more rounding errors when the coefficients are close. By dividing the ADC internal oscillator frequency, namely ADC12OSC, with four and setting the number of sampling cycles of each input signal to 768, the ADC sampling rate for each of the six input signals is set to $f_{ADC,calc}$=1.25 MHz/(6*(768+13))=266.75 Hz. The sampling rate is sufficiently small to result in small rounding errors and larger than the Nyquist rate for the presumed maximum frequency of normal head motions (20 Hz). The measured sampling rate is $f_{ADC,meas}$=244 Hz. The discrepancy between the measured and the calculated values is because of variation in the ADC12OSC frequency with individual devices, supply voltage, and temperature [69].

4.2. Vector-Matrix Multiplication (VMM)

To generate the signals for the three canals and two otoliths, digitized angular and linear rate sensor signals are multiplied by 3-by-3 and 3-by-2 matrices, respectively. The matrix elements take values between -1 and +1. When a sinusoidal input that is applied to all channels is multiplied by the weight elements [1 1 1] and [-1 -1 -1], the resultant waveforms are shown in Figure 76.

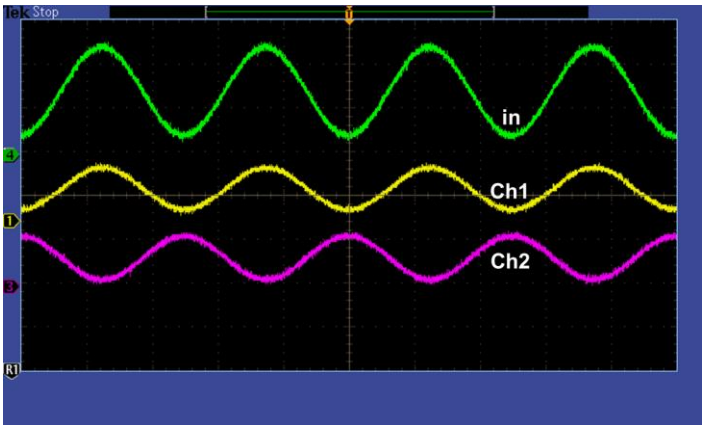


Figure 76. Output signals on Ch1 and Ch2 when a sinusoidal signal is multiplied with [1 1 1] and [-1 -1 -1] matrices, respectively.

4.3. IIR Filters

SCC and otolith neuron firing-rate dynamics are implemented using IIR filters, which are designed by discretizing continuous-time filters presented in [7] and [12] with a sample rate, $f_{ADC,meas}$=244 Hz. The MATLAB code generated to calculate the IIR constants

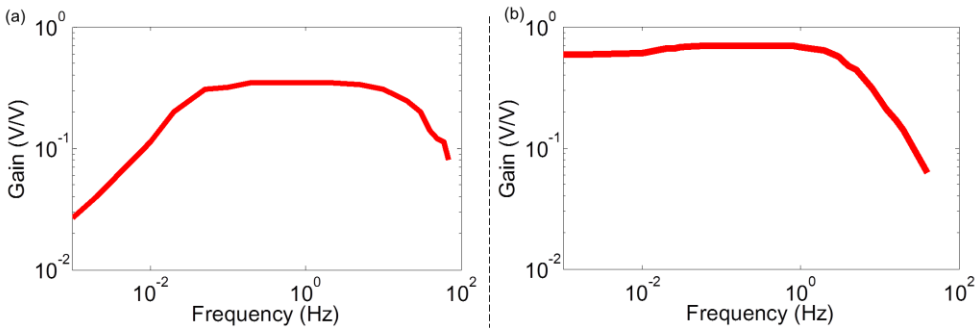


Figure 77. IIR filter frequency responses. (a) SCC. (b) Otolith.

is given in the Appendix B. The measured frequency responses of the IIR filters are shown in Figure 77.

4.4. Pulse Generation

For slow angular/linear head motions, neuron firing rates vary almost linearly with the rotational speed/linear acceleration. Faster head motions, however, cause the firing rates to saturate. Therefore, the firing-rate vs. angular velocity/linear acceleration curves are characterized by sigmoid shape functions [7],[11], which are implemented using the following base function:

$$f_{pulse} = f_{dc} + C\tanh\left(\frac{y_{IIR}}{A}\right), \tag{51}$$

where f_{dc} is the baseline firing rate, y_{IIR} the IIR output, A and C the constants setting the slope of the curve in linear region and the range, respectively. To convert f_{pulse} into pulses, one of the 16-bit timers is utilized in continuous mode to generate five independent output frequencies from the reciprocal of f_{pulse} weighted by a constant controlling the output frequency range. The clocks needed to control an H-Bridge circuit are generated inside a

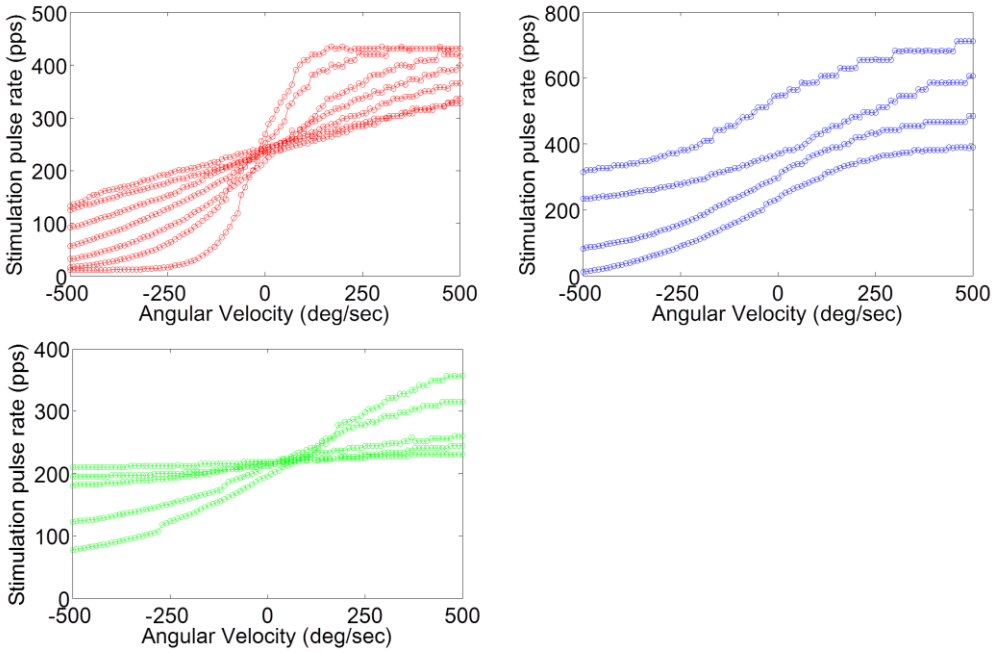


Figure 78. Illustration of control of the parameters in (51).

port interrupt routine, which is entered at the rising edges of output frequencies that the timer generates. The frequency variation with input signal is presented in Figure 78.

Control over clock pulse widths and phase difference between the clocks are illustrated in Figure 79.

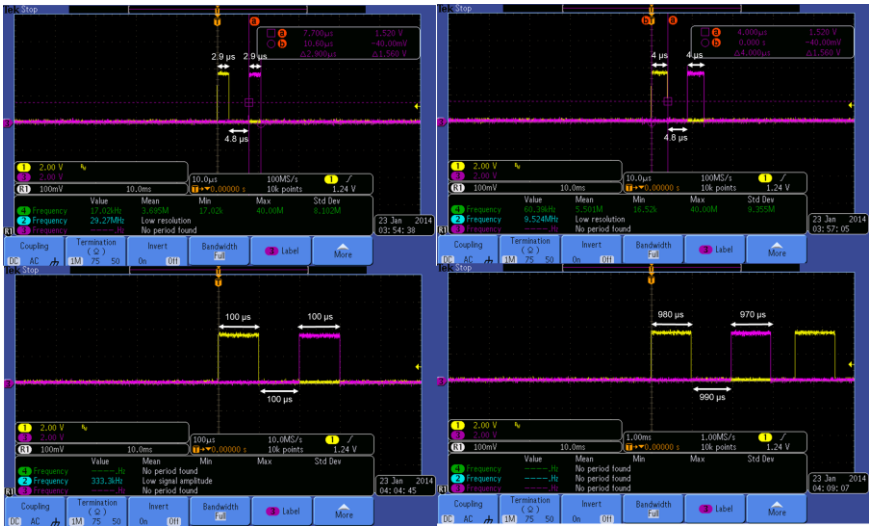


Figure 79. Illustration of control of time-related parameters of the two clocks.

4.5. Performance Parameters

4.5.1. Power

In an effort to reduce the power consumption, the time in low power mode 3 (LPM3) is maximized by using interrupts. The MSP430 chip draws 7 mA of current from a 3.2 V of supply voltage, implying 22.4 mW of power consumption.

4.5.2. Area

The footprint of the 100-pin MSP430FG4619 chip is 17.4 mm x 17.4 mm.

4.5.3. Noise

The output frequency generated by the MSP430 VP signal processing implementation fluctuates in time, which limits the minimum detectable angular velocity/linear acceleration. To estimate those values, a frequency distribution around a

frequency of 73.5 Hz, which corresponds to the baseline firing rate, is obtained. The data set consists of 516 frequency points, from which the variance and the standard deviation are calculated as 1.1 Hz^2 and 1.05 Hz, respectively (Figure 80). If a maximum frequency of 300 Hz is assumed, for the SCCs, the signal processor converts an angular velocity range of 500 deg/sec to ~227 Hz of output frequency. Therefore, the minimum detectable angular velocity is found as ~2.3 deg/sec. With the same maximum frequency assumption, for the otoliths, a range of 4 g of linear acceleration is converted into ~227 Hz of output frequency, implying a minimum detectable linear acceleration of ~18.5 mg.

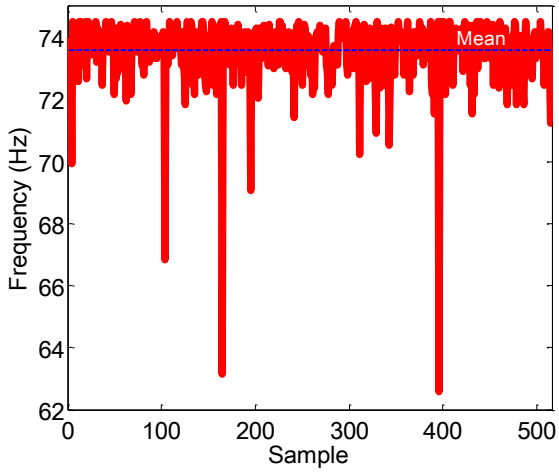


Figure 80. Fluctuation in the output frequency of the MSP430.

4.6. The MSP430 vs. the ASIC

A comparison between the MSP430 and the ASIC concretizes the potential of subthreshold analog signal processing techniques for a complete vestibular prosthesis system. It should be noted that both the MSP430 and the ASIC are fabricated with Texas Instruments processes, from which it can be concluded that the process-related differences are not significant.

Although the MSP430 is a reconfigurable platform that enables rapid implementation of the VP signal processing functions with accuracy that is inherent to

digital computations, because of its large area and high power consumption, it is impractical to use it as a prosthetic device.

On the other hand, making use of subthreshold analog signal processing techniques, the ASIC offers an energy and area-efficient signal processing circuitry for a VP system. It should be noted that, the measured power values of the ASIC do not include power values from the memory and the DAC circuitry that are needed to assist the core signal processing circuitry. However, with careful design of those blocks, current consumption of the custom chip could still be kept in the sub-mW range.

Based on the measurements on the output frequencies, minimum detectable angular velocity and linear acceleration values of both solutions exceed the requirements of the biology. However, the noise performance of the ASIC can be improved to potentially match the sensing thresholds of the vestibular organs.

In Table 9, the performances of the two solutions are evaluated based on the requirements of the VP.

Table 9. Performance Comparison of the ASIC and the MSP430.

Property	**ASIC**	**MSP430**
Area	↑	↓
Power	↑	↓
Noise	↓	↓

CHAPTER 5

CONCLUSION AND FUTURE WORK

In this dissertation, design and validation of an energy-efficient signal processing circuitry for a vestibular prosthesis (VP) is presented. To compare analog and digital signal processing domains, three approaches are followed: (1) FPAA implementation (analog), (2) Custom-design (analog), and (3) Microcontroller implementation (digital). In the sections below each approach is summarized and all three approaches are compared (Table 10). In the Table 10 the abbreviations CST and VSP refer to the functions coordinate system transformation and vestibular signal processing, respectively. After the comparison, the contributions of this research are summarized. The chapter is concluded with a discussion of future work.

Table 10. Summary of the Three Approaches.

Property	**FPAA**	**ASIC**	**MSP430**
Functions	V-to-F (1 SCC)	CST (3 SCCs+2 otoliths) VSP (2 SCCs+1 otolith)	CST (3 SCCs+2 otoliths) VSP (3 SCCs+2 otoliths)
Area	166 cm^2	10 mm^2	302.7 mm^2
Power	0.4 mW	1.24 mW	22.4 mW

5.1. Three Approaches

5.1.1. FPAA Implementation

For a single SCC, the signal processing circuitry that converts angular velocity into pulse rate is implemented on an FPAA. To implement the sigmoid firing rate-angular velocity relationship of the SCC neurons in an energy efficient fashion, the *tanh* current-voltage relationship of an OTA in subthreshold is utilized resulting in an overall power

consumption of 400 µW excluding the power consumption of the off-the-shelf DAC. The programmability of the FPAA chip enables control of the patient-dependent baseline value and the range of the output frequency.

Implementing the coordinate system transformation and the complete vestibular signal processing circuitry for all three SCCs and two otoliths on a single FPAA chip is not possible because of the limited number of elements. Furthermore, the FPAA platform has a large footprint, ~166 cm^2.

In addition to the signal processing circuitry, a neural stimulator is implemented to explore voltage and current limitations of the FPAA. To depolarize vestibular neurons the stimulator generates high current values. However, the voltage headroom is limited to the supply voltage of the FPAA, 3.3 V. As a result the FPAA is not suitable for *in-vivo* experiments.

5.1.2. ASIC

The ASIC provides CST circuitry for three SCCs and two otoliths as well as VSP functions for two SCCs and one otolith. The design can be interfaced with the analog output of gyroscopes and accelerometers having sensitivities as large as 0.4 mV/º/sec and 62.5 mV/g respectively. The ASIC generates the clocks necessary to drive an H-Bridge circuit. In turn biphasic current pulses to eliminate the unwanted charge accumulation at the stimulation sites can be generated. Considering the mid-range SNR values of the peripheral vestibular organs, a majority of the circuitry is designed to perform subthreshold analog signal processing techniques.

Two vector-matrix multiplication blocks (VMM) are designed to perform the CSTs. Multiplication is performed by a four-quadrant transconductance subthreshold multiplier. To improve the poor linear range performance due to subthreshold operation, active attenuation stages are employed at the inputs of the multiplier. This way, inertial sensors having large sensitivities can be interfaced with the design.

In the subthreshold region, the effect of device mismatches on the circuit performance can be significant. To reduce calculation errors due to device mismatches as well as the power consumption, a single multiplier is employed to perform all multiplications in a time-division multiplexed way. The addition operation is performed in a passive manner at a voltage averaging circuitry that makes use of charge distribution on capacitors connected in parallel. For an input clock frequency of 10 kHz, the power consumption of the 3-by-3 VMM is measured as 5.1 μW and the calculation is completed in 1.6 ms, which is less than the human vestibuloocular reflex response time range of 7.5 ms to 10.3 ms.

Considering the low-frequency nature of the head motion signals, the dynamics observed in the SCC and the otolith neurons are implemented using a modified version of the regular OTA-C filter architecture, which has a power consumption directly related to the bandwidth of the filters. To improve the area performance of the regular OTA-C filter architecture and allow tuning of the time-constants, the average output currents of the OTAs are controlled by switches at the outputs of the OTAs. The time-constants are tuned by modulating the pulse-widths of the clocks controlling the switches. This way, time constants as large as 106 s and 13.2 s can be obtained by the SCC and the otolith filters having footprints of 2.4 mm^2 and 1.35 mm^2, respectively. The power consumption of the SCC filter is measured as 6.96 μW.

A V-to-F stage is designed to encode the signals representing the head motions into frequency-modulated signals. Similar to the FPAA vestibular signal processing implementation, an OTA in subthreshold region performs the core signal processing function of this stage, namely implementing the sigmoid firing rate - head motion relationship. Unlike the FPAA implementation, the OTA inputs are attenuated by an amount controlled by the user, thereby enabling the linear region slope control of the sigmoid function, which varies from patient-to-patient. The asymmetric variation of the neuron firing rate in response to the excitatory and the inhibitory inputs is reflected by an

asymmetric current mirror stage, which enables control over the degree of asymmetry. The V-to-F output frequency satisfies the typical maximum firing rate value used in clinical vestibular studies (300 Hz). The V-to-F footprint is 0.55 mm^2 and the maximum power consumption is measured as 405 µW when the output frequency is at its typical maximum value of 300 Hz.

5.1.3. Microcontroller Implementation

To compare the custom-design with an existing commercial solution, CST and the VSP functions for three SCCs and two otoliths are implemented on a microcontroller. To compare the custom-design with a state-of-the-art VP as well, an ultra-low power TI MSP430 series microcontroller is selected. The time in low-power-mode-3 is maximized to reduce the power consumption. The ADC sampling rate is selected as the smallest value possible satisfying the Nyquist criterion for the sensor signals having a bandwidth of 100 Hz. This way, not only the power consumption but also the rounding error at the filtering stage is reduced. The microcontroller has a footprint of 302.7 mm^2 and consumes 22.4 mW of power at an ADC sampling rate of 244 Hz.

5.2. Comparison of the Three Approaches

The FPAA and microcontroller both offer ease of customization, but at the expense of large areas. An additional feature of the FPAA is low power. However, the limited number of circuit elements prevents the FPAA as a complete system solution. It is concluded that the FPAA is an attractive energy-efficient solution enabling rapid revision of signal processing functions making is a viable option during testing in animal models when signal processing functions of the VP are being characterized. In contrast, the MSP430 can implement a complete system; however, the power consumption is prohibitive at 22.4 mW.

The custom IC (ASIC) is the most promising in terms of performance, size, and power. To improve the energy-efficiency the design makes use of subthreshold signal processing techniques. More specifically, it should be noted that the power consumption of the Current-to-Frequency converter of the V-to-F dominates the overall power. Therefore, as discussed previously in Section 3.3.5, reducing the inverter transistor dimensions of the Current-to-Frequency inverter stages can improve the overall ASIC power consumption by 87% (162.8 µW). With careful design of the supporting blocks; namely bias circuitry, memory, and DAC; it is projected that a complete system that implements the CST and the VSP for three SCCs and two otoliths can fit inside a square of 6.5 mm x 6.5 mm (42.25 mm^2). A sub-mW power consumption is estimated where the signal processing functions would consume 262.4 µW.

Functionally the ASIC advances the state-of-the-art VP systems by potentially improving stimulation efficacy. Namely, the design (1) provides a precompensation strategy that eliminates false representation of head motions due to current spread, (2) performs both linear and angular motion signal processing, and (3) enables representation of patient-specific data.

In summary the contributions of this research are as follows:

1. FPAA implementation of a vestibular signal processing circuitry.
2. Design and validation of a custom-design VP signal processing circuitry that advances the state-of-the-art by improving both the efficacy of stimulation and energy-efficiency.
3. Design and validation of a novel time-multiplexed VMM circuit operating in subthreshold region.
4. Microcontroller implementation and validation of the vestibular signal processing functions for three SCCs and two otoliths.

5.3. Future Directions

5.3.1. Signal Processing ASIC Performance

- Improving the power consumption. The circuit is designed to benefit from the energy-efficiency of subthreshold analog signal processing. The power performance can be further improved by resizing the inverters of the current controlled oscillator.
- Improving the noise performance to achieve the sensation thresholds of the vestibular organs. Without modifying the architecture of the system, the flicker noise can be reduced by changing the transconductance elements form nMOS-input to pMOS-input and increasing the input transistor dimensions. In general, the larger input devices result in increase in the load capacitances of previous stages, thereby reducing the white noise as well. Furthermore, a PCB prepared for the ASIC would improve the noise performance.
- Designing supporting blocks to program the circuit with patient-dependent parameters. Memory elements, D/A converters, and a digital communication block are necessary to build a complete system.
- System integration and tests with inertial sensors and current stimulators. The measurement results would lead to *in-vivo* testing.

5.3.2. A Complete VP Interface Circuitry

- Design and validation of the following components of the VP interface circuitry.
    - The current stimulator. For improved stimulation efficacy, the design needs to enable multipolar stimulation techniques, namely current steering and focusing [70].
    - Wireless link. The stimulation parameters need to be transmitted to the implant units via an energy-efficient wireless link. The link also needs to transmit power to the implanted units.

- Power management blocks. This block would generate the supply voltages of the signal processing and the stimulator circuitry.

- Performing animal tests of the complete VP interface circuitry to evaluate the performance and explore the design space for future versions.

5.3.3. Reflecting the Biology

- Based on animal experiments, the vestibular neurons that innervate the vestibular organs have been grouped into two; the regular and the irregular neurons. The main difference between the two types is their discharge regularity. The two type of neurons are different in various other aspects including the threshold levels, sensitivities, and response dynamics. The research presented is based on the properties of regular neurons that are believed to encode stimulus more efficiently than the irregular neurons [1]. However, it is also assumed that irregular neurons contribute to the vestibular sensation in distinct ways [1]. Although currently the methods for selective stimulation of the two types of afferents are not known yet, once those techniques are developed, it would be desired to modify the VP system to provide both regular and irregular afferent dynamics, thereby providing the optimum stimulation dynamics that will best replace the natural dynamics.

APPENDIX A

A FINITE ELEMENT ANALYSIS OF A BIOMIMETIC ANGULAR ROTATION SENSOR FOR A VESTIBULAR PROSTHESIS

A finite-element-modeling analysis of a novel fluidic angular rotation sensor for a vestibular prosthesis is presented below [52]. A key function of a VP is to sense angular head rotation. Thus far all experimental VPs have relied upon contemporary gyroscopes that lack the power efficiency necessary for an implantable device. As an effort to build a complete VP system, a purely passive custom-design angular rotation sensor that mimics the natural sensors in a human ear, the semicircular canals (SCCs) is being developed [71]. The cupula-endolymph system of an SCC is modeled as a torsion-pendulum system having a band-pass frequency characteristic [72]. Using COMSOL (COMSOL Inc, Burlington, MA) the SCC is modeled as a structural glass cylindrical disk containing a fluid filled toroidal cavity (Figure A.1(a)). Similar to the SCC model, there are two time constants associated with the band-pass response that determine the sensor dimensions; the radius of the torus= 2.6 mm, and the radius of the lumen, r_d=160 µm. The cupula is modeled as a thin and flexible PMMA (poly methyl methacrylate) metalized diaphragm, having a thickness, t_d. A rigid PMMA structure with a suspended metallized electrode is placed at a distance, d_e, away from the diaphragm serving as the reference electrode. A sense capacitance, C_s, is formed by the sensing and the reference electrodes with a resting value of $C_s = C_{s0}$. The capacitance varies by ΔC_s as the diaphragm responds to angular acceleration applied to the glass structural disk.

A typical diaphragm displacement response to a sinusoidal rotation is shown in Figure A.1(b). In response to normal head rotations frequencies (0.05 to 16 Hz), the diaphragm displacement encodes the angular velocity as shown in Figure A.1(c), and does not vary with the frequency. For 1 Hz of sinusoidal rotation at an angular velocity of 400

˚/sec, the diaphragm displacement is 33.65 nm, 3.72 nm, and 0.35 nm, for t_d= 5 µm, 10 µm, and 20 µm, respectively. When t_d=2 µm, a maximum angular velocity of 500 ˚/sec results in a diaphragm displacement of ~550 nm. Based on the electrostatics simulations; when the angular velocity is changed from +500 ˚/sec to -500 ˚/sec, for d_e=2, 4, and 6 µm; C_{s0}=1.1pF, $\Delta C_{s,max}$=0.44 pF; C_{s0}=0.72 pF, $\Delta C_{s,max}$=0.12 pF; and C_{s0}=0.57 pF, $\Delta C_{s,max}$=0.06 pF, respectively.

Because the custom-design angular rotation sensor presented does not require any vibrating mechanical elements to sense rotations, the power consumption of it is expected to be significantly smaller than most contemporary micro-machined gyroscopes. Furthermore, introducing the band-pass frequency response of the system in the sensor, the need for a band-pass filter in the interface circuitry will be eliminated, which potentially decreases the total power consumption further.

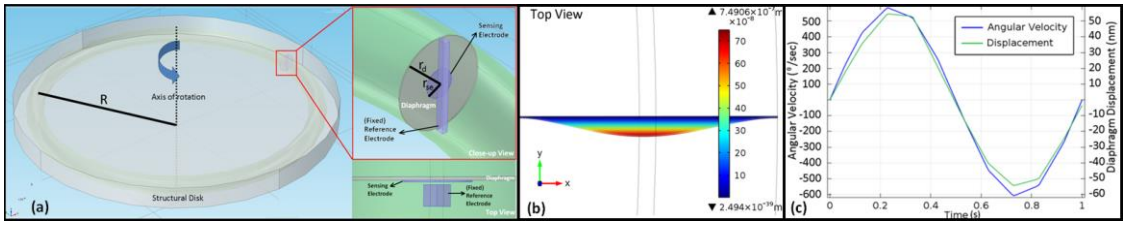


Figure A.1. Angular rotation sensor. (a) Overall model of the simulation environment and sensing and reference electrode. (b) A typical displacement of the diaphragm in response to disk rotation. In this figure t_d=1 µm, and at that instant the maximum displacement, which occurs at the center of the diaphragm, is ~749 nm. (c) The diaphragm displacement in response to a 1 Hz of sinusoidal angular velocity input for t_d=5 µm.

APPENDIX B

MATLAB CODE USED TO GENERATE THE IIR FILTER COEFFICIENTS

```
close all
clear
clc


% Constants
av_scc=0.34;
tau1=4.37;
tau2=7e-3;
tauA_scc=80;

% Zeros, Poles, and Gain
z_scc=[0 0];
p_scc=[-1/tau1 -1/tau2 -1/tauA_scc];
k_scc=av_scc/tau2;

% Continuos Time Transfer Function
H_scc=zpk(z_scc,p_scc,k_scc)

H_zeros=H_scc.z{1}
H_poles=H_scc.p{1}
H_gain=H_scc.k

[H_num,H_den]=zp2tf(H_zeros,H_poles,H_gain);


% Sampling Time
T=1/244;   %244 Hz

% Cont-to-Discrete Time Conversion using FOH method
Hd_scc=c2d(H_scc, T, 'foh') % discretize with FOH method and
                            % T seconds= sample time
Hd_zeros=Hd_scc.z{1};
Hd_poles=Hd_scc.p{1};
Hd_gain=Hd_scc.k;

% Convert pole-zero form into Polynomial form
[Hd_num,Hd_den]=zp2tf(Hd_zeros,Hd_poles,Hd_gain);

% IIR Coefficients (SCC)
A_scc=[Hd_num./Hd_den(1)]
B_scc=[Hd_den(2:length(Hd_den))./Hd_den(1)]

% Constants
av_oto=30;
tauM=46e-3;
tauAz_oto=13.2;
```

```
tauAp_oto=11;

% Zeros, Poles, and Gain
z_oto=[-1/tauAz_oto];
p_oto=[-1/tauAp_oto -1/tauM];
k_oto=av_oto*tauAz_oto/(tauAp_oto*tauM);

% Continuos Time Transfer Function
H_oto=zpk(z_oto,p_oto,k_oto)

% Sampling Time
T=1/220;

% Cont-to-Discrete Time Conversion using FOH method
Hd_oto=c2d(H_oto, T, 'foh') % discretize with FOH method and
                            % T seconds= sample time
Hd_zeros=Hd_oto.z{1};
Hd_poles=Hd_oto.p{1};
Hd_gain=Hd_oto.k;

% Convert pole-zero form into Polynomial form
[Hd_num,Hd_den]=zp2tf(Hd_zeros,Hd_poles,Hd_gain);

% IIR Coefficients (Otoliths)
A_oto=[Hd_num./Hd_den(1)]
B_oto=[Hd_den(2:length(Hd_den))./Hd_den(1)]
```

APPENDIX C

C CODE IMPLEMENTED ON MSP430

```
#include <msp430.h>
#include <math.h>

unsigned int ADCresult1,ADCresult2,ADCresult3,ADCresult4,ADCresult5,ADCresult6;
unsigned int tanh_freq_1,tanh_freq_2,tanh_freq_3,tanh_freq_1o,tanh_freq_2o;

// VMM coefficients
const float vmm[3][3]={
  {1,  0,  0},
  {0, -1, -1},
  {0,  0,  1}
};

const float vmm2[3][2]={
  {0.5,  0},
  {0.5, -1},
  {0,    0}
};


//SCC IIR Coefficients calculated when fs=244.4 Hz.
const float A[4]= {0.0825074307814478,-0.0971031527358560,-
0.0533159868726316,0.0679117088270398};    /*numerator coefficients*/
const float B[3]= {-2.55638528827951,2.11320750292066,-0.556822193455079}; /*denominator
coefficients*/

//Otolith IIR Coefficients calculated when fs=244.4 Hz.
const float Ao[3]= {1.72144990880856,-0.0552191934260081,-1.66506456358121};    /*numerator
coefficients*/
const float Bo[2]= {-1.90549784638096,0.905536718107667}; /*denominator coefficients*/



volatile float X_1[3]= {0};          /*delay samples*/
volatile float Y_1[3]= {0};          /*delay samples*/
volatile float X_2[3]= {0};          /*delay samples*/
volatile float Y_2[3]= {0};          /*delay samples*/
volatile float X_3[3]= {0};          /*delay samples*/
volatile float Y_3[3]= {0};          /*delay samples*/
volatile float X_oto1[2]= {0};         /*delay samples*/
volatile float Y_oto1[2]= {0};         /*delay samples*/
volatile float X_oto2[2]= {0};         /*delay samples*/
volatile float Y_oto2[2]= {0};         /*delay samples*/
volatile float x_1,y_1,x1_1,x2_1,x3_1,x4_1,y1_1,y2_1,y3_1,period_1;
volatile float x_2,y_2,x1_2,x2_2,x3_2,x4_2,y1_2,y2_2,y3_2,period_2;
volatile float x_3,y_3,x1_3,x2_3,x3_3,x4_3,y1_3,y2_3,y3_3,period_3;
volatile float x_oto1,y_oto1,x1_1o,x2_1o,x3_1o,x4_1o,y1_1o,y2_1o,y3_1o,period_oto1;
volatile float x_oto2,y_oto2,x1_2o,x2_2o,x3_2o,x4_2o,y1_2o,y2_2o,y3_2o,period_oto2;
int i;
```

```
float
dc=1548,Gper=100000,tanh_slope=400,tanh_mag=1280,dco=1548,Gpero=100000,tanh_slopeo=80000,tan
h_mago=1280;


int main(void)
{
  WDTCTL = WDTPW + WDTHOLD;                 // Stop WDT

  FLL_CTL0 |= DCOPLUS + XCAP18PF;           // DCO+ set, freq = xtal x D x N+1
  SCFI0 |= FN_4;                            // x2 DCO freq, 8MHz nominal DCO
  SCFQCTL = 121;                              // (121+1) x 32768 x 2 = 7.99 MHz
  P6SEL |= 0x3F;                            // SCC Inputs are sampled on P6.0, P6.1, and P6.2
                                  // Otolith Inputs are sampled on P6.3, P6.4, and P6.5
  P2SEL |= 0x0C;                            // P2.2,3 option select
  P2DIR |= 0x0C;                            // P2.2,3 outputs
  P3SEL |= 0x10;                            // P3.4 option select
  P3DIR |= 0x10;                           // P3.4 output
  P10DIR |=0x7F;                            // P10.0, P10.1, and P10.2 are outputs for CLK1s of CH1-CH2-CH3,
P10.3-P10.6 are outputs for CLK1s and CLK2s of Otolith CH1 and CH2
  P9DIR |=0xE0;                             // P9.0, P9.1, and P9.2 are outputs for CLK2s of CH1-CH2-CH3

  P1DIR |=0x08;                             // P1.3 output

  ADC12CTL0 = ADC12ON|SHT0_11|MSC|REF2_5V|REFON;     // Turn on ADC12, Sample and hold
256 ADC12CLK cycles
  //TBCCR0 = 13600;                         // Delay to allow Ref to settle
  //TBCCTL0 |= CCIE;                        // Compare-mode interrupt.
  //TBCTL = TBCLR + MC_1 + TBSSEL_2;          // up mode, SMCLK
  //__bis_SR_register(LPM0_bits + GIE);       // Enter LPM0, enable interrupts
  //TBCCTL0 &= ~CCIE;                       // Disable timer interrupt
  //__disable_interrupt();                  // Disable Interrupts

  ADC12CTL1 = SHP|CONSEQ_3|ADC12SSEL_0|ADC12DIV_3;      // Use sampling timer, set mode
  ADC12IE = 0x10;                                 // Enable ADC12IFG.4 for ADC12MEM2
  ADC12MCTL0 = SREF_1|INCH_0;                     // ADC0 Vref+ and GND, A0 goes to MEM0
  ADC12MCTL1 = SREF_1|INCH_1;                     // ADC1 Vref+ and GND, A1 goes to MEM1
  ADC12MCTL2 = SREF_1|INCH_2;                     // ADC2 Vref+ and GND, A2 goes to MEM2
  ADC12MCTL3 = SREF_1|INCH_3;                     // ADC3 Vref+ and GND, A3 goes to MEM3
  ADC12MCTL4 = SREF_1|INCH_4;                     // ADC4 Vref+ and GND, A4 goes to MEM4
  ADC12MCTL5 = SREF_1|INCH_5|EOS;             // ADC5 Vref+ and GND, A4 goes to MEM4, end of
sequence
  __enable_interrupt();                           // Enable interrupts

  while(1)
  {

  DAC12_0CTL = DAC12IR + DAC12AMP_5 + DAC12ENC; // Int ref gain 1
  ADC12CTL0 |= ENC;                       // Enable conversions
  ADC12CTL0 |= ADC12SC;                     // Start conversion

  //VMM

  x_1=((long)ADCresult1*vmm[0][0])+((long)ADCresult2*vmm[1][0])+((long)ADCresult3*vmm[2][0]);
  x_2=((long)ADCresult1*vmm[0][1])+((long)ADCresult2*vmm[1][1])+((long)ADCresult3*vmm[2][1]);
  x_3=((long)ADCresult1*vmm[0][2])+((long)ADCresult2*vmm[1][2])+((long)ADCresult3*vmm[2][2]);
```

```
x_oto1=((long)ADCresult4*vmm2[0][0])+((long)ADCresult5*vmm2[1][0])+((long)ADCresult6*vmm2[2][0]);

x_oto2=((long)ADCresult4*vmm2[0][1])+((long)ADCresult5*vmm2[1][1])+((long)ADCresult6*vmm2[2][1]);

 //SCC 1
 //x_1=(long)ADCresult1;
 x1_1=A[0]*x_1;
 x2_1=A[1]*X_1[0];
 x3_1=A[2]*X_1[1];
 x4_1=A[3]*X_1[2];
 y1_1=B[0]*Y_1[0];
 y2_1=B[1]*Y_1[1];
 y3_1=B[2]*Y_1[2];
 y_1=x1_1+x2_1+x3_1+x4_1-y1_1-y2_1-y3_1;
 X_1[2]=X_1[1];
 X_1[1]=X_1[0];
 X_1[0]=x_1;
 Y_1[2]=Y_1[1];
 Y_1[1]=Y_1[0];
 Y_1[0]=y_1;

 tanh_freq_1=dc+tanh_mag*tanh(y_1/tanh_slope);
 period_1=Gper/tanh_freq_1;
 //DAC12_0DAT=tanh_freq_1;

 //SCC 2
 //x_2=(long)ADCresult2;
 x1_2=A[0]*x_2;
 x2_2=A[1]*X_2[0];
 x3_2=A[2]*X_2[1];
 x4_2=A[3]*X_2[2];
 y1_2=B[0]*Y_2[0];
 y2_2=B[1]*Y_2[1];
 y3_2=B[2]*Y_2[2];
 y_2=x1_2+x2_2+x3_2+x4_2-y1_2-y2_2-y3_2;
 X_2[2]=X_2[1];
 X_2[1]=X_2[0];
 X_2[0]=x_2;
 Y_2[2]=Y_2[1];
 Y_2[1]=Y_2[0];
 Y_2[0]=y_2;

 tanh_freq_2=dc+tanh_mag*tanh(y_2/tanh_slope);
 period_2=Gper/tanh_freq_2;
 //DAC12_0DAT=tanh_freq_2;

 //SCC 3
 //x_3=(long)ADCresult3;
 x1_3=A[0]*x_3;
 x2_3=A[1]*X_3[0];
 x3_3=A[2]*X_3[1];
 x4_3=A[3]*X_3[2];
```

```
y1_3=B[0]*Y_3[0];
y2_3=B[1]*Y_3[1];
y3_3=B[2]*Y_3[2];
y_3=x1_3+x2_3+x3_3+x4_3-y1_3-y2_3-y3_3;
X_3[2]=X_3[1];
X_3[1]=X_3[0];
X_3[0]=x_3;
Y_3[2]=Y_3[1];
Y_3[1]=Y_3[0];
Y_3[0]=y_3;

tanh_freq_3=dc+tanh_mag*tanh(y_3/tanh_slope);
period_3=Gper/tanh_freq_3;
//DAC12_0DAT=tanh_freq_3;

//Otolith 1
x1_1o=Ao[0]*x_oto1;
x2_1o=Ao[1]*X_oto1[0];
x3_1o=Ao[2]*X_oto1[1];
y1_1o=Bo[0]*Y_oto1[0];
y2_1o=Bo[1]*Y_oto1[1];
y_oto1=x1_1o+x2_1o+x3_1o-y1_1o-y2_1o;
X_oto1[1]=X_oto1[0];
X_oto1[0]=x_oto1;
Y_oto1[1]=Y_oto1[0];
Y_oto1[0]=y_oto1;

tanh_freq_1o=dco+(tanh_mago*tanh(y_oto1/tanh_slopeo));
period_oto1=Gpero/tanh_freq_1o;
DAC12_0DAT=tanh_freq_1o;

//Otolith 2
x1_2o=Ao[0]*x_oto2;
x2_2o=Ao[1]*X_oto2[0];
x3_2o=Ao[2]*X_oto2[1];
y1_2o=Bo[0]*Y_oto2[0];
y2_2o=Bo[1]*Y_oto2[1];
y_oto2=x1_2o+x2_2o+x3_2o-y1_2o-y2_2o;
X_oto2[1]=X_oto2[0];
X_oto2[0]=x_oto2;
Y_oto2[1]=Y_oto2[0];
Y_oto2[0]=y_oto2;

tanh_freq_2o=dco+tanh_mago*tanh(y_oto2/tanh_slopeo);
period_oto2=Gpero/tanh_freq_2o;
//DAC12_0DAT=tanh_freq_2o;


TBCCTL1 = OUTMOD_4+CCIE;                // TBCCR1 interrupt enabled
TBCCTL2 = OUTMOD_4+CCIE;                // TBCCR2 interrupt enabled
TBCCTL3 = OUTMOD_4+CCIE;                // TBCCR3 interrupt enabled
TBCCTL4 = OUTMOD_4+CCIE;                // TBCCR4 interrupt enabled
TBCCTL5 = OUTMOD_4+CCIE;                // TBCCR5 interrupt enabled

TBCTL = TBSSEL_1+MC_2+TBIE;             // SMCLK, continuous mode, interrupt enabled
```

```
  P2IE |= 0xE3 ;  // Interrupt on Input Pin P2.0, P2.1, P2.5, P2.6, and P2.7
  P2IES |= 0xE3 ; // High to Low Edge Pin P2.0, P2.1, P2.5, P2.6, and P2.7

  __bis_SR_register(LPM3_bits + GIE);       // Enter LPM3
  }
  }

// Interrupt Vectors: (1) ADC12 Interrupt (2) Timer B1 Interrupt (3) Port2 Interrupt
#pragma vector = ADC12_VECTOR
__interrupt void ADC12_ISR(void)
{
  ADCresult1 = ADC12MEM0;
  ADCresult2 = ADC12MEM1;
  ADCresult3 = ADC12MEM2;
  ADCresult4 = ADC12MEM3;
  ADCresult5 = ADC12MEM4;
  ADCresult6 = ADC12MEM5;
  P1OUT ^= 0x08;

  //__no_operation();                       // SET BREAKPOINT HERE
  __bic_SR_register_on_exit(LPM3_bits);    // Exit LPM3
}


// Timer_B1 Interrupt Vector (TAIV) handler
#pragma vector=TIMERB1_VECTOR
__interrupt void Timer_B1(void)
{
  switch( TBIV )
  {
  case  2:
  TBCCR1 += period_1;                     // Add Offset to TACCR1
  break;

  case  4:
  TBCCR2 += period_2;                     // Add Offset to TACCR1
  break;

  case  6:
  TBCCR3 += period_3;                     // Add Offset to TACCR2
  break;

  case  8:
  TBCCR4 += period_oto1;                      // Add Offset to TACCR2
  break;

  case  10:
  TBCCR5 += period_oto2;                      // Add Offset to TACCR2
  break;
  }
}


#pragma vector = PORT2_VECTOR
__interrupt void InterruptVectorPort2()
{
```

```
if(P2IFG & 0x01)
{
//P10OUT &= ~0x01;                    // P10.0 = 0
//for(i=1;i>0;i--);                   // IPG (delay)
//{
//}
P10OUT |= 0x01;                       // P10.0 = 1
for(i=870;i>0;i--);                   // IPG (delay)
{
}
P10OUT &= ~0x01;                      // P10.0 = 0
for(i=868;i>0;i--);                   // IPG (delay)
{
}
P9OUT &= ~0x020;                      // P9.5 = 0
for(i=0;i>0;i--);                     // IPG (delay)
{
}
P9OUT |= 0x020;                       // P9.5 = 1
for(i=870;i>0;i--);                   // IPG (delay)
{
}
P9OUT &= ~0x020;                      // P9.5 = 0
for(i=1;i>0;i--);                     // IPG (delay)
{
}
P2IFG &= ~0x01; // Clear Interrupt Flag
}

if(P2IFG & 0x02)
{
P10OUT &= ~0x02;                      // P10.1 = 0
for(i=92;i>0;i--);                    // IPG (delay)
{
}
P10OUT |= 0x02;                       // P10.1 = 1
for(i=92;i>0;i--);                    // IPG (delay)
{
}
P10OUT &= ~0x02;                      // P10.1 = 0
for(i=10;i>0;i--);                    // IPG (delay)
{
}
P9OUT &= ~0x040;                      // P9.6 = 0
for(i=92;i>0;i--);                    // IPG (delay)
{
}
P9OUT |= 0x040;                       // P9.6 = 1
for(i=92;i>0;i--);                    // IPG (delay)
{
}
P9OUT &= ~0x040;                      // P9.6 = 0
for(i=10;i>0;i--);                    // IPG (delay)
{
}
P2IFG &= ~0x02; // Clear Interrupt Flag
```

```
}

if(P2IFG & 0x80)
{
P10OUT &= ~0x04;                    // P10.2 = 0
for(i=92;i>0;i--);                  // IPG (delay)
{
}
P10OUT |= 0x04;                     // P10.2 = 1
for(i=92;i>0;i--);                  // IPG (delay)
{
}
P10OUT &= ~0x04;                    // P10.2 = 0
for(i=10;i>0;i--);                  // IPG (delay)
{
}
P9OUT &= ~0x080;                    // P9.7 = 0
for(i=92;i>0;i--);                  // IPG (delay)
{
}
P9OUT |= 0x080;                     // P9.7 = 1
for(i=92;i>0;i--);                  // IPG (delay)
{
}
P9OUT &= ~0x080;                    // P9.7 = 0
for(i=10;i>0;i--);                  // IPG (delay)
{
}
P2IFG &= ~0x80; // Clear Interrupt Flag
}

if(P2IFG & 0x20)
{
P10OUT &= ~0x08;                    // P10.3 = 0
for(i=92;i>0;i--);                  // IPG (delay)
{
}
P10OUT |= 0x08;                     // P10.3 = 1
for(i=92;i>0;i--);                  // IPG (delay)
{
}
P10OUT &= ~0x08;                    // P10.3 = 0
for(i=10;i>0;i--);                  // IPG (delay)
{
}
P10OUT &= ~0x10;                    // P10.4 = 0
for(i=92;i>0;i--);                  // IPG (delay)
{
}
P10OUT |= 0x10;                     // P10.4 = 1
for(i=92;i>0;i--);                  // IPG (delay)
{
}
P10OUT &= ~0x10;                    // P10.4 = 0
for(i=10;i>0;i--);                  // IPG (delay)
{
```

```
  }
  P2IFG &= ~0x20; // Clear Interrupt Flag
  }

  if(P2IFG & 0x40)
  {
  P10OUT &= ~0x20;                    // P10.5 = 0
  for(i=92;i>0;i--);                  // IPG (delay)
  {
  }
  P10OUT |= 0x20;                     // P10.5 = 1
  for(i=92;i>0;i--);                  // IPG (delay)
  {
  }
  P10OUT &= ~0x20;                    // P10.5 = 0
  for(i=10;i>0;i--);                  // IPG (delay)
  {
  }
  P10OUT &= ~0x40;                    // P10.6 = 0
  for(i=92;i>0;i--);                  // IPG (delay)
  {
  }
  P10OUT |= 0x40;                     // P10.6 = 1
  for(i=92;i>0;i--);                  // IPG (delay)
  {
  }
  P10OUT &= ~0x40;                    // P10.6 = 0
  for(i=10;i>0;i--);                  // IPG (delay)
  {
  }
  P2IFG &= ~0x40; // Clear Interrupt Flag
  }

}
```

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