LOW VOLTAGE AUTONOMOUS BUCK-BOOST REGULATOR

FOR WIDE INPUT ENERGY HARVESTING

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[Dedicated to My Family]

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SUMMARY

While high power buck-boost regulators have been extensively researched and developed in the academia and industry, low power counterparts have only recently gained momentum due to the advent of different battery powered and remote electronics. The application life-time of such applications, e.g., remote surveillance electronics can be extended tremendously by enabling energy autonomy. While battery powered electronics last long but they must be replenished once the battery is depleted either by replacing the battery or by retrieving the electronics and then recharging. Instead, energy harvesting from available ambient sources on the spot will enable these electronics continuous operation unboundedly, probably even beyond the lifetime of the electronics. Interestingly enough, recent advancements in micro-scale energy transducers compliment these demand [1-13]. Micro-transducers producing energy from different ambient sources have been reported. These transducers produce enough energy to support a wide range of operations of the remote electronics concurrently. These transducers along with an additional storage elements greatly increase the energy autonomy as well as guaranteed operation since harvested energy can then be stored for future use when harvestable energy is temporarily unavailable.

Recently several buck-boost regulators with low power and low input operating voltage have been reported both from academia and industry [14-24]. Some of this work focuses on increasing efficiency in the mid-load range (10mA-100mA), while some other focuses on lowering input range. However, so far no one has reported a buck-boost regulator operating with sub-200nW bias power while harvesting energy from sub-500mV

input range. This work focuses on the development of a low voltage low bias current buck-boost regulator to attain these goals.

In this work, complete design of a PFM mode buck-boost regulator has been discussed in details. Basic topology of the regulator and working principle of the implemented architecture along with the advantages of the specific topology over that of the others have been discussed in short to provide an uninterrupted flow of idea. Later, Transistor level design of the basic building blocks of the buck-boost regulator is discussed in details with different design features and how those are attained through transistor level implementation are discussed. Subsequently, the physical layout design technique and considerations are discussed to inform the reader about the importance of the layout process and to avoid pitfalls of design failure due to layout quality issues.

Measurement results are presented with the fabricated IC. Different characterization profile of the IC have been discussed with measured data and capture oscilloscope waveforms. Load regulation, line regulation, efficiency, start-up from low voltage, regulation with line and load transient events are measured, presented and discussed. Different characteristics of the prototype are compared with prior arts and are presented in a comparison table. Die micrograph is also presented along with the different issue of the IC testing.

CHAPTER 1

INTRODUCTION

Autonomous and battery power sensor networks are increasing in all application domains including, but not limited to, body area network, wireless sensor networks, structure monitoring, agricultural and environmental sensing, remote surveillance and space applications. Due to the recovery difficulty of the deployed sensors, in many systems, replenishing the discharged battery is difficult and in some cases, it is impossible. This draws the end of operating life for the whole electronics systems. Energy harvesting from ambient sources overcome this shortcoming by replenishing battery on the point of operation, without the need to collect them for recharging. Harvesting ambient energy however has its own challenges such as unpredictable energy output, variable and small potential difference as well as low energy throughput. Recent development of the energy transducers made harvesting easier however the challenge remains [1-13]. For example, while some transducers converts ambient photonic energy into electrical one, the potential difference at the transducers' output remains very low. Same goes for thermoelectric generators those produce electrical energy from temperature differential. Transducers such as [7,9,10] produce only 20mV-50mV from a temperature difference of 5°-10°C. The output is highly depended on temperature difference hence, as the temperature difference increases, the output voltage increases too. Other energy transducers such as, Photovoltaic (PV) cells and piezoelectric transducers have similar characteristics of producing very low to moderately high output voltage depending on ambient source condition. Since

electronics reliably operate only on a narrow region of bias, the energy produces by the transducers must be conditioned before being used for biasing. Conventionally, either boost or buck based energy conditioning circuits are used to provide regulated output either by increasing the transducer voltage or by decreasing it. A buck-boost regulator offers the advantage of both decreasing and increasing the source voltage while regulating a fixed output. A buck-boost regulator greatly increases the range of operation for energy harvesting transducers thereby harvesting more energy than either the buck or the boost system.

Energy sources generally produce widely varying output voltage, for which the following energy conditioning circuits are required to work from wide range of input. Buck-boost regulators are convenient since it guarantees a regulated output with wide range on input, both above and below the regulated output. Several works have been reported [14-24], those advances the use of buck-boost regulator in different application domain including photovoltaic and piezoelectric energy harvesting devices.
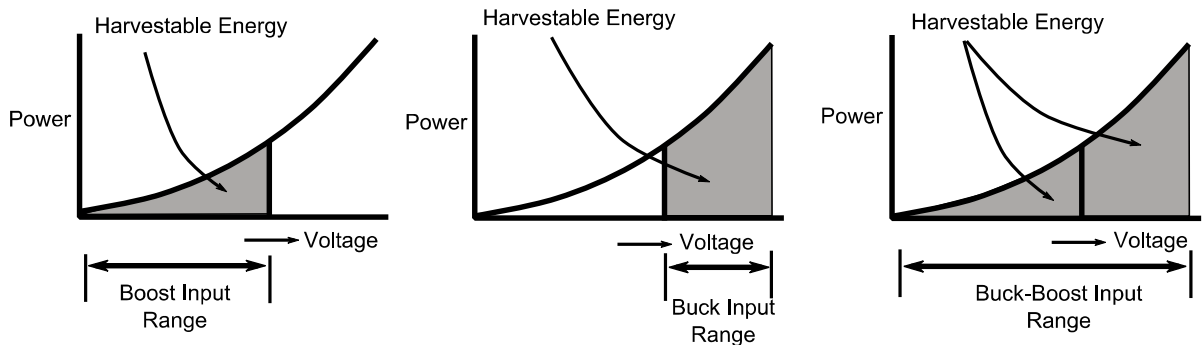
Fig.1.1: Pictorial representation of increased operating input range and harvestable energy through buck-boost topology in contrast with either boost or buck regulator.

Energy harvesting Buck-boost regulator in the literature and industry

High and medium power buck boost regulator has been extensively developed. However, low power counterparts have only recently gained interest due to the advent of battery powered and semi-autonomous electronics for wireless and remotely operated electronic applications. Several prior arts have been reported from both academia and industries[14-24]. Some of these works focus on increasing the efficiency in the mid-load range (10mA-100mA), while some other focuses on lowering input range. However, so far no one has reported a buck-boost regulator operating with sub-200nW bias power while harvesting energy from sub-500mV input range. This work focuses on the development of a low voltage low bias current buck-boost regulator to attain these goals.

Development of this thesis

This work focuses on the self-consumption minimization of the regulator and widening range of operating input voltage. A complete design of a PFM mode buck-boost regulator has been discussed in details. Basic topology of the switching regulator and working principle of the implemented architecture along with the advantages of the specific topology over that of the others have been discussed in short to provide an uninterrupted flow of idea in chapter 2. Later, in chapter 3, Transistor level design of the basic building blocks of the buck-boost regulator is discussed in details with different design features and how those are attained through transistor level implementation are discussed.

Chapter 4 discusses the measurement results are presented with the fabricated IC. Different characterization profile of the IC have been discussed with measured data and capture oscilloscope waveforms. Load regulation, line regulation, efficiency, start-up from low voltage, regulation with line and load transient events are measured, presented and discussed. Different characteristics of the prototype are compared with prior arts and are presented in a comparison table. Die micrograph is also presented along with the different issue of the IC testing. Chapter 5 discusses provides some insights in design limitations and proposes some future extension of this work. Chapter 6 concludes the works. Chapter 7 provides an appendix discussing the physical layout design process and techniques. This chapter is intended to provide some hands on guideline for custom layout design process and constraints. These techniques and considerations are discussed to inform the reader to avoid pitfalls of design failure due to layout quality issues.

CHAPTER 2

BUCK-BOOST ARCHITECTURE

The chapter discusses the top-level architecture of the design along with the functional block diagram and operating principle.

PWM / PFM architecture comparison

A switching regulator consists of primarily a complimentary power stages, an inductive element and capacitors at the input and output nodes. The topologies differ only in the generation of the control signal of the power stage. In PWM, as the name suggests, the pulse of the basic oscillator is modified by the error amplifier, which truncates the pulse and hence decides the duty cycle. PWM duty cycle decision is generated at every pulse. Each pulse is initiate by the oscillator and terminated by the error amplifier. When over drive is necessary, the error amplifier is clamped, and the duty cycle is at its highest value, a value usually predefined and inherent with the oscillator pulse.   In PWM architecture, the regulator is switching at a fixed frequency. The duty cycle in PWM architecture also defines the ratio of input to output by the following equation

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN}} \tag{2.1}$$

$$D_{BOOST} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{2.2}$$

PFM, on the other hand, does not control the duty cycle at every oscillator pulse. It rather enables and disables the oscillator itself, depending on the relative position of the output voltage and reference voltage. During the time when oscillator is enabled, the pulses

generated are all at maximum duty cycle. At the other time, when the oscillator is disabled, the signal remains low, turning the power stage off. In PFM, the burst of pulses are followed by the idle time. Because the decisions are not made at every pulse, there exist no closed loop analytical duty cycle equation for the PFM converters.

Table I : Comparison chart of PWM and PFM architectures

Item	PWM	PFM
Output sensing	Error amplifier	Comparator
Compensation	Yes. Pole-Zero compensations required for stable operation	No compensation is required
Output ripple	Ripple does not change with load current	Ripple might change with load current.
Frequency	Fixed. Does not depend on load or input/output voltage.	Maximum frequency is fixed, but operation frequency may be lower and variable.
Self-power consumption	Higher	Lower
Scalability / Digital Integration	Difficult	Easier

Buck-Boost Operation Principle

The buck-boost regulator delivers regulated output voltage from input that can be either higher or lower than the output voltage. Hence it incorporates more switches than
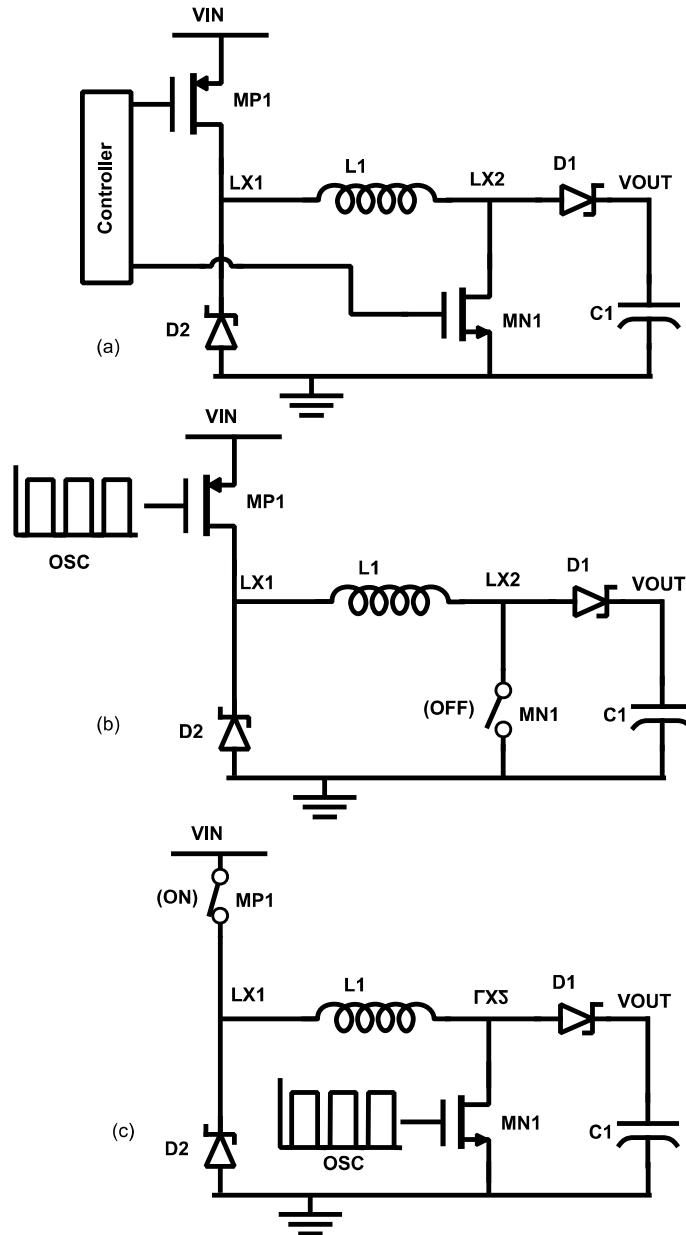
Fig. 2.1: Conceptual diagram of buck-boost regulator. (a) Simplified buck-boost diagram. The controller takes in OSC signal and depending on the mode select comparators output, decides to control either MP1 or MN1. (b) Buck operation. NFET MN1 remains off during this mode while PFET MP1 is controlled by the OSC signal that in turns charges the output through the inductor, and (c) boost operation. MN1 is controlled by the OSC while MP1 remains on to connect the input (VIN) to the inductor.

either boost or buck regulators. This subsection discusses the operating principle of the PFM mode Buck-Boost regulator.

Fig. 2.1 shows the conceptual system level diagram of a buck boost regulator with two active switches (MP1, MN1) and two passive devices (D1, D2). The active switches are controlled by the circuit block 'controller' which, based on the relative position of output and reference voltages, decides the oscillator enable/disable timings. During buck mode operation (when input is higher than output), the switch configurations are shown in Fig. 2.1(b). Switch MN1 remains OFF and diode D2 remains on for the whole duration of buck operation. The controller signal controls the MP1 gate using the oscillator signal, alternately turning it on and off. This let the inductor current to build up and ultimately energy is transferred to the output. The diode, D1 also operates in this mode, but in complementary fashion with respect to MP1. The boost mode-switching configuration is shown in Fig. 2.1 (c). In this mode, the switch MP1 (constantly on) and diode D2 (constantly reversed biased) remain passive, while MN1 and Diode D1 switches complimentarily. When MN1 is on, the inductor current builds up. At the end of the charging phase, the MN1 turns off, and the built up current in the inductor forces the D1 to turn on thus charging the output capacitor and increasing the output voltage. Once the output reaches higher than the reference voltage, the comparator turns off the oscillator and the converter goes into idle mode with both MP1 and MN1 off. During idle time in both buck and boost mode, the output voltage discharges under the load current. The oscillator turns back on when the output is discharged below the reference threshold, and the cycle repeats itself.

PFM mode Buck-Boost functional block diagram

Fig. 2.2 shows the functional block diagram of the PFM mode buck-boost regulator. The regulator senses the output voltage via external feedback network and regulates that at an externally set level. The input is sensed to switch the mode from the boost to the buck when the input voltage goes above the output voltage. The feedback voltage (VFB) is compared against internally generated reference (VREF) and EN signal is generated. This signal (EN)

Fig. 2.2: Functional block diagram of the proposed PFM boost regulator. Shaded boundary represents the proposed chip. External components, shown outside the shaded line, are required for the operation of the regulator.

can be viewed as top level architectural duty cycle. The EN signal determines the active mode and the idle mode of the converter. When VFB is lower than VREF, the EN is high and this forces the converter in active mode. During active mode the oscillator is turned on and it generates high duty cycle pulses. This pulse train propagates to the power stage through the driver circuits. Depending on the relative input level with respect to the output (whether lower or higher) the mode select comparator selects boost mode or buck mode respectively. In boost mode, the power FET MP1 is always on and NFET M1 is driven by the oscillator signal. On the other hand, when input is higher than the output voltage, the converter is in buck mode. In this mode NFET MN is fully turned off and PFET MP is driven by the inverted oscillator signal.

This buck-boost regulator consists for several circuit blocks for different functionality. The following subsections discuss the design of these circuit blocks. Some of the circuits are presented in an earlier work [25] and reused here with minor modification.

Oscillator

The circuit schematic of the proposed oscillator is shown in Fig. 2.3. The oscillator utilizes on-chip capacitors and internally generated current to produce high duty cycle binary pulse. The ON time and OFF time (T_{ON} and T_{OFF}) are produced by two symmetric, n-MOS threshold based comparators differing only in capacitor values (C_1 and C_2) and charging currents (I_1 and I_2 by means of widths of M_3 and M_8). Switches S_1 and S_2 are complementary current bypass paths to reset the capacitors at the end of the respective periods. At the beginning of T_{OFF} (signal OSC is low), S_2 opens allowing the current $I_2$to charge C_2, whose voltage rises linearly. Once the capacitor voltage crosses the threshold

of M_6, it pulls down the drain node which in turn generates a positive edge at 'S' input of the latch. This changes the states of OSC from low to high and marking the end of T_{OFF} and the beginning of T_{ON} phase. At the same time, switch S_2 closes, resetting the capacitor C_2 and switch S_1 opens initiating the charging of C_1. Similarly, when the increasing voltage of C_1 crosses the M_1 threshold, a positive edge is generated at 'R' input and marking the end of T_{ON}, and also the beginning of the next T_{OFF} period. The ratio of I_1/C_1 to I_2/C_2 determines the ratio of high time to low time. In this design, the $I_1/I_2 = 10$(designed by controlling widths of M3 and M8) and $C_1/C_2 = 7$, resulting a theoretical T_{ON}/T_{OFF} ratio of 70. However, in practice this ratio will change due to parasitic capacitances and threshold offsets. The discrepancies will be discussed further in the result section. The output of the oscillator is masked by the output of the feedback comparator (EN); OSC remains low when EN is low, and when EN is high, the output switches between high and low (regular operation).
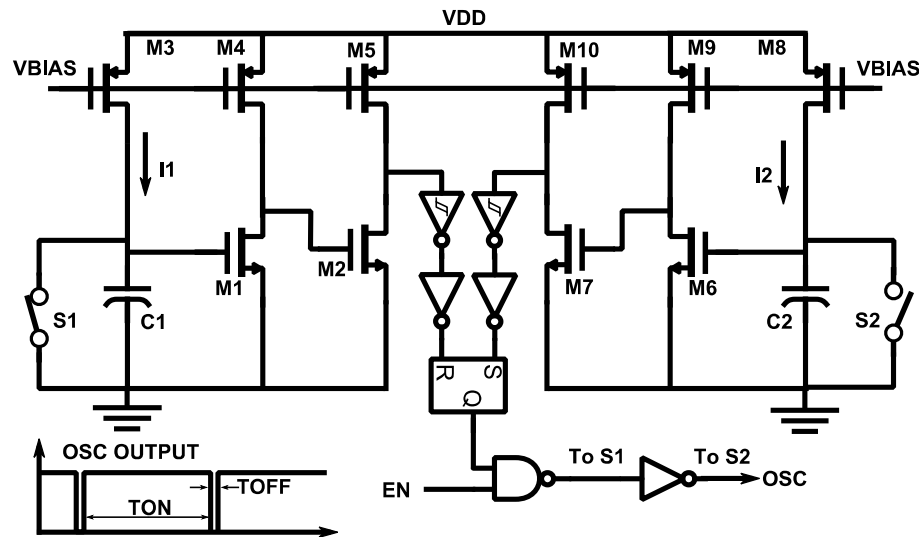
Fig. 2.3: Schematic of the oscillator circuit

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Reference and bias generator

The reference block has simplified supply independent current generator and V_{BE}-based reference voltage generator as shown in Fig. 2.4. A source degenerated MOSFET is used to generate the current that is mirrored through a diode and fed back to the same MOSFET to generate the negative feedback mechanism as shown in Fig. 4(a). Current in each branch is defined by the equation

$$I_{branch} = \frac{2}{\mu_0 C_{ox}(W/L)} \frac{1}{R^2} \left\{ 1 - \frac{1}{\sqrt{K}} \right\}^2 \tag{2.3}$$

where R, μ_0, C_{ox} and (W/L) are respectively, source degeneration resistance, carrier mobility, unit gate oxide capacitance and aspect ratio of the MOSFET while K is the aspect ratio factor between the current generating device M_2 and the diode connected n-MOS device M_1[26]. The ratio K is chosen to be 4 for this design. The generated bias current is mirrored in all other blocks. For simplicity the block level schematics (Oscillator, feedback comparator and current limiter circuit) are drawn with V_{BIAS} only, although in reality, all block level V_{BIAS} are locally generated through the standard current mirroring technique which too is shown in Fig. 2.4.

REFERENCE

VBIAS Generation at Block Levels
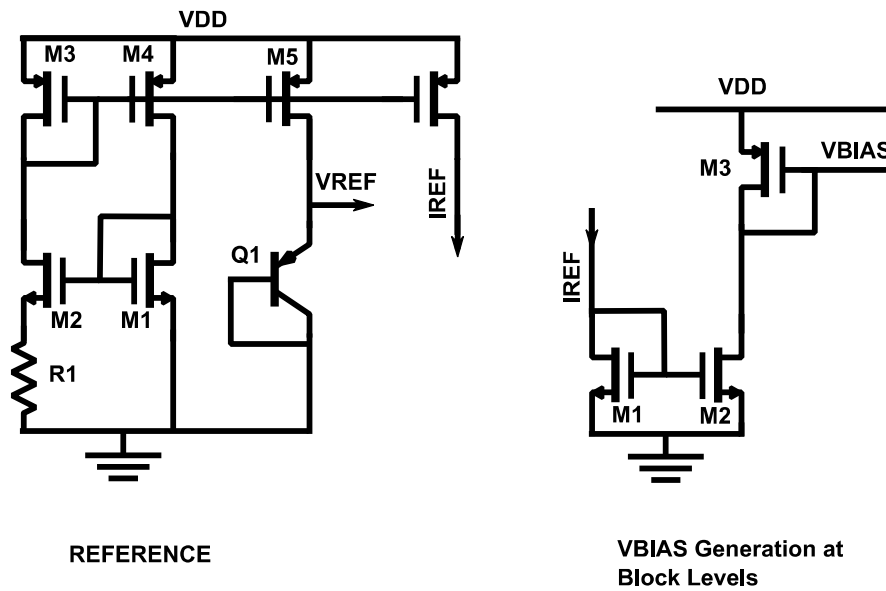
Fig. 2.4: Schematic diagram of the Reference and block level bias generation circuits

The design eliminates complex temperature correction and close loop bandgap reference generation techniques to reduce area and power overhead. The design choice is a tradeoff between temperature insensitivity with continuous biasing overhead and is justified by the fact that in many applications (e.g., Body area network) the actual operating range of temperature is quite narrow. The circuit is designed without cascoding element helping it to start generating current at subthreshold bias levels. Additionally fewer branches and elimination of the close loop control ensures only small bias current consumption.

Feedback Comparator block

Feedback comparator works as the core decision making circuitry for this hysteresis mode converter. Feedback voltage is sensed via the external resistive network and fed to the internal hysteretic comparator's negative input terminal. As shown in Fig. 2.5, the positive terminal of the comparator is connected to the internally generated reference. When the feedback signal is lower than reference, the output (EN) goes high, activating the oscillator. With successive pulses from oscillator, the output gets charged up and the feedback voltage reaches above the hysteresis threshold (15mV above the V_{REF}) of the comparator. Once the

Fig. 2.5: Feedback Comparator

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threshold is crossed, EN goes low, and this masks the oscillator output making it low as well. Also, the oscillator remains in idle mode until the EN goes high again which occurs when feedback falls below the reference as explained earlier. The feedback circuit consumes ~1μA of bias current. The design trade-off with such low bias cur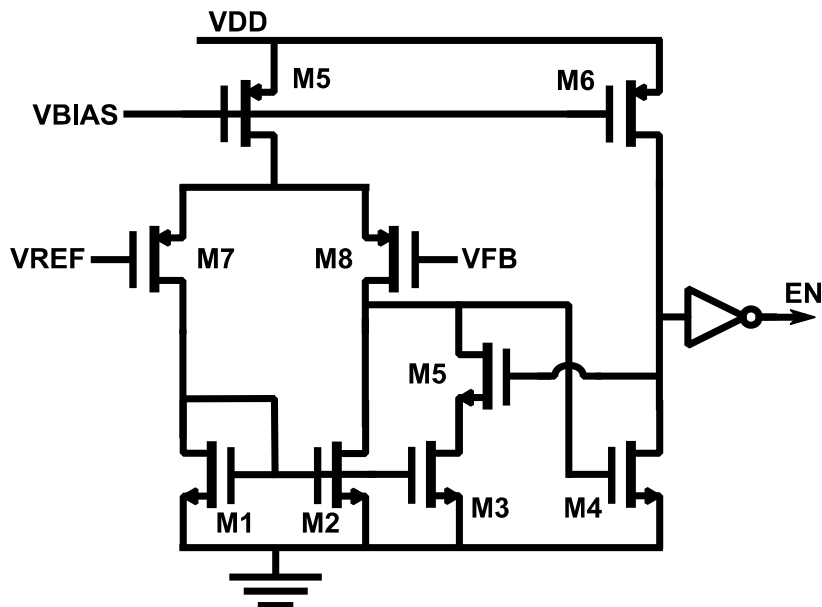rent is the delay of the comparator response time. The simulated delay is nearly 400ns that is expected to result a decrease of the regulated valley of the output voltage at different load conditions. The effect of delay is expected to be prominent at higher load condition. Further discussion is provided in the load regulation subsection under measurement results section. The cascode free design allows very low operating voltage of the comparator which in turn ensures that during low voltage self-start condition, the EN signal stays in the right condition to enable the oscillator.

Current Limit Circuit

For high impedance and low output current energy transducers, current limiter circuit is of crucial importance, lest the high inrush current cause severe droop resulting failure during start up. Fig. 2.6 shows the common gate configured current limiting circuit that compares current sense input (CS) with internally generated current sense reference (CS_{REF}). CS is generated by sampling 5% of the total current flowing through the power FET by a source degeneration resistance in one of the FET fingers. The CS_{REF} is generated by mirroring the reference bias current and pushing it through an on-chip polysilicon resistor. When the sensed current crosses the predefined threshold, i.e., the CS goes above CS_{REF}, the output of the high gain comparator changes state (Positive edge of I_{LIM} signal is generated). The output is reset at each T_{OFF} period of OSC, ensuring that at the beginning of next cycle the I_{LIM} signal remains at low state.
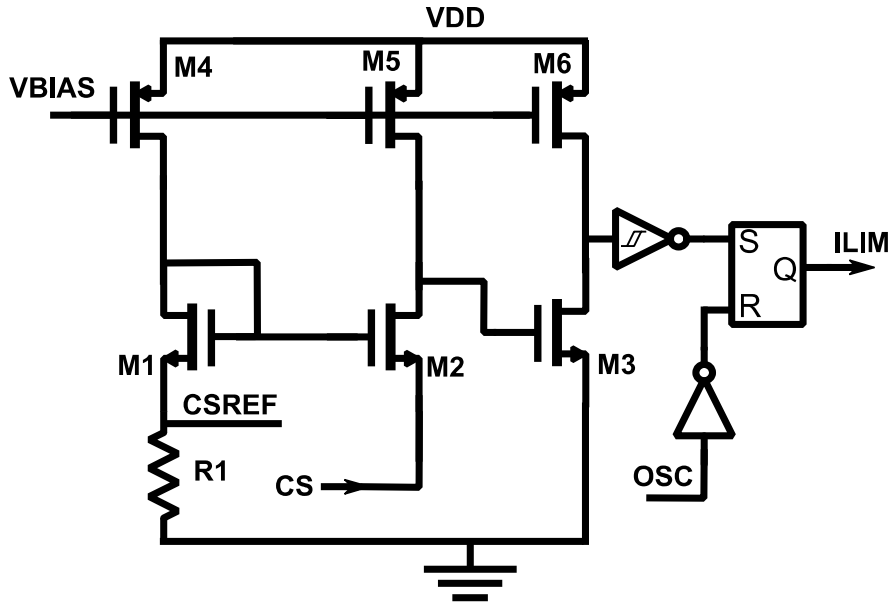
Fig. 2.6: schematic diagram of the current limit comparator for the current limit during boost mode. A similar circuit with complimentary devices can be designed for buck mode operation. In that case, the CSREF will be generated out of the source terminal of a pFET instead of nFET as shown here. Consequently , other elements will be complimentary too.

CHAPTER 3

MESUREMENT RESULTS

This chapter discusses the silicon measurement results of the proposed buck-boost regulator. Different characterization parameters of the chip are measured along with several oscilloscope snapshots to quantify the performance of the chip and to elaborate different operation.

The chip is fabricated in 130nm CMOS process. The die size is 550µm x 350µm. Fig. 3.1 shows the die photo of the chip. Different circuit blocks are also marked.
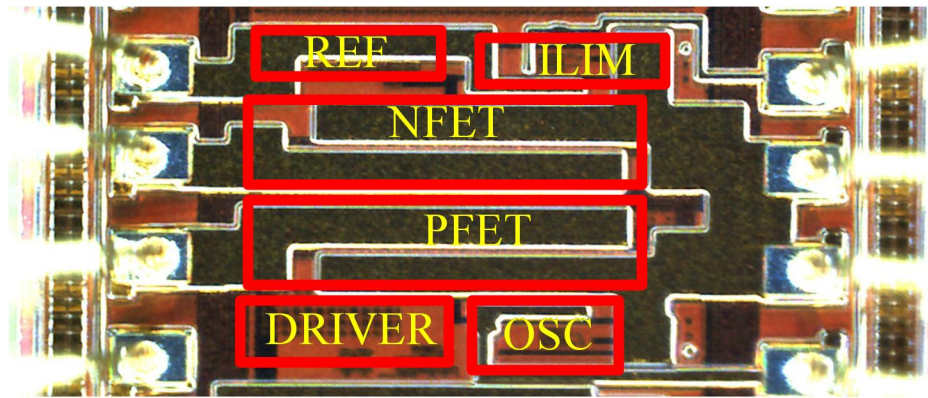
Fig. 3.1: Die photo of the implemented IC

The chip is packaged in Leadless Chip Carrier (LCC) package with 52 pins. The silicon is wire-bonded with the package with bondwires of 25µm diameter. The packaged part is then placed on mounting socket and eventually connected to external components on a printed circuit board (PCB). Fig. 3.2 shows the photo of the PCB with the socket cover opened to expose the die in the middle. External components are seen on the board. A

component table for typical measurement setup including different parasitic elements is given in Table 3-I.

Fig. 3.2: board setup.

Table 3-I: External components and parasitic elements

Item	Value
Inductor	100μH 450mΩ
Capacitor (input and output)	100μF
Schottky Diode	350mV at 200mA
Traces	10mΩ
Bondwire	20mΩ

Start-up Operation

The regulator can select mode of operation depending on the input level. However, it is also possible to the force the mode of operation externally. Connecting the FB_1 to V_{SS}
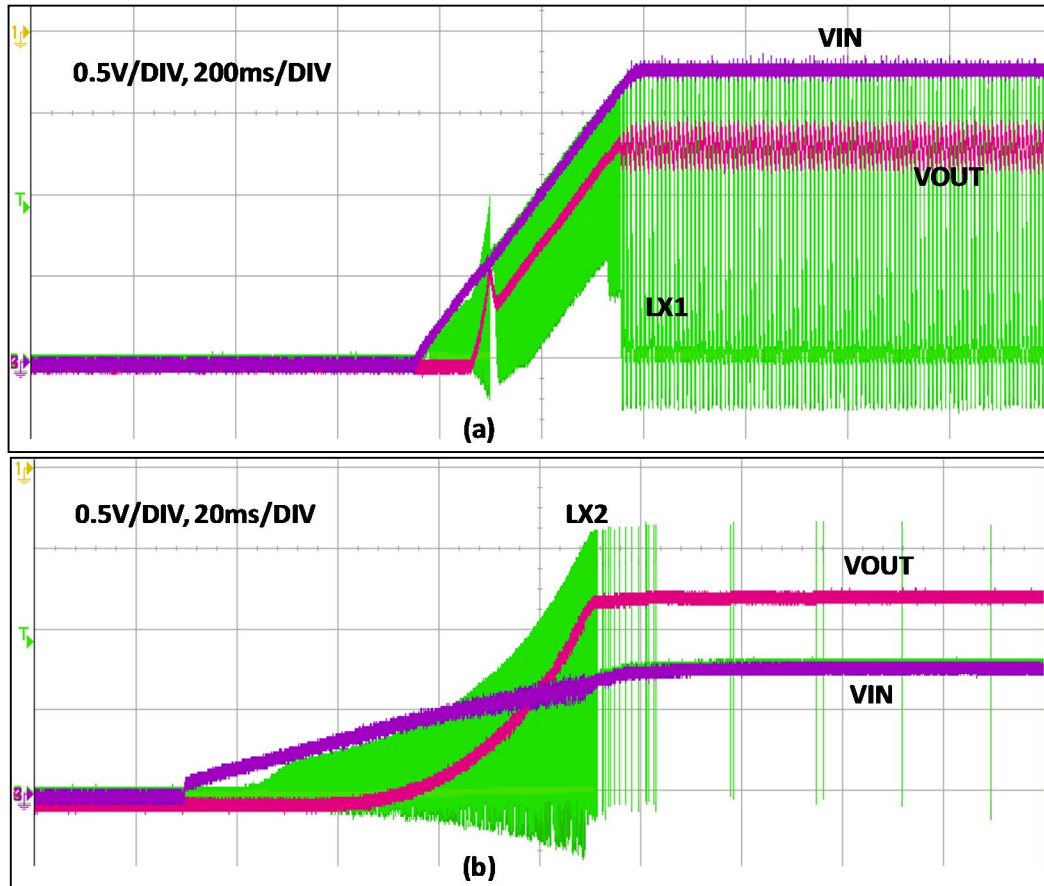
Fig. 3.3: Start up operation (a) buck and (b) boost mode.

forces the boost operation while connecting the FB_1 to V_{OUT} forces the buck operation. Fig. 3.3 shows the startup operation for the regulator in two different mode. Boost mode start up, shown in Fig. 3.3(a) begins when the input voltage rises above 400mV. Because of the PMOS MP_1, the effective input across the inductor is higher than zero only after the actual input is larger than the threshold voltage of the PMOS. Therefore, when input crosses V_{TH} of MP_1, inductor current starts to buildup in successive oscillator pulse. Accordingly, the output is charged at every pulse and continues to rise until it reaches the

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regulation threshold, which is externally set (in this case 1.2V). During the startup phase, the oscillator continues to generate pulse and is seen as a band in the LX_1 node. Once the regulation level is reached, the oscillator pulse becomes intermittent, which is decided the regulation loop's comparator (PFM decision-making comparator). Fig. 3.3(b) shows the
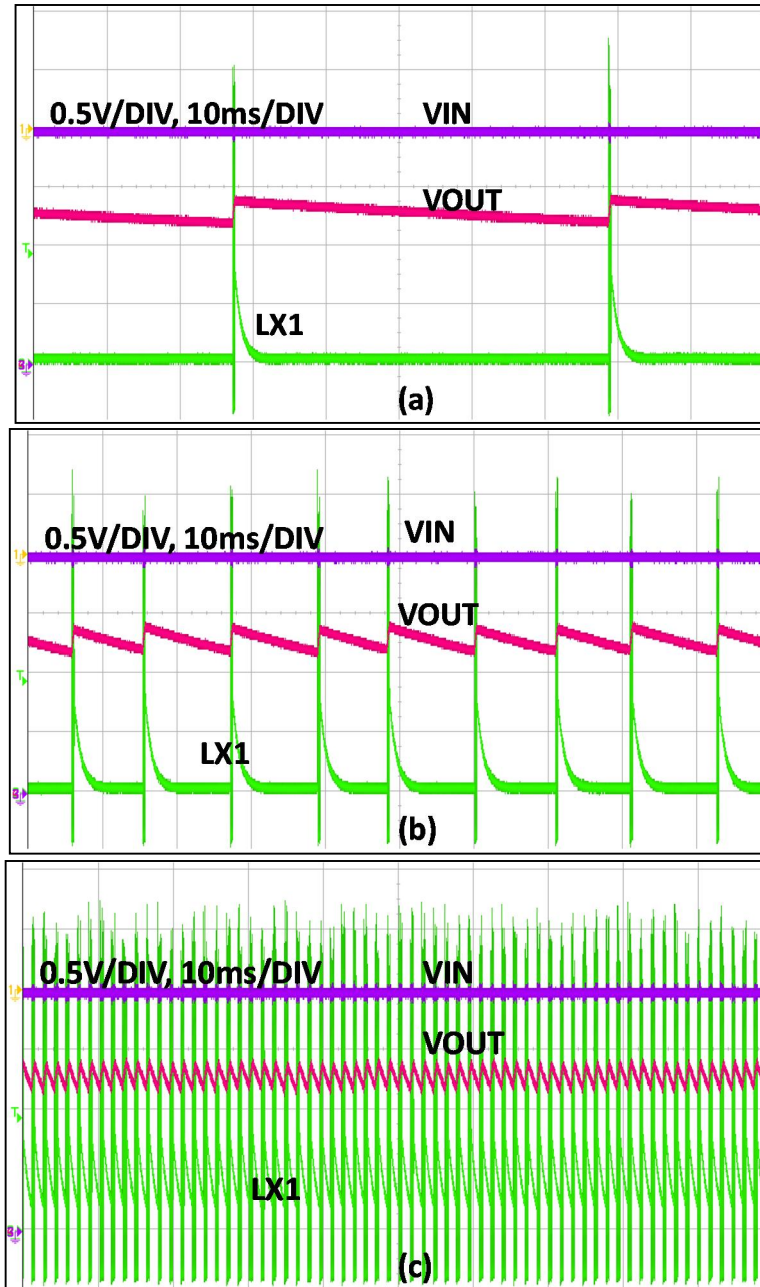
Fig. 3.4 : Pulse frequency modulation scheme shown in buck mode. With increasing load the ratio of active time to idle time increases. Regulator with (a) 0.1mA load, (b) 1mA, and (c) 10mA load current.

startup operation of the regulator in buck mode. Because the source itself if slew limited the output follows the input with nominal schottky diode drop until it reaches the regulation threshold. Once regulation level is reached, the oscillation pulse become intermittent based on the feedback compactor's (PFM decision-making circuit) decision.

PFM Operation at Varying Load

Fig. 3.4 shows the PFM behavior as a function of the load. At lower load as shown in Fig. 3.4(a), the regulator goes through spurious switching events. It remains in idle mode for long, after every switching event. As the load is increased, the pulse occur more frequently, which is shown in Fig. 3.4(b). This increases the active mode time to idle mode time ratio of the regulator. As the load is increased further, two successive switching events come even closer, as shown in Fig. 3.4(c). As the idle time between two adjacent switching events vanishes, the regulator fails to regulate the output voltage.

Line Regulation – Output at Varying Input

Fig. 3.5 shows the output regulation characteristic of the regulator with varying input range. The input voltage is initially 0.5V and the output is set at 1.2V, hence the regulator is in the boost mode. As the input increases, the switching events become sparser, since the conversion ratio decreases. At the same time, since at every pulse inductor current can build up to higher level (because of higher input voltage), the output ripple increase. Due to the inherent design topology, the output is regulated as the valley control mechanism and the ripple only grows upward keeping the valley of the regulation level constant. This

feature ensures minimum voltage requirement for the load. As the input voltage goes approximately 300mV above the regulated output level, the regulator switches mode to buck operation. Early in the buck operation, when input voltage is closer to output voltage, the inductor current is small at every pulse; hence, the ripple of the output is lower as well. As the input increases the ripple increase too, however the valley of the output is kept constant, similar as in boost operation. The mode transition threshold is externally set at 300mV higher than the output voltage to compensate the schottky diode drop during buck mode.
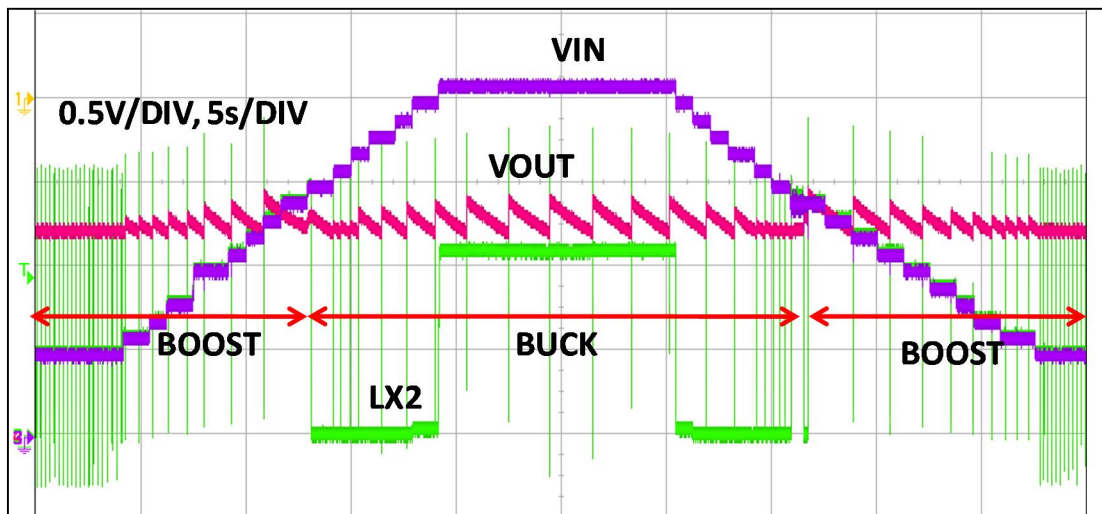
Fig. 3.5: Regulation of output voltage with dynamic input voltage. Buck and boost modes are marked.

Load Regulation – Output at Varying Load

Fig. 3.6 shows the load regulation characteristics of the regulator, both in buck and boost mode. In both cases, a load current step of 0.1mA to 10mA is given. At a lower load the regulator exhibits spurious switching. When the load current is increased, the switching frequency increases to keep the regulated output regulated. Because the inputs have not

changed in either of these cases, the ripple magnitude in both high and low load conditions

are approximately same.
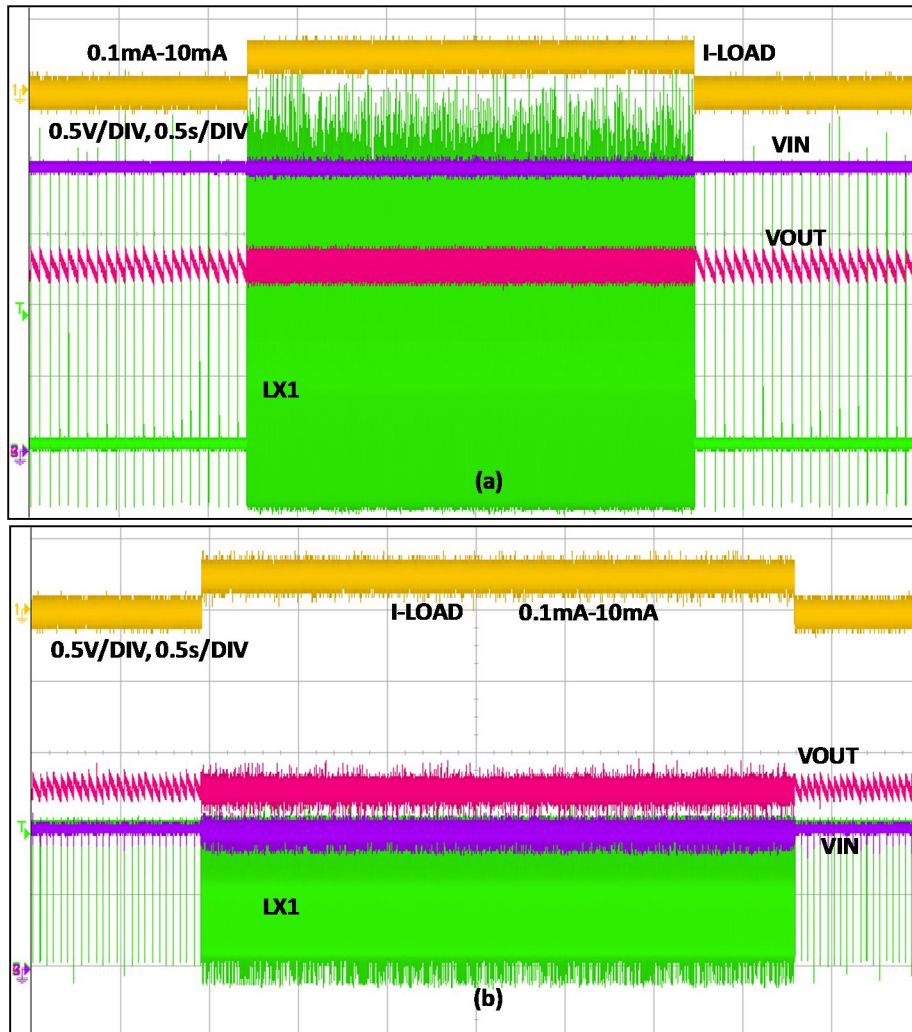
Fig. 3.6: Load transient behavior (a) buck and (b) boost mode.

Efficiency Measurement

Fig. 3.7 shows the measured efficiency of the regulator with varying input voltage in both

buck and boost mode of operation. The peak efficiency measured in the buck mode is 86%

when converting from 1.8V to 1.5V with 2mA of output current. Boost mode efficiency

peaks at 62% when supplying 10mA at 1.5V output voltage from 1.3V input. In boost

mode, the efficiency increases with increasing input voltage. This is because at higher input

voltage, at every pulse, more charges are transferred from input to output and the regulator
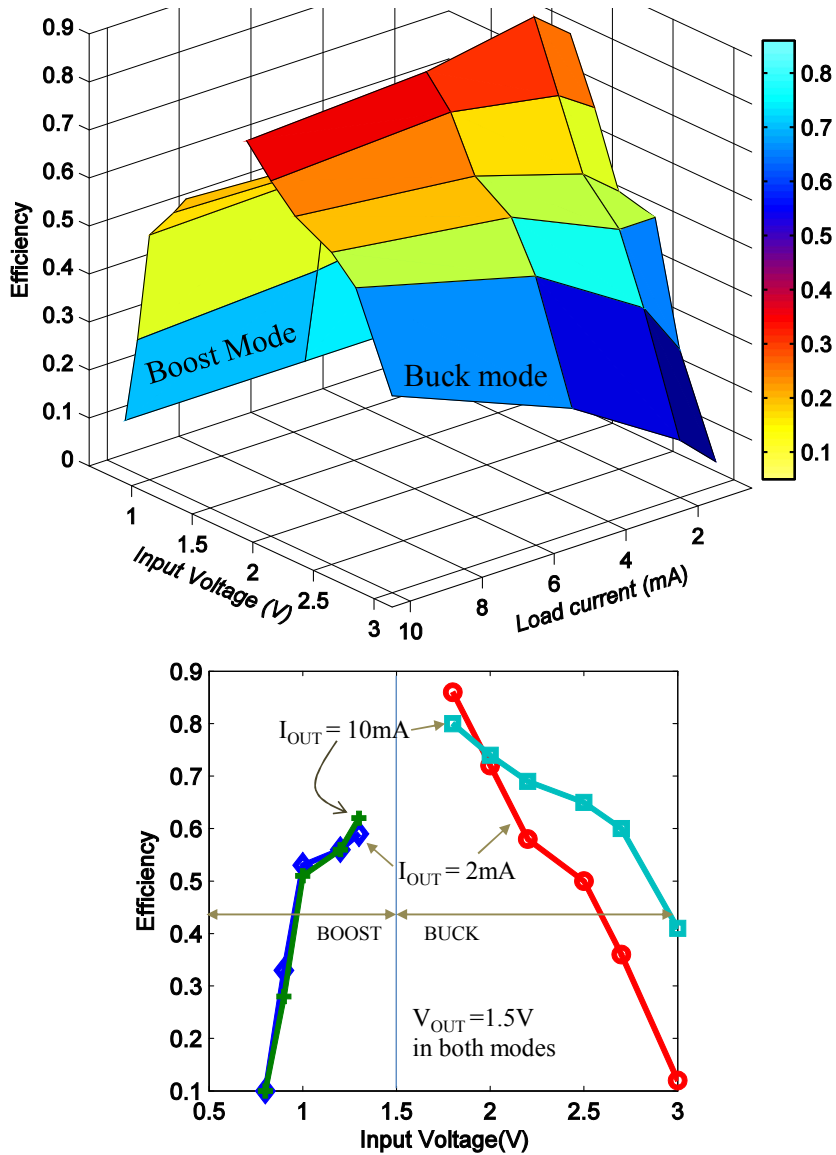
Fig. 3.7: Measured efficiency of the buck-boost regulator with varying input and load current. Output voltage is 1.5V in both modes. The bottom figure provides the projection of the efficiency plot for two different load current values.

has less switching and more idle time (same phenomena as observed with lower load, as

shown in Fig. 3.4). On the other hand, in the buck mode, increasing input voltage decreases

efficiency. Although the increasing input voltage produces higher inductor current, because

of the high conductive loss across the diode, the efficiency decreases with increasing input. The higher diode loss in the buck mode is attributed to the fact that, in the boost mode, the diode conducts current only during the falling phase of the inductor current (negative slope) but in buck mode it conducts during both rising and falling phases of the inductor current. During the boost mode, MP_1 remains on for in the series path of the inductor. Also, unlike the buck mode, the input is lower than the output hence, the gate drives are biased by the higher of these two voltages (i.e., the output voltage, 1.5V). With reduced biasing, the gate overdrive for power transistors have decreased, resulting a higher channel resistance. In addition, since the value of the input voltage defines the source-gate voltage of MP_1, boost mode gate over-drive is much smaller than that of buck mode. This increases the channel resistance substantially as well as prohibits the regulator operation beyond certain input voltage. This increased channel resistance causes the efficiency of the boost mode to be lower than that of buck mode with same current level. Chapter 4 discusses some design modification as future works to increase the efficiency of the proposed regulator.

Stability and Output Voltage Ripple

Because the regulator is designed with valley controlled hysteretic controller mode, the stability is guaranteed to the maximum load current capability. Beyond that, the regulator fails to provide enough current because of the inductor current limit protection scheme. However, the current capability of the design is easy to change from the design by changing the CSREF. Within the load current limit, the regulator recovers from transient droop with a single pole defined by the output capacitor and load impedance.

The output voltage ripple in this design is defined by the input voltage, inductor and output capacitor. For light load conditions, with single pulse operation, the ripple in boost and buck modes are defined by (3.1) and (3.2).

$$V_{RIPPLE\_BOOST} = \frac{V_{IN} T_{ON}^2}{2 L_{IN} C_{OUT}} \frac{1}{(k-1)} + \frac{V_{IN} T_{ON}}{L_{IN}} R_{ESR} \qquad (3.1)$$

$$V_{RIPPLE\_BUCK} = \frac{V_{IN} T_{ON}^2}{2 L_{IN} C_{OUT}} (1 - k) + \frac{V_{IN} T_{ON}}{L_{IN}} R_{ESR} \qquad (3.2)$$

Where R_{ESR} is the output capacitor ESR, and k is the conversion ratio (V_{OUT}/V_{IN}), in both cases and hence $k > 1$ for boost and $k < 1$ for buck mode. In both buck and boost cases, the output voltage ripple is directly proportional to the input voltage given that the T_{ON} is fixed; which is the case for this implementation. This is visible in the experimental results as shown in Fig. 3.5. Measured ripple in buck mode is found to be 260mV at 3V input and 50mV with 1.6V inputs (output 1.2V). The measured ripples in the boost mode are 220mV at 1V and 50mV with 0.4V (output at 1.2V). In boost mode, as the input increases the ripple magnitude increases. Intuitively, this is expected since given T_{ON} is fixed, with increasing input voltage, the inductor current increases as well. This translates to more charges being transferred to the output capacitor at every switching cycle and hence the ripple increases. Similarly in buck mode, the ripple increases with increasing input voltage. The regulated output is maintained by the valley-controlled mechanism; hence, the valley of the output voltage remains same and should be regarded as the regulated voltage level for this implementation. The ripple magnitude can be lowered either by increasing inductor or capacitor size or by increasing the frequency of the operation (hence decreasing T_{ON}). The design choice is guided by the sensitivity of the application to the voltage ripple and the

trade-off between quality of the regulated output and the self-power consumption due to increased frequency or increased component footprint.

Table 3-II: Regulator parameters

Item	Buck	Boost
IDD (no-switching) ((at VDD=3.3V))	87nA	88nA
IDD (continuous switching) (at VDD=3.3V)	43uA	28uA
VREF	0.66V	
FB Hysteresis	30mV	
Regulated Output	0.66V-3.2V	
Peak efficiency	86%	62%

A. Performance Summary

Table 3-II summaries the regulator parameters. The buck and boost controller being same consumes similar bias current of 88nA. The drivers of power transistors are different, hence during continuous switching mode, the buck consumes more current than the boost because the PMOS device capacitance is nearly twice than that of the NMOS device. The internally generated reference based on which the feedback and the mode select comparator decide,

Table 3-III: Comparison chart with state of the art reported works

Item	ISSCC '13 [14]	ISSCC '09 [15]	VLSI '11 [16]	TCAS '12 [17]	This Work
Min./Max V_{IN}	N/A	0.6V/4.2V	1V	0.9V/4.5V	0.4V/3.3V
V_{OUT}	1V-3V	1V/3V	1.8V-.5V	2.5V	0.66V- 3.2V
Bias/Power	400nW	N/A	6μA	N/A	88nA
Peak efficiency	83%	N/A	88%	54%	Buck: 86% Boost: 62%
P_{OUT_MAX}	10mW	1mW	42mW	0.25mW	60mW
Frequency	20KHz	2MHz	100KHz	1MHz	60KHz
Process	0.18μm	0.5μm	0.35μm	0.18μm	0.13μm
Area	4.5mm^2	0.2mm^2	4.6mm^2	0.05mm^2	0.2mm^2

is measured to be 0.66V. Excluding the bonding pads, the design occupies an active silicon area of $0.2mm^2$ in 130nm process.

Table 3-III compares this work with other recent publications. It achieves lower operating input voltage, lower bias current consumption than other relevant works. While it does not achieve highest reported efficiency, few design modifications will considerably increase the efficiency.

CHAPTER 4

FUTURE WORKS AND CONCLUSION

This chapter discusses some design issues of this works, proposes some improvements and provides conclusion.

Although this regulator achieves low operating bias current, the operating efficiency is low, specially, in the boost model. This is arising from the significant on-resistances of MP_1 in boost mode and D_2 in Buck mode. With suitable upsizing of MP_1, the boost mode efficiency can be improved. Additionally, replacing the diodes D_1 and D_2 by synchronous devices (PMOS and NMOS, respectively) will help increase the efficiency further.

The minimum input voltage achieved by this design is primarily limited by the design of the PMOS device MP_1. As shown in Fig. 2.1(c), the MP_1 is kept on (gate connected to ground) for the boost mode operation. As V_{IN} decreases, the gate-source voltage of MP_1 decreases too. When the V_{IN} falls below the threshold voltage of MP_1, it turns off and the regulator fails to operate. A transmission gate power device (parallel NMOS and PMOS) will help alleviate the issue. In that case, the parallel NMOS resistance will offer alternate current path, allowing further lowering of input and improving efficiency, especially at low input voltage conditions.

This PFM mode buck-boost regulator is designed with fixed T_{ON} topology, hence the peak inductor current varies linearly with input. So, it incurs variable conduction losses. To appease this issue, a constant peak current topology may be realized by designing an input-

depended on-time generator which decreases the T_{ON} values with increasing V_{IN}, thus, keeping the inductor peak current constant.

In conclusion, this work presents a low current buck-boost regulator for remote energy harvesting applications. Best usage are for applications such as remote surveillance, motion detection, low frame rate image sensing, intermittent ambient environmental sensing and wireless data transmission; those have intermittent power usage and long sleep time. The significant low bias consumption of this design helps minimize energy wastage during the time of prolonged low or no-activity periods. Additionally, to capture energy from dynamically varying energy sources, the proposed design offers wide input operating range making it suitable for the use with sources such as photovoltaic or thermoelectric generators whose output voltages might vary widely depending on ambient environmental conditions.

APPENDIX - A

PHYSICAL LAYOUT DESIGN AND ISSUES

This appendix discusses the layout design steps for general analog power management ICs, and some design considerations to improve the quality of layout in circuit design such as the buck-boost regulator presented in this thesis. It is assumed that all layout placement are performed manually.

Basic Layout Terminologies

DRC: Design Rules Check – An automated check that monitors different physical design rules e.g., distance between same layer metal lines, minimum width of layers, distance between different layers. The chip level DRC additionally checks different layer densities throughout different sections of the chip.

LVS: Layout Versus Schematic check – An automated check that monitors whether the physical design matches the schematics. All connections in the physical design must be present although they might exist only as abstract connections in the schematic.

PEX: Parasitic Extracted (netlist): A compiler generated netlist from the physical design and can be simulated instead of the schematic. The PEX netlist consists of all the devices from the layout (they must also exist in the schematic) and parasitic components e.g., capacitance due to physical connections, resistance due metal routing etc.

GDS: Global Data Stream, is a binary file generated from the final layout, using the foundry provided syntax. It includes the information of the all polygons drawn in all layers in the layout with their size and positions. This is only file sent to the foundry, from which

the foundry is able to decode the actual layout. The syntax and ways of generating GDS files are provided by the foundry.

Layout Steps

After the design has been passed through successful schematic level simulation phase, the layout of different blocks are started. The layout is intended for physically placing different circuit elements along with all physical and logical interconnects noted in the schematic. The die size and I/O pads are also carefully considered before layout is started. Fig. A-1 shows the flow chart of the layout design.

```
┌──────────────┐      ┌──────────────┐      ┌──────────────┐
│Area Estimation│      │ Device Layout │      │  Block Level  │
│ and Floor-   │─────▶│   DRC, PEX   │─────▶│    Layout     │
│  planning    │      │              │      │ DRC, LVS, PEX │
└──────────────┘      └──────────────┘      └──────────────┘

┌──────────────┐      ┌──────────────┐      ┌──────────────┐
│  Mid-Level   │      │  Top-Level   │      │ Chip-Level    │
│  Hierarchy   │─────▶│  Hierarchy   │─────▶│Hierarchy, incl.│
│  DRC, LVS    │      │ DRC, LVS, PEX│      │   I/O pads    │
│              │      │              │      │ DRC, LVS, PEX │
└──────────────┘      └──────────────┘      └──────────────┘

┌──────────────┐      ┌──────────────┐      ┌──────────────┐
│Add Chip Edge │      │Chip-level DRC│      │               │
│ and other    │      │ (density), off-│    │ Generate GDS, │
│Foundry specific│───▶│grid check, LVS,│──▶│send to Foundry│
│  layers      │      │    PEX       │      │               │
└──────────────┘      └──────────────┘      └──────────────┘
```

Fig. A-1: Layout design flow chart
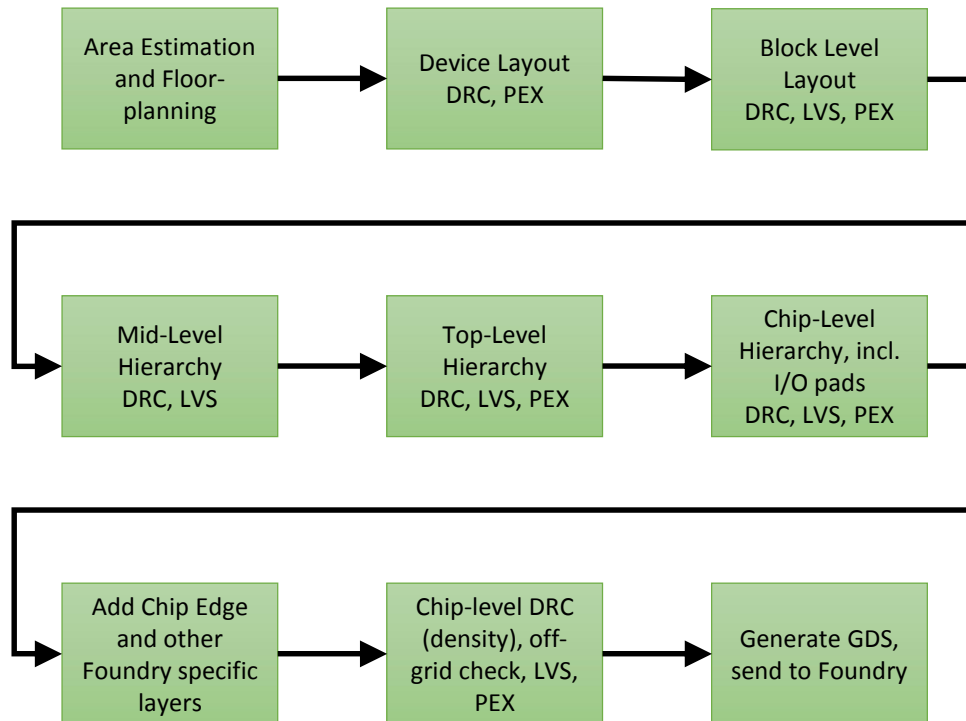
Referring to Fig. A-1, the steps are elaborated below,

1. Floorplan: A floorplan is the abstraction of the actual placement of the individual circuit blocks. This is done to optimize the interconnect lengths between different blocks and with I/O pads. Floorplans must specify the I/O pad positions relative to the blocks. The areas of different circuit block might be approximated but the

aberration must be minimized through reasonable sizing analysis from the transistor existing transistor counts and from anticipated changes in the design.

2. Block level design: Each block must be individually laid-out from ground-up. Instead of flattening, hierarchical approach should be taken, where any block can be reused by some other block as a unique instances and if required, multiple times.

3. Mid-Level Hierarchy design: once the individual blocks are finished, blocks must be grouped based on operation and from mid-level hierarchy. A mid-level hierarchy might consists of level unique blocks, generating a single output for most of the cases. This also helps to manage the top level with greater ease.

4. Top level hierarchy: mid-level hierarchical blocks are then combined to generate the top level hierarchy. Top level hierarchy uses all circuit blocks.

5. Chip level hierarchy: once the top level hierarchy is completed, it is combined with the I/O pad and ESD protection circuits to form chip level. Chip level hierarchy also has other foundry relevant non-design blocks such as chip edge, text label, and fab ID etc. chip level layout is finally converted into the GDS file and sent to the foundry.

Layout Level	DRC (cell level)	DRC (chip level)	LVS	PEX	GDS
Device layout	Yes	X	Yes	Yes	X
Block level	Yes	X	Yes	X	X
Mid-level hierarchy	Yes	X	Yes	X	X
Top-level hierarchy	Yes	X	Yes	Yes	X
Chip-level hierarchy	Yes	Yes	Yes	Yes	Yes

Schematic based simulation provide approximate results, and fails to capture parasitic elements. Hence after the actual layout is done, a parasitic extracted simulation must be performed. The delays of different critical circuit paths, mismatches between routing, and mismatches between mirror devices are sources of systematic timing and voltage offsets in circuits. For example, in a comparator whose devices are not matched in the layout and the routing from the sense point to the input transistors are not identical, will exhibit a systematic offset in parasitic extracted simulation but will not be captured in schematic simulation. Hence to avoid unwanted circuit failure, a post layout (parasitic extracted) simulation is critical. Once the circuit passes all the specifications from post layout simulation, it can be finalized for the GDS extraction and be sent to the fab.

REFERENCES

[1]   Xiao Yu; Yanxiang Liu; Tie Li; Hong Zhou; Xiuli Gao; Fei Feng; Yuelin Wang, "Thin-film-based thermoelectric energy generator device with a card structure," Sensors, 2012 IEEE , vol., no., pp.1,4, 28-31 Oct. 2012.

[2]   Kim, M.K.; Kim, M.S.; Jo, S.E.; Kim, H.L.; Lee, S.M.; Kim, Y.J., "Wearable thermoelectric generator for human clothing applications," Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII), 2013 Transducers & Eurosensors XXVII: The 17th International Conference on , vol., no., pp.1376,1379, 16-20 June 2013

[3]   Apertet, Y. and Ouerdane, H. and Goupil, C. and Lecoeur, Ph., "Influence of thermal environment on optimal working conditions of thermoelectric generators," Journal of Applied Physics, 116, 144901, 2014.

[4]   O. Yamashita , S. Tomiyoshi , and K. Makita , " Bismuth telluride compounds with high thermoelectric figures of merit," J. Appl. Phys. **93**, 368 (2003).

[5]   R. McCarty , " Thermoelectric power generator design for maximum power: It's all about ZT," J. Electron. Mater. **42**, 1504 (2013)

[6]   http://www.cui.com/product/resource/cp85.pdf

[7]   www.enocean.com/en/enocean_modules/STM_31x_Data_Sheet_Apr13_10.pdf/

[8]   http://www.digikey.com/product-detail/en/430857-500/926-1178-ND/2269538

[9]   http://lairdtech.thomasnet.com/item/thermoelectric-modules-2/optotec-series-thermoelectric-coolers/pn-4146

[10]   http://www.lairdtech.com/brandworld/library/THR-DS-eTEC-HV14%200512.pdf

[11]   Joseph P. Heremans, Mildred S. Dresselhaus, Lon E. Bell & Donald T. Morelli "When thermoelectrics reached the nanoscale" Nature Nanotechnology 8, 471–473 (2013)

[12]   Olga Bubnova, Zia Ullah Khan, Abdellah Malti, Slawomir Braun, Mats Fahlman, Magnus Berggren & Xavier Crispin "Optimization of the thermoelectric figure of merit in the conducting polymer poly(3,4-ethylenedioxythiophene)" Nature Materials 10, 429-433, 2011

[13]   Daniel Kraemer, Bed Poudel, Hsien-Ping Feng, J. Christopher Caylor, Bo Yu, Xiao Yan, Yi Ma, Xiaowei Wang, Dezhi Wang, Andrew Muto, Kenneth McEnaney, Matteo Chiesa, Zhifeng Ren & Gang Chen "High-performance flat-panel solar thermoelectric generators with high thermal concentration" Nature Materials 10, 532–538 (2011)

[14]   K. W. R. Chew, et. al., "A 400nW single-inductor dual-input-tri-output DC-DC buck-boost converter with maximum power point tracking for indoor photovoltaic energy harvesting," IEEE International Solid-State Circuits Conference (ISSCC), 2013, pp. 68-69.

[15]   K. Suhwan et. al., "Single-inductor dual-input dual-output buck-boost fuel-cell-li-ion charging DC-DC converter supply," IEEE International Solid-State Circuits Conference (ISSCC), 2009, pp. 444-445.

[16]   D. Mengmeng, et. al., "A reconfigurable SITITO boost/buck regulator with sub-threshold cross-regulation-free dual-mode control for energy-harvesting applications," Symposium on VLSI Circuits, 2011, pp. 240-241.

[17]   I. Vaisband, et. al., "A Closed-Loop Reconfigurable Switched-Capacitor DC-DC Converter for Sub-mW Energy Harvesting Applications," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.62, no.2, pp.385,394, Feb. 2015.

[18]   S. Kim, et. al., "Dual-source single-inductor 0.18μm CMOS charger-supply with nested hysteretic and adaptive on-time PWM control," IEEE International Solid-State Circuits Conference (ISSCC), 2014, pp.400-401, 9-13.

[19]   I. M. Darmayuda, et al., "A Self-Powered Power Conditioning IC for Piezoelectric Energy Harvesting From Short-Duration Vibrations," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 59, pp. 578-582, 2012.

[20]   E. Lefeuvre, et. al., "Buck-Boost Converter for Sensorless Power Optimization of Piezoelectric Energy Harvester," IEEE Transactions on Power Electronics, vol. 22, pp. 2018-2025, 2007.

[21]   J. J. Chen, et. al, "A High-Efficiency Positive Buck–Boost Converter With Mode-Select Circuit and Feed-Forward Techniques," IEEE Transactions on Power Electronics, vol.28, no.9, pp.4240-4247, 2013.

[22]   E. Lefeuvre, D. Audigier, C. Richard, and D. Guyomar, "Buck-Boost Converter for Sensorless Power Optimization of Piezoelectric Energy Harvester," *Power Electronics, IEEE Transactions on,* vol. 22, pp. 2018-2025, 2007.

[23]   http://www.linear.com/product/LTC3531

[24]   http://www.ti.com/lit/ds/symlink/tps63001.pdf

[25]   K. Z. Ahmed and S. Mukhopadhyay, "A wide conversion ratio, extended input 3.5µA Boost Regulator with 82% Efficiency for Low Voltage Energy Harvesting," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2013.

[26]   B. Razavi, Design of Analog CMOS Integrated Circuits, 2001.