

**DESIGN AND CHARACTERIZATION OF BICMOS
MIXED-SIGNAL CIRCUITS AND DEVICES FOR
EXTREME ENVIRONMENT APPLICATIONS**

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The Academic Faculty

By

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**DESIGN AND CHARACTERIZATION OF BICMOS
MIXED-SIGNAL CIRCUITS AND DEVICES FOR
EXTREME ENVIRONMENT APPLICATIONS**

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To my Lord and Savior, Jesus the Christ

Whose unconditional love,

and blessings has enabled me to complete this work. “Proverbs 3:5-6”

To my mother, Firmina, an epitome of selfless love. Eu te amo minha mãe.

To my “sweet” son, Samuel, a God answered prayer and,

To my wife, my “beauty”, Dilvia.

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SUMMARY

State-of-the-art SiGe BiCMOS technologies leverage the maturity of deep-submicron silicon CMOS processing with bandgap-engineered SiGe HBTs in a single platform that is suitable for a wide variety of high-performance, highly-integrated applications (e.g., system-on-chip (SOC), system-in-package (SiP)) [1]. In a space environment, the electronics experience constant bombardment by a wide spectrum of energetic photons and particles. Typical examples are communication satellites in geosynchronous orbit. For electronic systems to reliably operate in such radiation-rich environments, each of their individual components and sub-blocks must be thoroughly characterized for robustness. Silicon-Germanium (SiGe) heterojunction bipolar transistors (HBTs) have already demonstrated strong potential for many extreme environment applications (e.g., remote sensing systems, communications satellites, space exploration systems, and energy exploration) [2, 3].

Due to their bandgap-engineered base, SiGe HBTs are also naturally suited for cryogenic electronics [2] and have the potential to replace the costly de facto technologies of choice (e.g., Gallium-Arsenide (GaAs) and Indium-Phosphide (InP) in many cryogenic applications such as radio astronomy. The cryogenic electronics market continues to grow, and the range of applications has increased. Some of these applications range from space-based electronics (e.g., satellite systems, high-precision instrumentation and detector electronics for deep-space and planetary space missions), commercial applications (e.g., pre-amplifiers for cell-phone base stations that are cooled to improve the signal-to-noise ratio [4]), to biological/medical applications (e.g., medical instrumentation and sensors), and interface circuitry for quantum computing.

This work investigates the response of mixed-signal circuits (both RF and analog circuits) when operating in extreme environments, in particular, at cryogenic temperatures and in radiation-rich environments. The goal of this work is to attempt to fill the existing gap in knowledge on the cryogenic and radiation response of specific RF and analog circuit blocks

(i.e., RF switches, voltage references, and voltage controlled oscillators, and high-speed latch comparators). This knowledge will enable system architects and circuit designers to better understand how individual circuit blocks can be impacted by both cryogenic temperatures and radiation exposure, and more importantly, how to leverage the circuit response to mitigate for any adverse effects observed. In addition, the characterization of Field Effect Transistors (FET) and SiGe HBTs were performed and the results are presented to provide insight into any negative effects observed in the circuits' response. Radiation mitigation strategies to counterbalance the damaging effects are also investigated. The contributions of this dissertation are summarized as follows:

- One of the lowest reported loss performance of wideband RF single-pole double-throw (SPDT) switches designed in 180-nm RF CMOS on SOI technology (IBM 7RF) is presented. The SPDT RF switch achieves an insertion loss of less than 0.5 dB at 20 GHz and less than 2.0 dB at 40 GHz. A one-bit 180° switched-line phase-shifter was designed and characterized to evaluate the capabilities of this switch performance [5].
- The cryogenic performance of low-loss, wideband SPDT RF switches designed in a 180-nm SOI-CMOS technology is presented. A comprehensive characterization of the SPDT switches at room-temperature (300 K) and at cryogenic temperatures reveal that all key performance metrics (i.e., insertion loss, isolation, large- and small-signal linearity) improve with cooling [5,6].
- The impact of total ionizing dose (TID) on the RF performance of wideband (1 GHz to 40 GHz) and high isolation (>35 dB at 40 GHz) single-pole single-throw (SPST) FET-based RF switches are investigated for the first time. The switches were designed and fabricated in a 130-nm SiGe BiCMOS technology. Post-irradiation results reveal that the RF performance is dependent on the accumulated total dose. [7,8].

- A detailed study on the effects of single event transients (SETs) on single-pole double-throw (SPDT) RF switch circuits designed in a commercially-available, 180 nm second-generation SiGe BiCMOS (IBM 7HP) technology is presented. Two-photon absorption (TPA) experiment results reveal that the SPDT switches are sensitive to SETs. Potential implications are discussed and mitigation strategies are proposed [9, 10].
- An investigation of the impact of single event transients (SETs) and total ionization dose (TID) on precision voltage reference circuits designed in a 4th-generation, 90 nm SiGe BiCMOS technology (IBM 9HP). Two new circuit-level radiation-hardening-by-design (RHBD) techniques are proposed. An RHBD technique using inverse-mode (IM) transistors is demonstrated for the first-time. Also, a novel PIN diode VRC is presented as a potential SET and TID tolerant, circuit-level RHBD alternative [11, 12].
- Large-signal (P_{1dB}) and small-signal (OIP3) RF linearity of silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) fabricated in a new 4th generation, 90-nm SiGe BiCMOS technology operating at cryogenic temperatures are studied. SiGe HBTs with two different layout configurations, CBE (collector-base-emitter) and CBEBC (collector-base-emitter-base-collector), were characterized over temperature. The results reveal that SiGe HBT RF linearity does not significantly change with cooling [13].

CHAPTER 1

INTRODUCTION

The cold war fueled the space exploration race, and in the process a new industry was born — the “extreme environment” electronics (EEE) industry [14]. Although the EEE industry is considered a niche market that focuses mainly on military and defense related applications, it has grown significantly in the commercial arena since its early beginnings in the 1960’s. This industry now represents a large segment of the trillion-dollar global electronics infrastructure and continues to grow as new applications are developed [2, 15]. Commercial applications where EEE are widely used range from the automotive industry, to telecommunications (e.g., satellites), aviation, energy exploration (e.g., oil drilling), power industry (e.g., nuclear power plants), and many more.

Extreme environments pose major challenges to electronics. For instance, the electronics in satellites that are in low earth orbit are exposed to damaging radiation and wide temperature fluctuations. The current mitigation approach for electronics that are sent into space involves the use of extensive shielding and temperature control (i.e., “warm-boxes” or “electronics vaults”). Although this is the verified and accepted solution, it comes with significant penalties. The most significant penalties are increased weight, volume, and power. In addition, the overall system will have a high risk of performance reduction since extensive wiring is required with this approach. The “holy grail” solution is to completely remove the “warm-boxes” and to implement a distributed, in-environment electronic systems where the wiring is significantly reduced or eliminated, and the electronics are placed in close proximity with sensors and other interface instrumentation. This proposed approach improves the overall performance of the system while significantly reducing the cost. However, the electronics must first demonstrate reliable operation in a simulated “extreme environment” before they can be qualified for space programs.

Both silicon-germanium (SiGe) BiCMOS and silicon-on-insulator (SOI) CMOS technologies are considered serious contenders for EEE. For several EEE applications the SiGe BiCMOS has become the preferred technology platform (e.g., space and planetary exploration, satellites, advanced military radar systems, GPS) that are considered critical to the well-being of society. The SiGe HBT has inherent hardness to ionizing radiation up to multi-Mrad dose levels and improved performance with cooling when compared to the traditional bulk CMOS processes [2, 15]. The objective of the proposed research is to design and characterize mixed-signal circuits using the SiGe BiCMOS and SOI CMOS technologies, and to investigate the responses when exposed to both radiation and cryogenic temperatures. This process required the characterization of devices to provide insight into any negative effects observed in the circuits' response. Mitigation strategies to counterbalance the damaging effects are also proposed and investigated.

1.1 Research Objectives

The objective of this dissertation is to investigate and to gain new understanding of the response of mixed-signal (RF and analog) circuits and devices when operating in “extreme environments”, particularly at cryogenic temperatures and in radiation-rich environments. Specifically, the dissertation encompasses:

1. Design and characterization of single-pole double-throw (SPST) and single-pole four-throw (SP4T) RF switches at cryogenic temperatures.
2. Design of a low-loss, wideband (dc to 40 GHz) single-pole double-throw (SPDT) RF switch implemented in a 180 nm SOI CMOS technology.
3. Full characterization of a SPDT switch RF performance at cryogenic temperatures.
4. Investigation of the radiation response (Total Ionization Dose and Single Event Transients) of FET-based RF switches.

5. Design of voltage reference circuits in 90 nm SiGe BiCMOS technology for the purpose of understanding their radiation robustness (Total Ionization Dose and Single Event Transients).
6. Investigation of the RF Linearity of SiGe HBTs in a 4th Generation, 90 nm SiGe BiCMOS technology at cryogenic temperatures.

1.2 Thesis Outline

The organizational structure of this Thesis is as follows:

- A background and literature review of extreme environment electronics, a brief overview of SiGe BiCMOS technology, radiation effects on electronics, and cryogenic temperature effects on electronics are presented in Chapter 2.
- In Chapter 3, the design and characterization of high-isolation single-pole single-throw (SPST) and single-pole four-throw (SP4T) RF switches is presented. The study also includes the investigation of RF cryogenic performance of these switch circuits. dc characterization of individual transistors is performed and analyzed to provide insight into the mechanisms underlying the observed changes in the RF switches.
- The design of a low-loss, wideband (dc to 40 GHz) single-pole double-throw (SPDT) RF switch implemented in a 180 nm SOI CMOS technology is examined in Chapter 4. The insertion loss of the 1.5 V switch is less than 0.5 dB from dc to 20 GHz and less than 2.0 dB at 40 GHz. A switched-line one-bit 180° phase shifter, designed using this low-loss switch, demonstrates an insertion-loss better than 3 dB at 18 GHz [5].
- The RF cryogenic performance of the low-loss, wideband (dc to 40 GHz) SPDT RF switch is investigated in Chapter 5. The purpose of this work is to examine the impact of cryogenic temperature on the RF performance of a low-loss, wideband

SPDT switch. Standalone devices with sizes comparable to those used for the switch designs were characterized to aid in the analysis of the circuit performance [5,6].

- In Chapter 6, the impact of proton irradiation on the performance of FET-based high-isolation SPST RF switches designed in a 130 nm SiGe BiCMOS technology is presented. Also, 10-keV X-ray radiation experiments were performed on individual transistors with sizes comparable to those used for the switch design. These measured results help to explain the underlying mechanisms that influence the switch RF performance under irradiation [7,8].
- The impact of single event transients (SETs) on single-pole double-throw (SPDT) RF switch circuits designed in a commercially-available, 180 nm second-generation SiGe BiCMOS (IBM 7HP) technology is investigated in Chapter 7. To verify one of the proposed mitigation techniques, SPDT switches were also designed in a 180 nm twin-well SOI CMOS (IBM 7RF-SOI) technology [11,12].
- In Chapter 8 an investigation on the impact of single event transients (SETs) and total ionization dose (TID) on precision voltage reference circuits designed in a 4th-generation, 90 nm SiGe BiCMOS technology is presented. A first-order uncompensated bandgap reference (BGR) circuit is used to benchmark the SET and TID responses of these voltage reference circuits (VRCs). Based on the first-order BGR radiation response, new circuit-level radiation-hardening-by-design (RHBD) techniques are proposed. An RHBD technique using inverse-mode (IM) transistors is demonstrated in a BGR circuit. In addition, a PIN diode VRC is presented as a potential SET and TID tolerant, circuit-level RHBD alternative [9,10].
- In Chapter 9, the large-signal (P_{1dB}) and small-signal (OIP3) RF linearity of Silicon-Germanium (SiGe) heterojunction bipolar transistors (HBTs) fabricated in a new 4th generation, 90 nm SiGe BiCMOS technology operating at cryogenic temperatures is studied. The linearity response of two different SiGe HBT layout variants, CBE

(collector-base-emitter) and CBEBC (collector-base-emitter-base-collector) is compared here. Both *dc* and *ac* figures-of-merit are presented to aid in understanding the linearity results at cryogenic temperatures, and also to provide an overall performance comparison between the two layout configurations, CBE and CBEBC [13].

CHAPTER 2

BACKGROUND AND LITERATURE REVIEW

2.1 Electronics in Extreme Environments

The term “extreme environment” refers to any environment that is outside the limits defined by commercial or military applications [1, 2, 15], i.e., environments that present wide temperature changes, chemical corrosion, intense vibrations, intense magnetic fields, high levels of radiation, or a combination of all these potentially destructive elements. In this work, “extreme environment” will only encompass the near-space environment (i.e., a low and geosynchronous Earth orbit). A classical example is the surface of the the Moon, where the ambient temperature fluctuates widely (e.g., +120°C to -180°C day to night). The surface of the moon also experiences heavy doses of radiation. Electronics in this environment experience constant bombardment by a spectrum of energetic particles (e.g., electrons, neutrons, protons, and heavy ions), in addition to having to sustain wide temperature variations.

The current mitigation approach for space electronics is to use commercial-off-the-shelf (COTS) parts that are typically designed for end-user products inside protective “warm-boxes” and heavy-weight shielding for radiation to emulate an Earth-like environment for the electronic circuits [16]. An example of a space system that employs this approach is shown in Figures 1 and 2, the NASA Mars Rovers. Several drawbacks, ranging from a large increase in the overall system weight and wiring complexity, to a significant reduction in the system performance and reliability, are presented by the “warm-boxes” approach. However, the major drawback of this approach is cost.

Due to the aforementioned problems of using “warm-boxes” and COTS products for

extreme environment applications, alternative approaches have been developed to provide custom-made electronics that are robust and are able to withstand extreme environment conditions [15]. To minimize or reduce radiation-induced failures the alternative approaches rely on either process modifications, and/or system design modifications. These mitigation approaches are classified as follows: (1) radiation hardening-by-process (RHBP), (2) radiation hardening by-reconfiguration (RHBR), and (3) radiation hardening-by-design (RHBD) [15, 16]. Depending on the application requirements, one or a combination of these techniques may be employed when developing extreme environment circuits. From these three approaches, the RHBP is the least desirable due to the increased fabrication costs. On the other hand, RHBD techniques typically require significantly more power and area to achieve acceptable levels of radiation tolerance (e.g., a classical RHBD approach is triple modular redundancy (TMR) [17]). The RHBR approach is particularly relevant for mixed-signal high-performance RF and microwave systems. The goal of RHBR is to develop circuits and systems that autonomously recover from radiation-induced loss of RF performance by employing on-die RF performance sensing, feedback control mechanisms, and tunable elements to compensate for damage [18–22]. This approach is not meant to repair the damage to the devices and circuits themselves, but rather to “heal” circuit performance from accrued damage by adjusting “tuning knobs” on the circuit blocks [22].

The “holy grail” in space electronics is the development of IC technology solutions that enables high-performance, system-on-chip (SoC) or system-in-package (SiP) solutions for space electronic systems that are radiation tolerant and invariant to temperature changes with minimal or no shielding [2]. Therefore, it is important to research and develop electronic systems that are capable of functioning reliably in a space environment without the need for extensively shielding the electronics. This solution would significantly decrease the overall space electronics cost (i.e., the cost to send the payload to space) as well as improve the overall system reliability and performance. As will be discussed in the following section, Silicon-Germanium (SiGe) technology is a viable technology option for

low-temperature and radiation-rich environment applications [15].

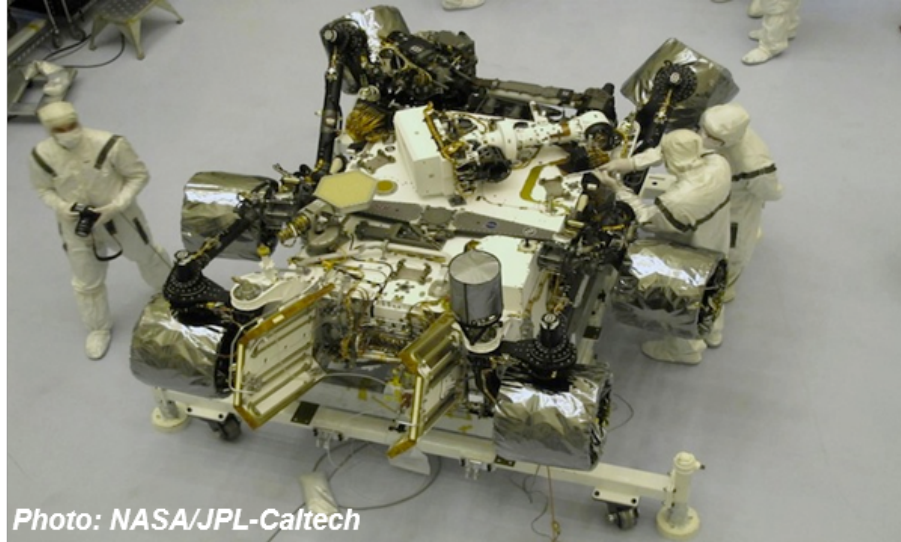


Figure 1. A photo of NASA's Mars Rover to highlight the shielding used to protect sensitive electronics.

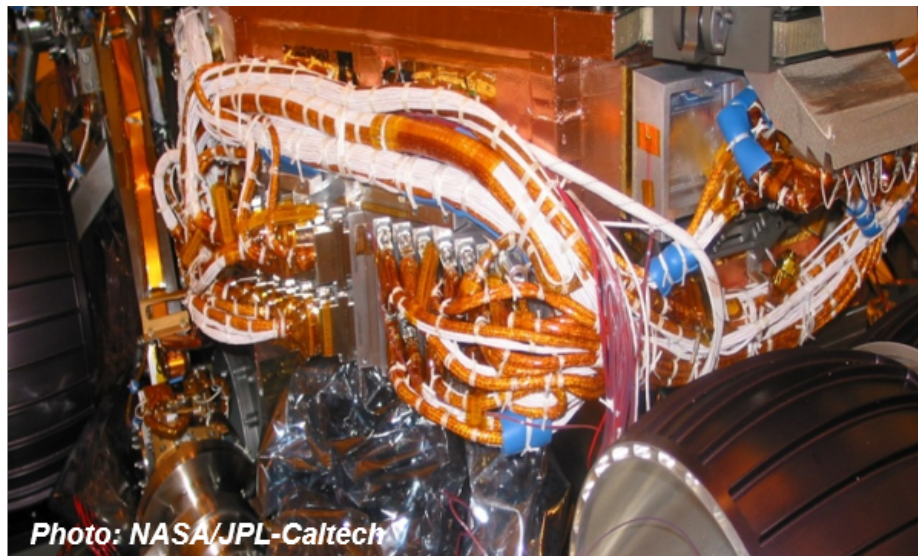


Figure 2. A closer view of NASA's Mars Rover to show the amount of shielding and wiring used.

2.2 SiGe BiCMOS Technology for Extreme Environments

As previously stated, electronics operating in space experience constant bombardment by a wide spectrum of energetic photons and particles. SiGe BiCMOS technology has proven to be a strong candidate for extreme environment applications (i.e., electronics that will have

to operate reliably over a wide temperature range or radiation-rich environment) [1, 2]. Examples of these applications range from communication and meteorological satellites in low orbit and geosynchronous orbit, to remote sensing systems, space exploration systems, energy exploration, and many more. SiGe BiCMOS technology plays a vital role in niche markets within the mixed-signal and RF domain. Silicon-Germanium (SiGe) BiCMOS technology leverages the potential of bandgap-engineered SiGe heterojunction bipolar transistors (HBTs) with conventional CMOS transistors in a platform that provides the high integration and functionality required for diverse SoC and SiP solutions that are highly attractive for EEE applications. For electronic systems to reliably operate in such harsh environments, each of their individual components and sub-blocks must go through rigorous characterization and reliability testing.

The effects of radiation on MOS and HBTs devices have been well documented, including several detailed studies on total ionizing dose (TID) response of metal-oxide-semiconductor field-effect transistors (MOSFETs) (both bulk and SOI) [14, 23, 24], and single event effects (SEE) of both HBTs [3, 25–29] and MOSFETs [29–35]. Many recent studies have also reported on the performance robustness of irradiated RF and mixed-signal circuits designed in SiGe BiCMOS technologies [36–42]. However, most of these studies were primarily focused on SiGe HBT-based circuits since the HBTs have been proven to be more TID tolerant than MOSFETs. RF circuit blocks have not been investigated as much as the digital and analog circuits. A large focus of this work is to investigate the radiation effects (TID and SEE) and the impact of cryogenic temperatures on the RF performance of n-channel field effect transistor (nFET) switches designed and fabricated in 130 nm and 180 nm SiGe BiCMOS technologies. For RF switch design, FETs would be typically used instead of SiGe HBTs because the use of FETs represents a good tradeoff between the RF specifications such as the switch insertion loss, isolation, and linearity, and the overall circuit *dc* power consumption. This fact is particularly important for EEE systems which are likely to have stringent power budget constraints (e.g., satellites).

2.3 Radiation Effects on Electronics

The birth of the radiation field of study can be traced to the early 1960s when the first Telstar satellite (Telstar 1) experienced a catastrophic failure because of the radiation damage caused by surface-related effects in semiconductor devices [14, 15]. Prior to this incident, radiation-effects studies primarily investigated the bulk properties of semiconductor materials and devices [14]. Based on these early investigation findings, engineers and research scientists were able to successfully repair the satellite while it was still in orbit [14]. Today, the relevance of this field has evolved beyond the early focus that was based on military threats and natural space radiation, to new areas that range from industrial applications (e.g., nuclear power plants) to medical applications (e.g., medical imaging electronics, Magnetic Resonance Imaging (MRI)).

The focus of the radiation effects discussed in this work is only on the space environment. These effects are grouped into three categories: total ionization dose (TID), displacement damage (DD), and single-event effects (SEEs). TID damage in electronics results from cumulative long-term ionizing damage caused primarily by high-energy proton and electron particles [14, 23]. TID is most detrimental to oxide regions of the device, and it can cause threshold voltage shifts, increase in leakage currents, and timing skews in circuits [15]. Some of these TID effects have the potential to cause permanent functional failure. DD is a cumulative long-term non-ionizing damage [15]. The DD effects are mainly derived from protons, but it can also be caused by electrons and secondary neutrons [43,44]. These high energy particles can cause actual dislocation of lattice atoms in semiconductor materials that results in permanent degradation of device properties (e.g., carrier mobility and carrier lifetime). This degradation in turn can affect the overall performance of the device and impact the system performance. SEEs are caused by direct ionization of a single energetic charged particle passing through a sensitive junction of a device [15, 30]. The charged particle (i.e., heavier ions and secondary products) are typically produced by incident protons. SEEs are typically classified into several sub-categories, including, but not

limited to, single-event upsets, single event burnout, single-event latchup, and single-event transients (SETs). However, this work will focus mainly on TID and SETs response of RF and analog circuits.

2.4 Cryogenic Temperature Effects on Electronics

“Cryoelectronics” is defined as the field of low-temperature electronics. Traditionally, this research area was solely viewed as the field for studying the physical properties of semiconductor materials and devices [45]. However, the field has evolved considerably since the first recorded experiment by Pearson and Bardeen in 1949, when the first electrical properties of pure silicon and silicon alloys were reported [45]. This growth is attributed to an increasing number of commercial applications that range from food storage, to telecommunications, medical instruments such as MRI, sensors and satellites, energy storage, space exploration and several others.

Several recent studies on the cryogenic performance of SiGe HBT-based integrated circuits (ICs) have been published (e.g., an X-band LNA [46], a K-band power amplifier (PA) [47], a bandgap voltage reference [48]). These circuit demonstrations and studies further support the potential of SiGe HBTs for high-performance and high-frequency cryogenic applications. The cryogenic electronics market continues to grow, and the range of applications has increased. Some of these applications range from space-based electronics (e.g., satellite systems, high-precision instrumentation and detector electronics for deep-space and planetary space missions), commercial applications (e.g., pre-amplifiers for cell-phone base stations that are cooled to improve the signal-to-noise ratio [4]), to biological/medical applications (e.g., medical instrumentations and sensors), and interface circuitry for quantum computing.

SiGe HBTs have demonstrated strong potential for many extreme environment applications including operation at cryogenic temperatures (e.g., remote sensing systems, communications satellites, spacecraft exploration systems, and energy exploration) [2]. Bandgap-engineered SiGe HBTs exhibit improvement in all device metrics and robust reliability when cooled down to cryogenic temperatures. This improvement stems from the bandgap-engineering of the SiGe HBTs. It is well known that cooling down to cryogenic temperatures provides a practical way to study the device physics, and to help determine the ultimate performance scaling limits of the devices [15]. SiGe HBTs with f_{MAX} near 0.8 THz [49] and with over half-terahertz f_T [50, 51] at deep-cryogenic temperatures have been reported recently. In addition, RF circuits have also been demonstrated operating at cryogenic temperatures, further confirming the benefits of operating circuits at cryogenic temperatures to meet the high-performance requirements of EEE. A significant part of this work focuses on the cryogenic temperature effects of RF switch circuits and high precision voltage reference circuits.

Prior works have shown that operating CMOS transistors at low temperatures improves the device and circuit performance [45,52]. The use of low temperatures encompass a broad range of benefits — such as substantial increase of the carrier mobility and saturation velocity, lower power consumption, reduced thermal noise, decreased leakage current, increased thermal conductivity, and improvement of the threshold voltage (V_{th}) [53, 54]. However, these potential improvements may be offset by the reliability limitations (e.g., kink phenomenon, impurity freeze-out, transient behaviors, device lifetime [54]). Understanding these benefits and limitations is outside the scope of this work. Additional information can be found in literature [45, 54]. The increased mobility and threshold voltage reduction are particularly important for RF switches, as it accounts for the overall circuit performance improvement (i.e., S-parameters and linearity) with decreased temperature.

2.5 On the Operation of FETs for RF Switch Circuits

This section provides a brief overview of the regions of operations of FETs, in particular nFET transistors for RF switch circuits. In this work p-channel FETs are not used because of their inherently lower carrier mobility (holes) and thus, higher on-resistance (R_{ON}) in comparison to nFETs. Understanding the mode of operations of the transistor helps to identify the inherent design choices and trade-offs, including the cryogenic results (presented in chapter 5).

For an RF switch circuit, the two relevant modes of operation for an nFET are the cut-off and linear regions. The cut-off region is also known as subthreshold or, weak-inversion. In this mode of operation the transistor is biased with $V_{GS} < V_{TH}$, where V_{GS} is the voltage between the gate and the source and V_{TH} is the threshold voltage of the device. For RF applications, the transistor in cut-off region is considered to be completely turned-off (e.g., no I_D current). However, there is a weak-inversion current that varies exponentially with the V_{GS} , and this current is significantly small, $<10^{-12}$ (pico-Amperes) [55], [56]. In the cut-off region, the resistance of the transistors R_{ds} (as shown in Figure 3) is considered very large at low frequencies [56]. This approximation is based on the fact that the inversion channel is not yet formed and very few charge carriers (i.e., electrons for nFETs) are able to travel from the source to the drain. Therefore, in this bias configuration a high resistance between the drain and source terminals of the device is presented.

Ideally, when the transistor is turned OFF no RF signals should propagate from one terminal to the other (from input to output), and this is true at low frequencies. However, as frequency increases the RF signals are likely to leak from one terminal to another because of the the finite resistivity of the silicon substrate in FETs, and the parasitic capacitances [57]. The potential signal paths for both bulk and TW transistors are illustrated in Figure 3(a) and (b), respectively. The potential RF leakage paths are highlighted in blue dashed lines for a bulk nFET as frequency increases. These paths can be formed by either individual or a combination of any of the parasitic capacitances — bulk-to-source

(C_{bs}), bulk-to-drain (C_{bd}), gate-to-drain (C_{gd}), and gate-to-source (C_{gs}), as depicted in Figure 3(a). However, the main factors in determining the device insertion loss (measured as S_{21} when the switch is on) are the bulk-to-source (C_{bs}) and bulk-to-drain (C_{bd}) junction capacitances, and the associated parasitic resistances because of the conductive nature of silicon substrate [58].

An alternative to the bulk nFET device is the nFET Triple-well (TW) transistor. A schematic view of the TW transistor is shown in Figure 3(b) along with the parasitic capacitances and resistance. The TW is becoming a prevalent option on most CMOS and BiCMOS technologies, and the added cost is not significant in comparison to the bulk-only technology processes. A cross-sectional view of the TW device is shown in Figure 4, and this type of device structure provides added substrate isolation and body bias control [57] through the N-Well terminal. This added isolation increases the effective substrate resistance, and reduces the parasitic losses of the transistors. Therefore, minimizing the amount of RF leakage through the substrate, and this increased substrate isolation in turn improves the insertion loss of the switch (as described in Chapter 3). The purpose of R_G and R_B shown in Figure 3 (b), is to minimize the fluctuations of V_{GS} and V_{GD} at the source and drain terminals. The use of these resistors also improves the dc bias isolation (i.e., prevents the RF signal from leaking to undesired terminals) and enhances the transistor reliability by limiting the voltage swing at those terminals [59], [57].

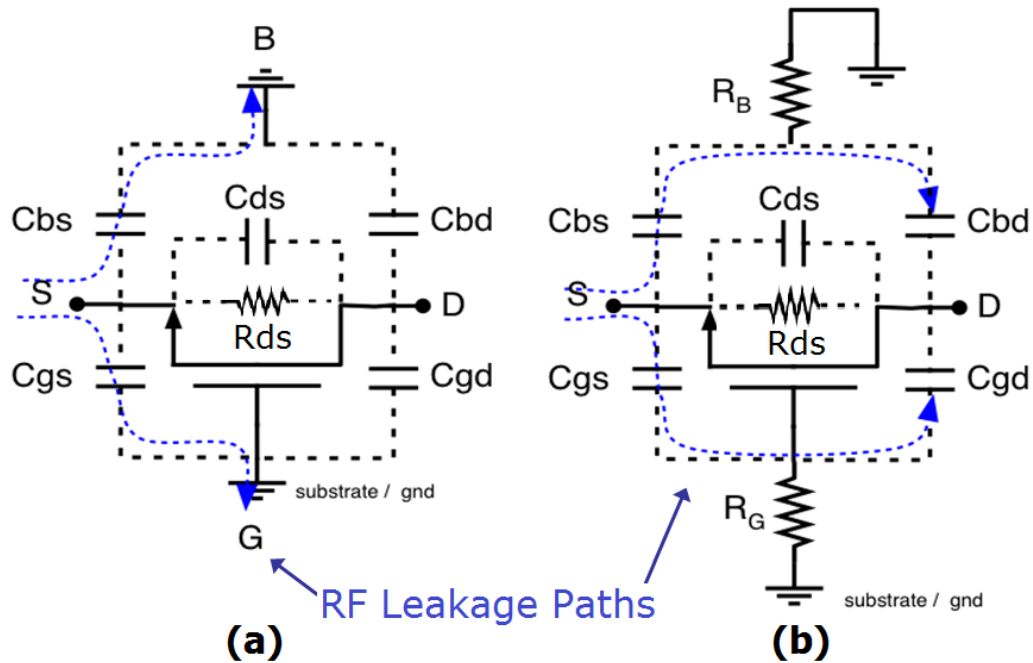


Figure 3. nFET transistor diagrams highlighting the parasitic devices and RF leakage paths for (a) bulk nFET and (b) triple-well isolated nFET with floating body resistors [57].

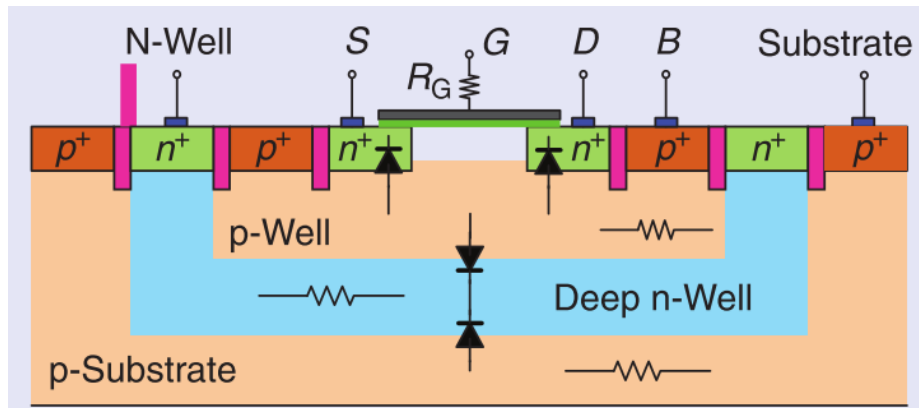


Figure 4. Cross-sectional view of a triple-well nMOS transistor [55].

The second mode of operation is the linear-region, also known as the triode or the ohmic region. The transistor bias condition is such that $V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$, where V_{DS} is the voltage between the drain and the source terminals. Figure 5 shows a cross-sectional view of a generic bulk nFET transistor under this bias condition. In this figure the induced inversion channel is shown below the oxide and the gate, and it is important

to understand how it influences the device operation because it ultimately controls the conductance of the charge carriers in the transistor channel. Assuming a volumetric sample, this conductance can be expressed as shown in Equation 1; it is evident that it is dependent on the carrier mobility, μ and the free carrier density, n [45]. The W , X_j , and L represent the width, depth, and length, of the device, respectively.

$$\sigma = \left(\frac{WX_j}{L} \right) q\mu n \quad (1)$$

As V_{GS} exceeds V_{TH} the charge-carrier density in the channel increases, and the magnitude of the current, I_D rises. This increased I_D translates to an improved conductance that is directly equivalent to a reduced device resistance [56]. Therefore, for a set transistor size (W/L) the lowest device resistance is attained by biasing the transistor with the maximum recommended V_{GS} , which increases the channel depth and the inversion layer conductance. This resistance is often referred to as the on-Resistance (R_{on}) or R_{ds} of the transistor (see Figure 3), and it is a dominant factor of the switch design because it is the main contributor of loss (insertion loss (IL), measured as S_{21} when the switch is on) at low frequencies. Therefore, finding the optimal device size (see Chapter 3) and the proper bias conditions are essential requirements for optimal switch performance results. Equations 2 and 3 show that I_D is directly proportional to $V_{GS} - V_{TH}$ and V_{DS} , and V_{GS} and V_{DS} are the main bias tuning knobs. A detailed derivation of this equation is found in several microelectronics books, including [56], [55]. As stated previously, at higher frequencies the parasitic capacitances become the main source of insertion loss due to capacitive coupling to the substrate [58].

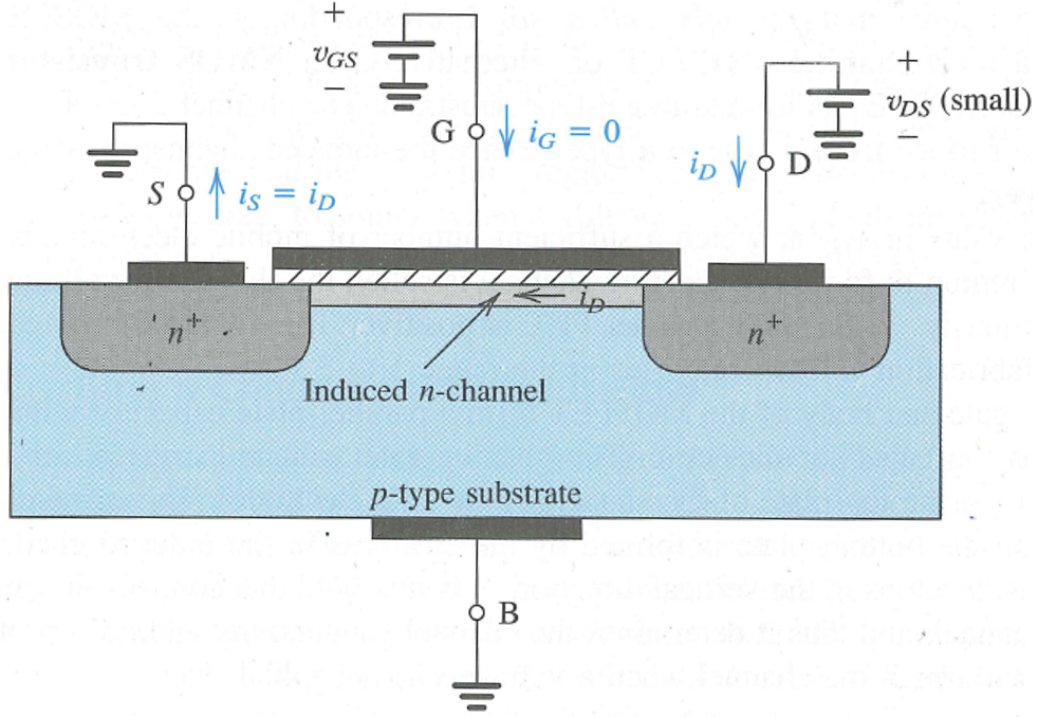


Figure 5. Cross sectional view of generic bulk nFET transistor biased in the linear region showing the induced n-channel layer [53].

$$I_D = k'_n \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (2)$$

Assuming a very small V_{DS} (i.e., 50 mV),

$$I_D \cong k'_n \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} \quad (3)$$

where,

$$k'_n = \mu_o C_{ox} \quad (4)$$

The term k'_n in Equations 2 and 3, is known as the process transconductance parameter, and it is expressed in terms of μ_o , the charge carrier mobility and C_{ox} , the capacitance per unit gate area, as shown in Equation 4. The I_D (Equation 3) is relevant in this investigation since it easily provides information about important parameters, such as the carrier mobility μ_o and the on-resistance (R_{ON}) of the transistor. From these measurements the transistor

behavior at low temperatures can be determined and in turn it provides understanding about the RF performance of the switch circuits.

2.6 RF Switches Overview

RF switches are widely used in various mixed-signal applications for space-based electronics (e.g., radar systems, satellite communications systems, and various instrumentation systems) [60]. Therefore, it is important to understand the robustness of their RF performance while operating in extreme environments (i.e., radiation-rich environment and at cryogenic temperatures). This knowledge will help system architects and circuit designers better comprehend how system operation can be influenced by both radiation exposure and cryogenic temperatures. More importantly, these results will provide the knowledge needed to design mitigation strategies for the damaging effects. An application highlighting the relevance of RF switches is shown in Figure 6, a conceptual block-diagram of a phased-array radar system. In this example, the single-pole double-throw (SPDT) switch interfaces with three different and essential circuit blocks: the phase-shifter, the power amplifier (PA), and the low-noise amplifier (LNA). Recent studies have reported on single event effects (SEE) on various RF circuit blocks [36, 39, 41]. However, very little attention has been placed on the RF switch. In this work, only nFET-based RF switches are considered.

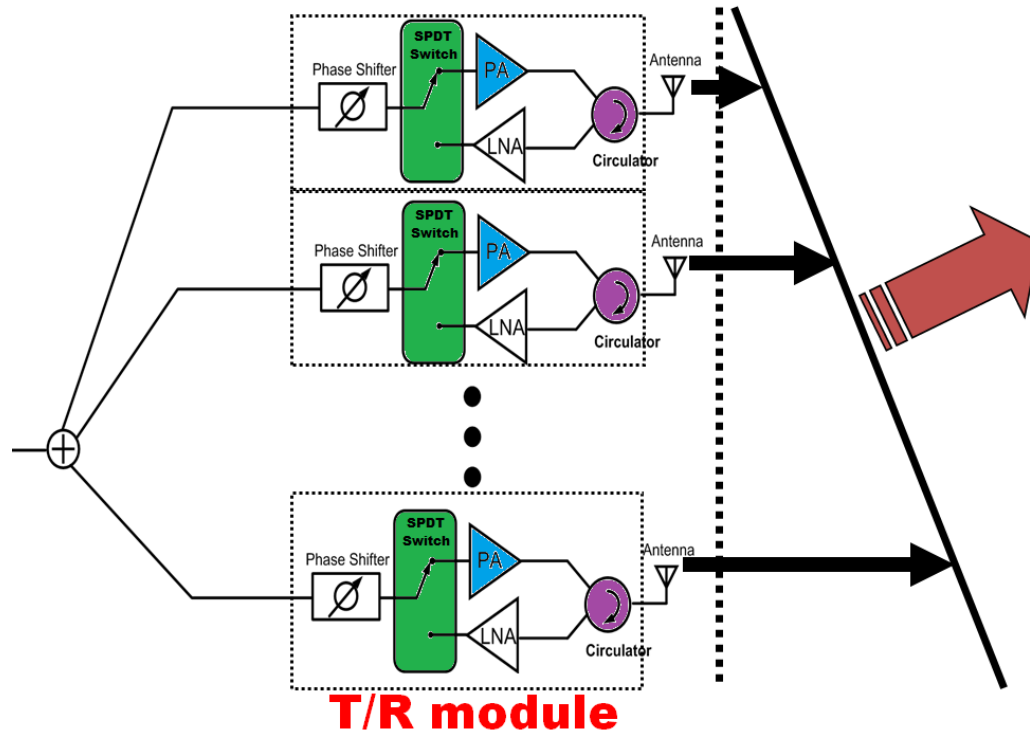


Figure 6. Block diagram of conceptual phased array radar system, showing the various sub-blocks circuits in transmit-receive (T/R) modules including the RF switches.

The main advantage of using nFETs over SiGe HBTs in the design of RF switch blocks for space-based electronic systems is the reduction in *dc* power consumption while simultaneously satisfying low IL, moderate isolation (ISO), and linearity requirements. Space-based electronic systems have stringent *dc* power constraints (e.g., the Mars Rover Curiosity, a robotic system for space-exploration). Therefore, using SiGe HBT-based switches instead of FET-based switches in such systems would increase the power budget significantly. According to the literature [61, 62], an HBT-based switch consumes approximately 3 to 10 mA of *dc* current as it transitions between the ON and OFF state. On the other hand, FET-based switch consumes approximately 2 μ A to 10 μ A. Due to the BiCMOS nature of all SiGe platforms, using SiGe HBTs for the RF functionality (PA, LNA, etc.) and FETs for the RF switches constitutes a necessary tradeoff between the circuit RF specifications (e.g., IL, ISO, and linearity) and the circuit *dc* power consumption [8].

The key figures-of-merit (FoM) for an RF switch are insertion loss (IL), isolation (ISO) and linearity. The IL and ISO are measured using the two-port scattering parameter (S-parameter) S_{21} , which is computed from the ratio of the transmitted signal power at port 2 (output) to the incident signal power at port 1 (input). S_{21} translates to IL when the switch is “ON” and ISO when it is “OFF” [7]. The linearity can be measured by either the power at the 1-dB compression point (P_{1dB} , i.e., large signal) or by the input-referred third-order intercept point (IIP3, i.e., small-signal). P_{1dB} indicates the input power level (P_{in}) that causes the insertion loss (S_{21}) at a certain frequency to drop by 1 dB. IIP3 is the extrapolated point where the fundamental tone and the third order distortion product intersect. The design specifications for the RF switch block vary according to the system application requirements. An optimum RF switch design should achieve a low IL, moderate ISO, and high linearity. Due to inherent limitations (resulting from the low resistivity substrate) of the bulk CMOS FETs, meeting all of the above requirements simultaneously becomes very challenging for wideband applications [57].

CHAPTER 3

DESIGN AND CHARACTERIZATION OF HIGH-ISOLATION SPST AND SP4T RF SWITCHES

The design and characterization of high-isolation SPST and SP4T switches at room temperature and at cryogenic temperatures are presented in this chapter. This work is the first demonstration on the cryogenic performance of wideband and high-isolation RF switches. The goal of this work is to investigate and analyze how the switch RF performance is impacted at low temperatures.

3.1 SPST RF Switch Design

The switch circuit topology and the corresponding photomicrograph are shown in Figure 7(a) and (b). The topology chosen is based on an alternating shunt-series configuration. The main benefit of this topology is that it achieves high isolation by using two shunt transistors, M_1 and M_3 . M_1 can be sized independently of M_3 , thus becoming an additional tuning knob to improve the input matching (S_{11}) of the switch. In multi-throw switches for multi-band applications, this extra tuning knob becomes an important advantage, as each switch throw-arm can be individually configured for a certain frequency band.

While the use of two shunt-arm transistors achieves high isolation (ISO), the additional shunt arm M_3 provides an extra leakage path due to parasitics, and degrades the insertion loss (IL). To compensate for this IL degradation, triple-well (TW) devices were used for the series arms (M_2 and M_4). The TW provides added substrate isolation and body bias control through the n-well terminal. The additional isolation increases the effective substrate resistance, thereby minimizing the amount of RF leakage through the substrate. Parasitic loss is reduced, and this reduction results as an improvement to the switch IL to compensate for the additional shunt arms, M_1 and M_3 . A cross-sectional view of a TW nFET is shown in Section 2.5 of Chapter 2.

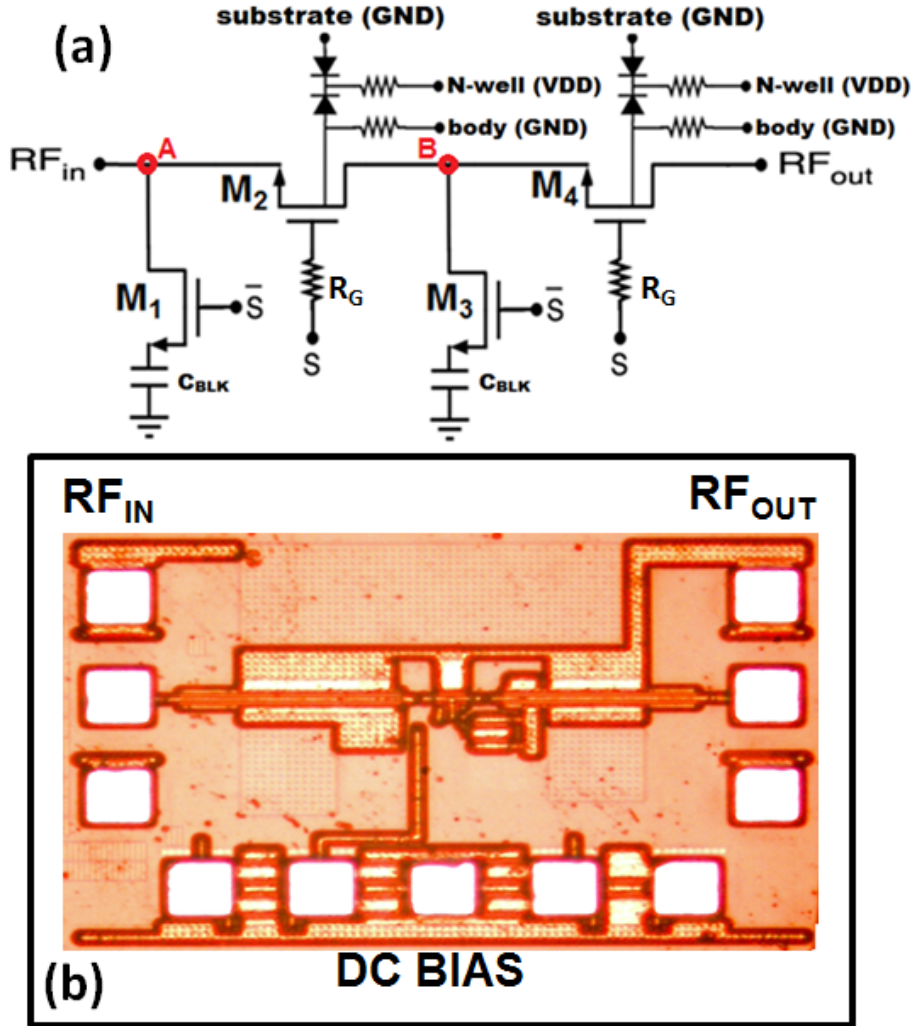


Figure 7. (a) The circuit schematic diagram for the single-pole single-throw (SPST) switch and (b) Photomicrograph of the SPST circuit.

Standard bulk nFETs were used for the shunt arms M_1 and M_3 , as TW devices do not provide any added improvements in isolation [59]. This assumption was verified through circuit simulation. All four devices were sized to maximize ISO and provide moderate IL at the bandwidth of interest (1 to 40 GHz). Optimal gate widths for the series transistors M_2 and M_4 were $30\ \mu\text{m}$ each, implemented as 10 fingers with each finger being $3\ \mu\text{m}$ wide. The first shunt arm M_1 was $9\ \mu\text{m}$ (made of 3 fingers with each being $3\ \mu\text{m}$ wide). The second shunt arm M_3 was $20\ \mu\text{m}$ wide (5 fingers each $4\ \mu\text{m}$ wide). All devices had the minimum effective gate length of $120\ \text{nm}$, less than the lithographic (mask) gate length of

130 nm. The SPST switch presented here was designed for radar applications that require high ISO (> 35 dB at 40 GHz) and moderate IL (< 6 dB at 40 GHz) over a very wide frequency band.

3.2 SP4T RF Switch Design

The SPST switch described in the previous section 3.1 was used as a building block for the SP4T switch circuit. The SP4T block diagram and its corresponding photomicrograph are shown in Figure 8(a) and (b), respectively. The main design challenge while combining the SPST block into an SP4T switch was to maintain the switch IL within the design specification (i.e., < 6 dB from 1 GHz to 40 GHz) without reducing the ISO. To achieve these specification M_3 and M_4 were carefully optimized to provide adequate trade-off between the IL and the output return loss. CMOS inverter blocks (not shown in the diagram) were implemented to drive the gates of the transistors along with a two-to-four decoder circuit to reduce the number of digital inputs required for testing and when integrating it in a RF system.

The connecting RF transmission lines were implemented using a grounded coplanar waveguide (CPW). The CPW lines were designed and simulated using Sonnet, a full-wave EM modeling tool. The simulation results showed a mutual coupling of less than 70 dB at 40 GHz, while maintaining a 50- Ω match at the input and output ports. To further minimize coupling and increase isolation between adjacent input ports, the layout was carefully planned so that each adjacent throw-arm was placed horizontally shifted in an alternating pattern, as shown in the photomicrograph Figure 8(b).

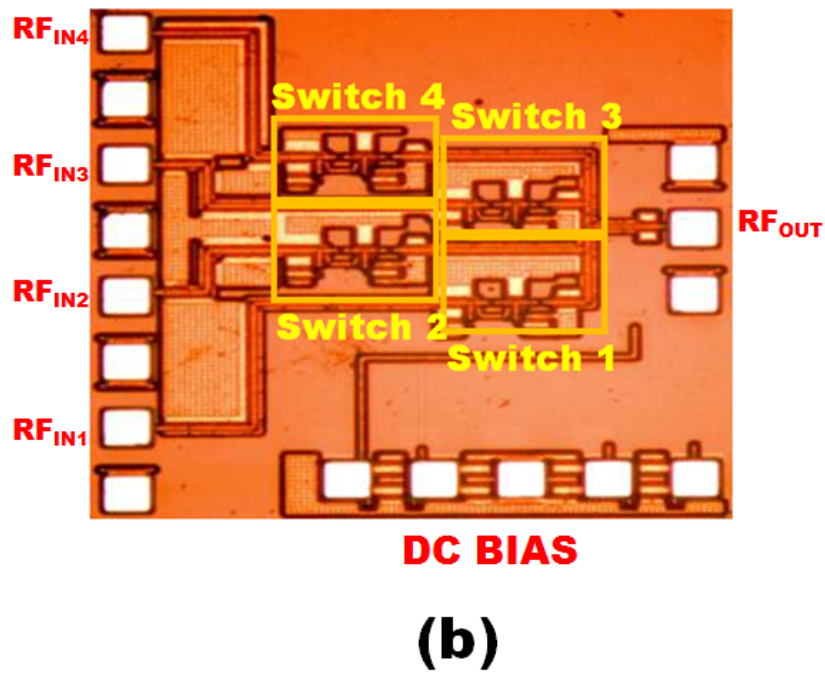
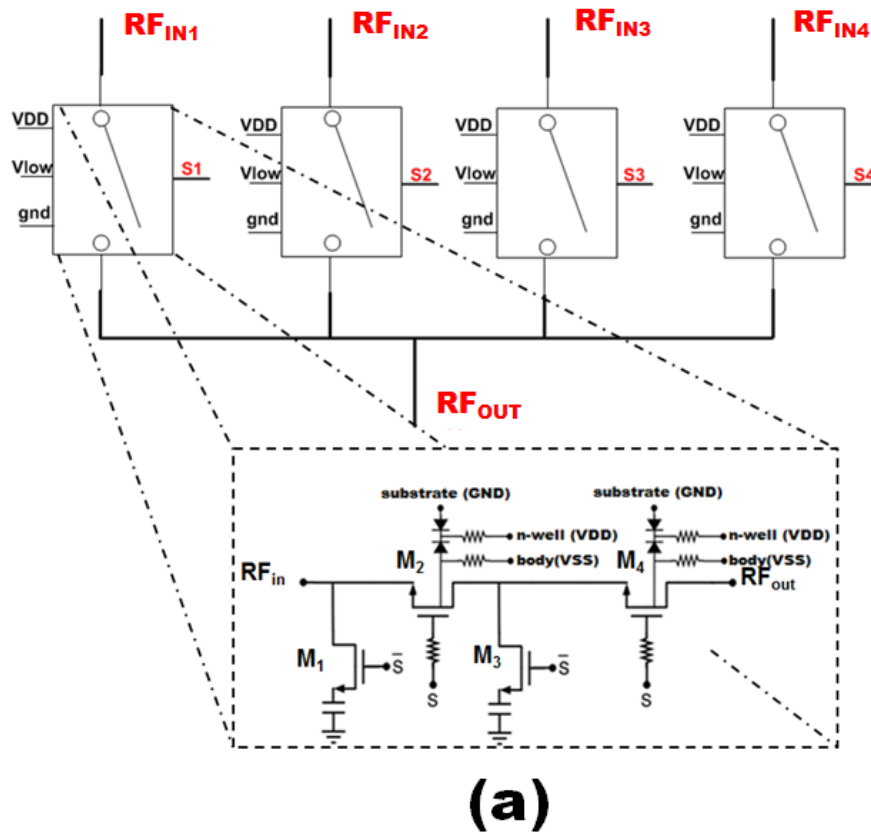


Figure 8. (a) Block diagram of the single-pole four-throw (SP4T) switch circuit using the SPST as the building block (b) Photomicrograph of the fabricated SP4T switch.

3.3 Experimental Setup

Figure 9 illustrates the custom-designed, on-wafer, open-cycle liquid nitrogen (LN₂ temperatures) probe station made by Lakeshore Cryotronics. A closer view of the on-wafer cryogenic dewar highlighting some of the relevant equipment (e.g., dc and RF probes, calibration substrate, camera) is shown in Figure 9. The RF performance of both SPST and SP4T switches was measured over a temperature range of 300 K down to 90 K. Cable and probe losses were measured on-wafer using the Short-Open-Load-Through (SOLT) calibration with an Impedance Standard Substrate (ISS) at each temperature point. S-parameters were measured from 10 MHz to 30 GHz using an Agilent E8364C PNA. The results presented here were reproducible over multiple measurements and samples. The cryogenic linearity measurements required a careful de-embedding procedure to verify that the results were correct. The same cryogenic probe station was used for the linearity measurements in addition to the following equipment: signal generator (HP E83732A), power meter (Agilent E4419), wideband amplifier (HMC-C004), bi-directional coupler (Agilent 87301D), and isolators (Ditom D3I8018). A block diagram of the complete cryogenic measurement setup for both linearity and S-parameters characterization is shown in Figure 10. A total of six samples were characterized over-temperature, three SPST and three SP4T circuits.

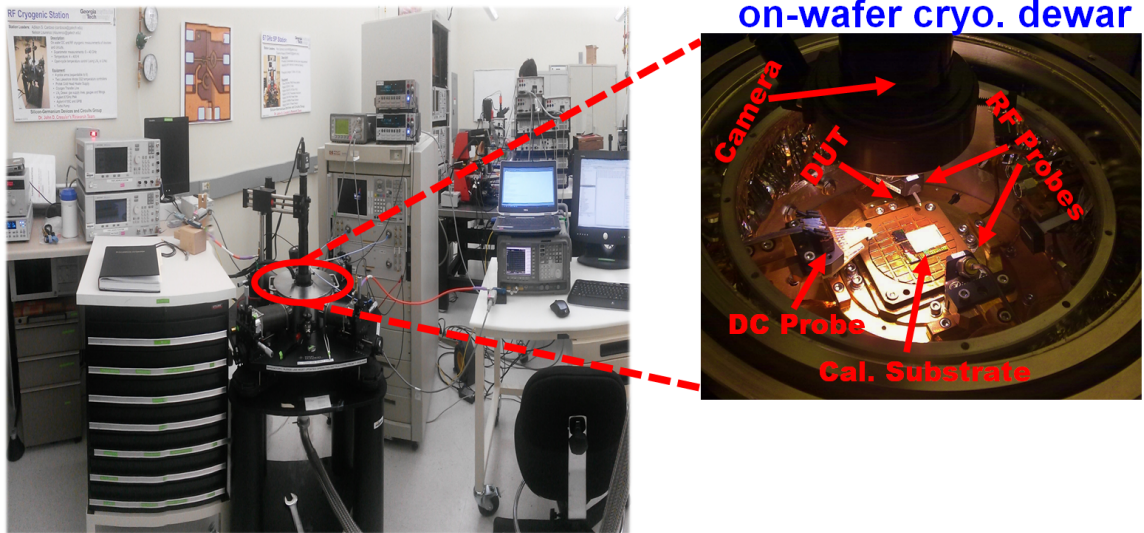


Figure 9. Photo of the open-cycle cryogenic station measurement setup, and a closer view of the on-wafer cryogenic dewar.

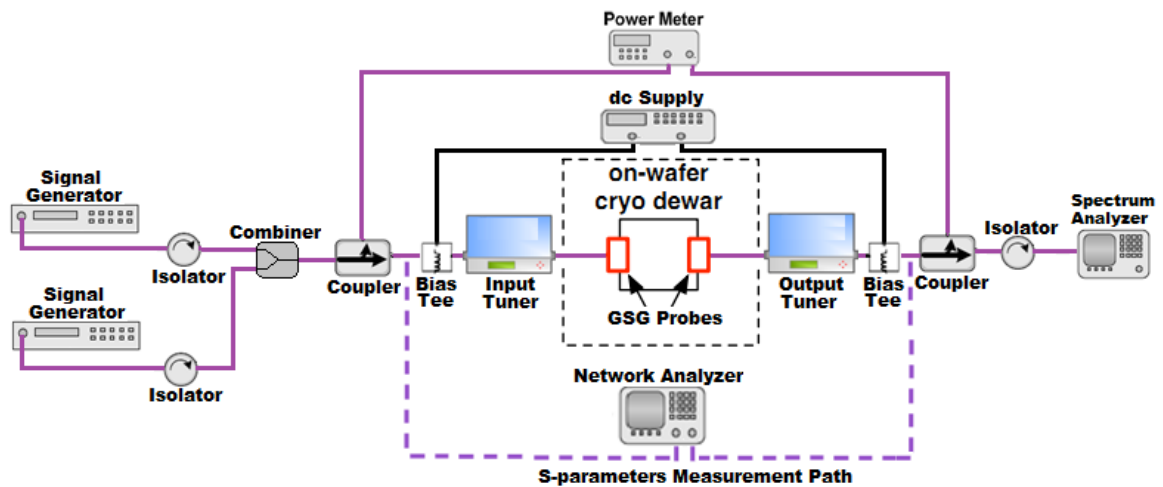


Figure 10. Cryogenic measurement setup for both linearity and S-parameters characterization.

To account for the losses between the signal generator and DUT (device under test), a “2-tier fixture calibration” procedure was performed. At the end of this procedure, three files will be created: an input file, an output file, and an input-coupled path file that were used to de-embed the measurements to the reference plane at the DUT pads. The first step was to verify the input coupled path using a Vector Network Analyzer (VNA) from Agilent

(model E8364B); the test setup used is depicted in Figure 11. The dashed lines around the “isolator” block means that it was not used on this experiment, however, it is recommended to use an isolator in case the DUT has a poor input match (S_{11}). The result file needs to be saved in units of dB using the “.s2p” file extension format (e.g., file name “Input-Coupled-Path.s2p”). The coupling factor depends on the loading termination (return loss, S_{11}) of the output port of the coupler; therefore, a 50- Ω termination is needed at the “thru” path of the coupler. In case of poor input match an isolator should be used (marked in red dashed lines in Figure 11), and if it used, it needs to be accounted for in the input-coupled path measurement. The next step after verifying the input coupled path is to perform a cable level calibration using coaxial calibration standards and the results is to be saved in the “.s2p” file format (e.g., file name “Cable-Cal.s2p”).

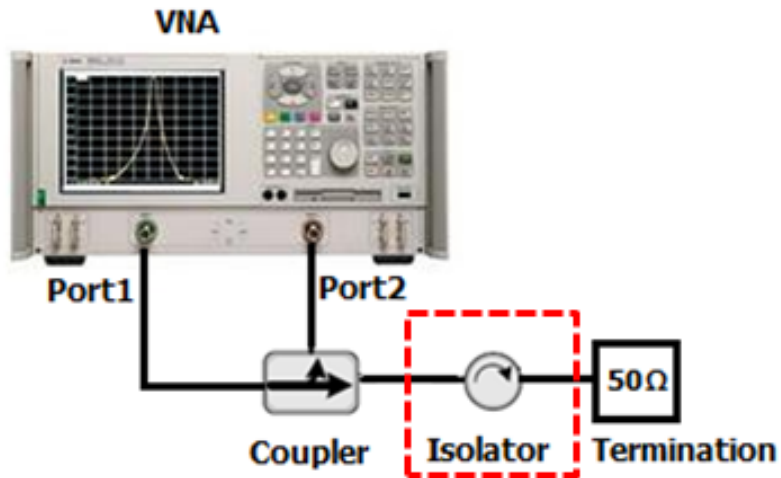


Figure 11. Measurement setup to verify the input coupled path loss.

The final step in this procedure is to perform a probe level calibration using the setup shown in Figure 12. In this test setup, the coupled path of the coupler is terminated using a 50- Ω termination standard, SOLT calibration substrate is used with an VNA to capture the S-parameters. The files need to be saved as “.s2p” file format (e.g., file name “Probe-Tip-Cal.s2p”). Once this calibration is complete, VNA can be used to create the input and output de-embedding fixture files.

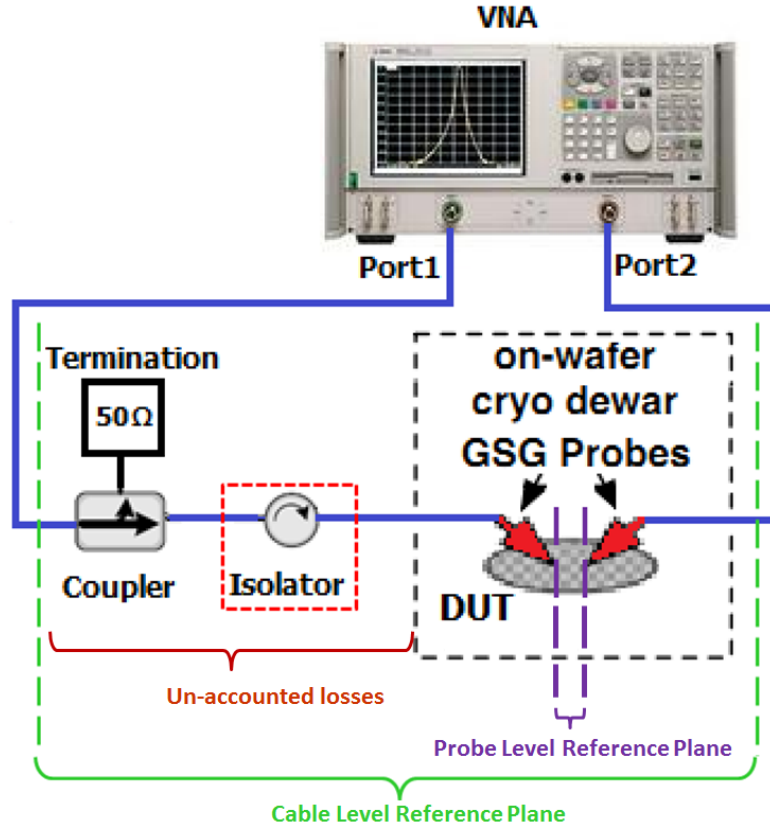


Figure 12. Probe level calibration measurement setup to de-embed for un-accounted equipment and cable losses.

3.4 SPST Switch RF Performance at Cryogenic Temperatures

The measured RF performance, IL, ISO, and linearity of the SPST switch at three different temperature points, 290 K, 190 K, and 90 K are shown in Figures 13, 14, and 15, respectively. At lower frequencies (< 15 GHz) the SPST IL shown in Figure 13 decreases with reducing temperatures (> 1.5 dB). However, at high frequencies (> 15 GHz) the IL does not follow the same trend as temperature decreases from 190 K to 90 K. The limiting factor that prevents the IL from continuing to improve with high frequency as temperature is lowered is potentially due to an increase of the parasitic capacitances. The parasitic capacitance increases the capacitive coupling to the substrate resulting in an increase in the RF signal loss [63].

The measured switch ISO is shown in Figure 14, and it appears that it does not vary

significantly with temperature; however, the inset graph reveals that the switch ISO does improve as the temperature decreases (e.g., around 30 GHz the ISO is ≈ -37 dB at room temperature (296 K), at 190 K it improves to ≈ -39 dB, and at 90 K it further improves to -41 dB). The power handling capability (i.e., switch linearity) is another important figure-of-merit for a switch. The measured P_{1dB} of the SPST switch as a function of temperature at three different frequencies, 10 GHz, 15 GHz and 20 GHz are shown in Figure 15. For all three frequency points the switch linearity shows a increase of approximately 2 dB with from 300 K down to 78 K.

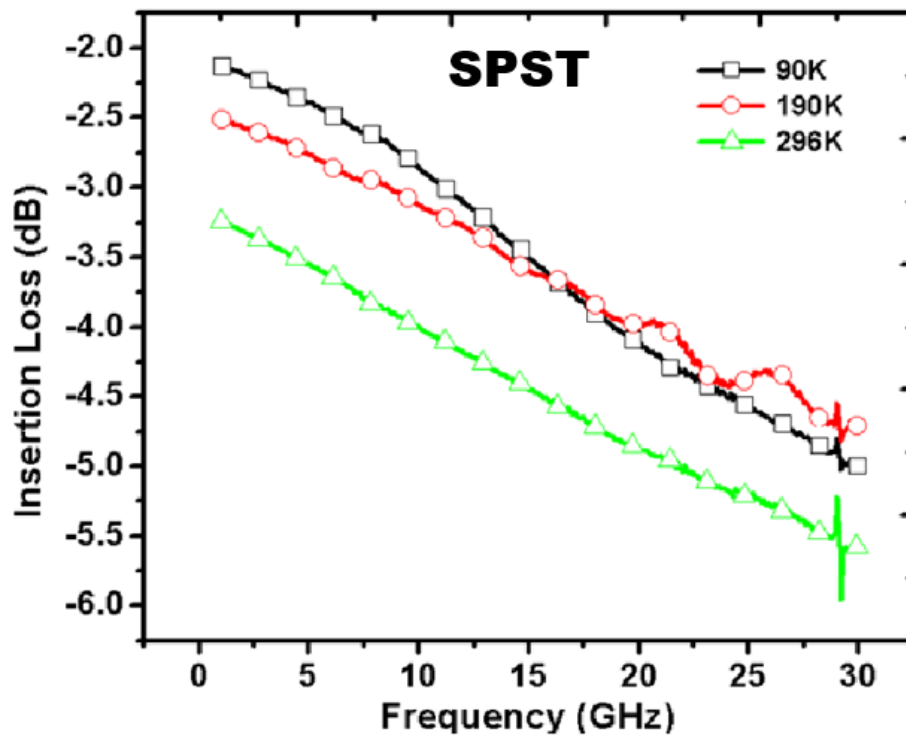


Figure 13. SPST RF switch measured Insertion Loss (IL) performance at various temperature points.

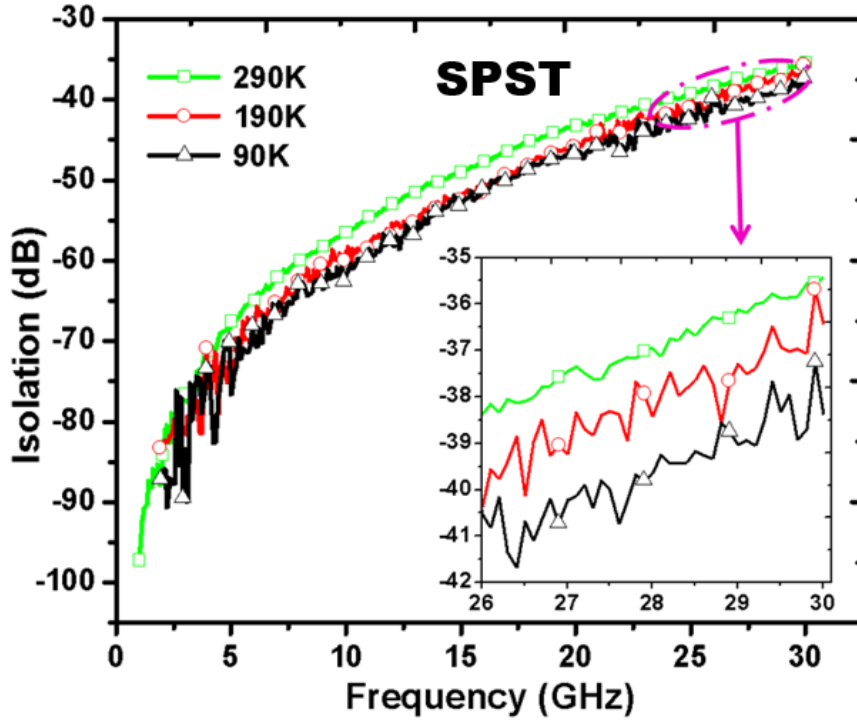


Figure 14. SPST RF switch measured Isolation (ISO) performance at various temperature points.

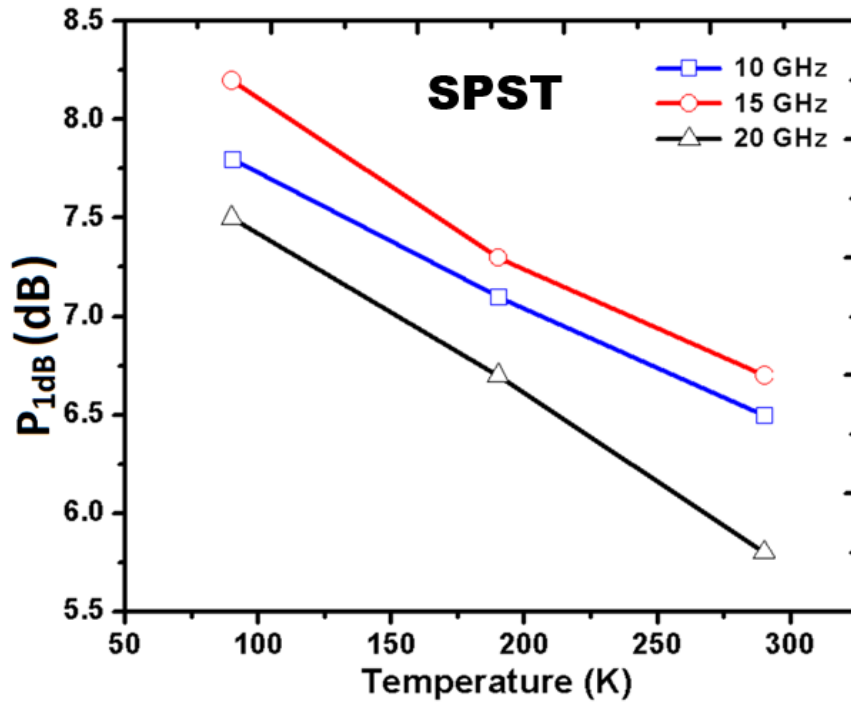


Figure 15. SPST RF switch measured large-signal linearity (P_{1dB}) performance at various temperature points.

3.5 SP4T Switch Performance at Cryogenic Temperatures

The measured SP4T RF performance (i.e., IL, ISO, and linearity) at various temperature points are shown in Figures 16 (IL), 17 (ISO), and 18 (P_{1dB}). As anticipated, the IL of the SP4T switch improves as temperature decreases down to cryogenic temperatures (as shown in Figure 16). The SP4T circuit IL improves by more than 3 dB from 10 to 30 GHz. The SP4T isolation (S_{21} when switch is OFF), measured from input to output terminals follows a similar trend as the SPST circuit as shown in Figure 17. At mid-band frequencies (10 GHz to 25 GHz) the data shows a higher isolation improvement with the decreasing temperature, ≈ 10 dB at 15 GHz. This mid-band isolation improvement may be attributed to the constructive interaction of the parasitic capacitances at the output node of the SP4T circuit. Based on a first-order approximation, the parasitic capacitances were previously shown to be temperature independent. However, the parasitic devices are frequency dependent. At low frequencies (< 5 GHz) and at high frequencies (> 25 GHz) the observed improvement is minimal < 1 dB. The SP4T isolation result is a good example of how the device parasitics (e.g., resistance and capacitances) can impact the switch performance at different frequency points. The measured SP4T linearity at three frequency points (10 GHz, 15 GHz, and 20 GHz) are shown in Figure 18. These measured results follow a similar trend as the SPST switch (i.e., insertion loss, isolation, and linearity improve with decreased temperature). To better understand these results single transistor test structures were characterized across temperature, and the measured results and analysis are presented in Section 3.6.

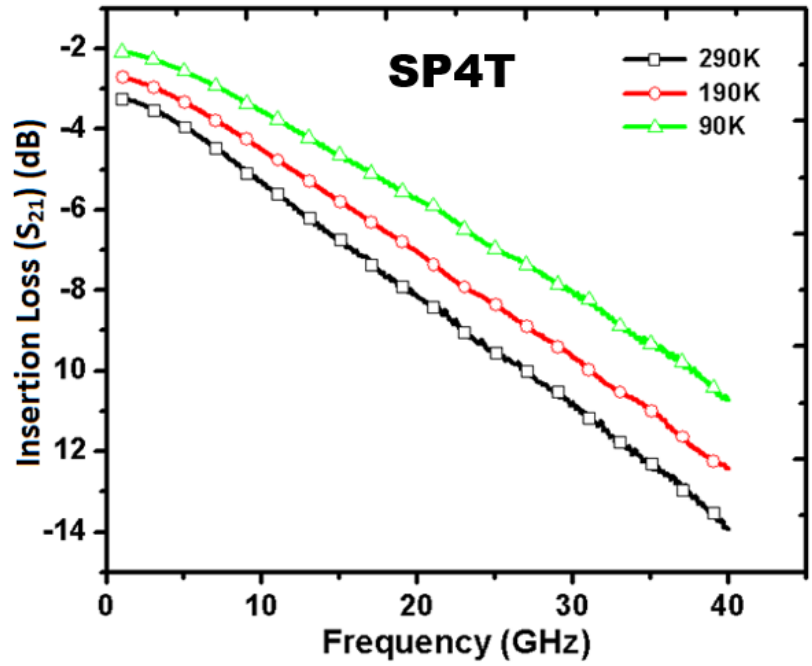


Figure 16. SP4T RF switch measured Insertion Loss (IL) performance at various temperature points.

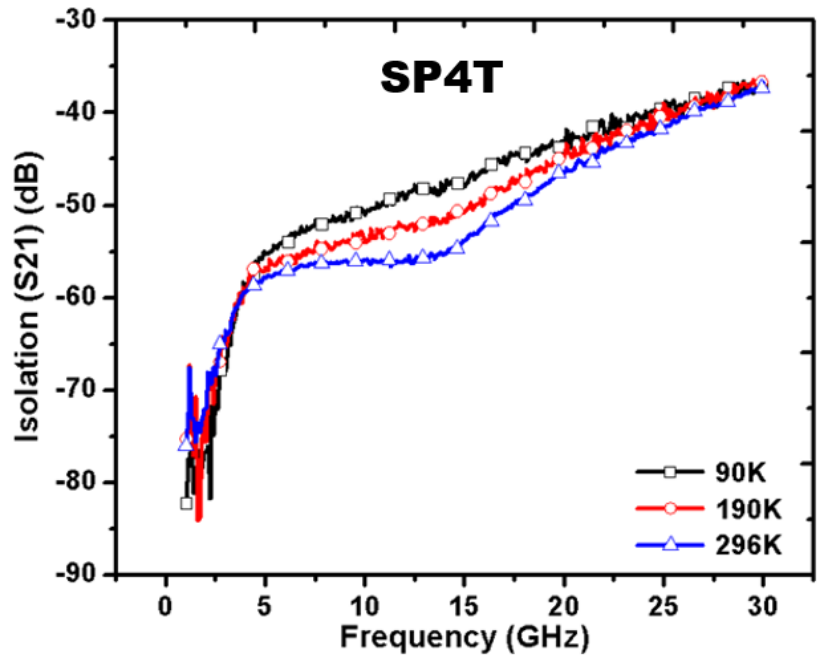


Figure 17. SP4T RF switch measured Isolation (ISO) performance at various temperature points.

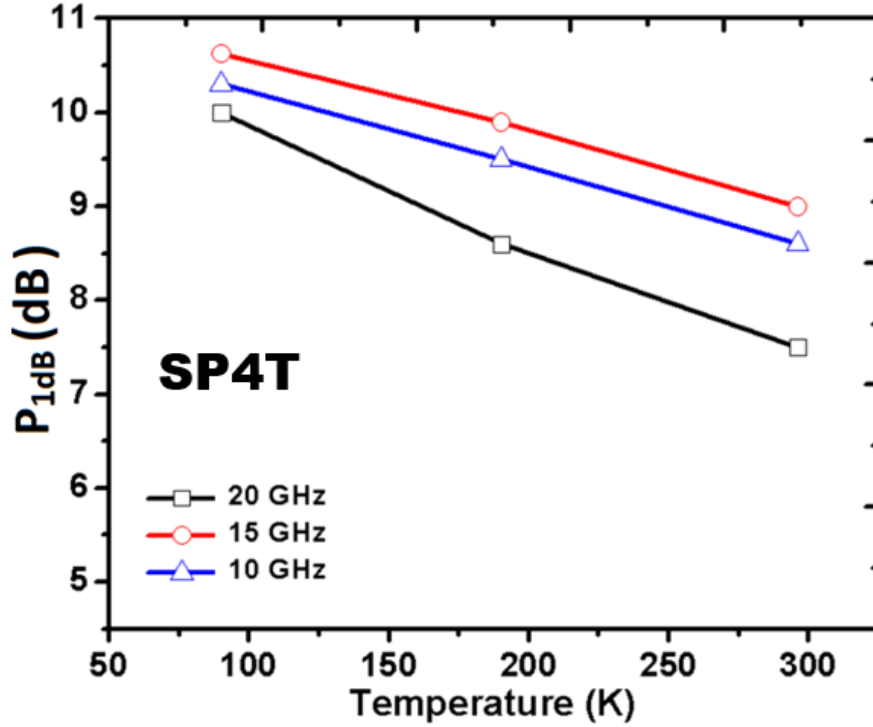


Figure 18. SP4T RF switch measured large-signal linearity (P_{1dB}) performance at various temperature points.

3.6 Cryogenic Operation of Standalone FET Devices

The measured dc performance is presented to a more in-depth understanding on the cryogenic results obtained from the FET-based RF switches. Prior works have demonstrated that the main advantages of operating FET transistors at liquid nitrogen (LN2) performance are the reduction in power delay product, decreased chance of latchup, increased switching speeds (i.e., the required time to charge and discharge circuit capacitances), increased carrier mobility, and improvement of the threshold voltage (V_{th}) [53]. The increased carrier mobility with cooling is important in understanding the RF performance of the switches at low temperatures.

3.6.1 FET DC Cryogenic Performance

The dc measurements, g_m and I_D as a function of V_{GS} of the bulk nFET biased in the linear region measured at three different temperatures are depicted in Figures 19(a) and (b),

respectively. These results confirm the literature findings, i.e., for the same bias condition the carrier mobility increases with decreasing temperature, thus the observed increase in the device transconductance, g_m . The measured g_m as function of gate voltage V_g at three temperature points, 296 K, 150 K, and 90 K is shown in Figure 19(a) for a bulk nFET device. From Equation 5, it is evident that g_m increases as the effective carrier mobility (μ_e) increases with decreasing temperature. The parameters in Equation 5, C_{ox} represents the gate-oxide capacitance, W the gate channel-width, L the the gate channel-length, V_{GS} the gate-to-source voltage potential, and V_{TH} the threshold voltage. The measured transfer characteristics (drain current, I_D as function of gate voltage, V_g) is shown in Figure 19(b). The g_m parameter is relevant because is the reciprocal of the on-resistance, R_{on} . The R_{on} parameter directly impacts the switch IL. Bulk devices of similar dimensions (0.12 μm length and 10 μm width) as the ones used on the RF switch circuits were characterized at the same temperature points.

$$g_m = \frac{\partial I_{DS}}{\partial V_{DS}} = \mu_e C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \quad (5)$$

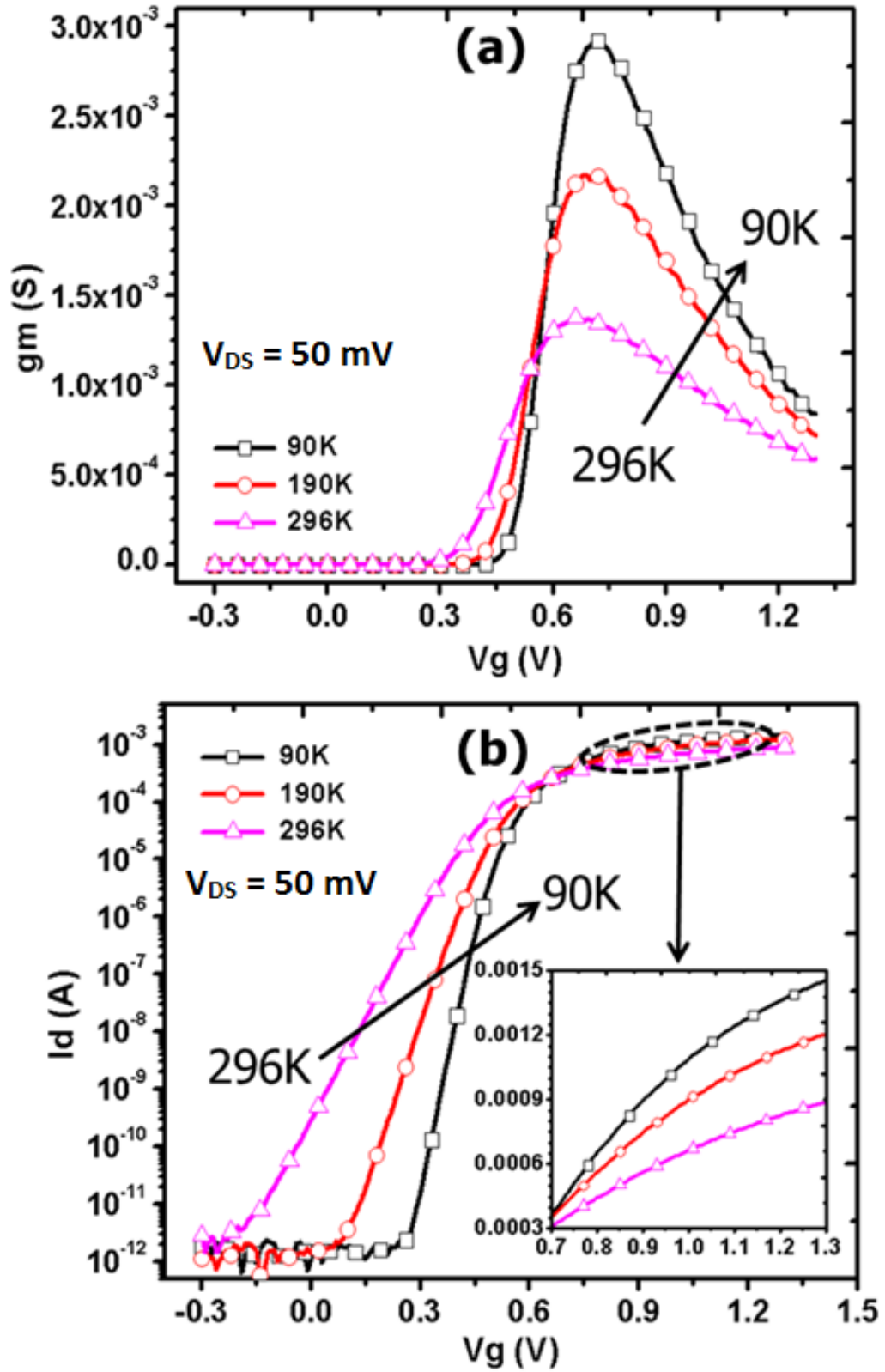


Figure 19. (a) Measured transconductance (g_m) as function of gate-source voltage (V_g), (b) Measured transfer characteristics of bulk nFET biased in linear mode at three temperature points, 296 K, 150 K, and 90 K.

The carrier mobility improves because the carrier scattering mechanisms reduce at low temperature [53]. There are three main scattering mechanisms that dictate the carrier mobility in the inversion layer of transistors — the Coulomb, the surface, and the phonon scattering [54]. Coulomb scattering is mainly due to charge impurities, whereas surface scattering is caused by the roughness of the surface, crystal defects, foreign atoms, open bonds, and/or phonon scattering, also known as lattice vibrations. Lattice vibration is related to how a charge carrier traverses through a semiconductor crystal [45]. According to [54], only the Coulomb and the surface roughness mechanisms prevail at low temperature, and phonon scattering/lattice vibrations are more evident at room temperature. The calculations provided by [45] and [53] prove that the carrier mobility due to phonon scattering does increase as temperature decreases, and it is because of the reduced number of phonon at low temperature.

The measured transfer characteristics and calculated g_m for the TW device are shown in Figures 20(a) and (b). The TW devices follow a similar trend as the bulk devices. Based on measured results, g_m , I_D , and V_{TH} increase as the temperature decreases. After a close inspection, the TW device demonstrated a larger improvement in comparison to the bulk devices at cryogenic temperature. The larger improvement for the TW devices is attributed to the increased substrate resistance and smaller parasitic influences at low temperatures. However, since the TW transistors are approximately three times wider than the bulk transistors (i.e., TW is 32 μm wide and bulk is 10 μm for the same minimum gate length of 0.12 μm) this assumption was not confirmed.

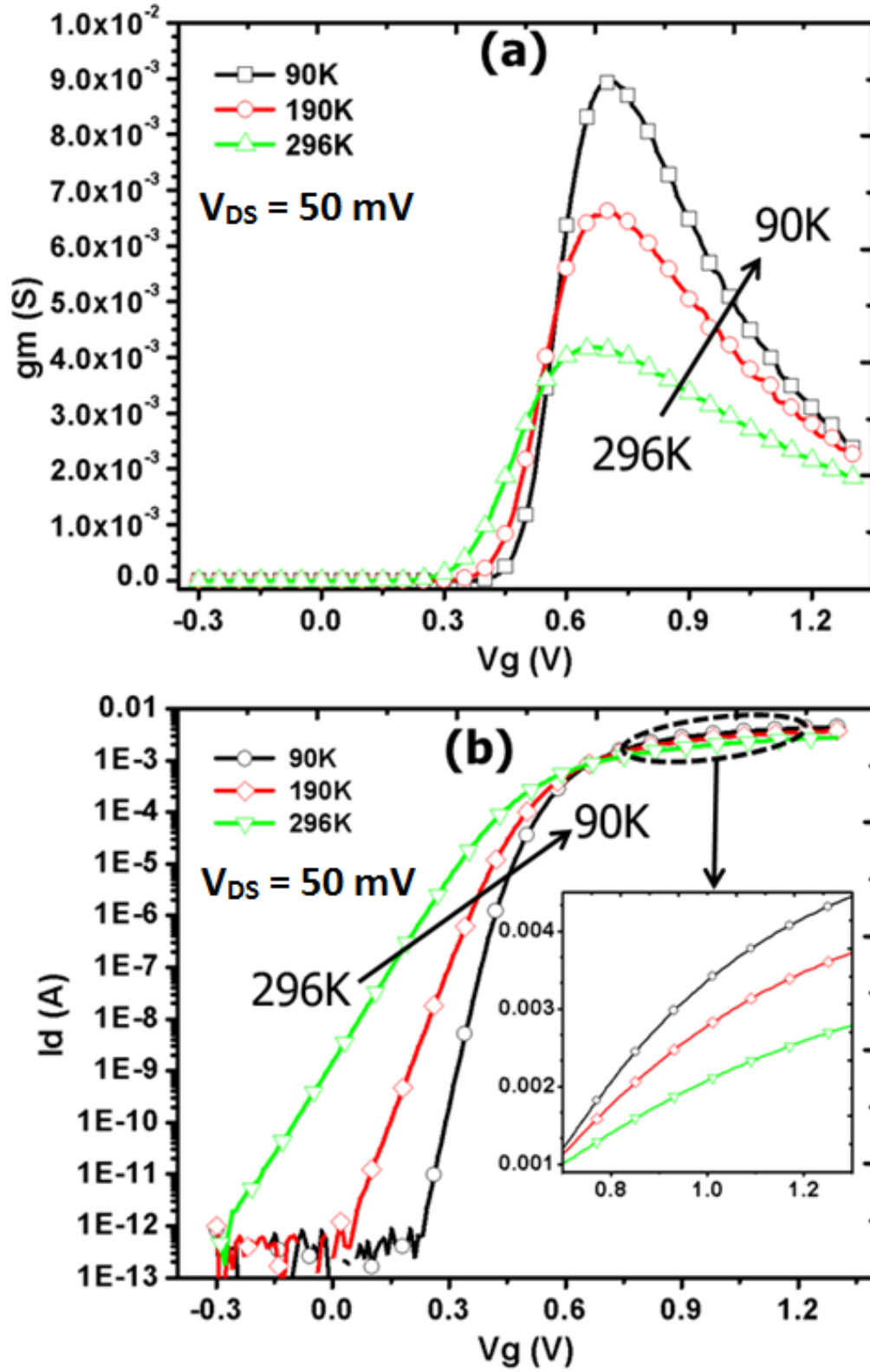


Figure 20. a) Measured transconductance (g_m) as function of gate-source voltage (V_g), (b) Measured transfer characteristics of TW nFET biased in linear mode at three temperature points, 296 K, 150 K, and 90 K.

3.6.2 FET RF Cryogenic Performance

The measured dc results confirm that the conductivity of the inversion layer is dependent on the carrier mobility, and since the mobility improves with decreasing temperature, the RF performance of the transistors is expected to improve at lower temperatures. The measured results are shown in Figure 21, and these results confirm the stated assumption. The measured IL, S_{21} , of the bulk FET at three temperature points, 90 K, 190 K, and 296 K are illustrated. As stated previously, the R_{on} of the switch directly influences the IL, and the response of R_{on} versus temperature can be analyzed using the triode current equation, Equation 2 (presented in Chapter 2.5). Since V_{DS} is close to zero (because both drain and source are biased at the same voltage), the R_{on} can be found to be as shown in Equation 6. By taking the ratio of this equation at cold temperature (COLD) and at room temperature (RT), the result is shown in Equation 7. These results confirm that as temperature decreases the electron mobility increases and R_{on} decreases (i.e., improves) for nFET devices. The equation also shows that as the threshold voltage, V_{TH} , rises at low temperatures the R_{on} will increase, thus degrading the IL. However, the electron mobility increases exponentially with decreasing temperature, while the threshold voltage only increases linearly [53]. Thus, the mobility ratio dominates the trend, causing an overall decrease in on-resistance which in turn decreases the IL of the devices at low temperatures.

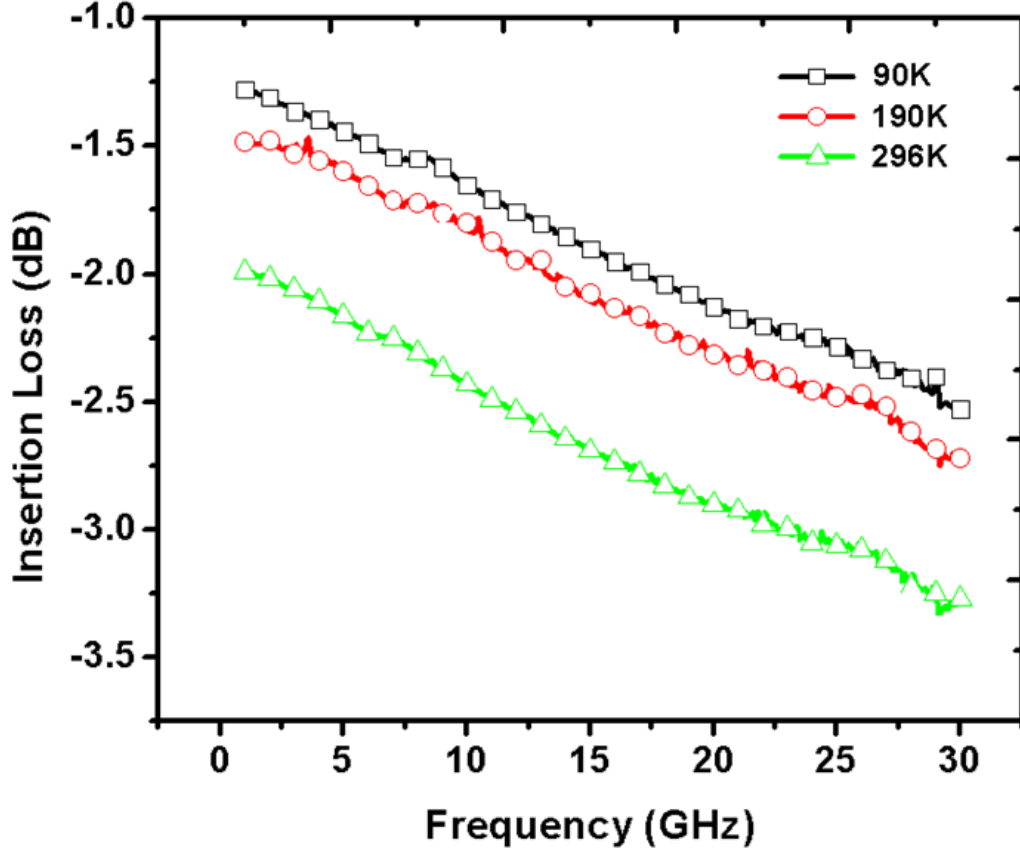


Figure 21. Measured insertion loss, IL (S_{21}) of a single bulk nFET device.

$$R_{on} = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right)^{-1} = \frac{L}{\mu_o C_{ox} W (V_{GS} - V_{TH})} \quad (6)$$

$$\frac{R_{on-COLD}}{R_{on-RT}} = \frac{\mu_{RT}}{\mu_{COLD}} \frac{(V_{GS} - V_{TH-RT})}{(V_{GS} - V_{TH-COLD})} \quad (7)$$

The measured RF performance of a single transistor (TW nFET) configured as an RF switch is shown at different temperature points in Figure 22. As anticipated, the results follow a similar improvement as the bulk devices. The improvements of the IL is directly related to the improvement of carrier mobility as temperature reduces. The carrier mobility improvement is proportional to the on-state current (I_D) and the on-state resistance (R_{on}) of the transistor. The S_{21} enhancement for the TW device is significantly higher than the bulk

(i.e., ≈ 1.1 dB) in comparison to (~ 0.6 dB), respectively. This significant improvement can be attributed to the TW devices having a higher substrate resistance and lower parasitic capacitances effects than the bulk devices. However, since the characterized devices did not have the same dimensions, this assumption was not confirmed.

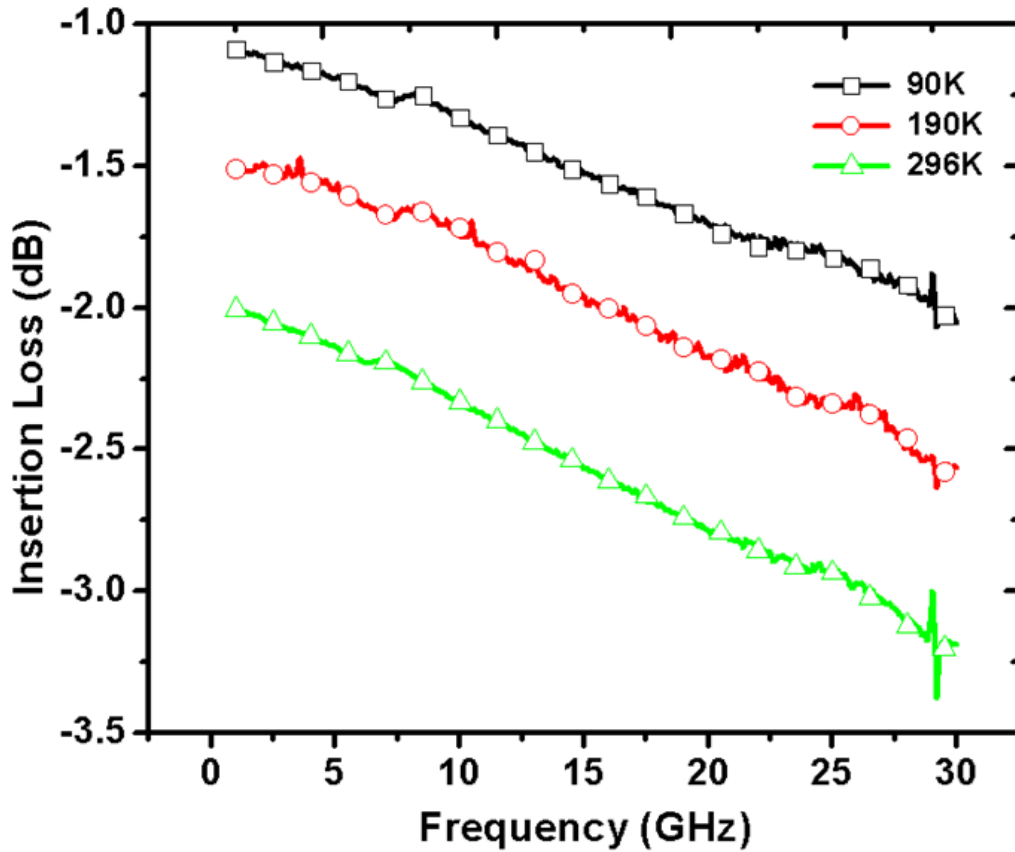


Figure 22. Measured insertion loss, IL (S_{21}) of a single TW nFET device.

3.7 Summary

An alternating SPST switch topology configuration was proposed, and the measured results demonstrated high isolation with excellent input matching and good linearity performance. The SPST demonstrated a measured isolation of greater than 46 dB at 23 GHz. The SPST circuit was used as the building block to design a SP4T switch. The SP4T switch achieved isolation between inputs ports of more than 40 dB, and input-to-output port isolation of >35 dB at 40 GHz. The SP4T also demonstrated acceptable linearity results, IIP3 of 19.6

dBm. Both SPST and SP4T circuits were characterized at cryogenic temperatures. The results at low temperature show that all key performance metrics like IL, ISO, large- and small-signal linearity improve with decreasing temperature. The IL improves by more than 3 dB for the SP4T and ≈ 1.5 dB for the SPST from 10 to 30 GHz. Stand-alone devices were also characterized at cryogenic temperatures to aid in understanding the performance enhancement. The results reveal that the carrier mobility increase at cryogenic temperature is the main reason for the RF switch performance improvement.

CHAPTER 4

DESIGN OF A LOW-LOSS, WIDEBAND SPDT SWITCH AND SWITCHED-LINE PHASE SHIFTER IN A RF CMOS ON SOI TECHNOLOGY

Low-loss, wideband (DC to 40 GHz) single-pole double-throw (SPDT) RF switches implemented in a 180 nm SOI CMOS technology are presented [5]. As it was discussed in chapter 3 high performance radio-frequency switches find widespread application in a variety of electronic systems. Switched-line phase shifters, transmit-receive (T/R) switches, multi-mode and multi-band transceivers, phased arrays, reconfigurable and self-healing systems are a few of the applications that require high-performance RF switches. An application highlighting the use of RF switches is illustrated in Figure 23, a conceptual block-diagram of a generic RF transceiver. In this example, the single-pole double-throw (SPDT) switch interfaces with three different and essential circuit blocks: the RF antenna, the power amplifier (PA), and the low-noise amplifier (LNA). In such application, the performance of the system is primarily limited by the insertion loss (IL). Thus, the IL of the switch is often the most important design metric.

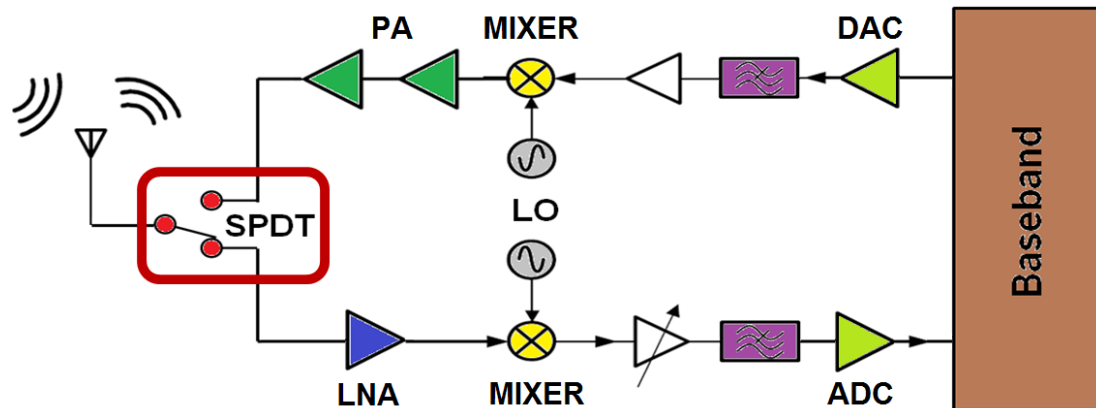


Figure 23. A conceptual RF transceiver block diagram.

Minimizing IL involves a trade-off with other switch performance metrics such as ISO, bandwidth, and signal handling capability [57]. In narrow-band designs, it is typical to

take advantage of LC resonance (or inductive peaking) to reduce loss [64]. For wide-band switches, the options to reduce the loss are limited. The primary method of achieving low-loss is to reduce the loss through the gate and substrate of the FETs [65, 66]. Another common method to reduce high-frequency signal power from leaking to the substrate is to add a large resistor to the gate, but this limits the switching speed [8].

SOI CMOS technologies are naturally suited for low-loss FET-based switches since the isolated bulk reduces the loss through the substrate [67]. For this switch design a π -matching network is implemented to achieve one of the lowest reported IL switches in 180 nm CMOS on SOI. This design is targeted towards low-loss and wideband applications (e.g., transmit/receive modules in an RF transceiver front-end) [5]. This switch design can be easily migrated to any 180 nm SOI based BiCMOS process. With the added leverage of integrated high-performance bipolar transistors, BiCMOS processes are better suited for a wide range of high-frequency applications, a liberty that is not currently available in a 45 nm SOI process. Although [63] has reported a comparable IL at 45 nm with a similar topology, a 180 nm implementation provides a decided advantage for low-cost applications.

4.1 Switch Design

The switch schematic diagram and the corresponding photomicrograph is shown in Figure 24(a) and (b), respectively. The SPDT circuit is based on a series-shunt topology. The device dimensions were chosen based on the competing requirements of IL, ISO, and linearity. The tradeoff between the switch IL and ISO as the width of the series FET changes is shown in Figure 25. Large series devices (M1, M3) reduce the switch on-resistance, and hence, IL at low frequency. However, at the same time, increased parasitic capacitances due to the large devices limit the bandwidth of operation and degrade ISO. Increasing the size of the shunt devices (M2, M4) improves ISO at the cost of a small decrease in IL due to the added parasitic capacitance. Two versions of the switch using low (1.5 V) and high-voltage (2.5 V) FETs were designed. For the 1.5 V design, the sizes of M1, M3 and M2,

M4 are 125/0.18 μm and 40/0.18 μm , respectively. For the 2.5 V design, larger devices were used; the size of M1, M3 is 260/0.32 μm and that of M2, M4 is 105/0.32 μm . Large gate resistances ($R_1, R_3 = 17.5 \text{ k}\Omega$ and $R_2, R_4 = 13 \text{ k}\Omega$) were chosen to minimize RF signal leakage through the gate.

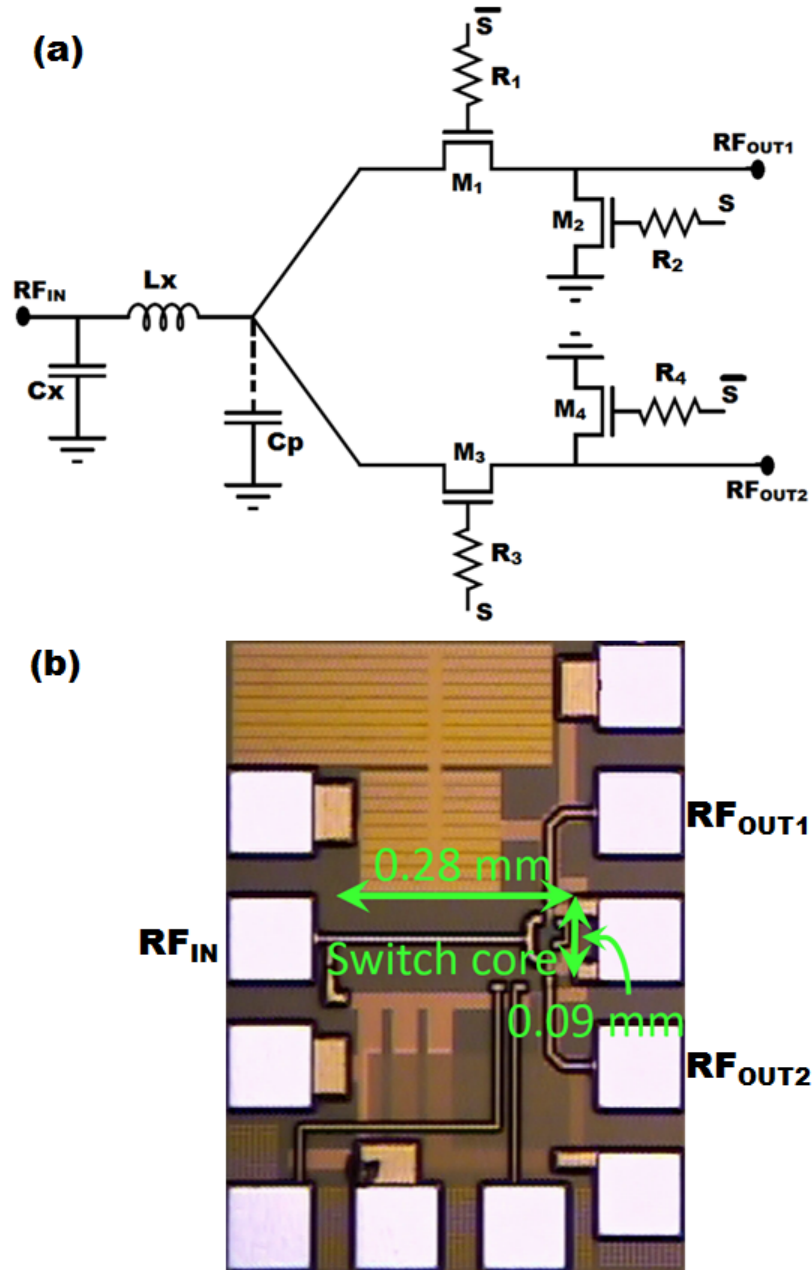


Figure 24. (a) Schematic of the SPDT RF switch, and (b) Photomicrograph of the fabricated SPDT circuit.

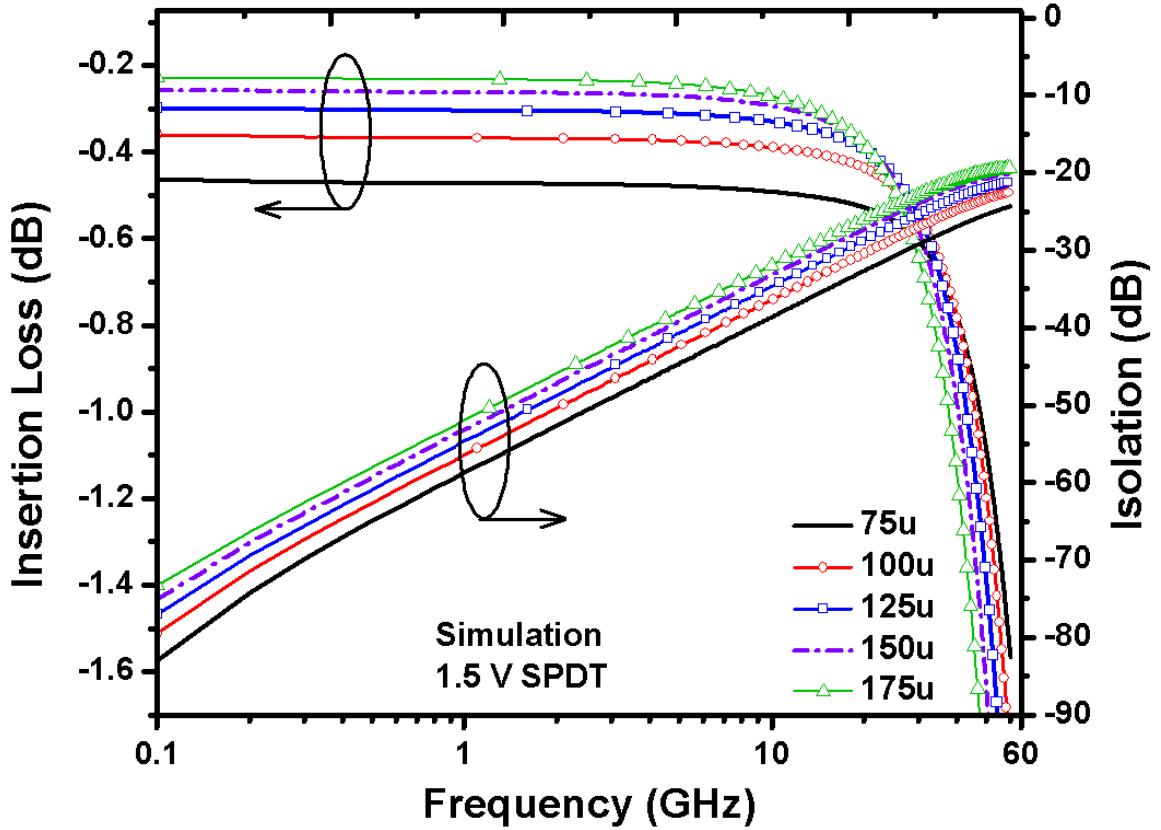


Figure 25. Simulated IL and ISO as a function of series FET width.

The matching network implemented consists of a series inductor, L_x and a shunt capacitor, C_x (shown Figure 24(a)). A die photograph of the 1.5 V switch is shown in Figure 24(b). The parasitic capacitances (C_p), together with the matching network, form a π -match, which improves matching and IL at higher frequencies (as depicted in Figure 26). The switch has perfect matching at DC, assuming all the ports are terminated with 50Ω resistances. The matching network introduces a notch in the S_{11} response. The location of the notch depends on the values of L_x and C_x , and it was placed such that the S_{11} stays below the required value throughout the desired range of frequencies. To maximize the matching bandwidth, the π -network was made symmetrical by setting $C_x = C_p = 33$ fF. The value of the inductor (L_x) was computed to be 198 pH based on the cut-off frequency ($1/(2\pi \sqrt{L_x C_x})$), and the location of the notch in the S_{11} response.

The π -matching network displays superior S_{11} , when compared to inductive peaking

in terms of improving matching bandwidth as shown in Figure 27. Inductive peaking is primarily used to reduce loss at high frequencies. Using a single inductor it is not possible to provide good matching (> 10 dB) at any frequency other than DC. The π -matching, on the other hand, can be designed to provide an exact match to 50Ω at a higher frequency in addition to DC, thus improving the matching bandwidth of the switch significantly.

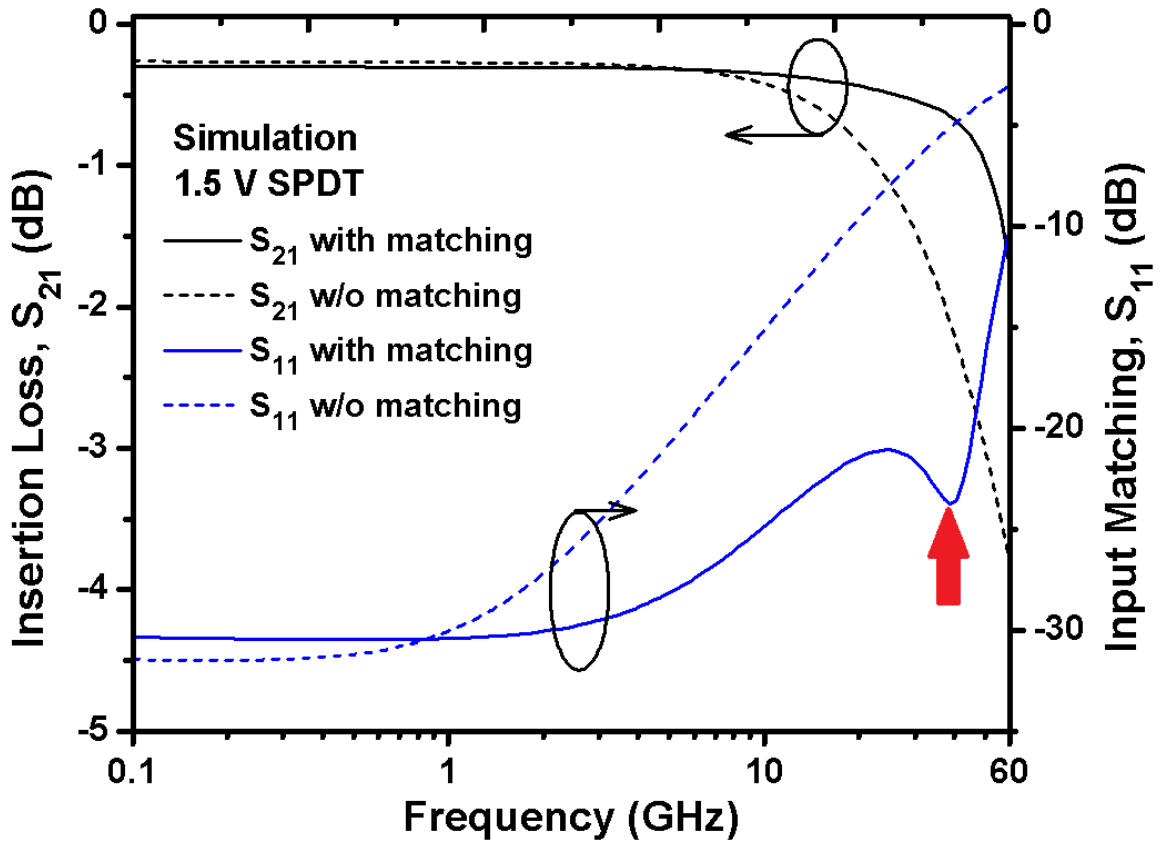


Figure 26. Simulation results showing effects of matching network on the IL (S_{21}) and the input matching S_{11} . The arrow indicates the notch due to input matching.

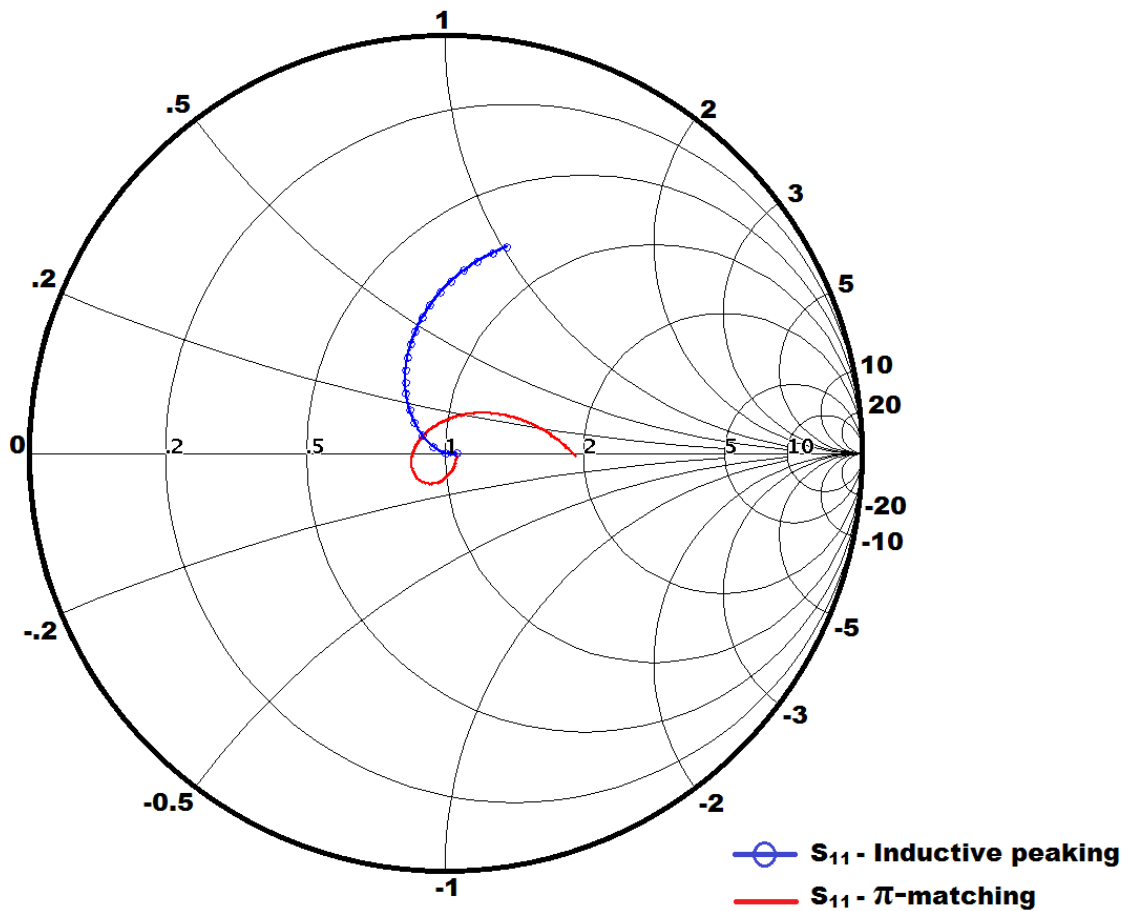


Figure 27. Smith chart showing the simulation results of S_{11} for inductive-peaking (blue curve) and π -matching network (red curve).

The input-referred large-signal linearity (P_{1dB}) of this series-shunt topology is limited by the shunt devices under negative voltage swing [64]. The simulated P_{1dB} of the 1.5 V switch is 12 dBm, while the measured value is 11 dBm. The signal handling capacity can be improved by using higher-voltage FETs, at the cost of degraded IL and reduced bandwidth. Additionally, the P_{1dB} of this switch topology can be changed simply by changing the DC bias of the RF signal. As illustrated in Figure 28, increasing the DC bias improves P_{1dB} up to a certain level, with a corresponding increase in IL. This technique reveals that the DC bias can be used as a tuning knob to change the performance of the switch post-fabrication. Reconfigurable, adaptive or self-healing systems [18] can make use of such

low-loss adaptive switches. For example, when used as a T/R switch, the nominal low-loss bias setting can be used in receive mode and a high- P_{1dB} setting can be turned on in transmit mode, enabling much greater design flexibility.

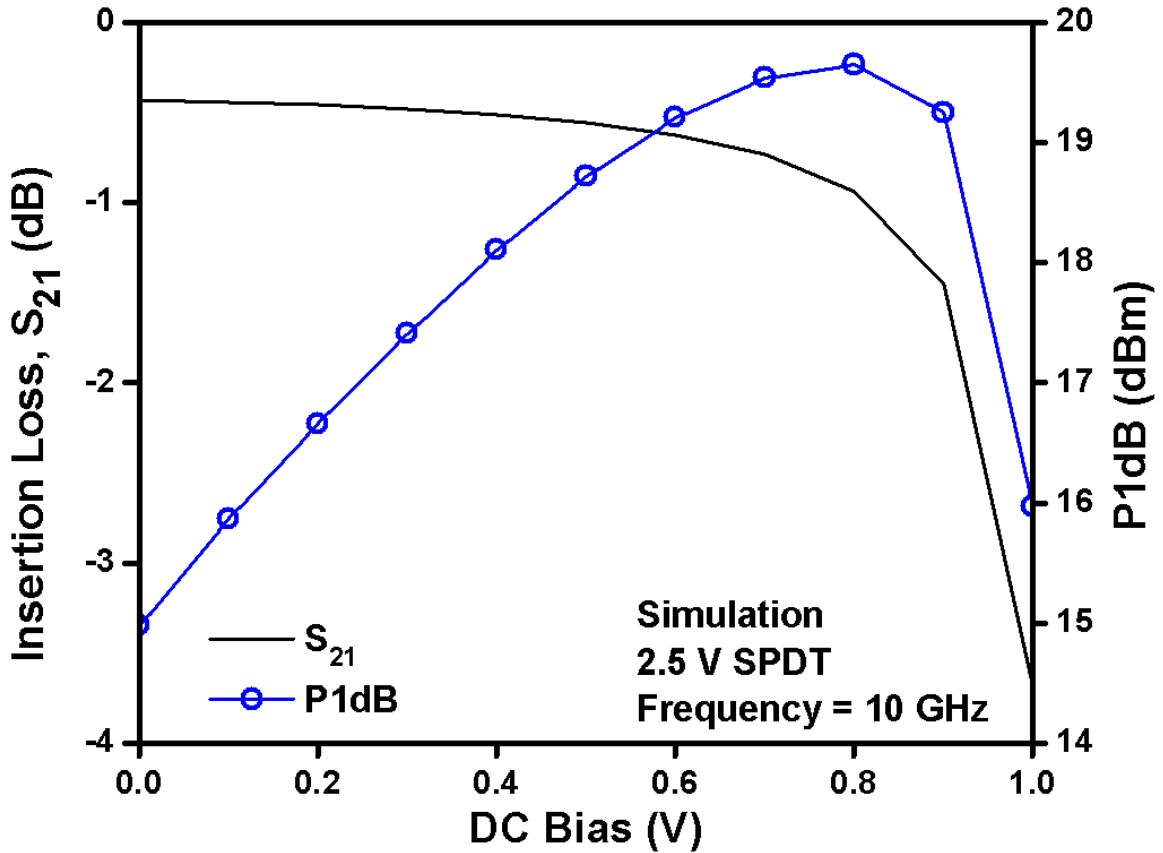


Figure 28. Simulation results showing effects of DC bias variation on IL and large signal linearity, P_{1dB} .

4.2 Results Discussion

The switches were fabricated in a commercially-available twin-well CMOS on SOI process (IBM 7RF-SOI) on a high-resistivity ($\approx 1000 \Omega\text{-cm}$) SOI substrate with 3 metal layers. The core of the chip measures $0.28 \times 0.09 \text{ mm}^2$. The S-parameters of the switches were measured using a VNA and de-embedded using open-short structures on-wafer. Measured data of the switches under nominal conditions are plotted in Figures 29 and 30. The IL of the 1.5 V switch is less than 0.5 dB up to 20 GHz and below 2.0 dB at 40 GHz. To the best of the author’s knowledge, this is one of the best reported loss performance for any

wide-band CMOS switch in this range of frequencies at this technology node. The input matching is better than 10 dB and the ISO between the input and output ports is > 15 dB. These switches consume negligible *dc* power (< 7 nW).

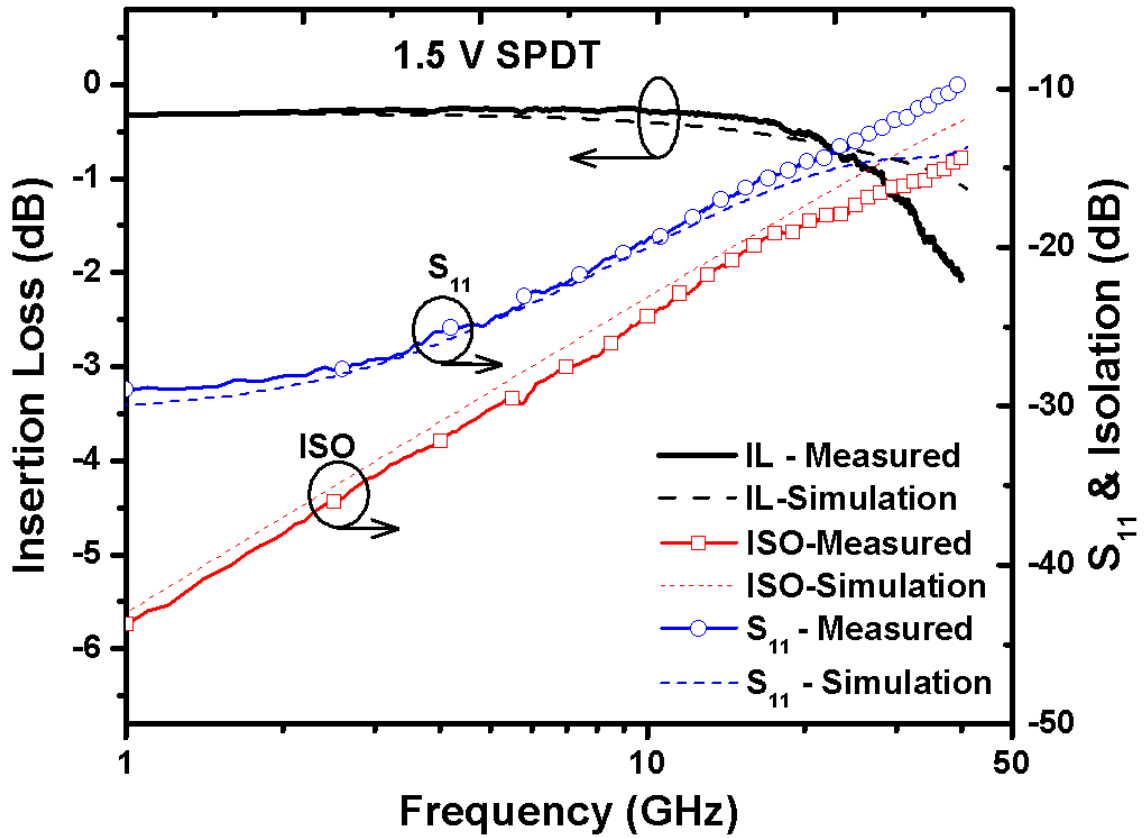


Figure 29. Measured (solid lines) and simulated (dashed lines) S-parameters of the 1.5 V SPDT RF switch.

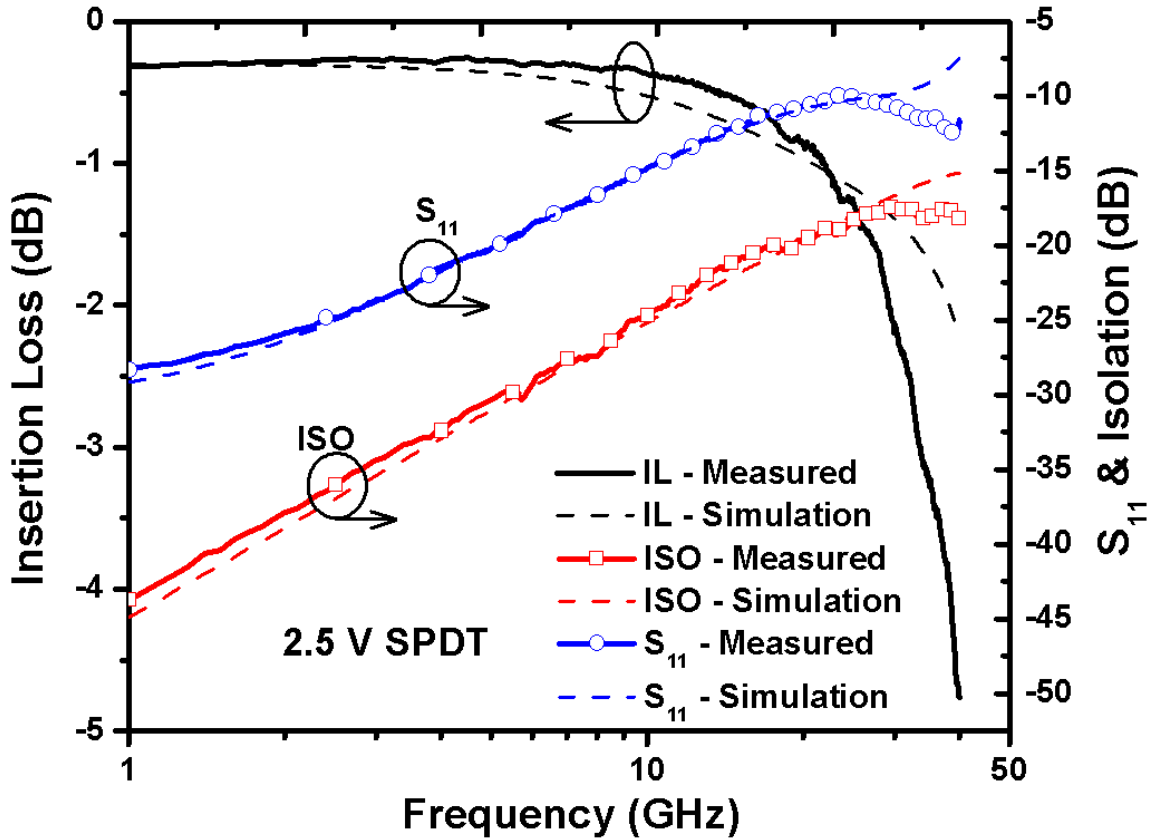


Figure 30. Measured (solid lines) and simulated (dashed lines) S-parameters of the 2.5 V SPDT RF switch.

These SPDT RF switches are compared with other published data in Table 1. Some of the prior works employ additional techniques to improve certain performance metrics. For example, [68] uses a negative body bias to improve P_{1dB} , which will require an additional dc power supply for operation. [64] uses LC resonance and the reported values are valid only at a single frequency, 35 GHz. Although the switch reported by [63] demonstrates lower IL at 40 GHz (< 1.6 dB in comparison to < 2.0 dB) the present design has higher power handling (9.6 dBm at 40 GHz). The switch presented here was designed in a higher lithography node (180 nm), and the design can be migrated to SiGe BiCMOS processes. This higher lithography node would allow leveraging the enhanced analog and RF performance of SiGe HBTs for a variety of mixed-signal extreme environment applications (e.g., space exploration systems) [8].

Table 1. Performance comparison of different SPDT switches

Ref.	BW (GHz)	IL (dB)		ISO (dB)	P_{1dB} (dBm)	Technology	
		DC-20 GHz	20-40 GHz				
[6]	DC-60	<1.25	<1.6	>20	2	45 nm CMOS	
[8]	DC-60	<2.5	<3.0	>48	17	90 nm CMOS	
[2]	26-40	N/A	2.6	27	12	130 nm CMOS	
[4]	DC-20	<2.0	N/A	>15	N/A	130 nm SiGe BiCMOS	
[3]	DC-50	<3.0	<4.0	>30	19.6	180 nm CMOS	
This work	1.5 V	DC-40	<0.5	<2.0	>15	11	180 nm SOI CMOS
	2.5 V	DC-40	<1.0	<5.0	>17	15	180 nm SOI CMOS

To demonstrate the capabilities of this switch, a one-bit, 180° switched-line PS was designed at 18 GHz using the 1.5 V low IL switch. The measured IL and S_{11} results are plotted in Figure 31, while the resultant phase difference is shown in the inset graph of Figure 31. As a result of using the high-performance switches, the PS exhibits an IL better than 3 dB, S_{11} of 16 dB, and a 180° phase shift at 18 GHz. The PS photomicrograph is shown in Figure 32.

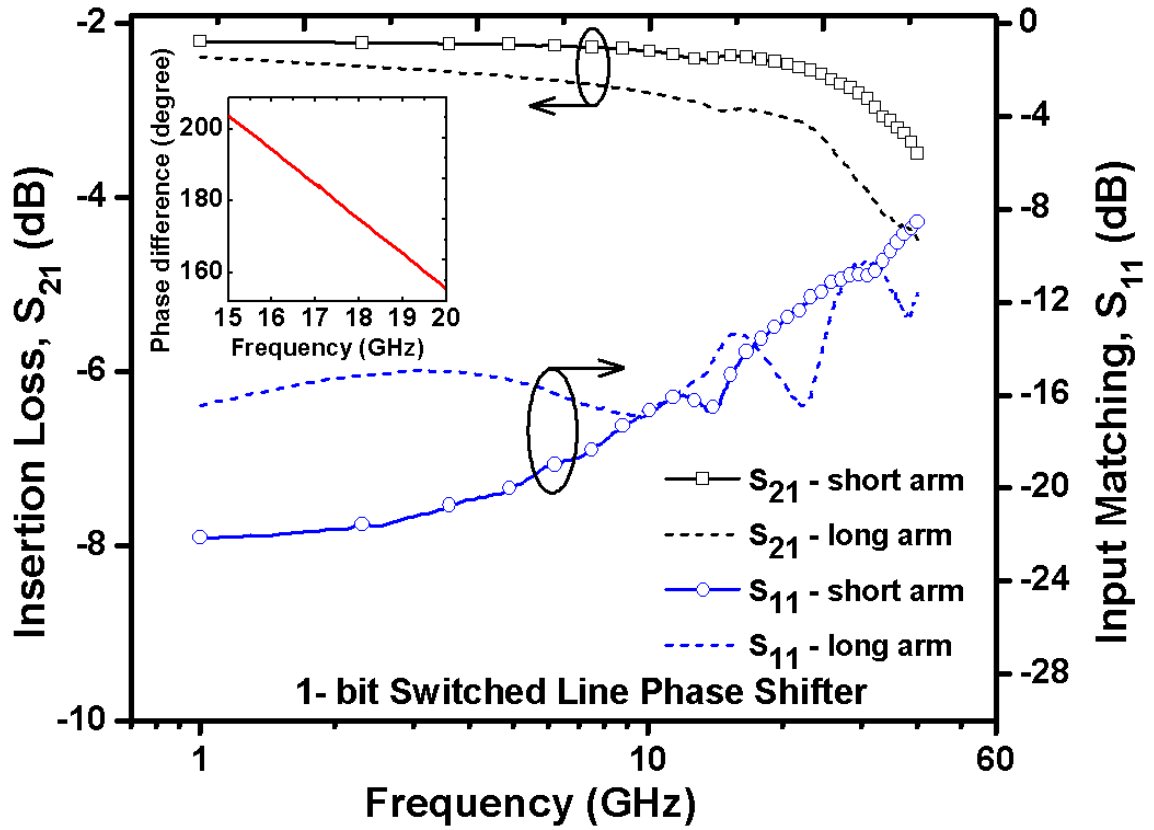


Figure 31. Measured S-parameters of the one-bit switched-line 180° phase-shifter (PS) using the 1.5 V switches. The inset graph shows the phase difference.

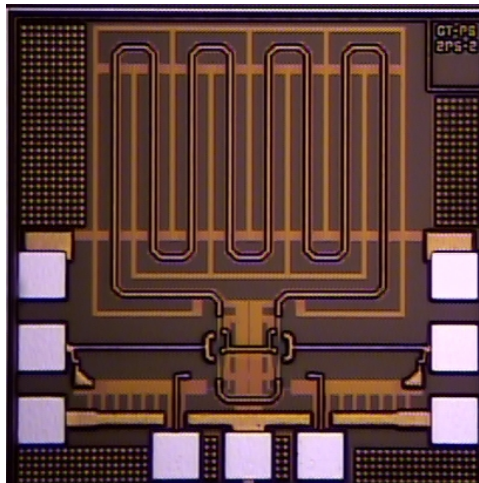


Figure 32. Die photograph of the switched-line phase shifter.

4.3 Summary

In this chapter, the design of two low-loss SPDT RF switches and a one-bit 180° switched-line PS fabricated in a 180 nm CMOS on SOI technology was presented. A π -matching network was used to extend the bandwidth and reduce IL. It was demonstrated that P_{1dB} can be improved using different biasing schemes. The switches combine best-in-class IL performance, good input matching, moderate ISO and linearity, while using the most conservative lithography node reported to date.

CHAPTER 5

ON THE CRYOGENIC PERFORMANCE OF SPDT RF SWITCHES DESIGNED IN AN SOI-CMOS TECHNOLOGY

RF switches are used in a wide variety of space-based electronic systems (e.g., satellites, deep-space remote sensing electronics, and spacecraft navigation systems) [3]. Therefore, it is important to investigate and understand the operational integrity of the RF switches while operating in extreme environments where radiation and cryogenic temperatures are commonplace. This information will provide mission architects and circuit designers with a better understanding of how system operation can be influenced by cryogenic temperatures, and more importantly, how to potentially leverage the circuit response for cryogenic operation.

This chapter presents the first full RF characterization of the FET-based SPDT switch at cryogenic temperatures. The switch has the lowest reported insertion loss (<1.25 dB at 40 GHz) on a silicon-based technology operating at 78 K. Although [63] has reported a comparable IL at 296 K (room temperature), that SPDT was designed in a 45 nm SOI CMOS technology. The radiation robustness of these switches are presented in Chapter 7.

5.1 Switch Design

A brief description of the switch design are included here to provide insight into the cryogenic performance. The switch circuits were designed and fabricated in a commercially-available 180 nm twin-well SOI CMOS (IBM 7RF-SOI) process on high-resistivity ($\approx 1000 \Omega\text{-cm}$) substrate with 3 metal layers [5]. The detailed design and RF performance of the SPDT at ambient temperature (≈ 300 K) is presented in Chapter 4 (only results at room temperature were discussed). As discussed previously, a π -matching network consisting of series inductor (L_X), shunt capacitor (C_X), and the parasitic capacitance (C_P) from M_1 and M_2 (denoted as C_P in Figure 33) was realized to improve the SPDT input matching and IL

at higher frequencies.

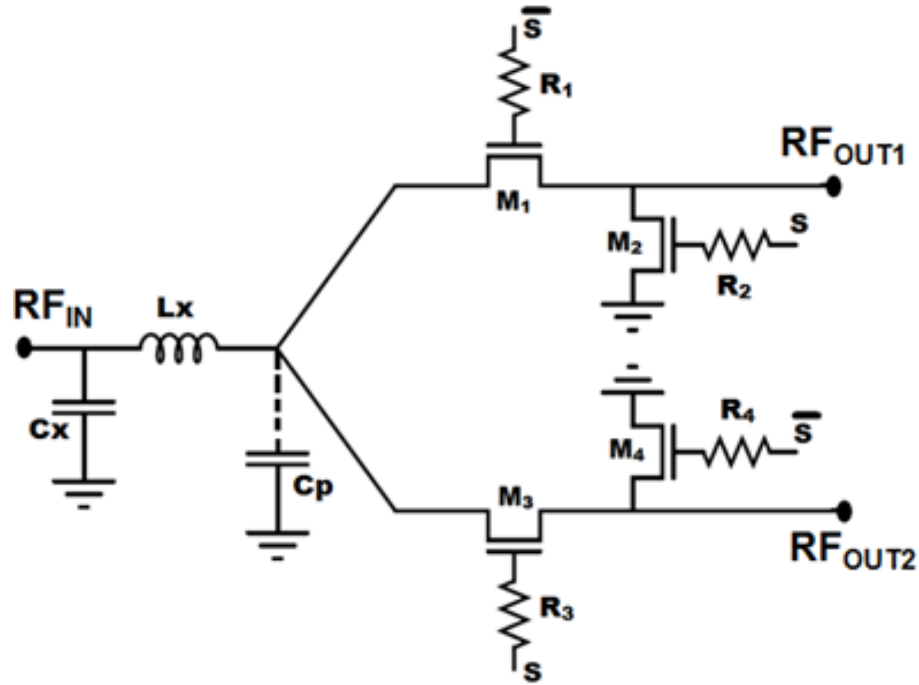


Figure 33. (a) Schematic diagram of the 7RF SPDT switch circuit.

5.2 Measured Results and Analysis

As illustrated in Figure 34, the switch IL (on-state) improves with decreasing temperature; <1.25 dB at 78 K, 1.73 dB at 150 K, and 2.25 dB at 300 K over the bandwidth of 40 GHz. The IL is <0.13 dB from DC to 20 GHz at 78 K. These are significant results, since the IL is typically the primary specification for applications, as it can impact the overall system performance. The reduction in IL can be explained by the extracted ON-resistance (R_{ON}) and carrier mobility (μ_e) results shown in Figures 35(a) and 35(b), respectively. As temperature is reduced, the R_{ON} decreases due to an increase in μ_e . The R_{ON} and the μ_e parameters were extracted over temperature from dc measurements using similar sized devices as in the SPDT.

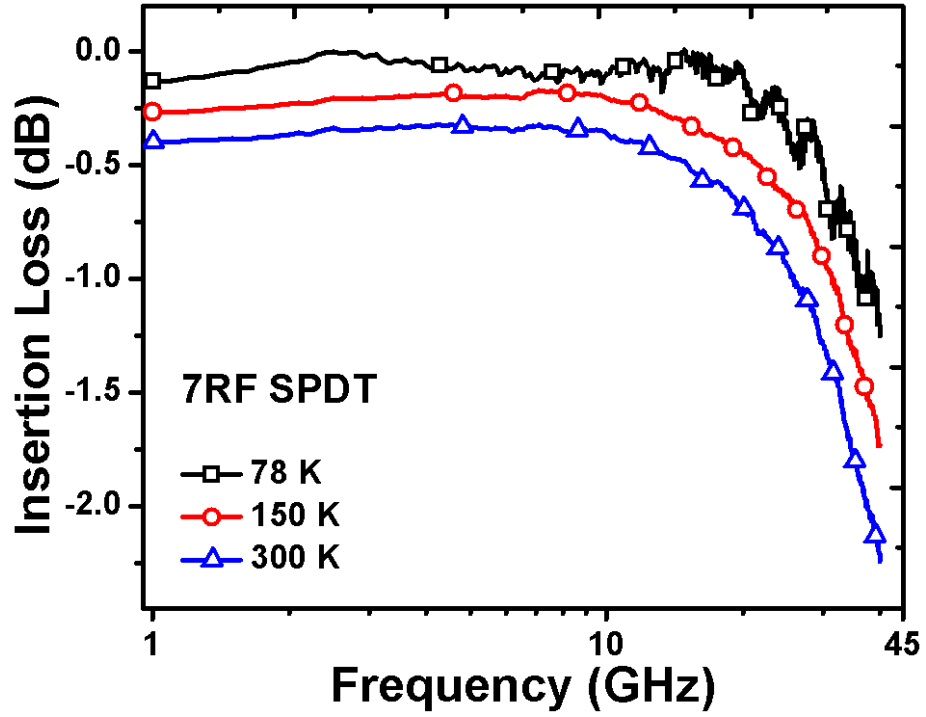


Figure 34. Measured insertion loss for SPDT at 300 K (blue triangle), 150 K (red circle), and 78 K (black square) traces.

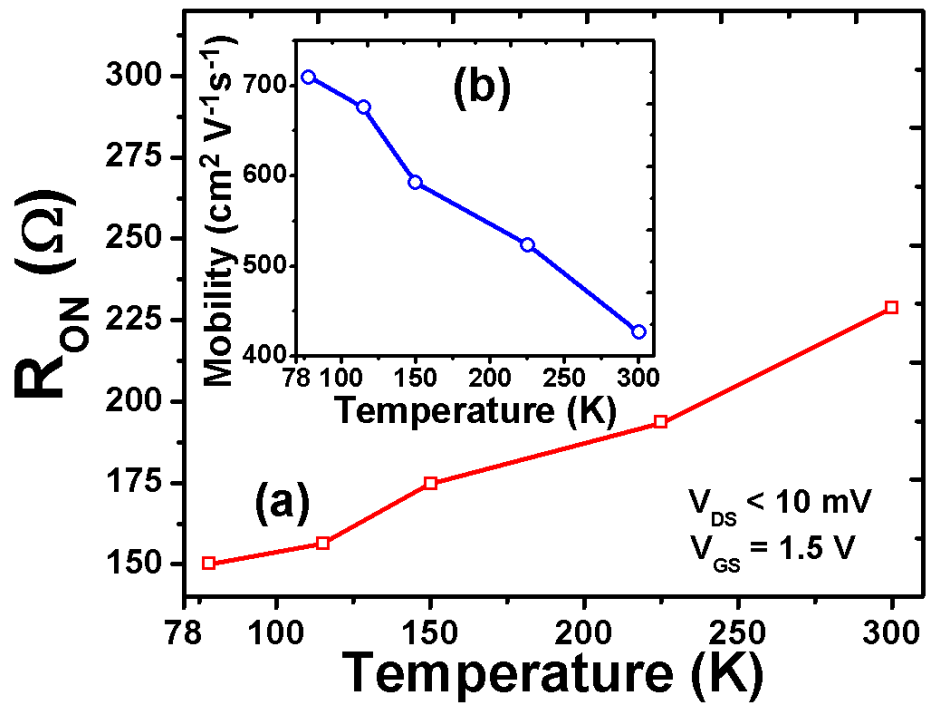


Figure 35. (a) Extracted ON-resistance (R_{ON}) and (b) Mobility as a function of temperature.

Figure 36 depicts the measured ISO (off-state) at various temperature points. The isolation (ISO) results follow a similar trend as the IL. The switch ISO improves (i.e., its magnitude increases) with decreasing temperature. A larger ISO improvement is observed at lower frequencies, from DC to 20 GHz (≈ 4.5 dB difference between 300 K and 78 K). At 20 GHz and above, the ISO enhancement is only ≈ 1.8 dB. The ISO does not continue to improve at high frequencies because the parasitic capacitances of the OFF devices (e.g., when RF_{OUT1} is enabled, M_1 and M_4 are ON while M_2 and M_3 are OFF) begin to oppose and cancel out the added benefit of cooling (reduction in IL) from the devices that are ON. The ISO improvement with decreased temperature is most likely due to a decrease in the parasitic source-drain junction capacitances as temperature is lowered. However, at higher frequency the ISO degrades due to the increased parasitic coupling to the substrate [69].

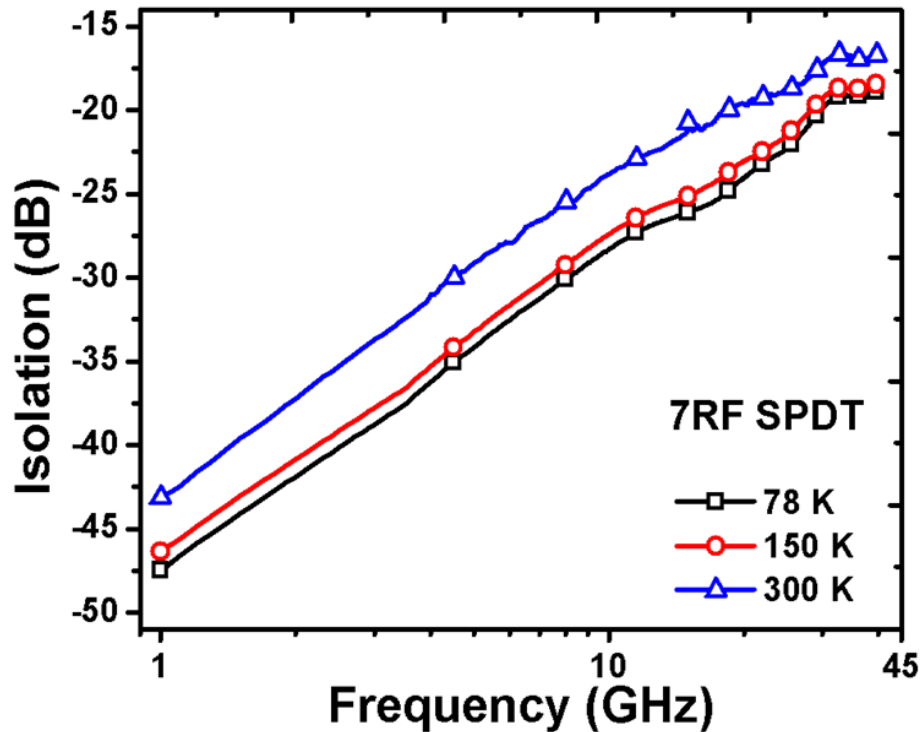


Figure 36. Measured ISO for SPDT at 300 K (blue triangle), 150 K (red circle), and 78 K (black square) traces.

The measured input and output reflection coefficients, S_{11} and S_{22} are shown in Figures 37(a) and (b), respectively. Below 10 GHz, the worst-case variation is about 5 dB from

300 K to 78 K. Since the S_{11} and S_{22} values are high (>20 dB) the temperature-induced variations do not impact the overall switch performance. At high frequencies (>10 GHz) the influence of temperature on S_{11} and S_{22} is small, and no discernable trend is observed. As anticipated, the S_{11} results demonstrate that the designed π -matching network is not too sensitive to temperature changes.

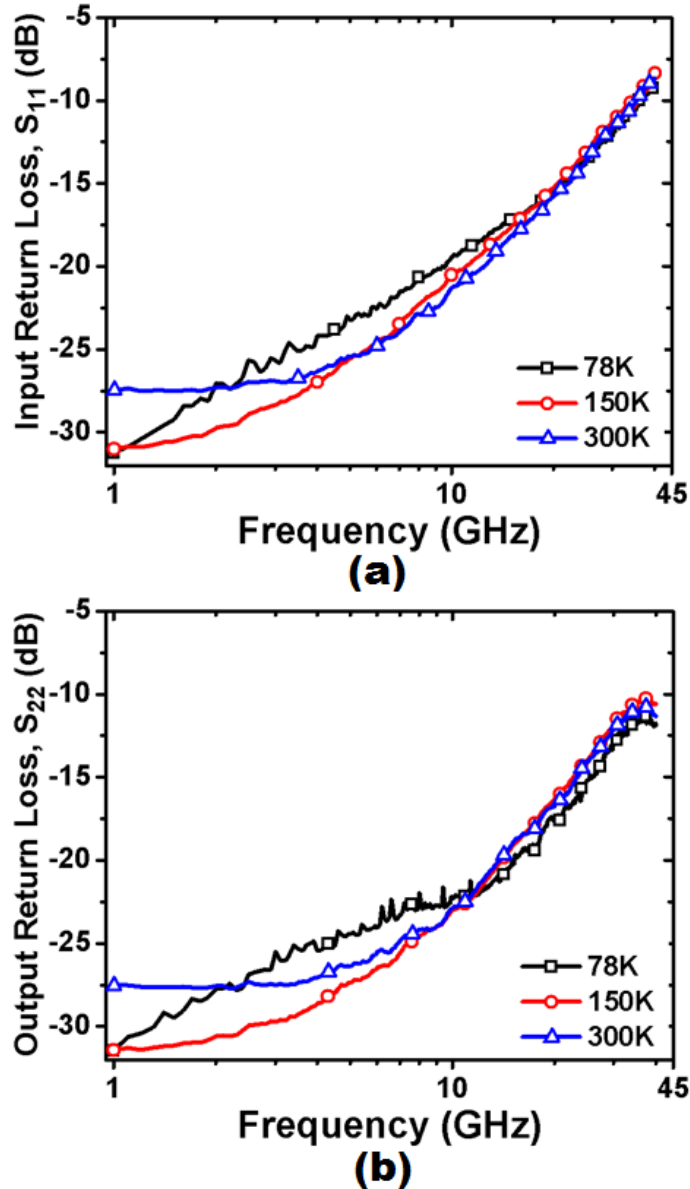


Figure 37. (a) Measured SPDT input return loss, S_{11} and (b) Output return loss, S_{22} at 300 K (blue triangle), 150 K (red circle), and 78 K (black square) traces.

The power handling capability of the SPDT was also characterized over temperature. The output power (P_{OUT}) and IL (S_{21}) as the input power is swept at a fixed frequency (8 GHz) is shown in Figure 38. The large-signal linearity, P1dB (input-referred) was extracted from Figure 38 results. The measured Large-signal linearity (P_{1dB} in blue square) and small-signal linearity, IIP3 (black triangle) and OIP3 (red circle) are plotted as a function of temperature in Figure 39. As temperature decreases, the P_{1dB} improves from ≈ 11 dBm at 300 K to ≈ 12.6 dBm at 78 K (as shown in Figure 39). Small-signal linearity measurements were performed using two-tone RF signals at 8 GHz with a 10 MHz frequency spacing. The third-order intercept points (TOI) IIP3 and OIP3 were extracted, and as expected, the results follow the same trend as P1dB; both IIP3 and OIP3 increase with decreasing temperature.

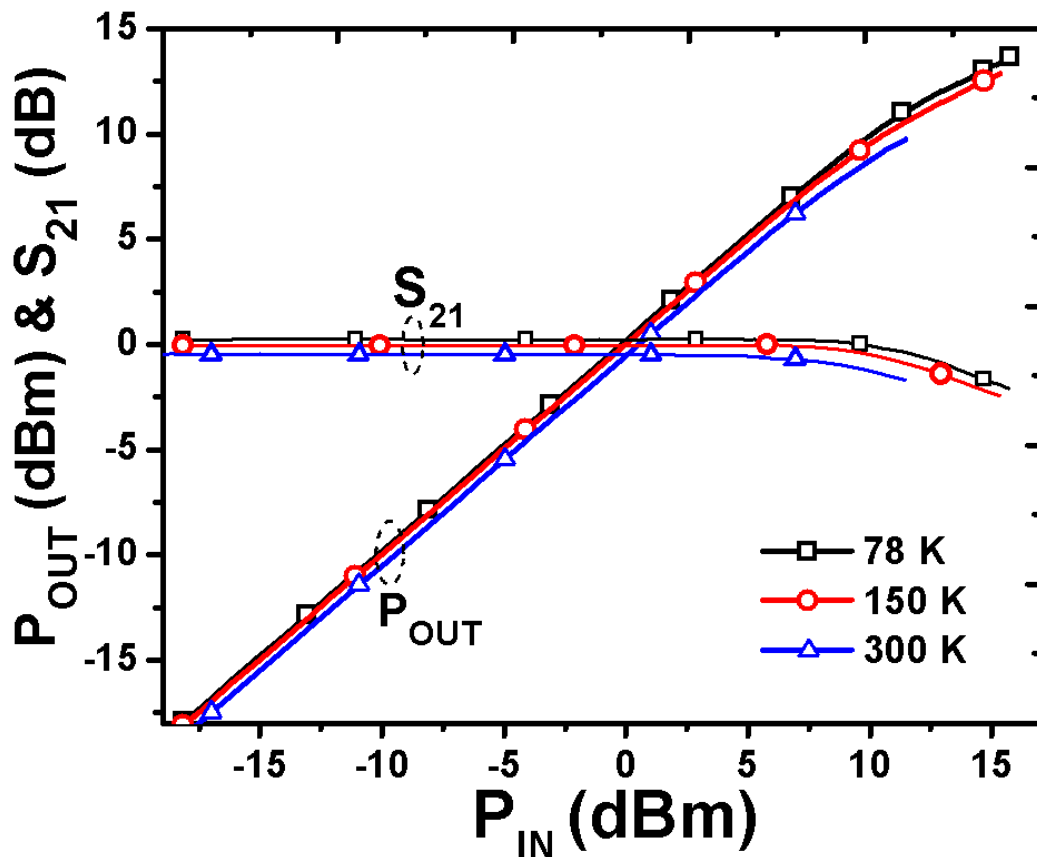


Figure 38. Measured SPDT output power (P_{OUT}) and insertion loss (S_{21}) as a function of input power (P_{IN}) at 300 K (blue triangle), 150 K (red circle), and 78 K (black square) traces.

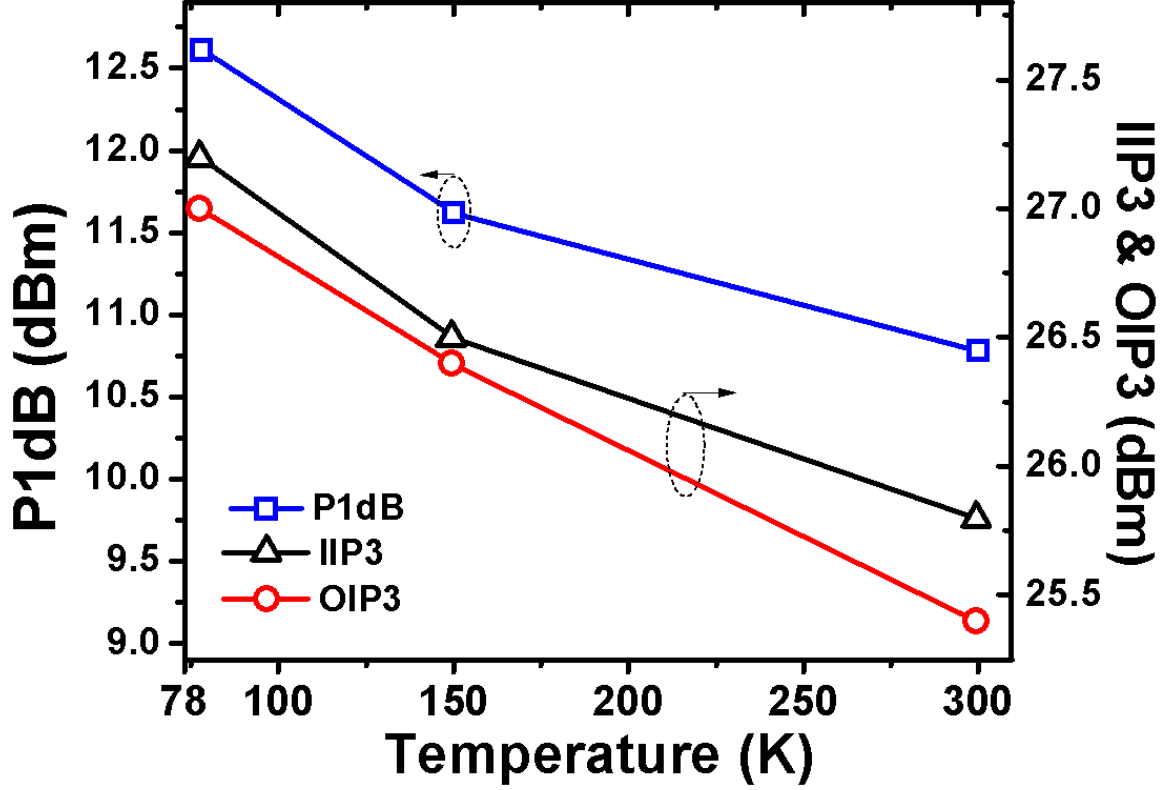


Figure 39. Large-signal linearity (P_{1dB} in blue square) and small-signal linearity, IIP3 (black triangle) and OIP3 (red circle) as a function of temperature.

This observed improvement in linearity is due to the increase in μ_e (as shown in 35(b)). The P1dB and TOI expressions for FET (previously derived in [70]) confirm that the observed improvement in both large- and small-signal linearity is due to the increase in μ_e as temperature decreases. In equations 8 and 9 the parameter “ v_{sat} ” represents the saturation velocity, “ L ” the transistor gate length, “ R_s ” the input impedance, and “ μ_1 ” is the effective carrier mobility. In equations 10 and 11, μ_0 is the low-field mobility and θ is the mobility degradation factor due to the applied perpendicular electric field [70].

$$P_{1dB} = \frac{1 + \left(\frac{\mu_1 V_{od}}{2v_{sat}L}\right)^4}{2R_s \left(\frac{\mu_1}{2v_{sat}L}\right)^2 \left[V_{od} \left(1 + \frac{\mu_1 V_{od}}{4v_{sat}L}\right) + \frac{6.88v_{sat}L}{\mu_1 \left(1 + \frac{\mu_1 V_{od}}{2v_{sat}L}\right)^2} \right]} \quad (8)$$

$$IIP3 = \frac{8v_{sat}L}{3\mu_1 R_s} V_{od} \left(1 + \frac{\mu_1 V_{od}}{4v_{sat}L}\right) \left(1 + \frac{\mu_1 V_{od}}{2v_{sat}L}\right)^2 \quad (9)$$

where

$$\mu_1 = \mu_0 + 2\theta v_{sat}L \quad (10)$$

$$V_{od} = V_{GS} - V_{TH} \quad (11)$$

5.3 Summary

The RF performance of SPDT switches designed in a 180 nm SOI-CMOS technology has been demonstrated at cryogenic temperatures. All key performance metrics like insertion loss (IL), isolation (ISO), large- and small-signal linearity improve with decreasing temperature. For this technology, operation of the SPDT at low temperatures can be leveraged to meet challenging system requirements, particularly for applications that require low-loss switches operating in cryogenic environments. dc characterization of individual transistors reveal that the increase in mobility is the key contributor for the RF performance improvement at cryogenic temperatures.

CHAPTER 6

TID RESPONSE OF FET-BASED HIGH-ISOLATION RF SWITCHES IN A 180-NM SiGe BICMOS TECHNOLOGY

SiGe BiCMOS technology platforms have proven to be strong candidates for many extreme environment applications (i.e., wide temperature range and radiation-tolerant electronics) [1]. Typical examples are satellites in geosynchronous orbit, where the electronics are constantly bombarded by a spectrum of energetic photons and particles. For electronic systems to reliably operate in such radiation-rich environment, each of their individual components and sub-blocks must be thoroughly characterized for robustness. The effects of radiation on MOS devices and circuits has been well documented, including numerous studies on total ionizing dose (TID) response of MOSFETs (bulk n-channel and p-channel transistors) [14, 23]. Recent studies have reported on the performance robustness of irradiated RF and mixed-signal circuits designed in SiGe BiCMOS technologies [37, 38]. However, both of these studies were primarily focused on SiGe HBT based circuits since the HBTs have been proven to be more TID tolerant than MOSFETs.

This work reports the effects of 63 MeV proton radiation on nFET-based SPST switches [7, 8]. Standalone transistors with sizes comparable to those used for the switch design were irradiated using ARACOR 10 keV X-ray source separately. From the ARACOR 10 keV X-ray measured results, the *dc* performance of stand-alone triple-well (TW) and bulk transistors were analyzed to provide insight into the underlying mechanisms that cause the observed changes in RF performance. This study is one of the first attempts to investigate the radiation robustness of a nFET based shunt-series-shunt-series type of single-pole single-throw (SPST) RF switch. The goal of this work is to investigate the effects of TID on the RF performance of switches implemented in a 130 nm (drawn length) SiGe BiCMOS technology [24]. The gate oxide thicknesses are approximately 4 nm for this technology (IBM 8HP).

6.1 Experiment Details

The RF samples were wire-bonded into dual in-line packages (DIPs) and irradiated using the 63.3 MeV proton facilities at the Crocker Nuclear Laboratory, University of California at Davis. The RF samples consisted of the SPST switches, and stand-alone bulk and TW nFET transistor structures. The stand-alone transistor test structures were of the similar dimensions and were configured similarly to the devices used in the SPST switches (e.g., 10 k Ω resistors connected to the gate, drain, and source). Table 2 lists the various SPST bias configurations used during irradiation. The TID radiation experiments were performed at room temperature under three bias conditions, as summarized in Table 2: (1) when the switch is “ON”, (2) when the switch is “OFF”, and (3) with all terminals grounded (as a control). The radiation source and dosimetry system have been previously described in [71] and have an error margin of about 10%. A total of nine RF samples were irradiated, three for each radiation dose level, 100 krad(*SiO*₂), 500 krad(*SiO*₂), and 2 Mrad(*SiO*₂). The average proton fluence attained during the experiment for each dose were, 7.40×10^{11} p/cm², 3.71×10^{12} p/cm², and 1.49×10^{13} p/cm², respectively. The bias configurations during irradiation for the stand-alone *dc* is also shown in Table 3.

Table 2. Bias configurations of the SPST circuit during irradiation

	Switch “ON”		Switch “OFF”		Switch “Grounded”	
	TW	Bulk	TW	Bulk	TW	Bulk
V_D (V)	1.2	1.2	1.2	1.2	0	0
V_S (V)	1.2	1.2	1.2	1.2	0	0
V_G (V)	2.4	1.2	1.2	2.4	0	0
V_{N-well} (V)	2.4	----	2.4	----	0	----
V_{P-well} (V)	0	0	0	0	0	0

Table 3. Bias configurations of the stand-alone *dc* samples during irradiation

	"Biased" <i>dc</i> Sample		"Grounded" <i>dc</i> Sample	
	TW	Bulk	TW	Bulk
V_D (V)	≈ 50 m	≈ 50 m	0	0
V_S (V)	0	0	0	0
V_G (V)	1.2	1.2	0	0
$V_{N\text{-Well}}$ (V)	1.2	---	0	0
$V_{P\text{-Well}}$ (V)	0	0	0	0

The on-wafer RF performance was measured at room-temperature for the pre- and post-irradiated samples using an Agilent E8363B Vector Network Analyzer (VNA) and Keithley 2400 *dc* power supplies for the bias voltages. The post-irradiation measurements were performed approximately 120 hours after the samples were irradiated because the packages were activated, and thus not safe to handle. However, there was no evidence of significant changes in the post-irradiation performance with the additional wait time. This assumption was verified by re-measuring the samples again after 240 hours. The margin of error in the S-Parameter measurement system was verified to be between 0.1 dB and 0.15 dB, for all the measured samples.

The switch design details and measured RF performance are presented in chapter 3.1. The SPST circuit schematic diagram is shown in Figure 40 to aid the discussion. The source and drain terminals of the FETs were biased using 10 k Ω resistors to enhance the switching linearity and minimize the *dc* power dissipation. The gates of the FETs were RF-floated using 10 k Ω resistors to improve the *dc* bias isolation and the device reliability [59]. Since the drains of the transistors were pulled up to 1.2 V, *dc* blocking capacitors " C_{BLK} " were used in series with the shunt transistors, M_1 and M_3 as shown in Figure 40. This blocking capacitor prevents *dc* current from flowing through the shunt arms when the FETs are turned on. The capacitors were sized to act as an electrical short for the RF signal over the desired operating frequency range.

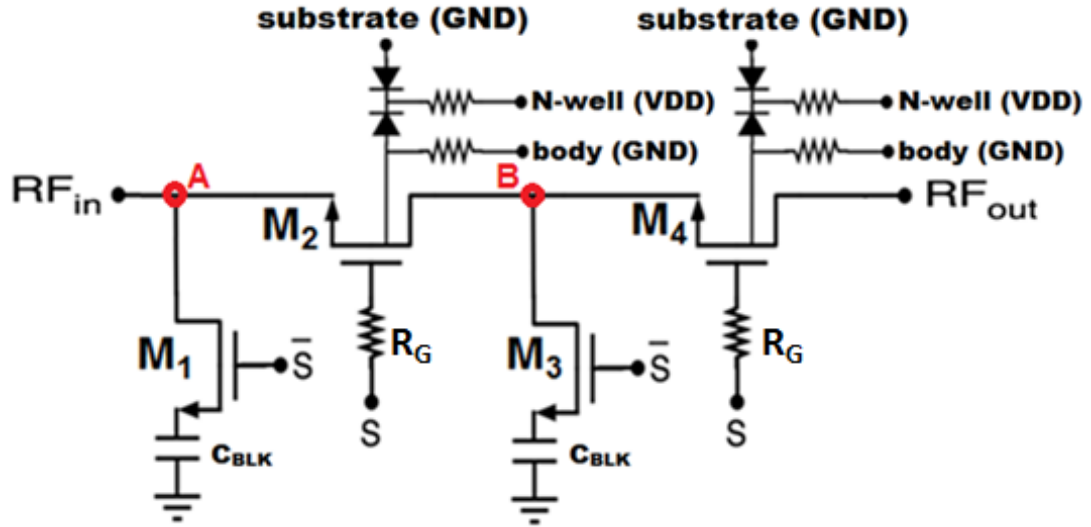


Figure 40. Single-pole single-throw (SPST) switch circuit schematic diagram.

A total of 6 *dc* samples were irradiated at room-temperature using an ARACOR 10 keV X-ray source at a dose rate of 31.5 krad(*SiO₂*/min) [35]. The *dc* devices structures were also wire-bonded into dual in-line packages. The biasing schemes utilized for the RF samples and the switch circuits were duplicated during X-ray exposure, as summarized in Table 3. The device dimensions were selected to be similar to the RF samples; the bulk nFET had a W/L of 10/0.12 (in μm), while the TW nFET had a W/L of 3/0.12 with 32 fingers. The *dc* characteristics of the devices were obtained before and after the radiation exposure at room temperature using an Agilent 4155 Semiconductor Parameter Analyzer. These *dc* samples were irradiated using the ARACOR 10 keV X-ray source instead of the 63.3 MeV proton source because of its availability and accessibility. For the RF and *dc* samples used in this work, 3 and 2 devices were tested under each irradiation condition, respectively. However for readability, the results and discussion only include data from a single device at each dose. The presented data was fully representative of the data set measured across all the samples.

6.2 Results and Discussion

The results of the samples irradiated under the (1) “Biased” conditions, and (2) “Grounded” irradiation results are presented in this section. The “Grounded” results provide a basis for comparison with the “Biased” results, and to help understand the observed bias dependence of the radiation-induced effects on the switch circuits. However, for brevity, only some of the relevant “Grounded” data are presented here.

6.2.1 Irradiated Results under “Biased” Conditions

The measured SPST switch IL response for the biased irradiation condition is depicted in Figure 41. The switch was biased in the “ON” state during irradiation. When the switch is “ON”, the series nFETs M_2 and M_4 are operating in the linear region, as V_{GS} is set to 1.2 V and V_{DS} is very low (< 50 mV) because both the source and drain terminals are pulled to the same potential through large resistors (Table 2). At the same time, the shunt transistors M_1 and M_3 are in the cut-off region, because their V_{GS} is set to 0 V. The IL (or S_{21}) improves by ≈ 0.8 dB for the 100 krad(SiO_2) and 500 krad(SiO_2) doses across the measured frequency band (1 to 50 GHz). However, the IL at the 2 Mrad(SiO_2) dose point degrades by ≈ 0.9 dB across the bandwidth.

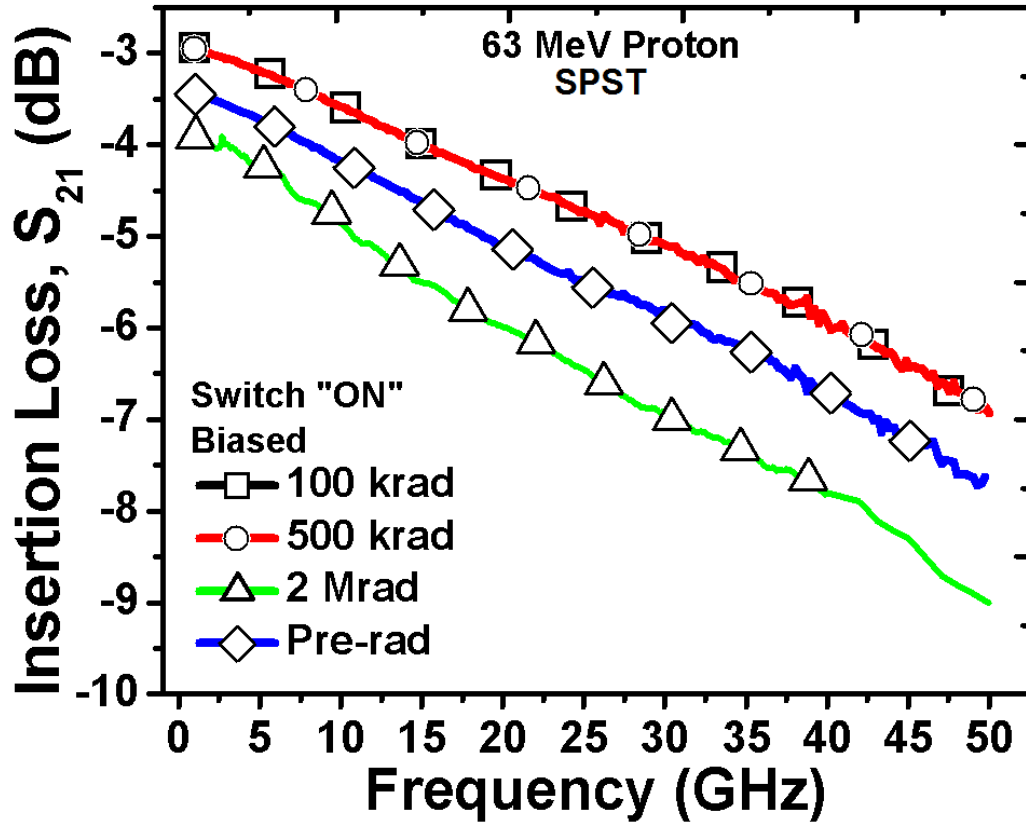


Figure 41. Comparison of the pre- and post-irradiated SPST IL, S_{21} when switch is “ON”. The switch was biased on-state during irradiation.

To gain insight into the above results and understand why the IL improves at low to medium dose, but degrades at a high dose, stand-alone RF and *dc* test structures were irradiated. Using the stand-alone device structures helps to decouple the potential radiation effects on the switch from the biasing circuitry. The results of the pre- and post-irradiated TW device IL, S_{21} is shown in Figure 42. These results follow a similar trend as the SPST switch in Figure 41 for 100 and 500 krad(SiO_2) doses. In comparison to the pre-radiation data, the IL improves by a maximum value of ≈ 0.4 dB between the three samples across the measured frequency bandwidth (1 to 50 GHz) for the 100 and 500 krad(SiO_2) doses, respectively. However, for the 2 Mrad(SiO_2), dose no significant degradation (S_{21} increase) was observed. This difference may be explained by examining the irradiated *dc* responses of the individual transistors.

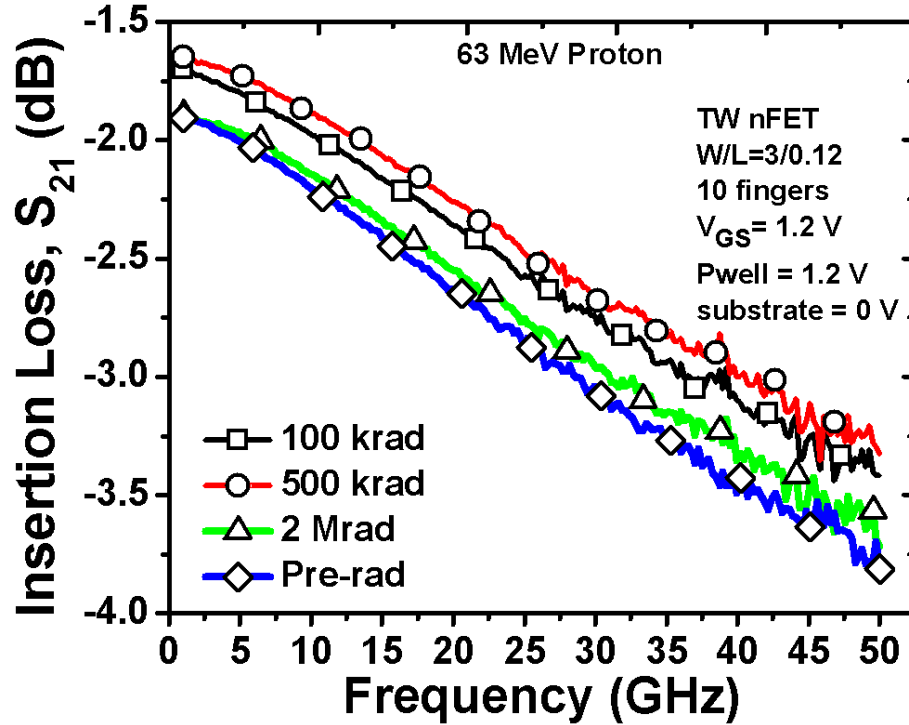


Figure 42. Comparison of the pre- and post-irradiated Triple-Well device IL, S_{21} . The device was biased on-state during irradiation as follows: $V_{GS} = 1.2$ V, $P_{well} = 1.2$ V, and substrate = 0 V.

The measured transfer characteristics of the TW and bulk nFETs irradiated at different total doses are illustrated in Figure 43 and Figure 44. The same bias conditions were used for the TW RF samples and the SPST switch (Table 2) during irradiation. As anticipated, the results show that for both transistors, TW and bulk, the V_{TH} shift and the subthreshold current leakage are more pronounced at 2 Mrad(SiO_2) dose when compared to other dose points. Prior works have shown that the radiation-induced positive trapped charge in the STI causes the parasitic sidewall conduction, which enables the leakage current to flow between the source and drain of the transistors, thus increasing the subthreshold current and decreasing the threshold voltage of the transistor [72]. At high radiation doses these increased leakage currents become important, and it is manifested by the M_1 and M_3 transistors on the SPST switch. The interdevice leakage paths degrade the ability of these transistors to provide a high impedance node to ground (nodes “A” and “B” as highlighted in Figure 40). Thus, some of the signal power is shunted to ground, increasing the overall

IL when the switch is “ON”.

In the context of IL, analyzing the linear region on-state current when the device is biased at V_{GS} of 1.2 V is relevant in understanding the TID response of the single device RF structures. The on-state current determines the transistor R_{ON} . Higher on-state current yields a lower R_{ON} , which translates to lower switch IL (S_{21} when switch is “ON”). The transfer characteristics for the TW device ($W/L = 1.0/0.12$, 32 fingers) is presented in the inset Figure 44, and it shows the current as a function of total dose near the device operating point. The improvement of the SPST switch and TW RF samples IL (implying decrease in S_{21}), can be attributed to the increase in the on-state current.

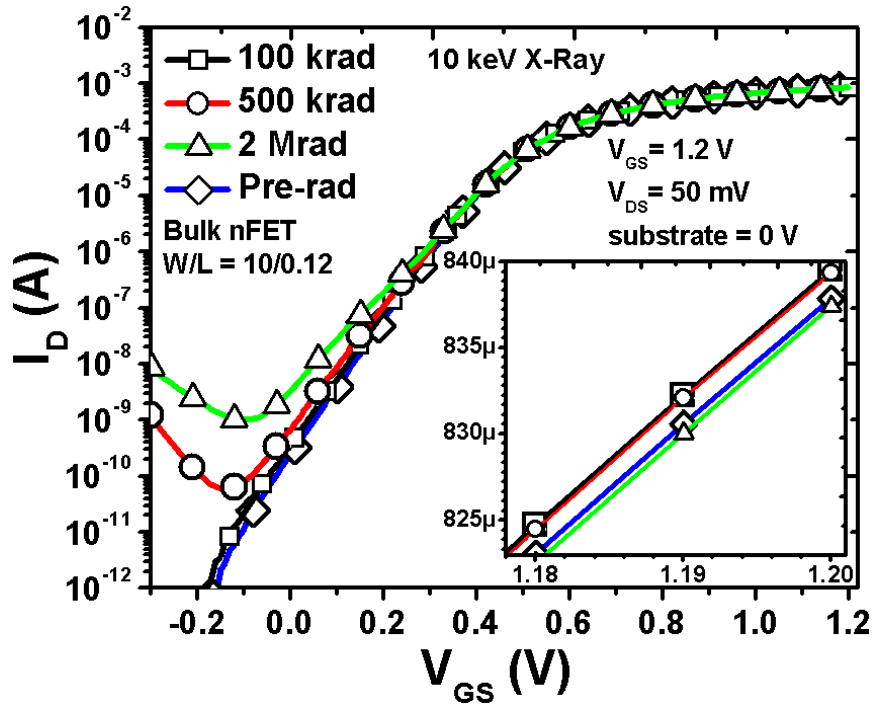


Figure 43. Pre- and post-irradiated $I_D - V_{GS}$ curves for Bulk device. The devices were biased during irradiation as follows: $V_{GS} = 1.2$ V, $V_{DS} = 50$ mV, and substrate = 0 V.

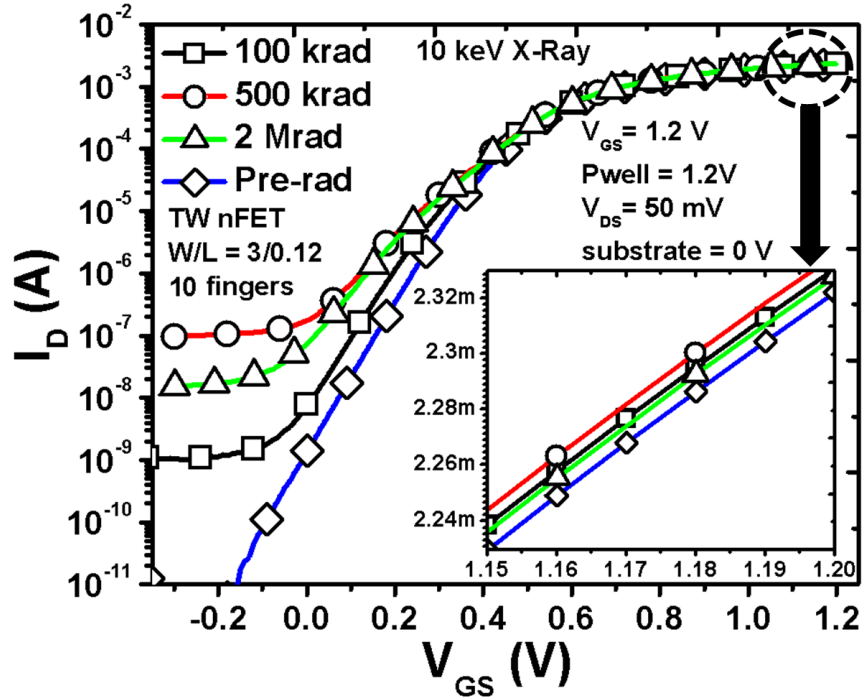


Figure 44. Pre- and post-radiated $I_D - V_{GS}$ curves for TW device. The devices were biased during irradiation as follows: $V_{GS} = 1.2$ V, $V_{DS} = 50$ mV, $P_{well} = 1.2$ V, and substrate = 0 V.

Previous works have shown that the increased subthreshold leakage in this technology is attributed to trapped charges in the STI oxide [72–74]. However, at high radiation dose, the subthreshold region *dc* response of the TW samples do not follow the typical bulk nFET trend of monotonically increasing drain-to-source leakage current with total dose, as reported in [75]. For these samples the leakage current increases from its pre-radiation value to 100 krad(SiO_2) and further for the 500 krad(SiO_2) samples, but it then decreases for the 2 Mrad(SiO_2) dose. This phenomenon was also observed in bulk devices fabricated in a 0.18 μm commercial CMOS process in [76]. The leakage current decrease at high radiation doses (2 Mrad(SiO_2) here) was attributed to an increase of negatively charged interface traps at the silicon/STI interfaces. This trend increasingly compensates for the initial positive charges trapped in the STI field oxide at lower radiation doses, thus effectively decreasing the total leakage current [76]. This compensating effect was also reported by [74], and was attributed to the fact that the formation of negatively charged interface

states is a much slower process in comparison to the trapped positive charge buildup in the STI oxide [77].

As emphasized previously, the switch isolation (S_{21} when the switch is “OFF”) is a key design specification. Typically the isolation degrades (S_{21} increases) as frequency increases, due to the increased parasitic coupling to the substrate [59]. The SPST measured isolation as a function of total dose is shown in Figure 45, and these results follow the same trend as the IL. For the 100 krad(SiO_2) dose, the isolation does not show any degradation in comparison to the pre-rad data. However, the structures irradiated to 500 krad(SiO_2) and 2 Mrad(SiO_2) show significant degradation in isolation, approximately 4 dB and 10 dB at mid-band 5 to 30 GHz, respectively. Radiation-induced interdevice leakage paths are a possible reason for the observed deviations [72, 74]. The nodes that are particularly susceptible to leakage are nodes “A” and “B” as highlighted in Figure 40. This interdevice leakage may occur because the drains of M_1 and M_3 transistors are physically connected to the sources of M_2 and M_4 , respectively.

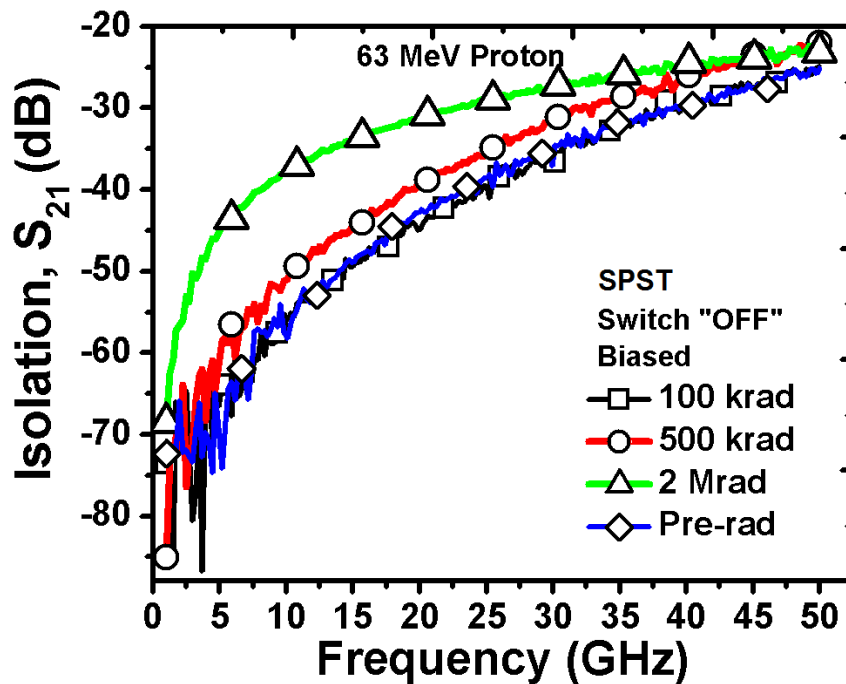


Figure 45. Comparison of the pre- and post-irradiated SPST ISO, S_{21} when switch is “OFF”. The switch was biased off-state during irradiation.

To better understand these results and eliminate the influence of the TW nFETs (M_2 and M_4) and bias circuitry, stand-alone RF nFET test structures were characterized and irradiated. The measured S_{21} results for these bulk test structures is depicted in Figure 46. The data follows a similar trend as the irradiated TW RF test structures shown in Figure 42. The S_{21} value in Figure 46 estimates the ability of the transistor to easily shunt the RF signal to ground. The lower this number is, the higher the switch isolation will be. As observed, the S_{21} improves slightly at 100 and 500 krad(SiO_2) doses (by ≈ 0.4 dB), but not as significantly for the sample irradiated up to 2 Mrad(SiO_2).

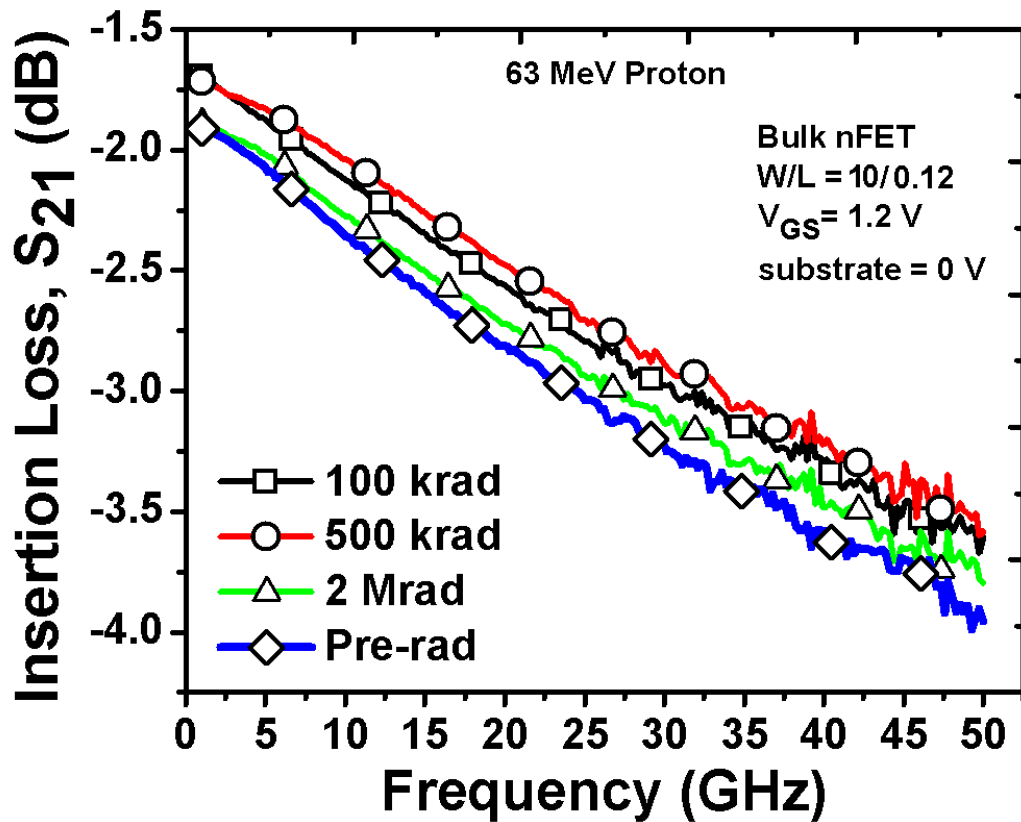


Figure 46. Comparison of the pre- and post-irradiated Bulk device IL, S_{21} . The devices were biased during irradiation as follows: $V_{GS} = 1.2$ V, $V_{DS} = 50$ mV, and substrate = 0 V.

Examining the transfer characteristics of the bulk nFET once again (Figure 43) provides further understanding on RF performance of the devices and circuits. The dc bulk device structures were biased with V_{GS} of 1.2 V, V_{DS} of 50 mV, and the substrate at 0 V. The inset

in Figure 43 shows how the current changes as a function of radiation near the transistor bias point ($V_{GS} = 1.2$ V). Similar to the TW devices, it was observed that an increase in drain-to-source current (approximately $1.5 \mu\text{A}$) at the same bias point for the 100 and 500 $\text{krad}(\text{SiO}_2)$ dose. For the 2 Mrad(SiO_2) sample, the measured current is approximately $0.5 \mu\text{A}$ lower. The decrease in on-state current along with radiation-induced leakage paths at 2 Mrad(SiO_2) dose cause the reduction in the switch isolation. In addition, the off-state current for the TW transistors M_2 and M_4 (seen in Figure 44) increases at 2 Mrad(SiO_2) dose. The off-state current increase is due to positive charges trapped in the STI oxide at the edges of the device width, producing an inversion layer in the p-type silicon between the source and drain, thus causing a shunt leakage current to flow [72, 74]. [76] provides an in-depth study of the contributions related to the oxide trapped charge and the interface traps in the STI.

The leakage paths can be caused by: (1) “drain-to-source leakage” in a single FET, (2) “interdevice leakage” [72]. The interdevice leakage is further subdivided into “drain-to-source” leakage between two different devices, and source-to-well leakage between two different devices. Interdevice leakage substantiates the reason why M_1 and M_3 transistors in the SPST circuit would be compromised, causing the IL to increase (Figure 41). Therefore, two effects couple to degrade the overall switch isolation, the on-state current reduction and the leakage paths in between devices.

The post-irradiation linearity of the SPST switch was measured at 16 GHz. The results for both small-signal, IIP3 and large-signal P_{1dB} as a function of the TID are shown in Figure 47. In comparison to the pre-irradiation data, the P_{1dB} improves by ≈ 0.4 dBm and ≈ 0.2 dBm at 100 and 500 $\text{krad}(\text{SiO}_2)$, respectively. The IIP3 results follows similar trend as P_{1dB} , improving by ≈ 1.9 dBm at 100 $\text{krad}(\text{SiO}_2)$ and ≈ 1.1 dBm at 500 $\text{krad}(\text{SiO}_2)$ dose. However, in comparison to the pre-rad data both small- and large-signal switch linearity at high dose, 2 Mrad(SiO_2), are severely degraded, by 5.6 dBm and 5.5 dBm, respectively. This reduction of the switch linearity is attributed to the radiation-induced leakage paths

in M_1 and M_3 transistors. In addition, the junction diodes of the bulk transistors, M_1 and M_3 , are the other major limiting factor determining the power handling capability of the SPST switch. These junction diodes can become forward-biased when the applied RF input voltage peak gets higher than ≈ 0.7 V [78]. As stated previously, at high radiation dose M_1 and M_3 transistors are compromised due to the radiation-induced leakage paths.

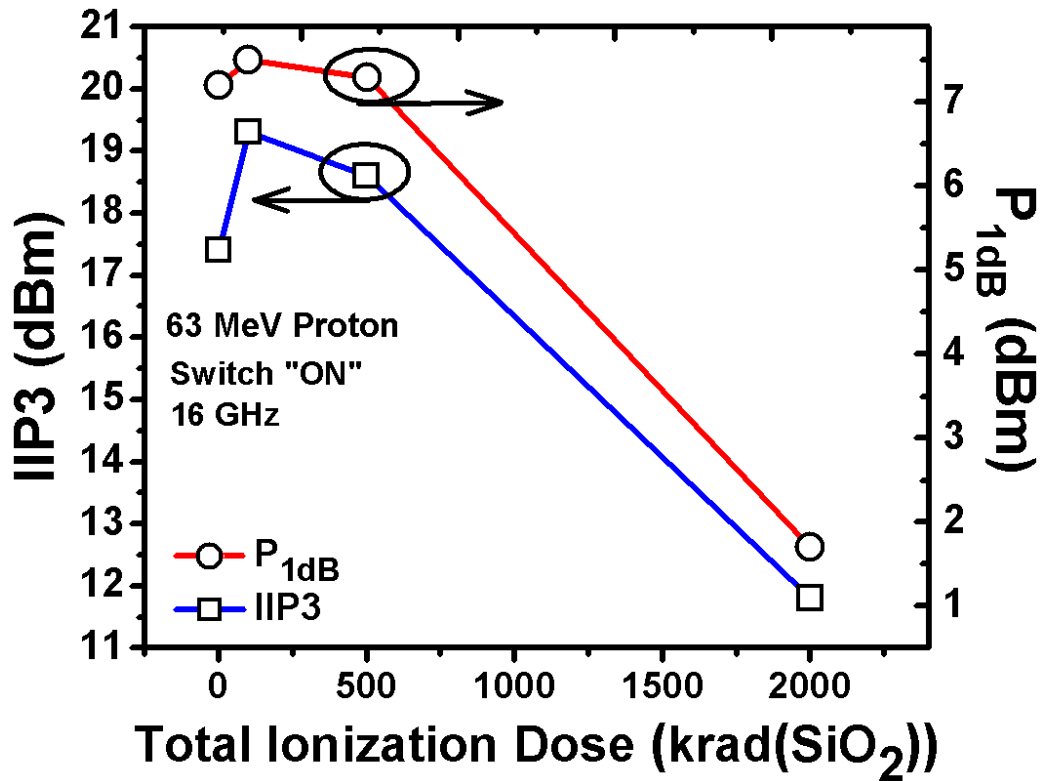


Figure 47. Pre- and post-irradiated SPST linearity (P_{1dB} and IIP3) performance as a function of radiation. The switch was biased on the on-state during irradiation.

6.2.2 Irradiated Results with all Terminals “Grounded”

Additional samples (including dc and RF samples) were irradiated with all terminals “Grounded” to further probe into the effects of bias on the RF performance of SPST switch. The measured SPST switch IL and ISO responses are illustrated in Figure 48 and Figure 49, respectively. The RF responses are clearly different than the “Biased” SPST results presented earlier (Figure 41 and Figure 45). As expected, for the “Grounded” samples, the IL responses do not significantly deviate from the pre-radiation result across the frequency

bandwidth (1 to 50 GHz) as the TID increases. The 2 Mrad(SiO_2) response shows a slight IL improvement (S_{21} decreases) in comparison to the pre-radiation data, ≈ 0.15 dB at 20 GHz. However, this difference is well within the measurement variability. To validate these results, bulk and TW RF samples were also irradiated, and their measured IL response are shown in Figures 50 and 51, respectively. As anticipated, the S_{21} responses for both RF samples are nearly identical, and no significant variation are observed when compared to the pre-radiation results.

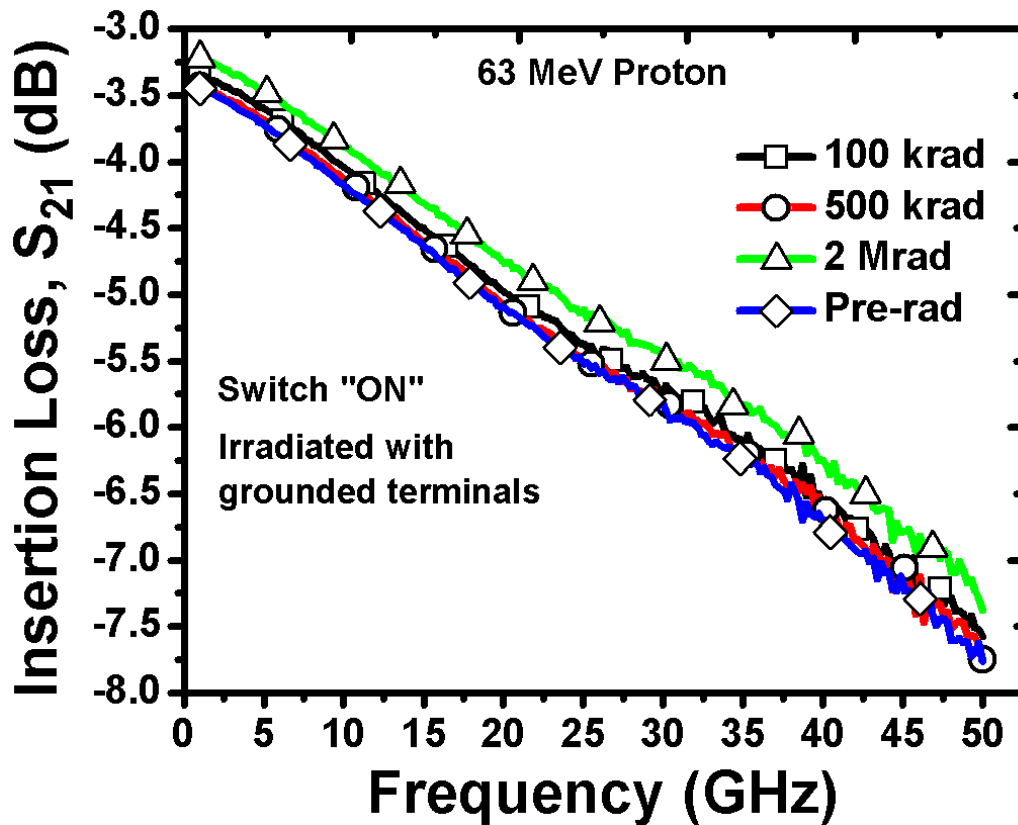


Figure 48. Comparison of the pre- and post-irradiated SPST IL, S_{21} when switch is "ON". All terminals grounded (0 V) during irradiation.

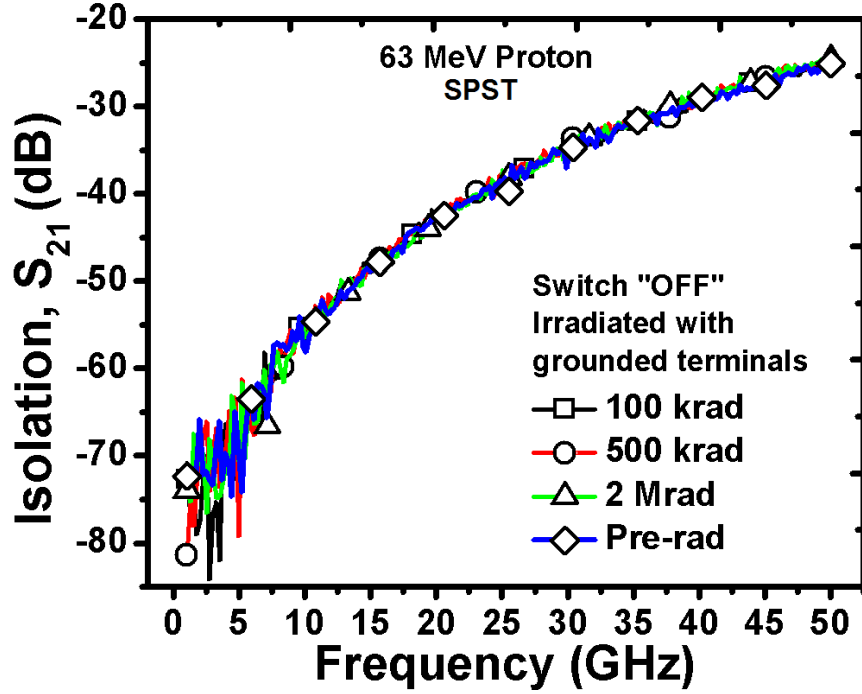


Figure 49. SPST isolation, S_{21} when switch is "OFF" response comparison between pre-, and post-irradiated data. All terminals grounded (0 V) during irradiation.

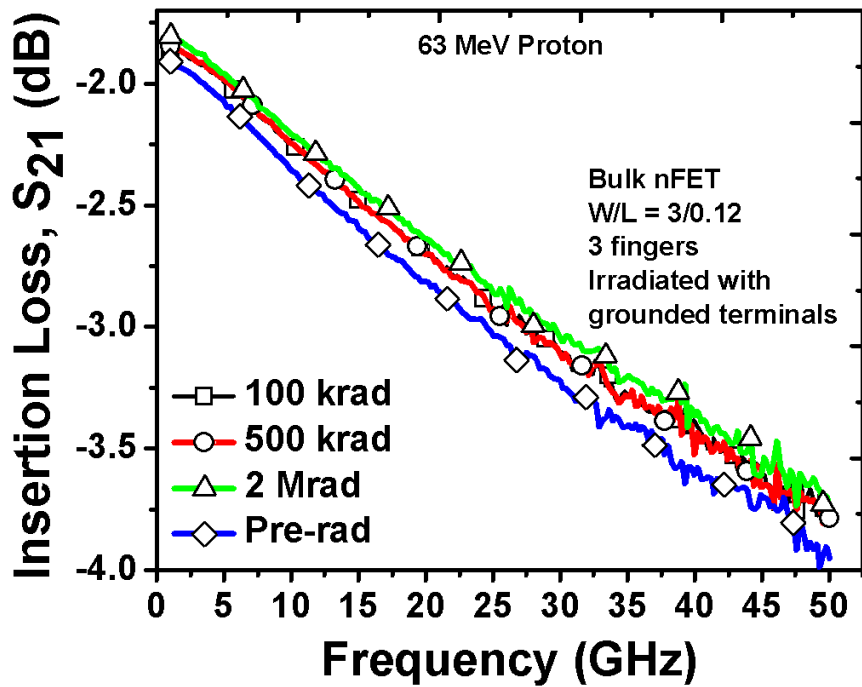


Figure 50. Bulk IL response comparison of pre- and post-radiated results with all terminals grounded (0 V).

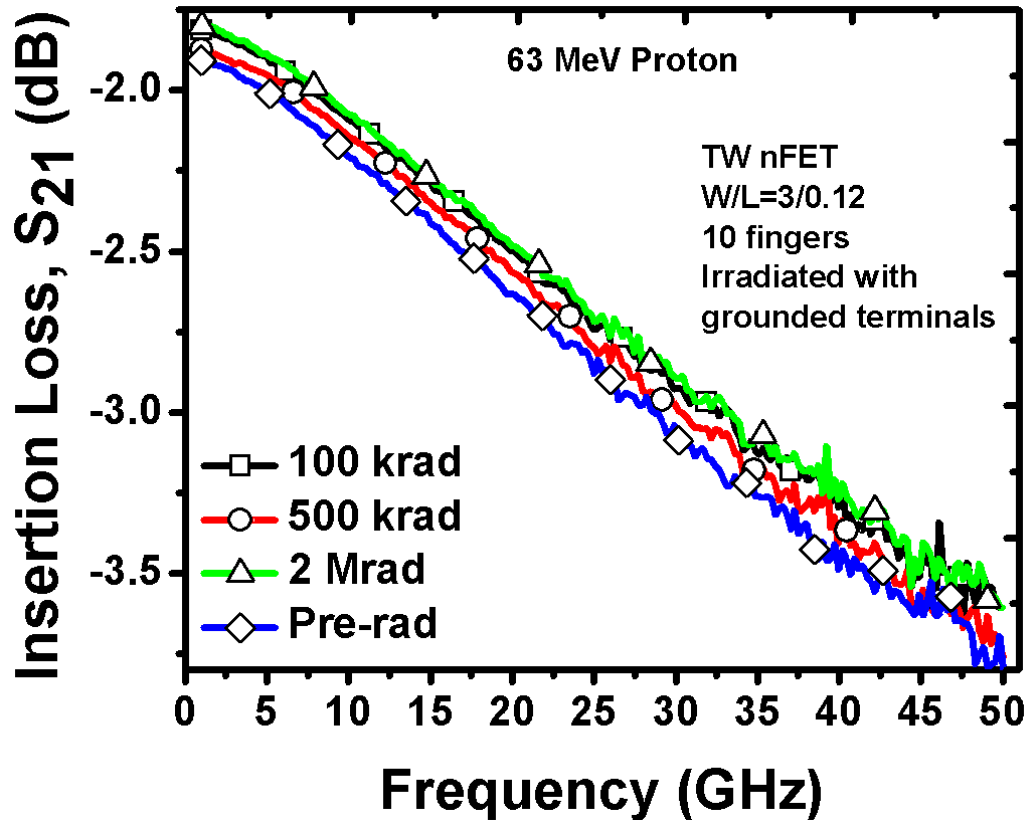


Figure 51. TW IL response comparison of pre- and post-irradiated results with all terminals grounded (0 V).

As previously reported in [14, 23], the bias applied to the samples during irradiation plays a key role on the observed responses. The extracted threshold voltage (V_{th}) as a function of TID for both the TW and bulk transistors under the ‘Biased’ and ‘Grounded’ irradiated conditions is shown in Figure 52. The V_{th} was extracted using the extrapolation of the linear region (ELR) method. The results were also verified using the second derivative logarithmic method [79]. The ‘Biased’ dc samples demonstrate a significantly larger V_{th} shift with increased radiation dose, in contrast to the ‘Grounded’ samples. This is because for the ‘Biased’ samples the transistors have a positive electric field during the irradiation that causes the radiation-generated holes to move towards the STI oxide instead of the gate oxide [14]. This mechanism helps to account for the reason why the RF performance of the SPST switches, and the RF samples (TW and bulk) irradiated with all terminals ‘Grounded’ are not as damaged by the radiation as the samples irradiated under ‘Biased’

conditions. However, the “Grounded” samples still demonstrate V_{th} shift, as the results in Figure 52 illustrate. This is because of the radiation-induced hole trapped charges located at the Si/STI interface have a lower density than the “Biased” samples [76]. As previously stated, the TW V_{th} data for the “Biased” condition displays a trend of a “rebound effect” at a high dose, as noted earlier in the TW dc transfer characteristics in Figure 44. These results affirm the conclusions drawn for the TW transistor: namely, as the radiation dose increases the negative charges from interface traps compensate for the positive trapped holes in the STI, and is manifested as a lower V_{th} shift [14].

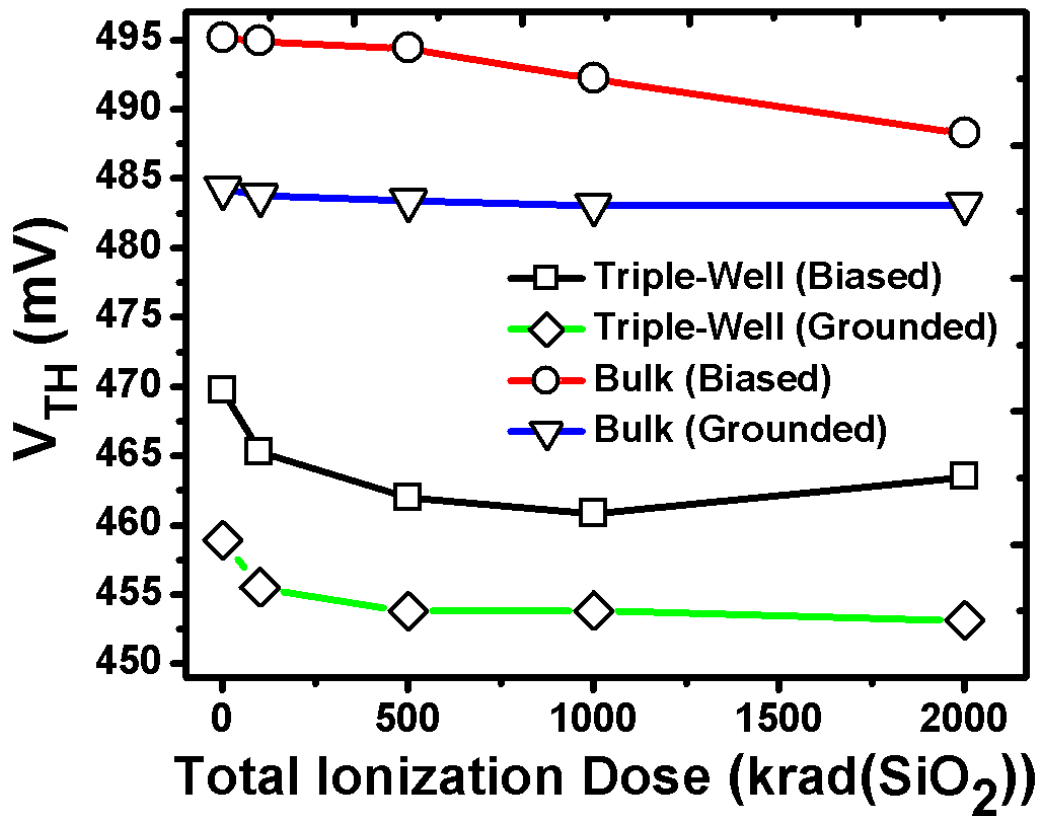


Figure 52. Extracted threshold voltage of both, Bulk and TW devices for the biased and grounded conditions.

6.3 Summary

In this chapter, a comprehensive investigation of the response of SPST RF switches to ionizing radiation was presented. The biased irradiation results show that the RF switch IL improves (S_{21} increases) at 100 and 500 krad(SiO_2), but degrades (S_{21} decreases) at 2 Mrad(SiO_2). The switch ISO shows marginal degradation at 100 and 500 krad(SiO_2), but more than 10 dB reduction at mid-band (10 to 30 GHz) for the 2 Mrad(SiO_2) case. In comparison to the pre-radiation measured data, the SPST switch small-signal (IIP3) linearity increases at low and medium radiation doses, by 1.1 dBm and 1.9 dBm, respectively. But at a high dose of 2 Mrad(SiO_2), it decreases by 5.6 dBm. The large-signal linearity (P_{1dB}) shows a similar trend, with an increase at 100 and 500 krad(SiO_2) dose and then a sharp decrease at 2 Mrad(SiO_2), by ≈ 5.5 dBm. To gain better insight on these results and identify the underlying degradation mechanisms, irradiated measured results of both RF and *dc* transistor samples were performed and analyzed. Additionally, the impact of bias applied to the samples during irradiation was examined. The results show that the RF performance of the “Grounded” samples is not as sensitive to TID as the “Biased” samples. Prior literature supports our conclusion that the main cause of RF performance differences with respect to bias is the density of the radiation-induced hole trapped charges located at the Si/STI interface, which is influenced by the electric fields experienced by the individual devices in the circuit.

CHAPTER 7

EVALUATING THE EFFECTS OF SETS IN FET-BASED SPDT RF SWITCHES

The impact of single event transients (SETs) on single-pole double-throw (SPDT) RF switch circuits designed in a commercially-available, 180 nm second-generation SiGe BiCMOS (IBM 7HP) technology is investigated [10]. The intended application for these SPDT RF switches requires a 1 GHz to 20 GHz band of operation, relatively low insertion loss (< 3.0 dB at 20 GHz), and moderate isolation (> 15 dB at 20 GHz). The two-photon absorption (TPA) experiment results reveal that the SPDT switches are vulnerable to SETs due to biasing effects as well as the triple-well (TW) nFETs, which are found to be more sensitive to SETs than bulk nFETs. From these results, potential implications are discussed and mitigation strategies are proposed. To verify one of the proposed mitigation techniques, SPDT switches were also designed in a 180 nm twin-well SOI CMOS (IBM 7RF-SOI) technology. A different biasing technique is implemented to help improve the SET response. The fabricated SOI SPDT switches achieve an insertion loss of < 1.04 dB at 20 GHz and > 21 dB isolation at 20 GHz. For this circuit, no transients were observed even at very high laser energies (≈ 5 nJ). In this chapter, the impact of single event transients (SETs) on RF SPDT switches is investigated [10]. Mitigation strategies are also presented to eliminate potential detrimental effects on the system-level performance due to SETs potentially propagating from the SPDT circuit into and through the overall RF transceiver chain.

7.1 7HP SPDT Switch Design

The 7HP SPDT switch was designed and fabricated in a commercially-available, 180 nm SiGe BiCMOS (IBM SiGe 7HP) technology [80]. The RF switches were designed using only FETs, with the understanding that other transceiver circuits in the RF chain (e.g., LNA, PA, VCO, etc.) would be fabricated using SiGe HBTs to leverage their enhanced RF

performance and improve robustness to extreme environments [2]. The switch design and measured RF performance were previously discussed in [59] (excluding radiation results). However, a brief description of the design choices are included here to provide insight into the SET response presented. The switch schematic diagram and the corresponding photomicrograph is shown in Figures 53(a) and (b), respectively. The SPDT topology is based on a standard shunt-series configuration. The isolated triple-well (TW) nFET devices, M_1 and M_2 , are used on the series arms to improve the insertion loss of the switch. The TW device provides added substrate isolation and body bias control through the n-well terminal. Standard bulk nFETs were used for the shunt arms M_3 and M_4 , as TW devices were not found to provide any added improvement for isolation [8]. This isolation assumption was verified through circuit simulations. The switch outputs RF_{OUT1} and RF_{OUT2} are complementary, and the digital signal “S” is used to select which output is enabled (ON) or disabled (OFF).

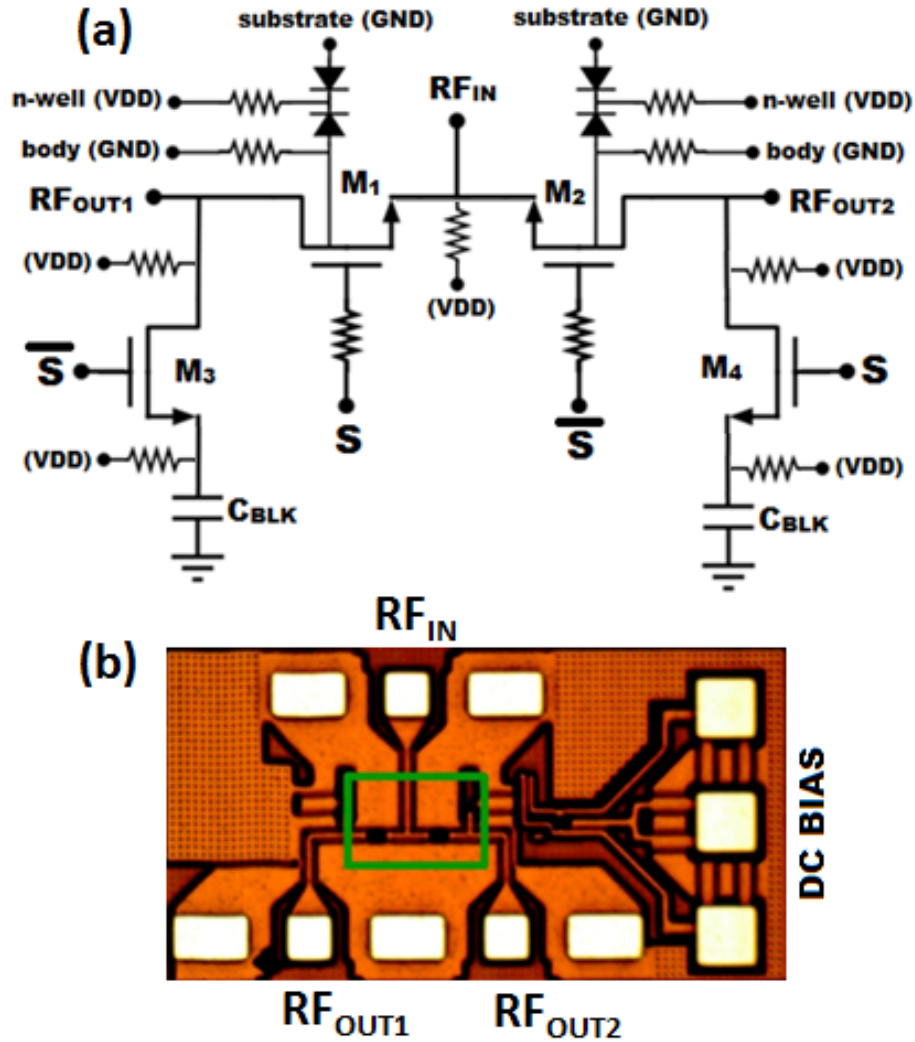


Figure 53. (a) Schematic of the 7HP SPDT switch circuit, (b) Photomicrograph of the fabricated SPDT circuit [11],[57].

All four FETs were sized to minimize insertion loss (IL) and provide moderate isolation (ISO) at the bandwidth of interest (1 to 20 GHz). The TW nFETs were sized with a W/L of 120/0.18 μm , while the bulk nFETs had a W/L of 25/0.18 μm . The source and drain terminals of the nFETs were biased using 10 k Ω resistors to minimize the *dc* power consumption. The use of these large bias resistors does not affect the RF response of the switches. The RF performance of the switches was verified through Cadence simulations and experimentally. In order to improve the *dc* bias isolation and the linearity, the gates, the

body, and the n-well terminals of the FETs were also RF-floated using 10 k Ω resistors [81]. The n-well terminals are biased to “VHIGH”, 3.6 V. Since the drains and sources terminals were pulled up to “VDD” (1.8 V) using large resistors, *dc* blocking capacitors (“ C_{BLK} ”) were used in series with the shunt transistors, M_3 and M_4 . The “ C_{BLK} ” prevents *dc* current from flowing through the shunt arms when the shunt FETs are turned on. The capacitors were sized (≈ 2 pF) to act as an electrical short for the RF signal over the desired operating frequency range. The zero due to C_{BLK} and the transistor R_{ON} was determined to be outside the frequency band of interest. Cadence simulations were used to estimate the R_{ON} value ($\approx 85\Omega$) for the M_3 and M_4 transistors. The “zero” favorably impacts the switch isolation (i.e., S_{21} increases) but, it does not degrade the switch insertion loss (i.e., S_{21} when the switch output is ON).

The switch biasing matrix is shown in Table 4 and it is used to aid in the analysis of the switch SET response. In Table 4, V_{GS} is the gate-to-source voltage. Measurements were performed and the actual transistor V_{DS} varied from ≈ 46 mV to ≈ 53 mV. Simulations and measurements demonstrate that this V_{DS} potential difference is due to the resistor mismatch used to bias the drain and source terminals. This inadvertent V_{DS} potential difference does not affect the FETs in the desired regions of operation. The FETs in the circuit operate between the cutoff and the linear regions. The digital signals “ S ” and “ \bar{S} ” (as shown in Figure 1) are used to modulate the FETs’ gate terminals between these two regions of operation. For example, in the case when RF_{OUT1} is ON and RF_{OUT2} is OFF, the M_1 transistor is operating in linear region since V_{GS1} is set to 1.8 V (i.e., $V_{GS1} = V_{G1} - V_S = 3.6 \text{ V} - 1.8 \text{ V} = 1.8 \text{ V}$), and this value is greater than the V_{TH} ($\approx 0.67 \text{ V}$). The V_{DS} of all transistors are kept constant (≈ 50 mV). For the same bias condition, the M_2 transistor is in the cutoff region since its V_{GS2} is set to $\approx 0 \text{ V}$ (i.e., $V_{GS2} = V_{G2} - V_S = 1.8 \text{ V} - 1.8 \text{ V} = 0 \text{ V}$). The 7HP switch was not originally designed for operation in a radiation-rich environment. Therefore, the design choices mentioned previously will provide understanding of the measured SET results and lead to potential mitigation strategies.

Table 4. SPDT switch-biasing matrix

Device	RF_{OUT1} ON & RF_{OUT2} OFF		RF_{OUT1} OFF & RF_{OUT2} ON	
	S (V)		S (V)	
	7HP	7RF	7HP	7RF
M_1	3.6	1.5	1.8	0
M_2	1.8	0	3.6	1.5
M_3	1.8	0	3.6	1.5
M_4	3.6	1.5	1.8	0

7.2 7RF SPDT Switch Design

The isolated substrate in a Silicon-on-Insulator (SOI) technology makes it naturally suited for use in low-loss FET switches. The 7RF-SOI SPDT switches were designed and fabricated in a commercially-available 180 nm twin-well SOI CMOS (IBM 7RF-SOI) process fabricated on high-resistivity ($\approx 1000 \Omega\text{-cm}$) SOI substrates with three metal layers [5]. The detailed switch design and measured switch RF performance at room temperature is presented in Chapter 4. A brief description of the switch design is included here to provide understanding into the SET response presented in section 7.4.1. The switch topology is similar to the 7HP SPDT switch; it is based on a classical series-shunt topology as shown in Figure 54. The transistor dimensions were selected to minimize insertion loss, increase bandwidth, and improve isolation. The sizes of M_1 , M_3 and M_2 , M_4 are 125/0.18 μm and 40/0.18 μm , respectively. Similar to the 7HP SPDT design, large gate resistances were chosen to minimize RF signal leakage through the gate (R_1 , $R_3 = 17.5 \text{ k}\Omega$ and R_2 , $R_4 = 13 \text{ k}\Omega$).

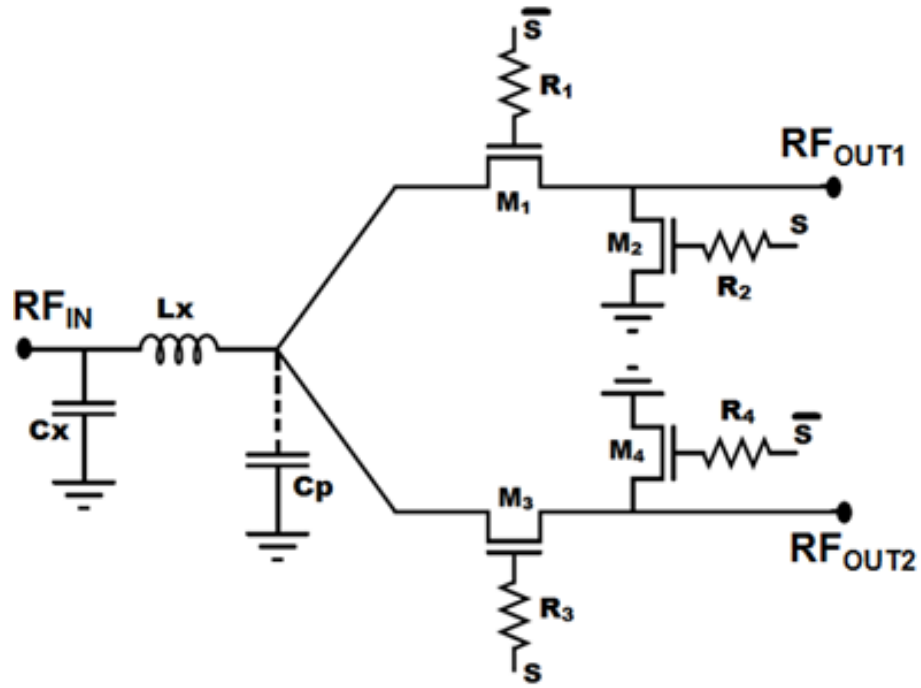


Figure 54. (a) Schematic diagram of the 7RF SPDT switch circuit.

The two main differences between the 7HP and 7RF-SOI SPDT switch designs are the input matching network and the *dc* biasing of the source and drain terminals of the nFETs (i.e., no pull-up resistors are used to bias the source and drain terminals). The latter design choice is important for understanding the SET robustness of the 7RF-SOI SPDT switches. The input matching network consists of L_x and C_x , as shown in Figure 54. The estimation of C_p was based on simulation results and it is used to design a symmetrical π -network by setting $C_x = C_p \approx 33$ fF. The inductor value, $L_x \approx 199$ pH, was computed using the cut-off frequency (40 GHz) and the formula, $1/(2\pi\sqrt{L_x C_x})$ [5]. The parasitic capacitances (C_p), together with the matching network, form a π -match, and are used to improve the input matching and insertion loss at higher frequencies [5]. This LC input matching can potentially influence the SET response of the switch since transients signatures (e.g., duration and peak) are dependent on the effective impedance presented at the transistor terminals [82].

7.3 Experimental Details

The SET experiments were performed at the Naval Research Laboratory (NRL) in Washington, D.C. using charge deposition by through-wafer two-photon absorption (TPA). The laser system is capable of producing a $1.0\ \mu\text{m}$ full-width-at-half-maximum (FWHM) diameter charge distribution profile [83]. The system is configured to produce optical pulses at 1260 nm at a repetition rate of 1 kHz and a pulse width of approximately 150 fs [84]. The system provides the ability to perform 3-D position-dependent (XYZ) time-resolved single event transients non-destructively, and the capability to simulate the effects of heavy ions in space [85]. The laser-induced transient waveforms are captured using a high-speed, high-bandwidth Tektronix DPO71254 12.5 GHz, 50 GS/sec real-time oscilloscope and the Tektronix TCA-SMA RF probes (rated up to 18 GHz). The SPDT switch circuits under test were packaged using a high-speed custom-designed printed circuit board (PCB). The switches were *dc* biased using bias-tees to isolate the *dc* levels from the RF signals and the output transients. All measurements were performed at $50\ \Omega$ characteristic impedance. The translation platform used to secure the PCB has a $0.1\ \mu\text{m}$ position resolution in all three axes, XYZ. All data were collected in a rectangular XY grid at a fixed Z position. For each measurement, the Z position was optimized to place the sensitive volume at the peak focus of the laser beam. [83] provides a detailed description of the measurement system. A photo of the the measurement setup is shown in Figure 55.

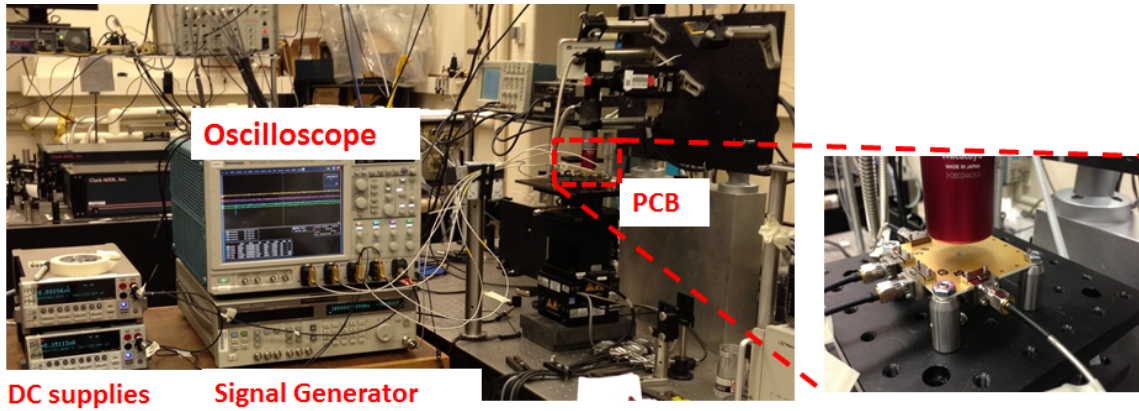


Figure 55. Photo of the SET measurement setup at Naval Research Laboratory including the two-photon absorption system.

7.4 Results and Discussion

7.4.1 7HP SPDT Switch SET Results

To study SETs in the SPDT switches, 2-D scans were performed on all four FET devices that are part of the RF switch. Transients were measured at the output and the V_{DD} terminals for the following two switch configurations: first, when RF_{IN} is connected directly to RF_{OUT1} (when RF_{OUT1} ON), and second, when RF_{IN} is connected to RF_{OUT2} (when RF_{OUT2} ON).

In Figure 56(a) and (b), the recorded transient peak magnitudes at the RF_{OUT1} terminal resulting from the laser strike on the M_3 (shunt) bulk FET are plotted as a function of the incident laser position when RF_{OUT1} and RF_{OUT2} are ON, respectively. Figure 57(a) and (b) show similar data for the M_4 shunt transistor at the RF_{OUT2} terminal. These results reveal that both shunt transistors (M_3 and M_4) are sensitive to SETs. From these results it cannot be determined which of the transistor terminals is more sensitive to laser strike because the focused spot size ($\approx 1.0 \mu\text{m}$) is larger than the gate-to-source and gate-to-drain spacing ($\approx 0.45 \mu\text{m}$). While the sensitive areas for both transistors are similar, the transient peak magnitude varies depending on which RF output is enabled. That is, a strike on M_3 when RF_{OUT1} is ON results in a slightly higher peak magnitude current in comparison to when

RF_{OUT2} is ON, as seen in Figures 56(a) and (b), respectively. A strike on M_4 follows an identical response, as shown in Figures 57(a) and (b). The sensitive areas appear larger than the actual device geometry. This discrepancy likely ensues from the large pulse irradiance used for this set of experiments coupled with the finite spot size of the laser pulse. The apparent size of the sensitive area in Figures 56 and 57 is a consequence of the overlap of the tails of the Gaussian laser pulse profile with the sensitive region of the device [34].

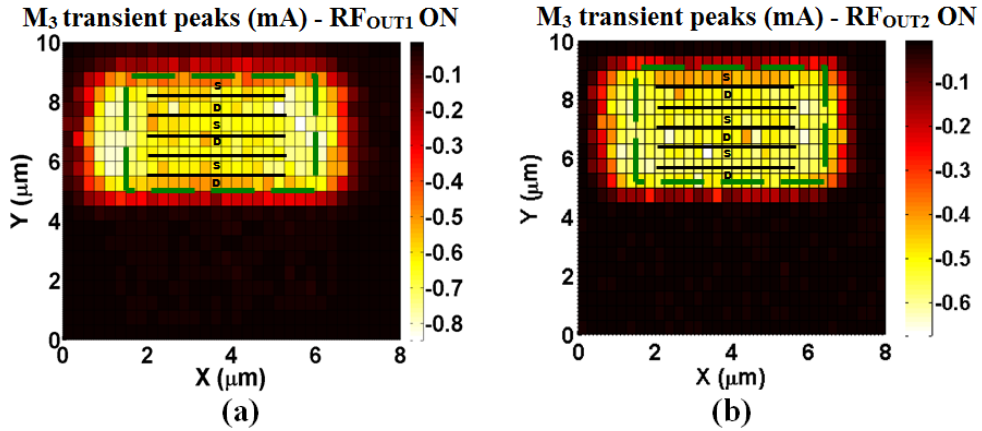


Figure 56. Measured peak transient currents at the RF output terminals as a function of position resulting from a laser strike on M_3 , with an incident laser pulse energy of 1.7 nJ when (a) RF_{OUT1} is ON and when (b) RF_{OUT2} is ON.

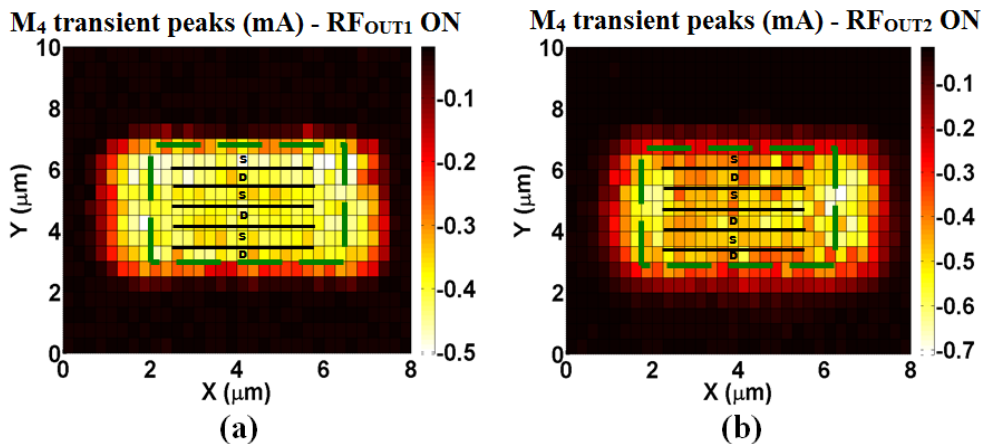


Figure 57. Measured peak transient currents at the RF output terminals as a function of position resulting from a laser strike on M_4 with an incident laser pulse energy of 1.7 nJ when (a) RF_{OUT1} is ON and when (b) RF_{OUT2} is ON.

To gain further understanding of these 2-D results, the time-resolved transients at similar XY positions are shown in Figures 58 and 59 for the M_3 and M_4 FETs, respectively. These results are based on XY positions that yield the largest (worst-case) transient peak magnitude. The transient response for strikes on M_3 when the corresponding and the complementary RF output nodes are ON is shown in Figures 58(a) and (b) (i.e., comparing transients on M_3 FET when RF_{OUT1} is ON or RF_{OUT2} is ON). The transient peak amplitude and duration decrease by ≈ 0.2 mA and ≈ 800 ps, respectively. The transient's duration for M_3 is 993 ps when RF_{OUT1} is ON, and 194 ps when RF_{OUT2} is ON. The results from M_4 (Figure 59) are similar to those observed for M_3 but, in opposite order. As the RF output is toggled, the transient peak amplitude and duration increase by similar amounts as M_3 , ≈ 0.2 mA and ≈ 800 ps, respectively. These results confirm that the recorded peak and duration of the transients at any output terminal are dependent on which transistor in the switch the laser pulse strikes. The effective impedance presented on any output node (e.g., RF_{OUT1}) is dependent on which output is enabled, thus altering the shape of the observed transients [82]. According to [33] the duration of the transient pulse is dependent on the rate at which the holes are removed from the p-well. The criterion used to calculate the transient's duration is based on the initial value of the current prior to the transient pulse and the time it took for the current to reset to this initial value. A threshold value of ± 0.0025 mA was used to extract the SETs durations.

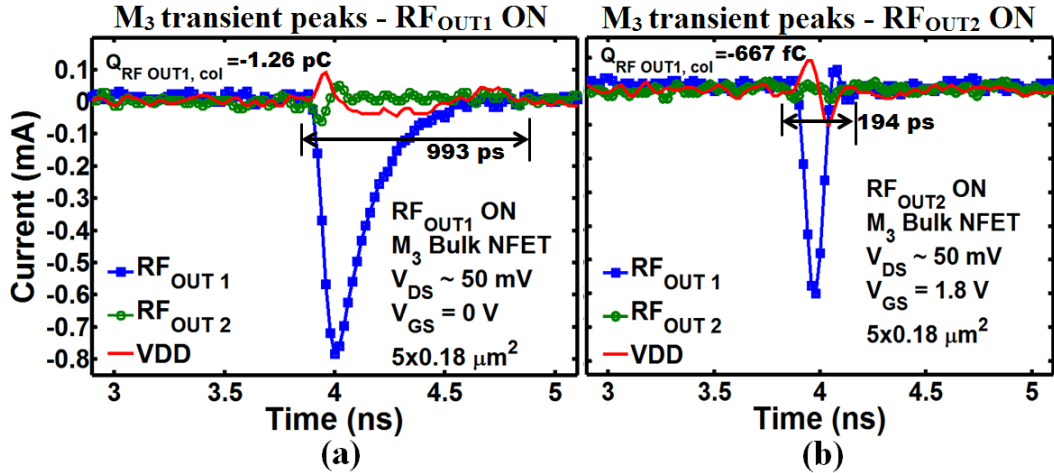


Figure 58. Transient currents at the RF output terminals from a laser strike on M_3 (bulk FET), for an incident laser pulse energy of 1.7 nJ when (a) RF_{OUT1} is ON, and (b) RF_{OUT2} is ON (The pulse duration numbers shown on the plots here represent exact values as extracted from the waveform, while the range bars are visual guidelines and not to scale).

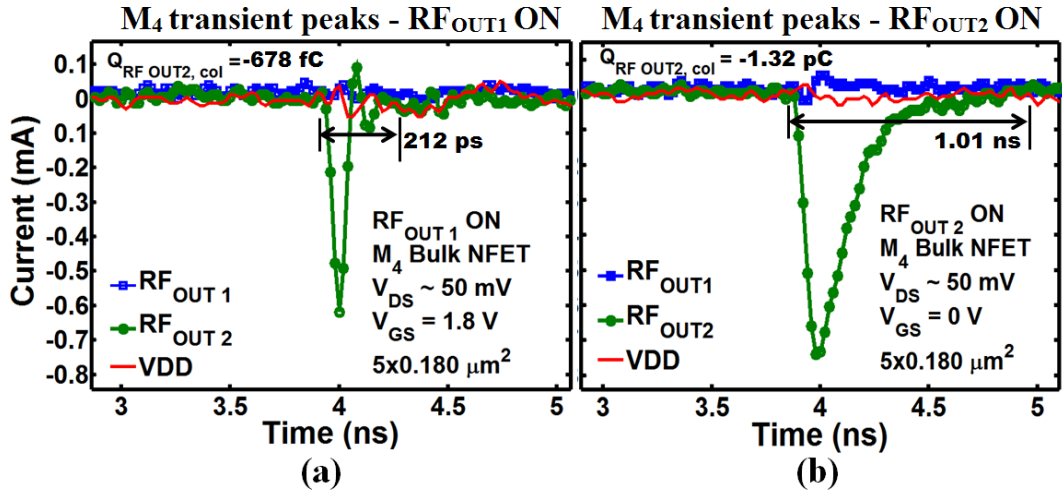


Figure 59. Transient currents at the RF output terminals from a laser strike on M_4 (bulk FET), for an incident laser pulse energy of 1.7 nJ when (a) RF_{OUT1} is ON, and (b) RF_{OUT2} is ON (The pulse duration numbers shown on the plots here represent exact values as extracted from the waveform, while the range bars are visual guidelines and not to scale).

The peak transient currents recorded at the output terminals from laser strikes at similar XY positions on the series TW FETs, M_1 and M_2 , are plotted as a function of time in

Figures 60(a) and (b), respectively. The results from strikes on both FETs (M_1 and M_2) exhibit similar transients when the corresponding output terminal is ON (i.e., RF_{OUT1} ON during strike on M_1 with its V_{GS} set to 3.6 V; or RF_{OUT2} ON during a strike on M_2 with its V_{GS} set to 3.6 V, as summarized in Table 4). From Figure 60, peak transients are only observed on the corresponding output (e.g., for M_1 strike at RF_{OUT1} which is ON) but not at the complementary output (RF_{OUT2} which is OFF). In other words, Figure 60(a) shows captured current transient peaks from laser strikes on M_1 when RF_{OUT1} is ON, and transients are only present on the RF_{OUT1} terminal and not on RF_{OUT2} .

However, when the biasing is changed for a strike on M_1 , i.e., M_1 is OFF and M_2 is ON, enabling RF_{OUT2} and turning RF_{OUT1} OFF (see Table 4) as shown in Figure 61(a), transients are now observed on both output terminals. The plots in Figure 61 indicate that this phenomenon is possibly due to a charge sharing mechanism between the source terminals of the two FETs, M_1 and M_2 . This is because the source terminals of M_1 and M_2 are electrically connected; they form a single node as shown in Figure 53(a). Therefore, transient signals are observed on both RF_{OUT1} and RF_{OUT2} outputs because M_2 presents a low impedance path from M_1 to RF_{OUT2} . Transient results for M_2 are shown in Figure 61(b); it follows the same response as M_1 .

As previously reported in [33], TW devices collect more charge during a single event strike compared to bulk (dual-well) devices. During a single event strike more holes are accumulated in the p-well of the TW device. This causes the p-well potential to rise and forward bias the source-p-well junction, thus forcing the source terminal to inject electrons into the p-well. This mechanism was termed “p-well potential de-bias” [33]. This additional collected charge can potentially be subjected to charge sharing with other nodes in close proximity (i.e., the source terminals of M_1 and M_2 TW devices are electrically connected). The charge sharing results from the diffusion of the carriers in the substrate/well as a direct result of a laser strike [31]. The wells of the OFF TW transistor (i.e., $V_{GS} = 0$ V) are struck during the 2-D laser scan, and some of the charges generated from the strikes

will be collected at the terminals of the OFF transistors (high impedance nodes). These collected charges produce small pulses at the output terminal, as shown in Figures 58 and 59. These small pulses are illustrated by the green and red traces in Figure 58, and by the blue and red traces in Figure 59.

Long current transients duration (> 10 ns) on the V_{DD} terminal of the switch are observed in Figures 60 and 61. These transients are likely caused by the deposited charges that do not readily diffuse out or recombine, which are then collected by the substrate or well contacts [31]. As the drain, source, and deep n-well terminals of the TW FETs are biased using large impedances (to float the nodes under RF conditions), the charges collected at these terminals couple together, and thus are manifested as long current transients on the V_{DD} terminal due to the high impedance presented. These long transients on V_{DD} can potentially impact the overall RF system performance by disturbing the bias of other circuit blocks in the RF chain (e.g., LNA, VCO) that could be sharing the same supply rail.

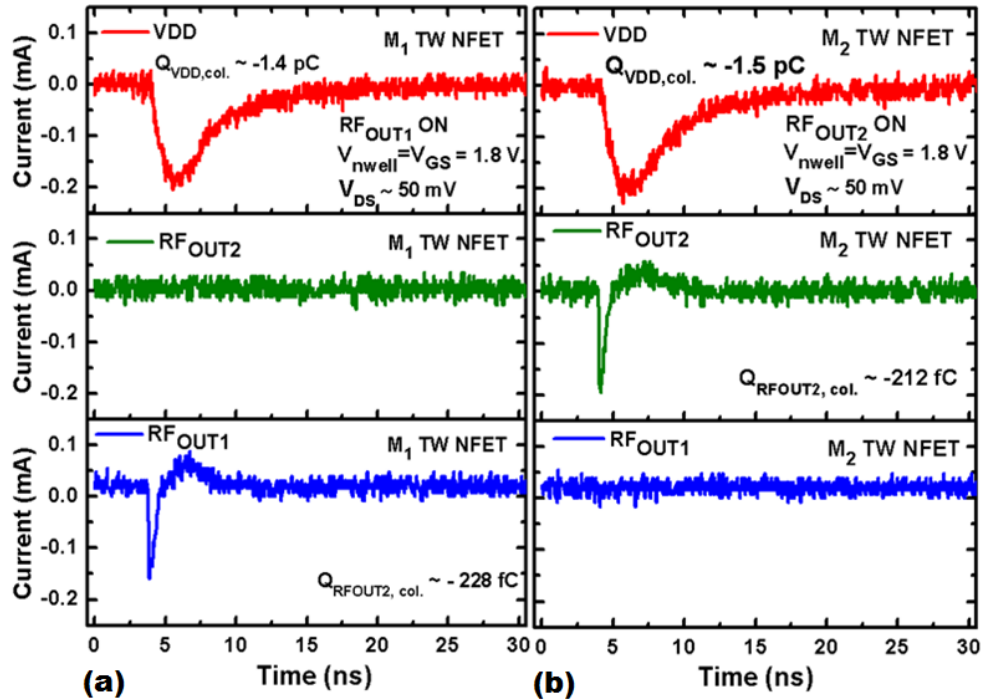


Figure 60. Transient currents for a incident laser (a) on M_1 TW transistor when RF_{OUT1} is ON, (b) on M_2 TW transistor when RF_{OUT2} is ON, using a laser pulse energy of 1.7 nJ.

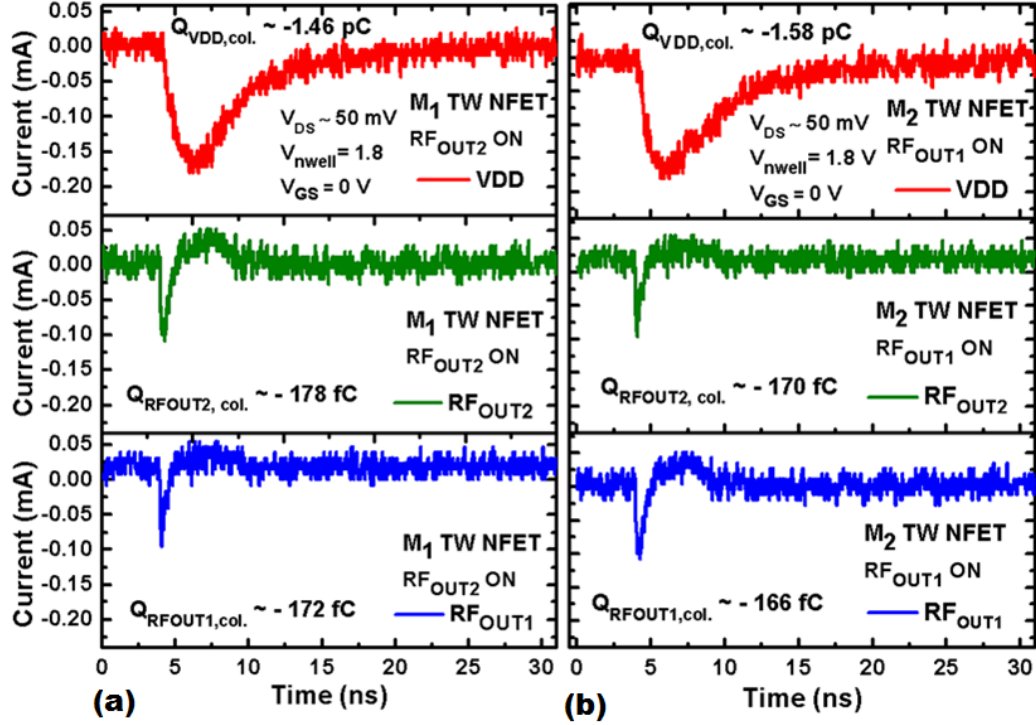


Figure 61. Transient currents for a incident laser (a) on M_1 TW transistor when RF_{OUT2} is ON, (b) on M_2 TW transistor when RF_{OUT1} is ON, using a laser pulse energy of 1.7 nJ.

The 7HP SPDT measured results presented thus far do not consider the impact of the laser-induced transient waveforms on an RF signal. The measured results when a 1 GHz and 150 mV peak-to-peak RF signal applied on the input terminal (RF_{IN}), with RF_{OUT1} ON during a strike on M_3 (bulk) and RF_{OUT2} ON during a strike on M_4 (TW) are shown in Figures 62(a) and (b), respectively. The measurements were limited to 1 GHz to simplify the capture and analysis of the laser-induced transient waveforms by the oscilloscope. These results confirm that the RF signals are susceptible to amplitude distortion due to SETs. In the following section, current injection simulations are performed using “worst case” measured transients as a first attempt to provide additional insight and further understanding of the implications of laser-induced transients on RF signals propagating from the SPDT circuit into other RF blocks.

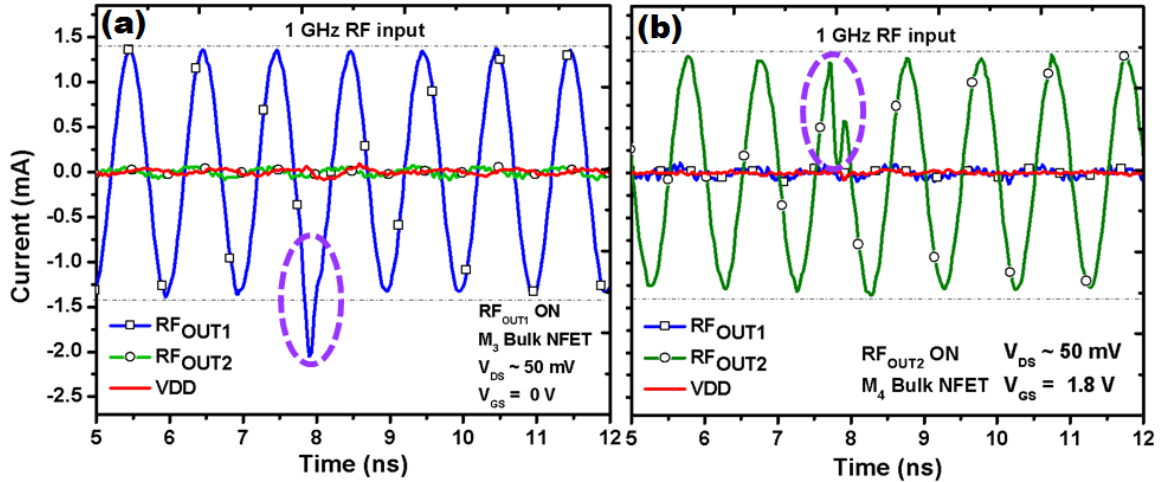


Figure 62. Measured transient currents at the RF output terminals of the 7HP SPDT switch from a laser strike on (a) M_3 and (b) M_4 transistors for an incident laser pulse energy of 1.7 nJ; RF input signal of 1 GHz and 150 mV peak-peak.

7.4.2 7RF SPDT Switch SET Results

Based on the 7HP SPDT SET results, three potential SET mitigation techniques are proposed: 1) design and fabricate the switch on an SOI technology (note that SiGe BiCMOS on SOI technologies do presently exist in multiple foundries); 2) use a different device biasing scheme designed to minimize the charge collection mechanism at device terminals from single event current pulses (e.g., by maintaining V_{DS} at ≈ 0 V); and lastly, 3) use only non-TW, bulk transistors, as TW devices are known to collect more charge during single event strikes when compared to dual-well devices [33]. The SOI has a reduced volume for charge carrier generation in comparison to 7HP, thus decreasing the charge collection depth of normal incident charged particles [15]. The results from only two of these techniques are shown in the present chapter; (1) the design and fabrication of the switch on SOI, and (2) the use of a different biasing scheme on the SOI switch.

Using a similar topology as the 7HP switch (as shown in Figure 54), the SPDT circuit was re-designed and fabricated using 7RF-SOI technology. The SOI switch circuits were packaged and SEE testing was performed using the same setup described in section

7.3. The observed robustness of the 7RF-SOI switch was significantly better than the 7HP switch. This can be attributed to differences in design and technology. For the 7RF switch no transients were observed even at very high laser energies, and the FETs experienced breakdown before any transients were observed. As stated previously, the drain and source terminals of the 7RF-SOI SPDT switches were not biased with large pull-up resistors, and the reason for this design choice is to keep V_{DS} at ≈ 0 V. This biasing scheme prevents charge carriers generated during a strike from being collected at the drain and/or source due to the absence of elevated electric fields between the drain and source terminals. The transistors are biased in two regions: 1) the linear region ($V_{GS} = 1.5$ V and $V_{DS} \approx 0$ V), or 2) the cut-off region ($V_{GS} = V_{DS} = 0$ V). Furthermore, the size of the transistors and the effective impedance at the sensitive nodes does impact the nature of the transients and the overall circuit sensitivity to SETs.

For the 7RF-SOI SPDT switches, transients were only observed when a “forced V_{DS} ” potential (≈ 150 mV peak-to-peak) was imposed on the input and output terminals. This “forced V_{DS} ” was performed using external bias-tees to set the dc potential on the drain terminals (RF_{OUT1} and RF_{OUT2}) and 0 V (ground) on the source terminal (RF_{IN}). The measured results for a strike on M_1 with RF_{OUT1} ON, and M_4 with RF_{OUT2} ON at a laser pulse energy of 5 nJ are shown in Figure 63(a) and (b), respectively. A 1 GHz, 200 mV peak-to-peak input RF signal was applied at the input terminal. The results shown in Figure 63(a) follows a response similar to that of the 7HP switches (Figures 62(a) and (b)); the laser-induced transients distorts the amplitude of the RF signal. However, when the strike is on the shunt transistor, M_4 and the complementary output ON (i.e., the RF signal is routed to RF_{OUT1} instead of the corresponding output RF_{OUT2}) the output RF signal is not perturbed.

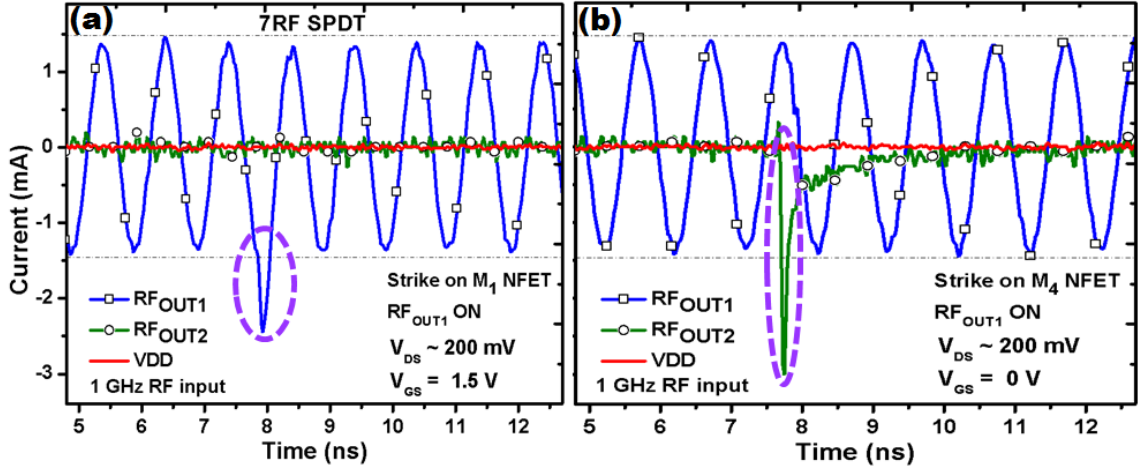


Figure 63. 7RF-SOI SPDT “forced V_{DS} ” transient currents for a incident laser (a) on M_1 transistor when RF_{OUT1} is ON, (b) on M_4 transistor when RF_{OUT1} is ON, using a laser pulse energy of 5 nJ.

However, a noticeable transient (> 2.5 mA) is observed at the RF_{OUT2} terminal, the corresponding output. Reference [44] reports that this increase in current can be attributed to parasitic source-body-drain bipolar structure which has the potential to significantly amplify the charge deposited in the body region. The 7RF switches were implemented with floating-body FETs. As previously reported in [32], floating-body FETs are more sensitive to this effect than body-contacted FETs. The two mechanisms that can contribute to transients when the body potential moves above the source potential are: 1) the increase in the channel current from the reduced threshold voltage due to the body effect, and 2) the parasitic bipolar transistor turning on as a result of an increase in the body current from the laser strike depositing charges in the body, thus resulting in a drain current larger than the body current [32].

For the “forced V_{DS} ” bias condition, larger transients due to charge sharing mechanisms were observed on the 7RF-SOI switches, as compared to the 7HP switches. During a strike on the shunt transistors for the “forced V_{DS} ” bias, the recorded output currents increased to a maximum of approximately 6 mA, as shown in Figure 64. The peak transient at the RF_{OUT2} (green trace) has a time delay in comparison to the peak transient at the RF_{OUT1} (blue trace). The time shift between the pulses is potentially due to propagation delay

from M_3 through M_4 . This propagation delay consists of three components: the parasitic bipolar delay, transmission line delay, and the FET delay. The transmission lines referred to here are the metal traces used to connect the devices within the switch. The transmission lines were designed using the Sonnet Electromagnetic Simulator software to present 50Ω characteristic impedance in the bandwidth of interest, 1 to 20 GHz.

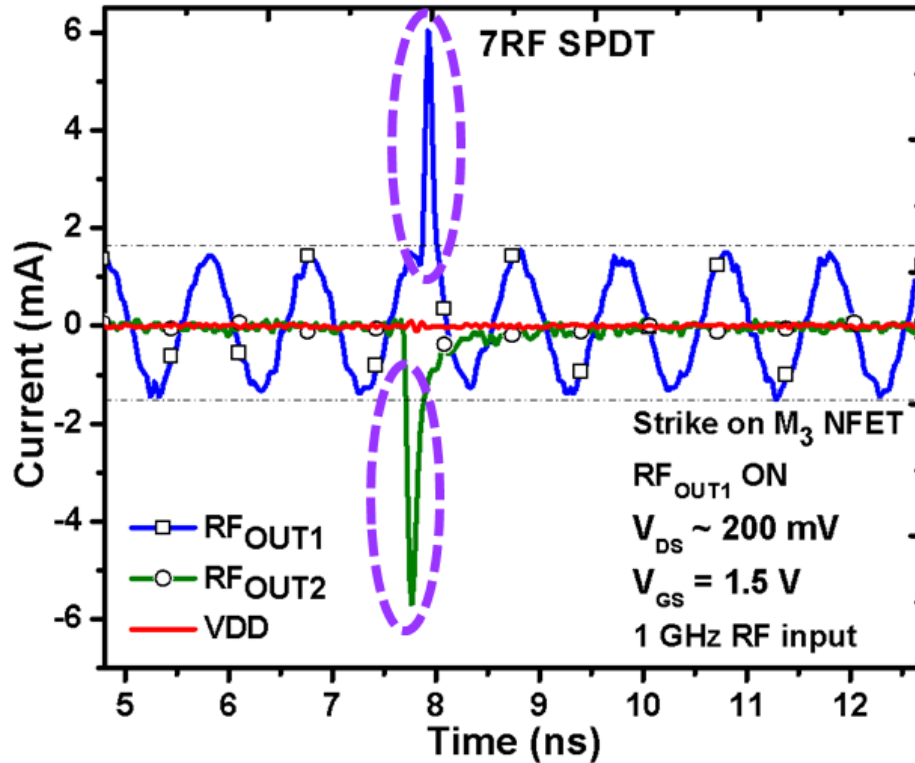


Figure 64. Transient currents for a incident laser on M_3 transistor when RF_{OUT1} is ON, using a laser pulse energy of 5 nJ.

7.5 Current Injection Simulation Results

Current-injection simulations were carried out as a first step to provide additional insight into how the propagating SET current transients (e.g., from the SPDT output terminals to the input of an LNA circuit) can potentially affect high frequency input and output signals of subsequently connected circuit blocks in the RF chain. The Cadence Spectre tool was used for the current injection simulations. For these simulations, an LNA circuit was used,

and its schematic is shown in Figure 65. The design and RF performance of the LNA is detailed in [86]. The injected transient current pulses have two different pulse signatures. The first pulse was recorded from a laser strike on the 7HP SPDT M_3 shunt bulk transistor, and has a higher peak amplitude of ≈ 0.8 mA with a relatively fast duration of ≈ 0.9 ns. The second transient was recorded from the 7HP SPDT M_2 transistor, and the signal has a lower peak amplitude of ≈ 0.31 mA and a longer duration of ≈ 2.6 ns. Figures 66(a) and (b) illustrate the transient simulation results at the input (RF_{IN}) and the output (RF_{OUT}) of the LNA, respectively.

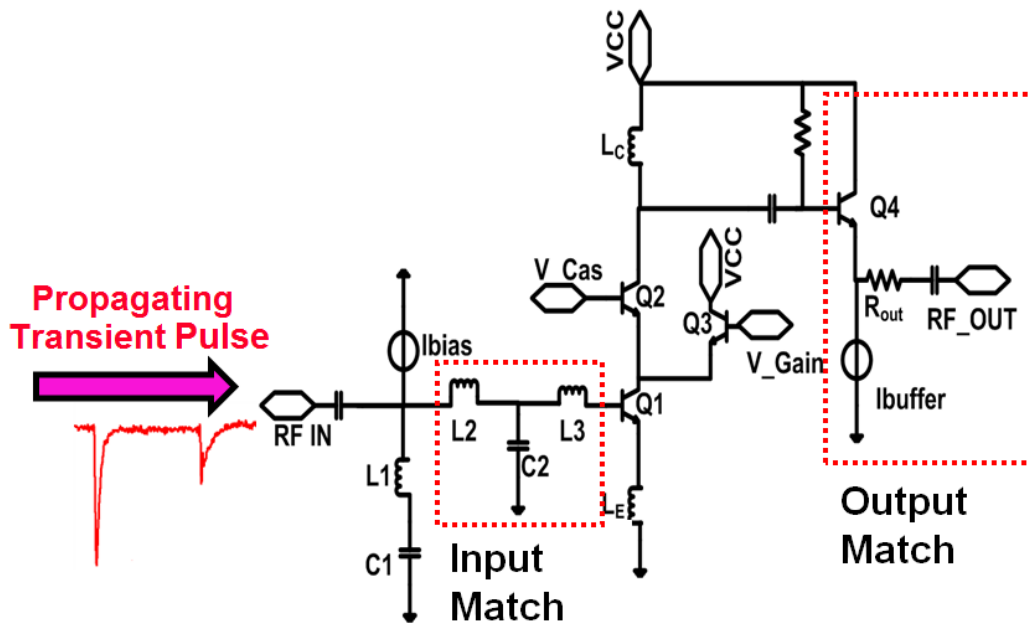


Figure 65. LNA schematic diagram and an illustration of the current injection simulation performed [84].

The current injection SET simulation results are depicted in in Figure 66, at the LNA input (a), at the input terminal (RF_{IN}) (b), and at the output terminal (RF_{IN}) (c). Simulations results reveal that the injected SET current transient (shown in Figure 66 (c)) does appear to cause voltage amplitude distortions on both the input and output signals. However, the distortion on the output signal appears to be minimal compared to the input. The simulated amplitude distortions are potentially due to quiescent bias voltage shifts caused by the propagating SET through the LNA transistors. These preliminary simulation results

represent a first attempt to demonstrate that propagating transients through an RF switch can impact the input and output signals of subsequently connected RF circuit blocks in the transceiver chain.

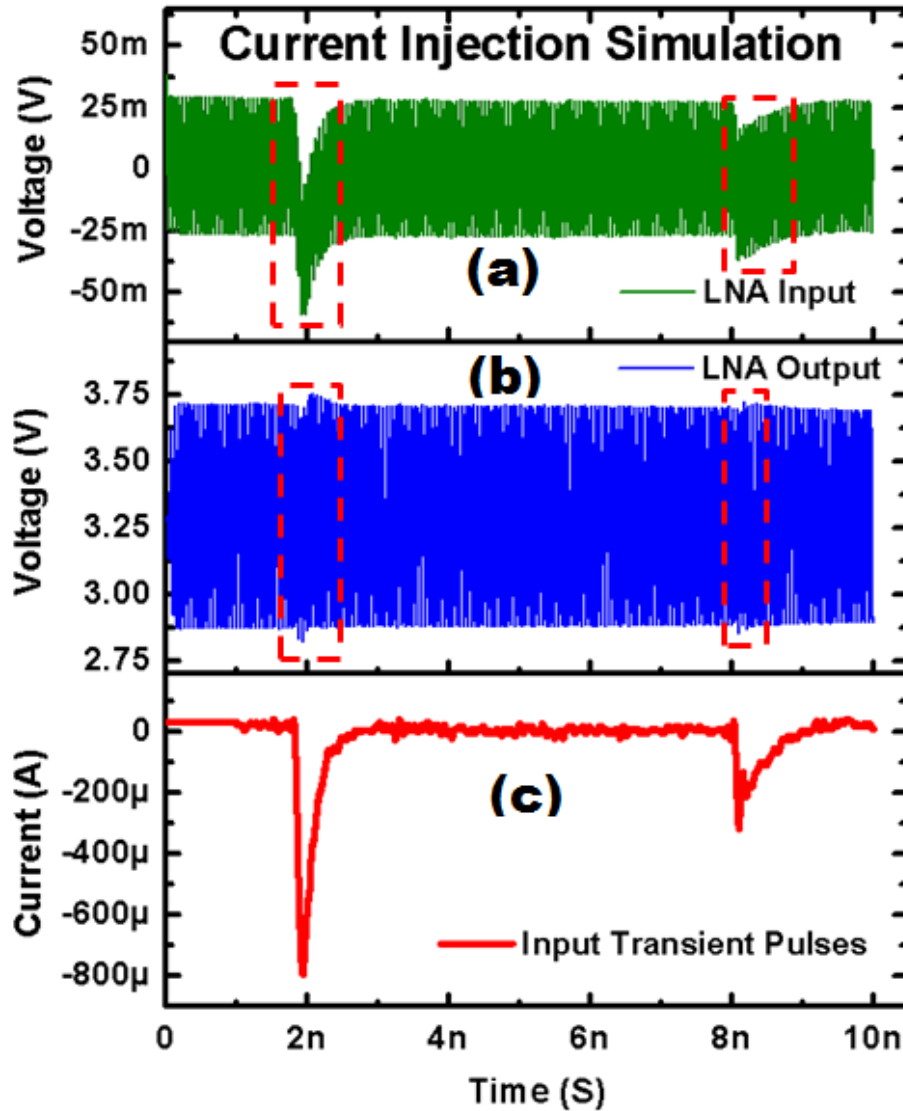


Figure 66. Current injection SET simulation results at (a) LNA input, RF_{IN} and (b) LNA output, RF_{OUT} . (c) The injected measured transient pulses.

7.6 Summary

This chapter presented an investigation of the impact of single event transients (SETs) on RF SPDT switches using charge deposition by through-wafer two-photon absorption

(TPA). The SPDT switch was designed and fabricated in the commercially-available 180 nm SiGe BiCMOS (IBM SiGe 7HP) technology. The TPA measured results reveal that both shunt transistors M_3 and M_4 are susceptible to SETs. These results confirm previous findings that the TW nFETs are more sensitive to SETs than bulk nFETs. This is because TW devices collect more charge during a single event strike compared to bulk (dual-well) devices, through a mechanism known as “p-well potential de-bias”. Another important design aspect that can influence the SET response of the 7HP SPDT switches is the biasing scheme. The large pull-up resistors used to dc bias the drain and source terminals should be avoided or careful layout techniques should be applied to prevent unintended dc potential across the drain-to-source terminals. The V_{DS} affects the charge collection on the switch nodes.

Based on the measured 7HP SPDT results, three mitigation strategies were proposed to minimize SETs from propagating from the SPDT circuit into other connected circuits (e.g., LNA, Mixer, VCO). However, only two out the proposed three mitigation strategies were implemented and discussed here: 1) design and fabricate the switch on an SOI technology; 2) the use of a different device biasing scheme designed to minimize the charge collection mechanism at the device terminals. A second SPDT circuit was designed and fabricated using a commercially-available 180 nm RF-CMOS on SOI (IBM 7RF) technology to evaluate the aforementioned mitigation strategies. For the 7RF SPDT switch, no transients were observed even at very high laser energies, and the FETs experienced breakdown before any transients were observed. However, when a V_{DS} dc potential is forced across the device being struck, large transients are observed. The parasitic bipolar amplification is potentially the reason for the large transient current peaks. TPA experiments were also performed with a 1 GHz RF signal at the input of the SPDT switch circuits. The results show that the RF signal amplitude can be distorted by the SETs; this distortion increases as V_{DS} dc potential increases. Current-injection simulations were also performed to provide additional insight into the system-level impact of propagating SET current transients.

CHAPTER 8

SET AND TID RESPONSE OF VOLTAGE REFERENCE CIRCUITS DESIGNED IN A 90-NM SIGE BICMOS TECHNOLOGY

Voltage reference circuits (VRCs) (e.g., bandgap voltage references (BGRs)) are ubiquitous building blocks in a wide variety of electronic systems. The main objective of VRCs is to generate a robust and stable bias voltage that is invariant to process, supply voltage, and temperature (PVT) variations. The robustness requirements are inherently more challenging for space-based electronics, such as satellites in a geosynchronous orbit, due to exposure to the radiation-rich environment. In a space environment, the electronics experience constant bombardment by a wide spectrum of energetic photons and particles. Therefore, it is imperative to have bias circuitry that is radiation tolerant. SiGe BiCMOS technologies provide a single platform that enables a wide variety of high performance, highly-integrated applications such as monolithic microwave integrated circuits (MMICs) and system-on-chip (SoC) solutions. SiGe BiCMOS technology has been proven to be a strong candidate for these types of extreme environment applications [2, 3].

Recent investigations have reported total ionization dose (TID) and single event transient (SET) response of SiGe BiCMOS voltage references [40, 87–89]. Some of these studies concluded that SiGe BGR total dose response is dependent on the radiation source used for the exposure [87, 88], but TID impact on the output voltage of the BGR circuit is minor. [40, 89] have demonstrated that SiGe HBT-based BGR circuits are sensitive to SETs. Prior studies concluded that SiGe HBTs lack of immunity is due to charge collection through the reverse-biased lightly-doped p-type substrate to n-type subcollector junction [90–92]. Therefore, the main focus of this work will be on the SET response of the BGR circuits and the proposed circuit-level RHBD approaches. The results presented to date were primarily focused on circuits designed in first- and third-generation SiGe BiCMOS technologies. [89] proposed a SET radiation-hardening-by-design (RHBD) technique

that required device-layout modifications, but this is not a desirable approach since it increases the area and the fabrication cost. Furthermore, this proposed RHBD approach only provides partial mitigation and is likely not to be TID robust due to an additional pn junction [92].

The goal of this work is to investigate and analyze how the VRC radiation response (both SET and TID) is impacted by technology scaling to a new 4th-generation SiGe BiCMOS technology [12]. Based on these findings, new circuit-level RHBD techniques are proposed that have little or no power, area, or cost penalty, and provide high degree of immunity to SETs. The circuit-level RHBD techniques for mitigating SETs are implemented by carefully using inverse-mode (IM) transistors in the circuit while trying to maintain the overall VRC performance. We also present a PIN diode VRC as a potential SET and TID circuit-level RHBD alternative. The SET and TID responses of this new PIN-based VRC topology are compared against the first-order and the IM BGR circuit topologies presented here. SET and TID response at transistor level were also measured to aid the understanding of our results. SiGe HBTs are implemented instead of Si bipolar transistors (e.g., parasitic vertical pnp) because of the enhanced performance at cryogenic temperature and the low noise capability (i.e., low 1/f noise and phase noise) [93], [94]. Both, reliable cryogenic temperature operation and low noise performance are important requirements when designing electronics for space applications.

8.1 Voltage Reference Circuit Design

The VRCs were designed in a 4th-generation IBM SiGe BiCMOS process technology (9HP). This technology integrates 90 nm CMOS and high-speed SiGe HBTs in a single design platform. The SiGe HBT has an f_T/f_{MAX} of 300/350 GHz and an advanced back-end-of-the-line (BEOL), which includes a full suite of mm-wave passive elements. The details of the device structure and the fabrication process are provided in [95]. The use of 300 GHz f_T devices in space electronics can enable a new integrated system solution

similar to the Multi-Chip Module remote sensor interface reported in [96,97].

The schematic diagrams of the first-order, IM-first-order, PIN diode VRCs implemented in 9HP SiGe technology are shown in Figures 67, 68, 69, respectively. The core of the topology for all three VRCs is based on a first-order, uncompensated BGR (i.e., no extra internal circuit is added for temperature compensation) [87]. For the purposes of this study, a simple first-order compensation topology (Figure 67) was chosen to minimize circuit design complexity and to aid in the understanding of the circuit radiation response. The higher-order BGR compensation techniques will not be discussed here, but are widely available in literature. This topology consists of a startup circuit, with the M_1 transistor, followed by a bias stage where a proportional to absolute temperature (PTAT) current is generated for the next stage. This PTAT current stage is composed of transistors M_2 - M_7 , Q_1 - Q_2 , and the resistor R_1 . The third and final stage cancels the negative temperature dependence of the base-emitter voltage of Q_3 with the positive voltage generated by the previous stages. This cancellation is accomplished by mirroring the PTAT current using transistors M_8 and M_9 and then passing it through resistor R_2 to generate an output voltage, V_{OUT} , that is invariant to temperature. The geometry of the SiGe HBTs Q_1 and Q_3 are $0.1 \times 2.0 \mu\text{m}^2$ and $0.1 \times 0.78 \mu\text{m}^2$, respectively. The area of the transistor Q_2 consists of three parallel copies of Q_1 .

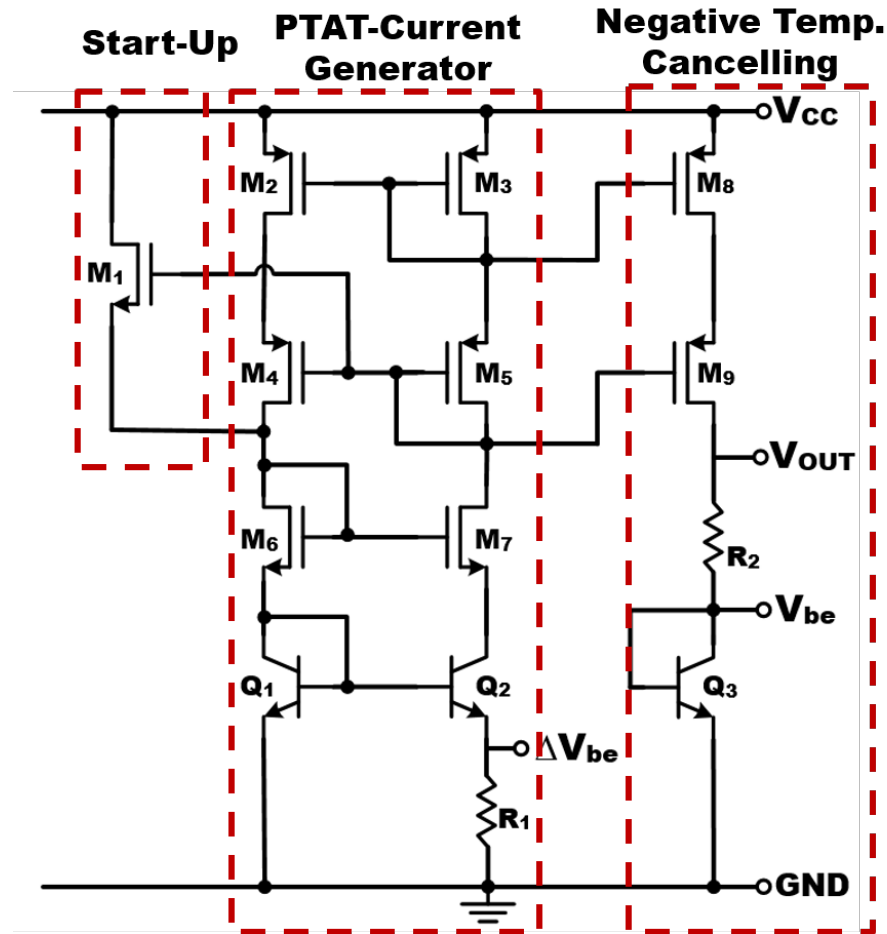


Figure 67. Schematic diagram of the 1st-order voltage reference circuit (VRC).

The schematic diagram of the inverse-mode (IM) VRC is shown in Figure Figure 68, and it follows the same topology as the first-order VRC. The main difference is the use of SiGe HBTs Q_1 and Q_2 in the IM of operation (i.e., devices are operated with the collector and emitter terminals electrically swapped [98]). The results presented in [26] show that IM SiGe HBTs provide a significant improvement in circuit-level SET sensitivity. This RHBD approach has been investigated for digital circuits [98] and [99]; the present work demonstrates its application in an analog circuit. The use of IM devices required additional tuning of the device parameters (mainly resistors R_1 and R_2 , and transistors M_8 and M_9) for this circuit to achieve temperature coefficient (TC) performance equivalent to that of the first-order circuit. The geometry of the SiGe HBTs Q_1 and Q_2 remained the same as the

first-order BGR, but only the area of the transistor Q_3 increases to $0.1 \times 1.5 \mu\text{m}^2$.

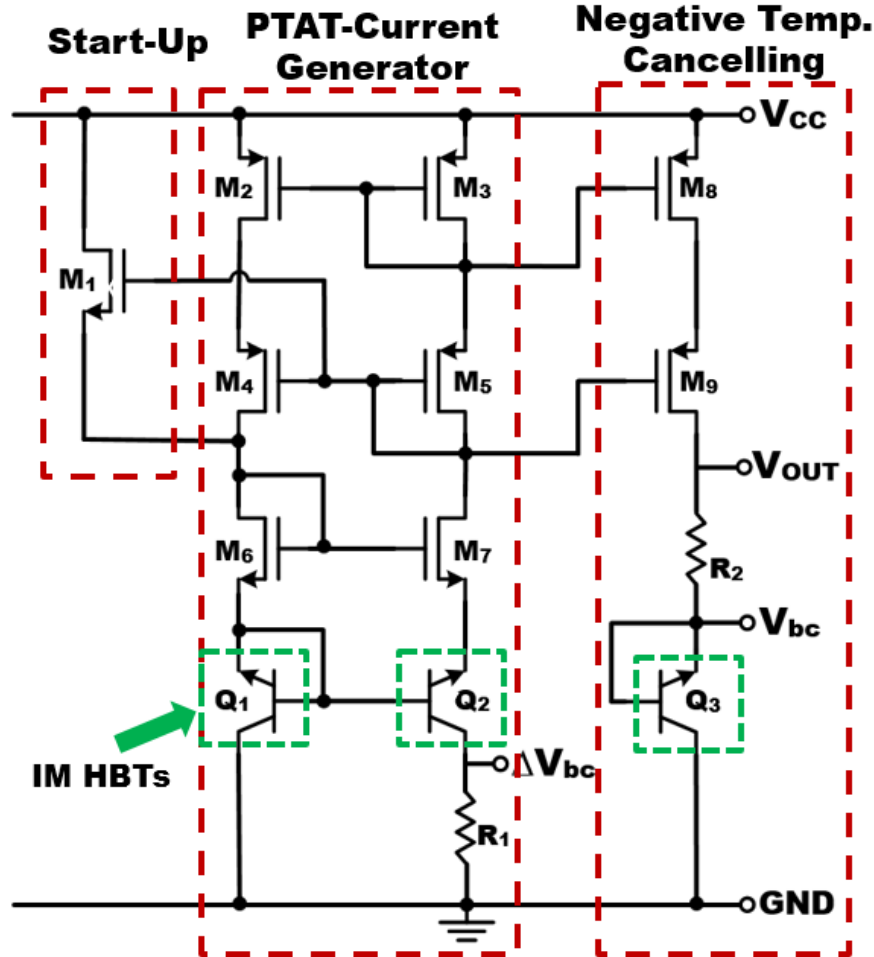


Figure 68. Schematic diagram of the Inverse-Mode 1st-order voltage reference circuit (VRC).

The core circuit for the PIN VRC follows the same topology as the first-order VRC (schematic diagram is shown in Figure 69). However, in this circuit the PIN diodes D_1 and D_2 replace transistors Q_1 and Q_2 in the second stage, the PTAT-current generator branch. The PIN diodes are made of a P+/N junction; the fabrication steps are similar to the extrinsic base-collector junction of the SiGe HBT. The cathode contacts are made with an N+ reach-through that wraps around the entire periphery of the anode (P+) to provide a low-impedance path to the NS subcollector and minimize series resistance in the cathode. The NS subcollector is deep trench (DT)-isolated. The D_1 and D_2 PIN diode parameters (i.e., the cathode width, the anode width, length, and the number of anode fingers) along with the

R_1 and R_2 parameters were parametrically adjusted to achieve a simulated TC value that is comparable to the first-order and the IM VRCs. Both simulation and measurement results showed that the generated PTAT current using PIN diodes varies less with temperature in comparison to the SiGe HBT-based VRCs. For this circuit a first-order temperature compensation was not implemented for the purpose of minimizing the circuit complexity and to enable a direct radiation response comparison with the other two VRCs, the first-order and the IM VRCs. The main implication of this design choice is that the output voltage displays a PTAT slope that yields a higher TC. All three circuits were designed for operation with a power supply voltage of 2 V. The supply voltage was chosen to meet the circuit voltage headroom requirement since cascode current mirrors were implemented to improve the power supply rejection (i.e., the amount of noise from a power supply that a circuit or device can reject).

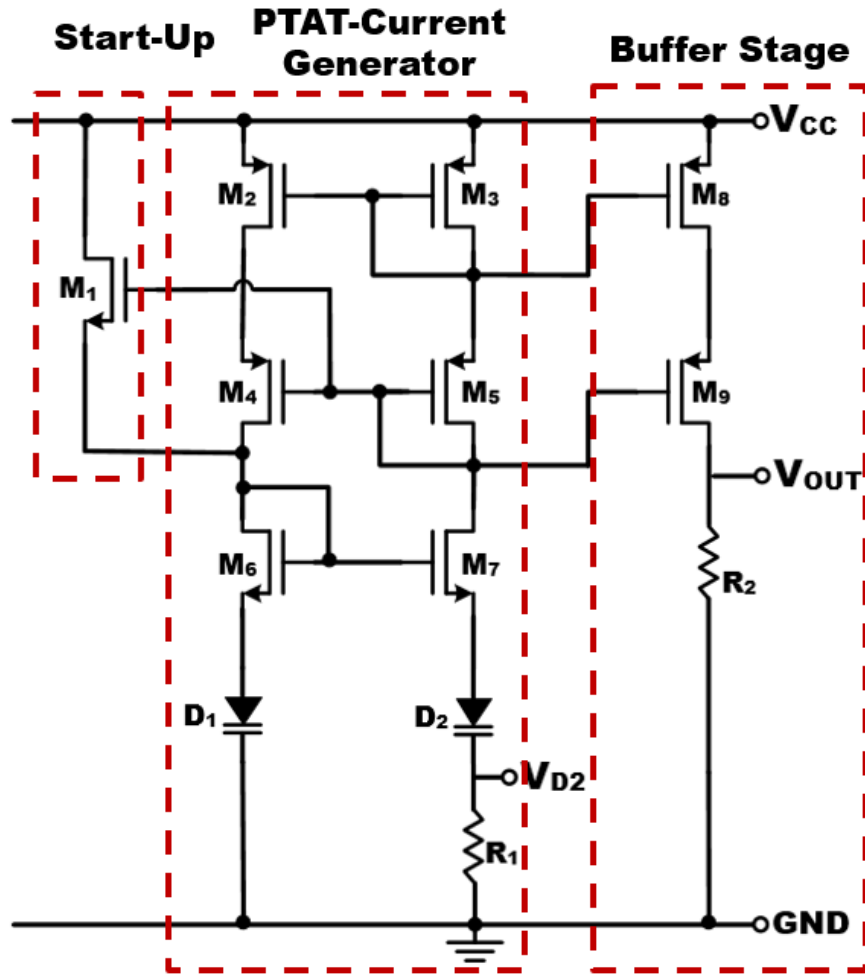


Figure 69. Schematic diagram of the PIN diode voltage reference circuit (VRC).

8.2 Experimental Details

Three different radiation experiments were performed. In the first experiment, SET measurements were conducted at the Naval Research Laboratory (NRL) using the two-photon absorption (TPA) backside pulsed laser system. This setup is identical to that reported in [10]. The system is capable of producing a $1.2 \mu\text{m}$ full-width half-maximum (FWHM) spot size diameter charge distribution profile [84]. The system provides the ability to perform 3-D position-dependent (XYZ) time-resolved SETs non-destructively in a laboratory setting. The TPA system was configured to produce optical pulses at 1260 nm at a frequency of 1 kHz, with a pulse width of approximately 120 fs. The laser-induced transient

waveforms were captured using a high-speed high-bandwidth Tektronix DPO71254 12.5 GHz, 50 GS/sec real time oscilloscope. The voltage reference circuits under test were packaged using a high-speed custom-designed printed circuit board (PCB). The translation platform used to secure the PCB has a 0.1 μm position resolution in all three axes, XYZ. All data were collected in a rectangular XY grid at a fixed Z position. For each measurement the Z position was optimized to place the sensitive volume at the focus of the laser beam. A detailed description of the measurement system can be found in [83].

For the second and third experiments, the total dose exposures were conducted at Vanderbilt University using an ARACOR 10-keV X-ray source and a 2 MeV Pelletron (proton) source. For the 10-keV X-ray experiments, the samples were mounted on 28-pin ceramic dual-in-line packages and irradiated at a dose rate of 31.5 $\text{krad}(\text{SiO}_2)/\text{min}$ or 525 $\text{rad}(\text{SiO}_2)/\text{s}$. The measured equivalent total dose for the 10-keV X-ray experiment started at 100 $\text{krad}(\text{SiO}_2)$ and was incrementally increased to a final value of 6 $\text{Mrad}(\text{SiO}_2)$. For the low energy proton irradiation, the samples were packaged using the same high-speed custom-designed printed circuit board as used in the SET experiments. The samples were irradiated at various total dose levels, starting at 33 $\text{krad}(\text{Si})$ (proton fluence of 4.92×10^{10} p/cm^2), to a TID of 2 $\text{Mrad}(\text{Si})$ (proton fluence of 1.97×10^{12} p/cm^2). The voltages and current biasing were monitored and measured in-situ using Keithley dc supplies and Agilent digital multimeters. For all three experiments, the samples were irradiated at room temperature under normal operating conditions. For both TID experiments, a total of 6 samples were irradiated and measured (i.e., two of each VRC).

8.3 Results and Discussion

8.3.1 SET VRC Response

All of the circuits and devices were characterized before irradiation. The measured pre-irradiation output voltages for all three VRCs are shown in Figure 70. All three VRCs demonstrate acceptable performance across temperature. As previously stated, temperature compensation was not implemented for the PIN diode VRC. The impact of this design

choice is observed in Figure 70 (closed triangle symbols); the output voltage decreases with decreasing temperature ($< 0^{\circ}\text{C}$). The data presented here are for one of the packaged samples; these are representative of the data set measured across all the samples.

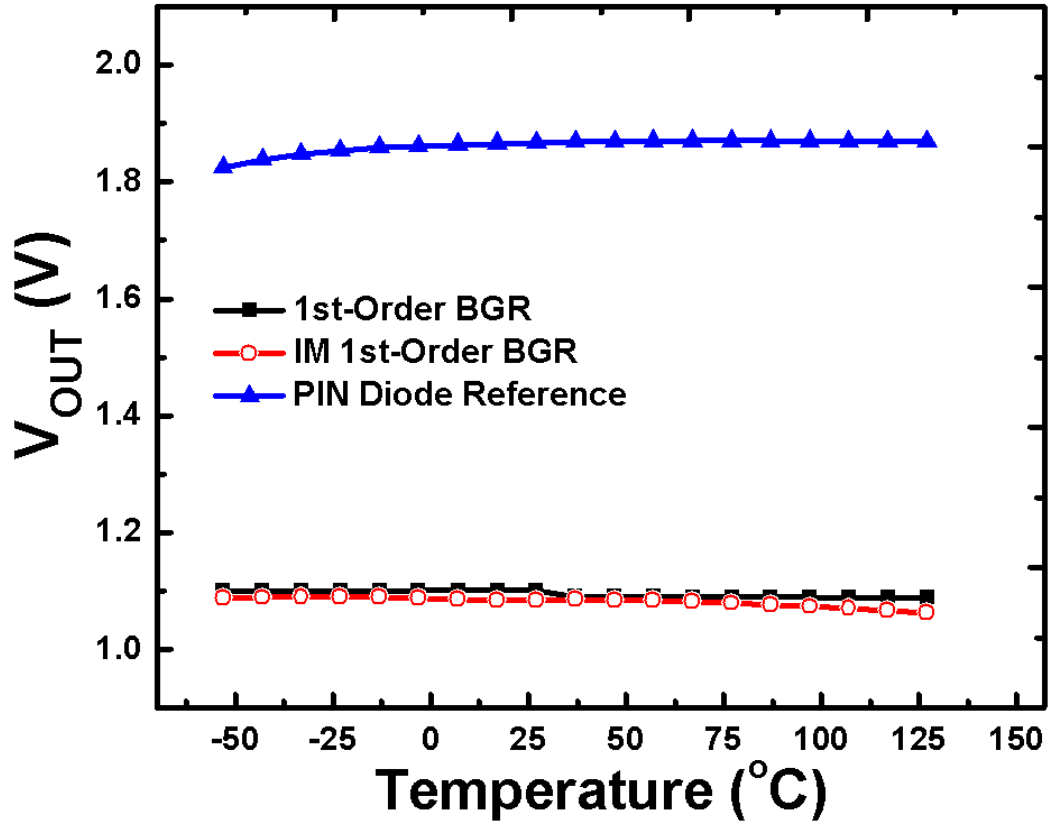


Figure 70. Output voltage as a function of temperature for the three voltage reference circuits: 1st-order BGR, IM 1st-order BGR, and PIN diode voltage reference.

To investigate SETs in the VRCs, the TPA system was used to perform 2-D raster scans on all of the devices while monitoring the key nodes in the circuits, V_{CC} and V_{OUT} , and also two internal nodes V_{BE} and ΔV_{BE} for the first-order BGR, V_{BC} and ΔV_{BC} for the IM BGR, and V_{D2} for the PIN VRC. Sensitive devices responsible for generating transients with large peak magnitudes and duration were identified. The recorded peak currents and the corresponding collected charge at the output terminal V_{OUT} as a function of the incident laser position is illustrated in Figures 71. The most sensitive devices were determined after initial raster scans on all non-FET devices. For both the first-order and IM BGRs, the raster

scans revealed that the most sensitive device is Q_2 . Q_2 consists of three parallel copies of Q_1 with an emitter area of (A_E) $0.1 \times 2 \mu\text{m}^2$. For some of the raster scans the sensitive areas appear larger than the actual device geometry. This discrepancy likely arises from the large pulse irradiance used for this set of experiments coupled with the finite spot size of the laser pulse. The apparent size of the sensitive area is a consequence of the overlap of the tails of the Gaussian laser pulse profile with the sensitive region of the devices [34].

The measured peak transient currents (in top row) and collected charge (in bottom row) at the V_{OUT} terminal as a function of position resulting from a laser strike on first-order BGR circuit Q_2 transistor (Figure 71(a)), inverse-mode BGR circuit Q_2 transistor (Figure 71(b)), and D_2 device in the PIN diode voltage reference circuit (Figure 71(c)), for an incident laser energy of 31 pJ are shown in Figures 71. As anticipated, the first-order BGR demonstrated greater sensitivity in its SET response (Figures 71(a)) when compared to the IM BGR and the PIN diode VRC, as shown in Figures 71(b) and (c), respectively. From these results, a worst-case transient peak current of ≈ 0.2 mA and a corresponding collected charge of ≈ 400 pC at the V_{OUT} terminal (Figures 71(a)) were measured. The captured transients at the V_{CC} terminal (not shown here) follow an identical response as the ones recorded for the V_{OUT} terminal, with the only difference being the opposite polarity of the transients and collected charge. Figures 71(b) depicts the measured 2-D raster scan response of the IM BGR. The results indicate a significant reduction of the total sensitive area as seen by the decrease in the transient peaks and the corresponding collected charge when compared to the first-order BGR response.

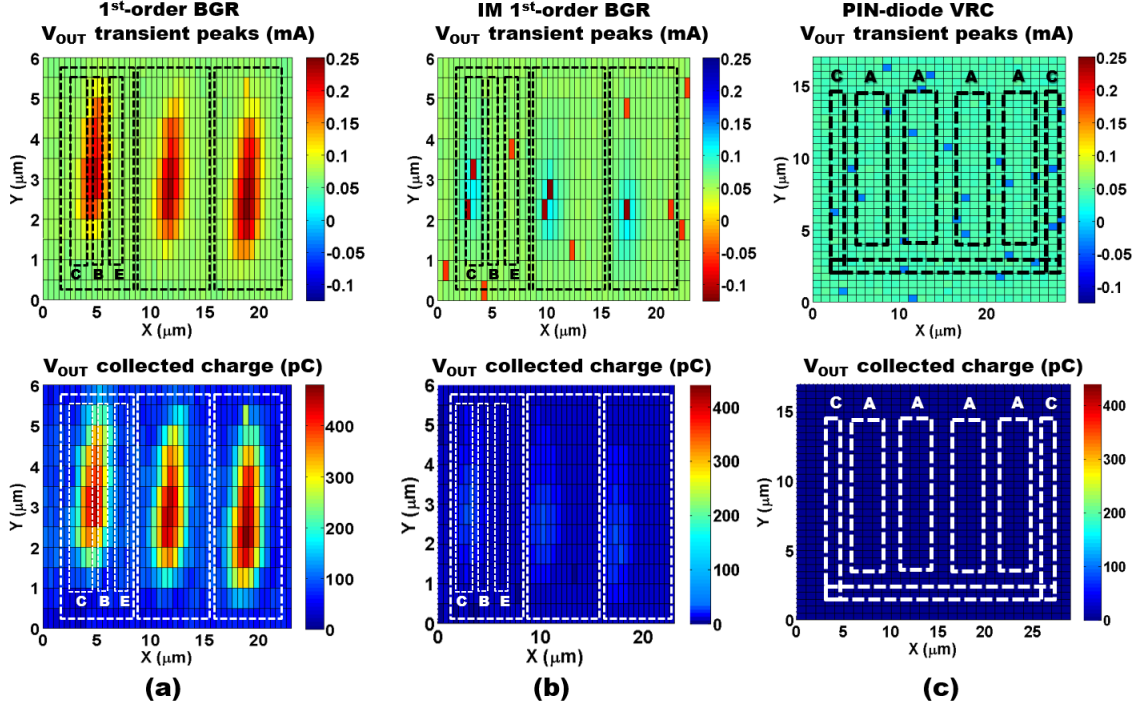


Figure 71. Measured peak transient currents (in top row) and collected charge (in bottom row) at the V_{OUT} terminal as a function of position resulting from a laser strike on (a) first-order BGR circuit Q_2 transistor, (b) inverse-mode BGR circuit Q_2 transistor and (c) D_2 device in the PIN diode voltage reference circuit, for an incident laser energy of 31 pJ.

The time-resolved transients at similar X-Y positions are shown in Figures 72 and 73 for both the first-order and the IM BGRs, respectively. These two figures provide additional information that cannot be ascertained simply from 2-D raster scan responses (shown in Figure 71). The results reveal that the measured peak transient current at the V_{OUT} and V_{CC} terminals of the IM BGR (Figure 73(a)) is reduced by approximately 0.1 mA in magnitude, when compared to the first-order BGR. The transient duration for the first-order and IM BGRs are also plotted in Figures 72(b) and 73(b), respectively. From these two plots the full-width at half-maximum (FWHM) duration were extracted from the measured transient signals at the V_{OUT} terminal for both first-order and IM BGRs, and the values were ≈ 600 ns and ≈ 0.7 ns, respectively. The FWHM duration decreases by approximately three orders of magnitude. These results confirm that the proposed IM circuit-level RHBD technique

can be used for SET mitigation on this type of ubiquitous analog circuit.

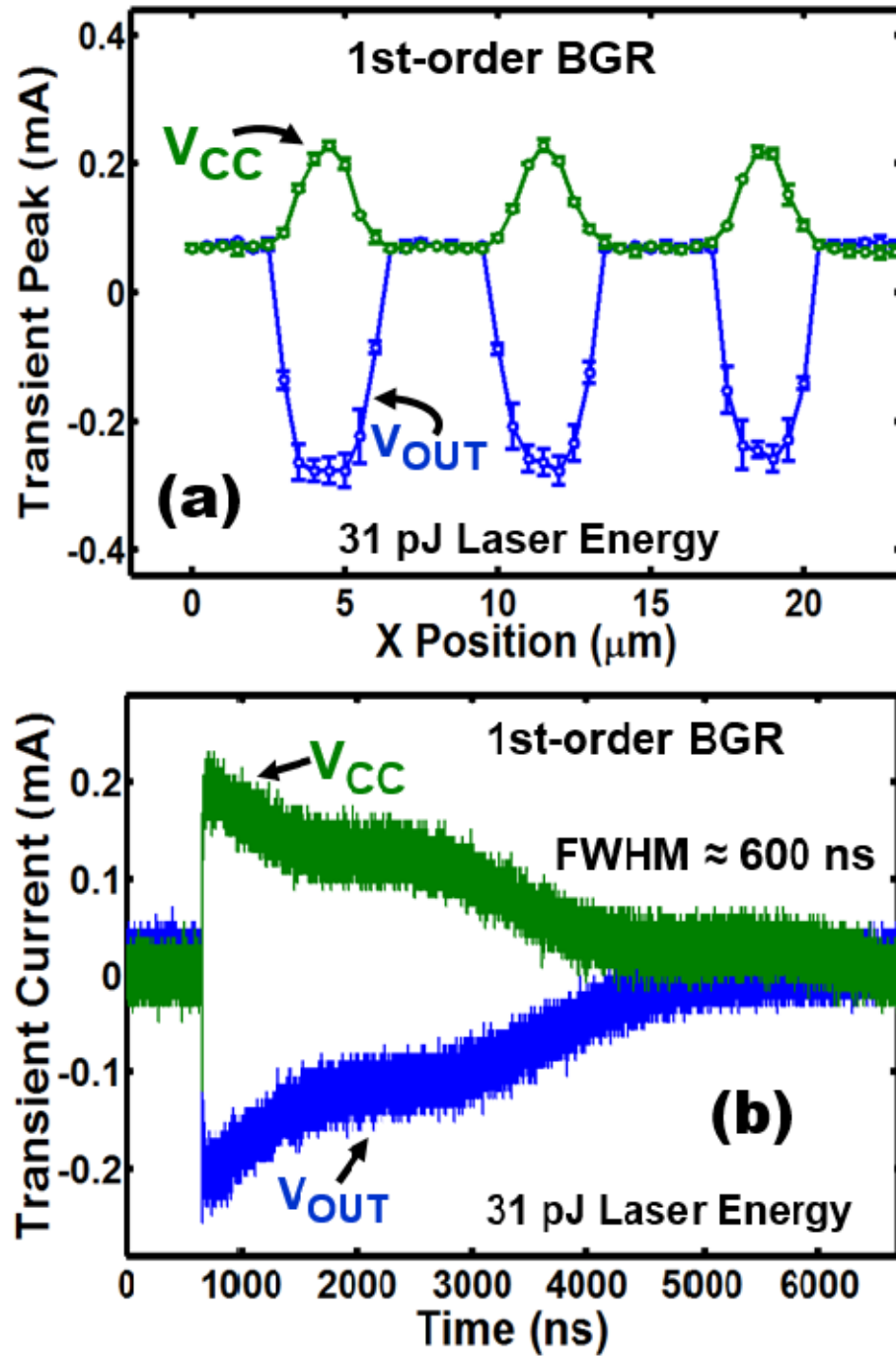


Figure 72. First-order BGR (a) transient peaks over the width of the device and (b) transient current of the resulting transient captured at the V_{OUT} and V_{CC} terminals from laser strikes on Q_2 (SiGe HBT), with an incident laser pulse energy of 31 pJ.

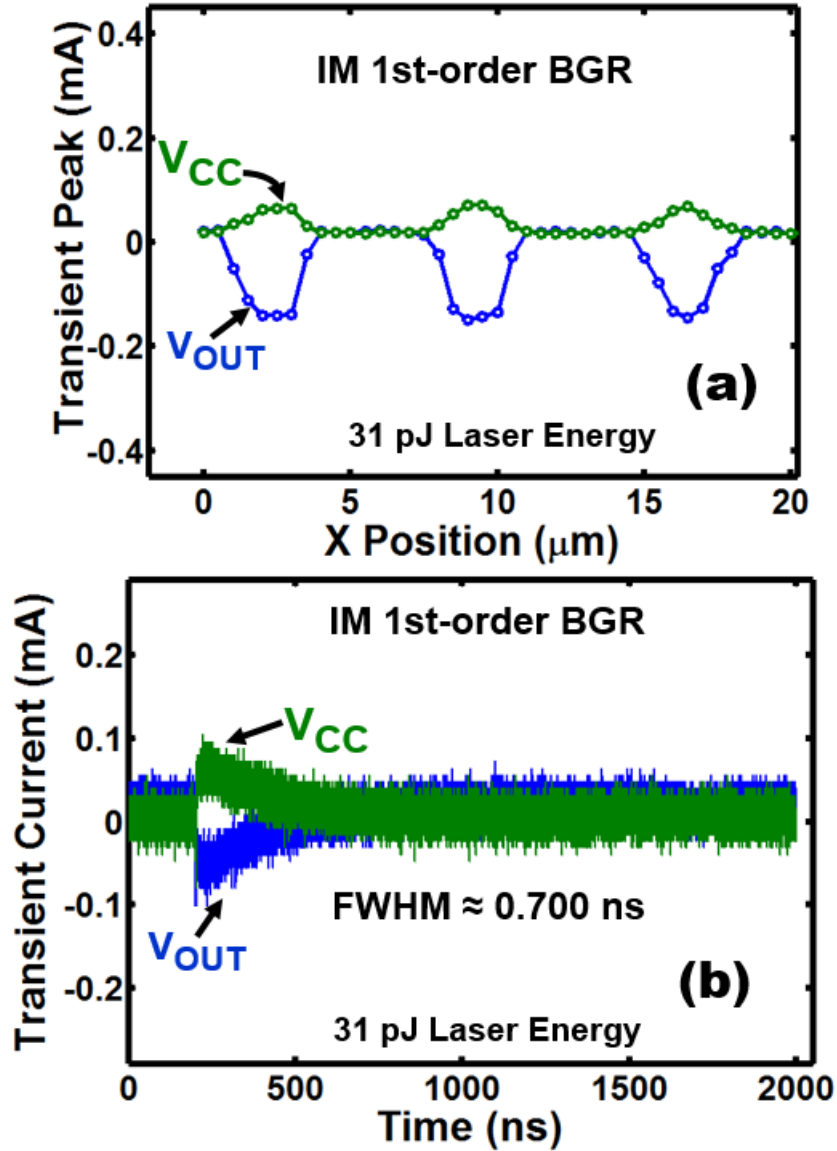


Figure 73. Inverse-Mode (IM) first-order BGR (a) transient peaks over the width of the device and (b) transient current of the resulting transient captured at the V_{OUT} and V_{CC} terminals from laser strikes on Q_2 (SiGe HBT), with an incident laser pulse energy of 31 pJ.

The observed decrease in transient peak current, transient duration, and collected charge occurs because the electrical collector (physical emitter) of the IM SiGe HBTs are electrically isolated from the sensitive subcollector-substrate junction [98]. This isolation leads to a reduction in the ion-shunt region (two linked junctions due to high-injection concentrations of excess carriers) since the electrical collector current is no longer a superposition

of the emitter-collector ion-shunt and substrate diffusion current, thus reducing the overall transient peaks magnitude and the reduction in transient duration at sensitive circuit nodes [26]. The reduction in total transient duration is attributed to both the absence of the subcollector-substrate diffusion tail and the ion-shunt region as described in [26,98]. [26] provides an in-depth study of the contributions related to the oxide trapped charge and the interface traps in the shallow trench isolation (STI) for both forward- and inverse-mode SiGe HBTs fabricated in 90 nm SiGe BiCMOS process.

The 2-D raster scan response from laser strikes on diode D_2 of the PIN VRC is shown in Figure 71(c), and no transients are observed at either the V_{OUT} or V_{CC} terminals. The measured collected charge at V_{OUT} are < 0.2 pC, a calculated value that is within the noise floor capability of the measurement equipment (Tektronix oscilloscope). Current transients of ≈ 0.2 mA in magnitude were captured at the cathode terminal V_{D2} (not shown here) as 2-D raster scans were performed. However, it was determined that the observed transient signals do not propagate to the V_{OUT} and V_{CC} terminals because the PIN diode is forward biased. Under this bias condition, only a small amount of charge is collected at the anode terminal from the laser strikes due to the small electric field present that limits the charge separation. Thus, any electron-hole pairs generated from the laser strike quickly recombine in the space charge region and charge collection is minimized at the anode. In addition, charge collection at the anode is further minimized because the P+ region is DT-isolated.

Also, Cadence simulations confirm that the PIN diode is forward-biased with ≈ 0.8 V and ≈ 70 μ A across the device. Under this bias condition the PIN diode presents a large resistance at the source of nFET transistor M_7 (Figure 69). The parasitic capacitances from the nFET transistor and the PIN diode, along with this large resistance, act as a filter for the transients resulting from laser strikes on D_2 . A total of 4 samples were exposed for two separate experiments, and the results reveal that this VRC is insensitive to SETs, clearly an important result. The proposed RHBD approach using PIN diodes instead of IM SiGe HBTs provides complete immunity to SETs at the circuit level.

8.3.2 TID VRC Response

The results from 10-keV X-ray and 2 MeV proton irradiation of the first-order BGR are shown in Figures 74(a) and (b), respectively. As previously reported in [88], the TID response of the first-order BGR is radiation source dependent. The measured data indicate that total dose effects are minor for these circuits, and that higher output voltage changes are observed for the samples exposed to X-rays. The first-order BGR V_{OUT} shows a worst-case change of about 2.5% (≈ 28 mV). The primary reason for the change in V_{OUT} is the excess base leakage current generated in the SiGe HBTs. This excess base leakage current is demonstrated by the observed trends of the measured V_{BE} and ΔV_{BE} voltages shown as open circle and open triangle symbols in Figure 74(a), respectively. This increase in base current is due to radiation-induced G/R traps located at the EB oxide spacer [100]. The base current increase was also verified by performing pre- and post-irradiation dc characterization of individual transistors with similar A_E and at similar operating bias points as the devices in the VRCs (data not shown here for brevity).

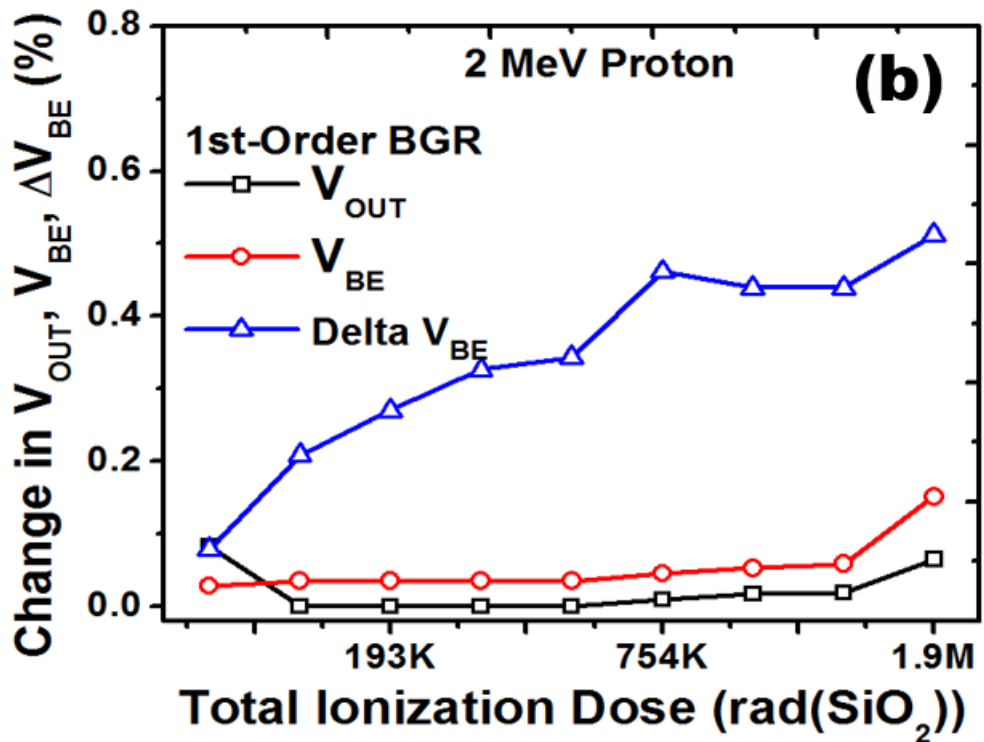
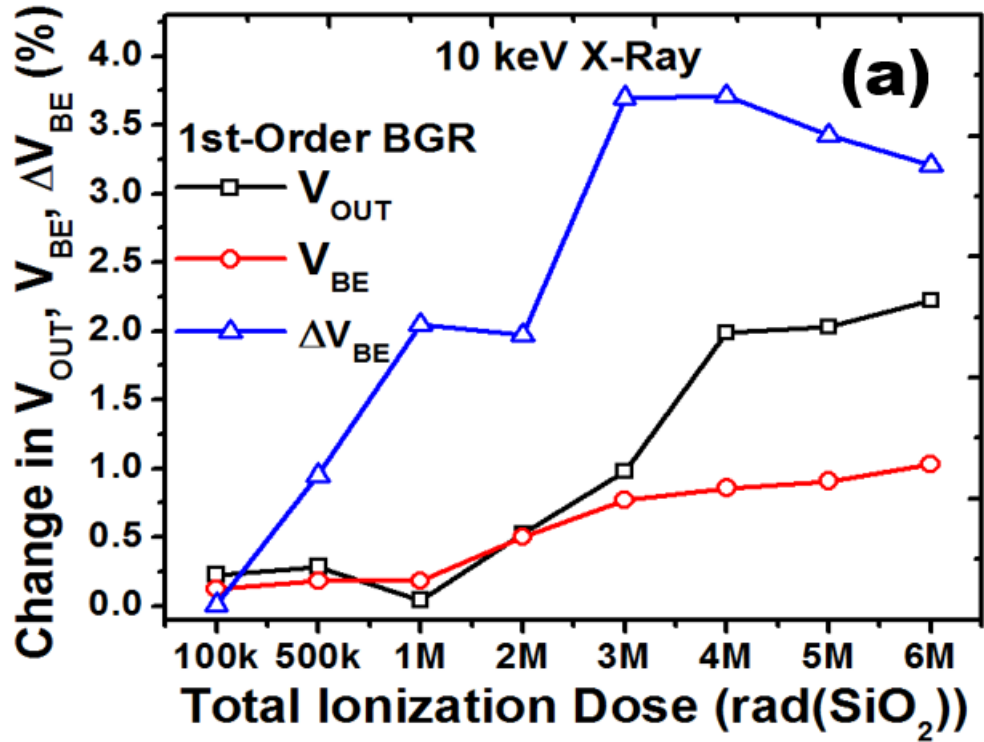


Figure 74. Change in the output voltage, V_{OUT} , base-emitter voltage V_{BE} of Q_3 , and ΔV_{BE} of Q_3 inside first-order BGR irradiated at room temperature as a function of total accumulated dose for samples after a) X-ray irradiation, (b) 2 MeV proton irradiation.

For the 2 MeV proton irradiation the observed changes are less than 0.1%. These results are consistent with the measured forward Gummel characteristics (data not shown here for brevity). The radiation source dependency can be attributed to fundamental differences in the local recombination rates in the emitter-base and STI interface regions [101]. Standalone test structures confirm that for a V_{BE} bias voltage of ≈ 0.8 V the change in base current is minimal with increased proton irradiation dose.

IM BGRs were irradiated under similar conditions as the first-order BGR and the results are shown in Figure 75 (open circle symbols). Similar to first-order, the IM BGR exhibits worst case V_{OUT} change for the samples exposed to X-rays as shown in Figure 75(a) (open circle symbols). The V_{OUT} terminal shows an average change of $\approx 1.5\%$ as total dose increased to 6 Mrad(SiO_2). This approximate change is attributed to a small increase in the base current of the SiGe HBT with increased TID. The inverse Gummel results of irradiated standalone IM SiGe HBTs confirms that the base current for a V_{BC} bias voltage of ≈ 0.8 V displays very small changes (from ≈ 250 pA to ≈ 380 pA) with increased dose, thus the nearly constant BGR output percentage change. The 2 MeV proton measured response for the IM BGR shown in Figure 75(b) (open circle symbols) reveals that the change in V_{OUT} is less than 1% at a total dose of 1.9 Mrad(SiO_2). The change in V_{OUT} displays an increasing trend with increased total dose. This may result from the fact that both ΔV_{BC} and V_{BC} increase with dose, according to the measured data not shown here. The base-collector voltage ΔV_{BC} of transistor Q_2 is related to the PTAT current, which is then mirrored to the output stage for negative temperature compensation. Therefore, any significant change in the PTAT current affects the BGR output voltage.

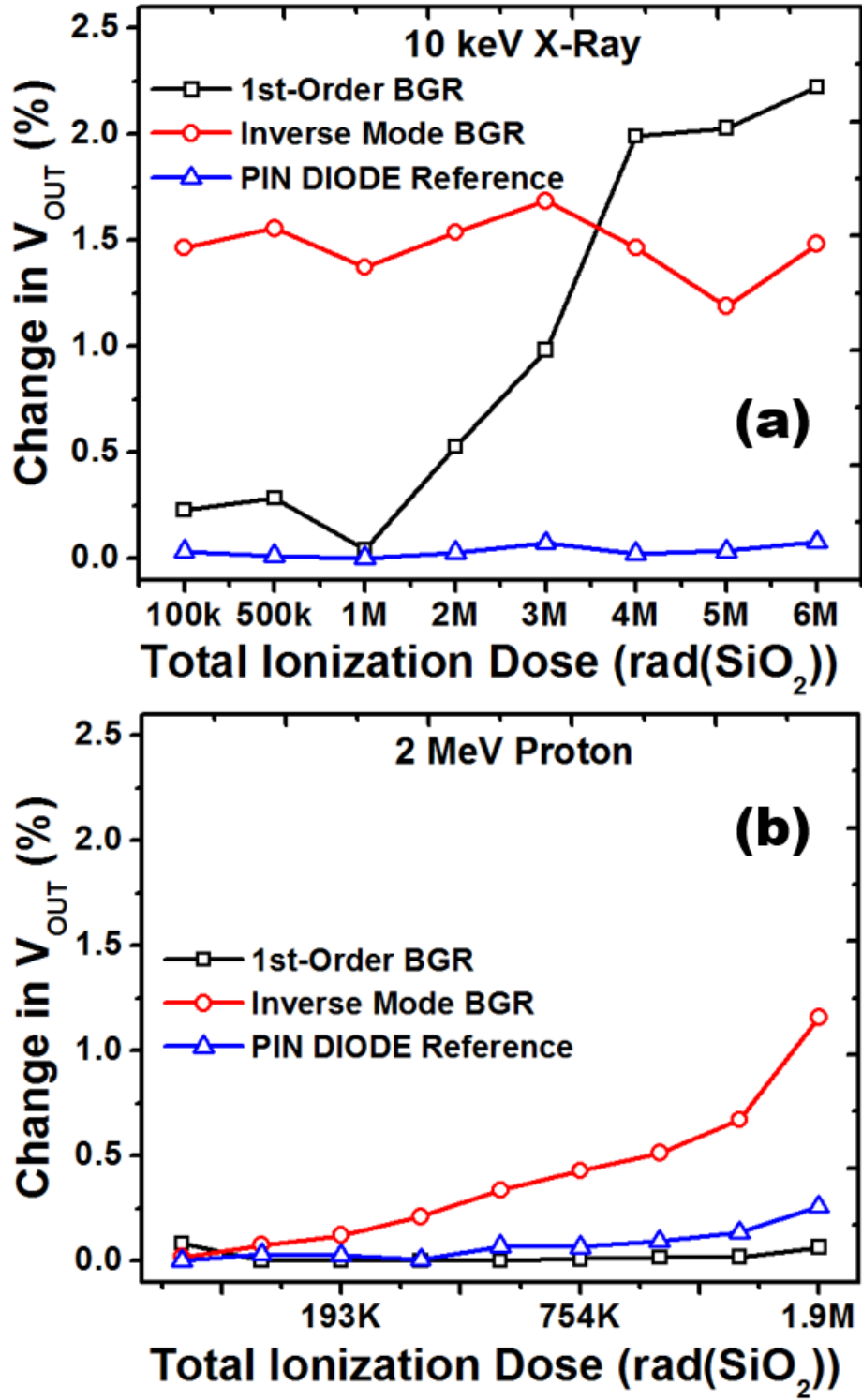


Figure 75. Voltage reference circuits comparison plotted as functions of total dose and change in V_{OUT} for (a) X-ray irradiation and (b) 2 MeV proton irradiation.

The measured change in V_{OUT} for the PIN diode VRC as a function of TID for both X-ray and proton is shown in Figures 75(a) and (b) (open triangle symbols), respectively. The maximum measured change in V_{OUT} for both irradiation experiments is $\approx 0.25\%$. This percentage change satisfies the majority of applications that require robust bias circuitry (e.g., DACs and ADCs). To understand why the PIN diode VRC demonstrates an overall better response to TID in comparison to first-order and IM BGRs, stand-alone PIN diode device structures of similar size and using same bias conditions as in the VRCs were irradiated. The measured results at different total doses are illustrated in Figure 76. Both X-ray (Figure 76(a)) and proton (Figure 76(b)) results confirm that the change in diode current for a V_{AC} bias at ≈ 0.8 V is minimal, and thus the impact on the VRC output is insignificant.

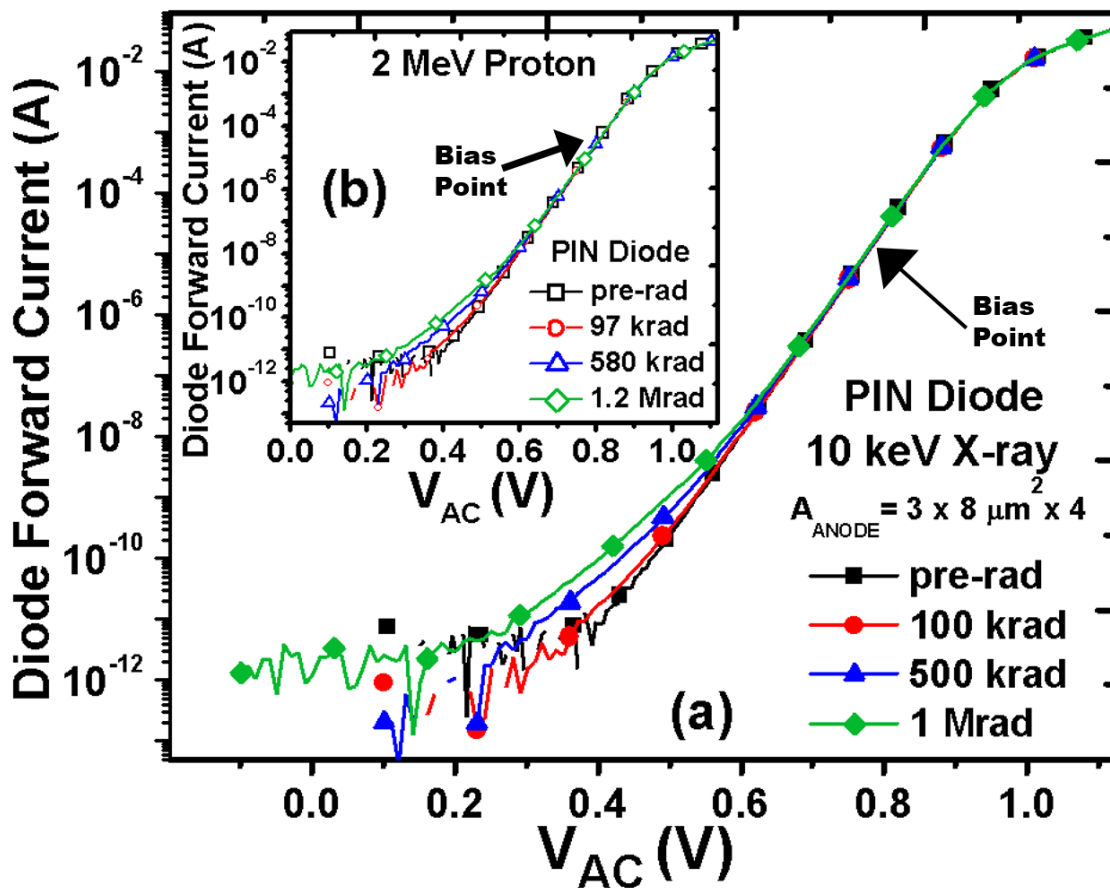


Figure 76. Measured PIN diode transfer characteristics as a function of total accumulated dose for standalone samples after (a) X-ray irradiation and (b) 2 MeV proton irradiation. The same bias conditions were used for the PIN diodes during irradiation, V_{AC} of ≈ 0.8 V.

The change in V_{OUT} comparison between the three VRCs for both X-ray and proton experiments is shown in Figures 75(a) and (b), respectively. Since the X-ray source yielded the worst-case VRC performance degradation, the VRCs were characterized before and after X-ray irradiation from $-53\text{ }^{\circ}\text{C}$ to $127\text{ }^{\circ}\text{C}$ at equivalent total dose level of $6\text{ Mrad}(\text{SiO}_2)$. The measured dc performance of the VRCs is summarized in Table 5. The results confirm that both proposed RHBD approaches improve the circuit robustness to TID when compared to the non-RHBD first-order BGR. The percentage change of the VRCs TC is also calculated and included in Table 5. The TC value is measured in parts per million per degree Celsius (ppm/ $^{\circ}\text{C}$) and is one of the most important specifications for a VRC, since it measures how much the VRC output voltage changes for a given temperature range. According to the values shown in the table, the TC value implies that the IM BGR is more robust to TID exposure than the PIN VRC. However, as previously stated in section 8.1, unlike the first-order and IM BGRs, the PIN diode VRC does not incorporate any temperature compensation technique. Therefore, when comparing the respective calculated TC values this fact needs to be taken in consideration. The post-irradiation data present in this table only include X-ray data since it yielded the worst-case VRC performance degradation.

Table 5. Measured dc performance comparison of the voltage reference circuits (VRCs) for the X-ray irradiation.

Reference Voltage Circuit	V_{OUT} (V) @ $27\text{ }^{\circ}\text{C}$			I_{CC} (μA) @ $27\text{ }^{\circ}\text{C}$			Temp. Coefficient (ppm/ $^{\circ}\text{C}$)		
	Simulation	Measured		Simulation	Measured		Measured ($-53:127\text{ }^{\circ}\text{C}$)		
		pre-rad	post-rad*		pre-rad	post-rad*	pre-rad	post-rad*	% Δ
First-order BGR	1.079	1.083	1.008	332	320	565	24	189	155
Inverse-Mode (IM) BGR	1.064	1.061	1.088	319	278	310	43	64	39
PIN Diode	1.858	1.855	1.863	85	69.5	73	67	174	88

*Post-rad data are for 10 keV X-ray exposure at equivalent total dose level of 6 Mrad (SiO_2).

8.4 Summary

SET and TID experiments were performed on first-order BGR circuits designed in a 4th-generation 90 nm SiGe BiCMOS technology. The results presented in this chapter confirm that SiGe-based BGR circuits are sensitive to SET, but the circuits demonstrate minimal degradation to TID exposure. Based on first-order circuit results, circuit-level RHBD techniques using IM SiGe HBTs and a PIN diode VRC as potential RHBD strategies were presented. The extracted FWHM transient duration at the V_{OUT} node for the IM BGRs decrease by approximately three orders of magnitude when compared to the first-order BGR, 600 ns and 0.7 ns, respectively. A decrease in transient peak, transient duration, and collected charge was observed. This occurs because the electrical collector (physical emitter) of the IM SiGe HBTs are electrically isolated from the sensitive subcollector-substrate junction. These results are significant, as it confirms that the proposed IM circuit-level RHBD technique can be used for SET mitigation on this type of an ubiquitous analog circuit without increasing the TID sensitivity.

For the PIN VRC no transients were observed when 2-D raster scans were performed from laser strikes on diode D_2 . Transients were not observed at the V_{OUT} terminal of the PIN diode VRC because: 1) charge collection at the anode is minimized because the P+ region (anode) is DT-isolated; the forward-biased diode limits charge separation and reduces charge collection at the sensitive node (source of nFET transistor M_7); and 2) any transients at this sensitive node are potentially filtered out because the large resistance from the PIN diode along with the parasitic capacitances of nFET M_7 and diode M_7 form an RC low pass filter. The proposed PIN diode RHBD approach demonstrates a higher degree of immunity to SETs at the circuit level, in comparison to the first proposed RHBD approach that uses IM SiGe HBTs.

The 10-keV X-ray and 2 MeV proton irradiation experiments confirm that both the first-order and IM BGRs have radiation-source dependence. The X-ray source yielded the worst-case changes at the V_{OUT} terminal. At a TID of 6 Mrad(SiO_2) the largest observed

changes at V_{OUT} are $\approx 2.2\%$, $\approx 1.5\%$, $< 0.25\%$ for the first-order, the IM BGR, and the PIN diode BGR, respectively. Since the X-ray source yielded the worst-case VRC performance degradation, the VRCs were characterized over-temperature pre- and post-irradiation (TID of 6 Mrad(SiO_2)). The calculated TC value implies that the IM BGR is more robust than the PIN VRC to TID exposure.

CHAPTER 9

ON THE CRYOGENIC RF LINEARITY OF SIGE HBTs IN A 4TH GENERATION SIGE BICMOS TECHNOLOGY

SiGe HBT performance (i.e., *dc*, *ac*, noise, and reliability) has been demonstrated to improve with cooling [94, 102, 103]. Recent work has reported record performance of SiGe HBTs at cryogenic temperatures (e.g., $f_T >$ half-terahertz [50], [51], and peak f_{MAX} of 0.8 terahertz [49]). In addition, several recent studies on the cryogenic performance of SiGe HBT-based integrated circuits (ICs) have been published (e.g., an X-band LNA [46], a K-band power amplifier (PA) [47], a bandgap voltage reference [48]). These circuit demonstrations and studies further support the potential of SiGe HBTs for high-performance and high-frequency cryogenic applications. The cryogenic electronics market continues to grow, and the range of applications has increased. Some of these applications range from space-based electronics (e.g., satellite systems, high-precision instrumentation and detector electronics for deep-space and planetary space missions), commercial applications (e.g., pre-amplifiers for cell-phone base stations that are cooled to improve the signal-to-noise ratio [4]), to biological/medical applications (e.g., medical instrumentations and sensors), and interface circuitry for quantum computing.

To the best of the author's knowledge, only two reported works have attempted to investigate the RF linearity of SiGe HBTs at cryogenic temperatures [104], [105]. Both of these studies focused on the output power (P_{OUT}) and the adjacent channel power ratio (ACPR) as figures-of-merit for linearity. The most widely used figures-of-merit for RF linearity are the power at the 1-dB compression point, P_{1dB} (large-signal), and the third-order intercept, TOI (small-signal). TOI is expressed as either the input- (IIP3) or output-referred third-order intercept point (OIP3). P_{1dB} indicates the input power level (P_{IN}) that causes the small-signal gain (i.e., S_{21}) at a set frequency to drop by 1 dB. OIP3 (or IIP3) is the extrapolated point where the fundamental tone and the third-order distortion product intersect

for a given frequency.

The present chapter investigates both the large-signal (P_{1dB}) and small-signal (OIP3) response of SiGe HBTs at cryogenic temperatures in a new state-of-art, fourth-generation, SiGe BiCMOS technology [13]. The linearity response of two different SiGe HBT layout variants, CBE (collector-base-emitter) and CBEB (collector-base-emitter-base-collector) are presented and compared here. Analyses of both large- and small-signal linearity response of individual transistors are important to understand the factors that limit the power-handling capability of this new technology, and to assess if the layout configuration (i.e., contact stripes) can potentially impact the linearity performance of the devices at low temperatures [13]. This information will provide system architects and circuit designers with a better understanding of how system operation can be influenced by cryogenic temperatures and, more importantly, how to potentially leverage the circuit response to meet the ever-growing stringent system specification requirements.

9.1 Device Technology

The SiGe HBTs used in this study are from a new state-of-the-art 90 nm SiGe BiCMOS platform (IBM 9HP). The details of the device structure and the fabrication process for this new technology are presented in [95]. However, a brief description of the technology is included here to provide insight into the measured cryogenic performance. This platform integrates 90 nm RF-CMOS and 90 nm SiGe NPN HBTs. The SiGe HBT has a target f_T/f_{MAX} of 300/350 GHz and an advanced BEOL, which includes a full suite of radio frequency (RF) and mm-wave passive elements. The SiGe HBT structure was fundamentally changed from its predecessors. Optimization of both the lateral and vertical profiles were made to improve the transistor performance. Some of the changes made include a larger Ge mole fraction, thinner base and collector profile, and a new device structure that minimizes parasitics associated with the collector-base junction [100]. All of these process changes ensure that low emitter resistance is maintained with scaling. Innovative process changes

were employed to ensure clean interfaces are achieved in the emitter/base and poly emitter/tungsten plug region [95]. The 9HP technology offers both high performance (HP) and medium breakdown (MB) vertical NPN SiGe HBT in both CBEBC and CBE configurations. All data presented here are for HP devices. The same emitter area, A_E of $0.1 \times 6.0 \mu\text{m}^2$ was used in this study for both configurations. All SiGe HBTs test structures were characterized in a common-emitter (CE) mode. The exception was specific *dc* measurements that required common-base biasing (i.e., the avalanche multiplication factor, M-1).

9.2 Experimental Details

The *dc* and RF measurements of SiGe HBTs from 300 K down to 78 K were performed using a custom-designed, on-wafer, open-cycle liquid nitrogen (LN_2) probe station. The S-parameter measurement setup (displayed in dashed-lines in Figure 77) consists of a network analyzer, bias-tees, input and output tuner, Keithley 2400 source-measurement meters (SMU), and the on-wafer cryogenic dewar chamber. S-parameters were measured on-wafer to 50 GHz using an Agilent E8363B Network Analyzer (NA). Cable and probe losses were de-embedded using the Thru-Reflect-Line (TRL) calibration with an Impedance Standard Substrate (ISS) at each temperature. In addition, on-wafer “open” and “short” de-embedding test structures were measured to remove the parasitic impedances associated with the pads and wiring (i.e., those extrinsic to the device) from the measured S-parameters. The tuners were initialized to 50Ω impedance during the S-parameters measurements.

A screenshot of the Focus Microwaves software illustrating the cryogenic-temperature measurement setup is shown in Figure 77. The Focus Microwaves software was used to create the de-embedding files, to control the tuners, and to run the linearity measurements. For both single-tone (P_{1dB}) and two-tone linearity (OIP3) measurements, the setup included the following measurement equipment: two signal generators (Agilent HP83732A), two *dc* supplies (Keithley 2400 SMU), three isolators (Ditom model D3108), one combiner (Narda model 30183), two bias-tees (Anritsu model K251), one power meter (Agilent E4419), two

bi-directional couplers (Krytar model 2618), two Focus Microwaves programmable tuners (model CCMT-1818), and one spectrum analyzer (Agilent E4407B). The instruments and tuners were controlled using the Focus Microwaves Load-Pull Explorer software program. To ensure accurate power readings while performing the linearity measurements, calibration loss files were generated for the input and output paths using power flatness and multiple reference planes calibration techniques. Before running the linearity measurements, source- and load-pull were performed at each temperature at 8 GHz and 18 GHz using a constant input power, P_{IN} set to -20 dBm. However, for brevity, only the 8 GHz data are presented here. The source and load impedances were tuned for maximum P_{OUT} at each temperature: 300 K, 225 K, 150 K, 115 K and 78 K. A total of six samples were measured, three CBE and three CBEBC. The results presented here were reproducible over multiple measurements.

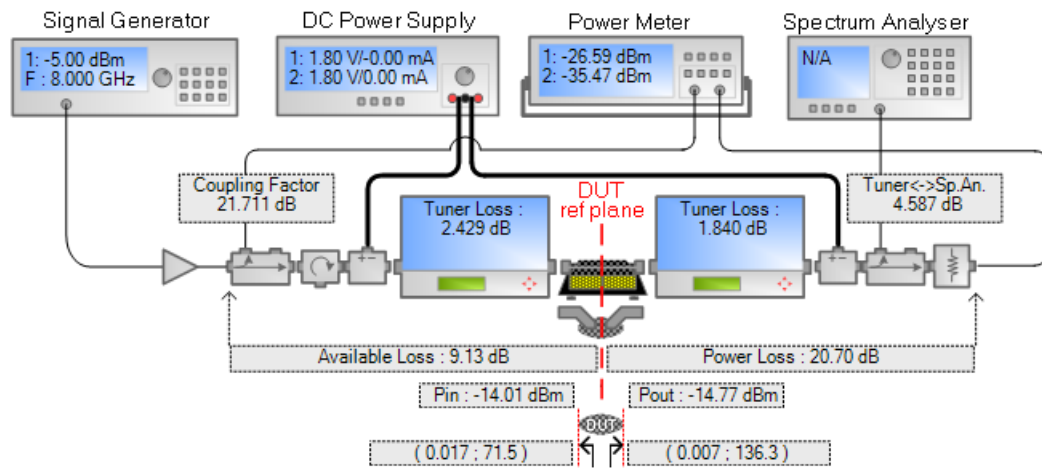


Figure 77. A screen capture of the characterization software showing the measurement block diagram of cryogenic test bench (Courtesy of Focus Microwaves).

9.3 Results and Discussion

9.3.1 SiGe HBT *ac* and *dc* Performance at Cryogenic Temperatures

Figures 78(a) and (b) depict the extracted peak f_T and f_{MAX} as a function of collector current density at 300 K and 78 K, using constant V_{CE} of 1.2 V for CBE and CBEBC devices,

respectively . The f_T and f_{MAX} values were extracted by extrapolating the measured small-signal current gain h_{21} and Mason's unilateral gain ($MUG^{1/2}$) for a frequency range of 15 GHz to 35 GHz. In this frequency range the measured data shows an ≈ 20 dB/dec roll-off. The peak f_T/f_{MAX} for CBE (Figure 78 (a)) and CBEBC (Figure 78 (b)) at 300 K is $\approx 277/264$ GHz and $303/290$ GHz, respectively. At 78 K the f_T/f_{MAX} peaks increase to $\approx 387/350$ GHz for the CBE, and $\approx 420/410$ GHz for the CBEBC.

The larger improvement in f_T/f_{MAX} for the CBEBC devices at cryogenic temperatures is attributed to the RC delay reduction and the symmetric spread of injected electrons at the collector region that helps to suppress the onset of Kirk effect [94, 106]. The extracted total forward transit time (emitter-to-collector delay, τ_{EC}) for both CBE and CBEBC is shown in Figure 78(c). τ_{EC} for CBEBC decreases from 0.42 ps at 300 K to 0.33 ps at 78 K, while for CBE it decreases from 0.45 ps at 300 K to 0.35 ps at 78 K. τ_{EC} values were extracted from the extrapolated y-intercept of $1/2\pi f_T$ vs $1/J_C$ as described in [49,94]. Based on [94], the decrease in base and emitter transit times is one of the main factors resulting in a higher f_T/f_{MAX} at low temperatures. The total emitter-base and collector-base depletion capacitance, C_{T-EC} (not shown here) also decreases with cooling. This reduction is due to the increase in junction built-in potentials as temperature decreases [15].

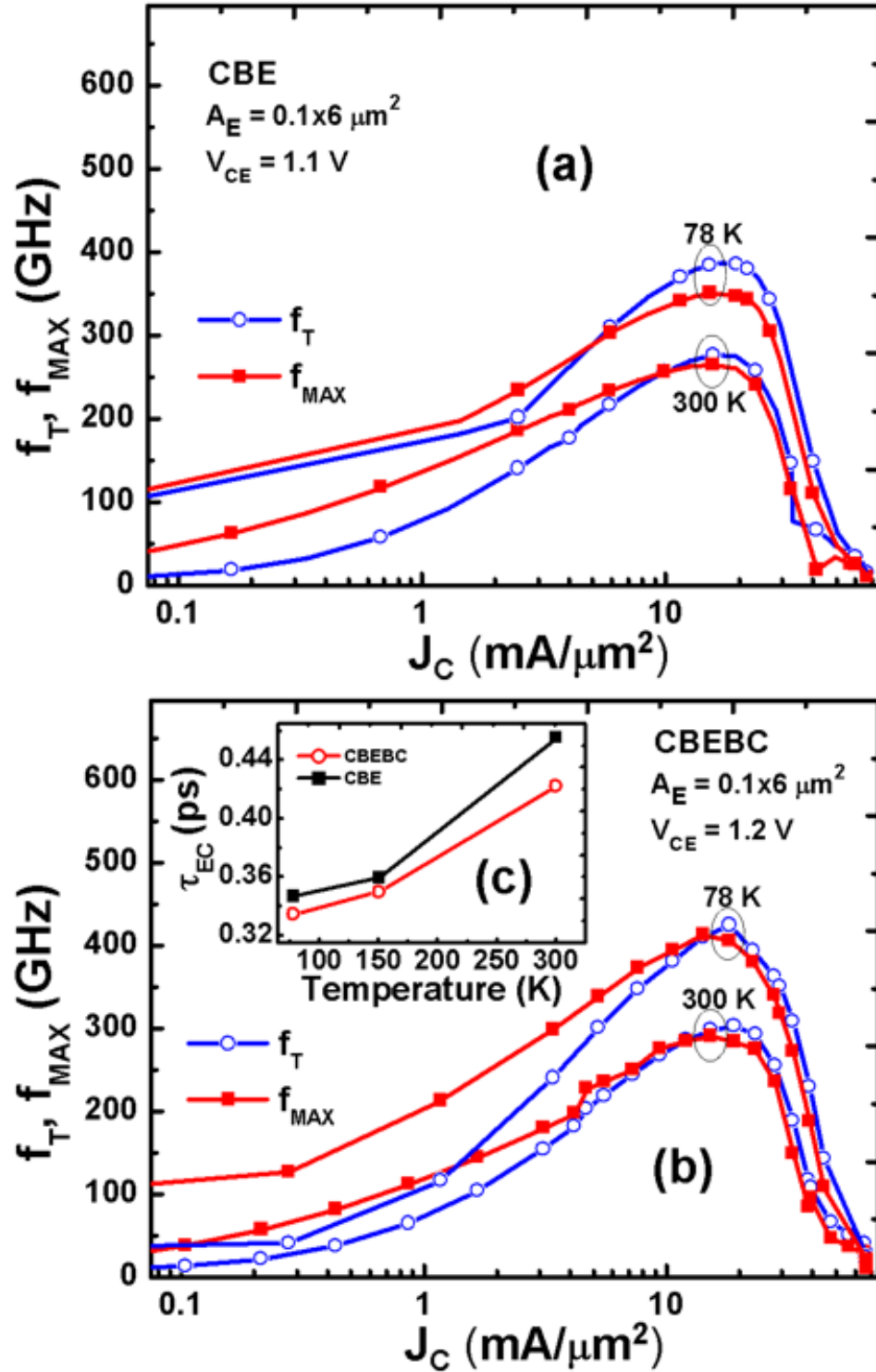


Figure 78. Extracted unity gain cutoff frequency, f_T and maximum oscillation frequency, f_{MAX} as a function of J_C at 300 K and 78 K for: (a) CBE and (b) CBEBC layout configuration. (c) Plot of the extracted total forward transit time (emitter-to-collector delay, τ_{EC}) as a function of temperature.

Both device configurations, CBE and CBEBC, showed reasonably ideal *dc* forward Gummel characteristics from 300 K down to 78 K. The changes to SiGe epitaxial growth and doping profile for this technology help to limit the emitter-base tunneling and recombination at low temperatures [15]. As anticipated, the peak *dc* current gain (β_{DC}) and transconductance (g_m) increase with decreased temperature (as shown in Figure 79), for both device configurations. At 300 K, the peak g_m and peak β_{DC} values are comparable, but with cooling the values diverge. At 78 K the CBE peak β_{DC} rises to $> 8,000$, while CBEBC peaks at $\approx 6,500$. The peak g_m at 78 K is higher for the CBEBC than CBE (460 mS compared to 435 mS). The observed differences in peak β_{DC} and g_m for CBE and CBEBC may be due to an increase in the intrinsic high-current effects and the extrinsic parasitic resistances from the two layout configurations at these low temperatures. Carrier freeze-out is insignificant in these devices because the emitter and base regions are doped above the Mott-transition. The *dc* and *ac* figures-of-merit at 300 K and 78 K are summarized in Table 6 for both configurations. Table 6 shows the extracted r_{bb} values for CBE and CBEBC, and they decrease with cooling. The CBEBC values are lower than those for CBE since the layout reduces the intrinsic and extrinsic base resistance when compared to the CBE configuration. The impedance-circle technique described in [94] was used for the r_{bb} extraction.

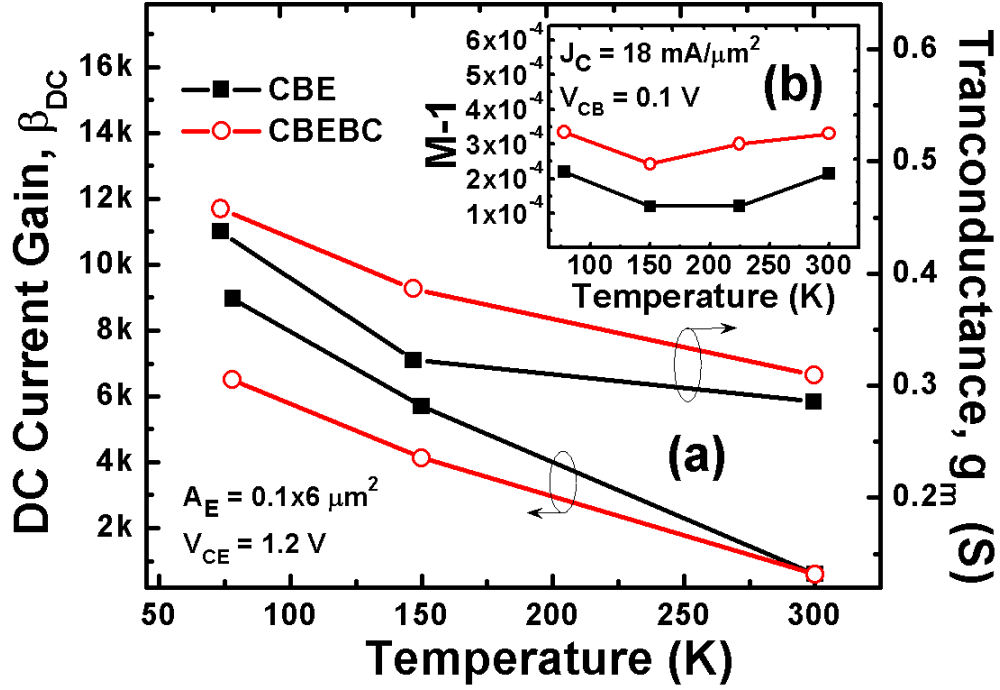


Figure 79. (a) Peak *dc* current gain, β_{DC} (left y-axis) and peak transconductance (right y-axis) plotted as a function temperature. (b) Plot of avalanche multiplication coefficient, $M-1$ as a function of temperature at $\approx J_C$ of $18 \text{ mA}/\mu\text{m}^2$ for both CBE and CBEBc.

Table 6. SiGe HBT *dc* and RF cryogenic performance summary

Figure-of-Merit	CBE		CBEBc	
	300 K	78 K	300 K	78 K
Peak DC Current Gain, β_{DC}	580	8900	595	6500
Peak g_m (mS)	286	423	309	458
Avalanche Multiplication Coefficient($M-1$)	0.30×10^{-3}	0.33×10^{-3}	0.21×10^{-3}	0.22×10^{-3}
r_{bb} at Peak f_T (Ω)	28.0	22.2	21.5	10.4
Peak f_T (GHz)	277	387	303	425
Peak f_{MAX} (GHz)	254	350	290	413
J_C at Peak f_T ($\text{mA}/\mu\text{m}^2$)	15.6	17.2	18.9	18.2
Total Transit-Time, τ_{EC} (ps)	0.45	0.35	0.42	0.33
C_{T-EC} (fF), where $C_{T-EC} = C_{BC} + C_{BE}$ (fF/ μm^2)	9.9	6.2	10.8	7.0
Small-Signal Gain, S_{21} (dB)	25.6	34.1	26.4	23.3
P_{1dB} at Peak f_T (dBm)	-27.6	-36.98	-28.65	-29.2
OIP3 at Peak f_T (dBm)	7.9	9.8	7.6	10.5

9.3.2 SiGe HBT RF Linearity at Cryogenic Temperatures

At the device-level, there are several factors that can impact the linearity of SiGe HBTs (e.g., bias, impedance termination, device geometry, frequency of operation) [107]. Since accurate measurement of transistor linearity (i.e., P_{1dB} and OIP3) at cryogenic temperatures requires substantial experimental effort, several measurement choices were made to minimize the test setup complexity and to ensure data integrity:

- To eliminate the bias dependence on the linearity measurements across temperature the collector current was set to a given value (i.e., J_C of 18 mA/ μm^2 , near peak f_T/f_{MAX}) and V_{CB} to 0.1 V for both device configurations. This high J_C biasing is required to achieve the high-speed and high power density requirements for RF and microwave power amplifiers.
- To remove the impedance dependence from the linearity measurements source- and load-pull measurements were performed at each temperature point at a fixed input power of -25 dBm.
- To exclude the geometry dependence a single common emitter area of A_E of 0.1 x 6.0 μm^2 were selected for both device configurations, CBE and CBEBC.
- To verify the linearity response dependence on frequency two frequency points were selected, 8 GHz and 18 GHz. These frequency points were chosen based on the application requirements.

The Smith charts depicting the P_{OUT} Smith chart contours for CBE and CBEBC devices at 300 K, 150 K, 78 K are shown in Figures 80, 81, 82, and 83. These results reveal that the source (i.e., base terminal) of both devices (shown in Figures 80(CBE) and 82(CBEBC)) does not change significantly with cooling. However, the load (i.e., collector terminal) demonstrates considerable variation with temperature as shown in Figures 81 and 83 for CBE and CBEBC, respectively. Therefore, it is recommended to perform at minimum load-pull measurements when characterizing the SiGe HBTs linearity over temperature. The

source and load impedances were optimized at each temperature point before the single-tone linearity measurements were performed. Figures 84(a) and 85(a) show the measured input-referred P_{1dB} response at 8 GHz as a function of temperature for CBE and CBEBC, respectively. The inset plots shown in Figures 84(b) and 85(b) illustrate the measured small-signal gain as a function of temperature.

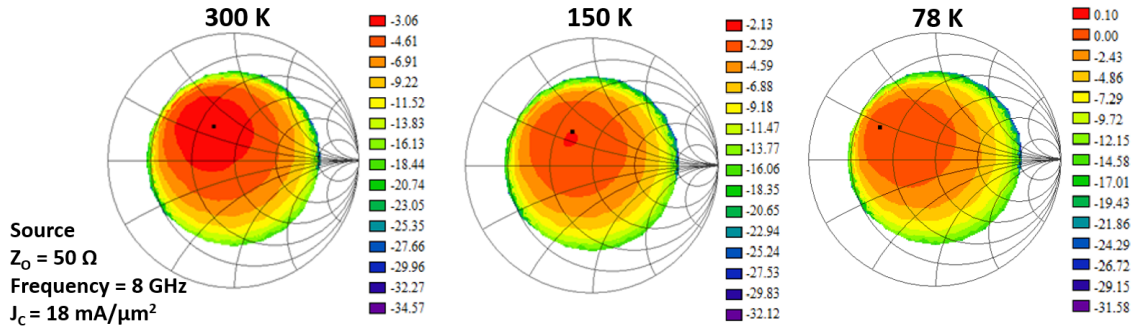


Figure 80. CBE device output power (P_{OUT}) Smith chart contours after load-pull measurement at source (base) terminal for three temperature points: 300 K, 150 K, and 78 K.

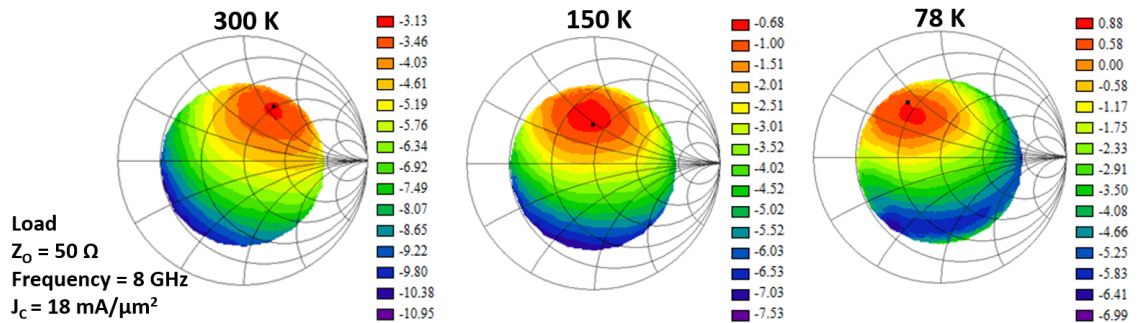


Figure 81. CBE device output power (P_{OUT}) Smith chart contours after load-pull measurement at load (collector) terminal for three temperature points: 300 K, 150 K, and 78 K.

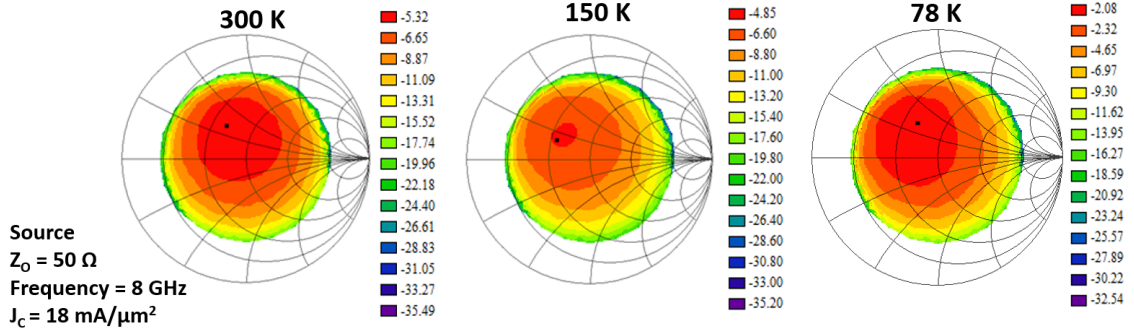


Figure 82. CBEBC device output power (P_{OUT}) Smith chart contours after load-pull measurement at source (base) terminal for three temperature points: 300 K, 150 K, and 78 K.

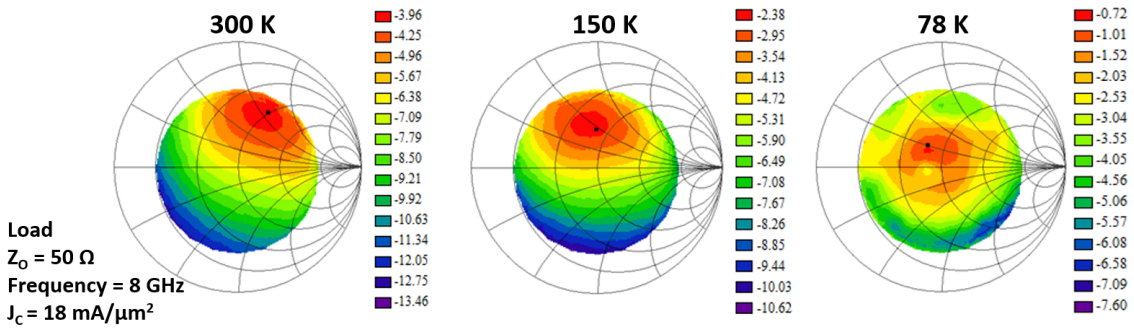


Figure 83. CBEBC device output power (P_{OUT}) Smith chart contours after load-pull measurement at load (collector) terminal for three temperature points: 300 K, 150 K, and 78 K.

The CBE devices demonstrate a fairly constant P_{1dB} of ≈ -28 dB with decreased temperature. However, from 115 K to 78 K the P_{1dB} degrades by ≈ 6 dB. This reduction in P_{1dB} can be attributed to higher saturation mechanisms for CBE at 78 K. The g_m and the input base-emitter conductance nonlinearities are higher in CBE than CBEBC configuration. According to [108], the power saturation is a direct result of the device entering the saturation region for a portion of its operating cycle (i.e., the signal-voltage swing enters the cutoff or saturation regions, thus increasing the nonlinearities for the large-signal transconductance and base-emitter conductance). Based on the results shown in 85(a), CBEBC devices are not impacted by these nonlinearities as much as CBE devices, clearly an important result. For this layout configuration P_{1dB} remains reasonably consistent (≈ -28 dBm) across temperature. The observed increased variation in the measured data (larger error-bars at lower

temperatures) is due to contact resistance change with temperature, and may also be due to the device-to-device process variation.

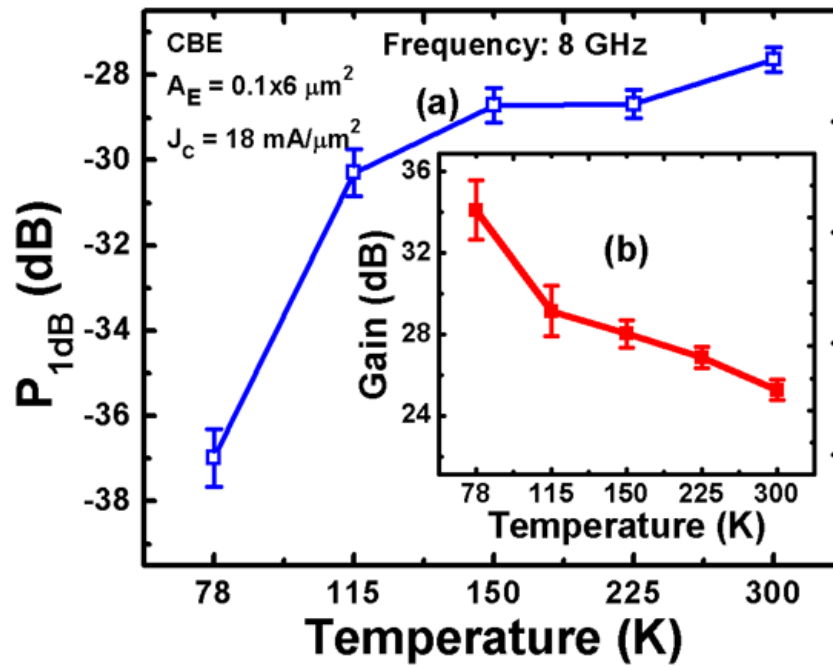


Figure 84. Plots of (a) Large-signal linearity, P_{1dB} and (b) Gain as a function of temperature for CBE SiGe HBTs at 8 GHz frequency. Devices were biased at a J_C of $18 \text{ mA}/\mu\text{m}^2$.

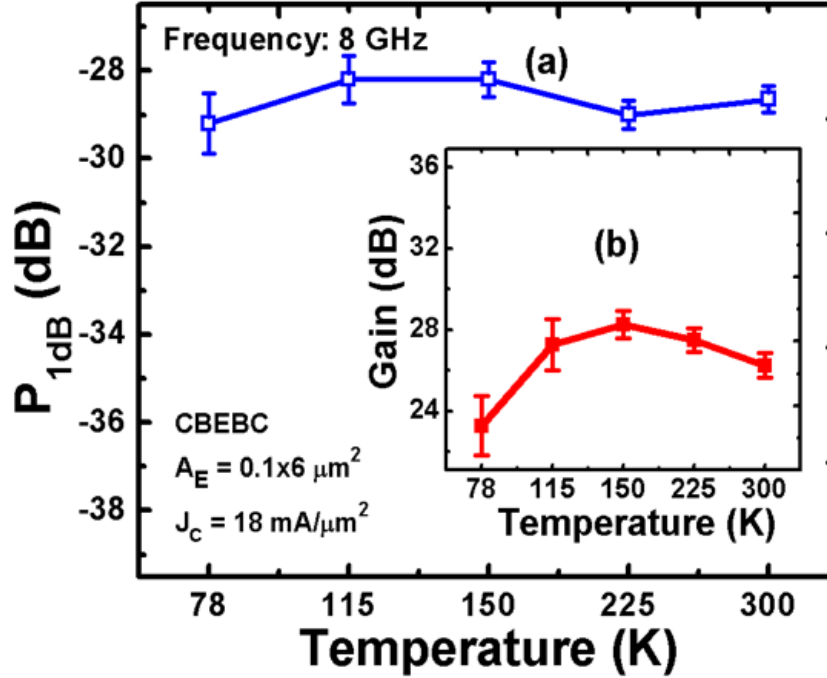


Figure 85. Plots of (a) Large-signal linearity, P_{1dB} and (b) Gain as a function of temperature for CBEBc SiGe HBTs at 8 GHz frequency. Devices were biased at a J_C of $18 \text{ mA}/\mu\text{m}^2$.

The CBE devices show a continual increase in gain with decreased temperature, ≈ 25 dB at 300 K to ≈ 35 dB at 78 K (Figure 84(b)). On the other hand, CBEBc gain increases from 300 K to 150 K, and then gradually decreases to ≈ 4 dB from its peak value of ≈ 28 dB at 150 K (Figure 85(b)). These results confirm that P_{1dB} is dependent on the high-current gain roll-off characteristics of the transistor. At 78 K the high-current effects (i.e., base push-out or Kirk effect) for the CBE devices occur at lower J_C than the bias current used (i.e., J_C of $18 \text{ mA}/\mu\text{m}^2$) when compared to CBEBc devices. The high-current effects and high power levels lead to gain compression and large distortion on the devices. The 78 K large-signal response difference between the two configurations is more clearly observed in Figures 86(CBE) and 87(CBEBc). The results show the measured gain and output power P_{OUT} as a function of P_{IN} at various temperature points. For CBE the gain continues to increase as temperature decreased, whereas for the CBEBc gain decreases at 78 K.

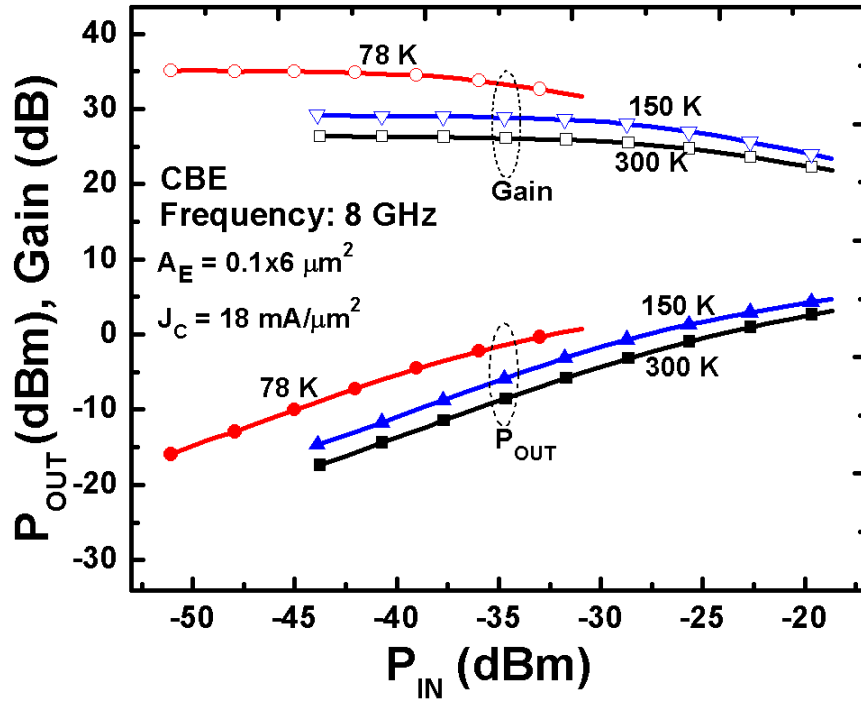


Figure 86. Output power (P_{OUT}) and small-signal gain, S_{21} , as a function of input power (P_{IN}) for CBE devices at 300 K, 150K and 78 K.

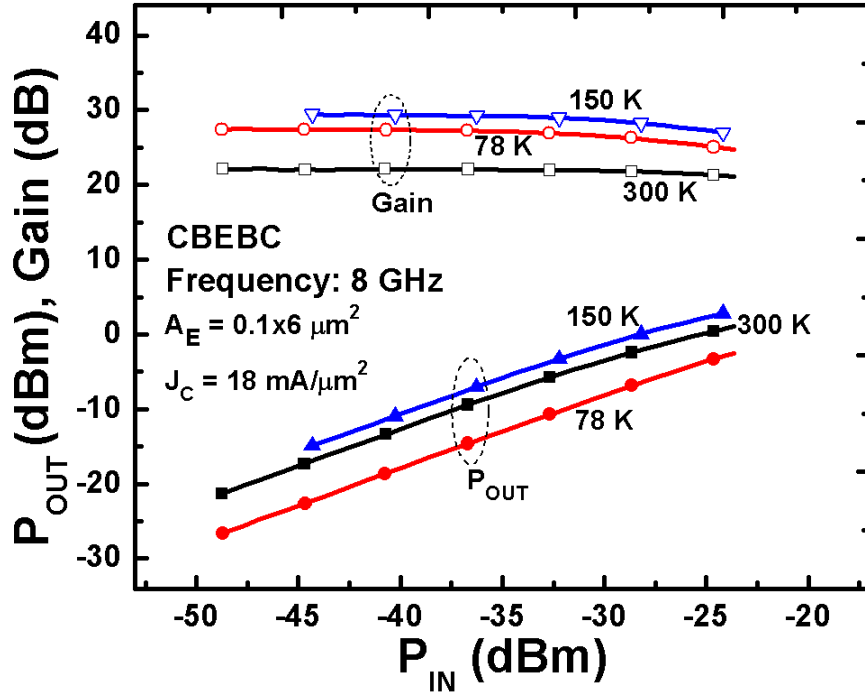


Figure 87. Output power (P_{OUT}) and small-signal gain, S_{21} , as a function of input power (P_{IN}) for CBEBE devices at 300 K, 150K and 78 K.

The measured OIP3 and the corresponding third order intermodulation distortion products (IMD3) (in the inset graph) as a function of temperature at 8 GHz for a fixed collector bias, J_C of $18 \text{ mA}/\mu\text{m}^2$ and V_{CB} of 0.1 V are illustrated Figures 88 (CBE) and 89 (CBEBE). The OIP3 measurements were performed with fundamental tone frequencies of 8 GHz and 18 GHz (the latter data not shown), and 10 MHz tone spacing. The linearity at 18 GHz is marginally higher than at 8 GHz; however, the results follow a similar trend with cooling. Previous studies have observed a similar effect, linearity improves at higher frequencies [109]. At first glance, the measured OIP3 for both devices shows an increasing trend with cooling. However, after careful inspection, the OIP3 of CBE devices exhibits a small decrease at low temperatures (i.e., from 115 K to 78 K the OIP3 reduces by ≈ 2 dBm). This OIP3 decline is due to an increase in IMD3 at 78 K, as shown in the inset plot Figure 88(b). However, for the CBEBE devices the IMD3 products (shown in Figure 88(b)) continue to reduce with decreased temperature, thus resulting in a slight OIP3 increase with cooling.

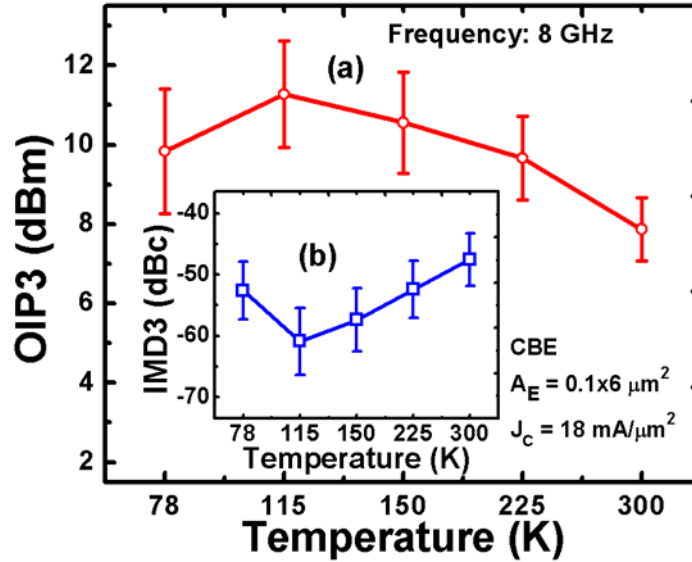


Figure 88. (a) Plot of measured OIP3 as a function of temperature at 8 GHz frequency after source- and load-pull measurements for CBE devices. The source and load impedances were tuned for maximum output power (P_{OUT}); devices biased with a J_C of $18 \text{ mA}/\mu\text{m}^2$. (b) Measured third-order intermodulated distortion products (IMD3) as a function of temperature.

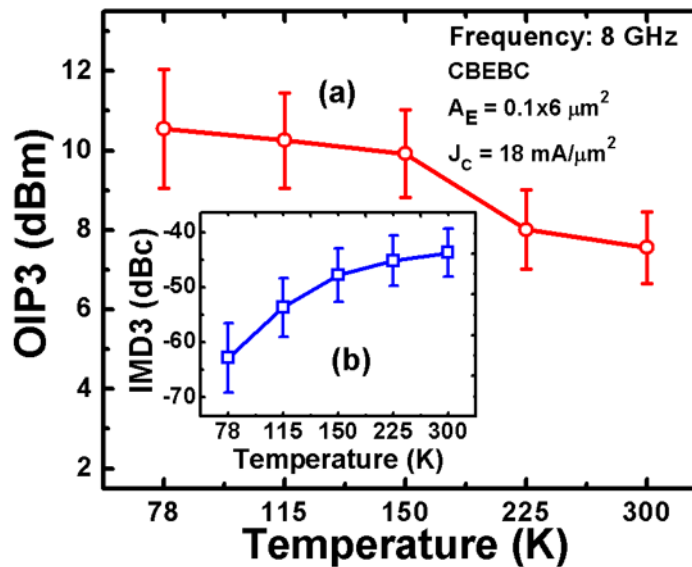


Figure 89. (a) Plot of measured OIP3 as a function of temperature at 8 GHz frequency after source- and load-pull measurements for CBEB devices. The source and load impedances were tuned for maximum output power (P_{OUT}); devices biased with a J_C of $18 \text{ mA}/\mu\text{m}^2$. (b) Measured third-order intermodulated distortion products (IMD3) as a function of temperature.

According to [110], two potential dominant nonlinearity factors impact the SiGe HBT small-signal response, the I_{CB} nonlinearity due to avalanche multiplication, and the C_{CB} nonlinearity due to the collector-base (CB) capacitance. The I_{CB} nonlinearity dominates at low J_C , and C_{CB} nonlinearity dominates at high J_C [110]. Since the SiGe HBTs were biased at a J_C of $18 \text{ mA}/\mu\text{m}^2$, it is likely that the C_{CB} nonlinearity is the limiting factor for both CBE and CBEB. To verify this assumption, avalanche multiplication coefficient (M-1) values were extracted at J_C of $\approx 18 \text{ mA}/\mu\text{m}^2$. The extracted M-1 as function of temperature are shown in Figure 79(b) for both configurations. The M-1 values were extracted using a common-base forced-emitter current measurement, as described in [111]. The results show that M-1 does not significantly change with cooling at the given J_C bias, thus confirming that the C_{CB} nonlinearity is likely the dominant nonlinearity factor in these SiGe HBTs.

To better understand the impact of bias on OIP3 response with cooling, two-tone intermodulation measurements were carried out at 300 K and 78 K. The measurements were performed with the input and output terminals set at 50Ω terminations, V_{CE} set to 1.2 V, and P_{IN} at -25 dBm. Measured OIP3 results across bias at 8 GHz are shown in Figures 90(a) and 91(a) for CBE and CBEB devices, respectively. For both device configurations the results reveal that the OIP3 does not significantly change with cooling. The IMD3 products as a function of J_C are shown in the inset plots in Figures 90(b) and 91(b). At low- and medium-injection the measured IMD3 products are $\approx 10 \text{ dBm}$ higher at 78 K when compared to 300 K temperature point. However, in the high-injection region (i.e., $J_C > 10 \text{ mA}/\mu\text{m}^2$) the IMD3 values converge. The I_{CB} and C_{CB} nonlinearities are potentially the limiting factors of the small-signal linearity for these SiGe HBTs at low-temperatures.

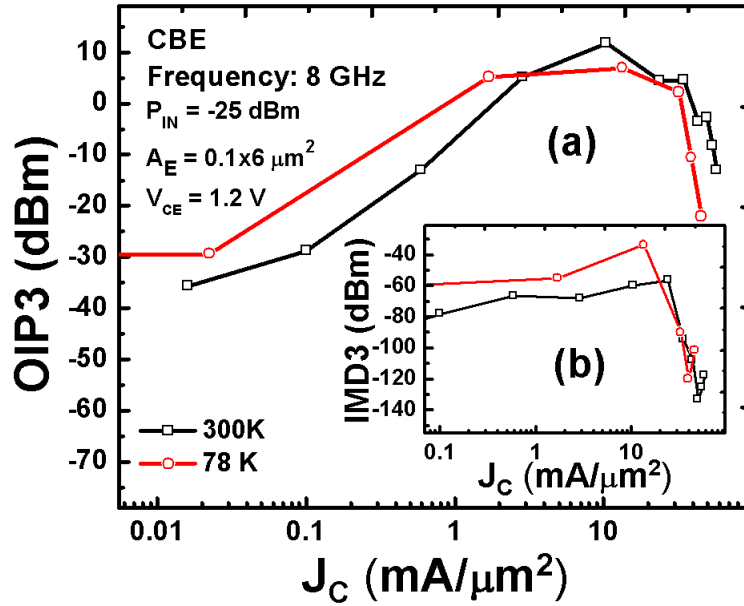


Figure 90. OIP3 as a function of current density (J_C) at (a) 8 GHz and (b) 18 GHz with 10 MHz tone spacing, V_{CE} of 1.2 V, input power (P_{IN}) of -25 dBm, for CBE devices. The input and output were terminated with 50 Ω impedance.

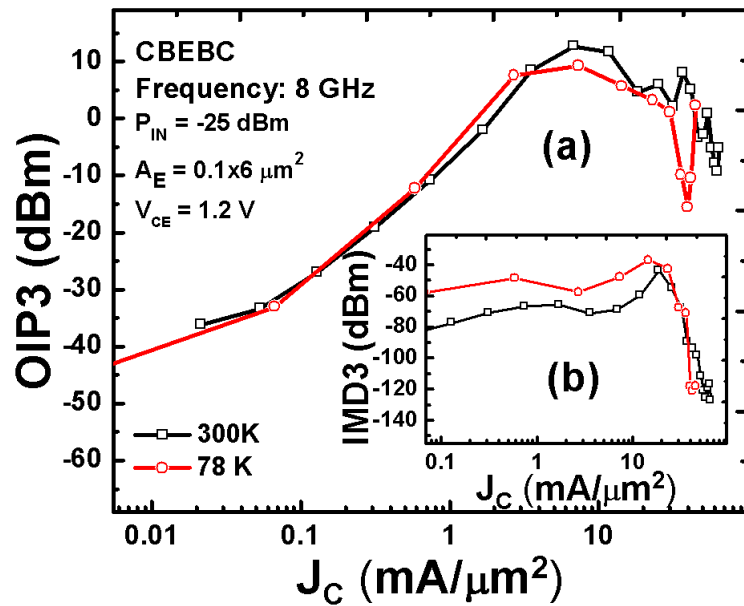


Figure 91. OIP3 as a function of current density (J_C) at (a) 8 GHz and (b) 18 GHz with 10 MHz tone spacing, V_{CE} of 1.2 V, input power (P_{IN}) of -25 dBm, for CBEB devices. The input and output were terminated with 50 Ω impedance.

At J_C of $18 \text{ mA}/\mu\text{m}^2$ the measured OIP3 values are $\approx 5.25 \text{ dBm}$ for CBE and 4.7 dBm for CBEB. The OIP3 values are considerably lower when compared to the values previously shown in Figure 88 (9.84 dBm for CBE) and Figure 89 (10.55 dBm for CBEB). This OIP3 reduction is likely due to the impedance difference during measurements. These results confirm the fact that small-signal linearity is sensitive to load variation [105], [110]. As previously stated, the results shown in Figures 90 and 91 were measured with both input and output terminals set to 50Ω impedances, whereas the data in Figures 88 and 89 were done after source- and load-pull measurements and setting the tuner impedances for maximum P_{OUT} . The load dependence of linearity in these HBTs is likely due to CB feedback, emitter resistance (R_E) feedback, Early effect, and collector-substrate capacitance (C_{CS}) nonlinearity [110]. However, R_E , Early effect, and C_{CS} contribution to the load dependence were determined to be negligible [110].

The dc , ac , and RF linearity figures-of-merit at 300 K and 78 K for both CBE and CBEB configuration is summarized in Table 6. The results show that the peak f_T/f_{MAX} values occur at comparable J_C for CBEB at 300 K and 78 K . However, for CBE this value increases with cooling due to an increase in the electron saturation velocity [94]. The C_{T-EC} (in $\text{F}/\mu\text{m}^2$) is also listed to show the impact of temperature on depletion capacitances. Both devices show a decrease in C_{T-EC} as temperature decreased, and this reduction can favorably contribute to the SiGe HBT's linearity response at cryogenic temperatures.

9.4 Summary

The dc , ac , and RF linearity results of SiGe HBTs fabricated in a 4th generation, 90 nm SiGe BiCMOS technology platform operating at cryogenic temperature were presented in this chapter. This work compares the performance of two SiGe HBT layouts, CBE and CBEB, across temperature. The results presented here confirm previous findings; namely, that both dc and ac performance of SiGe HBTs improve with decreasing temperature. The RF linearity of these SiGe HBTs was anticipated to improve with cooling. However, the

results show that the RF linearity response of these SiGe HBTs (i.e., large-signal P_{1dB} and small-signal, OIP3) at cryogenic temperature does not significantly increase. Both device configurations show an average improvement up to 115 K. The most notable difference between the two device layout configurations occurs at 78 K for the P_{1dB} (i.e., the CBEB devices P_{1dB} remained fairly constant at ≈ -29 dB whereas for CBE it degraded by > 6 dBm (≈ -37 dB).

Based on the results presented here the CBE devices are more susceptible to high-current effects and high power levels at low temperatures than the CBEB devices. The high-current effects causes gain compression and significant distortion, thus limiting the large-signal response. The more stable linearity response for the CBEB is due to its layout configuration. The CBEB layout allows a symmetric spread of injected electrons that reduces the high-current effects and other nonlinearity effects that impact the CBE configuration at low-temperatures. The two potential dominant nonlinearity factors that impact the SiGe HBT small-signal response at cryogenic temperature are the I_{CB} nonlinearity due to avalanche multiplication and the C_{CB} nonlinearity due to the collector-base (CB) capacitance. At a J_C bias of $18 \text{ mA}/\mu\text{m}^2$, the M-1 measurements confirmed that avalanche multiplication is not the dominant nonlinearity for these devices. Two-tone intermodulation measurements across bias reveal that OIP3 does not significantly change with cooling (300 K to 78 K). The over-bias OIP3 results also show that the response is sensitive to changes in load impedance. The CBEB configuration demonstrated the most consistent RF linearity performance at cryogenic temperature out of the two layout choices. The results support the fact that SiGe HBTs can be used for high-performance and high-frequency cryogenic applications.

CHAPTER 10

CONCLUSIONS AND FUTURE WORK

The purpose of this research work is to provide insight on the response of mixed-signal (RF and analog) circuits and devices when operating in extreme environments, particularly at cryogenic temperatures and radiation-rich environments. This work makes use of commercially available SiGe BiCMOS and SOI CMOS technologies because of their strong potential for use in extreme environment applications. The research presented in this dissertation will assist in development of next-generation space-based electronics that are able to withstand extreme environments (e.g., the space environment) with minimal or, no shielding required. In this chapter, the contributions of this dissertation are summarized, and suggestions for future research are provided.

10.1 Contributions

The contributions of this work can be summarized as follows:

1. Design and characterization of high-isolation SPST and SP4T RF switch circuits using a 130 nm SiGe BiCMOS technology for use in a novel radar transceiver system. Both, SPST and SP4T switches achieve more than 40 dB isolation from 1 to 20 GHz. The switch performances were investigated at room-temperature and at cryogenic temperatures. The results at low temperature show that all key performance metrics including insertion loss, isolation, large- and small-signal linearity improve with decreasing temperature.
2. Demonstration of one of the lowest reported loss performance wideband SPDT switches. The switch was designed and fabricated in 180 nm CMOS on SOI technology. The SPDT switch has an insertion loss of less than 0.5 dB from *dc* to 20 GHz, and less than 2.0 dB at 40 GHz. To evaluate the capabilities of this switch, a one-bit 180° switched-line phase-shifter was designed and characterized.

3. A comprehensive characterization of the SPDT switches RF performance designed in a 180 nm SOI-CMOS technology was demonstrated at cryogenic temperatures. All key performance metrics, i.e., insertion loss, isolation, large- and small-signal linearity improve with decreasing temperature. To provide insight into the mechanisms underlying the observed changes in the switch performance at low-temperature, individual transistors were characterized across temperature.
4. The impact of proton irradiation on the performance of high-isolation SPST switches designed in 130 nm SiGe BiCMOS technology was investigated. Measurement results confirm that the worst-case response occurs when the switch is biased during irradiation, and it also reveals that the switch total dose response is bias dependent. Irradiated measured results of both RF and *dc* individual transistor test structures were also performed and analyzed to assist with the circuit analysis.
5. An investigation of the impact of single event transients (SETs) on RF SPDT switches using charge deposition by through-wafer two-photon absorption (TPA) was presented. The SPDT switch was designed and fabricated in the commercially-available 180 nm SiGe BiCMOS (IBM SiGe 7HP) technology. Based on the presented results, the SPDT switches are sensitive to SETs. Three mitigation strategies were proposed to minimize SETs from propagating from the SPDT circuit into other connected circuits (e.g., LNA, Mixer, VCO). Only two out of the three proposed mitigation strategies were implemented and demonstrated: (1) design and fabricate the switch on an SOI technology; (2) the use of a different device biasing scheme designed to minimize the charge collection mechanism at the device terminals.
6. Precision voltage reference circuits (VRCs) were designed using a new state-of-the-art 4th-generation 90 nm SiGe BiCMOS technology. Single event transient and total ionization dose experiments were performed on the VRCs. The first-order BGR

VRC results confirm that SiGe-based BGR circuits are sensitive to SET, but the circuits demonstrate minimal degradation to TID exposure. Based on first-order circuit results, two circuit-level RHBD techniques using inverse-mode (IM) SiGe HBTs and a PIN diode VRC as potential RHBD strategies were proposed and demonstrated.

7. The *dc*, *ac*, and RF linearity results of SiGe HBTs fabricated in a 4th generation, 90 nm SiGe BiCMOS technology platform operating at cryogenic temperature were investigated. The performance of two SiGe HBT layouts, CBE and CBEBC, across temperature were compared. The results reveal that the CBE devices were shown to be more susceptible to high-current effects and high power levels at low temperatures than the CBEBC devices. The more stable linearity response for the CBEBC is due to its layout configuration. The CBEBC layout allows a symmetric spread of injected electrons that reduces the high-current effects and other nonlinearity effects that impact the CBE configuration at low-temperatures.

10.2 Future Work

The research work presented in this thesis establishes several interesting opportunities for future work:

1. Design and fabrication of SPDT circuits using only bulk transistors (e.g., non-TW) to provide a more complete understanding on the radiation (TID and SET) biasing dependence, and to compare its response to the hybrid SPDT design presented here.
2. Compare the TID response of the RF switches using different radiation sources, 63 MeV proton, 10 keV X-ray, and gamma Cobalt-60 (Co-60).
3. Conduct detailed current-injection simulations through an entire RF receiver and/or transmitter chain using mixed-mode TCAD tools to understand the system-level impact of propagating SET current transients.

4. Experimentally investigate the SET implications of laser-induced transients on RF signals that may propagate from SPDT circuits to other RF blocks (e.g., LNA, PA, VCO)
5. Conduct SET experiments on RF circuits using modulated RF signals as input instead of continuous wave (CW) signals.
6. Perform heavy-ion testing to correlate SET results between TPA laser energy and LET for both SPDT RF switches and voltage reference circuits.
7. Investigate low-temperature operation and radiation response of high-speed latch comparators (circuits were designed and fabricated in two different BiCMOS technologies, IBM 9HP and IHP SG13-G2).
8. Study the linearity response (large-signal and small-signal) of SiGe HBTs across different process technologies (e.g., IBM, Jazz, IHP, TI) and device geometry sizes at cryogenic temperatures.
9. Model the SiGe HBT's nonlinearity contributions at low temperatures with the Volterra series to better understand the small-signal response difference between CBE and CBEBC layout configurations.
10. Investigate low-temperature operation and the radiation response of RF building blocks (e.g., RF switches, VCO, LNA).
11. Re-design the PIN diode voltage reference circuit to improve its temperature performance, and experimentally characterize its SET radiation response at a heavy-ion broad-beam and two-photon absorption backside pulsed laser.

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VITA

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