ENERGY EFFICIENT ACTIVE COOLING OF INTEGRATED CIRCUITS USING EMBEDDED THERMOELECTRIC DEVICES

A Thesis
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Master of Science in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2014

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To My Parents and Grandparents

ACKNOWLEDGEMENTS

This dissertation would not have been possible without the guidance and the help of several individuals who in one way or another contributed and extended their valuable assistance in the presentation and completion of this thesis. First and foremost, my utmost gratitude to my academic advisor, Dr. Saibal Mukhopadhyay, whose sincerity and encouragement I will never forget. His excellent guidance, patience, and providing me with an excellent atmosphere for doing research has resulted in this thesis. I also thank my committee members, Dr. Sudhakar Yalamanchilli and Dr.Satish Kumar for their time, encouragement and insightful comments.

I would like to thank both current and past members of the 'Gigascale Reliable Energy Efficient Nanosystem (GREEN) Lab'. I would like to thank Dr. Jeremy Tolbert, Dr. Minki Cho, Dr. Subho Chatterjee and Dr. Kwanyeob Chae, for their support when I just started my master's program. I thank my fellow lab mates – Amit Trivedi, Denny Lie, Boris Alexandrov, Wen Yueh, Khondker Ahmed, Sergio Carlo, Jae ha Kung, Monodeep Kar, Krishnamurthy Yeleswarapu, Duckhwan Kim, Jong Hwan Ko and Mohammed Amir for the stimulating discussions and for all the fun we have had in the last two years. I would also like to thank my friends Upplli Raghunathan, Srikrishna Sitaraman, Vijay Sukumaran, Gokul Kumar, Satyan Tellikepalli, Karthik Swaminathan and all other people who have helped me throughout my stay here at Georgia Tech.

I would also like to thank my parents for their love, support and wise guidance for the past 24 years that has molded me into what I am today. Last but not the least, I express my gratitude to almighty, without which all these wouldn't have been possible.

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SUMMARY

With technology scaling, the amount of transistors on a single chip doubles itself every 18 months giving rise to increased power density levels. This has directly lead to a rapid increase of thermal induced issues on a chip and effective methodologies of removing the heat from the system has become the order of the day. Thermoelectric (TE) devices have shown promise for on-demand cooling of ICs. However, the additional energy required for cooling remains a challenge for the successful deployment of these devices. This thesis presents a closed loop control system that dynamically switches a TE module between Peltier and Seebeck modes depending on chip temperature. The autonomous system harvests energy during regular operation and uses the harvested energy to cool during high power operation. The system is demonstrated using a commercial thin-film TE device, an integrated boost regulator and few off chip components. The feasibility of the integration of the TEM and the automated mode switching within the microprocessor package is also evaluated. With continuous usage of thermoelectric modules, it starts to degrade over time due to thermal and mechanical induced stress which in turn reduces the cooling performance over time. Impact of thermal cycling on thermoelectric cooling performance over time is evaluated using the developed full chip package model.

CHAPTER 1

INTRODUCTION

The doubling of microprocessor performance every 18 months has given rise to two new factors: more transistors per chip and super linear scaling of the processor clock with technology generation [1]. However, technology scaling along with frequency and complexity increase has resulted in a significant increase of power density levels in a chip, which is currently becoming a key limiting factor state of the microprocessors [2, 3]. This power density, which has been doubling every two to three years, is likely to continue in future generations as well [4]. One of its most important side effects is increased heat dissipation [5, 6], which causes numerous problems. Among others, it has a negative effect on the cost of cooling methodologies [7], leads to less energy efficient designs [8], triggers throttling events which in turn decreases performance [9], and makes the CPU less reliable [10].

Integrating all the cores on a chip can extend the performance improvement rate [11] but is likely to reduce the per-core cooling ability and increase the negative effects of temperature-induced problems. Additionally, having multiple cores stacked together can trigger execution scenarios that can cause excessive thermal stress or significant performance capabilities. For every 10°C rise of the junction temperature, the device failure rate doubles [12]. Hence, it becomes imperative for the designer to remove the waste heat generated inside a package before the reliability of the device is compromised. Thermal solutions range from the simplest to the complex. The simplest form of heat removal is the movement of ambient air over the device. While these simple thermal

solutions cannot remove concentrated hot spots in a processor, more sophisticated measures such as heat sinks, heat pipes or even liquid-cooled heat plates are considered as viable options.

Localized regions of higher temperature, known as hot spots, are becoming more severe as local power density and overall die power consumption increases. The temperature differential across a microprocessor die can vary from 5 to 30 C due to large variations in heat flux density. Present day microprocessors have an average heat flux of 5-50 W/cm^2 and peak hot spot fluxes up to 250 W/cm^2. Thus, hot spots, instead of the overall chip temperature essentially drive the thermal design challenge [13]. Lately, embedded thermoelectric devices have shown a promising approach for addressing the critical issues of hot spot management by serving as an active hot spot thermal management applicant. Thermoelectric modules act as a cooler based on the principle of Peltier effect, wherein when an electric current is driven through two dissimilar materials sandwiched between the legs of the module, heat is absorbed at one junction and released at the other junction. The two dissimilar materials are usually made up of an n-type and p-type semiconductor. The movement of heat provides a solid-state cooling capability that is ideally suited for applications where temperature stabilization, temperature cycling or directed cooling is required. Precise control of the junction temperature can also be achieved by adjusting or reversing the polarity of the applied DC cooling current. Operating the thermoelectric module for a prolonged period of time can take a toll on its performance capabilities due to reliability issues.

For thermoelectric devices and systems, reliability is one of the fundamental features and is determined as the ability of the device to sustain its operation well within

the established limits without deteriorating its ability to perform functions necessary under given modes and conditions of use, technical maintenance, repairs, storage and transportation [14,15]. Thermoelectric module reliability data entails some risk because there are numerous application parameters and conditions that will affect the end result. Although reliability data is valid for the conditions under which a test was conducted, it is not necessarily applicable to other configurations. Module assembly, power supply, temperature control systems and techniques, temperature profiles, together with a host of external factors, can combine to produce failure rates ranging from extremely low to very high. Thermoelectric module failures typically may be classified into two groups: catastrophic failures and degradation failures.

Degradation failures tend to be long-term in nature and usually are caused by changes in semiconductor material parameters or increases in electrical contact resistance. High temperature exposure may lead to material parameter changes and, therefore, reduced thermoelectric performance. Since the thermoelectric devices are usually fabricated using integrated circuit technology, it is reasonable to assume that the degradation of these devices will be caused by one or more of the failure mechanisms associated with silicon ICs. Three main degradation mechanisms are contact migration, corrosion and intermetallic diffusion/formation. Among them the prominent failure mechanism is intermetallic diffusion/formation due to its high value of activation energy (> 0.6 eV) [16]. Some of the electrical performance reliability issues is affected by varying temperature profiles. Above 80°C copper and silicon diffusion into the thermo elements occurs due to increasing solid solubility in the thermoelectric material and increasing diffusion rate thus resulting in void formation. Such voids may migrate, merge

together and eventually lead to open circuit failure. At 100 - 110°C the combined solubility and diffusion rate can result in approximately 25% loss of device performance within 100 hours [17, 18].

Temperature control methods also have an impact on thermoelectric module reliability. Linear or proportional control should always be chosen over ON/OFF techniques when prolonged life of the module is required. Thermal cycling affects the thermoelectric performance and studies have shown the effect of varying temperature on the characteristics of the module such as Seebeck/Peltier coefficients, thermal conductivity, output power and figure of merit [19-21]. Several factors relate to failure rate in thermal cycling including (1) the total number of cycles, (2) the total temperature excursion over the cycle, (3) the upper temperature limit of the cycle, and (4) the rate of temperature change. Thermally induced mechanical stresses are greater in larger modules and such modules generally have a greater number of couples resulting in many more individual solder connections which may become fatigued by thermal stress. Thermoelectric devices have been successfully subjected to shock and vibration requirements for various applications. While a thermoelectric device is quite strong in both tension and compression, it tends to be relatively weak in shear. When in a severe shock or vibration environment, care should be taken in the design of the assembly to ensure "compressive loading" of thermoelectric modules. ICs fabricated with improper mechanical stress considerations and un-flat heat sinks can cause severe shear forces resulting in severe war-page of the device resulting in a mechanical failure [22-24]. Overcoming all these issues is a big challenge for a designer as he the effects of aging

and material degradation need to be incorporated in the initial design so that efficient cooling can be achieved till the end of cycle (EoC).

Looking beyond cooling, a portion of heat still manages to traverse the entire path from the chip through the thermal insulating material (TIM) layers onto the thermoelectric module and finally to the heat sink through the heat spreader during the non-cooling mode of operation. The junction temperature of the chip/processor is maintained at an user-defined value only at the expense of spending energy in the form of sending in DC cooling current through the legs of the thermoelectric module to initiate cooling. The same thermoelectric module can also operated as an energy harvesting device by converting the waste heat rejected by the system into electricity by making using of the Seebeck property of a thermoelectric module. The dynamic switching of the module into both the cooling and harvesting modes of operation can serve as a new method for active hotspot thermal management of processors.

1.1 Thesis Outline

The thesis outline is as follows: Chapter 2 discusses the various reliability effects on a thermoelectric module. In this chapter, the impacts that aging could have on the cooling performance of the module and design optimizations which need to be considered over time are presented.

Chapter 3 demonstrates a new system level design and control mechanism for switching a thermoelectric module between the Peltier and Seebeck modes of operation.

Chapter 4 summarizes and concludes the thesis. An extension of the existing work is discussed in brief. It also discusses the future work and improvements that can be done based on the present work.

CHAPTER 2

RELIABILITY AND AGING EFFECTS

2.1 Introduction

The performance of thermoelectric modules degrades significantly over time with thermal cycling as the constituent materials and interfaces are exposed to large temperature gradients [16, 20, 22, 25]. The legs of the thermoelectric module are attached to the copper interconnects through a thermally conductive but mechanically brittle solder joints. Performance reduction and device failure is primarily caused by the larger number of thermal cycles and thermal stress acting on the modules. The CTE (coefficient of thermal expansion) mismatch between the solder joints and the copper interconnects accounts for the thermal stresses observed at the contacts. These stresses at the interfaces also induce material diffusion into the N and P legs of the TE module thereby accelerating the rate of device degradation. Through cycling it is observed that the current applied through the TE module forms micro cracks at the interface between the connecting metal and the TE element [26]. Optical and infrared images of a TE pellet before and after thermal cycling are shown in figure 2.1. Thermal cycling was performed on a commercial TE module [27], by oscillating the TE module between +146 ^{o}C and -20 ^{o}C for 45000 cycles until failure in [26]. The four main properties of a TE module namely: 1) Seebeck coefficient 2) Thermal Conductivity 3) Electrical conductivity and 4) Figure of Merit were measured at intervals during the thermal cycling process. Figure 2.2 shows the effect of thermal cycling on the electrical resistance module of the TE module.

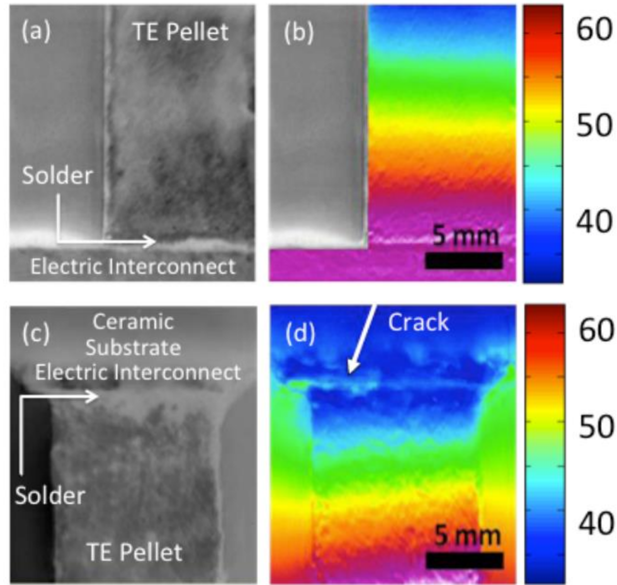


Figure 2.1: (a) Optical and (b) Infrared image of a TE pellet before thermal cycling (c) Optical and (d) Infrared image of a TE pellet after thermal cycling *{adapted from [26]}*

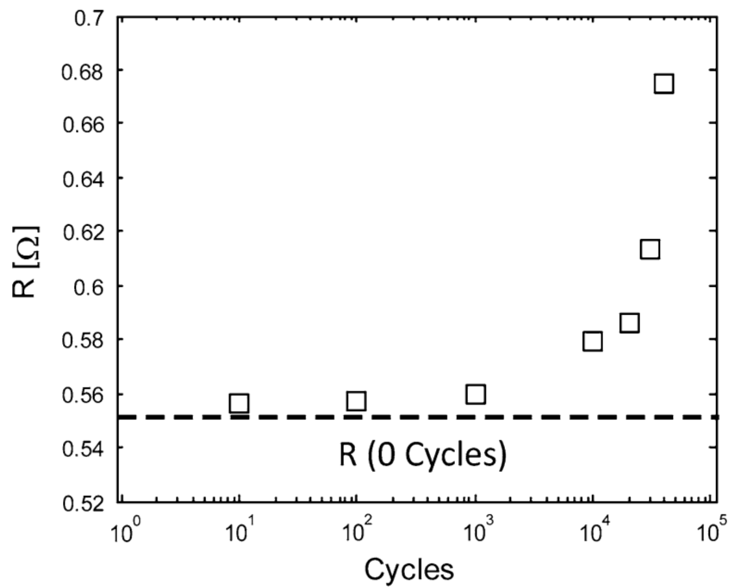


Figure 2.2: Effect of thermal cycling on the electrical resistance of the TE module *{adapted from [26]}*

The electrical resistance of the module was found to increase with the number of thermal cycles due to the formation of cracks between the interconnect and TE leg

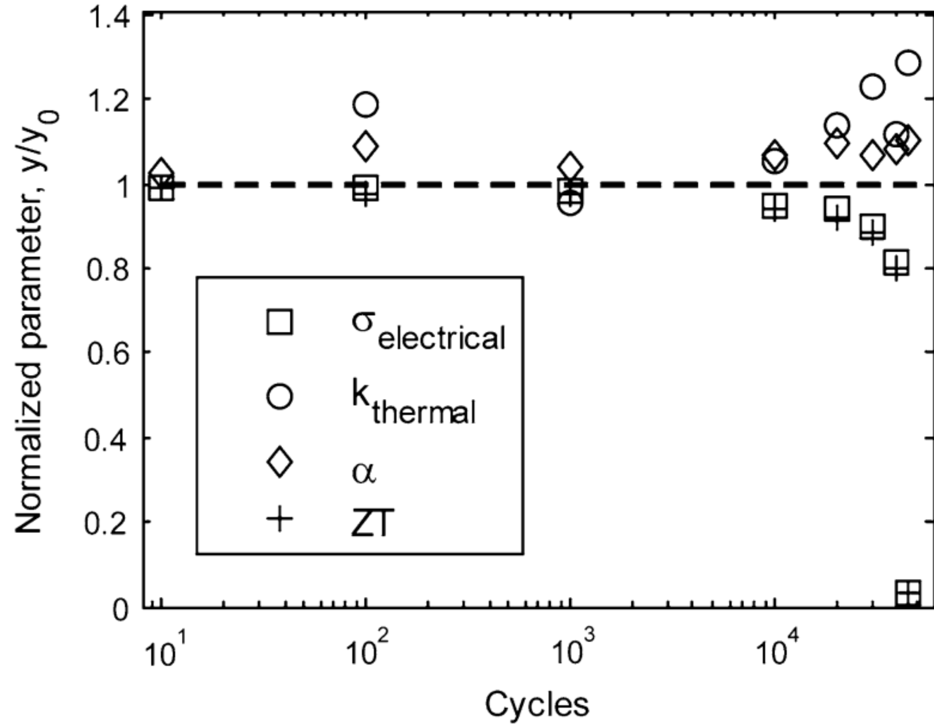


Figure 2.3: Effect of thermal cycling on thermoelectric properties ***{adapted from [26]}***

interface. This in turn increases the contact resistance and results in the reduction of the figure of merit (ZT).

The variation of the various thermoelectric properties with progressing thermal cycles with values normalized relative to the baseline value measurements taken at 0 cycles is shown in figure 2.3. Compared to the condition of a TE module before thermal cycling, the Seebeck coefficient remained relatively stable, the thermal conductivity increased by 20%, the electrical resistance increased by 22% and as a cumulative result the figure of merit of the module dropped by 3%. The legs of a TE device are connected electrically in series and thermally in parallel. Hence, the micro cracks formed at the interface has a profound impact on the electrical resistance as the net resistance created by these cracks sum up while the thermal conductivity remain less affected.

With the results obtained in [26] serving as a motivation to look into the operation of the thermoelectric module as a cooler over time, a spice model of a thermoelectric module embedded in a package is formulated. The effects of thermal cycling on the cooling performance is studied in this chapter.

2.2 Simulation Framework

The embedded thermoelectric device inside a package model was developed based on [28]. The system model considers a silicon chip, thermal interface material (TIM), heat spreader and heat sink. The TE device is integrated inside the TIM. The 3D distributed RC based thermal models of the integrated system is presented in figure 2.4.

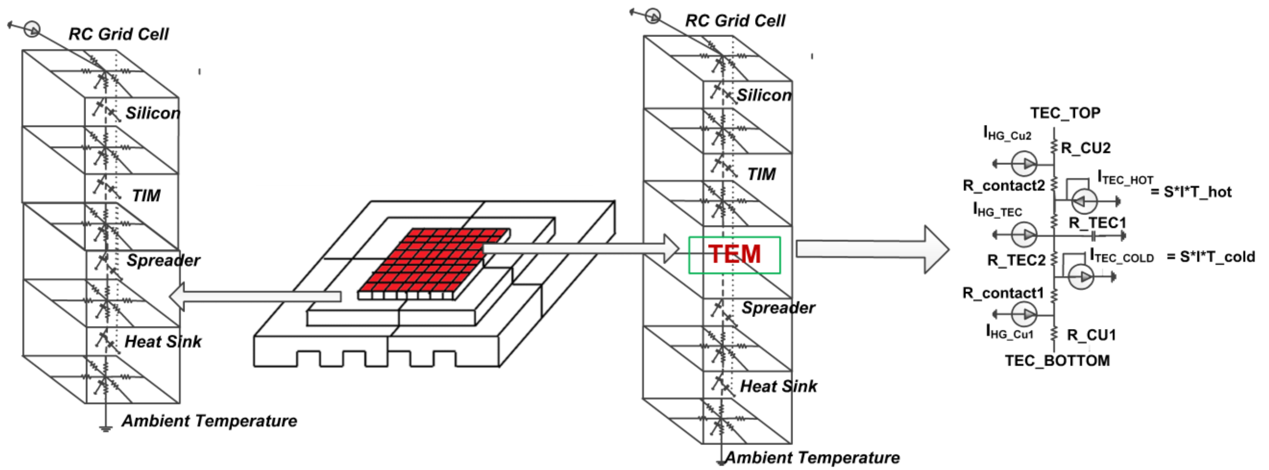


Figure 2.4: Overall simulation model showing the package grid structure locations without the TEM, Flip chip package; Package grid locations with the TEM; TEC model of the TEM

The TE module in the simulation model is similar to the commercial module used in [26] and is modelled as per the specifications given by the manufacturer [27]. A 11.50 mm x 11.50 mm x 3.18 mm, 17 couple TEM (composed of bismuth telluride, Bi_2Te_3) is embedded into the middle of the package between the TIM, silicon and heat spreader

layers. The TE module is the same size as the chip and covers the entire TIM layer similar to the setup in [26]. The conduction resistance and capacitance values of the RC thermal model are given by R_{conv} and C, where L is the thickness of the unit cell, A- the cross-sectional area, K – thermal conductivity, ρ – resistivity and Cp – specific heat. The TEC behavior using an equivalent compact SPICE circuit is considered which accounts for the Peltier cooling effect, the I^2R losses through the contact resistances, and the Joule heating effect [28]. Heat is added at the hot side and is subtracted at the cold side to model Peltier cooling. Current sources are also used to model the I^2R losses at the contact regions. The package parameters and values are chosen based on the results from prior works [28 – 31]. The TE module parameters namely: Seebeck coefficient (412 μV/K), thermal conductivity (37 W/mK), internal resistance of the module (0.55 Ω) and electrical conductivity (2.83 e-05 S/m) were chosen as the starting values based on the values prior to thermal cycling at 0 cycles from [26].

2.3 Simulation Setup and Results

With the simulation framework for analyzing the impact of thermal cycling on thermoelectric cooling performance setup, the feasibility analysis of 'DC' cooling is studied. The TE module is always turned on and provides cooling at all times. Figure 2.5 shows the steady state silicon temperature at the center of the TE module location. Each curve represents the number of thermal cycles the TE module has undergone. To study the effect of thermal cycling on the module, values of the main thermoelectric properties

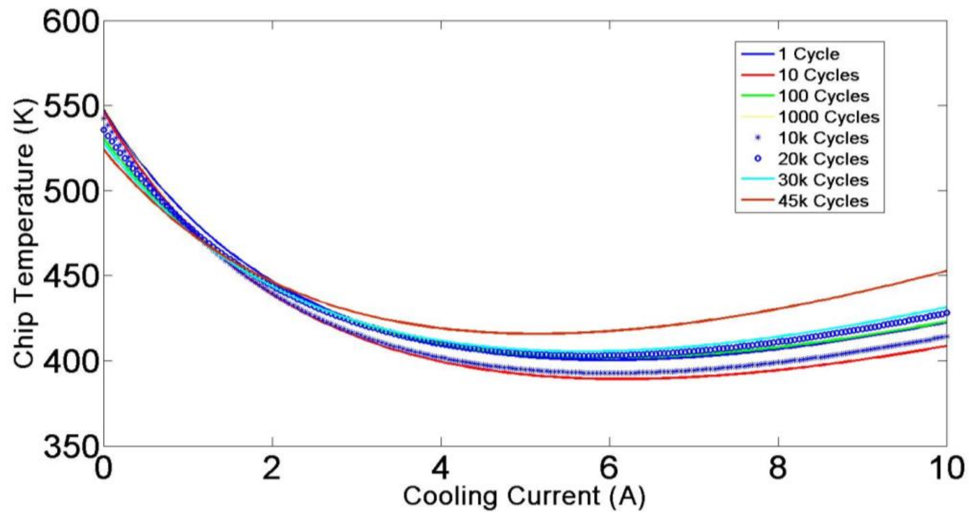


Figure 2.5: Variation of steady state chip temperature over cycles

namely Seebeck coefficient, internal resistance, as well as electrical and thermal conductivity are updated at regular intervals as per figures 2.2 and 2.3. With varying cooling current for every cycle the TEC assisted cooling is observed as the chip temperature drops. It is also observed that as the cooling current increases (beyond 5A) eventually more Joule heating is introduced leading to higher steady state temperatures. At higher cooling current Joule heating becomes larger than Peltier cooling and consequently it becomes unadvisable to operate at higher cooling currents.

It can also be observed from figure 2.5 that for the initial thermal cycles (from 0 to 1000) there is not an observable change in the device's cooling performance as noticeable changes aren't noticed in the thermoelectric properties. After 10,000 cycles the cooling performance starts to deteriorate. For instance, the chip temperature with 4A of cooling current at 45,000 cycles is much higher than the chip temperature with the same amount of cooling current at 0 cycles. This is indicative of the fact that the changes in the

internal properties of the module as a result of thermal cycling has caused the increase in chip temperature.

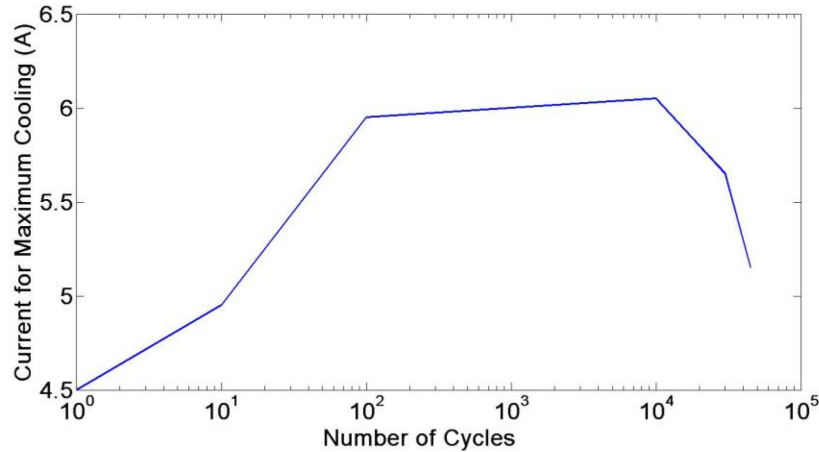


Figure 2.6: Variation of cooling current for maximum cooling

The cooling current that needs to be supplied to achieve maximum cooling (maximum dip in chip temperature when compared to the baseline case i.e. 0A cooling current) is observed to change with increasing number of cycles. It increases initially with the increase in the number of cycles (0 to 10,000) and reduces beyond 10,000 cycles. Hence, an adaptive cooling technique wherein, the cooling current utilized for cooling changes over time is required. Figure 2.7 discusses the effect of having an adaptive scheme over a fixed cooling methodology.

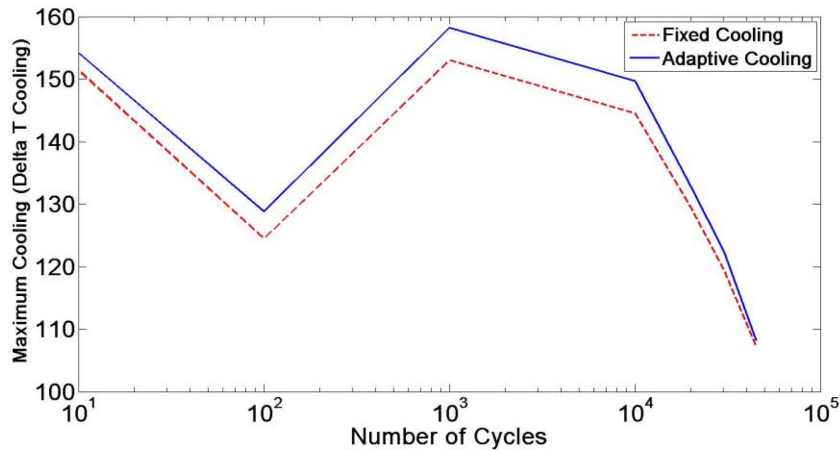


Figure 2.7: Effect of adaptive over fixed cooling

In the case of adaptive cooling technique, the cooling current required for maximum cooling is changed with respect to the number of cycles the TE module has undergone. For the fixed cooling methodology, the value of cooling current for which maximum cooling is obtained at 0 cycles is first obtained and the same cooling current is sent into the module for the rest of the cycles. Adaptive cooling provides a higher cooling performance when compared to the fixed cooling case as the adaptive cooling case takes into account the material and module degradation over time. This stretches the performance capabilities of the module to the maximum possible extent.

2.4 Summary

In this chapter, the thermoelectric performance over time is studied using an embedded model in SPICE. The material degradation over time is input as parameters into the model and the system performance is measured at gradually increasing number of cycles. The simulation results show that the thermoelectric cooling performance deteriorate over time. By predicting the future performance of the TE module, appropriate design considerations can be implemented as the aging cycle progresses. The simulation results also indicate that the amount of cooling current to obtain maximum cooling required by the module isn’t a fixed value and changes over time. Hence, an adaptive cooling technique can play an important role in maximizing the output performance while maintaining the required cooling performance.

CHAPTER 3

AUTONOMOUS MODE SWITICHING OF A TE MODULE

3.1 Introduction

The on-demand active cooling of microprocessors using thermoelectric devices (TE) has emerged as promising direction for thermal management. A TE Cooler (TEC) operates on the basis of the Peltier effect that helps to reduce the junction temperature by dumping heat from the cold side to the hot side when a current flows through it [28-33]. The integration of Bi_2Te_3 based thin film super-lattice TECs within microprocessor package has been experimentally demonstrated [29]. The design and run-time approaches for integration of TEC are also being explored. Long et al. have explored algorithms for optimal placements of TECs in a chip to maximize the cooling efficiency [31, 32]. The

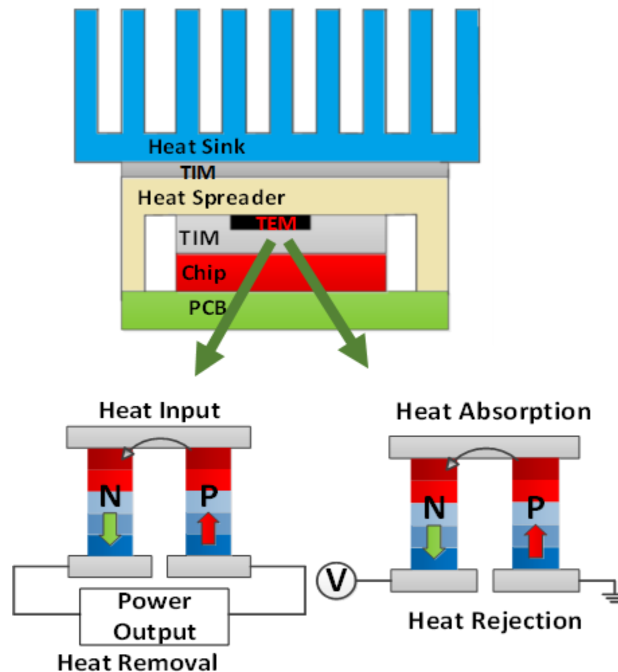


Figure 3.1: Embedded thermoelectric module

applications of TECs in dynamic thermal management of microprocessors have been studied [28, 33]. Integrated TECs help sustain a high power pulse for a longer time-period, thereby avoiding the need for thermal throttling and hence, improving performance. A major challenge for TEC assisted cooling is the need for additional cooling energy. The TE devices can harvest electrical energy form heat based on Seebeck effect [34]. The TE Generators (TEG) have been used for harvesting waste heat from electronic circuits [34-37]. The Peltier and Seebeck effects in a TE device motivates the concept of *energy-efficient cooling* where cooling is achieved with minimal external energy. The concept of dynamic mode switching between TEC and TEG has been introduced before [38]; however, a control system for on-demand energy efficient cooling and its experimental characterization has not been presented before.

This chapter explores potential of on-demand *energy-efficient cooling* using a single TE module (TEM) integrated within the package of an Integrated Circuit (IC) as shown in Figure 3.1. A control system is presented in figure 3.2 to regulate the junction temperature of the IC below a threshold by dynamic switching of the TEM between Peltier (TEC) and Seebeck (TEG) modes. The TEM operates in the TEG (harvest energy)

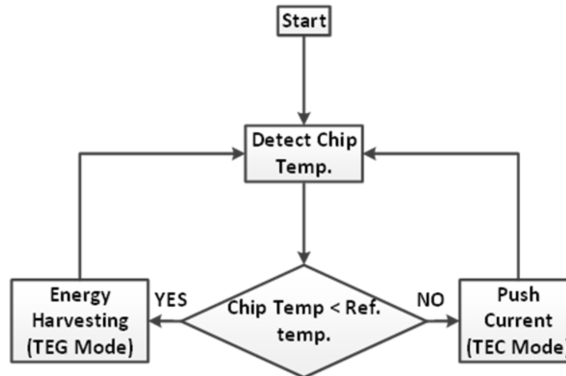


Figure 3.2: Basic control principle for toggling the TE module between the two modes

mode when the temperature is lower than the threshold and; and switch to the TEC mode (consumes energy) when temperature crosses the threshold. Over a long duration of IC operation with multiple power modes, the energy harvested during nominal power of the IC is used for cooling during high power modes. However, the more intriguing property of the controller is that the dynamic mode switching continues to occurs within the high power mode itself using a hysteretic control; hence, energy efficient cooling is achieved even during a persistent high power condition. The proposed control system allows an IC to sustain a high power pulse for a longer time duration with minimal additional energy and without violating thermal constraints. The control principle is also experimentally demonstrated using a commercial isolated TE module [39]. The controller is designed using discrete electronic components and a boost regulator test-chip integrated in a board.

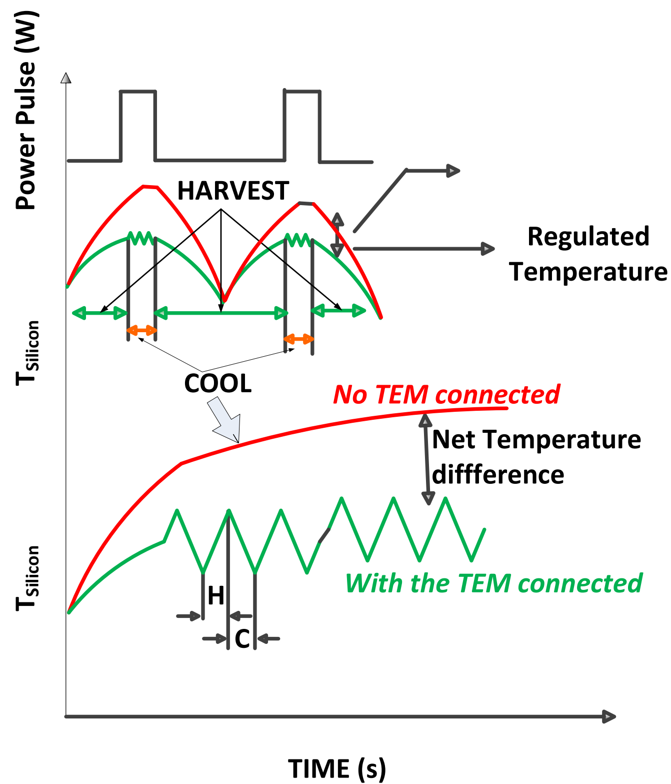


Figure 3.3: Dynamic mode switching of a TE module

The application of the control principle for integrated TE device is projected based on full-chip electro-thermal simulations considering a Bi_2Te_3 based thin film super-lattice TE device and circuit level model of the integrated controller [28, 30].

3.2 Module Characterization

The control principles and circuits for energy-efficient cooling and temperature regulation using automatic mode switching of a TE module are verified experimentally

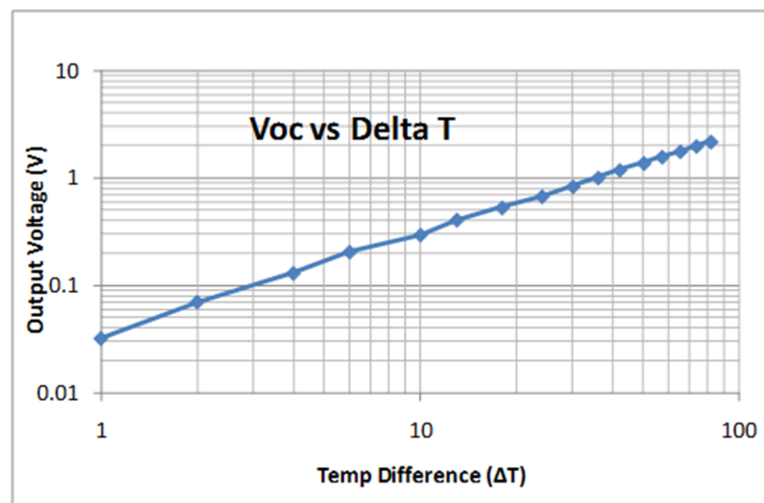


Figure 3.4: TE device [40] performance as an energy harvester

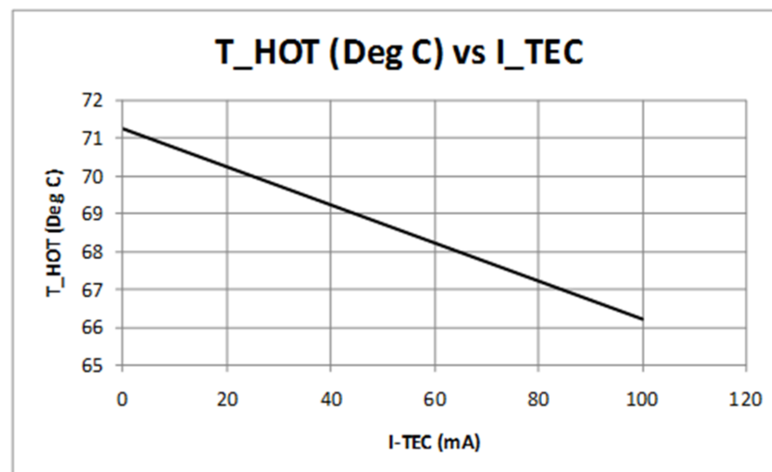
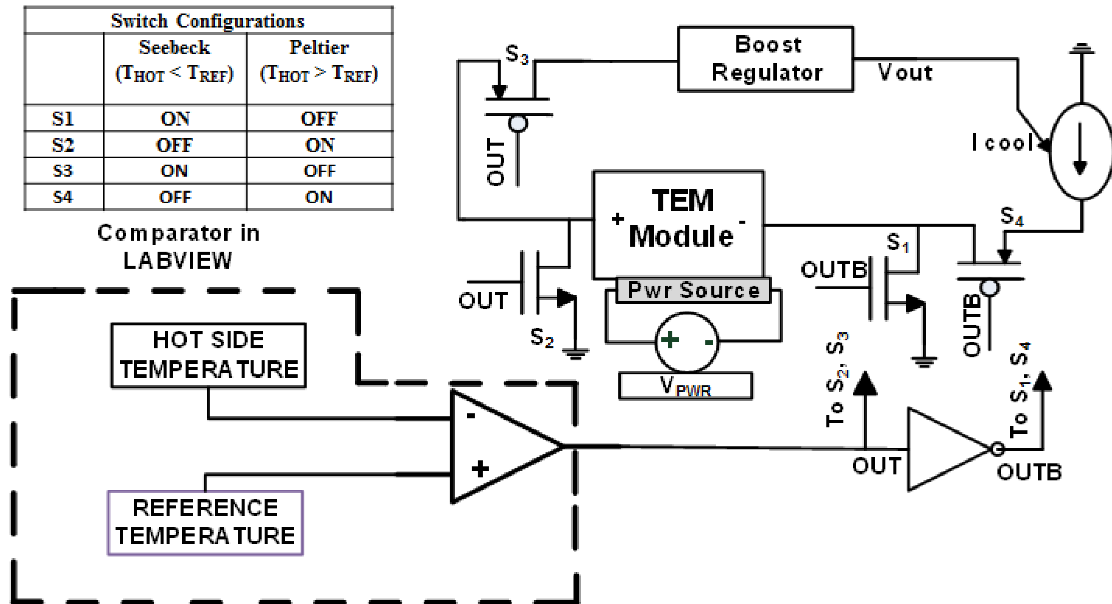


Figure 3.5: TE device [40] performance as a cooler (T_Hot – Hot side temperature)

using a TE device integrated with a heater [39]. The TE module is initially characterized in the harvesting and cooling modes of operation. Figures 3.4 and 3.5 depict the performance of the device as an energy harvester and cooling device.

3.3 Control Principle

Figure 3.3 describes the basic principle of the controller. A simple threshold based controller is used for the TEC-TEG mode switching and temperature regulation. A temperature sensor is considered to estimate the temperature. The proposed controller first senses the operating temperature of the chip. If the chip temperature is higher than a critical threshold, the TEM is switched to the TEC mode by pushing current through the TEM. Once the temperature reduces below the target, TEM reverts to the TEG mode of operation. During TEG mode, the voltage at the TEM output is boosted using a boost converter and stored in capacitor or fed back to a rechargeable battery to support cooling. The TEG-to-TEC transition is controlled by the maximum temperature threshold and the



Switch Configurations		
	Seebeck ($T_{HOT} < T_{REF}$)	Peltier ($T_{HOT} > T_{REF}$)
S1	ON	OFF
S2	OFF	ON
S3	ON	OFF
S4	OFF	ON

Figure 3.6: The TEG-TEC controller design: The overall controller circuit and the switch configuration

TEC-to-TEG transition is controlled by setting a lower temperature threshold (hysteretic control).

3.4 Experimental Implementation

Figure 3.6 describes the overall schematic of the controller. The temperature of the power generating region (the chip) is sensed and compared against a threshold. In the absence of an on-chip temperature sensor, the sensing can be performed by feeding the hot side thermocouple data to the NI PXI DAQ unit for the temperature based control mechanism as discussed in figure 3.2. The sensed temperature is fed to an onboard virtual comparator in LABVIEW which also receives a user defined reference temperature value. The temperature is sensed every Tsense seconds and the output of the comparator (either a 0V signal or +5V signal) is fed to complimentary switches to control the current flow during TEC and TEG modes.

The cooling period essentially is same as the temperature sensing period. When temperature of the IC is below the threshold, switches S1 and S3 turns on connecting the negative terminal of TEM to ground and positive terminal to a boost regulator. This allows harvesting thermal energy and storing it in the output capacitor of the converter. Since the temperature difference across the TE module is expected to be small, a boost converter is used. When the temperature of the IC crosses the pre-defined threshold, the comparator output switches to +5V from 0V. This marks the beginning of the cooling phase and S2 and S4 turn on. S4 connects the current source to the TEM and S2 shorts the positive terminal of the TEM to ground allowing the current to flow. After one fixed cycle of cooling for Tsense seconds, the temperature is again compared and the decision whether to continue cooling for another cycle or to return to the harvesting mode is made

by the virtual comparator. If a high power pulse persists, the TE module continuously switches between the TEG and the TEC mode as long as the temperature oscillates up and down around the reference value. The performance of the controller depends on the sensing time; the response time of the electrical components including the comparator and the switches; and most importantly, the response time of the thermal system. To ensure a stable operation, the response time of the electronic components should be much smaller than the thermal response time.

3.5 Measurement Results

The circuit shown in Figure 3.6 is implemented and a photograph of the system is shown in Figure 3.7 with different system components. A simple heater (Power Source)

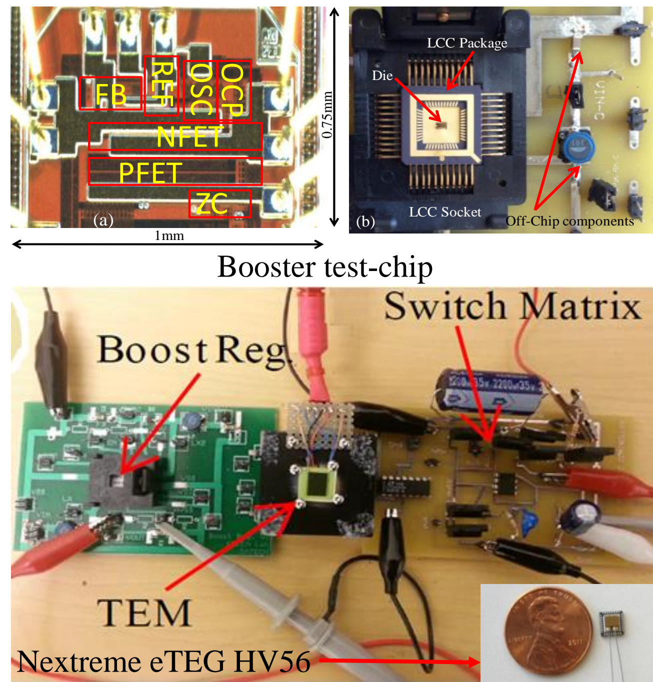


Figure: 3.7: Experimental setup showing the test board, the die-photo of the booster test chip [40], and the Nextreme eTEG HV56 element [39]

is attached with the TEM to emulate the hot temperature surface of IC. The boost regulator used as the harvester IC in the system is fabricated using the 130nm CMOS process node and consumes 110nA at 1V [40]. The synchronous booster is autonomously bias gated and has a battery less operation starting at 265 mV. It generates regulated 1V output from 30mV input and regulated output ranging from 0.78V-3.3V. An efficiency of 83% is obtained for a 10μA load and 85% for a 10 mA load. The details of the boost regulator design and its performance is available in [40]. A commercial TEM [39] is used to generate power from the heat extracted from the heater and to cool it on demand.

Two Thermocouples are placed at both the ends of the TEM (hot and cold sides) to obtain the temperature across the TEM. The TEM module is characterized for both Seebeck and Peltier mode of operation. The heater temperature is increased slowly and at any given temperature differential between the hot and cold side, the maximum power delivered is measured by varying load at the TEM output. The above measurements demonstrate potential of using the same TEM for as both TEC and TEG. A voltage level is applied to the heater to emulate high power mode operation of the chip. Figure 3.8 demonstrates the overall system behavior considering the transient heater levels. Once the heater voltage level increases, the temperature ramps up and once it crosses the reference temperature, regulation process starts and the TEM switches back and forth between the TEC and TEG mode. In the TEG mode it charges the output capacitor which is equivalent to providing energy back to a system battery. During TEC mode the energy is drawn from the system battery. An external current source is used in the experiment which results in a constant current flow through the TE device during the TEC mode. The waveform of the different internal control signals are also shown in Figure 3.8. The

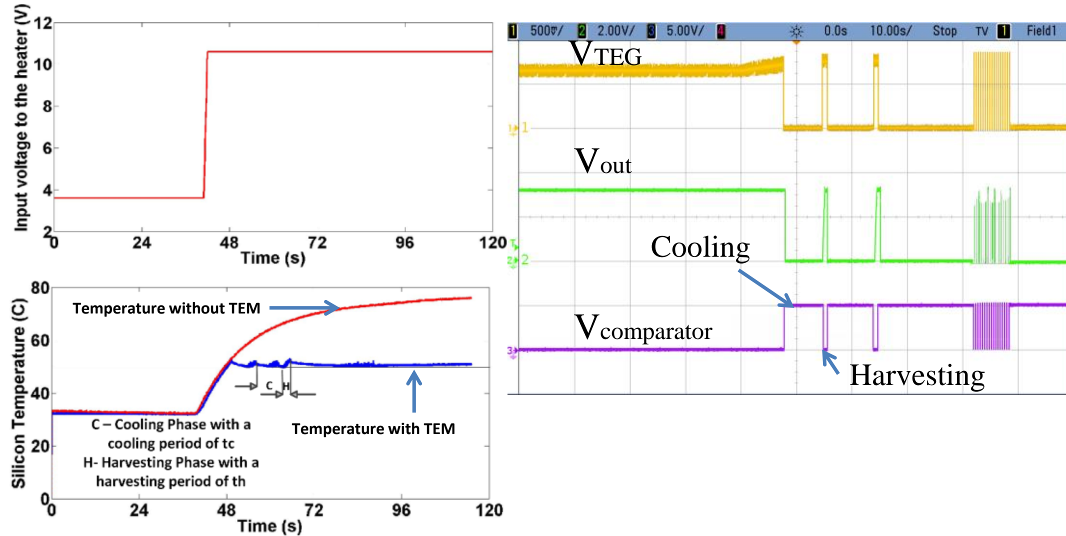


Figure 3.8: Measurement results demonstrating the control system for automated mode swtiching between TEG and TEC depending upon the chip temperature

measurement demonstrates temperature initial temperature regulation when the TE device oscillates between cooling and harvesting mode. Eventually, the temperature cannot be regulated and TE switches to TEC mode to provide cooling and temperature continues to increase although slowly (compared to no TEM case).

To characterize the energy-efficiency of the proposed control system, we vary the heater power level, i.e., generated heat in the chip. Whenever the TE is in the TEG mode, the harvested output energy is computed by monitoring the voltage changes in the output capacitor of the booster. On the other hand, during TEC mode, the consumed cooling energy is measured by monitoring the external current source, i.e., integrating the constant external cooling current over the duration of the TEC mode. The time spent in the TEC mode can be obtained by monitoring the output signal of the comparator. Figure 3.9 depicts the variation of regulation period with different heater levels. The 'regulation period' is defined as the time period over which the controller can maintain the temperature below a pre-defined threshold. Due to the inherently high thermal time

constants of the external TEM-heater combination, the measurement time scales are large.

Temperature is recorded using NI PXI DAQ unit. As expected the regulation period increases with a higher cooling current and lower heater power level (i.e., reduced power density of the chip). However, note that a higher cooling current requires more cooling energy. The energy dissipated during the TEC mode for a given cooling phase is given by: $E_{TEC} = I_{TEC}{}^{2}\ (R_{TEC} + R_{FET}\ )t_{c}$ where, I_{TEC} is the cooling current, R_{TEC} – the internal resistance of the TEM, R_{FET} – the ON resistance of the switches in the cooling path and t_c – cooling period during the cooling phase. E_{TEC} depends on the cooling period tc and the cooling current I_{TEC}. Likewise a lower heater power level, i.e., a reduced heat flux, implies a reduced power output from the TE in the generator mode (i.e. less harvested energy). Therefore, we need to characterize the effect of TEG-TEC control on the energy-efficiency. Figure 3.10 (a) shows the net cooling energy as a function of regulation period for various power density of the heater. The net cooling energy is

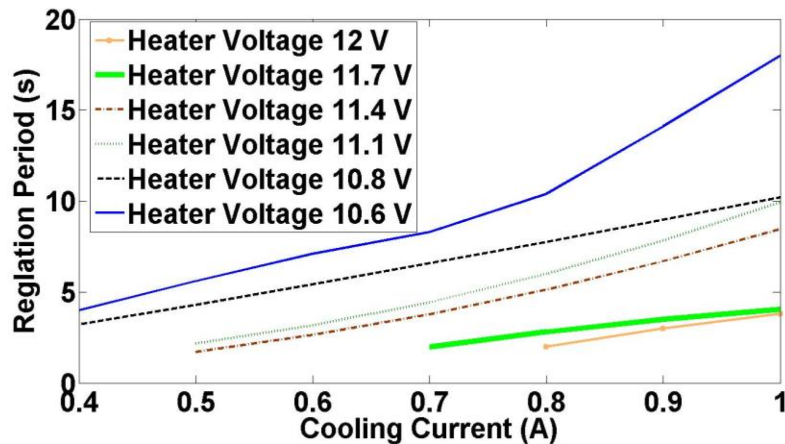


Figure 3.9: Measurement results showing the regulation period as a function of cooling current and heater power density

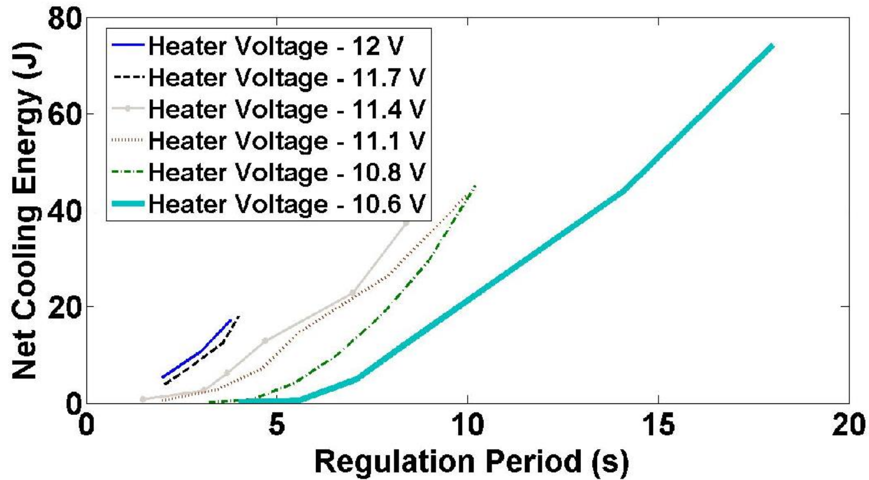


Figure 3.10 (a): The net cooling energy = Cooling Energy (E_C) – Harvested Energy (E_H)

computed by subtracting the harvested energy from the cooling energy. Figure 3.10 (b) depicts the percentage of harvested energy to cooling energy for different heater power density. Prior works on TEC based active cooling considers that TEC remains off when temperature is below threshold, i.e., a threshold based TEC on-off control [28], unlike this work where the TEC makes transitions to a TEG mode. Hence, the percentage of the harvested energy represents the percentage of cooling energy that is saved by the proposed automated TEG-TEC operation, compared to prior works on threshold based TEC on-off control [28].

For each power density, the cooling current is varied following Figure 3.9, to measure the regulation period and corresponding net cooling energy and energy saving with TEG-TEC operation. It can be observed that the automated TEG-TEC mode transition can help reduce the cooling energy required for temperature regulation. Figure 6 shows that at moderate power density, the significant regulation period can be achieved with almost no additional cooling energy. As in a threshold based TEC on-off control TEC remains off when temperature is below threshold, only switches S2 and S4 are

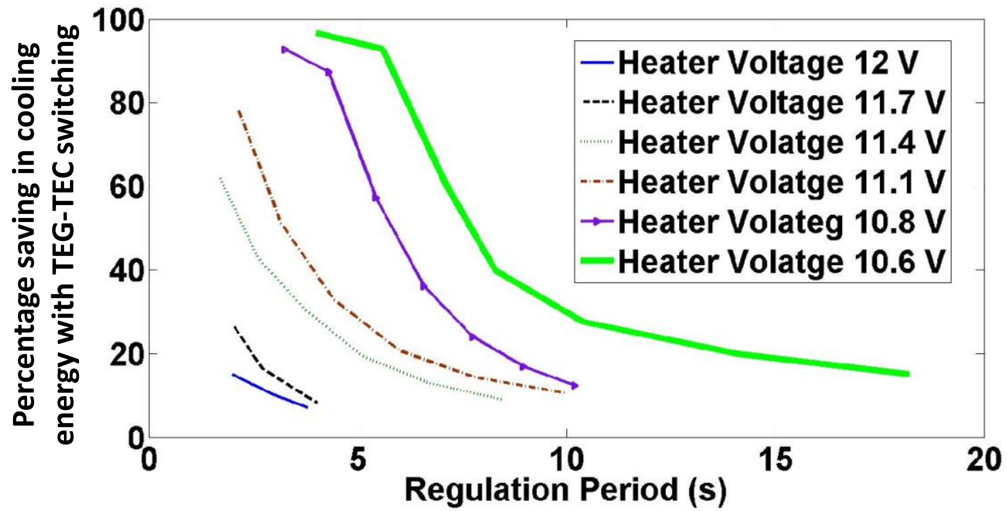


Figure 3.10 (b): The percentage savings in cooling energy over the baseline system where the TEC is turned off when temperature is below threshold (TEC on-off control)

required. Therefore, the overheads of using the TEG-TEC operation proposed in this work, compared to prior work of TEC on-off control, are the boost converter, the switch S1, and the switch S3. However, they do not additional energy dissipation during the TEC mode as they are off. During the TEG mode, these switches results in power loss and reduces the overall harvested energy. Moreover, they also add additional load to the comparator and hence, increases the switching energy loss of the comparator. However, both of these components are much less compared to the cooling energy and have been considered in the analysis of the '*net cooling energy*' shown in Figure 3.10.

3.6 Simulation Analysis Considering Integrated TE Module

The energy efficient use of harvested energy in cooling the same system, can be extended to find "Zero-additional Energy Cooling" (ZEC) point where the system cools without using any additional energy; i.e., the energy required for cooling can be harvested

fully from the extracted energy from the heat generated (a *self-sustained cooling*). While the measurement results using the external TEG and heater experiment shows the possibility of self-sustained cooling, the overall efficiency is limited due to the larger electrical and thermal resistances of the contacts of the TE device. Motivated by the promise shown in the experiments, we study the potential of self-sustained cooling using an integrated TEM (Fig. 3.1) through electro-thermal simulations. A super-lattice TEM integrated inside the package between the chip and heat spreader is used for analysis. The integration of super-lattice Bi_2Te_3 based super-lattice TEMs have been previously demonstrated through experiments [29]. In this work, a 9mm x 9mm full chip package was modeled using SPICE to simulate the thermal and electrical behavior of the TEM based on models developed by Alexandrov et. al. [28]. A single 3mm x 3mm, 8µm thick, 49 couple TEM (made of p-type Bi_2Te_3/Sb_2Te_3 and n-type $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$) is embedded onto the middle of the package in between the TIM, silicon and heat spreader layers. The conduction resistance and capacitance values of the RC thermal model are given by Rcond and C, where L is the thickness of the unit cell, A- the cross-sectional area, K – thermal conductivity, ρ – resistivity and Cp – specific heat.

3.7 Modelling Framework

The framework for autonomous TEC/TEG switching is an improvement over the prior model presented by Alexandrov et al. [28]. The system model considers a silicon chip, thermal interface material (TIM), heat spreader, and heat sink. The TE device is integrated inside the TIM. The model proposed in [28] is improved, by integrating the TEG model to study the automated TEG-TEC mode switching. The 3D distributed RC

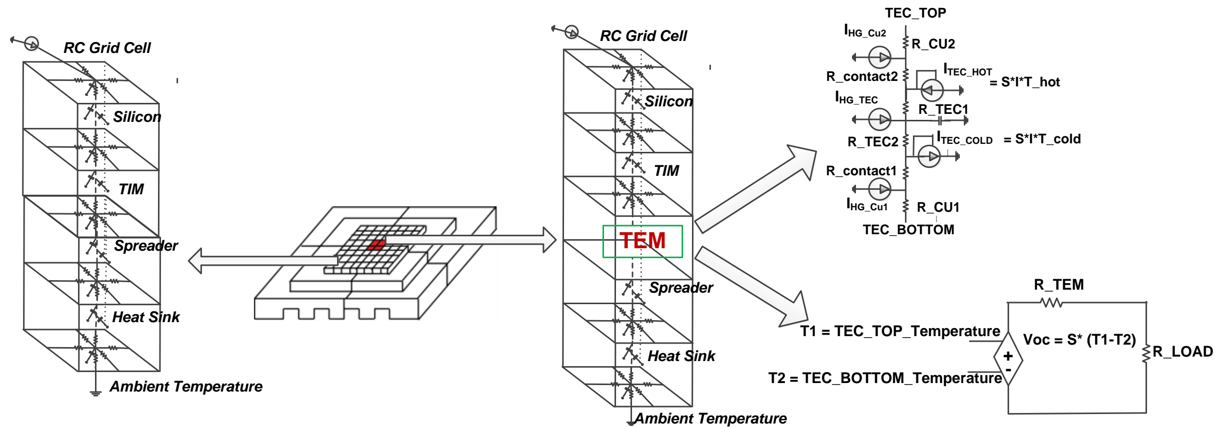


Figure 3.11: The overall thermal simulation model showing the package grid locations without the TEM; Flip chip package; Package grid locations with the Tem; TEG and TEC models of the TEM

based thermal models of the integrated system is presented in Figure 3.11. The TEC behavior using equivalent compact SPICE circuit is considered that accounts for the Peltier cooling effect, the I^2R losses through the contact resistances, and the Joule heating effect [28]. Heat is added at the hot side and is subtracted off at the cold side to model the Peltier cooling. Current sources are also used to model the I^2R losses at the contact regions. Along with the TEC model, the hot and cold side temperatures of the TEM are also used by the TEG compact SPICE model to generate voltage. A voltage controlled voltage source with the hot and cold side temperatures as the controlling parameters is used to model the TEG effect [41]. During the closed loop TEG operation, current flows through the TEG which also results in power loss in the contacts and also Peltier cooling. Therefore, the system model considers the TEC to be always ‘on’; the TEC current is equal to the external current during cooling and to the closed-loop current flowing through the harvesting system during generation. The device parameters and values are chosen based on the results from prior works [28, 29, 41, 42]. A simple behavioral controller is used to model the TEC-TEG mode switching and temperature regulation following the principle/circuit discussed in section 3.3.

3.8 Simulation Results

A transient pulse is fed to the package to simulate the varying high power load operation of an IC. Figure 3.12 demonstrates the overall system simulation considering a varying power pulse. Energy is harvested using the TEG mode when the power is low. Once the power increases the silicon temperature ramps up and once it crosses the reference temperature, regulation process starts. During the regulation period, the TEM switches between the TEC and TEG mode. The silicon temperature falls during the cooling cycle and rises during the harvesting cycle. The inset figure shows a magnified image of the events which occur during the regulation period. Eventually the generated heat increases beyond the cooling capacity of the TEC and temperature continues to rise (TEM remains in the TEC mode). The net effect is the integrated TEC/TEG mode allows the system to sustain a high power pulse for a longer time duration compared to the

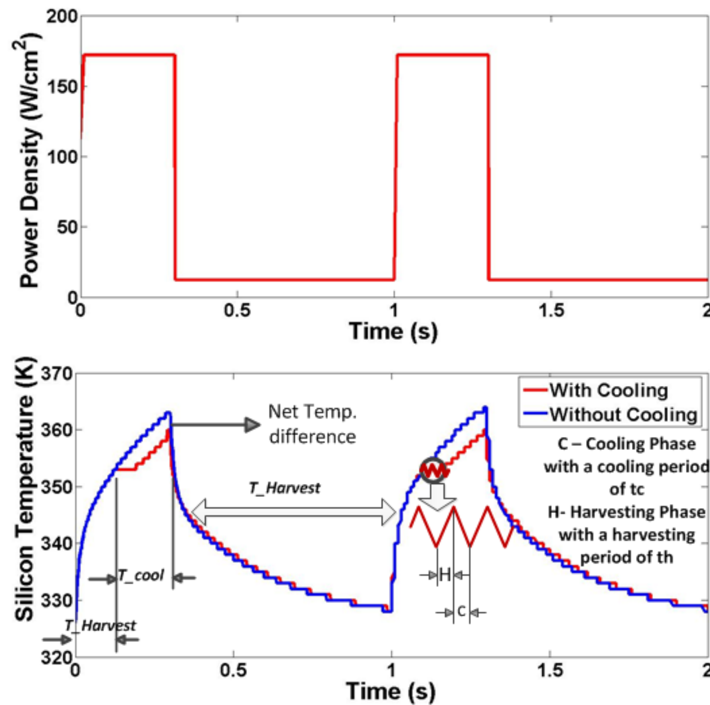


Figure 3.12: Simulation results showing the coupled TEG and TEC operation of the integrated TE module

baseline system. The net cooling energy as a function of regulation period for various high power densities is shown in Figure 3.13. Figure 3.14 shows the percentage of energy saved using the proposed automated TEG-TEC control over conventional approach of threshold based TEC on-off control. As explained earlier, the percentage energy saving is equal to the percentage of the harvested energy. As expected, for lower power levels, the regulation period and the energy saving is higher. The self-sustained cooling (i.e. energy saving ~ 100%) is possible over a considerable (~100s of milliseconds) time duration. As the power level increases, the regulation period reduces and self-sustained cooling is achieved over a smaller regulation period. The simulation results show the potential of self-sustained cooling over ~10s -100s of milliseconds of time duration using automated TEF-TEC switching. Beyond the self-sustained cooling region, the automated TEG-TEC switching helps reduce the net cooling energy.

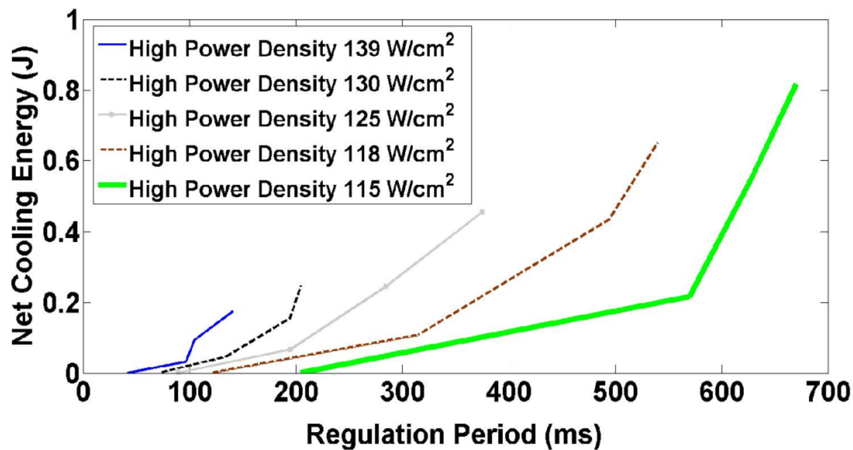


Figure 3.13: Simulation results demonstrating the energy-efficiency improvement: net cooling energy = cooling energy (E_C) – harvested energy (E_H)

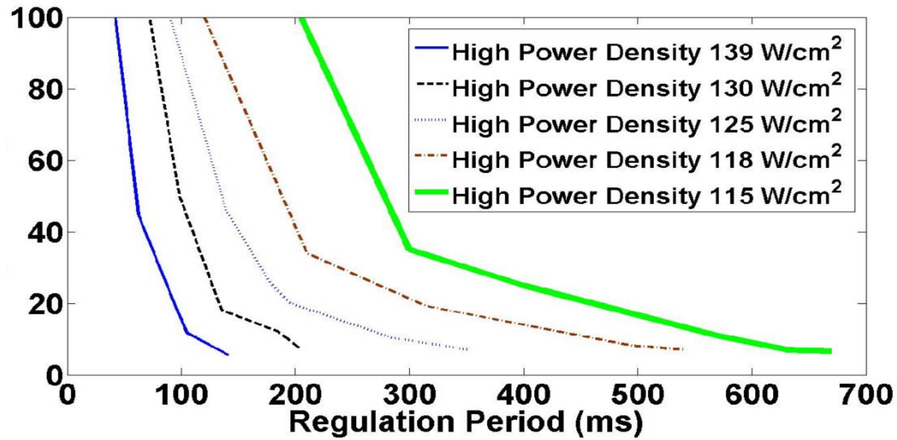


Figure 3.14: Percentage savings in cooling energy over the baseline system when temperature is below threshold (TEC 0n-off control)

3.9 Summary

This chapter presents design and validation of the dynamic autonomous switching capability of a single TEM between the energy harvesting and cooling stages. A control circuit is demonstrated for the automated mode switching. The control principle is verified experimentally using an external TEM module and through simulation considering a super-lattice TEC integrated inside a package. The analysis shows that the proposed automated mode switching can help reduce the total cooling energy for a target regulation period. The potential of self-sustained cooling, i.e., regulation of the temperature with zero additional cooling energy is demonstrated.

CHAPTER 4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

The thesis focuses on energy efficient active thermal management system for hot spot cooling in an integrated circuit. Two fundamental issues of thermal management were covered in this thesis, namely exploring the effects of aging and thermal cycling on thermoelectric cooling performance over time and designing a system to facilitate energy efficient cooling.

Thermoelectric coolers have lately shown promise in localized hot spot cooling. Its performance degrades over time with thermal cycling which is indicated by the change in the thermoelectric properties due to the formation of microscopic cracks at the TE device leg interfaces. A full chip package model with a TE module embedded in it was used to analyze the impact of thermal cycling on the cooling capabilities over the progressing cycles. Material degradation over time was incorporated into the model by changing the thermoelectric properties at specific cycle intervals. The simulation results showed that the maximum amount of cooling obtained cooling at 45,000 cycles was significantly less when compared to the initial starting cycle. Also, the cooling required over progressing cycles changes. Hence, an adaptive circuit which counts the number of times the TE module is activated is required so that a specific algorithm could supply the cooling current accordingly and tune the other system parameters. With hot spot cooling now a feasible approach, in a power and battery life restrained circuit world creating an energy efficient cooling system is the order of the day.

The second part of the thesis focuses on methods to design a cooling system which makes use of the extra heat that escapes into the ambient air through the heat sink from the system. The Peltier mode is activated only at specific intervals and during the non-cooling mode of operation (waste heat) traverses through the system and remains utilized. To utilize this waste heat, the TE module is autonomously switched between the cooling and harvesting mode of operation. A control system for dynamic mode switching of the TE device has been presented and experimentally demonstrated using a commercial off-the shelf TE module and discrete electronic components. Full package simulations considering an embedded super-lattice TE module were also performed. The analysis showed that the total cooling energy required for a target regulation period can be reduced by operating the TE module in the two modes. Also, self-sustained cooling operation without the need of extra cooling energy is demonstrated using the system.

4.2 Spatial Extension of TE Module and Future work

Hot spot cooling techniques traditionally has required a TE module to be placed directly on the top of the hot spot to facilitate temperature control around the region. This has served the purpose till date. However, a large amount of heat is displaced from the chip through the non-hot spot regions into the ambient atmosphere. The temperature gradients need not be as high when compared to the hot spots but would be sufficient enough to generate a substantial amount of energy. A large amount of energy could potentially be harvested for cooling if the entire chip could be covered with the thermoelectric module. By this, the thermoelectric material around the hotspot could be harvesting energy simultaneously while the hotspot is being cooled.

Using the full chip package model discussed in section 3.7, the effect of spatial extension of the TE module is studied through simulations. For a chip with a total area of 81 mm^2, the TE module [43] was initially placed over a hot spot area matching the TE module's dimensions – 2mm x 3mm. As a modification to the base case, the TE module size was increased to 81 mm^2 to cover the entire chip while the hot spot area was kept the same as the base case (2 mm x 3 mm). Figure 4.1 explains the two different cases that were used for the analysis. While the hot spot base level power density was kept at 50 W/cm^2, the base level power density for the rest of the chip excluding the hot spot region was kept at 20 W/cm^2 and 40 W/cm^2 respectively. Final temperature of the package with 0 A of cooling current is noted for each of the cases so that the regulation temperature is set to 10 K less than that of the no cooling (0A) case. The regulation temperature for the baseline case, modified case with back ground power of 20 W/cm^2 and 40 W/cm^2 were set to 372 K, 371 K and 407 K respectively.

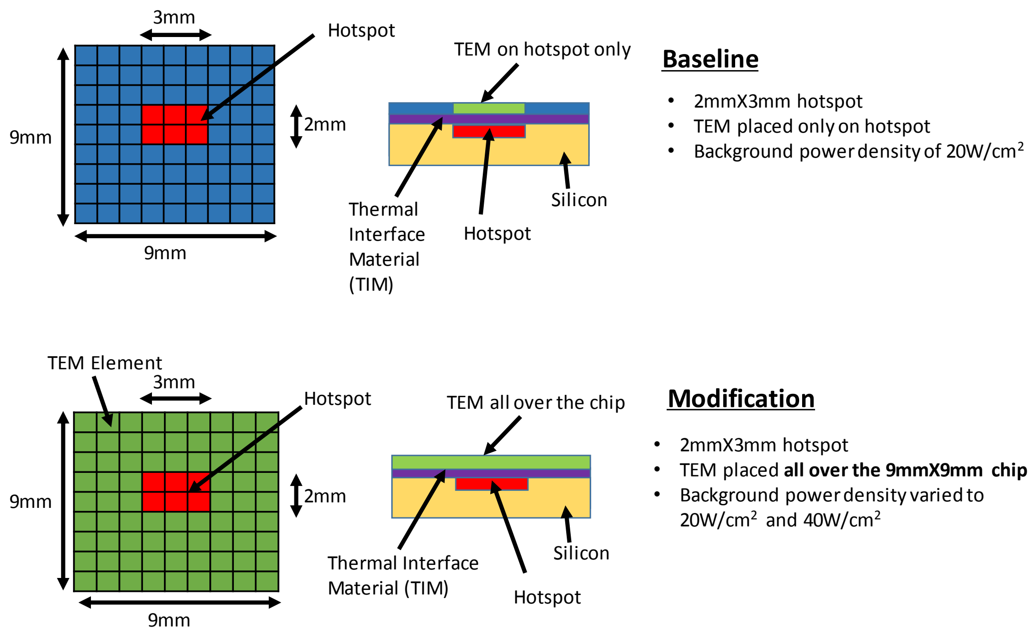


Figure 4.1: TE Module spatial extension – Two different configurations

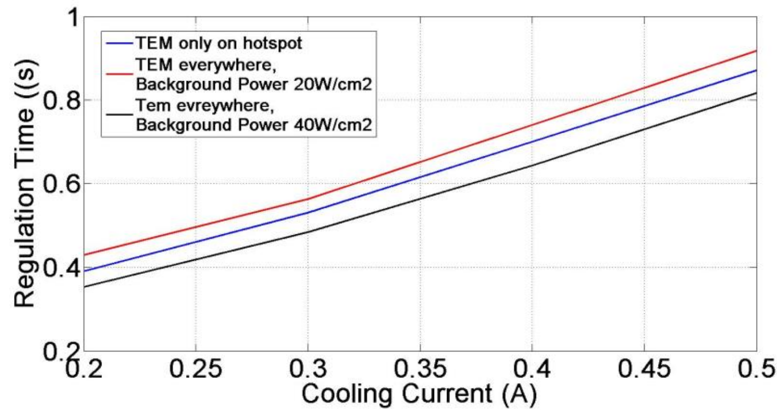


Figure 4.2: Regulation period as a function of cooling current and power level

As the cooling current is varied, the regulation period increases due to the Peltier effect and the variation of regulation period with cooling current is shown in figure 4.2. For the baseline case, the regulation period is lower as it covers the hot spot only. Increasing the size of the TE module to cover the entire chip increases the regulation period as the TE module has a better conductivity than the TIM and this causes a greater drop in temperature. However, increasing the background power of the non-hot spot regions to 40W/cm^2 increases the background temperature of the system thereby reducing the overall regulation period.

To pursue an energy-neutral operation, i.e. harvesting all the required energy for cooling from the TE module itself, the hotspot receives a pulsed power pulse wherein the 'on' period of the pulse denotes the high power density level and the 'off' period represents the base power level density. During the 'on' period of the pulse, the chip temperature starts to ramp up and is regulated at a user-defined level for some period of time. Energy is harvested during the 'on' period (whenever the TE module switches to the harvesting mode of operation) as well as the 'off/idle' period of the pulse. The 'on'

period of the pulse is equal to the regulation period so that the energy required to regulate the temperature is obtained from harvesting during the duration of the pulse. The thus obtained duty cycle is referred to as the 'duty cycle for unit conversion ratio'. Figure 4.3 depicts the same.

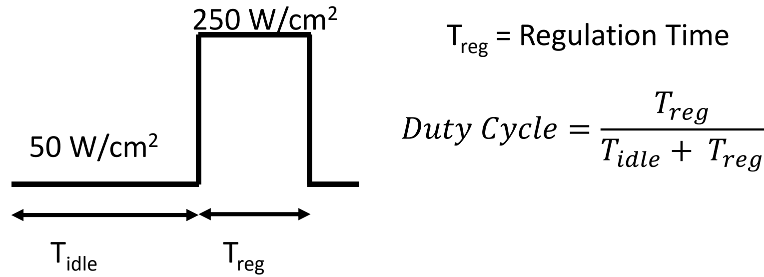


Figure 4.3: Duty cycle for unit conversion ratio

Figure 4.4 shows the variation of the duty cycles obtained for the three cases. As the cooling current increases, the active duty cycle is seen to fall drastically because the required energy for cooling has a quadratic dependence on cooling current (I^2R) and due to the high resistance of the TE module. For the modified case where in the TE module covers the entire chip, there is a large increase in the duty cycle, with energy neutral duty

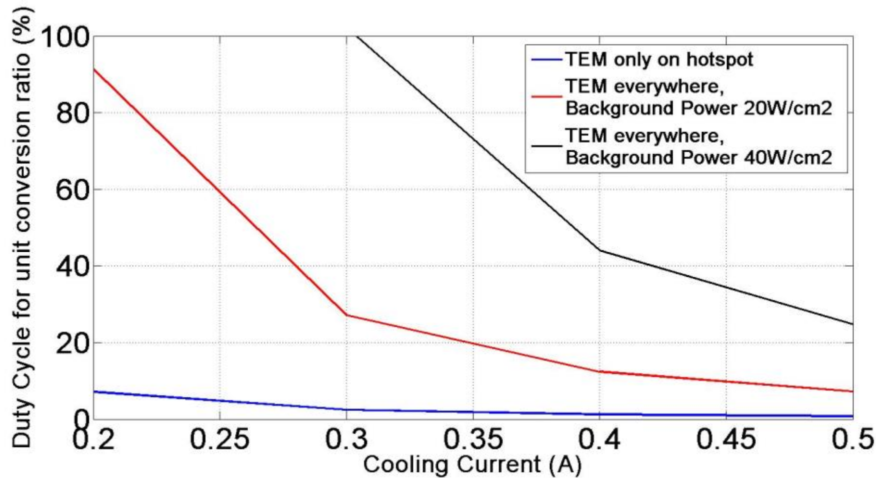


Figure 4.4: Variation of duty cycle over cooling current

cycles approaching 90% at low cooling currents. This is primarily because of the area of harvesting elements have increased by roughly one order (from 6mm^2 to 81 mm^2). Also, the TE module elements not on the hotspot continue to harvest even when the hotspot is being cooled. Increasing the background power level to 40W/cm^2 has a positive impact on the duty cycle as more energy can be harvested, thus allowing even higher duty cycles to be achieved. This can be seen from figure 4.3, where almost 100% duty cycle can be maintained with 0.3 A of cooling current. However, this does not mean that a power flux of 250W/cm^2 can be maintained indefinitely and throttling mechanisms would be invoked after the regulation period elapses.

The simulation results show that the spatial extension of the TE module does have an improvement in terms of energy-efficient operation capabilities. The proposed extension can be extended to 3D ICs and other non-uniform power topologies. Figure 4.5 shows a typical non-uniform power distribution in an IC. The amount of power/heat dissipated over the different blocks changes over time and hence a block not acting as a hotspot at one instance might have higher temperature profiles at a later instance. In this scenario, the TE module grid element have to controlled by an algorithm which co-ordinates with the processor to determine which grids need to harvest and which of them

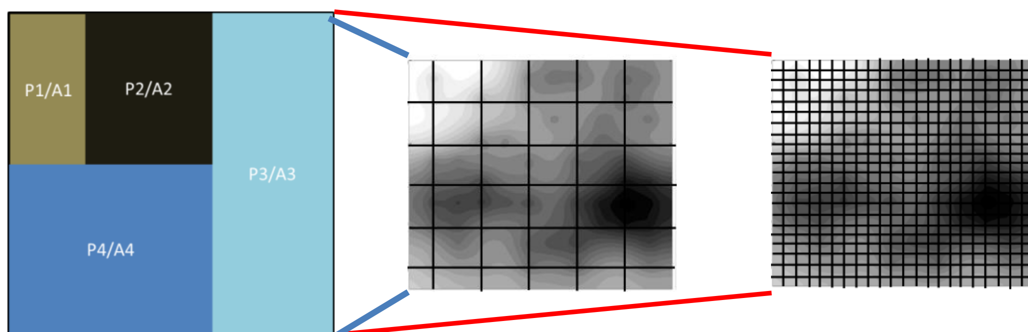


Figure 4.5: Non-Uniform power topology resulting in two different power drop at different instances *{adapted from [44]}*

should cool over time. The circuitry to aid the switching of the grid elements efficiently should also be designed in a cost-effective way. The same idea can be extended to a 3D IC wherein, the hotspot locations in each layer shifts from time to time. Figure 4.6 shows an example of a three layer 3D IC wherein the hotspots are denoted by the highlighted grid locations. Here, each layer requires a TE module grid structure to be fabricated on top of them. An independent controller circuit for each of the layers might also be required to switch the grid elements between the two modes of operation.

Lastly, a more concise method of formulating the degradation of thermoelectric material should be developed. The inherent losses occur due to the formation of cracks in the TE legs as a result of both shear stress and thermal stress acting on them. The package properties could also change over time due to the effect of thermal cycling. Hence, a full package cum TE module co-simulation framework in a multi physics solver domain is necessary to accurately compensate for the effects due to aging.

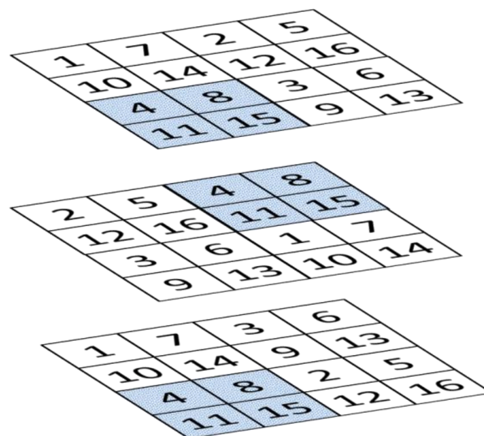


Figure 4.6: Hotpsot locations in a 3D IC ***{[adapted from [44]}***

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