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PD Activity in Void Type Dielectric Samples for Varied DC Polarity

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Abstract- **This paper discusses the DC testing of a dielectric sample (with voids) under DC conditions. The ramp test method was employed to assess whether the tests were repeatable. Three DC ramp tests were performed in quick succession. The polarity of the first/third tests was positive and the polarity of the second test was negative. The resultant partial discharge activity was analyzed for each series of tests and compared for positive and negative conditions. The results show that the inclusion of a negative ramp between two positive ramps enabled similar PD activity to be recorded in the first and second positive ramp tests. The negative cycle was used to re-initialise the test sample and allows trapped charge to migrate enabling similar PD activity in the subsequent positive ramp test. Changes in PD behavior were observed in the distribution of PD data between the tests.**

I. INTRODUCTION

The condition monitoring of a HVDC transmission link is critical as any loss of the link would bring significant costs in repair and lost revenue from power transfer activities. A valuable monitoring technique is the investigation of Partial Discharge (PD) an important area of research is on the detection of PD emission as an indicator of incipient insulation failure in a HVDC system. This work has been conducted as the emission of partial discharges from HVDC cables is yet to be fully understood to prevent such downtimes.

Partial discharge detection under AC conditions is well understood but still many measurement challenges remain. Under AC conditions the sinusoidal variation of voltage results in the voltage polarity reversing every half cycle. PD activity is strongly reliant on the applied voltage. The variation of voltage over the phase of the sine wave leads to a phase related PD activity. Common insulation defects exhibit different phase related PD behavior.

The field of PD detection under DC conditions has received less attention to date due to the lack of applications involving DC voltage. The main basis of PD detection under DC conditions was developed at TU Delft [1]. This work has been built on by a number of research groups around the world [2-4].

Voids are the most common defect in HVDC cable systems. In this paper, a dielectric sample with voids (from here on will be known as a voids-type dielectric sample) was tested under DC conditions. The dielectric sample was first subjected to AC excitation to ensure the sample yielded the expected PD activity. The phase resolved partial discharge (PRPD) plot was used to confirm the dielectric sample was producing void type

PD [5]. The ramp test method [6-7] was employed to investigate whether the DC PD testing was repeatable. Three series of DC ramp tests were performed on the dielectric sample in quick succession. The first and third series of ramp tests were of positive polarity. The second series of ramp tests was of negative polarity. During each series of ramp tests, the resultant PD events were recorded for subsequent analysis. The polarity reversal was applied to re-initialise the sample and dislodge trapped charge within the voids in the dielectric. Previous work [8] have shown that repeated DC ramp tests of positive polarity led to a reduction of PD events and change in PD behavior. The overall aim was to investigate whether the sample remained as active in subsequent DC ramp tests following re-initialisation.

II. Method

This section details the dielectric sample under test, the AC test method and the DC test method adopted during tests on the dielectric sample.

A. Sample under test

The sample under test had five air bubble voids introduced during the casting of an epoxy resin disk. The diameters of the five air bubbles were; 0.59, 0.46, 0.43, 0.32 and 0.21 mm. The voids are midway of the 2 mm thick, 90 mm diameter epoxy disk. On the upper and lower faces of the epoxy disk, plain electrodes were bonded directly above the five voids. The plain electrodes were 19 mm in diameter and the edges of the electrodes had a radius of curvature of 5 mm.

B. AC test method

AC testing was conducted on the sample to confirm that the dominant source of PD from the dielectric sample was of internal PD. The test circuit is as detailed in Fig. 1, a
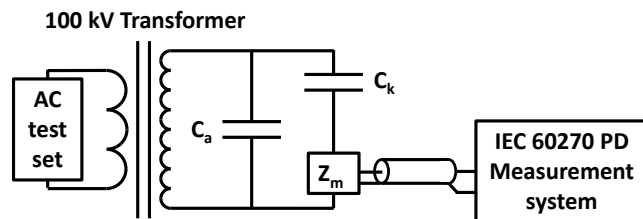

Fig. 1. AC test circuit. Consisting of the the AC test set, single phase 100/0.38 kV transformer, coupling capacitor (C_k), sample under test (C_a) and a measuring impedance (Z_m) connected to the IEC standard PD measurment system.

measuring impedance and IEC 60270 standard measurement system was used to detect and record the PD activity. The AC voltage was increased until repetitive and sustained PD was observed on the PD measurement system. The IEC standard measurement system was set to record 10 seconds of PD data. The data recorded was the charge of the PD event and the phase of occurrence with respect to the AC supply.

AC PD analysis was performed using a phase resolved partial discharge (PRPD) plot to show the phase related PD behavior. Common PD producing defects have characteristic behavior which can be evident on a PRPD plot [5].

C. DC test method

A DC ramp test method [6-7] was used to apply a controlled and repeatable voltage profile to the dielectric sample. The voltage steps in the ramp profile were determined from the peak value of the AC inception voltage (V_R). The four voltage steps used were $V_R/2$, V_R, $3V_R/2$ and $9V_R/5$. Originally the voltage ramp had three steps but in previous work it was found necessary to extend the ramp by a further step ($9V_R/5$) to ensure the dielectric sample was active [8]. The hold period for the three lower voltages was 4 minutes. The hold period for the final voltage ($9V_R/5$) was 80 minutes to enable more PD data to be gathered for analysis purposes. The data under analysis in this paper is the 80 minutes of hold data at $9V_R/5$.

In this work three series of voltage ramps were applied to the dielectric sample in quick succession. Initially a positive series of DC ramp was applied to the sample, followed by a negative series of DC ramp and finally another series of positive DC ramp. The sample was grounded between voltage ramp tests whilst the test circuit was adjusted to enable the reversal of the voltage polarity (swapping the direction of the rectifying diode). In the negative voltage ramp the same four hold voltages were applied with only the polarity reversed.

The DC test circuit (Fig. 2) comprises of the AC power supply, transformer and diode rectifier to enable a DC voltage to be applied across the IEC 60270 test circuit. The measurement of PD was performed by a HFCT and IEC standard PD measurement system to detect and record PD activity for subsequent analysis.

Under DC conditions there is no phase reference and the measured quantities were the charge magnitude and the time of occurrence. The lack of a phase reference means that DC PD analysis is more suited to statistical analysis techniques. Analysis of PD activity was performed by plotting the charge magnitude of the PD events over time, cumulative charge over time, histograms to show the spread of data and the numerical assessment of skewness and kurtosis for the DC PD data sets.
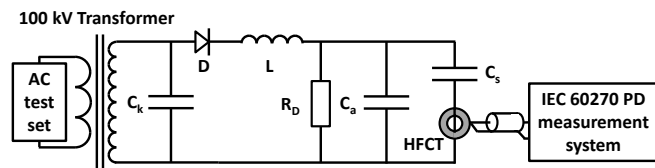
100 kV Transformer

Fig. 2. DC test circuit. Consisting of the AC test set, single phase 100/0.38 kV transformer, AC coupling capacitor (C_k), diode (D), inductor (L), 230:1 resistive divider (R_D), sample under test (C_a), DC coupling capacitor (C_s) and a HFCT connected to the IEC standard PD measurment system.

III. Results

The test results for the AC and DC tests are detailed in the followings sections.

A. AC test results

The AC voltage at which sustained and repetitive PD was observed was 8 kV rms. The PRPD plot of PD activity at 8 kV rms is detailed in Fig. 3. The PRPD plot shows that the PD activity occurs in the first and third quadrants before the peaks in the AC voltage waveform. The PD behavior on the PRPD plot is typical of void-type dielectric samples. The peak value of the inception voltage (V_R=11.3 kV) was used to derive the four voltage steps used in the DC ramp profile.

B. DC test results

AC testing confirmed the inception voltage of PD activity and the peak value of the inception voltage was used to derive the four voltage steps in the DC ramp profile. The magnitude of the voltage steps was 5.6 kV, 11.3 kV, 17 kV and 20 kV. The data under analysis in this work was the 80 minutes of data for the final hold voltage at 20 kV.

Fig 4 details the charge magnitude of the PD events over the 80 minute hold. The number of PD events remained consistent with 57 recorded in the first hold at +20 kV, 57 in the hold at -20 kV and 58 recorded during the second hold at +20 kV. The largest PD events occurred during the 80 minute hold at -20 kV and by comparison the PD magnitude during the first hold at +20 kV was generally smaller.

The cumulative charge over time plot is illustrated in Fig. 5. The first positive hold has the least cumulative charge accumulation over the 80 minute hold and the second positive hold has the most. The cumulative charge plot clearly shows the effect of the negative ramp test on increasing the overall PD activity recorded in the dielectric sample. The main difference in PD activity between the first and second positive tests is the larger initial PD events that occurred at the start of the 80 minute hold. Otherwise the two plots are similar throughout the hold over 80 minutes.

Histograms were used as a visual representation of the relative spread of PD activity for the three ramp tests. The charge magnitude histograms for the 80 minute hold data for the three ramp tests are detailed in Fig. 6. Void-type dielectric samples produce a distribution on a histogram with a characteristic peak to the left hand side of the distribution [1].
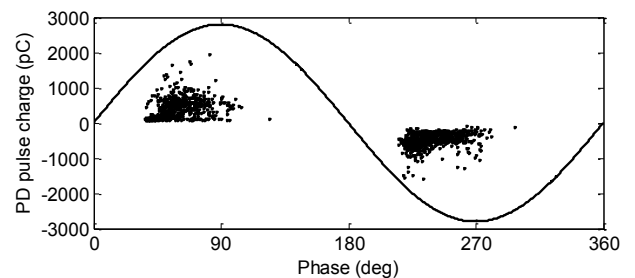

Fig. 3. PRPD plot from AC testing of the void-type dielectric sample at 8 kV rms. PD charge and phase of occurrence shown by dots and the test voltage shown by solid black line.
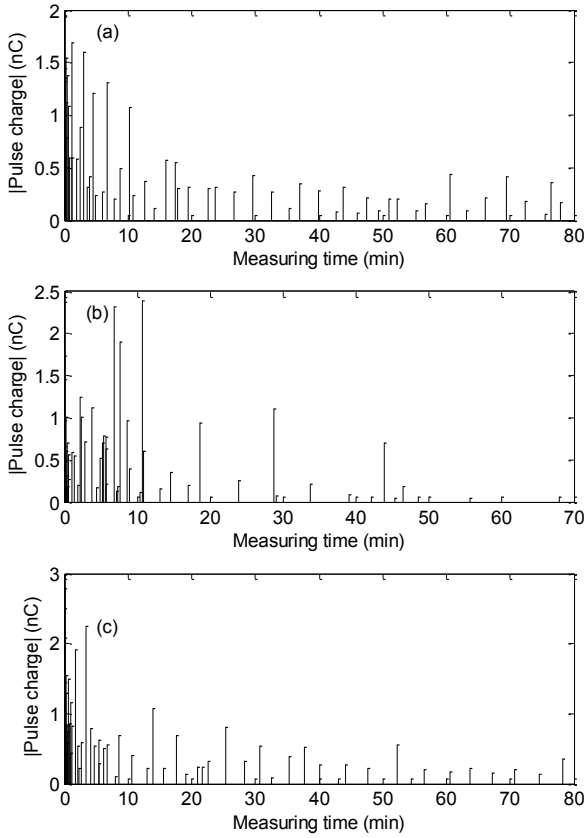
Fig. 4. Time versus charge magnitude plots for the dielectric sample whilst voltage held at ±20 kV (a) first positive ramp 80 minute hold at +20 kV (b) negative ramp 80 minute hold at -20 kV (c) second positive ramp 80 minute hold at +20 kV.

Fig. 6 Histogram of charge magnitude for the dielectric sample whilst voltage held at ±20 kV (a) first positive ramp 80 minute hold at +20 kV (b) negative ramp 80 minute hold at -20 kV (c) second positive ramp 80 minute hold at +20 kV.

The characteristic peak on the left hand side of the histograms remained throughout the three ramp tests and actually was accentuated by prior application of the negative ramp test before the final positive ramp test. In previous work it was found that this characteristic peak reduced when exposed to repeated positive DC ramp tests [8].

A numerical approach to assess the distribution of PD data was achieved through the calculation of skewness and kurtosis [9] for the data sets. The symmetry of the distribution of data around the mean is measured by skewness and kurtosis assesses the relative spread of data. Table I details the skewness and kurtosis of the three data sets in this study. The skewness increases between the data in the first positive hold
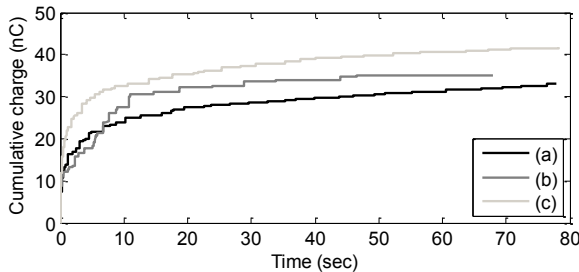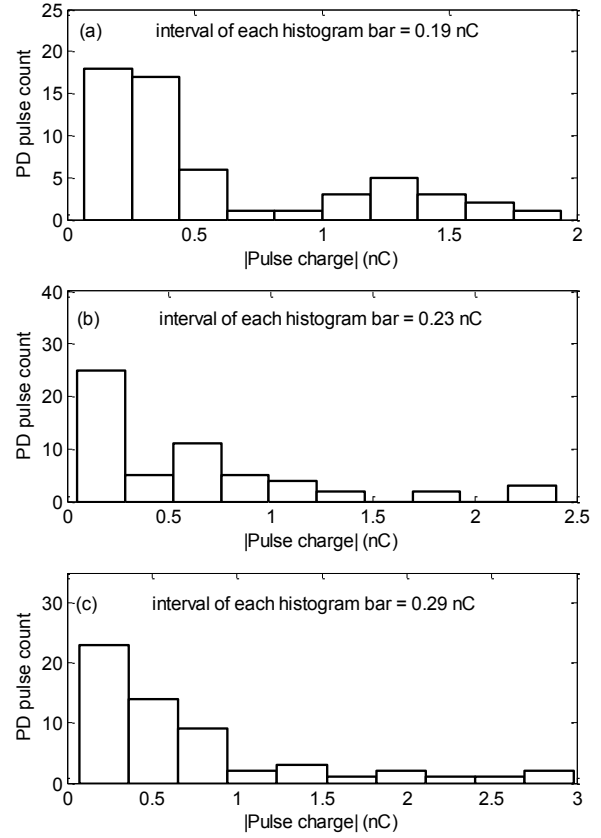
and the second positive. This confirms that more data in the data set is moving to the left hand side of the histogram in the second positive test. Similarly the kurtosis also increases between the first positive hold and the second positive. This change suggests that the spread of data is reducing and is becoming more leptokurtic.

IV. Discussion

AC PD testing was employed as a sense check to confirm that PD behavior from the dielectric sample was as expected. The AC PD test also provided the starting point for DC ramp testing through the identification of the inception voltage of PD. The peak value of the AC inception voltage (V_R) was used to derive the four voltage steps ($V_R/2$, V_R, $3V_R/2$ and $9V_R/5$) in the DC ramp test.

The ramp test profile [6-7] was modified with an additional hold period added at $9V_R/5$. The additional voltage step at $9V_R/5$ was added to ensure the sample emitted PD activity. The extended hold period at $9V_R/5$ was increased from 30

Fig. 5. Cumulative plot of charge magnitude for the dielectric sample whilst voltage held at ±20 kV (a) first positive ramp 80 minute hold at +20 kV (b) negative ramp 80 minute hold at -20 kV (c) second positive ramp 80 minute hold at +20 kV.

TABLE I
SKEWNESS AND KURTOSIS FOR THE DC RAMP TESTS (A) FIRST POSITIVE RAMP 80 MINUTE HOLD AT +20 KV (B) NEGATIVE RAMP 80 MINUTE HOLD AT -20 KV (C) SECOND POSITIVE RAMP 80 MINUTE HOLD AT +20 KV

	(a)	(b)	(c)
Skewness	1.1	1.5	1.7
Kurtosis	2.8	4.9	5.3

minutes to 80 minutes to enable more data to be gathered for the statistical analysis of the resultant PD data.

The ramp test method allowed controlled DC PD tests to be performed on the dielectric sample. The defined profile of the ramp test ensured that the voltage levels and hold periods were identical. The repeatability was important as two positive ramp tests were directly compared in this work. This approach enabled the effect on PD activity in the second positive ramp test caused by a negative ramp test to be studied.

The use of the time vs charge plots offered limited use in terms of analysis of the PD data and it was more suitably used as an initial inspection of the PD data to ensure the PD measurement system was not saturated due to an incorrect attenuator setting.

Interesting results were obtained through the analysis of cumulative charge accumulation over time. The cumulative charge observed in the negative and second positive tests was higher than that that of the initial positive test. The number of PD events in all the tests was similar but more importantly larger PD events were recorded in the negative and second positive tests.

Histograms provided a visual representation of the spread of PD data for the three ramp tests. In all of the tests the histograms had the characteristic peak to the left hand side of the distribution typical of histograms for void-type dielectric samples. It was observed that the characteristic peak was enhanced with more data falling into the histogram bins in the low charge range. The extension of the tail at the right hand side of the histogram was also evident with larger PD events recorded at the beginning of the negative and second positive tests.

The numerical approach to assess the distribution of PD data through the calculation of skewness and kurtosis confirmed the behavior observed on the histograms. The skewness increased between the first positive test and the second positive test. The more positive skew suggests that the mean was moving to the left of the data set as confirmed by the histograms. Similarly the kurtosis increased between the first positive test and the second positive test. The more positive kurtosis value suggests that the PD data had a reduced spread evident by the accentuation of the peak on the left hand side of the histograms.

The approach of using a negative ramp test in between two positive ramp tests ensured that the dielectric sample emitted a similar number of PD events over the three 80 minute hold periods. In contrast when subsequent positive ramp tests were performed in quick succession in previous work [8] the number of PD events reduced. The negative ramp test allowed the dielectric sample to be re-initialised.

IV. Conclusions

This paper has introduced a modification to the process of performing DC PD testing on a dielectric sample using a ramp test method. The voltage steps in the ramp test method were derived from the peak value of the AC inception voltage of sustained and repetitive PD. In this work the ramp profile was modified with an additional voltage step added at $9V_R/5$ and this hold was extended to 80 minutes.

In this paper three ramp tests were performed in quick succession on a void-type dielectric sample. The polarity of the first and third tests was positive and the second test was negative. The polarity reversal was performed to see the effect on the subsequent positive ramp test when the sample had been exposed to reverse polarity for an extended time period.

A number of approaches were used to analyze the PD activity. The approached used in this paper were the plotting of charge magnitude of PD events over time, cumulative charge over time, visual inspection of histograms and the numerical assessment of skewness and kurtosis.

The test results presented in this paper show the effect of reversing the polarity of DC voltage applied to a void-type dielectric sample. The sample remained as active in the first (57) and second positive (58) ramp tests in terms of the number of PD events recorded. Some changes in the behavior were observed in terms of maximum PD charge recorded and in changes to the distribution of the PD data were observed. The consistency of PD activity is expected to be caused by the re-initilisation caused by the polarity reversal of the negative ramp test.

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