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Hybrid Modular Multilevel Converter with Three-level Cells in HVDC Transmission System

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Abstract—A hybrid MMC with reduced three-level (TL) cells is proposed. As well as the dc fault blocking capability, the proposed hybrid MMC provides the benefits of: lower conduction losses; fewer diode and switching devices, and; fewer shoot-through modes. Guidelines are developed to determine the required number of three-level cells to block a dc-side fault. It is also demonstrated that a further reduction in the number a three-level cells is possible if a rise in cell current and voltage is acceptable. This reduction is investigated. A lower number of three-level cells reduces losses and capital cost further. The hybrid MMC with the reduced number of three-level cells proves to be the most attractive approach compared with other MMCs and hybrid MMCs. The semiconductor count and conduction loss are 92.1% and 90.3% respectively of that of the MMC based entirely on full-bridge cells, without exposing the semiconductors to significant fault currents and over-voltages. The simulation results demonstrate the feasibility of the proposed hybrid converter.

Keywords—dc fault blocking; HVDC transmission; hybrid modular multilevel converter (MMC)

I. INTRODUCTION

The modular multilevel converter (MMC) is a voltage source converter (VSC) for high-voltage dc (HVDC) transmission systems. The vulnerability of half-bridge (HB) based MMC (HB-MMC) to dc faults is a major issue that limits its application in HVDC systems [1, 2].

FB based MMC (FB-MMC) can block dc faults but requires twice the number of semiconductors in the conduction path [3]. The hybrid MMC proposed in [4] uses HB and FB cells in each arm to obtain the dc fault blocking capability and reduce the losses. However, it is at the expense of higher voltage stresses for sub-modules. Reference [5] proposes the clamp double (CD) sub-module to reduce the losses and block the dc fault. However, for the dc fault, the CD cell only utilizes half of the possible cell capacitor voltages to block dc faults.

To achieve the full dc fault blocking capability with reduced losses and semiconductor costs, the three-level (TL) cells with two active clamp switches is proposed in [6]. It fully utilizes the cell voltage to suppress the fault current and achieve the dc fault blocking capability. As a result fewer HB sub-modules have to be replaced by the TL cells to provide

adequate voltage to block the dc fault in the hybrid MMC, yielding lower conduction losses and capital cost. How to furthur improve the converter performance, however, is not considered.

In order to overcome the above problems, the hybrid MMC with reduced TL cells is presented. In Section II, the design principle and comparison with competitor hybrid MMC systems are addressed. The dc fault blocking capability is assessed in Section III. Section IV concludes the paper.

II. HYBRID MMC WITH REDUCED TL CELLS

A. Determination of TL Cell Number

Fig. 1 shows a generic version of the TL cell based hybrid MMC (TL-HMMC). All the devices of the TL-HMMC are arranged to endure the same voltage stresses, $V_c = V_{dc}/(2g+h) = V_{dc}/N$, where V_{dc} is the dc link voltage, h and g are the HB and TL cell numbers per arm respectively, and N is the equivalent cell number per arm where $N = 2g+h$. The on-state loss can be reduced by choosing a suitable ratio between the TL cell number g and HB cell number h, while still providing adequate reverse voltage to block the dc fault current. The process of choosing g and h is detailed in this section.
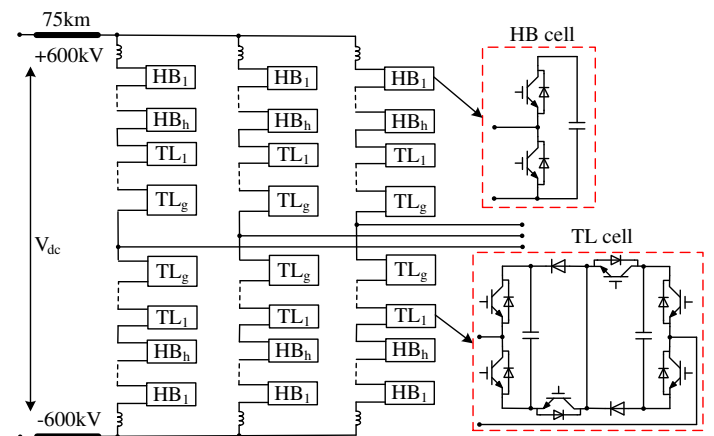

Fig. 1. Three-level cell based hybrid MMC (TL-HMMC) with dc fault blocking and minimized losses.

Once the dc fault is detected, typically within a few tens of microseconds, all the switches of TL-HMMC are turned off and the fault current flows through the anti-parallel diodes of HB cells. As a result the HB cells on the arms of the TL-HMMC do not contribute any voltage to block the dc fault current forced by the ac line voltages. However, the dc fault currents can be blocked by the voltage impressed by the series-connected capacitors of the TL cells which are inserted into the fault current path from the ac side to the dc side.
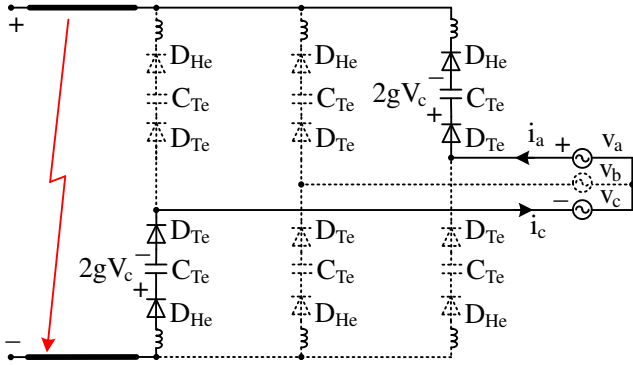

Fig. 2. Equivalent circuit of three-level cell based hybrid MMC (TL-HMMC) during dc fault demonstrating that the combined TL cell voltages ($4gV_c$) oppose input line voltage, v_{ac}.

The proposed TL-HMMC has inherent dc fault blocking capability that eliminates the ac grid contribution to the dc side fault current. With the TL cells turned off, the capacitors of the TL cells present a virtual dc link which drives the ac side current back towards zero, despite the collapse of the actual dc link voltage, Fig. 2. When TL cells are blocked, their cell capacitors charge for positive and negative arm currents, and this suppresses the uncontrolled inrush current from the ac side, as long as the converter remains blocked. In Fig. 2, the HB and TL cells per arm are modelled as a diode D_{He} and the series connection of diode D_{Te} and capacitor C_{Te} respectively. The internal resistances and forward voltages of D_{He} and D_{Te} are $(N-2g)R_{on}$, $4gR_{on}$, $(N-2g)V_f$ and $4gV_f$ respectively, where R_{on} and V_f denote the internal resistance and forward voltage of cell diode and can be obtained from its datasheet. The equivalent capacitor C_{Te} equals to $C/(2g)$ where C is the cell capacitance and its voltage is $2gV_c$.

After the fault is detected, the TL-HMMC is blocked and the impressed voltage that blocks the dc fault is the sum of the upper arm TL voltages on one phase and lower arm TL voltages on another phase. For example, in Fig. 2 phases 'a' and 'c' conduct as, in the particular instant, v_{ac} is the highest line voltage hence the upper arm of phase 'a' and the lower arm of phase 'c' conduct. If the initial impressed voltage ($4gV_c$) is higher than peak line voltage (V_{ac}), the fault current from the ac side will be forced to zero quickly and the fault current blocked, while the TL cell voltages remain constant approximately.

If the initial impressed voltage ($4gV_c$) is lower than the peak line voltage, the fault currents will not drop to zero immediately and may increase. The fault currents will charge the TL cell capacitors and the impressed voltage will increase. The fault currents will then reduce to zero and the impressed

voltage increases to approximately the line voltage peak. Thus, the fault current from the ac side can be suppressed and the fault current blocked on the condition that the TL cells can still function safely with an increased capacitor voltage $(1+r)V_c$, where r is the per unit voltage increase of the TL cell.

If all the HB and TL cells are to have the same voltage stress, to block the fault the following expression can be derived:

$$\frac{\sqrt{3}}{2}mV_{dc} \le 4g\frac{V_{dc}}{N}(1+r) \le 2V_{dc} \tag{1}$$

The number of TL cells required per arm, to block the dc fault, can then be determined:

$$\frac{\sqrt{3}mN}{8(1+r)} \le g \le 0.5N. \tag{2}$$

After the TL cell number g is chosen, the number of HB cells required per arm is simply

$$h = N - 2g. \tag{3}$$

Conventionally, the modulation index m and the per unit voltage increase of TL cell r are set at 1 and 0 respectively, according to the design approach in [4]. This means the initial impressed voltage is higher than peak line voltage and the fault currents are quickly suppressed, as previously mentioned. According to (2), the number of TL cells is governed by:

$$\frac{\sqrt{3}mN}{8(1+r)} = \frac{\sqrt{3}\times1\times N}{8\times(1+0)} = \frac{\sqrt{3}N}{8} \approx 0.22N \le g \le 0.5N. \tag{4}$$

B. TL-HMMC with Reduced TL Cells

To further reduce the semiconductor cost and improve the system efficiency, the TL-HMMC with reduced TL cells is proposed. When designing the HVDC system, the modulation index m is usually around 0.8 to enable control of the system with decoupled active and reactive powers and to guarantee system dynamics. Meanwhile, the cell's voltage margin is required and set around 50% conventionally to guarantee normal operation with the capacitor voltage ripple (±10%) and the high frequency voltage spikes caused by the parasitic inductances [7-9].

When calculating the number of TL cells required for a given system to block the dc fault, smaller m and larger r means fewer TL cells are needed, according to (2). Thus higher efficiency and lower semiconductor cost are expected. For the TL-HMMC with reduced TL cells, the number of semiconductors N_{con} in the current path per phase is smaller than that of TL-HMMC with normal TL cell number:

$$N_{con} = 2h + 8g = 2N + \frac{\sqrt{3}mN}{2(1+r)} < 2N + \frac{\sqrt{3}N}{2}. \tag{5}$$

When the modulation index m and the per unit voltage increase of the TL cell r are set at 0.8 and 0.2 respectively, the minimum number of TL cells is

$$\frac{\sqrt{3}mN}{8(1+r)} = \frac{\sqrt{3}\times 0.8 \times N}{8\times(1+0.2)} \approx 0.15N. \tag{6}$$

Thus the number of semiconductors in the current path N_{con} is calculated as 2.6N while it is 2.88N for both CD cell based hybrid MMC (CD-HMMC) and conventional TL-HMMC with normal TL cell number, Table I.

TABLE I.   COMPARISON BETWEEN TL-HMMC WITH REDUCED TL CELLS AND OTHER ALTERNATIVES.

ITEM (per phase)	CD-HMMC	Conventional TL-HMMC	TL-HMMC with reduced TL cells
IGBTs	4.88N	4.88N	4.6N
Diodes	6.64N	5.76N	5.2N
Semiconductors	11.52N	10.64N	9.8N
Semiconductors in current path	2.88N	2.88N	2.6N

Based on the conventional HB-MMC, the TL-HMMC with reduced TL cells replaces a lower fraction of HB cells (2×0.15N=0.3N) with the TL cells. This distribution of TL and HB cells reduces the number of power devices in the conduction path and improves the efficiency; meanwhile the dc fault can still be blocked without significant overcurrent and overvoltage. Its required semiconductors and the conduction losses are reduced to 92.1% (9.8N/10.64N) and 90.3% (2.6N/2.88N) respectively compared the conventional TL-HMMC with normal TL cell number, as shown in Table I. This yields higher efficiency and lower power device capital cost.

The fault currents of TL-HMMC with reduced TL cells do not cease to zero immediately and will charge the TL cell capacitors. However, with the increase of TL cell voltages, the fault currents are suppressed to zero in a short time and the dc fault can still be blocked. Also, the amplitude of fault current and the increase of TL cell voltages can be controlled to acceptable values. The TL cell voltage is slightly higher than the expected value, as the TL cell capacitors are charged by the fault currents until the fault currents are suppressed to zero. The resultant arm currents during the fault are dependent on the phase angle of the ac voltage at the time of the fault. As a result, the voltage increase of TL cells in different phase arms are different.

III.   DC FAULT BLOCKING CAPABILITY

The performance of the TL-HMMC with reduced TL cells in high-voltage applications is assessed using a model of a point-to-point HVDC link with TL-HMMCs at each station, Fig. 3. The parameters of the two converters (TL-HMMC$_1$ and TL-HMMC$_2$) are the same, Table II.

The simulated scenario assumes the system shown in Fig. 3 is subjected to a permanent pole-to-pole dc short circuit fault at the mid-point of the dc cable at t=0.75s. All the switches are turned off after 25μs from fault initiation. Based on the TL-HMMC in Section II A, the TL cell number g is reduced from 6 (0.22N) to 4 (0.15N) with the HB cell number h=16 obtained from (3) and (6). The dc fault blocking capability is demonstrated in Fig. 4.
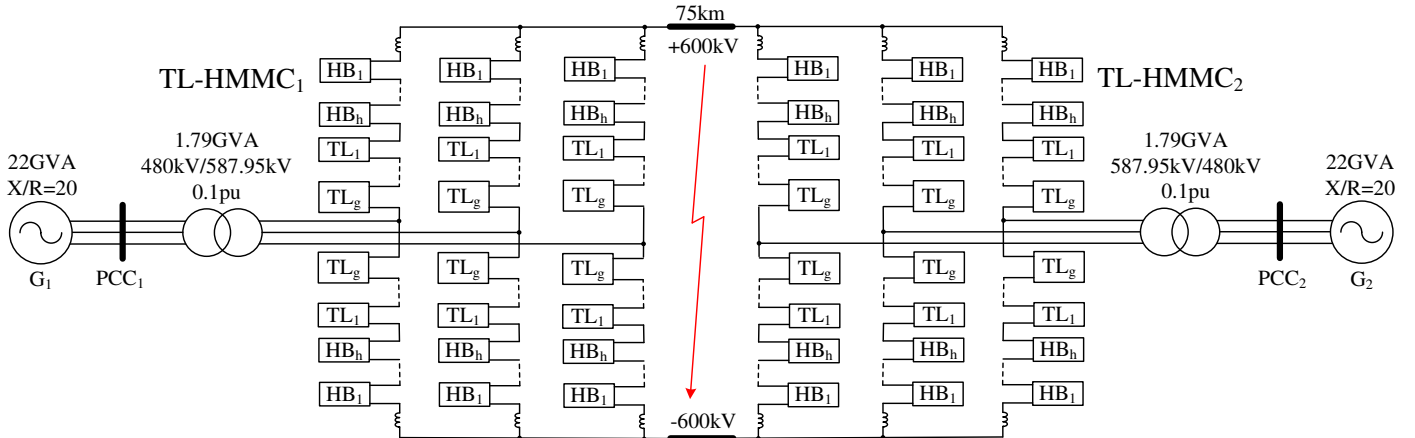

Fig. 3.   Point-to-point HVDC link with TL cell based hybrid MMCs (TL-HMMC1 and TL-HMMC2).

TABLE II.   NOMINAL PARAMETERS OF MODELED TEST SYSTEM.

PARAMETER	Nominal value
rated power	1.6GW
capacitor voltage of HB and TL cells	50kV
equivalent cell number N per arm	24
capacitance of HB and TL cells	793μF
arm inductance	94mH

The dc-link voltage drops to zero when the pole-to-pole dc fault occurs at t=0.75s, Fig. 4 (a). Following the fault, the gating signals of the two converters are inhibited, which activates their inherent dc fault blocking capabilities due to the TL cells in each arm. As the impressed voltage is lower than the line voltage peak, the fault currents will not drop to zero immediately. The three-phase currents, arm currents and dc current exhibit fault currents even though the TL-HMMCs are

blocked, thus the anti-parallel diodes still tolerate fault currents. However, the current stress increase during the fault is less than 0.45pu and lasts less than 1ms, Fig. 4 (j). This overcurrent can be tolerated by the diodes due to the design margin and overcurrent capability of the diodes.

Shown in Fig. 4 (k) and (l), all the capacitors of HB and TL cells remain balanced fluctuating around 50kV before the fault. After the permanent dc fault occurs, the TL cell capacitors are charged by the fault currents and their voltages V_{Tu} and V_{Tl} increase following the inhibition of TL-HMMCs. Meanwhile, the voltages of HB cells (V_{Hu} and V_{Hl}) remain constant as the fault currents only flow through their anti-parallel diodes. The fault currents charge the capacitors of TL cells to no more than 59.8kV (V_{Tu} and V_{Tl}) while the HB voltages (V_{Hu} and V_{Hl}) remain stable.

The TL cell does not require larger cell capacitance than that of conventional HB cells. The chosen capacitor voltage ripple determines the capacitance. In a practical application, the capacitor voltage ripples are usually set somewhere in the range ±5-10% to reduce the project cost [10-12]. Thus, the

energy stored in the MMC can be derived between 20kJ/MVA and 40kJ/MVA. In this paper, the voltage ripple is set within this range but at ~±5%, as shown in Fig. 4 (k) and (l). The cell capacitance is inversely proportional to the capacitor voltage ripples. As a result, when the capacitor voltage ripple is set at ±10%, the cell capacitance can be reduced and the energy stored in the MMC is still in the range of 20-40kJ/MVA suggested by [10-12]. In other words, the energy stored in the TL-HMMC depends on the intended capacitor voltage ripple. When the voltage ripple is set at ±10%, the stored energy is still in the range 20-40kJ/MVA.

With the voltage increase in the TL cells, the fault currents eventually reduce to zero after 60ms from fault initiation with the fault current peaks less than 1.45pu. The fault current and voltage stresses caused by the dc fault are still controlled well with acceptable values. The three-phase ac currents and arm currents are regulated to zero within 60ms of the fault, resulting in zero power exchange between the converters and their corresponding ac grids, Fig. 4 (c-f).
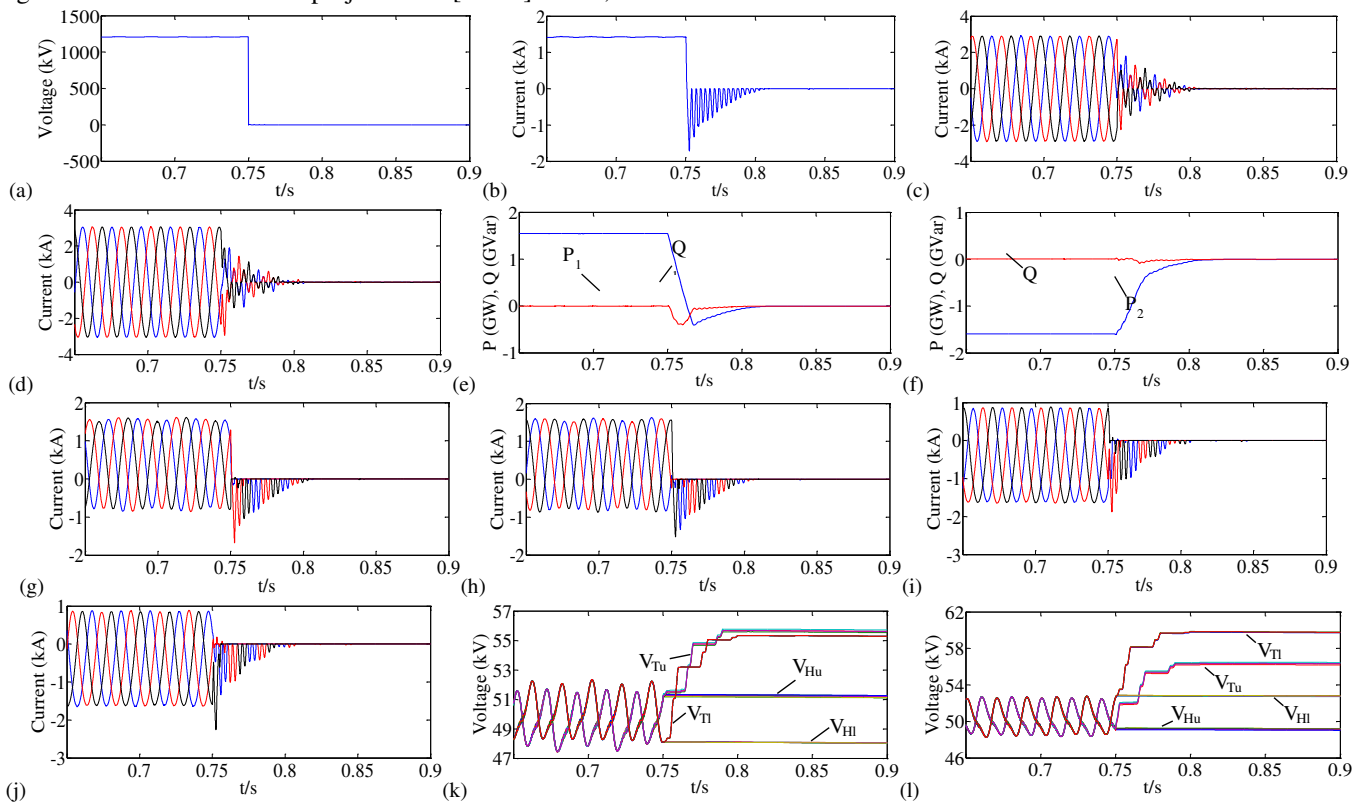

Fig. 4. DC fault blocking waveforms of TL-HMMCs with reduced TL cells (g=0.15N). (a) DC voltage. (b) DC current. (c) Three-phase currents of TL-HMMC1. (d) Three-phase currents of TL-HMMC2. (e) Active and reactive powers of TL-HMMC1. (f) Active and reactive powers of TL-HMMC2. (g) Upper arm currents of TL-HMMC1. (h) Lower arm currents of TL-HMMC1. (i) Upper arm currents of TL-HMMC2. (j) Lower arm currents of TL-HMMC2. (k) Capacitor voltages of HB and TL cells for TL-HMMC1. (l) Capacitor voltages of HB and TL cells for TL-HMMC2.

IV. CONCLUSION

The TL-HMMC with reduced TL cells is presented and its operation is detailed. Instead of blocking the fault immediately, the TL-HMMC with reduced TL cells (g=0.15) achieves dc fault blocking capability by charging the TL cell capacitors to an acceptable value without exposing the semiconductors to

significant fault currents. It demonstrates better overall performance compared with all other hybrid MMC topologies by achieving a compromise between performance during faults and performance during normal operation. Its semiconductor number and conduction losses are reduced to 92.1% and 90.3% of that for conventional TL-HMMC respectively, yielding lower semiconductor costs and higher

efficiency. Simulation results demonstrate, even with reduced TL cells, the TL-HMMC can still block the dc fault without significant fault currents and over-voltages.

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