# A Modular Multilevel Based High-Voltage Pulse Generator for Water Disinfection Applications

Mohamed A. Elgenedy, *Student Member, IEEE*, Ahmed Darwish, Shehab Ahmed, *Senior Member, IEEE*, and Barry W. Williams

***Abstract*—The role of irreversible electroporation using pulsed electric field (PEF) is to generate high voltage (HV) pulses with a predefined magnitude and duration. These HV pulses are applied to the treatment chamber until decontamination of the sample is completed. In this paper, a new topology for HV rectangular pulse generation for water disinfection applications is introduced. The proposed topology has four arms comprised of series connected half H-bridge modular multilevel converter cells. The rectangular pulse characteristics can be controlled via a software controller without any physical changes in power topology. The converter is capable of generating both bipolar and monopolar HV pulses with micro-second pulse durations at a high frequency rate with different characteristics. Hence, the proposed topology provides flexibility by software control, along with hardware modularity, scalability, and redundancy. Moreover, a cell's capacitance is relatively small which drastically reduces the converter footprint. The adopted charging and discharging process of the cell capacitors in this topology eliminate the need of any voltage measurements or complex control for cell-capacitors voltage balance. Consequently, continuity of converter operation is assured under cell malfunction. In this paper, analysis and cell-capacitor sizing of the proposed topology are detailed. Converter operation is verified using MATLAB/Simulink simulation and scaled experimentation.**

***Index Terms*—Modular multilevel converters (MMC), pulsed electric field, high voltage pulses, water disinfection.**

## I. Introduction

PULSED electric field (PEF) generators are applied for electroporation, that is a process in which a cell membrane is subjected to high electric field [1].

Manuscript received April 1, 2016; revised August 4, 2016 and accepted September 5, 2016. This work was supported by a National Priorities Research Program (NPRP) grant NPRP (7-203-2-097) from the Qatar National Research Fund (QNRF).

M. A. Elgenedy is with the Department of Electronic and Electrical Engineering, University of Strathclyde, G1 1RD Glasgow, U.K., and also with the Electrical Engineering Department, Faculty of Engineering, Alexandria University, Alexandria 21544, Egypt (e-mail: mohamed.elgenedy @strath.ac.uk).

A. Darwish, and B. W. Williams are with the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow G11XQ, U.K. (e-mail:ahmed.mohamed-darwish-badawy@strath.ac.uk barry.williams@strath.ac.uk).

S. Ahmed is with the Department of Electrical and Computer Engineering, Texas A&M University at Qatar, Doha 23874, Qatar (e-mail: shehab.ahmed@qatar.tamu.edu).

Usually, the targeted cell membranes are of microorganisms to be decontaminated. This is required when bacterial decontamination is sought in an irreversible electroporation, for example in water purification and in the food industry [2].

The parameters selection of the generated PEF is application dependent. However, voltage magnitude, pulse duration, repetition rate and pulse shape are the most important parameters. Hence, the main target of PEF generators is to generate a pulse of high-voltage (HV) across the terminals of the treatment chamber (which contains the substance) for sufficient pulse duration [3]. Among the different pulse shapes, rectangular pulses have high effective pulse areas; hence they are preferred for PEF application in water treatment [3].

The HV pulses can be monopolar and bipolar. The monopolar pulses continuously subject the cell membrane to an electric field in a fixed direction, and thus the membrane cannot recover. Alternatively, bipolar pulses subject the cell membrane to mechanical stresses in addition to electrical stresses, hence can expedite the lysing process [4].

For effective lysing for water disinfection, the pulse voltage should be at least 10 kV with pulse duration of a few micro-seconds (that is, 1 to 10 μs) [5].

Generating HV rectangular pulses, either monopolar or bipolar, is an established topic in the literature. Classically, Marx generators, pulse forming networks, and Blumlein lines are applied in PEF applications [6]. However, due to the evolution of power electronic switches, with high voltage withstand and fast ON/OFF switching operation, numerous solid-state based HV pulse generators have been proposed. Examples of solid-state pulse generators vary from mimicking the classical generators, such as the Marx generator [7], to emerging new topologies and converters for generating the HV pulses [8]-[16].

An important aspect in the newly developed HV pulse generators is modularity, which offers redundancy and robust pulse generation operation. In [8], the authors utilized several capacitor-diode voltage multiplier modules such that, with proper semi-conductor switching, the capacitors charge in parallel then discharge in series across the load which allows generation of HV pulses from a low voltage input AC supply. In [9] modularity is achieved via connecting several flyback converters in series/parallel in order to fulfill the output pulse

requirements. Although these topologies are modular, they are limited to monopolar pulse generation of a predefined duration.

Exploitation of the modularity in modular multilevel converters (MMC) is addressed in literature, where the half-bridge (HB) MMC cell, shown in Fig. 1a, is utilized to sequentially charge the MMC cell capacitors and then discharge them in series across the load [10]. However, extending this system to more than 3 kV pulses requires series connection of the used diodes, and it is only capable of generating monopolar pulses. In [11] and [12] a modified HB-MMC cell, shown in Fig. 1b, is used in a two arm topology (or, a single leg from the three-phase based MMC converter), the modified cell allows sensorless operation of the topology at a particular switching sequence of the MMC cells while generating the HV pulses. In [11] and [12] the default pulse generation is bipolar, however monopolar pulse generation is possible when changing the load ground point.

This paper proposes a topology based on the conventional HB-MMC cells that can generate both monopolar and bipolar HV rectangular pulses. Pulse generation is controlled via a software controller, hence no physical changes are required in the power topology. Although the default pulses generated by this converter are bipolar and monopolar rectangular pulses with uniformly distributed null periods, the converter software controller can be programmed to generate other different customised rectangular pulses namely: a train of variable-frequency rectangular bipolar pulses; a train of variable-duration bipolar rectangular pulses; and a train of variable-duration bipolar rectangular pulses with combined positive and negative null periods. Thus, the proposed converter provides software flexibility and hardware modularity, scalability, and redundancy.

The cell capacitors are responsible for clamping the voltage across the cell switches, thus the voltage stresses are equally distributed on the converter switches. The adopted charging and discharging patterns of the cell capacitors in this topology eliminate the need of any voltage measurement or complex control to provide cell-capacitors voltage balance. Moreover, in case of cell failure, the converter is able to continue functioning without interrupting converter operation. The topology utilizes small cell capacitance, hence its footprint is significantly reduced in comparison to conventional MMC converters used in HVDC transmission applications.

The proposed converter is introduced in section II, its operation principle outlined in section III, analysis and design given in section IV, and simulation and experimental result are present in sections V and VI respectively.

## II. Proposed Converter Topology

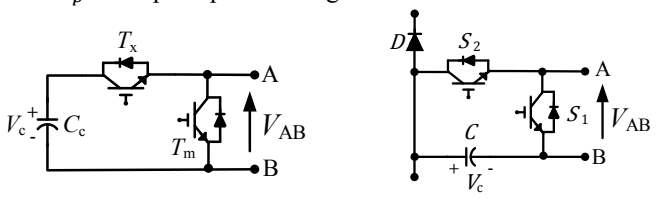
The proposed circuit topology is shown in Fig. 2. It consists of four MMC arms (Arm $z$, where $z \in \{1, 2, 3, 4\}$) forming together an H-bridge connected to supply voltage $V_s$ via an inductor $L_s$. Each arm is formed of $N$ series connected MMC cells, depending on the desired output voltage magnitude. Each arm comprises an arm inductor $L_a$ to supress the inrush current between the cell capacitors during their insertion. Each cell has a capacitor $C_c$ in series with an auxiliary insulated gate bipolar transistor (IGBT) switch/diode $T_x$ and both are parallel with a main IGBT switch/diode $T_m$, see Fig. 2. Depending on the switching sequence of the complimentary switches $T_m$ and $T_x$, the cell-terminal voltage $V_{AB}$ is either equal to the capacitor-voltage $V_c$ or zero as illustrated in the switching table in Fig. 2.

The proposed converter is capable of generating the bipolar ($v_{bi}$) and monopolar ($v_{mono}$) HV pulses shown in Fig. 3a and 3b respectively. The controlling parameters are namely: the repetition time ($T_s$) and the pulse duration ($t_p$). The generated pulses can be defined by the time durations in (1) and (2) for bipolar and monopolar pulses respectively, see Fig. 3.

$$v_{bi} = \begin{cases} +V_p\,, & 0 \geq t > t_p \\ 0\ (positive\ null), & t_p \geq t > ½T_s \\ -V_p, & ½T_s \geq t > ½T_s + t_p \\ 0(negative\ null)\,, & ½T_s + t_p \geq t > T_s \end{cases} \quad (1)$$

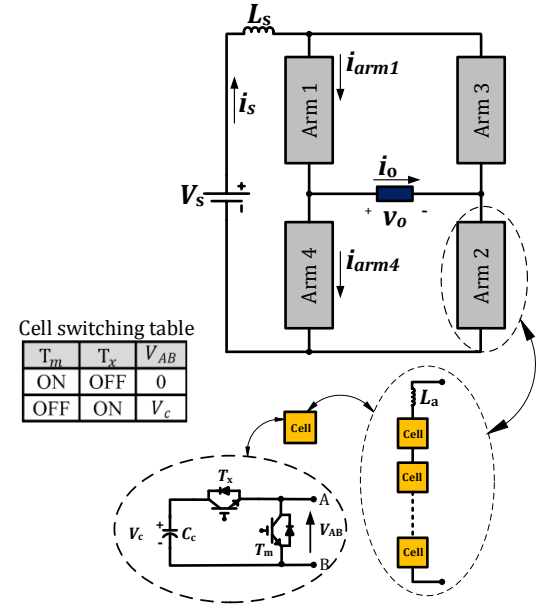
$$v_{mono} = \begin{cases} \pm V_p\,, & 0 \geq t > t_p \\ 0\ (positive\ null), & t_p \geq t > ½(T_s + t_p) \\ 0(negative\ null)\,, & ½(T_s + t_p) \geq t > T_s \end{cases} \quad (2)$$

where $V_p$ is the peak pulse voltage.




(a) (b)

Fig. 1. Half-bridge modular multi-level cell: (a) conventional and (b) modified [11].




Cell switching table

| $T_m$ | $T_x$ | $V_{AB}$ |
|---|---|---|
| ON | OFF | 0 |
| OFF | ON | $V_c$ |

Fig. 2. Proposed converter topology.

## III. Operating Principle

The same methodology is used to generate monopolar and bipolar pulses. The only difference is the omission of one

polarity during pulse generation. Accordingly, the following discussion will consider bipolar pulse generation to illustrate the basic concept. Additionally, the water under electroporation is modelled as a resistive load ($R$) [4].

For proper operation, each arm should be able to withstand the dc-link voltage $V_s$, therefore, each cell-capacitor voltage is $V_c = V_s/N$. Table I shows the circuit configuration and summarises the operating sequence in each period. Generally, during positive pulse generation Arm3 and Arm4 capacitors are inserted to discharge across the load, while Arm1 and Arm2 are inserted during negative pulse generation. The positive and negative null periods in (1) allow charging of the lower arms and the upper arms respectively.

The utilised MMC cells in each arm are all turned ON/OFF simultaneously, therefore, each IGBT switch is subjected only to the cell voltage. Thus, the cell capacitor clamps the IGBT voltage and enforces a symmetrical series voltage distribution. In both charging and discharging, the arm cell capacitors are inserted together forming a total capacitance of $C_c/N$ per arm.

## IV. Analysis and Design of the Proposed Converter

Based on the mentioned operating principle in Table I, provided all the arm switches are turned ON/OFF at the same time, a pictorial charging and discharging sequence of the equivalent arm capacitor is shown in Fig. 4. The instantaneous current flow through the load ($i_o$), the input inductor ($i_s$), Arm1 ($i_{Arm1}$), and Arm4 ($i_{Arm4}$) are shown in Fig. 5.

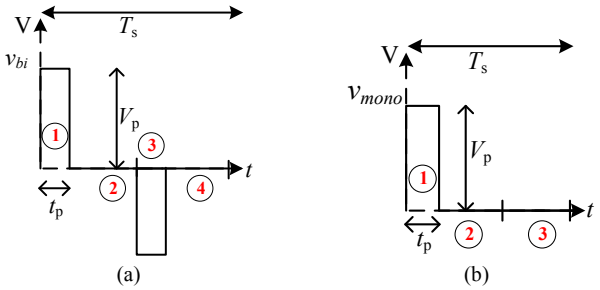



Fig. 3. Generated HV pulses: (a) bipolar rectangular pulse and (b) monopolar rectangular pulse.

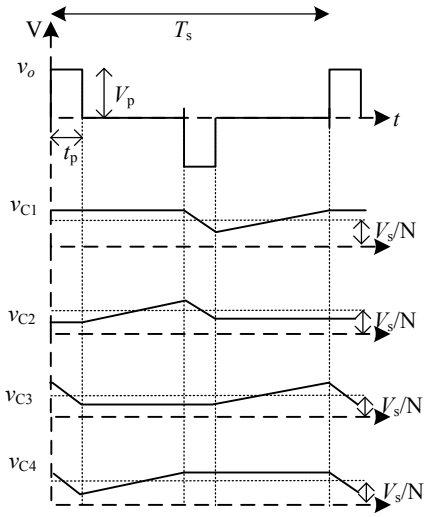
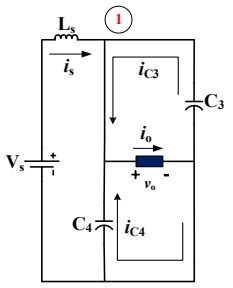
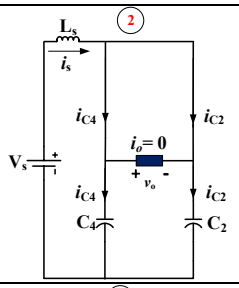
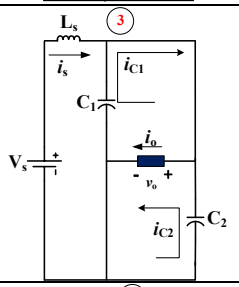
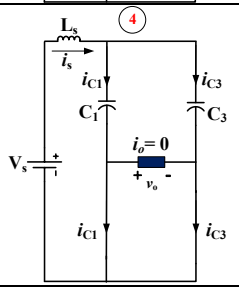



Fig. 4. Cell capacitors charging and discharging sequence for generating a bipolar pulse.

TABLE I
OPERATING PRINCIPLE OF THE PULSE GENERATOR

| | Circuit configuration | Sequence of operation |
|---|---|---|
| **Positive Pulse** |  | • Capacitors of Arm3 and Arm4, $C_3$ and $C_4$, are inserted simultaneously while Arm1 and Arm2 are bypassed such that load voltage is $+V_s$.<br>• Load current is formed by a combination of three energy sources; $C_3$, $C_4$ and $L_s$.<br>• $C_3$ and $C_4$ discharge during this period. |
| **Positive Null** |  | • Capacitors of Arm2 and Arm4, $C_2$ and $C_4$, are inserted, Arm1 and Arm3 are bypassed, and hence, the load voltage is nullified.<br>• The load current is zero.<br>• $C_2$ and $C_4$ are charged through $L_s$ during this period. |
| **Negative Pulse** |  | • Capacitors of Arm1 and Arm2, $C_1$ and $C_2$, inserted while Arm3 and Arm4 are bypassed such that the load voltage is $-V_s$.<br>• The load current is formed by a combination of three energy sources; $C_1$, $C_2$ and $L_s$.<br>• $C_1$ and $C_2$ discharge during this period. |
| **Negative Null** |  | • Capacitors of Arm1 and Arm3, $C_1$ and $C_3$, are inserted, Arm2 and Arm4 are bypassed, and hence, the load voltage is nullified.<br>• The load current is zero.<br>• $C_1$ and $C_3$ are charged through $L_s$ during this period. |

Assuming the voltages and currents notation in Table I are positive, the load current is calculated as

$$i_o = i_{Arm1} - i_{Arm4} = i_{Arm3} - i_{Arm2} \quad (3)$$

while the input current $i_s$ is

$$i_s = i_{Arm1} + i_{Arm3} = i_{Arm2} + i_{Arm4} \quad (4)$$

During positive pulse generation, the load current is supplied from three energy sources namely: Arm3 capacitors discharge through Arm1; Arm4 capacitors discharge through Arm2; and current from the input inductor. In contrast, during a negative pulse duration the load current is formed from three energy sources namely: Arm1 capacitors discharge through Arm3; Arm2 capacitors discharge through Arm4; and the input inductor current. Denoting the average input current as $I_s$, while neglecting semi-conductor losses:

$$V_s I_s = I_o V_o \quad (5)$$

where $I_o$ and $V_o$ are the load rms voltage and current.

Accordingly, $V_o$ is calculated using Fig. 3a as:

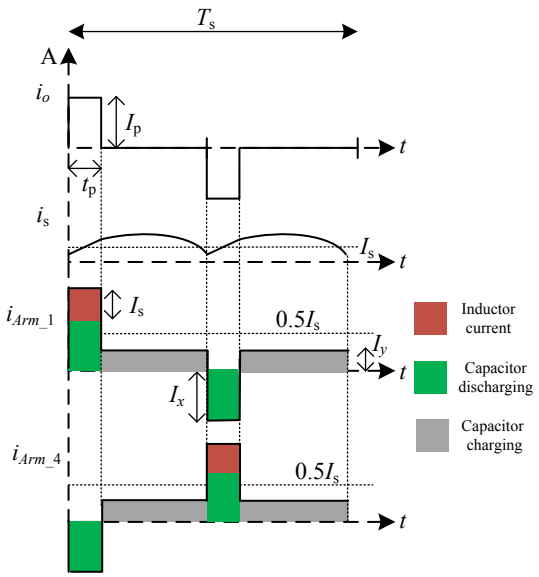



Fig. 5. Current waveforms through the load, the input inductor, Arm1, and Arm4.

$$V_o = \sqrt{\frac{2t_p}{T_s}} V_p \tag{6}$$

Since $I_o = V_p/R$, $I_s$ is

$$I_s = \frac{V_p^2}{V_s}\frac{2\delta}{R} \tag{7}$$

where $\delta = t_p/T_s$ is the pulse duty ratio.

From Fig. 5 and (3), the peak pulse current $I_p$ can be expressed as

$$I_p = I_s + 2I_x \tag{8}$$

where the capacitors discharging and charging currents are denoted by $I_x$ and $I_y$ respectively. Accordingly, the capacitors current-second balance yields

$$I_x t_p = I_y(½T_s - t_p) \tag{9}$$

whereas from Fig. 5 and (3) the capacitor charging current will be

$$I_y = ½I_s \tag{10}$$

Solving (8), (9) and (10) yields

$$I_y = \delta I_p \tag{11}$$

$$I_x = (½ - \delta)I_p \tag{12}$$

$$I_s = 2\delta I_p \tag{13}$$

As the average charge change in any cell capacitor should be zero, examination of either the charging or the discharging period is sufficient. Thus the equivalent arm capacitance $C_{Arm}$ can be defined as

$$C_{Arm} = \frac{I_x \Delta t}{\Delta v} \tag{14}$$

where $\Delta t$ is the discharging current duration and $\Delta v$ is the peak to peak voltage ripple. Substituting for variables from the previous equations gives

$$C_{Arm} = \frac{(½ - \delta)V_p\ \delta T_s}{R(\alpha V_s)} \tag{15}$$

where $\alpha$ is the percent peak to peak voltage ripple of an arm capacitor. Accordingly the cell capacitor can be calculated as:

$$C_c = \frac{(½ - \delta)V_p\ \delta T_s}{R(\alpha V_s)} N \tag{16}$$

If IGBT voltage drop and the internal resistance of $L_s$ are neglected, then $V_p \cong V_s$. Then (16) reduces to

$$C_c = (\frac{(½ - \delta)\ \delta T_s}{\alpha R} N)\beta \tag{17}$$

where, $\beta \geq 1$ is a safety factor to account for the neglected losses.

Resonance between the dc link inductor and arm capacitance during charging of either the two upper arms or the two lower arms should be avoided. Device switching frequency should be well away from the resonance frequency of the equivalent $LC$ circuits to avoid exciting resonance currents. Therefore, based on the calculated equivalent arm capacitance and the repetition time, an estimation of the inductance of $L_s$ is:

$$L_s > \frac{½T_s^2}{(2\pi)^2 C_{Arm}} \tag{18}$$

## V. Simulation Results

The proposed topology is assessed using MATLAB/Simulink simulations, with the parameters given in Table II. The capacitance of the cell capacitors are calculated based on (17) with $\beta = 1$, and (18) is used to estimate the input inductance. The simulations assess the ability of the converter to generate bipolar and monopolar pulses, as well as operation with faulty MMC cells.

The simulation results when generating 10µs bipolar HV pulses at 10 kHz are shown in Fig. 6. The generated pulses are shown in Fig. 6a, the 4 arms capacitor voltages are given in Fig. 6b with a zoomed view of arms 1 and 3. The response of the capacitor voltages followed the expected response shown in Fig. 4. As a result, in this case for $T_s = 100$µs, each arm capacitor is responsible of discharging across the load for 10µs, charging for 40µs while keeping their voltage unchanged for 50µs. Additionally, each capacitor voltage is oscillating around 1000 V, that is $V_s/N$, with less than 5% voltage ripple, as expected.

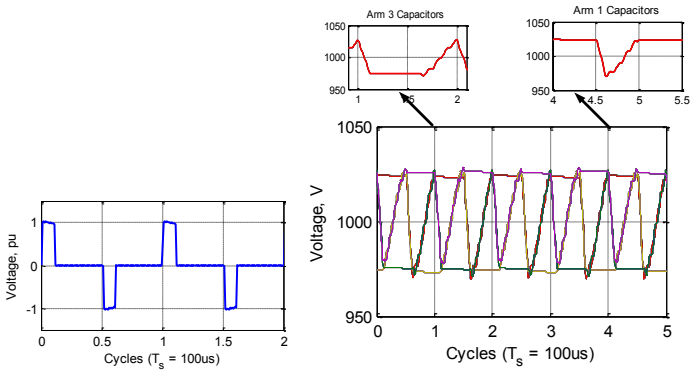
The proposed converter is capable of changing the pulse shape without changing the converter topology, specifically via software. Therefore, using the same specification as in Table II, the proposed converter is programmed to generate 10µs monopolar HV pulses with monopolar positive and negative polarities as well as 4µs bipolar and monopolar HV pulses, all at a 10 kHz repetition rate. The simulation results are shown in Figs. 7a and 7b for 10µs monopolar pulses, Fig. 7c for 4µs bipolar pulses while Fig. 7d shows the 4µs positive monopolar pulses. Moreover, generating rectangular pulses with different characteristics is explored in Fig. 8, where bipolar pulses with different positive and negative durations, 10µs and 4µs respectively, are shown in Fig. 8a. Combined null periods bipolar pulses are shown in Fig. 8b such that the positive pulse duration is 10µs and that of the negative pulse is

4µs. Fig. 8c shows the flexibility of the concept, with bipolar pulses of a variable repetition frequency. A train of 4µs pulses at 10 kHz is combined with a train of 10µs pulses at 5 kHz, with a 1200 µs repetition time.

The small voltage droop in the pulse peak is due to the decrease of the capacitor energy during pulse generation, this droop is reciprocal to the cell capacitor size viz. the larger the capacitor size the smaller the voltage droop and vice versa.

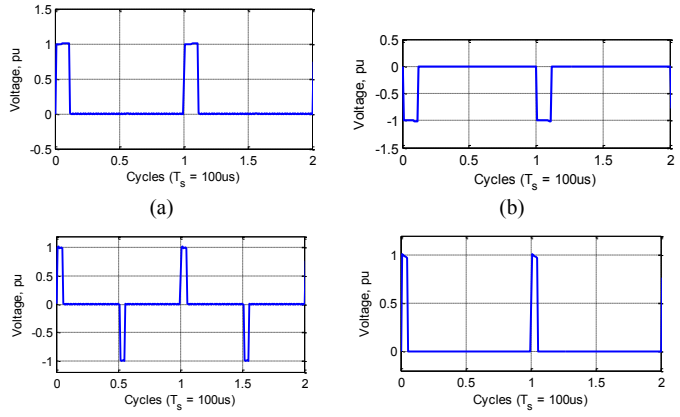
TABLE II
SPECIFICATION FOR SIMULATION AND EXPERIMENTATION

| Parameter | | Simulation | Experimentation |
|---|---|---|---|
| DC input voltage | ($V_s$) | 10 kV | 250 V |
| Input inductance | ($L_s$) | 1.5 mH | 0.5 mH |
| Number of cells/arm | ($N$) | 10 | 3 |
| Repetition time | ($T_s$) | 100 µs | 100 µs |
| Arm inductance | ($L_a$) | 15 µH | 10 µH |
| Load resistance | ($R$) | 1 kΩ | 500 Ω |
| Cell capacitance | ($C_c$) | 1 µF | 1 µF |
| Pulse duration | ($t_p$) | 10 µs and 4 µs | 10 µs and 4 µs |
| Percent voltage ripple | ($\alpha$) | 0.05 | 0.05 |
| Safety factor | ($\beta$) | 1 | 1 |




(a) (b)

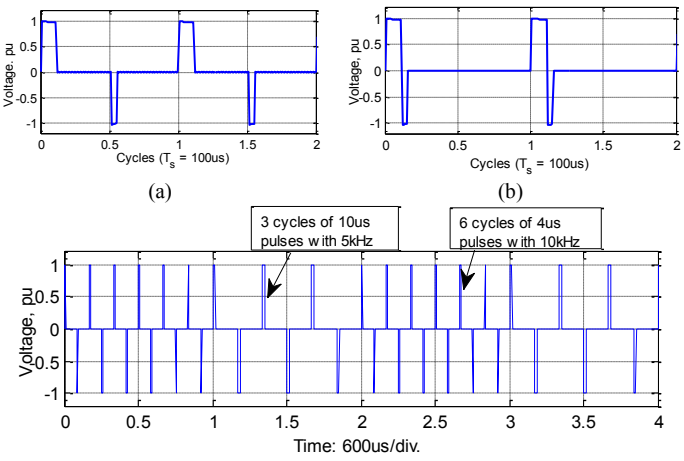
Fig. 6. Simulation results for bipolar HV pulses, $t_p = 10$µs: (a) output pulse, with base voltage 10 kV and (b) 4 arms capacitor voltages with zoomed view on Arms 1 and 3.




(a) (b) (c) (d)

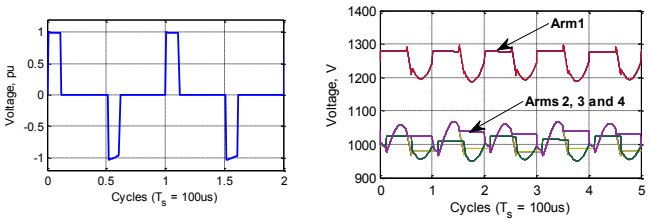
Fig. 7. Simulation results for output HV pulses with base voltage 10kV: (a) 10µs positive monopolar, (b) 10µs negative monopolar, (c) 4µs bipolar, and (d) 4µs positive monopolar.

It should be noted that the ability of the converter to generate the a wide range of rectangular pulses is solely depend on the speed of selected controller in executing the control software instructions, such that the total software execution time is lesser than the required pulse repetition time. Moreover, for high repetition rates and/or short pulse duartions the utilisation of fast semi-conductor switches is mandatory.




(a) (b) (c)

Fig. 8. Simulation results for output HV pulses with base voltage 10kV: (a) Different duration pulses, (b) Combined different duration pulses, (c) Variable pulse duration and repetition frequency.




(a) (b)

Fig. 9. Simulation results for output HV pulses when two faulty cells in Arm1, $t_p = 10$µs: (a) output pulse, base voltage 10kV and (b) 4 arms capacitor voltages.

The cell capacitors are responsible for clamping the voltage across the module switches to $V_s/N$ without any voltage measurements or control. Thus, if one or more cells are subject to failure, the excess voltage will be shared equally between the healthy cell-capacitors. Hence, the new cell voltage $V_{cf}$ under failure is

$$V_{cf} = \frac{V_s}{N - N_f} \tag{19}$$

where $N_f$ is the number of the faulty cells. The simulation results in Fig. 9 address a cell failure case, where two cells of Arm1 malfunction while the converter still able to generate the desired bipolar pulses, as shown in Fig. 9a. Nevertheless, in this case the cell-voltage of each healthy cell in Arm1 will be 1250V increased from its normal 1000V. Therefore, the

voltage stress is distributed between the healthy cells to alleviate the malfunction of the two cells, as shown in Fig. 9b.

## VI. Experimental Results

The test equipment to assess the proposed converter topology uses ultra-fast IGBT switches (STGW30NC60WD) while the control algorithm is implemented on Texas Instruments eZDSP F28335. The experimental parameters are given in Table II, and the scaled experimental rig is shown in Fig. 10. Fig. 11 shows the experimental results for bipolar voltage pulses with $t_p = 10$ µs.

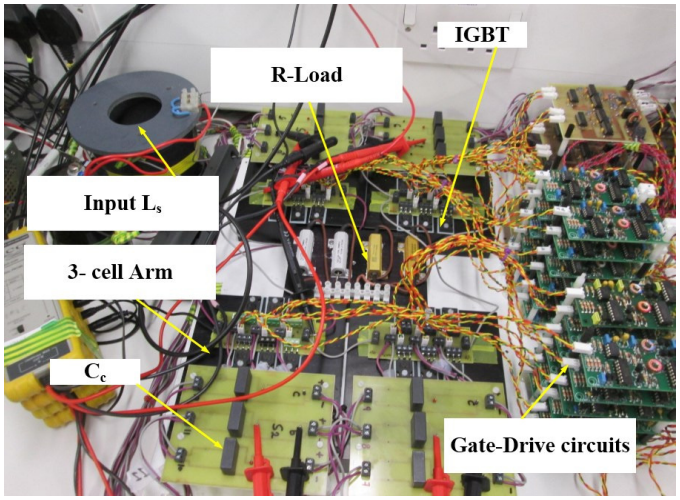



Fig. 10. The scaled experimental test rig.

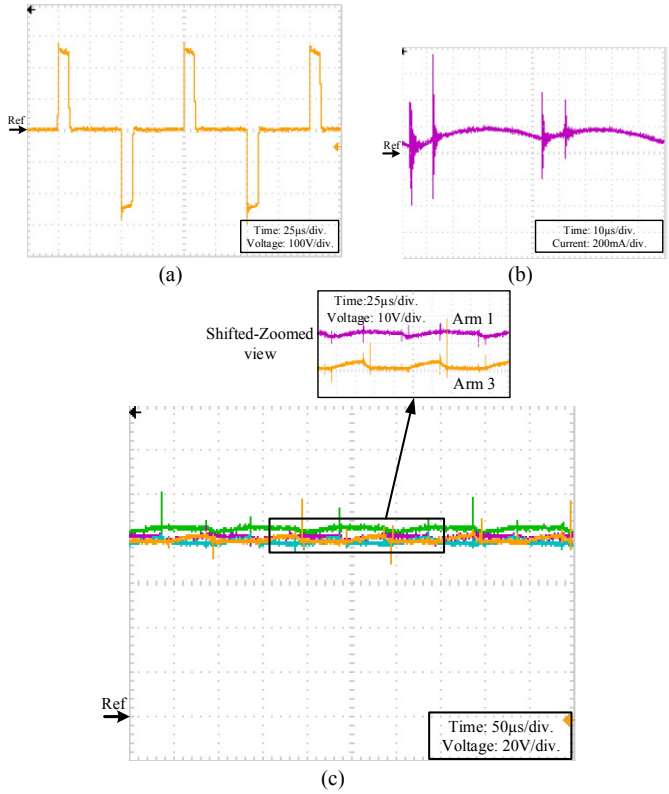



Fig. 11. Experimental results, $t_p = 10$ µs: (a) output bipolar voltage pulses, (b) input current, and (c) a cell capacitor voltage in each of the 4 arms.

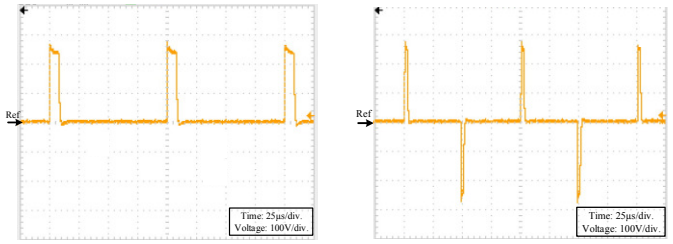



Fig. 12. Experimental results for the output voltage pulses: (a) monopolar at $t_p = 10$ µs and (b) bipolar at $t_p = 4$ µs.

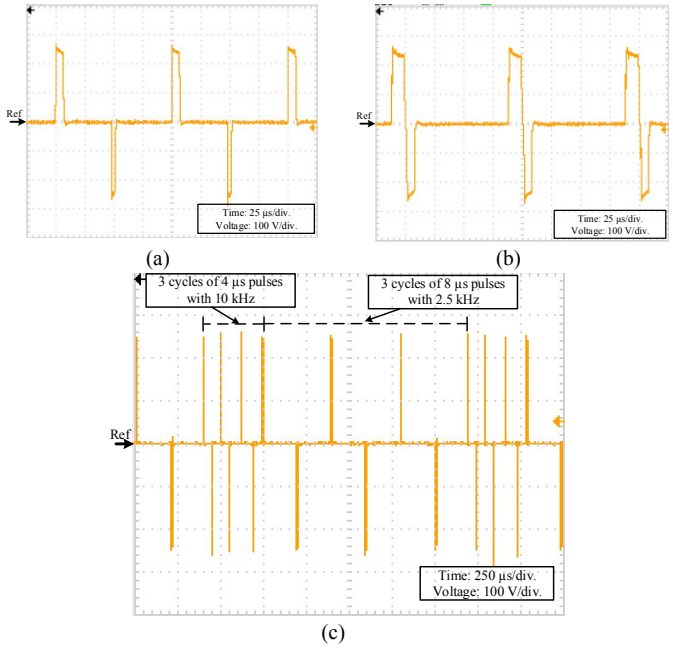



Fig. 13. Experimental results: (a) Different duration pulses, (b) Combined different duration pulses, (c) Variable pulse duration and repetition frequency.

The output voltage pulses and the input current through $L_s$ are shown in Figs. 11a and 11b respectively. The voltages across one capacitor in each of the 4 arms are given in Fig. 11c with a shifted-zoomed view of Arm1 and Arm3 capacitor voltages. Since the peak of the output pulse is 250V, each capacitor voltage should be around 83.3V, as shown in Fig.11c.

A $t_p = 10$ µs monopolar voltage pulse is shown in Fig. 12a while bipolar voltage pulses with $t_p = 4$ µs are depicted at Fig. 12b.

Generating customised rectangular pulse characteristics is explored in Fig. 13. Fig. 13a shows bipolar pulses with positive and negative pulse durations of 8µs and 4µs respectively. Combined null periods with positive and negative pulse durations of 8µs and 4µs, respectively, is shown in Fig. 13b. In Fig. 13c, a train of 4µs pulses at 10 kHz is combined with a train of 8µs pulses at 2.5 kHz, for a 1500µs repetition time.

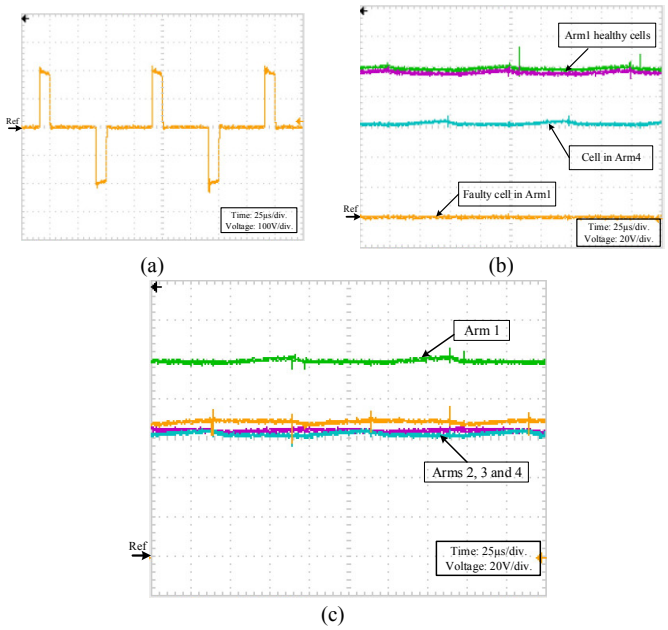



Fig. 14. Experimental results, when a cell in Arm1 is faulty: (a) output bipolar voltage pulses with $t_p = 10$ µs, (b) Arm1 cell capacitor voltages along with a cell in Arm4, and (c) a cell capacitor voltage in each of the 4 arms.

Finally, in order to verify the performance of the proposed topology during an MMC cell malfunction, one of the cells in Arm1 is deliberately short circuited while generating a bipolar pulse of $t_p = 10$µs. Again the parameters in Table II are used with an input voltage of $V_s = 200$V. The output voltage pulses in this case are shown in Fig. 14a. The faulty arm cell voltages are shown in Fig.14b along with a cell voltage in Arm4. The healthy cell voltages in Arm1 increase to 100V from 66.7V. The voltage across one capacitor in each arm for this case is shown in Fig. 14c.

## VII. Conclusion

This paper presented a new HV pulse generator topology based on half-bridge MMC cells. The rectangular pulse characteristics are controlled via software control without any physical change to the power topology. The converter can generate both bipolar and monopolar HV pulses with micro-second pulse durations at a high frequency rate with different characteristics. Hence, the proposed topology provides flexibility by software control, along with hardware modularity, scalability, and redundancy. The adopted charging and discharging process of the MMC cell capacitors assure voltage balance without any voltage measurements or complex control, consequently, continuous operation during cell malfunction is gained, where the voltage stress across each module is clamped to the capacitor voltage. Moreover, the cell capacitances are small, thereby reducing the converter's footprint. The presented simulations and experimental results confirm the feasibility and the features of the proposed topology for water disinfection applications.

## Acknowledgment

The statements made herein are solely the responsibility of the authors.

## References

[1] K. H. Schoenbach, F. E. Peterkin, R. W. Alden, and S. J. Beebe, "The effect of pulsed electric fields on biological cells: experiments and applications," *IEEE Trans. Plasma Sci.*, vol. 25, no. 2, pp. 284-292, 1997.

[2] J. Raso and V. Heinz, *Pulsed electric fields technology for the food industry*: *fundamentals and applications*, London, Springer, 2006.

[3] H. Bluhm, *Pulsed power systems: principles and applications*, Berlin, Springer, 2006.

[4] K. H. Schoenbach, R. P. Joshi, R. H. Stark, F. C. Dobbs, and S. J. Beebe, "Bacterial decontamination of liquids with pulsed electric fields," *IEEE Trans. Dielect. Elect. Insulation*, vol. 7, no. 5, pp. 637-645, 2000.

[5] A. Abou-Ghazala, S. Katsuki, K. H. Schoenbach, F. C. Dobbs, and K. R. Moreira, "Bacterial decontamination of water by means of pulsed-corona discharges," *IEEE Trans. Plasma Sci.*, vol. 30, no. 4, pp. 1449-1453, 2002.

[6] M. Reberšek and D. Miklavčič, "Advantages and disadvantages of different concepts of electroporation pulse generation," *Automatika–Journal for Control, Measurement, Electronics, Computing and Communications*, vol. 52, no. 1, 2011.

[7] E. Veilleux, B. T. Ooi, and P. W. Lehn, "Marx dc-dc converter for high-power application," *Power Electronics, IET*, vol. 6, no. 9, pp. 1733-1741, 2013.

[8] M. Rezanejad, A. Sheikholeslami, and J. Adabi, "Modular switched capacitor voltage multiplier topology for pulsed power supply," *IEEE Trans. Dielect. Elect. Insulation*, vol. 21, no. 2, pp. 635-643, Apr. 2014.

[9] P. Davari, F. Zare, A. Ghosh, and H. Akiyama, "High-voltage modular power supply using parallel and series configurations of flyback converter for pulsed power applications," *IEEE Trans. Plasma Sci.*, vol. 40, no. 10, pp. 2578-2587, Oct. 2012.

[10] A. A. Elserougi, A. M. Massoud, and S. Ahmed, "A Modular High-Voltage Pulse-Generator with Sequential Charging for Water Treatment Applications," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1-1, 2016.

[11] L. Lamy Rocha, J. F. Silva, and L. M. Redondo, "Multilevel high-voltage pulse generation based on a new modular solid-state switch," *IEEE Trans. Plasma Sci.*, vol. 42, no. 10, pp. 2956-2961, Oct. 2014.

[12] L. L. Rocha, J. F. Silva, and L. M. Redondo, "Seven-Level Unipolar/Bipolar Pulsed Power Generator," *IEEE Trans. Plasma Sci.*, vol. PP, no. 99, pp. 1-5, 2016.

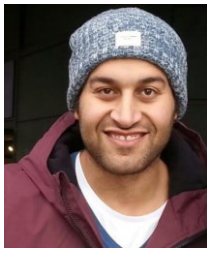
[13] A. Elserougi, S. Ahmed, and A. Massoud, "High voltage pulse generator based on DC-to-DC boost converter with capacitor-diode voltage multipliers for bacterial decontamination," IECON 2015, pp. 322-326.

[14] S. Zabihi, F. Zare, G. Ledwich, A. Ghosh, and H. Akiyama, "A novel high-voltage pulsed-power supply based on low-voltage switch-capacitor units," *IEEE Trans. Plasma Sci.*, vol. 38, no. 10, pp. 2877-2887, Oct. 2010.

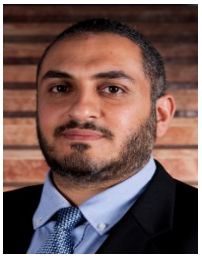
[15] L. M. Redondo and J. F. Silva, "Flyback versus forward switching power supply topologies for unipolar pulsed-power applications," *IEEE Trans. Plasma Sci.*, vol. 37, no. 1, pp. 171-178, Jan. 2009.

[16] S. Zabihi, F. Zare, G. Ledwich, A. Ghosh, and H. Akiyama, "A new pulsed power supply topology based on positive buck-boost converters concept," *IEEE Trans. Dielect. Elect. Insulation*, vol. 17, no. 6, pp. 1901-1911, Dec. 2010.

**Mohamed A. Elgenedy** received the B.Sc. (with first-class honors) and M.Sc. degrees in Electrical Engineering from Alexandria University, Egypt in 2007 and 2010 respectively. Currently he is working toward the Ph.D. degree at the University of Strathclyde, Glasgow, U.K. He is also an assistant lecturer with the Electrical Engineering Department, Faculty of Engineering, Alexandria University. In 2012, he was with Spiretronic LLC, Houston, TX, USA, as a Research Engineer. From 2013 to 2014, he was a Research Associate at Texas A&M University at Qatar. His research interests include high power electronics, electric machine drives, energy conversion, and renewable energy.



**Ahmed Darwish** received the B.Sc. and M.Sc. degrees in electrical engineering from the Faculty of Engineering, Alexandria University, Alexandria, Egypt, in 2008 and 2012, respectively, and the Ph.D. degree in electric engineering from the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, U.K., in 2015. From 2009 to 2012, he was a Research Assistant at Texas A&M University at Qatar, Doha, Qatar. He is currently a Research Associate with PEDEC Group at the University of Strathclyde. His research interests include dc–dc converters, multilevel converters, electric machines, digital control of power electronic systems, energy conversion, renewable energy, and power quality.



**Shehab Ahmed** (SM'12) was born in Kuwait City, Kuwait in July 1976. He received the B.Sc. degree in Electrical Engineering from Alexandria University, Alexandria, Egypt, in 1999; the M.Sc. and Ph.D. degrees from the Department of Electrical & Computer Engineering, Texas A&M University, College Station, TX in 2000 and 2007, respectively. From 2001 to 2007, he was with Schlumberger Technology Corporation working on downhole mechatronic systems. He is currently an Assoicate Professor with Texas A&M University at Qatar, Doha, Qatar. His research interests include mechatronics, solid-state power conversion, electric machines, and drives.

**Barry W. Williams** received the M.Eng.Sc. degree from the University of Adelaide, Adelaide, Australia, in 1978, and the Ph.D. degree from Cambridge University, Cambridge, U.K., in 1980. After seven years as a Lecturer at Imperial College, University of London, London, U.K., he was appointed to a Chair of Electrical Engineering at Heriot-Watt University, Edinburgh, U.K, in 1986. He is currently a Professor at the University of Strathclyde, Glasgow, U.K. His teaching covers power electronics (in which he has a free internet text) and drive systems. His research activities include power semiconductor modeling and protection, converter topologies, soft switching techniques, and application of ASICs and microprocessors to industrial electronics.