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A Low-Loss Hybrid Bypass for DC Fault Protection of Modular Multilevel Converters

I. A. Gowaid

Abstract— Without additional circuitry, the half-bridge modular multilevel converter (HB-MMC) is endangered under dc side faults. Typically, a bypass thyristor is augmented to each HB cell to take up fault current until ac circuit breakers interrupt the dc fault. This paper proposes a dc fault protection concept for HB-MMC stations that requires insignificant extra silicon area relative to the thyristor bypass concept. Herein, bypass thyristors of typical HB cells are rearranged such that an independent modular shadow rectifier bridge (SRB) is formed. A low-loss switch assembly is utilized to immediately isolate the MMC following fault detection and the SRB suppresses the fault current by injecting a reverse dc voltage. Among several advantages, the proposed arrangement incurs insignificant losses in steady state, and in some arrangements the MMC is capable of operating in STATCOM mode briefly after fault inception to support ac grid voltage. The proposed concept may be suitable for clearing temporary faults on overhead HVDC lines. Several structural variations will be viewed and discussed. Applicability for two-level VSC will be addressed. The concept is validated by detailed numerical simulations of a ±200kV HB-MMC station under dc fault.

Index Terms-- Modular multilevel converter, dc fault, and, HVDC.

I. Introduction

VOLTAGE source converters (VSC) are favored to conventional line-commutated converters (LCC) for multi-terminal high voltage dc (HVdc) connections. At the envisaged high voltage and power levels of such networks, the modular multilevel converter (MMC) concept has distinct advantages to other commercially available VSC concepts (e.g. two-level VSCs) for several technical and economic considerations [1-2]. However, the basic MMC structure – built of half-bridge (HB) cells – is endangered should the dc voltage dip at faulty conditions; particularly under pole-to-pole dc faults [3]. Without additional circuitry, semiconductor devices of the HB-MMC may be damaged by the uncontrollable high current rushing through freewheeling diodes into the dc side.

Several solutions have been proposed to address this problem. These can be classified into three generic concepts:

1. Diverting fault current into a bypass path until the fault is externally interrupted; typically by an ac side breaker,
2. Injecting a sufficient reverse dc voltage in the dc circuit to quickly suppress dc current, or;
3. Triggering a controlled ac side fault so as to inhibit fault current infeed from the ac circuit.

The bypass concept is typically realized using bypass thyristors triggered to share the fault current with affected freewheeling diodes until the ac side breaker trips the circuit, typically in 2-3 ac cycles [4]. Although in industrial use (e.g. Trans Bay Cable project), this solution is not optimal particularly for overhead dc lines. For instance, reclosing (re-energization) capability is limited and additional dc chokes (or sufficient arm reactors and ac side impedance) are needed to limit fault current slope to avoid overheating of bypass thyristors and vulnerable diodes.

Injecting reverse dc voltage in the dc circuit can be administered using a dc circuit breaker (DCCB) connected at the VSC dc side [5-6]. Regardless of the technology used to build said DCCB, the latter will need to dissipate the energy stored in the dc circuit, which can lead to excessive heating and restrict reclosing. Also, the VSC station must handle the fault current until the full DCCB operation cycle elapses. Thus, bypasses and large dc chokes may still be required.

Alternatively, sufficient reverse dc voltage can be produced internally within the MMC station when so-called blocking cells are utilized; such as the double clamp cell [3], full-bridge cell [7], semi-full bridge cell [8], and the blocking half-bridge cell [9]. The same can also be achieved when the alternate arm converter is employed [10].

In said protection concept, fault interruption time is primarily limited by detection and protection coordination delays. The converter absorbs dc circuit energy and quickly suppresses the dc current. The expense is extra complexity and a significant rise of silicon area and steady state conduction losses.

The third concept creates a controlled ac fault at the ac terminals of the VSC station to stop current infeed into the dc circuit under fault. For that, two anti-parallel thyristors are connected across the terminals of each HB cell and are turned on upon dc fault detection to trigger an artificial three-phase ac fault at the VSC terminals [11]. This concept employs double the number of thyristors utilized in the bypass concept. The authors of [12] proposed the use of anti-parallel thyristor valves in a separate ac side bridge rather than an anti-parallel thyristor pair in each HB cell. This implies an extra non-modular bridge structure is built in the valve hall with dedicated snubbing and protective circuitry.

This paper proposes a novel hybrid bypass arrangement for dc fault ride-through of HB-MMC stations. This is in essence similar to the dc fault interruption concept used in LCC HVdc systems. It merges the 'bypass' and 'reverse dc voltage injection' protection concepts to achieve relatively fast dc fault interruption with insignificant rise in station steady state

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losses or silicon area beyond the conventional bypass protection concept. The proposed protection concept shows potential for handling temporary dc faults on overhead HVDC lines. Utilization for cable HVDC links and multi-terminal networks will be discussed in light of possible configurations of the proposed concept.

II. The Proposed Hybrid Bypass Concept

Thyristors are robust devices of proven reliability and high pulse current capability. The commercial practice of connecting a thyristor across the terminals of each HB cell (e.g. by Siemens and Alstom) only partially bypasses the vulnerable freewheeling diode and rips said thyristor off the phase control capability. This capability can be recovered when the HB cell is reconfigured such that the bypass thyristor terminals are separated from cell terminals. Each HB cell power module becomes of four terminals and the thyristor voltage can be optionally clamped to the cell voltage using diodes (refer to section VI). Hence, thyristors per phase arm can independently form a controlled rectifier valve. The HB-MMC station evolves to a primary converter bridge (the HB-MMC) and a shadow rectifier bridge (SRB) which is out of the conduction path in steady state.

The extra degree of freedom provided by the SRB permits control of the VSC station dc bus voltage in faulty conditions (e.g. under a dc fault) when the dc rails of the MMC are isolated from the dc circuit and the SRB is operated independently. Isolation of the MMC from the dc circuit may be administered by a switch assembly connected, in the simplest form, in each dc pole. For effective and economic protection, the requirements set for said switch assembly are fast action and low losses. To meet these requirements, a hybrid switch comprising a semiconductor-based unidirectional low-voltage commutation switch (LVCS) and a fast mechanical switch (FMS) may be utilized to form a low-loss path. A similar low-loss path is utilized in [5].

For expedience, modular station designs will be presented in section VI after the basic hybrid bypass concept is developed and analyzed along sections III, IV, and V utilizing the functionally-equivalent non-modular hybrid bypass arrangement of Fig. 1.

III. DC Fault Interruption Sequence

DC fault current interruption sequence according to the proposed hybrid bypass concept will be explained with the aid of the symmetric monopolar arrangement of Fig. 1 and the current profiles depicted in Fig. 2. When a dc fault is detected ($t = t_o$) and a decision is made to interrupt the fault current the following actions are taken:

a. t_1: MMC IGBTs are blocked and all thyristors of the SRB are triggered and remain in operation at the minimum possible firing angle (ideally $\alpha \approx 0^o$).
b. t_1': each LVCS turns off.
c. t_2: trip signal is sent to each FMS.
d. t_3: each FMS is in open position. Immediately or after a delay, the controller inhibits SRB firing pulses, or firing angle is retarded to $\alpha > 90°$.
e. t_4: fault current hits zero and SRB firing is inhibited (if not inhibited at $t = t_3$), and reclosing timer is started.

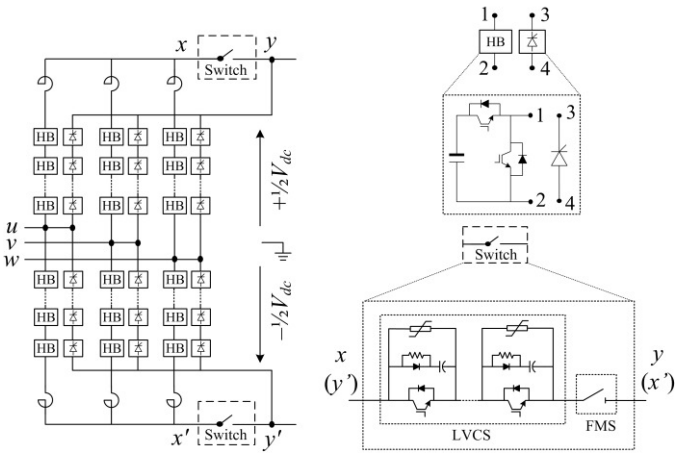

Fig. 1 The basic non-modular structure of the proposed hybrid bypass dc protection concept (a symmetrical monopole example).

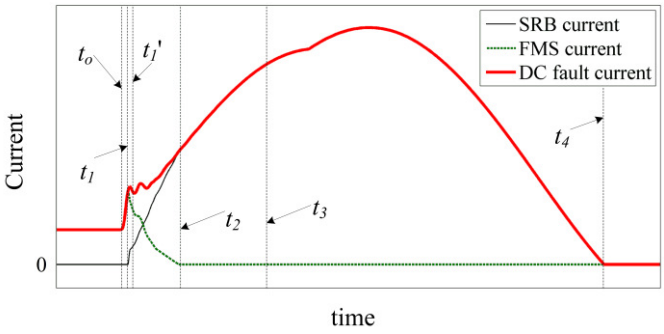

Fig. 2 DC Fault current through the MMC and SRB using the hybrid bypass protection concept (SRB firing pulses inhibited at $t = t_3$).

In sequence a – e, the interval $t_o - t_1$ is the time taken by fault detection and protection discrimination algorithms to make decisions. A short delay $t_1 - t_1'$ is inserted before opening each LVCS to make sure the SRB is triggered and shares fault current with the MMC.

Once fully triggered, the SRB produces nearly the same dc voltage across points y and *y'* as the blocked MMC produces across points x and *x'*; both converters being fed from the same ac source and the SRB resembling a diode rectifier being operated at $\alpha \approx 0^o$. This way, the voltage to be blocked by each hybrid switch during the interval $t_1' - t_3$ is minimal. This implies that each LVCS can be formed of one IGBT or a few series-connected IGBTs (Fig. 1) with an aggregate on-state voltage drop of a few volts. Such a low voltage drop is essential to achieve the low-loss property of each hybrid switch where full dc current flows in steady state.

In sequence a – e, a short delay $t_1' - t_2$ is inserted (Fig. 2). This delay is required when the MMC arm reactors are connected to respective dc poles (as in Fig. 1) in order to dissipate the energy stored in the MMC arm reactors before a tripping signal is sent to FMS actuators such that each FMS is opened at zero current.

Once the FMS is in open position with full dielectric strength, the SRB firing pulses are inhibited or retarded to $\alpha > 90°$ which allows the SRB inject a reverse dc voltage across points y and *y'* to bring the fault current to zero by exporting the fault energy from the dc side to the ac side. This

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is similar to so called 'force retard' operation of LCC HVDC converters under dc fault [13].

The FMS opening time is of primary influence on the interruption time span ($t_o - t_4$) of sequence a – e. A faster FMS leads to quicker fault current interruption and less heating of SRB thyristors. It is preferable that the FMS contacts open at zero current to avoid arcing and, in consequence, to realize the FMS as a disconnector switch. Opening times in the range of a few milliseconds are typical in such a case [5]. Reference [14] reports a disconnector design achieving 2ms opening time in a laboratory test at 320kV nominal insulation level using SF_6 as insulation medium. Subject to dc circuit voltage, series connection of disconnectors may be needed. In this case, switching the FMS at low volt will spare the need for grading capacitors to establish uniform dynamic voltage sharing [5].

Once each hybrid switch is in open position and the MMC is fully isolated from the dc circuit, the MMC can resume operation immediately as a static synchronous compensator (STATCOM) to support ac grid voltage. Since the dc fault interruption sequence does not require ac side breakers to trip, the MMC station may remain in STATCOM mode until, for instance, the ac bus voltage amplitude returns to a predefined band.

Independent operation of the SRB enables controlled reclosing attempts in the conventional manner exercised in an LCC HVDC link to quickly re-energize the dc line after temporary faults [13]. As the MMC is fully bypassed almost instantly, freewheeling diodes do not share the fault current with the SRB (unlike the case of conventional thyristor bypass). Hence, HB cells need not be dimensioned for fault current handling.

IV. Design and Characteristics

A. LVCS Blocking Voltage

When each LVCS turns off, MMC residual energy must be dissipated in a controlled manner when arm reactors are located as in Fig. 1 to avoid overvoltage transients. For that, each LVCS is shunted by an arrester bank to dissipate said residual energy (see Fig. 1). The arrester bank aggregate knee voltage V_{arr} should be carefully selected so as to minimize the MMC residual energy dissipation time t_d. Clearly, reduction of t_d would be traded for a higher value of V_{arr} and, hence, higher LVCS blocking voltage. This in turn leads to higher on-state losses in steady-state. For that, arm reactance may be minimized by shifting the dc fault current limiting duties to transformer impedance and/or dc chokes.

For the 700MVA ±200kV symmetric monopole system tested in section V (based on Fig. 1 arrangement), the MMC energy dissipation time $t_d \approx 2$ms (i.e. $t_2 \approx t_1' + 2$ms) when $V_{arr} = 15$kV per dc pole. The interval t_d drops to roughly 1ms with $V_{arr} = 20$kV per dc pole.

The correlation between V_{arr} and t_d can be further investigated with reference to Fig. 3 which depicts the equivalent circuit of the MMC and the hybrid bypass arrangement during the interval t_1' – t_2. When the MMC IGBTs are blocked at t_1 and before the LVCS is turned off, the MMC becomes effectively an uncontrolled rectifier. At LVCS turn-off ($t = t_1'$), the current i_r flowing in each MMC arm encounters a reverse voltage V_{rev}. The equivalent circuit seen by i_r and, consequently, the value of V_{rev} is subject to i_r direction at t_1. This is exemplified by the upper arm of phase v in Fig. 3 (loop a-b-x-y-c-d marked in bold red) and shown by (1) for $t_1' \le t \le t_2$, where V_C is the sum of cell voltages in the arm. It is worth noting that in the case of $i_r > 0$, $V_{rev} = V_C$ for $t_1 < t < t_1'$. Applying Kirchhoff's voltage law in the loop a-b-x-y-c-d for $t_1' \le t \le t_2$ yields (2).

$$V_{rev} = \begin{cases} V_{arr} & i_r < 0 \\ V_C - V_{arr} & i_r > 0 \end{cases} \tag{1}$$

$$V_{rev} - V_{th} + L_c \frac{di_r}{dt} + i_r \left(R_d + R_c \right) = 0 \tag{2}$$

In (2), L_c, R_d, and R_c are the arm inductance, MMC diode valve aggregate on-state resistance, and resistance of arm inductance, respectively. V_{th} is the voltage (in forward polarity) across the respective thyristor valve during interval t_1' – t_2. Solving (2), i_r can be expressed as in (3) for $t_1' \le t \le t_2$.

$$i_r(t) = i_{ro} e^{-\left(\frac{1}{L_c}(R_d + R_c)\right)t} + \frac{V_{rev} - V_{th}}{R_d + R_c} \left(e^{-\left(\frac{1}{L_c}(R_d + R_c)\right)t} - 1 \right) \tag{3}$$

In (3), i_{ro} is the unsigned value of arm current at t_1'. It can be seen from (1) – (3) that arm currents flowing in the reverse direction of MMC diode valves (i.e. when $i_r > 0$ as in Fig. 3b) encounter significantly larger reverse voltage. Subsequently, such arm currents diminish quickly relative to arm currents flowing in the forward direction of MMC diode valves (i.e. when $i_r < 0$ as in Fig. 3a). As far as the proposed hybrid bypass concept is concerned, the decay of arm currents where $i_r < 0$ at the instant t_1' is of most importance since it determines the span of interval t_1' – t_2 and, subsequently, affects dc fault current interruption time. Validation of the dissipation time t_d obtained by (1) – (3) will be highlighted in section V in relation to simulation results of the tested case study.

An alternative protection sequence that will not be treated in this paper due to space limits is to trip the FMS before the MMC residual energy is fully dissipated in LVCS arrester banks for faster fault current suppression (i.e. $t_2 < t_d$). The FMS and the LVCS could rather be tripped simultaneously at t_1'. An arc strikes across the FMS contacts and quenches once MMC residual energy is dissipated. SRB firing signals are to be inhibited or retarded only after a brief delay allowing for complete deionization of the FMS dielectric.

RCD snubbers are needed across LVCS IGBTs for voltage sharing (see Fig. 1). Said snubber arrangement allows a controlled capacitor discharge at LVCS turn-on, as well as short snubber charging interval at LVDC turn-off.

Once each LVCS turns off, respective snubber capacitors charge to V_{arr}. Thus, the average voltage difference between points x and *x'* in Fig. 1 during the time interval t_1' – t_3 can be approximated by (4) where V_{l-l}^{rms} is the RMS value of phase-to-phase ac bus voltage.

$$V_{xx'} \approx 2V_{arr} + \frac{3\sqrt{2}}{\pi} V_{l-l}^{rms} \cos\alpha \tag{4}$$

The second term in the right-hand-side of (4) represents the voltage developed by the SRB between points y and *y'*. When SRB firing angle is kept at $\alpha \approx 0°$, (4) illustrates that the uncontrolled rectifier formed by the blocked MMC becomes

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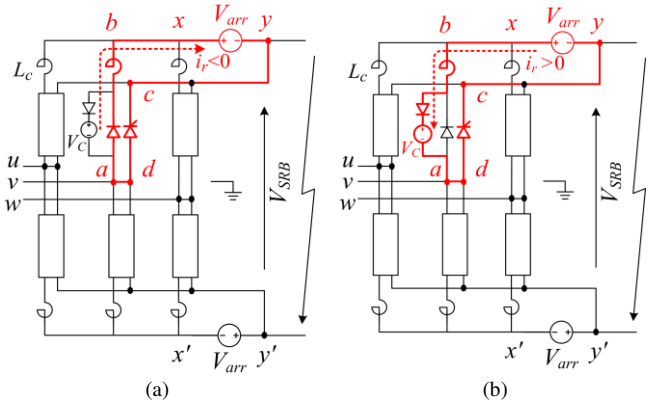

Fig. 3 Equivalent circuit of the MMC and the proposed hybrid bypass arrangement augmented thereto during the interval $t_1' - t_2$ of the associated protective sequence a – e for (a) $i_r < 0$ at $t = t_1'$, and (b) $i_r > 0$ at $t = t_1'$.

reverse biased at t_1' as soon as each LVCS injects V_{arr} with an opposing polarity to dc current flow. The reverse bias of the MMC rectifier ensures that the dc current is fully commutated to the SRB prior to tripping each FMS.

B. LVCS Reliability and Power Loss

A robust, redundant, and reliable design of the LVCS is necessary given the steady-state continuous flow of dc current through it [15]. Also, the maximum on-state loss of each LVCS determines the required cooling load. The on-state loss of an IGBT or a diode can be calculated using (5), where $i_d(t)$, V_o, and R_{on} are device instantaneous current, threshold voltage drop, and on-state resistance, respectively.

$$P_{loss} = \frac{1}{2\pi}\int_0^{2\pi}\left(V_o + R_{on} i_d(t)\right) i_d(t)\,dt \tag{5}$$

Equation (5) can be developed into (6) and (7) for the IGBT and the anti-parallel diode, respectively. In (6) and (7), superscripts refer to device type and subscripts C, E, and D, refer to collector, emitter, and diode, respectively.

$$P_{loss}^{IGBT} = V_{CEo} I_{C,av} + R_{CE} I_{C,rms}^2 \tag{6}$$

$$P_{loss}^{d} = V_{Do} I_{D,av} + R_D I_{D,rms}^2 \tag{7}$$

As a design example, when the 700MVA ±200kV tested system of section V utilizes a 15kV LVCS per dc pole, a series string of seven 4.5kV IGBT modules is needed to block the 15kV at nearly 2.1 kV per device for redundancy. When 4.5kV 2kA IGBT modules are used (e.g. 5SNA-2000K450300 [16]), two parallel IGBT strings are needed in each LVCS to take up the 1.5kA rated dc current with a safe margin. Utilizing said device of [16], maximum steady state power losses of each LVCS – calculated using (6) and (7) based on datasheet parameters – are roughly 18kW (a maximum of 1.3kW per module). Said LVCS losses amount to less than 1% of total station power losses assuming the MMC power conversion efficiency is 99%.

In conclusion, steady state losses incurred by the proposed hybrid bypass arrangement constitute a trivial fraction of the station power losses. This holds even when V_{arr} is doubled to reduce t_d. It follows that an insignificant cooling load is required from station's cooling plant.

C. Shadow Rectifier Bridge Design

The ac voltage across each SRB valve is equal to the MMC arm voltage, which is ½(1 ± m)V_{dc}; m being the modulation index. This implies the SRB valves are continually reverse biased in steady state. Uniform reverse and forward voltage sharing in each SRB valve can be achieved using passive snubber circuits (primarily RC snubbers) or, in a modular design, by clamping to HB cells voltages. In each SRB valve, dispersed (per HB cell) or lumped reactor is required to limit di/dt particularly at valve turn-on. Said snubber reactors along with RC snubbers act to limit the commutation overshoot of thyristors at valve turn off as well as the magnitude and dv/dt of any transient overvoltage applied to the valve in off state (e.g. lightning surge) [17]. Unlike snubbers of a conventional LCC system, SRB snubbers incur insignificant losses in steady state since the SRB is switched only under a dc fault.

When each MMC arm reactor is connected to the ac terminal such that it carries the respective SRB valve current, the reactor contributes to limiting the magnitude and dv/dt of any forward overvoltage transient impressed on the SRB valve. It may further reduce di/dt snubber requirement. This connection will also reduce time span $t_1 - t_3$ in sequence a – e.

D. Reverse Voltage Injection

The dc fault current suppression time is subject to the fault energy accumulated in the dc circuit, the speed of reverse dc voltage injection between terminals y and *y'*, and the latter's magnitude. The fault energy depends primarily on dc line type, fault location, dc chokes, and inherently on the speed of protective action. Observe that the SRB controller inhibits or retards the firing pulses at t_3 after each FMS is in open position. For a given hybrid switch isolation speed (i.e. span of interval $t_1' - t_3$), the longest time interval that elapses until the SRB injects the peak reverse dc voltage across terminals y and *y'* – when firing is inhibited – corresponds theoretically to 210º (11.7ms at 50Hz ac power frequency), and that is when the instant $t = t_3$ is in the vicinity of a commutation instant between two line-to-line ac bus voltages. The SRB dc voltage remains in reverse polarity for a further 90° up until $t_r = t_3 + 16.67$ms unless the fault current diminishes to zero before that (i.e. $t_4 < t_r$).

Alternatively, if the SRB firing angle is retarded to $\alpha > 90º$ (while accounting for a safe extinction angle γ), the dc voltage produced by the SRB can be kept at the average value given in (8) until dc fault current diminishes. In (8), $\delta = \pi - \alpha$.

$$V_{yy'} \approx -\frac{3\sqrt{2}}{\pi} V_{l-l}^{rms} \cos(\delta) \tag{8}$$

Under a dc fault, depreciation of ac bus voltage is expected. The depreciation level is subject to ac grid strength and fault current magnitude. Operation of the MMC in STATCOM mode as soon as each FMS is opened will help alleviate the voltage depreciation. This may ultimately assist in a quicker suppression of fault current. Further study of said STATCOM mode and its impact on ac voltage is required.

Selection of dc choke size is a design tradeoff. The dc choke must limit the fault current rising slope to minimize ac voltage depreciation particularly during the interval preceding MMC operation in STATCOM mode. In the same time, the dc choke size must not be too large not to trap a significant

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amount of energy during fault and, hence, delay fault current suppression. Therefore, transformer impedance can be designed to undertake a current-limiting duty.

V. A Case Study

For further study, a model of a 700 MVA ±200kV grid side HB-MMC station has been built in Simulink®/Matlab based on Fig. 1 arrangement. The station is connected to a 100km dc line in a symmetric monopole arrangement. System parameters are given in Fig. 4 and Table I. DC cable parameters are taken from the CIGRE B4 dc grid test system [18]. A 20mH dc choke is inserted in each dc pole (Fig. 4). The MMC averaged model developed in [19] is utilized. This model has been validated against a 10kW experimental platform and shows high accuracy for MMC dc fault studies [19]. The VSC station is vector controlled in a power flow control mode where dc voltage is dictated by a stiff dc source at the other side of the 100km dc cables.

Each LVCS is modeled as a 7x2 matrix of StakPak IGBT modules for an overall 15kV 1.5kA rating (refer to section IV.B). Each FMS is modeled as an ideal breaker. The SRB is modeled in detail. All IGBTs, diodes, and thyristors threshold voltages and on-state slope resistances are considered throughout as per datasheets. An inductance of 2mH per SRB thyristor valve is modeled to account for di/dt snubber reactors. This value limits di/dt to around 150A/µs.

A pole-to-pole fault 5km away from the station is simulated at t = 3s. Fault resistance is 1Ω. Figs. 5a, 5b, and 5c depict dc pole voltages and currents at the station at t = 3s when the MMC is blocked without further protective action. Fig. 5d depicts positive and negative dc pole fault current profiles when the hybrid bypass protection is activated for the same fault scenario and also when the fault distance is altered to 25km. Fig. 6 depicts various waveforms for the 5km dc fault scenario with the hybrid bypass protection and sequence a – e activated.

A 200µs fault detection time is inserted, by which the dc current hits 2pu. That's when the sequence a – e is triggered. Referring to Fig. 2, the following timing is scheduled: $t_o = 3s$, $t_1 = t_o + 250\mu s$, $t_1' = t_1 + 100\mu s$, and $t_3 = t_1' + 5ms$.

This way, a 100µs is inserted for current commutation after the SRB is triggered and 5ms elapses from LVCS turn-off until each FMS is in open position. With this timing, it can be seen the MMC is isolated in about 1ms and fault current is suppressed within 16ms (Fig. 5d and Fig. 6a) by action of the reverse dc voltage injected by the SRB (Fig. 6e).

The SRB assures a low voltage across each LVCS until the respective FMS is in open state (Fig. 6f). In Fig. 6i, the MMC dc side current is seen to diminish in $t_d \approx 2ms$ after LVCS turn-off. The corresponding value of t_d calculated by (3) using the parameters of Table I and devices datasheets is about 1.9ms, assuming an averaged voltage drop of $V_{th} = 300V$ in the SRB valves conducting the fault current during the interval $t_1' - t_2$. When the LVCS blocking voltage is designed at $V_{arr} = 20kV$, simulated value of t_d is found to drop to near 1ms; whereas (3) results in $t_d \approx 1.1ms$ in this case. It can be seen that t_d values calculated by (3) are in good agreement with numerical results.

Current distribution among the LVCS, arrester, and the snubber is shown in subplots 6j and 6k for the positive pole and negative pole LVCS arrangements, respectively. As soon as the LVCS turns off, current is seen to charge the capacitor up to the arrester protective voltage, then commutates to the conducting arrester and MMC residual energy is dissipated as confirmed by the arm currents shown in subplot 6l. Finally, Fig. 6h depicts the sum of cell voltages per arm pre- and post-fault. It reconfirms that MMC cells retain their stored energy, which assists in a quick generation of reactive power once STATCOM mode is commanded. Although operation as a STATCOM is not modeled in this example, the MMC would be able to enter this mode in about 5ms of fault detection in this example.

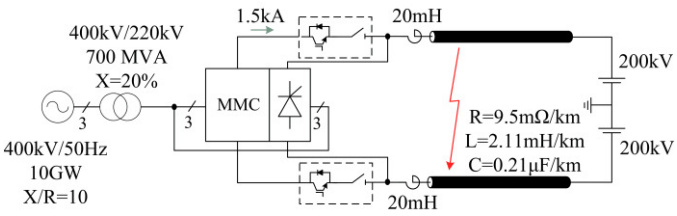

Fig. 4 A case study on a 700MVA, ±200kV MMC station.

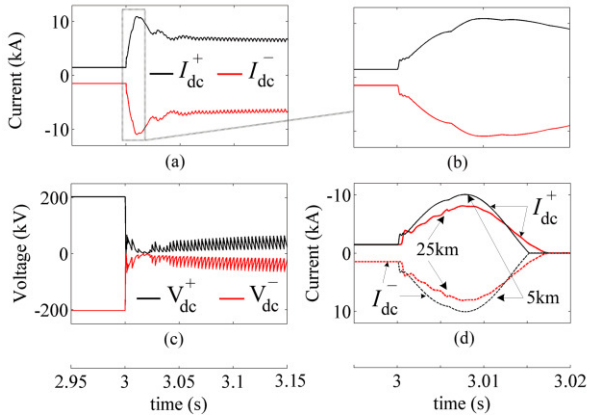

Fig. 5 Numerical simulation results for the ±200kV 700MVA test station under pole-to-pole fault 5km away at t = 3s without protection; (a) positive and negative dc pole fault current profiles with protection deactivated, (b) zoomed section of the fault current of (a), (c) positive and negative dc pole voltage profiles with protection deactivated, and (d) current profiles with hybrid bypass protection activated for two fault distances (5km and 25km).

TABLE I
PARAMETERS OF THE SIMULATED CASE STUDY

Cell capacitor (C_c)	8mF	SSCS Arrester voltage (V_{arr})	15kV
No. cells/arm (N)	135	Arrester knee current (A)	1000
Cell voltage (V_c)	3 kV	No of columns per bank	2
Arm reactor (L_{arm})	15mH	Snubber capacitor (C_s)	40µF
MMC IGBT modules		StakPak 5SNA-2000K450300 (4.5 kV – 2kA) [16]	
SSCS IGBT modules			
SRB Thyristor modules		ABB PCT 5STP 38Q4200 (4.2 kV – 6.7kA RMS) [20]	

VI. Alternative Configurations

A. Modular SRB Design

With reference to the basic hybrid bypass arrangement of Fig. 1, the SRB thyristor valves can be modularized and augmented to HB cells as introduced in section II. It follows that each thyristor needs to be at least at the same voltage rating as the cell IGBTs.

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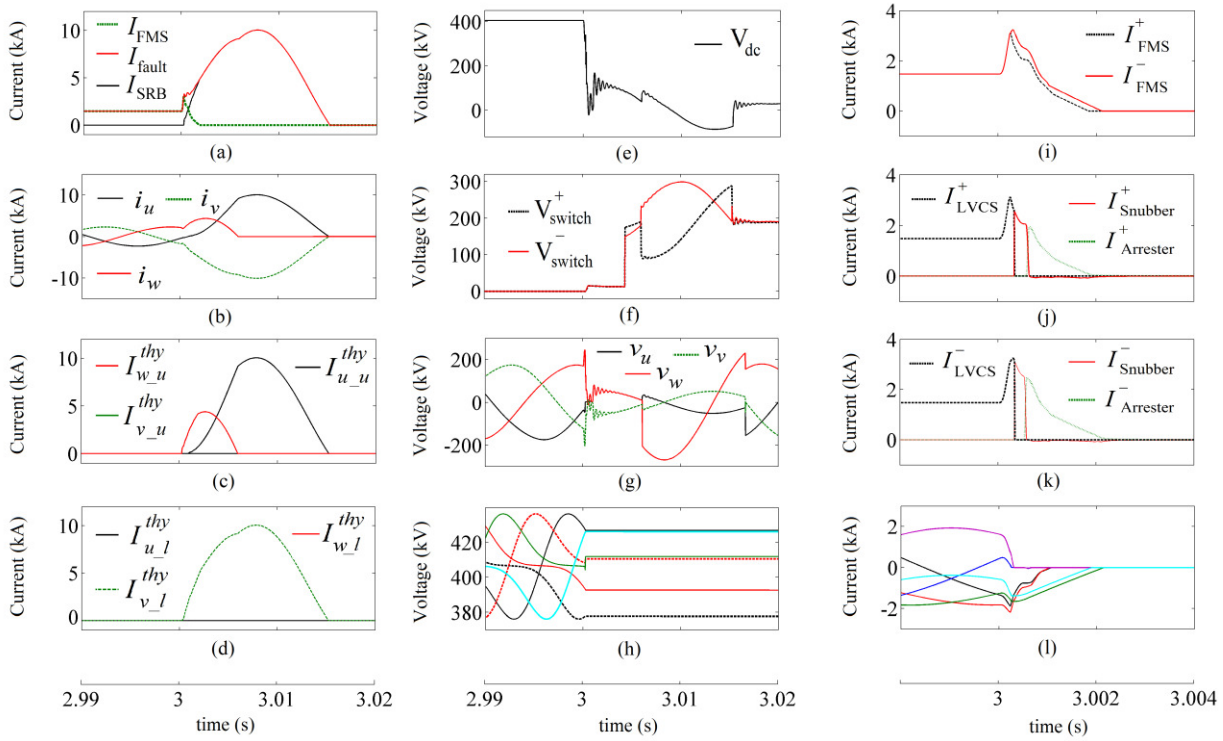

Fig. 6 Numerical simulation results for the same fault as in Fig. 4 with hybrid bypass protection scheme in operation ; (a) fault current commutation stages, (b) ac side phase currents, (c) and (d) SRB upper and lower thyristor valves currents, (e) pole-to-pole dc voltage at the SRB terminals, (f) voltage across each hybrid switch, (g) ac side phase voltages, voltage across each LVCS, (h) MMC aggregate arm voltages (sum of cell voltages), (i) currents in both FMSs , (j) and (k) current components through both switches, and (l) MMC arm currents.

When SRB thyristor valves are modularized in the manner shown by Fig. 7, FMSs need to be placed in the MMC arms. When connected otherwise in the dc poles, the trip of each FMS under fault will expose HB cells in the arms not conducting fault current to high voltages. While connecting a FMS in each MMC arm avoids this problem, it prohibits MMC operation in STATCOM mode during fault. Each FMS trips under zero-current and operating sequence a – e applies.

In each four-terminal HB cell, clamping diodes need to block the cell voltage when the thyristor is conducting. Thus, the blocking voltage of each diode should be selected higher than half the cell voltage. While said clamping diodes ensure a uniform distribution of reverse voltage among SRB valve thyristors, they are incapable of establishing a forward voltage sharing in the valve unless they have controlled-avalanche reverse characteristics (i.e. avalanche diodes). When the controlled-avalanche voltage is selected as above, the thyristor forward voltage is clamped to the cell voltage or slightly higher. SRB thyristors are forward biased only during or after a dc fault. Hence, the avalanche conduction of clamp diodes is limited to faulty conditions, whereas in steady state SRB voltage sharing is ensured by forward diode conduction. Observe that clamping diodes do not conduct neither load nor fault currents, thus can be selected with low continuous current rating.

It is worth noting that clamping diodes should be replaced with other form of voltage sharing snubber (e.g. an RC circuit) in the two outermost HB cells of each MMC phase leg. This is to break the balancing-current path created between the dc link and the phase leg cell capacitors through terminal clamp diodes. Said balancing-current path may otherwise interfere

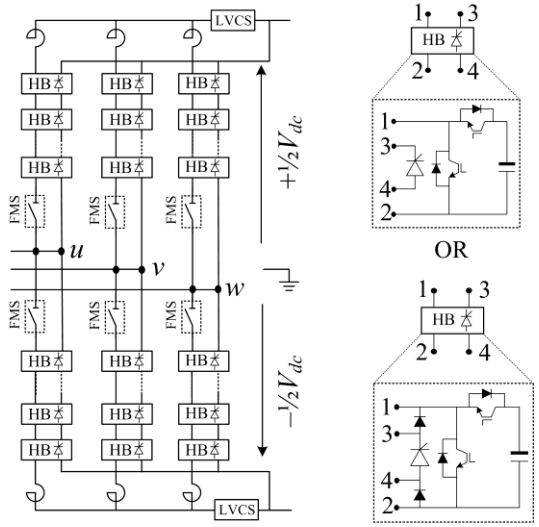

Fig. 7 A hybrid bypass protection configuration with a modular shadow rectifier bridge.

with MMC operation in steady state. Said balancing-current path could alternatively be broken if thyristor connection in said outermost HB cells is reversed, as depicted in Fig. 8. Observe that the HB cell connected to the ac pole (directly or through the arm reactor) requires a different clamping connection. Here, one clamp diode is utilized with avalanche voltage higher than the cell voltage.

B. Modular LVCS design

In another variation of the modular hybrid bypass arrangement, commutation voltage can be generated internally

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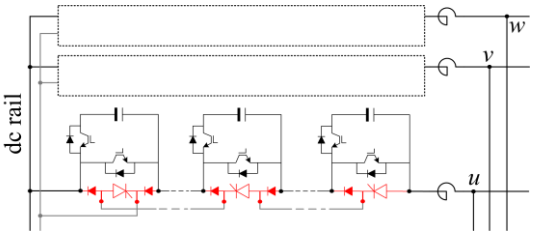

Fig. 8 Use of diodes to clamp thyristor voltages in each SRB valve.

in each MMC arm in order to divert the fault current to the SRB as part of the proposed protective sequence a – e.

Said configuration may offer further enhanced modularity by augmenting a string of a few cascaded HB commutation cells in each arm as illustrated in Fig. 9 to function as a LVCS. Said cells are connected in reverse polarity and are kept in state '1' in steady state. State '1' is defined by the IGBT T_1 being in on-state and the IGBT T_2 being in off-state (see Fig. 9). Each HB commutation cell employs a small capacitor and is shunted by an arrester bank. Under dc fault, each said commutation cell is switched to state '2' (where both IGBTs are off) at t_1' for arm current to commutate to the SRB.

Alternatively, said commutation cells can be of full-bridge (FB) or asymmetric FB structures, the latter being depicted in Fig. 9. With sufficiently high cell capacitance, FB commutation cells can operate as energy tanks in steady state contributing to MMC power conversion process. Under a dc fault, all IGBTs of the MMC, including FB commutation cells, are blocked. Hence, FB cells of each arm insert their voltage in reverse absorbing arm reactor energy. In configuration (a), where the arm reactor is off the SRB fault current path, shunt arresters may be used to dump any excess energy to avoid FB cells overvoltage. It follows that said arresters can be of lower energy rating relative to the basic LVCS design of Fig. 1.

With reference to Fig. 9a, the loop a-b-c-d is equivalent to that of Fig. 3 from the perspective of the arm current i_r. Consequently, equations (2) and (3) apply to the configuration of Fig. 9a. Here, however, V_{rev} opposing i_r flow in each MMC arm at t_1' is given as in (9).

$$V_{rev} = \begin{cases} V_{arr} & i_r < 0 \\ V_C & i_r > 0 \end{cases} \quad (9)$$

The MMC residual energy dissipation time t_d is irrelevant to the difference between (9) and (1) for $i_r > 0$. Thus, the same values of t_d obtained when the basic LVCS design of Fig. 1 is employed are expected for the design of Fig. 9a. This is confirmed in Fig. 10 which depicts numerical simulation results of the same case study of section V carried out with the MMC station configuration of Fig. 9a. Here, five commutation cells are connected in each arm with a capacitance of 40μF and about 3kV blocking voltage per HB commutation cell.

It can be observed from Figs. 10b and 10c that arm currents $i_{r(v1)}$ and $i_{r(w2)}$ start rapid decay at t_1 (since $i_r > 0$) due to the large reverse voltage as per (9), while the decay commences at t_1' at a slower rate in the arms where $i_r < 0$ at t_1. Fig. 10d shows that aggregate commutation cells voltage V_{cc} builds up rapidly to 15 kV starting at t_1' in arms where $i_r < 0$ at t_1.

In Fig. 9b where arm inductors are in the SRB fault current path, the MMC residual energy at t_1' is significantly lower. Therefore, the time span t_1' – t_2 is significantly shorter and

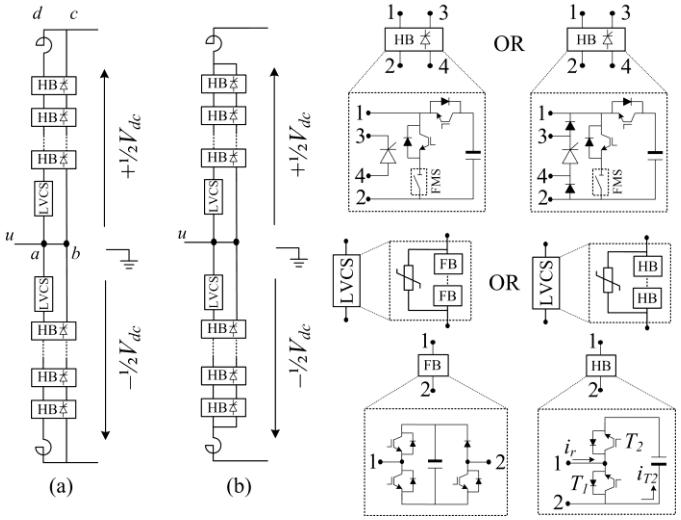

Fig. 9 Modularized configurations of the low-voltage commutation switch (LVCS) and the fast mechanical switch (FMS); (a) one phase leg of the MMC with the arm reactor off the SRB fault current path, and (b) one phase leg of the MMC with the arm reactor in the SRB fault current path.

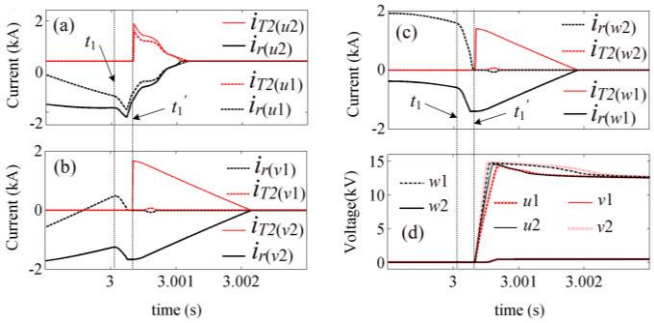

Fig. 10 Voltages and currents of HB commutation cells of the VSC station configuration of Fig. 9a simulated as part of the case study of section V; (a) phase leg u, (b) phase leg v, (c) phase leg w, and (d) Aggregate arrester knee voltages V_{cc} in all arms. [subscripts 1 and 2 denote upper and lower arm, respectively]

lower LVCS blocking voltage is required. This may facilitate a quicker fault current suppression.

C. Modular FMS design

The FMS connected in each MMC arm in Fig. 7 is depicted in Fig. 9 in modular design where a low voltage fast mechanical disconnector switch is connected in each HB cell such that its voltage is clamped by the cell voltage. Modularization of the FMS is likely to facilitate shorter trip time in comparison to the high voltage FMS design reported in [14]. On the other hand, HB cell volume will be affected and further study of the practical viability of actuation circuit in such a design is required.

D. Decoupling from AC Voltage Stiffness

Section IV-D has shown that ac voltage depreciation during the dc fault limits the reverse voltage developed across SRB dc rails. The depreciation may exacerbate when the interfaced ac connection is weak. Depending on the accumulated fault energy at the instant when the SRB firing is inhibited (at $t = t_3$), the fault current may not diminish at $t_4 \leq t_r - \gamma/\omega_s$;

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ω_s being the ac grid frequency. If t_4 does not satisfy the above relation, conducting SRB thyristor valves will remain in conduction for $t > t_r$ and the fault current will rise up again due to the forward ac voltage appearing across the SRB dc rails. Numerical simulations of such a case show that the fault current profile will resemble a 50Hz damped offset cosine wave which hits zero (and diminishes) after one or more cycles subject to ac bus voltage recovery and the fault energy.

One way to avoid this situation may be to fire SRB valves at $\alpha > 90^o$ at t_3 in a phase control mode. Alternatively, sophisticated firing schemes may be used. For instance, a controller may prohibit SRB firing signals at t_3 to inject maximum available reverse dc voltage then switch to phase control mode when needed (based on real-time measurements and estimators). Further study of SRB closed-loop dynamics impact on protection speed in this case is required.

When the MMC station is connected to a strong ac source, the above situation becomes less likely. Nevertheless, investigating the ac source strength in relation to dc fault current interruption tolerances is a primary indicator when the viability of the thyristor-based hybrid bypass arrangement for a certain application is assessed.

Otherwise, when the MMC station is interfaced to a weak ac source, the hybrid bypass concept can be modified such that fault current suppression and its time span become decoupled from the ac voltage stiffness. In doing so, the modified hybrid bypass arrangement dissipates the fault energy in arresters.

In said modified hybrid bypass design, thyristors of the SRB are replaced with diodes. An electromechanical DCCB is connected between each dc terminal of the SRB and the respective dc pole (for a symmetric monopole) as in Fig. 11. When fault current is fully commutated to the SRB and each FMS becomes in open position with full dielectric strength, fault current can be suppressed by tripping each DCCB while the MMC resumes operation in STATCOM mode. The protective sequence a – e of section III can be modified such that each DCCB is tripped at t_3 to interrupt dc fault current and insert a reverse voltage (arrester knee voltage) to dissipate dc fault energy. Since the MMC is off the fault current path as of the instant t_2, the requirements on fault breaking time are relieved due to the high pulse current rating of SRB diodes, which may facilitate the use of mechanical DCCBs with passive resonant branches.

To speed up fault current suppression in such a case, the FMSs and the electromechanical DCCBs may otherwise be tripped simultaneously at t_2. Normally, arc extinction in electromechanical DCCBs is slow relative to the operation of ultra-fast mechanical isolators. Thus, slower mechanical isolator can be used should ac source strength permit, and as long as its isolation time does not exceed the minimum arc extinction time of employed DCCBs.

The same simulation scenario of section V is repeated using the modified hybrid bypass arrangement where each DCCB is modelled as an ideal switch in parallel to an arrester bank. A delay of 10ms is inserted from fault detection before DCCB is opened in representation of the time to arc extinction. Each FMS is modelled to open 7ms after the current through the hybrid switch diminishes (i.e. $t_3 = t_2 + 7$ms). DCCB arrester knee voltage is set to 300kV which is 150% of pole voltage. DC pole fault currents and dc voltage at the MMC station is

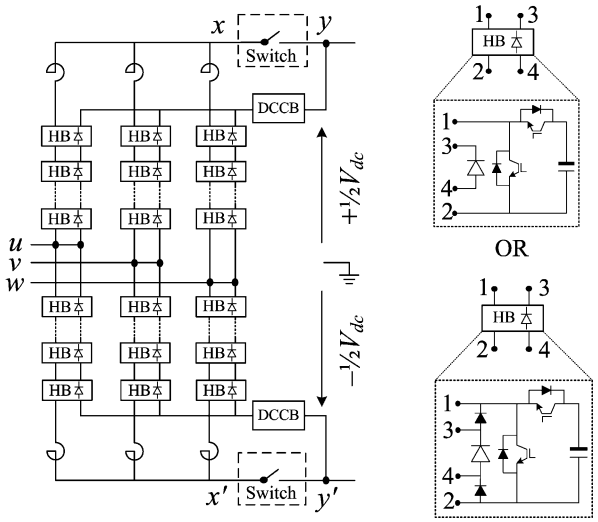

Fig. 11 A diode-based hybrid bypass protection configuration..

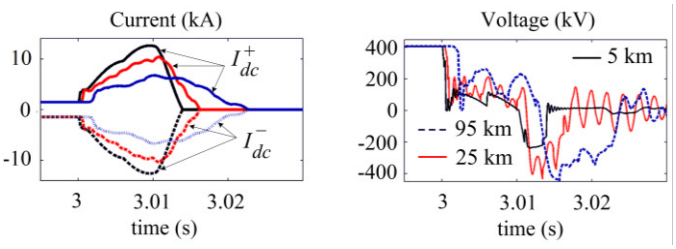

Fig. 12 Simulation results of the case study of section V utilizing the modified hybrid bypass protection configuration of Fig. 10. (a) positive and negative pole fault currents [Fault distance: 5km (black) – 25km (red) – 95km (blue)], and (b) dc voltage at the dc rails of the MMC station.

depicted in Fig. 12 for fault distances 5km, 25km, and 95km. Fig. 12 indicates that at the selected timings fault current suppression is not significantly slower than the thyristor-based hybrid bypass arrangement.

E. Utilization in VSCs with Lumped DC Capacitor

Conceptually, the hybrid bypass arrangement of Fig. 1 or Fig. 11 act to limit the high discharge current of the lumped dc-link capacitor under a dc fault as in the case of, for instance, two-level VSC stations. This is possible when the proposed protective arrangement is augmented to the VSC such that dc-link capacitor terminals are connected at points located between the LVCS and the FMS at each dc pole.

Applying the protective sequence a – e upon dc fault detection, the dc-link voltage does not drop beyond the SRB rectification voltage for the time interval $t_1 – t_3$. When each FMS is in open position at t_3, the dc-link capacitor becomes isolated from the dc poles and no further energy discharge occurs.

VII. Discussion

Currently, hybrid DCCB designs have relative advantages over other DCCBs for VSC protection. However, besides the high capital cost, the hybrid DCCB footprint may impact real estate costs of a VSC station. In comparing hybrid DCCBs to the proposed hybrid bypass arrangement for VSC dc fault protection, the semiconductors of the latter can be augmented

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to the existing MMC structure, with potential manufacturing and footprint advantages. Also, the incurred steady-state losses are comparable to these of hybrid DCCBs.

Holistically, with regards to VSC dc fault protection, the following can be identified as merits of the proposed hybrid bypass concept:

- The VSC can be immediately isolated and dc fault current commutates to a separate auxiliary path. Thus, VSC semiconductors need not be rated to handle high fault currents;
- Said auxiliary path comprises thyristors or diodes which are robust semiconductor devices of high pulse current capability;
- In the configurations of Fig. 1 and Fig. 11, the VSC can operate as a STATCOM before dc fault current is suppressed. This supports grid voltage and improves system stability;
- Insignificant increase of semiconductors in the conduction path in normal operation. Therefore, insignificant steady state conduction loss and cooling load are incurred by the hybrid bypass arrangement;
- Quick isolation of the VSC from the dc fault current path prevents full discharge of lumped dc link capacitor (if present);
- Total added semiconductor power is significantly lower than the solutions in which the VSC employs bipolar or blocking switching cell designs;
- Total added silicon area is comparable to the conventional thyristor bypass concept, albeit with the advantage of independent controllability of the bypass path;
- The hybrid bypass arrangement can be modularized in multiple ways such that modularity of the converter station is not compromised.
- With a thyristor SRB, dc fault current suppression does not involve switching overvoltages. Thus, high voltage varistors are not needed to dissipate dc circuit energy;
- Utilized thyristors or diodes undergo less thermal stress compared to the conventional thyristor bypass solution due to the faster fault current suppression; and;
- AC circuit breakers trip is not required for temporary dc faults. This facilitates 'reclosing' as in LCC HVDC systems.

In light of the above points, it can be concluded that the thyristor-based hybrid bypass arrangement may be advantageous for handling temporary dc faults on point-to-point overhead HVDC links when compared to fast DCCBs or the combination of slow DCCBs and thyristor bypasses at each VSC terminal.

With regards to reclosing after a dc fault on an overhead HVDC line, the thyristor SRB is capable of controlled re-energization of the dc line multiple times until the fault is cleared or considered permanent. In relevant configurations, reclosing attempts do not interfere with MMC operation as a STATCOM.

It is noteworthy that the dissipation of fault energy in arrester banks as needed in the diode-based hybrid bypass arrangement may restrict reclosing speed due to potential overheating of arrester banks unless faster DCCB designs are employed.

Conventional thyristor bypasses are normally deemed sufficient for VSC protection in cable HVDC links due to the permanent nature of dc faults. However, the resulting trip of ac breakers implies that the VSC cannot engage in reactive power support for at least over a hundred milliseconds following fault inception. This may have an adverse impact on ac voltage recovery in a weak ac connection, or may not be compliant with the applied grid code. The utilization of the hybrid bypass arrangement of Fig. 11 (and in theory that of Fig. 1) may offer some advantage in such cases since the VSC resumes operation in STATCOM mode in a few milliseconds after fault detection. The fault current suppression time in this case is irrelevant so long as the SRB semiconductors are not exposed to destructive overheating. Subject to design trade-offs and gird code requirements, high speed FMSs may not be a necessity in such a case and slower mechanical isolators may be tolerated.

The hybrid bypass concept might be suitable for VSC protection in radial (or lightly meshed [21]) multi-terminal HVDC networks particularly with overhead line sections. Nevertheless, DCCBs (or other means) are still required at internal dc nodes to create defined protection zones and to minimize fault impact on healthy network sections.

Without added equipment, the hybrid bypass protection may not be effective when more than one dc line is connected to the VSC station as a part of a meshed multi-terminal HVDC network. Protective action in response to a dc fault at one line will temporarily interrupt power flow in the other line(s) connected to the station. At current state-of-the-art, hybrid DCCBs may be one possible solution to avoid temporary outage of the healthy line(s) in such a case, despite their complexity, cost, and footprint.

VIII. Conclusion

A low-loss dc fault ride through scheme for HB-MMC stations, denoted hybrid bypass, is proposed. In its primary structure, it administers dc fault current suppression akin to LCC HVDC links. In a detailed case study, it was possible to fully bypass the MMC semiconductors right after protective action has been triggered in response to a near pole-to-pole dc fault. In said case study, dc fault current was suppressed in less than one cycle of ac voltage. It was shown that extra steady state losses incurred by the proposed arrangement are trivial compared to total converter station losses.

The proposed concept does not compromise converter modularity and offers controlled 'reclosing' which is desirable for recovery from temporary faults on overhead lines. Some configurations may also be useful for VSC dc fault protection in cable HVDC links interfaced to weak ac sources where reactive power support during fault may be important.

It was found that recovery from distant temporary dc faults on an overhead HVDC line connected to a weak ac source is relatively slower. Structural modifications of the hybrid bypass which decouple the protective action from ac source stiffness were proposed to address this issue. Said modifications require further technical and economical evaluations.

Overall, further investigations of system- and device-level aspects of the proposed VSC protection concepts are needed for better evaluation of their efficacy and practicality.

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