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Can conventional phase-change memory devices be scaled down to single-nanometre dimensions?

Hasan Hayat[1], Krisztian Kohary[2] and C. David Wright[1]

[1]*College of Engineering, Mathematics and Physical Sciences, University of Exeter, Exeter, EX4 4QF, UK*
[2]*Kalman Kando Faculty of Electrical Engineering, Obuda University, Becsi ut 94-96, H-1034, Hungary*

Email: hh264@exeter.ac.uk, kohary.krisztian@kvk.uni-obuda.hu, david.wright@exeter.ac.uk

Abstract

The scaling potential of "mushroom-type" phase-change memory devices is evaluated, down to single-nanometre dimensions, using physically realistic simulations that combine electro-thermal modelling with a Gillespie Cellular Automata phase-transformation approach. We found that cells with heater contact sizes as small as 6 nm could be successfully amorphized and re-crystallized (RESET and SET) using moderate excitation voltages. However, to enable the efficient formation of amorphous domes during RESET in small cells (heater contact diameters of 10 nm or less), it was necessary to improve the thermal confinement of the cell to reduce heat loss via the electrodes. The resistance window between the SET and RESET states decreased as the cell size reduced, but it was still more than an order of magnitude even for the smallest cells. As expected, the RESET current reduced as the cells got smaller; indeed, RESET current scaled with the inverse of the heater contact diameter and ultra-small RESET currents of only 19 µA were achieved for the smallest cells. Our results show that the conventional mushroom-type phase-change cell architecture is scalable and operable in the sub-10nm region.

Keywords phase-change memory, scaling, sub-10nm, RESET current, heat confinement

1. Introduction

Non-volatile, random-access phase-change memories (PCMs) are one of the prime contenders to supplement, or even replace, silicon-based memories in a number of important technology areas including those currently dominated by CMOS Flash-type devices, in the emerging sector of so-called storage class memory (SCM) and even possibly in DRAM-type applications [1, 2]. Novel functionalities demonstrated by phase-change memory-type devices, such as the implementation of neuronal and synaptic mimics [3-5], arithmetic and logic processing [6-9] all-photonic memories [10] and even the realization of non-volatile

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optoelectronic displays [11] have also heightened interest and elucidated the undoubted importance and potential of phase-change based devices.

In phase-change memory cells, information is stored in the local atomic arrangement of the 'active' region of the cell. For electronic, binary memory-type applications (the subject of this paper) the active region of the cell is switched between the high-resistance amorphous (or RESET) state and the low-resistance crystalline (or SET) state, using appropriate electrical excitations, i.e. appropriate voltage pulses. In general, higher-amplitude short-duration RESET pulses place the memory cell into the amorphous state, whereas more moderate and longer duration SET pulses switch it back to the crystalline state. The state of the cell (1 or 0) is read out by sensing the resistance using a low voltage read pulse that does not disturb the stored state.

A typical PCM cell consists of the active phase-change material, e.g. the chalcogenide alloy $Ge_2Sb_2Te_5$ (or GST) as used in this work, sandwiched between two metal electrodes (e.g. TiN and W) and insulated from adjacent cells using a dielectric material such as SiO_2. The most established structure in this regard is the so-called "mushroom" (or "lance") cell, for which a schematic and TEM image is shown in Figure 1 and in which the phase-change material and top electrode are planar layers deposited and patterned on a pillar-like bottom "heater" contact. Note that this bottom contact is usually fabricated from doped TiN and has a higher electrical resistance (and lower thermal conductivity) compared to usual metal electrode materials. In normal device operation, a portion of the phase-change layer sitting directly on top of the heater contact is switched between the amorphous and crystal phases such that the active region within the phase-change layer and the heater pillar resemble a mushroom in shape, hence the name (see the blue and orange shaded regions in Figure 1(a), and the amorphized dome in TEM image of Figure 1(b)). The use of the pillar-type contact in the mushroom cell is attractive since, as is obvious from Figure 1, it helps to limit the volume of phase-change material that has to be amorphized and re-cystallized, thus also limiting the switching current and power. Since during the amorphization (RESET) process the switching volume has to be heated up to temperatures above melting (~ 620 ^{o}C for GST), it is the RESET process that is the most current and power demanding process in PCM operation. The reduction of the RESET current and power is thus probably the primary issue of concern in terms of the development of viable phase-change memories.

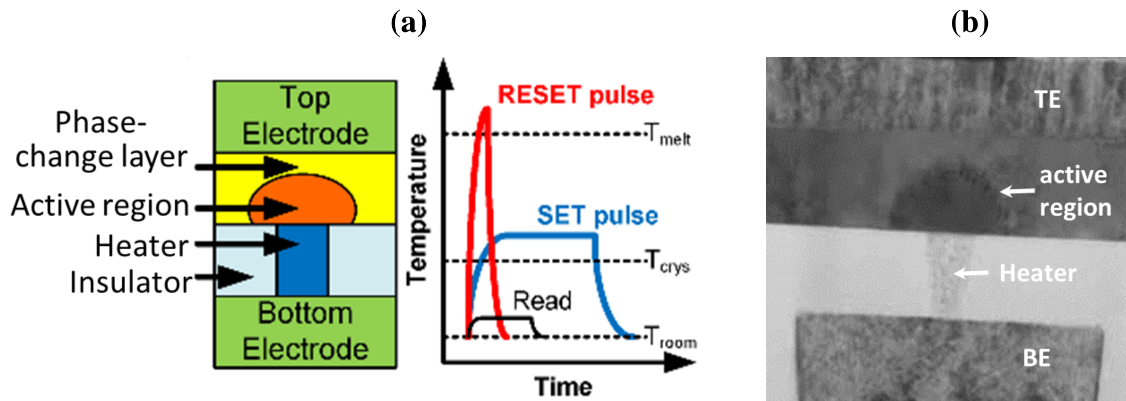

Figure 1. (a) Schematic of a typical mushroom cell structure widely used for PCM devices (and schematic of write and read pules). (b) TEM Cross-section of a mushroom type PCM showing the rounded amorphous dome formed above the heater. (Reprinted with permission from [12]; copyright AIP Publishing LLC 2011).

A key approach to reducing the RESET current (and power) is size-scaling; as the volume of phase-change material involved in the switching process is reduced (by shrinking the cell size, in particular the heater electrode contact area), the energy required for switching also reduces (and hence the current). However, despite the relative maturity of the mushroom-type PCM cell, it appears that the smallest such cells to have been successfully fabricated to date (or at least the smallest that have been publicly reported) are at the 90 nm node, with a corresponding heater contact diameter of approximately 60 nm [13]. In similar vein, most theoretical scaling studies have been either analytical in nature (e.g. [14-16]) and/or have not addressed the likely performance of mushroom-type cells at single-nanometer dimensions. From the results of research-oriented (and probably un-manufacturable, at least in a commercially-viable way) phase-change memory cell designs that used carbon nanotubes as electrodes [17-19] we know that it should be possible for phase-change memories to operate at single-nanometre length scales, but it is not clear whether or not this can achieved using practicable cell designs such as the conventional mushroom-type cell. To address this omission, in this paper we carry out detailed physically-realistic simulations of the performance of PCM mushroom-type cells down to single-nanometre dimensions (specifically down to heater electrode contact diameters of 6 nm) using a sophisticated phase change model, and investigate the effects of size scaling on key device characteristics, in particular the effects of scaling on what is the most critical performance limiting parameter in terms of PCM device operation, namely the RESET switching current.

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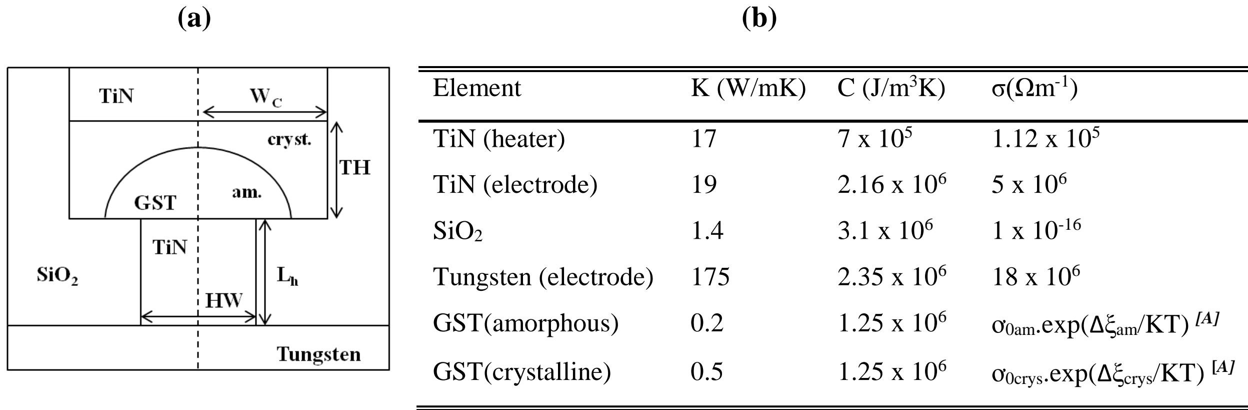
2. Simulation methods

In order to simulate in a physically realistic way the switching processes in the PCM cell we need to combine electrical, thermal and phase-transformation models. Our electrical and thermal models are implemented using finite-element software (COMSOL^{TM}) and solve, simultaneously, the Laplace and heat-diffusion equations to calculate at each time step and for any given electrical excitation (i.e. for any input voltage pulse), the 3D (or pseudo-3D, i.e. 2D with assumed cylindrical symmetry in the case of the mushroom-type cell) temperature distribution throughout the cell. This temperature distribution drives a phase-transformation model, for which we use a Gillespie Cellular Automata (GCA) approach that combines thermodynamic features of rate-equation methods with elements from probabilistic cellular automata models and uses the Gillespie algorithm for efficient time-stepping.

Our GCA model has been previously described in detail [20] but in summary considers a homogeneous, isotropic material in a square lattice where the state of the material is described through a set of points in the lattice that can be either crystalline or amorphous. The state of each point (i,j) in the lattice is described by two quantities; r_{ij} , the phase of the (i,j) site (which takes the values 0 and 1 for amorphous and crystalline respectively), and Φ_{ij} , which defines an orientation (with two adjacent crystalline sites belonging to same crystallite (crystal grain) if they have the same orientation). The local changes that can occur are defined by three events: nucleation, where site (i,j) and an adjacent site, originally both amorphous, become a single crystallite; growth, where site (i,j), originally amorphous, becomes attached to an adjacent crystal; dissociation, where site (i,j), originally crystalline, detaches from the crystal of which it is a part to become amorphous. The rate at which each of these three events occurs is determined by the system energy, which is usually described in terms of the Gibbs free energy G, where $G = (AS - Vg)$ and A and V are the surface area and volume respectively of a crystal cluster, S is the surface energy and g the bulk free energy difference between phases. The bulk energy difference term g is considered to be purely temperature dependent (for example as $g(T)= H_f (7T/T_m)[(T_m-T)/(T_m+6T)]$ where H_f is the enthalpy of fusion and T_m is the melting point) [21].

The form of mushroom cell simulated is that shown in the schematic in Figure 2(a) and having a heater diameter HW, a phase-change (GST) layer thickness of TH and with the horizontal extent (half-width) of the phase-change layer being W_c. Scaling of the PCM was achieved by simultaneously reducing HW, TH and W_c (specifically we reduced the heater width HW from 100 nm down to 6 nm while keeping the ratio of TH/HW and W_c/TH constant at 1.2 and 1.25 respectively). In our simulations the PCM cell was embedded into a virtual test bench consisting of an electrical pulse source and an external (series) load resistance of 10 kΩ. Trapezoidal RESET and SET and voltage pulses of various amplitudes (1.3 to 3.0 V) and durations (20 to 100 ns) were used to switch the cell, with fast fall times (5 ns or less) in the case of the

RESET pulse to facilitate the rapid cooling needed to form the melt-quenched amorphous phase. The electro-thermal material parameters used in our simulations are listed in Figure 2(b), and the phase-change modelling parameters are equivalent to those presented in [22].



Element	K (W/mK)	C (J/m^{3}K)	σ(Ωm^{-1})
TiN (heater)	17	7 x 10^5	1.12 x 10^5
TiN (electrode)	19	2.16 x 10^6	5 x 10^6
SiO_2	1.4	3.1 x 10^6	1 x 10^{-16}
Tungsten (electrode)	175	2.35 x 10^6	18 x 10^6
GST(amorphous)	0.2	1.25 x 10^6	$\sigma_{0am}.\exp(\Delta\xi_{am}/KT)$ *[A]*
GST(crystalline)	0.5	1.25 x 10^6	$\sigma_{0crys}.\exp(\Delta\xi_{crys}/KT)$ *[A]*

Figure 2. (a) Schematic of the PCM simulation cell showing the key scaled features of heater width, HW, GST layer thickness, TH, and GST layer (half) width, W_c. (b) Materials parameters used in the simulations equivalent to those presented in [22]. (*[A] See C. D. Wright et al, IEEE Transactions on Nanotechnology, 6, 1, (2006)*).

3. Results

3.1 The RESET process in nanoscaled PCM cells

Since RESET is the most critical process in terms of PCM performance limitations, we begin our study by investigating the effects of scaling on RESET process characteristics. We show in Figure 3(a) the simulated temperature distribution (at the point in the RESET process where the maximum temperature develops, which is invariably just before the start of the falling edge of the pulse) in a large cell having a 100 nm diameter heater electrode and subject to a 2.5 V, 40 ns input pulse (having rise/fall times of 15/5 ns). The RESET pulse heats the GST material adjacent to the heater contact to above its melting temperature, and it subsequently cools into a dome-shaped amorphous region, as shown in Figure 3(b). The amorphous dome is slightly larger than the bottom heater width (i.e. dome width > HW/2), ensuring, as desired, a high-resistance path on readout between the top and bottom electrodes. As we scale the cell size down, the size of the melted and subsequently amorphized region also scales down, as can also be seen in Figure 3(b). In all cases for heater widths down to 15 nm the cell was successfully amorphized, i.e. a region above the heater was heated to above melting temperature and a region larger than the heater width cooled

into the amorphous phase, for the 2.5 V, 40 ns RESET pulse used (indeed, successful amorphization was also achieved for lower amplitude, 2 V, input pulses). For cells with heater widths below 15 nm however, or more specifically for cells with heater widths of 10, 8 and 6 nm, it proved impossible to produce an amorphous dome for RESET pulses of 2.0 V or 2.5 V (or even for 3 V).

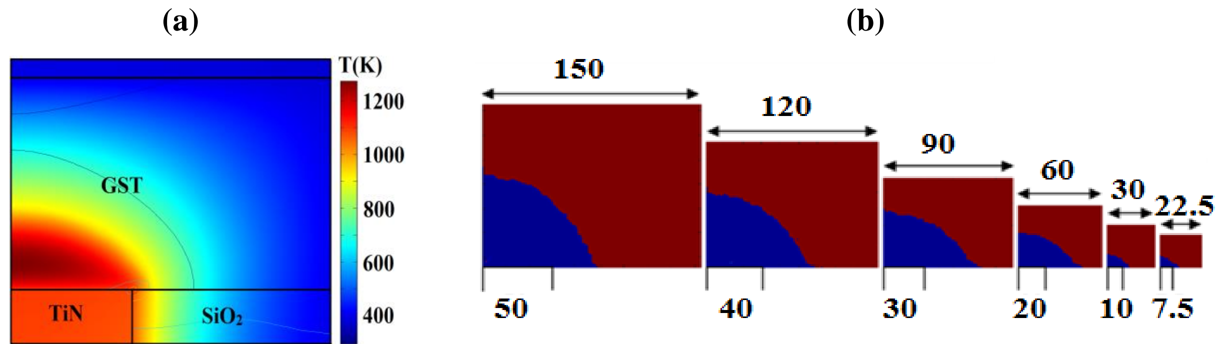


Figure 3. (a) Temperature distribution (at the time of occurrence of maximum temperature) during the RESET process (2.5 V, 40 ns pulse) in large PCM cell having heater width of 100 nm (it is clear that the melting temperature of GST is exceeded in a dome-like region above the heater contact). (b) Successful formation of amorphous regions (shown in blue) at the end of the RESET process as cells are scaled down in size and for heater widths down to 15 nm (plots show one half of the GST layer and numbers at the top and bottom of plots show the GST width, Wc and the heater half-width, HW/2 respectively, both in nanometres).

The reason for the inability to melt the active region, and hence form an amorphous dome, above the heater contact for the smallest cells (i.e. cells with heaters of widths 10 nm or less) is the additional heat loss to the electrodes, particularly to the top electrode, resulting from the scaling down of the cell. This results in lower temperatures, cf. larger cells, in the switching volume for a given RESET voltage pulse. This is illustrated in Figure 4(a), where the temperature distribution during RESET (using a 2.5 V, 40 ns pulse) for a cell with a 10 nm heater contact is shown; the maximum temperature reached in the GST layer is only 640 K and as a result no melting (and no subsequent amorphization) can occur (compare to the case for the larger cell of Figure 3(a) where the maximum temperature is 1250 K under the same RESET conditions). One obvious way to increase the maximum temperature reached in the GST layer is to increase the excitation energy provided by the RESET pulse, e.g. by increasing the RESET voltage amplitude. While this is certainly effective, for example we confirmed by simulation that a 5 V, 40 ns RESET pulse successfully amorphizes cells down to 6 nm heater sizes, it is undesirable since it significantly increases

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the RESET power, which is contrary to the main aim of scaling which is to reduce RESET power consumption. A more intelligent approach however is to use material engineering to modify the thermal properties of the cell so as to retain more heat, while at the same time still enabling the rapid cooling (typically several 10s of Kelvin per nanosecond) needed to quench the melted GST into the amorphous phase. One approach to this is the introduction of thermal barrier layers between the bottom and/or top electrodes. For example, Ahn et al. recently showed that graphene can provide a very useful thermal barrier layer in PCM cells, with PCM cells having a graphene layer inserted above the bottom electrode having ~ 40% lower RESET power as compared to notionally identical control devices without the graphene layer [23]. Another, more practicable, approach is to modify the thermal conductivity of the electrodes themselves, while at the same time maintaining adequate electrical contact. In particular, Lu et al. [24-25] found that by stacking many very thin layers of two commonly used electrode materials, TiN and W, together to create a super-lattice-like electrode structure, the thermal conductivity can be reduced to below 1 $Wm^{-1}K^{-1}$ (cf. typically > 10 and > 100 for single layers of TiN and W alone) and while retaining good electrical conductivity. Using such a multi-layered TiN/W super-lattice-like top electrode Lu et al. showed that significant reductions in RESET voltages and powers could be achieved, although their work was confined to very large cell sizes (190 nm diameter heater contracts).

We also found that the use of a stacked top electrode was very effective in terms of heat confinement and subsequent reduction of melting voltages. For example, in Figure 4(b) we compare the maximum temperature reached in the GST layer during a 2.5 V/40 ns RESET pulse, applied to a cell having 10 nm heater contract width, for both a single layer TiN electrode of 50 nm thickness and a multi-layer electrode (also of 50 nm total thickness) comprising alternating 5 nm layers of TiN and W (thermal conductivity, K, of 0.42 W/mK [25]). It is clear that the stacked TiN/W electrode enables very significantly increased temperatures (cf. the single layer TiN electrode) to be reached for the same excitation conditions, with the maximum temperature achieved in the stacked electrode case of approximately 1000 K being well above the melting temperature of GST (compared to only 640 K, well below the GST melting temperature, for the single layer TiN electrode). By using a stacked top electrode we were thus able to achieve successful amorphization in even the smallest cell sizes (and for RESET voltages as low as 2 V), as shown in Figure 4(c). As expected, our simulations confirm that the scaling down of the PCM cell has very advantageous effects on the RESET current and power, a point to which we will return in §4.

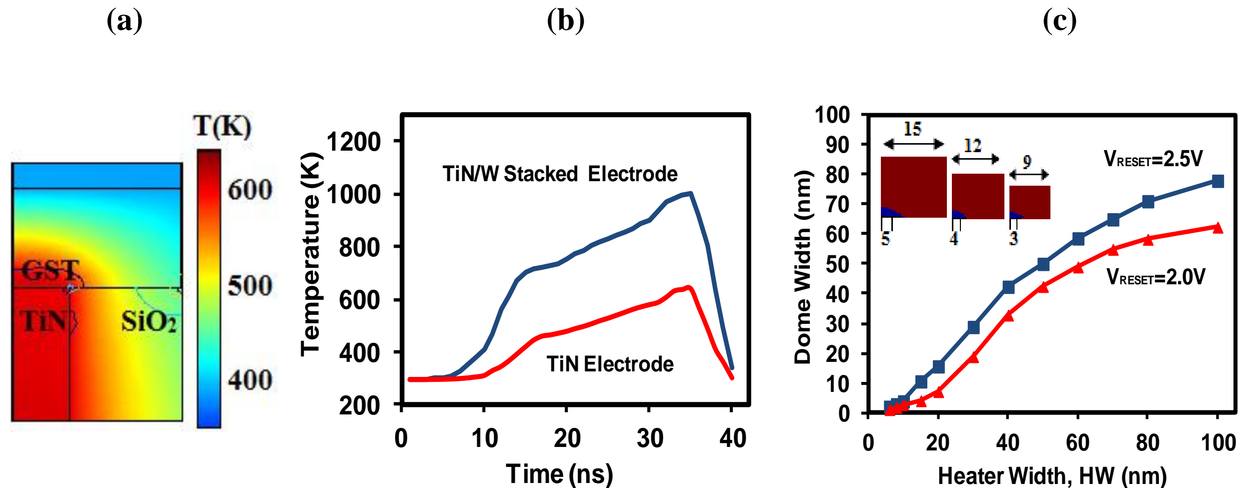

Figure 4. (a) Temperature distribution (at the time of occurrence of maximum temperature) during the RESET process (2.5 V, 40 ns pulse) in small PCM cell having heater width of 10 nm (it is clear that the melting temperature of GST is not reached). (b) Maximum temperature reached in the GST layer during a 2.5 V, 40 ns RESET process for a single layer TiN top electrode and a multi-layered TiN/W top electrode. (c) The width of the amorphized dome as a function of cell size (heater width) for 40 ns RESET pulses of 2.5 V and 2.0 V. Successful RESET is achieved in all cases (dome width > heater width), but for the smallest cells (heater widths ≤ 10 nm) a stacked TiN/W top electrode had to be used. Inset shows amorphous regions (blue) at the end of the RESET process for the smallest cells (numbers at the top and bottom of plots show the GST width, Wc, and the heater half-width, HW/2 respectively, both in nanometres).

3.2 The SET process in nanoscaled PCM cells

The SET process consists of re-crystallization of the amorphous region formed during the RESET process. Such re-crystallization can occur via nucleation and growth of new crystallites within the amorphous region and/or growth from the crystal-amorphous boundary existing at the edge of the amorphous dome (i.e. the border between the blue and brown regions in Figure 3(b) etc.). To ensure rapid crystallization, the amorphous region should be heated to temperatures close to those at which the maximum nucleation rate and/or crystal growth rate occurs. For GST such temperatures are around 400°C and 550°C respectively [26-27], considerably higher than the crystallization temperature of around 160°C that is usually measured in ‘static’ laboratory measurements (such as via heating samples on a hot-plate, see e.g. [28, 29]), but considerably lower than the melting temperature. SET pulse amplitudes are thus typically lower, and pulse durations longer (to allow time for full re-crystallization to occur) as compared to RESET pulses (see schematic in Figure 1(a)). Here we used SET pulses in the range 1.3 to 1.7 V in amplitude and 100 ns in

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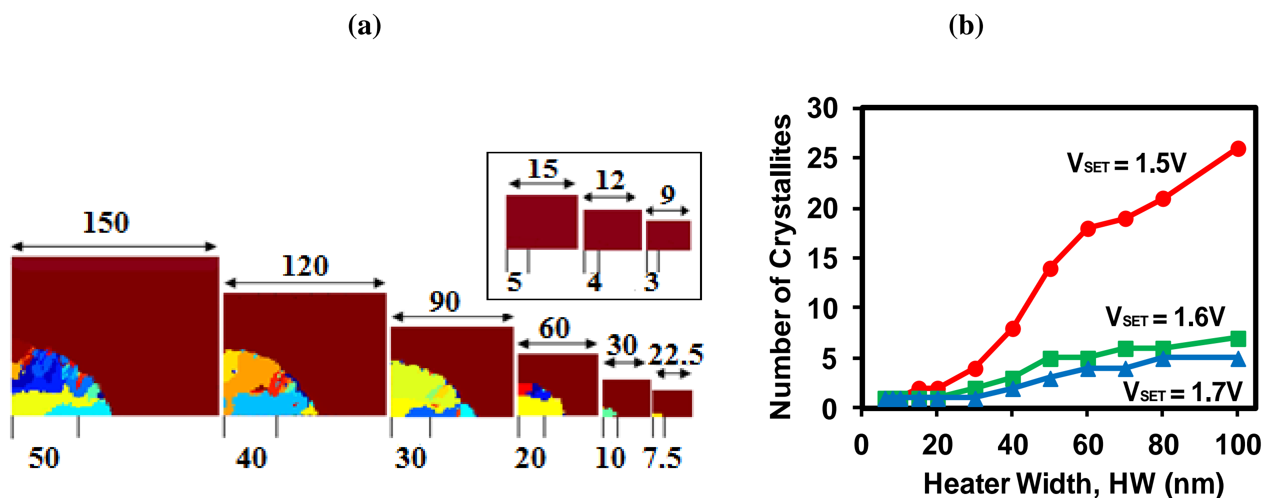
duration (with rise/fall times of 30/30 ns). We found that full re-crystallization of the amorphous domes was achieved for all cell sizes for SET pulses with amplitudes $V_{SET} \geq 1.5$ V.

The results for a typical set of re-crystallization simulations are shown in Figure 5(a), in this case for a SET pulse of 1.5 V and 100 ns. It can be seen that for the larger cells re-crystallization has occurred via the nucleation (and subsequent growth) of many new crystallites within the originally amorphous dome, but as the cell shrinks the number of new crystallites formed is reduced until, for smallest of cells (HW ≤ 10 nm) re-crystallization has occurred entirely via growth from the surrounding crystalline matrix (note: for HW ≤ 10nm, stacked TiN/W top electrodes were again used). This change in mechanism from nucleation-dominated to growth-dominated crystallization reflects both a change in temperature distributions as the cell is scaled down, as well as the fact that for any given nucleation rate the number of crystallites formed in a given time will be smaller in a smaller volume. Such behavior is corroborated in Figure 5(b) where we show the number of crystallites formed during the SET process as a function of cell size (heater width) for SET pulses of amplitudes 1.5, 1.6 and 1.7 V. We see that as the cell shrinks, the number of crystallites formed invariably falls, and that larger SET pulse amplitudes, which lead to higher temperatures preferentially favouring growth, also reduce the number of crystallites. Indeed, we can, using our GCA phase-transition simulation method, track the nucleation and growth processes during the entire SET process to reveal the nucleation and growth contributions to re-crystallization in detail, as shown in Figures 5(c) and 5(d).



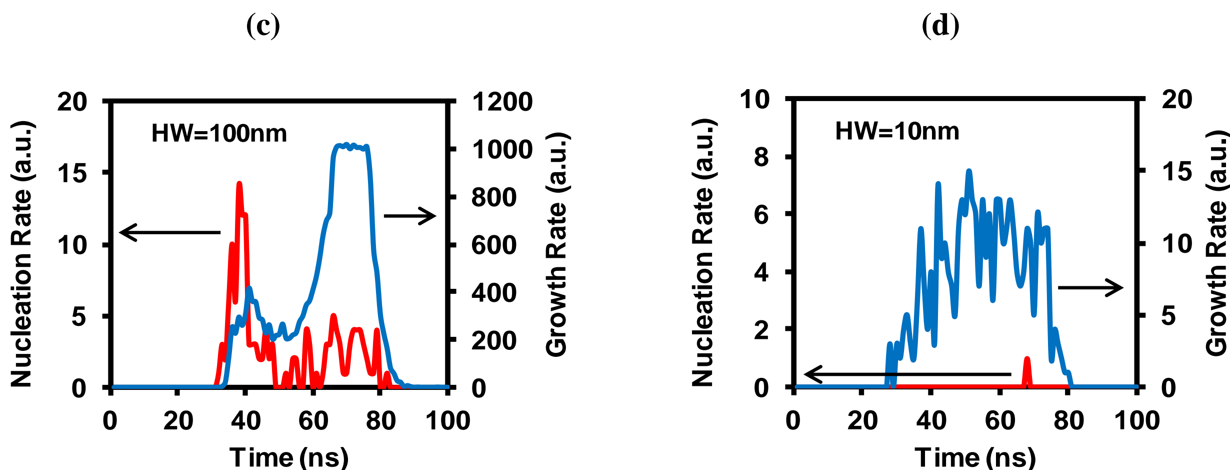


Figure 5. (a) Re-crystallization of the amorphous domes shown in Figure 3(b) and 4(c) using a SET pulse of 1.5 V and 100 ns duration. (b) The number of crystallites formed during the SET process as a function of cell size (shown as heater width) and for different SET pulse amplitudes. (c) & (d) The nucleation and growth rates during the SET process (1.5 V, 100 ns pulse) for a 100 nm (heater width) cell (c) and a 10 nm cell (d).

4. Discussion

The results of §3 above show that it should, using reasonable voltages, be possible to successfully amorphize and re-crystallize conventional phase-change mushroom-type cells scaled down to single-nanometre dimensions (specifically down to heater contact sizes of 6 nm). What we have not considered so far is the resistance window, i.e. the difference in resistances between the SET and RESET states, and how this is affected by scaling. The resistance window should remain large enough to allow for reliable differentiation on readout between the two states in the presence of noise, cell-to-cell variability etc. In addition, the SET resistance, R_{SET}, should not be too large since the value of R_{SET} affects the size of the readout current and ultimately determines the minimum time needed to sense the state of the cell during readout (see e.g. [30]). We therefore plot in Figure 6(a) the variation of cell resistance as a function of cell size (for the results of Figure 3(b), 4(c) and 5(a)). The resistance window decreases from a factor of around 100 for the largest cells, to just over 10 for the smallest. While such a window is still eminently usable, a larger window would be preferable. In addition it is clear from Figure 6(a) that the absolute value of resistance also increases as cells shrink in size, with R_{SET} increasing from around 10 kΩ to almost 430 kΩ. Such increases are largely due to geometric effects, since the cell resistance scales very approximately with 1/HW (see [14]). The undesirable rise in R_{SET} and the reduction of the resistance window can be compensated for to some degree by scaling of the heater length along with its width. For example, if we

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allow the heater length, L_H (see Figure 2(a)), to be reduced to 10 nm for the smallest cell sizes (i.e. those with HW $\leq$ 10 nm), then the SET resistance can be reduced, and the resistance window increased, as shown in Figure 6(a). This is because for the SET state the resistance, R_H, of the heater itself contributes very significantly to the total cell resistance and, since R_H scales with heater length L_H (since $R_H = 4\rho_H L_H/\pi(HW)^2$) we can reduce R_{SET} by shortening the heater.

Finally we turn our attention to probably the main advantage of device scaling in phase-change memories, namely that as we reduce the cell size the RESET current should also be reduced. Since large RESET currents are one of the main drawbacks of PCM technology at larger technology nodes (since it leads to large power consumption and the requirement for any selector devices used in the cell array to be have very high current density capabilities), moving to smaller PCM cell sizes is a most attractive proposition. Simple electro-thermal models (i.e. models with no phase-transformations included) of scaling in PCM devices predict that the RESET current should scale as 1/(contact size), and experimental results on a range of product-type cell designs (including the mushroom type) have roughly followed such a prediction, at least down to the smallest RESET currents (~ 100 μA) so far achieved in commercial-type devices (see Figure 6(b)). Our physically-realistic simulations of the performance of truly nanoscale product-type mushroom cells also show a RESET current amplitude that scales as 1/(contact size), as shown by the (green) triangle symbols in Figure 6(b). Indeed, we find that the most heavily scaled mushroom cells (6 nm heater diameter) deliver a RESET current as small as 19 μA, not so far removed from that (5 μA) obtained by Xiong et al. for experimental, research-type (i.e. non product-oriented) cells that used carbon nanotube (CNT) electrodes with ~ 3 nm contact diameter (result also shown in Figure 6(b). Our simulations show therefore that, with proper thermal design, the simple mushroom-type PCM cell design can indeed deliver excellent RESET performance when scaled to single-nanometre dimensions, matching that of much more ‘exotic’ cell designs.

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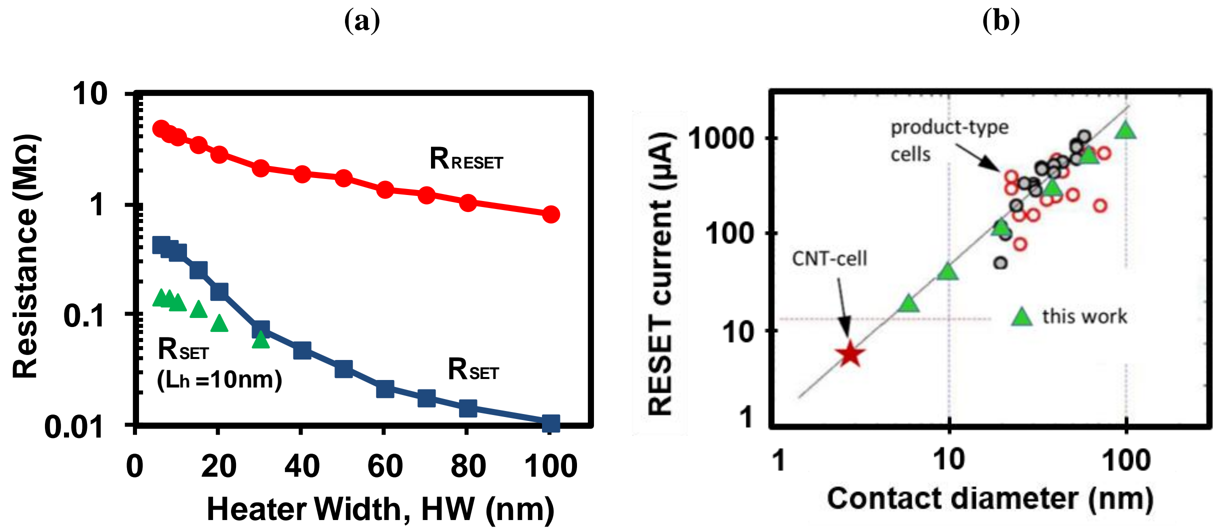

Figure 6. (a) Cell resistance in SET and RESET states as a function of heater contact size (green triangles show R_{SET} for the case of a reduced heater length of 10 nm). (b) RESET current amplitude as a function of contact size (adapted from [31] for the mushroom-type cells of this work (triangles), for various product-type cells reported in the literature (circles) and for the CNT-contact cell (star) reported by Xiong et al. [17].

5. Conclusions

We have investigated, using a physically-realistic simulation approach, the scalability of non-volatile phase-change memories having the conventional mushroom-type cell architecture. We found that such cells could be scaled successfully down to single nanometre dimensions, specifically down to heater electrode diameters of 6 nm and phase-change layer thicknesses of 7.2 nm. However, to enable the efficient formation of amorphous domes during the RESET process in small cells (heater contact diameters of 10 nm or less), it was necessary to improve the thermal confinement of the cell to reduce heat loss via the electrodes. We did this using a stacked, super-lattice like top electrode, but alternative approaches are also possible (e.g. via the use of a thermal barrier layer between one or more of the electrodes and the phase-change layer). The resistance window between the SET and RESET states decreased as the cell size reduced, but it was still more than an order of magnitude even for the smallest cells and could be improved by reductions in the length of the heater (which contributes significantly to the resistance of the cell in the SET state). Perhaps most importantly we found that the RESET current amplitude scaled as the inverse of the heater contact diameter, and ultra-small RESET currents of only 19 μA were needed to amorphize the smallest of cells, such values being comparable to those obtained using much more ‘exotic’ (and very difficult to manufacture) cell formats such as those using CNT electrodes.

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