Development of Electrically Pumped Vertical External Cavity Surface Emitting Lasers (EP-VECSELs)

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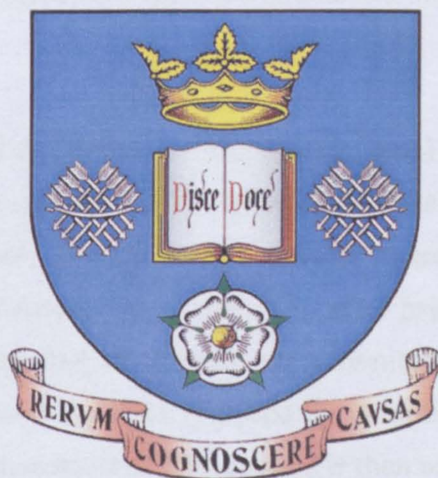

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Abstract

In this thesis design, development and realisation of a substrate emission electrically pumped vertical external cavity surface emitting lasers (EP-VECSELs) emitting in the 980 nm wavelength range is discussed. Chapter 1 provides a literature review of the relevant VCSEL and (OP-VECSEL) technology required for the design of an EP-VECSEL. In chapter 2, different areas of the device design are highlighted, including electrical and optical performance of the distributed Bragg reflectors (DBRs), active region design, device detuning and antireflective coating design.

Chapter 3 provides a description of the method used to fabricate EP-VECSEL devices and focuses on optimisation of different process steps, namely the trench etch profile and depth, as well as the contact metalisation. A method for characterising the detuning of a wafer is also presented. In chapter 4 measurements of fabricated EP-VECSEL are presented, with a method for the characterisation of the EP-VECSEL material by modulating the output coupler mirror reflectivity demonstrated. This method is then used to examine the affect of different substrate dopings on device performance. Data is also presented on beam quality, power scaling and thermal properties.

Chapter 5 investigates methods for improving electrical aspects of device operation, with improved n and p DBR designs proposed. In addition, analysis of SIMS data for an EP-VECSEL and n-DBR are presented, along with an investigation of the top contact geometry. In chapter 6 a discussion of the QW active region is provided, first by analysing the epitaxial material used in chapter 4 and then proposing improvements to the growth process. A comparison of a 3, 6 and 9 QW active region is then presented, where the trade offs in the optimum number of QWs are examined. Finally, this thesis is summarised and a new device design is proposed from the findings.

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J.R. Orchard, D.T.D. Childs, L.C. Lin, D.M. Williams, B.J. Stevens, R.A. Hogg, Trade-offs in the Realization of Electrically Pumped Vertical External Cavity Surface Emitting Lasers, **Journal of Selected Topics in Quantum Electronics**, Vol. 17, 6, pp1745-1752, 2011

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1 Introduction

1.1 Vertical Cavity Surface Emitting Lasers (VCSELs)

Vertical cavity surface emitting lasers (VCSELs) were originally proposed by Kenichi Iga in 1977 [1], with the first realization of a device presented in 1979 using a 1.3 μm GaInAsP/InP active region [2]. In 1986 a low threshold current of 6 mA was achieved using a GaAs based device [3], and a year later in 1987 the first room temperature CW operation was achieved from a metal organic vapour phase epitaxy (MOVPE) grown GaAs device [4]. Then in 1989 a group from AT&T demonstrated a VCSEL with an InGaAs active region with a 0.5 mA threshold current [5]. Since then technological improvements leading to improved device design has led to comparable or better performance of GaAs based devices over that of edge emitters in the lower power regime (~ 1 mW) [6]. As a result VCSELs exhibited the lowest threshold of any type of semiconductor laser [7], until the production of nano-cavity lasers [8] , and have achieved wall-plug efficiencies at high as 57% [3]. Although the main development of devices has come in the 0.8 - 1 μm region, device operation has also been demonstrated at 1.3 μm [9], and 1.55 μm using a wafer fusion technique [10]. Using a GaInAlAs active region, room temperature CW red emission has been achieved [11], with research on blue emitting GaN devices currently underway [12].

The large interest in this type of device has been driven by a large number of desirable device properties listed below:

- Extremely low threshold current as a result of the small active region volume of the device, achieving μA levels
- Single transverse mode operation

- Large relaxation oscillation (RO) frequency due to small active region volume, allowing for high speed modulation of the devices
- High power conversion efficiency allows for reduced heating in densely packed arrays
- Circularly symmetrical, low numerical aperture (NA) output beam, allowing for simple low loss coupling to fibers or optics
- Low chip cost as many devices can be tightly packed onto a single wafer with the ability to probe test devices before they are cut into discrete devices
- Devices can be arranged into densely packed 2D arrays, resulting in very high output powers [1]
- Long device lifetime, in excess of 10^7 hours [7]

Although all of these properties are easily obtainable in the 0.8-1 μm wavelength range, it is a more challenging task outside this range, as the refractive index contrast of the materials available from which to construct distributed Bragg reflector (DBR) mirrors is low making it difficult to achieve the high reflectivity required, whilst maintaining a low resistance. In addition, when the device diameter is increased for achieving high output power the single mode performance is lost.

The epitaxial structure of a VCSEL, shown on the right of *Figure 1.1*, is quite different to that of a Fabry-Perot edge emitting stripe laser, shown on the left of *Figure 1.1*, resulting in a number of physical differences, these are summarized in *Table 1.1* [1]. The most noticeable difference is that the active volume is three orders of magnitude smaller in the case of the VCSEL, and as a result of this a smaller threshold current can be obtained, leading to the ability to achieve a high relaxation frequency and a high power conversion efficiency. The other large difference is that of the reflectivity required for lasing is much greater; this is due to the small gain length product in the VCSEL necessitating a high reflectivity to offset this value.

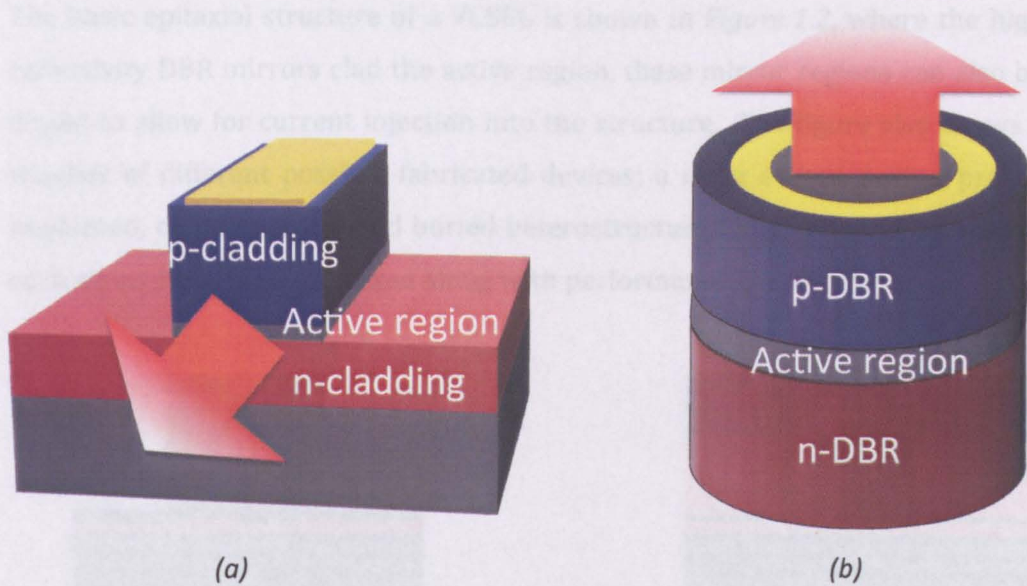

Figure 1.1 (a) Schematic of edge emitting laser (b) Schematic of VCSEL

Parameter	Symbol	Edge emitting laser	VCSEL
Active layer thickness	d	10 – 100 nm	8 – 500 nm
Active layer area	S	3 x 300 μm^2	5 x 5 μm^2
Active volume	V	60 μm^3	0.07 μm^3
Cavity length	L	300 μm	1 μm
Reflectivity	R	0.3	0.99 – 0.999
Optical confinement	Γ	~ 3%	~ 4%
Optical confinement (Transverse)	Γ_T	3 – 5%	50 – 80%
Optical confinement (Longitudinal)	Γ_L	50%	2 x 1% x 3 (3 QWs)
Photon Lifetime	τ_p	~ 1 ps	~ 1 ps
Relaxation frequency	f_r	< 5 GHz	> 10 GHz

Table 1.1 Comparison of edge emitter and VCSEL properties

The basic epitaxial structure of a VCSEL is shown in *Figure 1.2*, where the high reflectivity DBR mirrors clad the active region, these mirror regions can also be doped to allow for current injection into the structure. The figure also shows a number of different possible fabricated devices; a mesa etched device, proton implanted, oxide aperture and buried heterostructure. The technical aspects of each structure will be discussed along with performance characteristics.

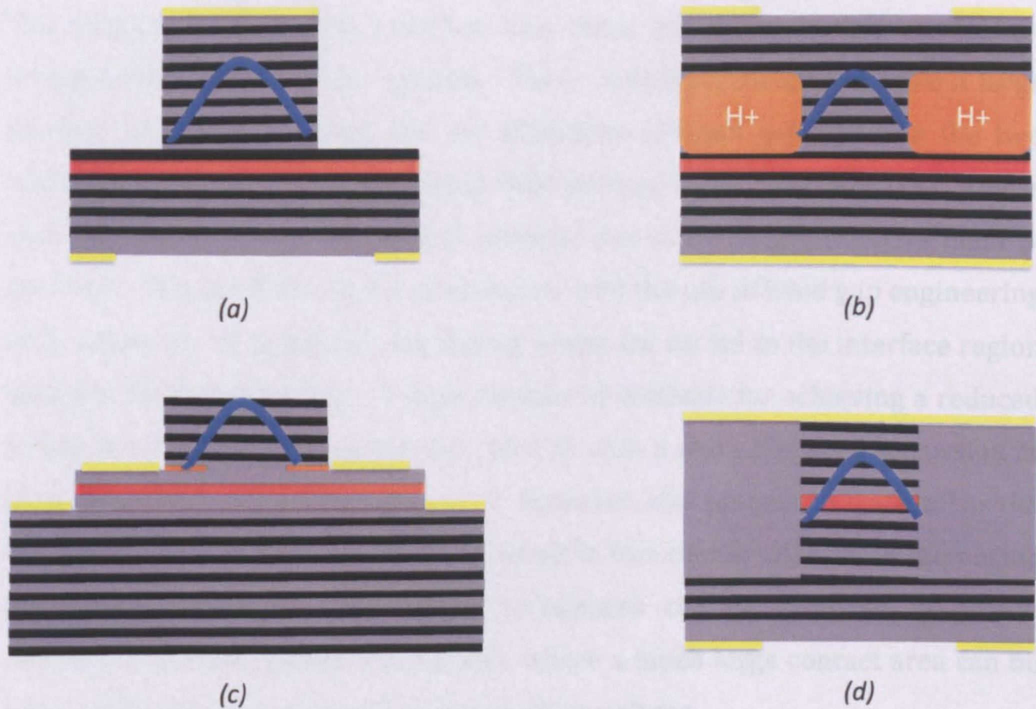

Figure 1.2 Schematic of different VCSEL structures where the blue line shows the optical confinement (a) Mesa etch (b) Proton Implant (c) Intra cavity contacted (d) Buried heterostructure

1.1.1 Etched Mesa Device

Figure 1.2a shows the device structure for an etched mesa VCSEL; in this case a square or round post like structure is formed. The mesa is usually etched to just above the active region to reduce surface recombination of carriers as well as reliability problems. Current is confined by lateral extent of the mesa, but can diffuse laterally in the active region, giving rise to a lateral leakage current, this can become significant in devices below 10 μm in diameter [6]. The device can be designed for either top or substrate emitting geometries, where either the

contact is apertured on the top or the bottom to allow transmission of light, in this case a bottom emitting arrangement is shown. Bottom emission has a number of advantages, the mesa can be gold plated and bonded to a tile to reduce the thermal resistance and parasitic capacitance [13]. However, absorption in the substrate caused by dopant atoms will lead to a reduced power output.

The problem with current injection into these structures is that conduction through the DBR mirror is required. These multilayer structures have a large number of heterointerfaces, and the difference in band gap between the two materials causes the formation of potential barriers at the interfaces [14]. This is exacerbated in the case of p-doped material due to the larger effective mass of the holes. This problem can be ameliorated with the use of band gap engineering [15], where the composition and doping levels are varied in the interface region between the two materials. A large number of methods for achieving a reduced resistance have been demonstrated [16-19], with a more in depth discussion of these solutions presented in chapter 5. However, this presents a trade off as the introduction of doping in the DBR will result in free carrier absorption increasing the device threshold. The lowest resistances can be achieved in proton implanted or oxide aperture structures where a much large contact area can be used, while still having a small, pumped active volume.

A method to circumvent the trade-off is to use intra-cavity contacts as shown in *Figure 1.2c*. These structures bypass the DBRs and inject current straight into the active region. These are most beneficial when used in conjunction with an oxide aperture to maintain good current confinement [20]. In the case of a simple etched mesa structure only a bottom intra-cavity contact is worthwhile [21], with it being required to etch through the active region.

Optical confinement within the mesa etched structure is achieved due to the refractive index difference between the post structure and the surrounding media. As this difference in step index is large (~1.5 - 2 for oxide or nitride coatings) the devices will support a large number of lateral modes. However, as

the sidewall etch profile is not perfectly smooth the higher order modes will suffer greater losses than the fundamental mode, meaning they will be suppressed. As sidewall scattering loss decreases with increasing device diameter, (as the ratio of edge to area decreases) single mode operation is maintained only for device up to 8 μm in diameter [13].

1.1.2 Proton Implanted Device

Figure 1.2b shows a planar proton implanted structure; this is a simple structure to fabricate with only a proton implantation and top and bottom metalisation required. The proton implantation induces damage in the crystal structure, making the implanted region insulating, allowing injected current to only flow in the undamaged region resulting on current confinement. The planar structure results in good thermal resistance as the heat can flow laterally through the implanted region as well as low contact resistance due to the ability to use large area contacts.

Problems with the proton implanted structure arise from the electrical conduction of the DBRs, discussed previously, and the implant depth within the device. In order that the implant does not penetrate and damage the active region the implant must stop a reasonable distance above it, as a result the current spreads and can leak out laterally above the active region. In the case the implant goes through the active region so that the current is effectively confined, the damage induced in the active region will result in large carrier losses as the carrier lifetime will be very short on the edge of the implanted regions. Deep implanted structure can also have problems with reliability. In addition to the electrical problems, the lack of any purposeful refractive index contrast will result in no index guiding within the structure. A weak guiding effect will be produced by the temperature profile across the device, known as thermal lensing [22]. Under CW conditions this is enough for stable operation, but when the device is modulated the lateral mode tends to be dependent on the data pattern used [23].

1.1.3 Oxide Aperture Device

Figure 1.2c shows a double intra-cavity contacted device with a dielectric aperture. In addition, structures in which a dielectric aperture has been used in conjunction with a etch mesa have demonstrated a performance improvement [3]. The insulating oxide layer is formed by steam oxidation of a high Al percentage AlGaAs layer within the structure, where the speed of the oxidation is proportional to the aluminium concentration [24]. The purpose of this dielectric aperture is to confine current within the device, in a similar manner to the etched mesa structure, as the aperture can be placed just above the active region. The aperture produced is superior to that obtained through proton implantation as there is no damage caused in active region material.

One of the most appealing features of the dielectric aperture is that is introduces additional flexibility into the device design allowing current and photon confinement to be achieved, but with independent control of each [6]. This is achieved, as the aperture allows for current injection into a volume smaller than the optical mode width and by placing the aperture at the node standing wave of the electric field it will have a negligible effect on the optical mode [25]. Using the dielectric aperture in conjunction with the double intra-cavity contacts it is possible to keep the device resistance and loss low. However, this design does not scale well to large diameters due to requirement for carriers to diffuse a large lateral distance. The use of dielectric apertures for improved carrier confinement has led to wall plug efficiencies of up to 57% being obtained [3].

1.1.4 Buried Heterostructure Device

A natural progression to the structures described previously is the buried heterostructure shown in *Figure 1.2d.* By surrounding an etched pillar device with a material with lower refractive index and higher band gap, current, carrier and optical confinement would be achieved simultaneously. In addition, large area contacts could be used to reduce contact resistance, lateral heat flow into the regrown material would result in a low thermal resistance and a planar device would allow for easy processing and mounting. However, at the time of

writing very little success in fabricating this type of device has been achieved [26]. This stems from the difficulty to regrow material on deep etched structures containing high percentage Al layers, a suggested method uses a sulfide treatment to passivate the surface [27] but so far the process is limited.

1.2 Optically Pumped Vertical External Cavity Surface Emitting Lasers (OP-VECSELs)

It can be seen from the previous section that semiconductor materials can access a very wide wavelength range, from UV to mid-IR, and can produce compact and efficient devices. For a large number of applications high power single transverse mode behaviour with a circularly symmetrical beam is required for low loss coupling to fibres and free space optics. These two properties can only be achieved simultaneously for output powers of below 1 W in semiconductor devices [28]. Much higher powers can be achieved but only with highly multimode low quality beams.

In the case of edge emitting lasers, small waveguide dimensions are required for single mode operation, but the waveguide aspect ratio results in an asymmetric beam with a large divergence. Scaling the area of the waveguide in order to achieve a higher output power, hundreds of milliwatts can be obtained in single transverse mode operation [29]. By further scaling of the device area, to ridge widths of the order of 100 μm, hundreds of watts of output power can be obtained, but with a poor aspect ratio output beam and multimode behaviour [28]. Several of these devices can then be placed together in a bar to obtain output powers in excess of one hundred watts, but still with multimode behaviour.

By contrast VCSELs, emit perpendicular to the plane of the laser with a circularly symmetrical low divergence beam. Single mode operation can be obtained for devices up to ~ 10 μm in diameter, which produce tens of milliwatts of power. To obtain greater output powers the device diameter must be increased, but this leads to a multimode output, as it is difficult to maintain uniform current

injection over a large area. In a similar manner to making a bar of a number of edge emitting lasers densely packed 2D arrays of VCSEL devices can be used to achieve high output powers.

In summary, VCSELs exhibit good quality, low divergence beams but only with low output powers of tens of milliwatts. While edge emitting lasers can emit several hundred milliwatts but with an elliptical beam profile. Conversely, solid-state lasers have excellent beam quality even at output powers of hundreds of watts [30]. However, these devices are limited to specific wavelengths by ion transition levels. It is therefore desirable to develop compact, efficient, high output power devices with good beam quality that exhibit wavelength selectivity by use of semiconductor band gap engineering.

By extending this concept to semiconductor materials, circular output beams can only be achieved using a VCSEL geometry. While a good quality beam with single transverse mode operation can be maintained with large area devices by the introduction of an external cavity, where different elements control the lasing mode, wavelength and beam diameter. Optical pumping can be used to inject a uniform carrier distribution over a large area. Combining these elements to produce a optically pumped vertical external cavity surface emitting laser.

Some of the first investigations of this concept involved diode pumping a GaAs VCSEL, which produced 10mW of CW power [31], the introduction of an external cavity to this set up yielded a very low power of 20 μW [32]. Using a InGaAs - InP external cavity surface emitting laser cooled to 77 K and pumped with an Nd:YAG laser, 190 mW CW output power was obtained [33]. In a similar manner, 77 K operation of a GaAs based external cavity VCSEL yielded 700 mW CW using a 1.8 W krypton-ion pump laser [34]. Specially designed InGaAs-GaAs edge emitting structures generated 4 W of output power using diode pump lasers [35]. However, the beams produced were not circularly symmetrical. It was not until 1997, when all of these aspects were combined to produced a TEM_{00} CW room temperature output power of 500 mW [36].

1.2.1 OP-VECSEL Design

Figure 1.3a shows the elements and arrangement of an OP-VECSEL device. The semiconductor element consists of a highly reflective DBR mirror with a gain region on top of it, due to the thin gain layers the single pass optical gain will be low. This structure is bonded on a heat sink to remove unwanted thermal energy. The incident pump beam is used to generate a uniform carrier distribution in the active region. The laser cavity is formed by the semiconductor DBR mirror and an output coupler mirror in the external cavity, which defines the transverse laser mode. Due to the low single pass gain the output coupler reflectivity must be kept high and the intracavity losses need to be minimised for efficient operation. By varying the size of pump spot incident on the gain chip, the output power can be scaled, with spot sizes varying from 50 to 500 μm, yielding output powers of between 20 mW and 20 W [28]. The operation of an OP-VECSEL can be thought of as a mode and wavelength converter, with a high power multimode pump beam at a given wavelength being converted to a circularly symmetrical single mode emission at a specifically designed wavelength.

Figure 1.3b shows the band structure of the semiconductor gain chip element of an OP-VECSEL. The right hand region shows the DBR mirror, this is designed for very high reflectivity (~ 99.99 %) and will have a large number of periods. Since the device is not electrically pumped, the DBR interfaces do not need to be graded, as mentioned in the previous section, and no doping is required in the structure. Incident pump photons, which have a higher photon energy than that of the pump absorbing regions (QW barriers), are absorbed, generating carriers that diffuse into the lower energy QW regions, emitting lasing photons at a lower energy. The spatial separation of the gain and absorption regions allows for individual optimisation of each of these regions. The QWs are placed at the antinodes of the standing wave set up in the cavity, in order to enhance the gain of the structure through a method known as resonant periodic gain (RPG) [37], [38], which is discussed further in chapter 2. The thickness of the active region is typically several wavelengths long, containing somewhere between 5 and 15 QWs [39]. At the top of the structure is a surface barrier, which has a higher

band gap in order to prevent non-radiative recombination at the surface that leads to depleted gain and results in reduced power conversion efficiency and device heating.

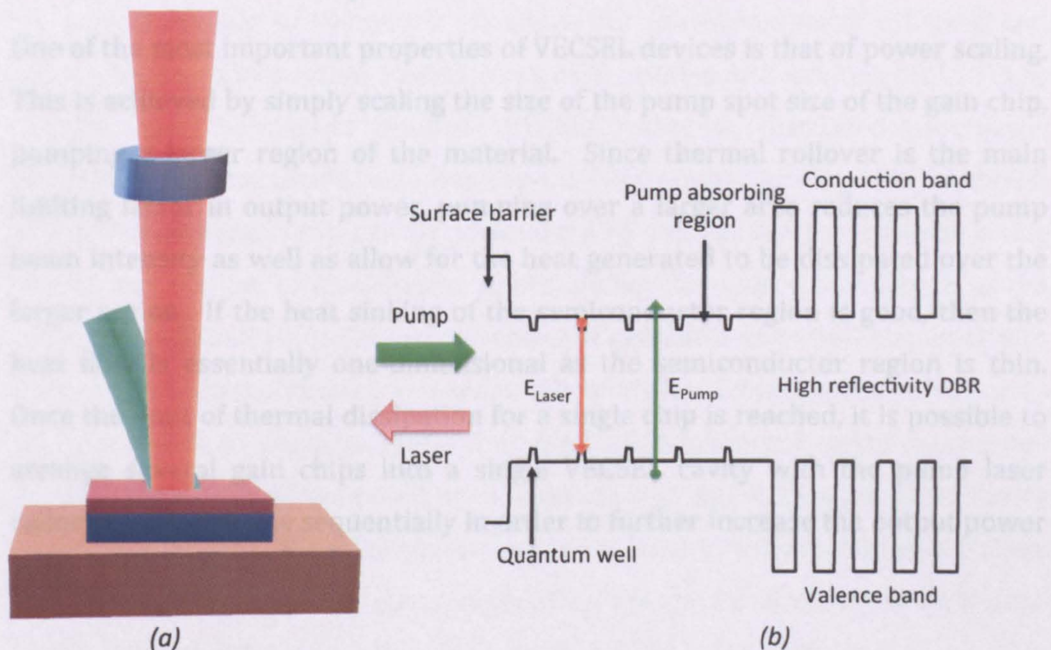

Figure 1.3 (a) Illustration of OP-VECSEL device (b) Schematic of OP-VECSEL epitaxial structure

The energy of the pump photons is greater than the energy of the emitted photons, this difference is known as the quantum defect and is a major factor in overall device efficiency. Along with non-radiative recombination processes these cause heating within the device that must be dissipated into the heat sink. Good heat sinking is essential, as increased active region temperature allows thermal carrier escape from the QWs, depleting gain and leading to thermal rollover. Thermal rollover is the dominant factor in limiting output power within a VECSEL device [40]. A reduction of the quantum defect will reduce the amount of heat generated, but the reduction in barrier height will also reduce the carrier confinement energy making it easier for carriers to escape thermally. Optimisation of this parameter is necessary to achieve efficient high power operation. Another method of improving efficiency, is to reduce the quantum defect by using in well pumping instead [41]. It is important to note, that unlike

solid-state lasers the broad wavelength absorption of semiconductor materials allows any pump wavelength below that of the absorption region to be used.

1.2.2 OP-VECSEL Properties

One of the most important properties of VECSEL devices is that of power scaling. This is achieved by simply scaling the size of the pump spot size of the gain chip, pumping a larger region of the material. Since thermal rollover is the main limiting factor in output power, pumping over a larger area reduces the pump beam intensity as well as allow for the heat generated to be dissipated over the larger region. If the heat sinking of the semiconductor region is good, then the heat flow is essentially one-dimensional as the semiconductor region is thin. Once the limit of thermal dissipation for a single chip is reached, it is possible to arrange several gain chips into a single VECSEL cavity with the pump laser reflecting off each one sequentially in order to further increase the output power [42].

Another important property is beam quality, M^2, which is the measure of how much the beam diverges angularly in the transverse and longitudinal directions compared with a single transverse mode diffraction limited beam with an $M^2 = 1$. The most important aspect in obtaining good beam quality, are the external cavity optics, these allow the pump spot size and the fundamental mode size of the laser to be matched. If the pump spot is too small in comparison to the mode size, the laser threshold will be increased due to additional loss of unpumped regions that are coupled to the mode. If the pump spot is too large, higher order transverse modes will be excited, resulting in multimode operation and degradation in the beam quality. An optimised spot size results in a higher gain in the fundamental mode compared to higher order modes, leading to stable fundamental mode operation. The large pump spot and laser beam sizes, the order of tens to hundreds of microns allows to ease of device alignment, resulting in a very mechanically stable cavity and hence a stable fundamental mode. In addition, for a device with good heat sinking negligible thermal lensing has been observed [42]. A thermal lens occurs when the thermal profile within

the chip causes changes in refractive index, resulting in an additional divergence in the beam.

An attractive advantage of the VECSEL device is its external cavity, which allows for a great amount of versatility. It allows for the formation of different and more complex cavity arrangements, such as V-cavities or Z-cavities [43]. These can be used to cascade multiple VECSEL chips as discussed previously. Intracavity spectral filters, including etalons [44], volume gratings [45] and high reflectivity gratings [46], can be introduced to control the longitudinal lasing modes and the use of birefringent filters allows the output wavelength of the device to be tuned [47]. The introduction of saturable absorbed elements into the cavity allows the VECSEL to be passively mode locked producing pulses up to sub picosecond in duration [43]. The length of the external cavity determines the repetition rate of the pulse, with rates as high as 50 GHz for short cavity lengths [48]. Optic elements placed in the external cavity can control the size and hence intensity of the spots incident on the gain and absorber materials, which is required to achieve mode locking [49]. Since the output coupler transmission from a VECSEL is low, ~ 1-5%, there will be a much higher intracavity power, of the order of 10 - 100 times greater than the emitted power. Coupling this high intracavity power with the high beam quality allows for very efficient non-linear processes to occur, by inserting non-linear media such as periodically poled crystals in the cavity. Non-linear processes, such as second harmonic generation [47] allow for wavelengths normally difficult to access with semiconductors to be obtained.

1.3 Electrically Pumped VECSELs (EP-VECSELs)

The next progression from OP-VECSELs is to develop electrically driven devices, by removing the pump source and optics it is possible to produce a highly compact low cost device. The introduction of electrical pumping into a VECSEL structure results in a number of additional design challenges, making the structure much more complex. In order to produce a state of the art device, ideas developed in VCSEL research can be combined with OP-VECSEL work. Up

to this point very little work on this topic has been published. A GaAs based device with a micro mirror output coupler has demonstrated 10 mW CW, with an M^2 of 1.2 for a 28 μm device diameter [50]. An InP based device has also been demonstrated, emitting 0.5 mW CW from a 20 μm device [51]. Moreover, simulation work on the design of GaAs based EP-VECSELs for mode-locking applications has been produced [52].

Much of the development work for EP-VECSEL operating at 980 nm was carried out by a company called Novalux, who were able to demonstrate single mode TEM_{00} operation with an output power of 500 mW from a 150 μm device [53]. In the process of developing these devices they spent a significant amount of investment capital and eventually went into administration. However, much of this work is proprietary, so little is know about the key design features and trade-offs required in operation. More recently, powers in excess of 100 mW have been demonstrated, but with low beam quality [54], [55]. By contrast, another research group has demonstrated TEM_{00} operation with an M^2=1.2, but with an output power of 10 mW [56]. In addition passive mode-locking of a Novalux device has been presented, achieving ~15 ps pulses at a 15 GHz repetition rate [57].

The main design challenge in the realization of EP-VECSEL device is producing a low resistance and low loss structure simultaneously, where device self-heating is the major limiting factor in output power. The requirement for high reflectivity DBR mirrors means that there will be a large number of heterointerface barriers, leading to a high resistance in the structure. This can be ameliorated by grading the interface between the two layers and adding doping to the structure, as discussed in the VCSEL section. An increased doping level leads to larger levels of free carrier absorption, resulting in higher threshold current densities. It can therefore be seen that a trade off between reduced resistance and increased loss is present.

Another significant factor in the design is current spreading in large diameter devices (100 μm and greater). An aperture in the top contact is required to

couple light out of the device, of the order of the device diameter, this means that in order for a Gaussian carrier distribution to be present in the active region the carriers must diffuse laterally over a distance half that of the aperture width. To aid this process a thick, doped current spreading region can be added to the structure. However, as a result of the large thickness and doping concentration, it will contribute a large loss to the device. By introducing an additional internal DBR, the electric field intensity in the current spreading region can be reduced, mitigating the loss. This DBR provides the added benefit of enhancing the electric field in the active region, allowing for an up to two-fold gain enhancement with careful active region design. However, this additional DBR lessens the influence of the external cavity mirror on the overall device, hence careful design of this additional element is required.

Taking all these design aspects into consideration, it is possible to create an illustration of the device structure. *Figure 1.4* shows a representation of on EP-VECSEL device, at the bottom of the device is the high reflectivity p-DBR (>99%), this region has been etched to provide carrier confinement and has a large area contact for low resistance. Above this is the active region, where the gain for the device is provided. On top of this is the intermediate lower reflectivity n-DBR (70-90%), followed by the thick current spreading layer. The current spreading layer can either be formed by epitaxial growth of material or by using the substrate and thinning it to the desired thickness. Above this layer is the n-type top contact, which has an aperture to couple light out of the device, deposited over the aperture region is a dielectric anti reflective coating.

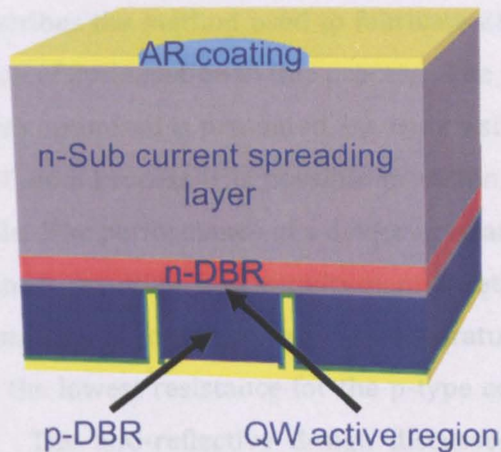

Figure 4 Schematic of EP-VECSEL device structure

1.4 Thesis Outline

This thesis will discuss the design and development of EP-VECSELs for use in mode-locking applications, where a substrate emission geometry with a QW active region is considered. Chapter 2 will discuss the design of DBRs for achieving high reflectivity, where a high index contrast between the two materials used is desirable. A brief mention of the electrical design of the DBRs will also be given, and using the results from the reflectivity modelling a number of p-DBRs were grown and characterised. Design of the active region will then be examined, where it will be demonstrated how to achieve an up to two fold gain enhancement by careful design of the active region. This will be followed by a discussion on strain compensation of QWs within the active region, required for low defect density growth. Then modelling on the affect of DBR reflectivity and growth thickness variation on the cavity resonance will be presented, where transmission from the cavity is highest when the reflectivity of both DBRs is equal and DBR thickness variations have a stronger influence on the cavity resonance wavelength than cavity thickness variations. This will then be linked to a discussion of detuning on device performance, where an offset in the spectral position of the QW emission relative to the cavity spectral position can result in increased output power. Finally, the chapter will investigate the performance of different dielectric anti-reflective coating designs, where 100% transmission can be achieve from structures greater than 4 layers.

Chapter 3 describes the method used to fabricate EP-VECSEL devices and looks at various areas of optimisation in this process. The process by which the trench etch profile was optimised is presented, by using a silicon dioxide hard mask and an $Ar:SiCl_4$ ICP etch process it is possible to obtain a deep etch with a smooth sidewall profile. The performance of a device in relation to the trench etch depth is also examined, resulting in a requirement to etch to just above the active region. Optimisation of contact annealing temperatures will be discussed, where 360 °C yields the lowest resistance for the p-type contact and 400 °C for the n-type contact. The anti-reflective design discussed in chapter 2 will be re-evaluated after growth of the design was carried out, with the single layer design being the best option due to its wavelength insensitivity. Finally a partially destructive method for the characterisation of the detuning across a wafer will be described.

Chapter 4 presents measurements taken from fabricated EP-VECSEL devices. Firstly a method for characterising the gain in an EP-VECSEL is presented, whereby the output coupler mirror reflectivity is changed, modulating the mirror loss, the corresponding threshold current can be measured and used to form a gain-threshold current relationship. Using the described method the affect of different n-doped substrate dopings on device performance will be examined, with the $4x10^{17}$ cm^{-3} substrate exhibiting lower loss and only a negligible difference in electrical performance compared to $1x10^{18}$ cm^{-3} doped substrate. Measurements of M^2 values from devices will be presented, with a value of 1.5 achieved from a 150 µm device at low output power. An investigation into the power scaling properties of the $4x10^{17}$ cm^{-3} doped substrate devices will then be carried out, where a non-uniform carrier distribution is present for devices of 100 µm and greater, leading to non-linear power scaling at higher device diameters. This notwithstanding output powers of 130 mW CW for a 100 µm device at a heatsink temperature of 0 °C have been achieved.

Chapter 5 provides a discussion of optimising electrical performance in the device. First, the affects of different grading systems in the p-DBR will be

examined, with a linear grading scheme exhibiting the lowest resistance. Then a simple model for calculating free carrier absorption loss in the DBR will be presented, using this the trade-off between loss and doping for lower resistance will be examined. Next, the same analysis will be presented for a n-DBR, with an single 30% AlGaAs step resulting in the lowest resistance in this case. This is supported by measurements of several grown designs. Subsequently, secondary ion mass spectrometry (SIMS) data will be presented and analysed for an n-DBR and an EP-VECSEL structure, with a significant variation in the doping incorporation of the p-DBR and carbon auto-doping of the n-DBR. Finally, the affect of the contact geometry and current spreading layer thickness on the carrier distribution in the device will be examined, with a reduced ring contact diameter resulting in a thinner current spreading layer being required. Furthermore, for a fixed ring contact diameter of 20 μm the required current spreading layer thickness for a uniform carrier distribution is 1.25 times than of the radius.

Chapter 6 presents a discussion of the performance of the quantum well (QW) active region, with an aim to optimise its design. Initially, a method for analysing the material gain of epitaxially grown material will be presented, and the material used in chapter 4 will be analysed. Transmission electron microscopy (TEM) analysis and low temperature linewidth measurements will also be presented, with the measurements indicating broadened QW emission due to poor interface quality in the QWs. As a result of this, a method for improving the interface quality will be discussed and material grown using this method will be similarly characterised and compared to the roughened material. With the flattened interface material exhibiting higher efficiency, a smaller low temperature linewidth and improved gain. Finally, an analysis of material containing 3, 6 and 9 QWs will be presented, with the 3 QW structure providing the best overall performance.

Lastly a summary of the work in this thesis will be presented, where an improved epitaxial designs will be presented with each section of the design optimised with regard to analyses presented in the various chapters of this work.

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2 Device Design

2.1 Introduction

In this chapter the areas of design critical for device operation will be discussed. *Figure 2.1* shows the structure of a fully fabricated EP-VECSEL device without the external cavity, where the important areas of the design are labelled. The fabrication of the device itself and the key elements and optimisations in the fabrication process are covered in chapter 3. The first part of this chapter will examine the design of DBRs; this is critical to device performance as high optical performance (low loss, high reflectivity) as well as high electrical performance (low resistance) is required. This can be achieved by the introduction of a layer with an intermediate composition in between the two DBR layers, where a thin layer has less effect of the optical properties of the DBR.

This is followed by the active region design, where spatial positioning of gain can lead to a factor two gain enhancement. The affect of the device design and layer thickness on the cavity resonance of the device is then discussed, the number of DBRs on each side of the cavity affecting the strength of the resonance and the thickness of the layers in the device affecting the resonance spectral position. This links in with device detuning, where a separation in the cavity resonance position and the gain peak is introduced in order to extend the point at which thermal roll over occurs, which is the major limit on output power in the device. A further discussion of quantum well performance is provided in chapter 6.

Finally a discussion of anti-reflective coatings will be presented, which are necessary to reduce the losses associated with coupling to the external cavity of the device. By adding additional layers it is possible to achieve 100 % transmission from the structure at the designed wavelength. An examination of current spreading layers and their properties is presented later in chapter 5.

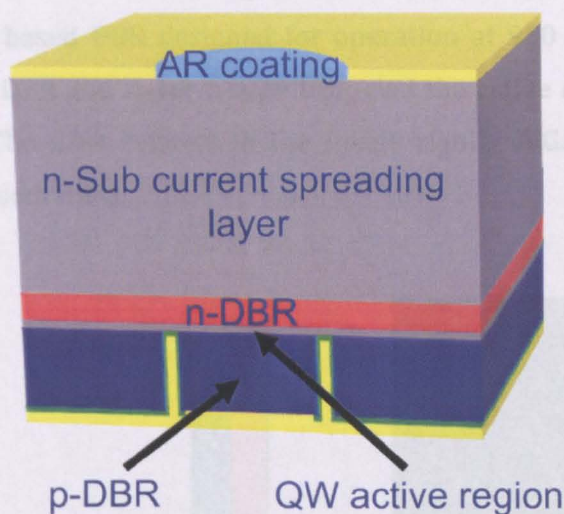

Figure 2.1 Schematic of EP-VECSEL device structure

2.2 Optical Properties of DBRs

Distributed Bragg reflectors or DBRs are mirrors comprised of a number of quarter wave thick layers of two alternating materials with different refractive indices. They can be used to give very high reflectivity (R~1) and can provide this high reflectivity over a given wavelength range, known as a stopband. *Figure 2.2a* illustrates the structure of a DBR, where each of the layer thicknesses is defined by

$$t_{DBR} = \frac{\lambda}{4n} \qquad (2.1)$$

where λ is the free space wavelength to be reflected and *n* is the refractive index of the layer of material. The blue and red layers denote materials of different refractive indices defined as n_H and n_L. The DBR is comprised of *m* periods of these two materials, where *m* can be any positive integer. It is also possible for *m* to take on values of multiples of ½ *i.e.* the DBR can finish on the same material it started with. The arrows illustrate that while only a small amount of light is reflected at each interface once the number of interfaces increases the reflectivity will increase.

Figure 2.2b shows a scanning electron microscope (SEM) image of an AlGaAs/GaAs based DBR designed for operation at 980 nm. In the image the upper p-type DBR and lower n-type DBR clad the active region in the middle of the image. The dark regions in the image signify AlGaAs, whereas the grey regions represent GaAs.

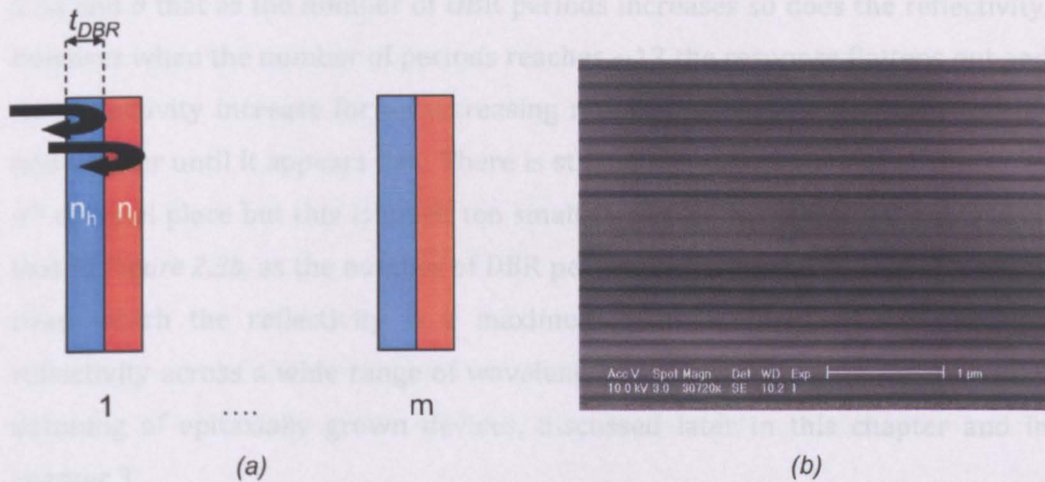

Figure 2.2 (a) Schematic of DBR layer construction (b) SEM image of EP-VECSEL with DBRs visible either side of the cavity

There are several possible methods that can be used to calculate the reflectivity of a multi-layer stack [1-3]. The method used in this thesis was a transmission matrix approach; this was implemented using CAMFR software [4], a fully vectorial Maxwell solver. Using this software, DBRs were described by entering the thickness and the refractive index of each of the layers in the DBR. The reflectivity could then be calculated over a user defined wavelength range and angle of incidence. In this case due to the vertical nature of the device only 0° was used.

The results of the simulation for an $Al_{0.9}Ga_{0.1}As$/GaAs based DBR designed for operation at 980 nm are shown in *Figure 2.3.* $Al_{0.9}Ga_{0.1}As$ was used in order to achieve a high index contrast as well as provide good thermal conductivity [5], while not being as susceptible to degradation as AlAs. The refractive indices used were 3.02 and 3.52 for the $Al_{0.9}Ga_{0.1}As$ and GaAs layers respectively and the layer thicknesses were calculated using equation *(2.1)*. *Figure 2.3a* plots the

maximum reflectivity (R_{DBR}) as a function of the number of DBR periods (m) on the left axis, as well as the full width half maximum of the stop band (FWHM) as a function of the number of DBR pairs (m) on the right axis. This information was derived from *Figure 2.3b*, which plots the reflectivity as a function of wavelength for a selection of different numbers of DBR period. It can be seen from *Figures 2.3a* and *b* that as the number of DBR periods increases so does the reflectivity, however when the number of periods reaches ~12 the response flattens out and the reflectivity increase for an increasing number of periods becomes smaller and smaller until it appears flat. There is still an increase occurring at the 3rd or 4th decimal place but this is much too small to see on the graph. It is also seen that in *Figure 2.3b*, as the number of DBR periods increase the wavelength range over, which the reflectivity is a maximum also increases. Having a high reflectivity across a wide range of wavelengths is important with regard to the detuning of epitaxially grown devices, discussed later in this chapter and in chapter 3.

The peak reflectivity of a DBR may also be calculated more simply by using the equation [3]

$$R_{DBR} = \left(\frac{1-\left({n_H}/{n_l}\right)^{2m}}{1+\left({n_H}/{n_l}\right)^{2m}} \right)^2 \tag{2.2}$$

This is referred to in *Figure 2.3a* as the simple model and is plotted along with the results obtained using CAMFR, labelled as Maxwell model. At a low number of periods there is a disparity in the values calculated, with the simple model giving an under estimation in each case. However, as a higher number of periods are approached the difference decreases before reaching a convergence, indicating equation *(2.2)* is useful for calculating the values for high reflectivity stacks. Another useful element highlighted by equation *(2.2)* that cannot be deduced from *Figure 2.3a* is that a greater reflectivity can be achieved by increasing the refractive index contrast between the two layers that make up the DBR.

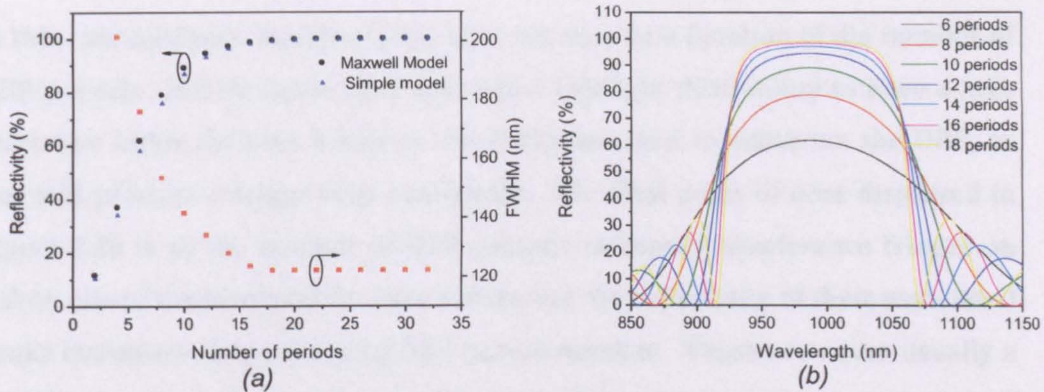

Figure 2.3 (a) Reflectivity and stopband width as a function of the number of DBR periods (b) Reflectivity spectrums for different numbers of DBR periods

At longer wavelengths the use of DBRs for both optical and electrical functionality becomes more complicated, due to reduction in the refractive index contrast, requiring for a greater number of DBRs to be used. This is also the case in InP based devices, hence realization of devices emitting at 1550 nm is challenging [6]. A method to counteract this problem is to use dielectric DBRs [7], or other materials with a large refractive index contrast [3] so that only a few periods are required, but since these materials do not conduct current devices will have to be intra-cavity contacted, as shown in chapter 1.

The other element illustrated in *Figure 2.3a* as well as *Figure 2.3b* is that as the number of DBR periods increases the FWHM or stopband bandwidth decreases in a mirror image of the reflectivity. Although it is desirable to have as large a stop bandwidth as possible, the 120 nm achievable from the model for a high reflectivity is still desirable. In a similar manner to equation *(2.2)* there is also a simple equation to calculate the stop bandwidth of a DBR [3] given by

$$\Delta\lambda_{stopband} = \frac{2\lambda\Delta n}{\pi n_{eff}} \quad (2.3)$$

where

$$\Delta n = n_H - n_L \qquad n_{eff} = 2\left(\frac{1}{n_H} + \frac{1}{n_L}\right)^{-1} \quad (2.4\ a\ \&\ b)$$

In this case however, equation *(2.3)* does not vary as a function of the number of DBR periods. But equation *(2.3)* does again highlight desirability to have a high refractive index contrast between the materials used to construct the DBR, as this will produce a larger stop bandwidth. The final point of note displayed in *Figure 2.3b* is as the number of DBR periods increases interference fringes on either side of the stopband become visible and the reflectivity of their associated peaks increases with increasing DBR period number. These are never usually a problem because their spectral position is far from the operating wavelength of the laser.

2.3 Electrical Properties of DBRs

As well as the optical properties described above, considerations have to be made for the electrical properties of the DBR structure, as current is required to flow through these regions in order to reach the active region. It is here where the negative aspects of DBR become apparent. As there is a requirement for high reflectivity (R~100%) and the refractive index contrast in the AlGaAs/GaAs material system at 980 nm is ~ Δn=0.54 means that a large number of DBR periods are required (m>30).

As the alternating layers used in the DBR have different bandgaps at each interface between the two materials, there will be a discontinuity in the band structure, which is brought about by the requirement to maintain a constant Fermi level across the bands. This discontinuity takes the form of a potential spike in the band, impeding the flow of carriers, requiring them to gain enough energy to get over the spike and contribute to conduction. Since the number of DBR pairs required for high reflectivity is in excess of 30, the large number of potential spikes encountered by carriers will cause the DBR structure to be highly resistive. High resistance devices will lead to a large amount of heat being generated and hence poor device performance. Doping can be used to reduce the resistance but this will result in increased optical loss in the structure and hence is undesirable.

A large amount of research effort has been put in over the years to solve the problem, with a large number of different methods being suggested [8-11]. The most widespread and successful of these methods is to introduce a thin (10-30 nm) layer of different material composition in between the two layers to reduce the potential spike. This method is illustrated in *Figure 2.4a* and *Figure 2.4b*, where *Figure 2.4a* shows the band structure for an abrupt interface (blue), a single intermediate step (black) and a linear graded interface (red). The band structure shown is for a p-doped DBR. Due to the low mobility of holes and the greater free carrier absorption loss [12] in p-type structures, much more attention is required in their design. *Figure 2.4b* shows the AlGaAs alloy composition for an abrupt interface (blue), a single intermediate step (black) and a linear graded interface (red), where d_{grade} is the thickness of the grading layer. In the case of the linear grade the aluminium composition of the layer is continuously changed from the starting composition to the end composition.

It can be seen in *Figure 2.4a* that the introduction of the grading layer greatly reduces the size of the potential spike, hence reducing the resistance. In the case of the single intermediate step (black) the band structure is broken up into two smaller potential spikes, whereas, for the linear graded structure, the potential spike is reduced further still and band is smooth and continuous between the two layers of the DBR. It is clear from *Figure 2.4a* that the addition of linear grading will significantly improve device performance, however, achieving such smooth variation in composition across such a small thickness is quite technically challenging. A more in depth discussion of the electrical aspects of DBR designs and their optimisations for both p and n doped structures is given in chapter 5.

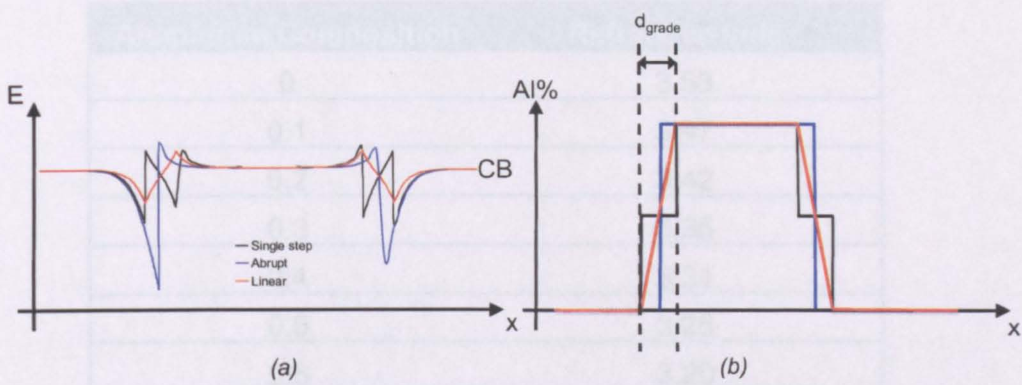

Figure 2.4 (a) Diagram of the conduction band energy for different types of DBR interface (b) Aluminium composition for different types of DBR interface

2.4 DBR Reflectivity Modelling

As discussed in the previous section, it is of great benefit to introduce a grading layer in-between the two layers in each DBR period to improve electrical performance. However, it is not know how these additional layers will affect the optical properties of the DBR. This section investigates the optical behaviour of the DBRs as a consequence of the introduction of grading layers with differing properties.

As discussed previously, these structures were modelled using CAMFR, where the refractive index and thickness of each layer is required for the simulation. For each simulation the DBR period was kept constant by reducing the thickness of the AlGaAs and GaAs layers such that

$$81.1\,nm - d_{grade} = d_{AlGaAs} \quad (2.5a)$$

$$69.6\,nm - d_{grade} = d_{GaAs} \quad (2.5b)$$

The number of periods was kept constant at m = 20 for all the simulations. The refractive indices for varying compositions of $Al_xGa_{1-x}As$ are given in *Table 2.1* below [13].

Aluminium Composition	Refractive Index
0	3.53
0.1	3.47
0.2	3.42
0.3	3.36
0.4	3.31
0.5	3.25
0.6	3.20
0.7	3.14
0.8	3.08
0.9	3.02
1	2.97

Table 2.1 Value of refractive index for different aluminium compositions [13]

Figure 2.5a shows the reflectivity as a function of wavelength for a single $Al_{0.5}Ga_{0.5}As$ intermediate step of varying thickness in an $Al_{0.9}Ga_{0.1}As$/GaAs DBR structure. *Figure 2.5b* plots the peak reflectivity and the stopband FWHM, derived from *Figure 2.5a*, as a function of the interface layer thickness (d_{grade}). In a similar manner *Figure 2.5c* plots the reflectivity as a function of wavelength for a single $Al_{0.2}Ga_{0.8}As$ intermediate step of varying thickness in the same $Al_{0.9}Ga_{0.1}As$/GaAs DBR structure. Likewise, *Figure 2.5d* shows the peak reflectivity and stopband FWHM as a function of the intermediate layer thickness (d_{grade}).

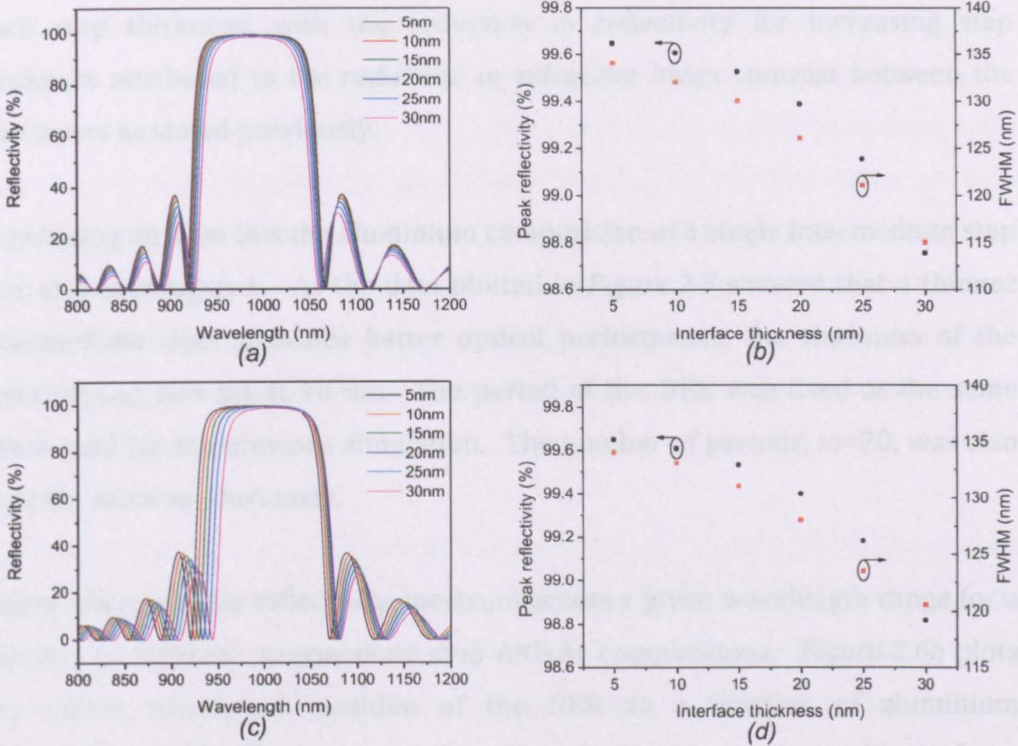

Figure 2.5 (a) Reflectivity spectrum for different thicknesses of $Al_{0.5}Ga_{0.5}As$ grading layer (b) Peak reflectivity and stopband width for different thicknesses of $Al_{0.5}Ga_{0.5}As$ grading layer (c) Reflectivity spectrum for different thicknesses of $Al_{0.2}Ga_{0.8}As$ grading layer (d) Peak reflectivity and stopband width for different thicknesses of $Al_{0.2}Ga_{0.8}As$ grading layer

It can be seen in all parts of *Figure 2.5* that as the intermediate layer thickness (d_{grade}) increases the stopband FWHM of the DBR decreases, this is caused by the reduction of the refractive index contrast that results from the thicker intermediate layer being more prominent within the structure. It is also worth noting that there are some interesting differences in how the stopband FWHM varies with the two different aluminium compositions. For the $Al_{0.5}Ga_{0.5}As$ step shown in *Figure 2.5a,* the FWHM decreases symmetrically about the centre, whereas the $Al_{0.2}Ga_{0.8}As$ step shown in *Figure 2.5c* is fixed about its right hand side and the lower wavelength end of the spectrum shifts up to a higher wavelength, reducing the FWHM. Also if *Figure 2.5b* and *Figure 2.5d* are compared, although the stopband FWHM is the same (134 nm) for a 5 nm step the values are different for a 30 nm intermediate step, 115 nm and 120.5 nm for $Al_{0.5}Ga_{0.5}As$ and $Al_{0.2}Ga_{0.8}As$ step compositions respectively. However, the peak

reflectivity for each of the two intermediate step compositions is identical for each step thickness, with the reduction in reflectivity for increasing step thickness attributed to the reduction in refractive index contrast between the two layers as stated previously.

Continuing on from this the aluminium composition of a single intermediate step was also investigated. As the data plotted in *Figure 2.5* showed that a thinner intermediate layer provides better optical performance, the thickness of the layer (d_{grade}) was set at 10 nm. The period of the DBR was fixed at the same value used for the previous simulation. The number of periods, m=20, was also kept the same as previously.

Figure 2.6a plots the reflectivity spectrum across a given wavelength range for a number of different intermediate step AlGaAs compositions. *Figure 2.6b* plots the centre wavelength position of the DBR as a function of aluminium composition. The figures show that, as the aluminium composition of the intermediate step increases, the centre wavelength of the DBR blue shifts to a lower wavelength. This shift behaves in a linear fashion across all aluminium compositions at a rate of 0.224 nm/Al%. It is also important to note that in *Figure 2.6a* the stopband FWHM remains constant for each aluminium composition and it is only the centre position that shifts, as described above.

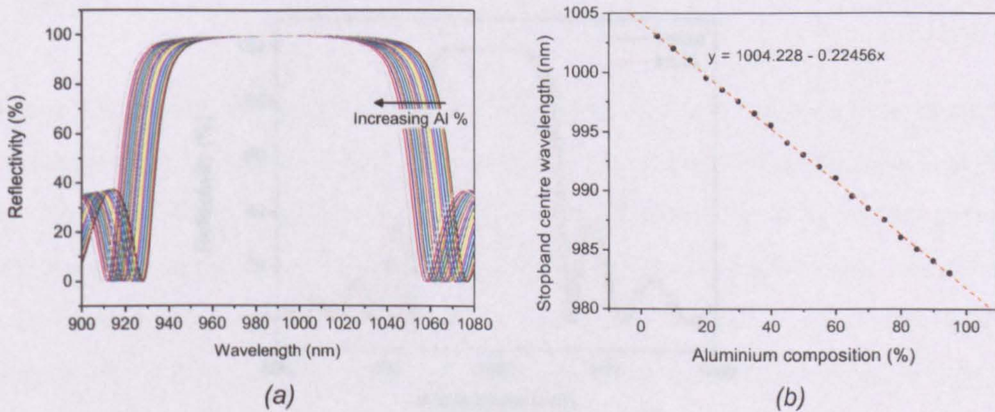

Figure 2.6 (a) Reflectivity spectrum for different aluminium compositions (b) Centre stopband spectral position as a function of aluminium composition in the interface layer

Combining all this information together, only a thin intermediate layer (d_{grade}) is required in order to achieve high optical performance. Any aluminium composition can be used and the DBR period can be adjusted so that the correct centre wavelength is achieved. In section 2.3 it was shown that linear grading could significantly improve DBR electrical properties, to investigate the optical properties, a linear graded structure was simulated. Along with a linear graded structure, some literature [14] suggested that a monolayer super lattice (MLSL) intermediate layer would also provide improved electrical performance, and so it was also simulated optically.

Using the knowledge gained from the earlier simulations, the grading layer thickness (d_{grade}) was set to 10 nm in each case, as well as the same constant period and number of periods used in the previous simulations. The grading layer for the MLSL structure was made up from 2 nm AlAs followed by 2 nm GaAs, then 4 nm AlAs and 2 nm GaAs. This structure was mirrored on the other side of the DBR layer. *Figure 2.7* plots the reflectivity spectrum for the linear grade and MLSL lattice structures described above. The shift between the two spectrums that can be seen in the figure is attributed to the different aluminium compositions present in their grading layers. Their performance compared to that of an $Al_{0.5}Ga_{0.5}As$ single step of the same thickness (10 nm) is shown in *Table 2.2*.

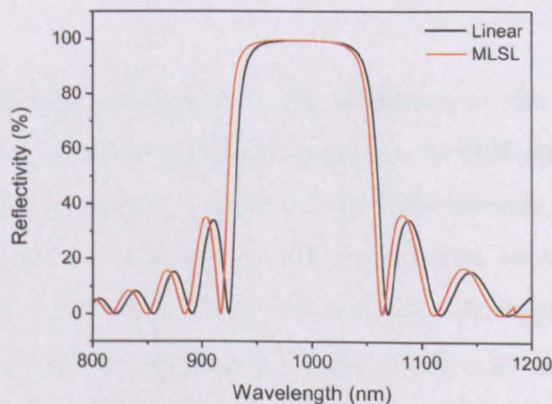

Figure 2.7 Reflectivity spectrum from linear and monolayer superlattice DBR gradings

The $Al_{0.5}Ga_{0.5}As$ single step has the highest value of reflectivity and stopband FWHM, as it maintains the highest index contrast through the DBR layers. The MLSL exhibits the next best performance in both areas, with the linear grade offering the lowest performance of the three. However, the difference in performance of the three structures is very minimal, with all three offering good overall performance. In summary, only the grading layer thickness is critical to DBR optical performance, with a thinner layer allowing for a greater index contrast between the two DBR layers. Hence the electrical performance of the structure is more critical.

	Peak Reflectivity (%)	FWHM (nm)
Single $Al_{0.5}Ga_{0.5}As$ step	99.6	132
MLSL	99.58	130
Linear grade	99.46	129

Table 2.2 Peak reflectivity and stopband width for different DBR grading schemes

2.5 p-DBR Characterisation

In order understand the optical and electrical performance of MOVPE grown p-DBRs it was necessary to have some designs grown. As a result of the modelling carried out in the previous sections, four different p-DBR designs were generated.

Figure 2.8 shows the composition and thickness of the intermediate grading layer as well as the average doping throughout the DBR structure for each of the four designs. Each design consisted of 20 DBR periods, with a design period thickness the same as given above. All the samples were grown on heavily p-doped substrates, with carbon used as a dopant throughout the structure and capped with a 200 nm p+ doped GaAs layer to allow for the formation of a good electrical contact. Design A has a single $Al_{0.47}Ga_{0.53}As$ intermediate step of thickness 25 nm and an average sample doping of 4×10^{18} cm^{-3}. Design B has a 10

nm MLSL graded interface of the same design and composition as described in the previous section and an average sample doping of 4x10^{18} cm^{-3}. Design C is similar to design A, but has a reduced intermediate step layer thickness of 10 nm, whereas design D is the same as design C but with the average doping decreased to 2x10^{18} cm^{-3}. The term average doping has been used, as the dopant incorporation in the different materials is different, as the gas flows were not calibrated to compensate for this effect, discussed further in chapter 5. In addition a linear graded structure was not proposed, as it would have been very difficult to achieve on the MOVPE reactor used for the epitaxy. The reason for this was that the aluminium source had an additional converter to reduce oxygen contamination and this introduced a significant lag in being able to provide reagents to the chamber when required.

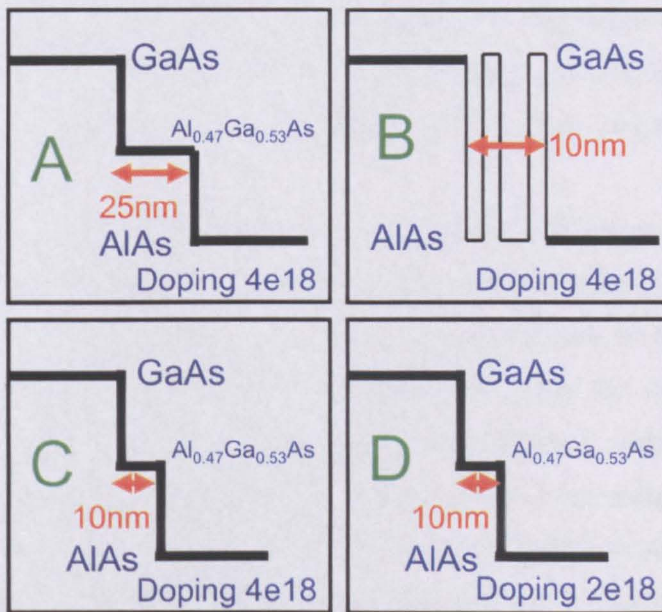

Figure 2.8 Schematic of different p-DBR grading designs (a) 25 nm $Al_{0.47}Ga_{0.53}As$ single step (b) 10 nm monolayer superlattice (c) 10 nm $Al_{0.47}Ga_{0.53}As$ single step (d) 10 nm $Al_{0.47}Ga_{0.53}As$ single step with half the doping

The four designs shown in *Figure 2.8* were fabricated into mesa diodes in order to test the electrical resistance of each design. This was done by firstly photolithographically patterning each wafer with mesas of varying diameters. The photoresist was then used as a mask to dry etch each of the samples using

$SiCl_4$ in an inductively coupled plasma etcher (ICP). It was important that the mesa was etched all the way through the DBR into the substrate, in order to measure the true DBR resistance. Au/Zn/Au ohmic contacts were then deposited on top of the mesas as well as on the backside of the wafer, the samples were then annealed at 360 °C in a rapid thermal annealer (RTA).

The resistance of each of the samples was measured using a Keithly 4200 semiconductor parameter analyser unit. This unit allowed for high precision current injection and voltage measurement of the samples. Each sample was placed on a copper block to contact the backside of the wafer; the copper block was then contacted with a probe. A probe was then used to contact mesas of varying diameters on the top of each sample and IV measurements were taken. A number of mesas for each different size were measured and then averaged to give the final resistance value. In addition, both probes were contacted on the copper block and a measurement was taken to determine the lead resistance of the system, this could then be subtracted from each of the values measured.

Figure 2.9a plots the resistance for mesas of different diameters for each of the four designs described above. In each case the samples behave as expected, with their resistance increasing as a function of the inverse of the mesa radius squared. Designs A and C have an identical behaviour but with the value of resistance for each of the mesa sizes greater for design A. Design B, the MLSL, has the greatest resistance for a 200 μm device and the increase in resistance as the mesa diameter decreases is more severe than in either design A or design C. Design D has very similar values to that of design B for the lower values of mesa diameter but has a value almost as low as design C for a 200 μm device. Due to the decreased doping in design D, it is believed that this low value is an erroneous point, as the lower doping should result in a higher resistance at each mesa diameter. It is clear to see from *Figure 2.9a* that design C, 10 nm $Al_{0.47}Ga_{0.53}As$ intermediate step, has the best electrical performance.

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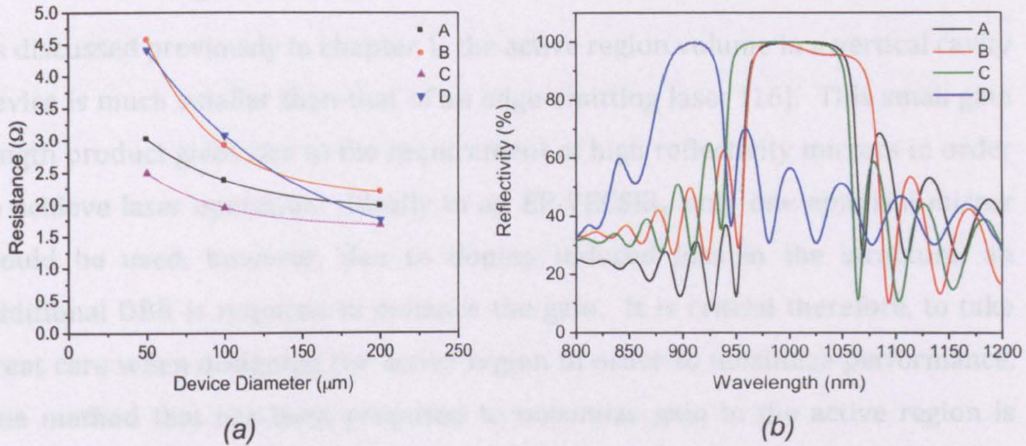

Figure 2.9 (a) Resistance as a function of mesa diameter for different p-DBR grading designs (b) Reflectivity spectrum for different p-DBR grading designs

In addition to the electrical performance, the optical characteristics of each of the designs were measured. As there were not facilities in Sheffield to perform high reflectivity characterisation of the samples, a quarter of each wafer was sent to our collaborator ETH in Zurich. The system used for the characterisation is described in the article [15]. In order to prepare each sample for characterisation the 200 nm p+ contact layer was etched off so it did not interfere with the measurement. *Figure 2.9b* plots the reflectivity over a given wavelength range for each of the different designs. Designs A and C again behave in a similar manner, the reduced stopband FWHM of design A attributed to the larger intermediate step thickness. Design B has a large bandwidth similar in size to design C, but the drop off in peak reflectivity is believed to be caused by an error in normalization of the data. For designs A, B and C the DBR centre wavelength is higher than predicted in the modelling, this is due to an increase in the grown layer thickness in the DBRs for each of these designs. The same characterisation was carried out for design D at a later date and the reflectivity spectrum produced was not as predicted. It is believed that the unexpected behaviour is caused by an error in measurement and not something resulting from the epitaxy of the structure. As a result of the information shown in *Figures 2.9a* and *b* design C provides the best overall performance and will be used as the basis for the full VECSEL structure shown in *Figure 2.1*.

2.6 Active Region Design

As discussed previously in chapter 1, the active region volume in a vertical cavity device is much smaller than that of an edge-emitting laser [16]. This small gain length product gives rise to the requirement of high reflectivity mirrors in order to achieve laser operation. Ideally in an EP-VECSEL, only one epitaxial mirror would be used, however, due to doping induced loss in the structure, an additional DBR is required to enhance the gain. It is critical therefore, to take great care when designing the active region in order to maximize performance. One method that has been proposed to maximize gain in the active region is called resonant periodic gain (RPG) [2], [17]. Since two highly reflective parallel mirrors surround the active region a standing wave will be formed.

Figure 2.10 shows the time-averaged energy density in the standing wave (*P*), with the red regions representing quantum wells of thickness d_{QW} placed at the antinodes of the standing wave. The value of *P* is given by the function

$$P = 2n\sqrt{\varepsilon_0}\, E_0^2 \cos^2(\beta z) \qquad (2.6)$$

where β is the propagation constant, and the positionally variant average value is $P_{av} = n\sqrt{\varepsilon_0}\, E_0^2$ and is a maximum $2P_{av}$ at the antinodes of the standing wave $\beta z = m\pi$ where $m = 0,1,2....$ Given that there is a periodic variation in the optical intensity with position, in a material with gain g this intensity variation will be given by

$$\frac{dP}{dz} = gP = 2gP_{av}\cos^2(\beta z) \qquad (2.7)$$

In the case where g is also varies with position it is possible to define an effective gain length product G given by

$$G = \int_{-\infty}^{\infty} g(z)\frac{P}{P_{av}}dz \qquad (2.8)$$

If a uniform gain g' exists and occurs over a length L, the gain length product for such a region is $G = g'L$. Now, if the gain is positioned as shown in *Figure 2.10* with N quantum wells each positioned at an antinode and having a thickness d_{QW}, then the spatial variation in gain is given by

$$g(z) = \sum_{i=1}^{N} d_{QW}\, g'\delta\left(z - \pi/_2\right) \quad (2.9)$$

The gain length is still the same $L = Nd_{QW}$, however, if the integral in equation *(2.8)* is now calculated, it can be seen that the gain length product has doubled compared to a uniform gain medium $G = 2g'L$. Hence positioning quantum wells in the manner shown in *Figure 2.10* allows up to twice as much gain to be obtained. Another point raised from the calculation is that quantum wells positioned at nodes of the standing wave pattern, *i.e.* zero electric field, will produce no gain. As an extension to this, it is possible to place multiple quantum wells at a single antinode in the cavity, hence being able to reduce the cavity length further. However, the result of this means a factor two gain enhancement is no longer achievable, with the maximum reduced to ~1.9.

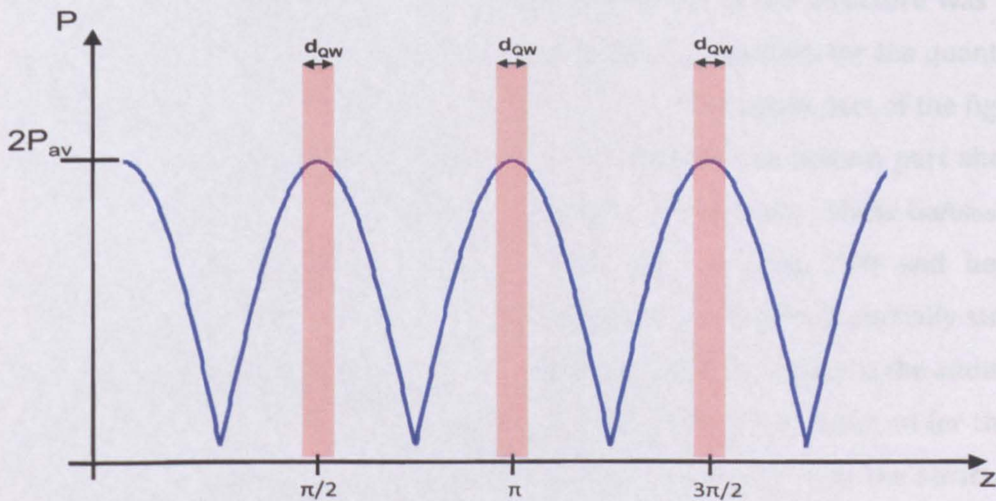

Figure 2.10 Illustration of the interaction between the electric field standing wave and the QWs in the active region

2.7 Strained Quantum Wells

Using the resonant periodic gain theory described above, the EP-VECSEL active region was designed incorporating six quantum wells separated into two groups of three and positioned at the standing wave antinodes to achieve maximum gain enhancement in a 3π/2 cavity. A six quantum well structure was chosen initially in order to make sure there was enough gain to offset the substrate loss. The quantum wells themselves were composed of $In_xGa_{1-x}As$, where varying the composition changed the emission wavelength. The thickness of each well was fixed at 8 nm. The use of InGaAs quantum wells in an AlGaAs/GaAs structure is desirable, as the difference in lattice constant between the two materials will result in the quantum wells being strained. This strain causes the light and heavy hole bands to separate leading to enhanced performance [18].

In the initial full EP-VECSEL test structures, the quantum wells were separated by GaAs barriers. However, these structures contained a large number of defects due to the accumulation of strain produced by the quantum wells and the DBRs. The defects seen as lines in the Nomarski image, *Figure 2.11a*, are a result of strain relaxation within the crystal, as the total strain in the structure was too high. The solution to this problem is to use $GaAs_{0.9}P_{0.1}$ barriers for the quantum wells instead of GaAs; this is shown in *Figure 2.11b*. The upper part of the figure shows the quantum wells with GaAs barriers, whereas the bottom part shows the same structure with the addition of the $GaAs_{0.9}P_{0.1}$ barriers. These $GaAs_{0.9}P_{0.1}$ layers have a lattice constant smaller than that of GaAs [19] and hence compensate for some of the strain in the structure resulting in a partially strain balanced structure. The InGaAs quantum wells are still strained, but the addition of these layers has reduced the total strain to below the level required for these defects to form. By incorporating the strain balancing layers into the structure, the full EP-VECSEL could be grown with a low defect density.

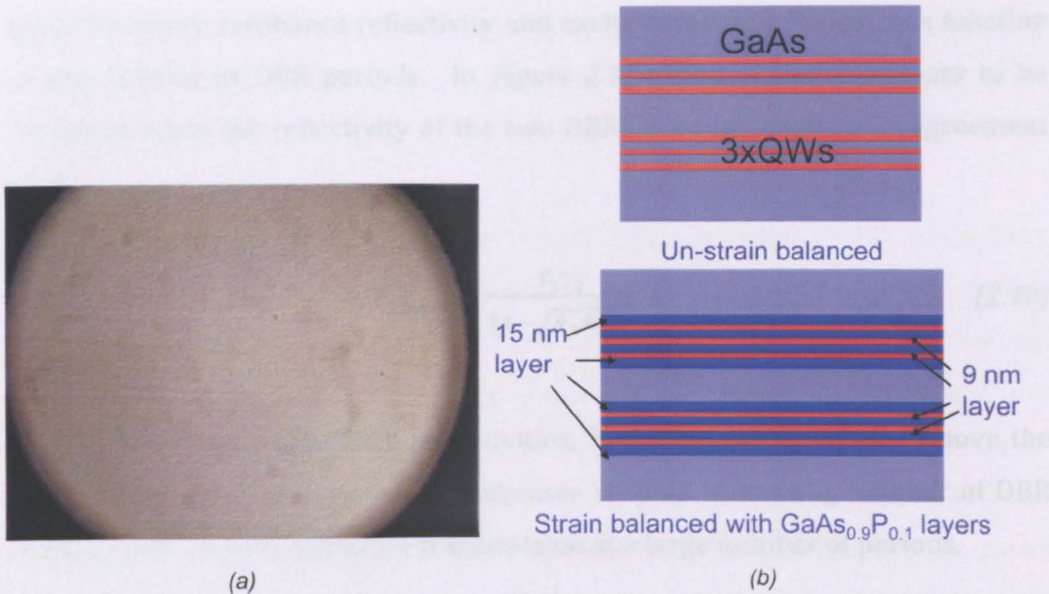

Figure 2.11 (a) Nomarski image of defective wafer (b) Schematic of QW active region without (top) and with strain compensating layers (bottom)

2.8 Cavity Resonance Position

Along with the spatial positioning of gain media within the active region, the spectral positioning is crucial for optimising device performance. The two parallel highly reflective DBRs in the structure form a high finesse cavity in which the active material is placed. This cavity also has an associated resonance position defined by the epitaxial structure; it is this resonance point from which the device will lase.

In order to observe the factors that affect the movement and shape of the cavity resonance with different design configurations, simulations were carried out. The simulations were once again performed using CAMFR. The DBR and cavity parameters were the same as those stated in previous section, however in this case a full VECSEL structure was simulated, *i.e.* an active region with a DBR on either side. In this case one DBR had a fixed number of periods m = 12 (R~90%) and the number of periods in the other DBR was varied, the reflectivity spectrums produced in each case can be seen in *Figure 2.12a*. It can be seen in the figure that the strength and spectral width of the resonance changes with the number of DBR periods, this is more clearly illustrated in *Figure 2.12b* which

plots the cavity resonance reflectivity and cavity resonance FWHM as a function of the number of DBR periods. In *Figure 2.12b* the resonance appears to be strongest when the reflectivity of the two DBRs is equal, which is in agreement with

$$T_{max} = \frac{T_1 T_2}{\left(1-\sqrt{R_1 R_2}\right)^2} \tag{2.10}$$

where R_1 and R_2 are the DBR reflectivities, $T_1 = 1-R_1$ and $T_2 = 1-R_2$. Above the point where $R_1=R_2$ the resonance decreases with an increasing number of DBR periods until there is almost no transmission at a large number of periods.

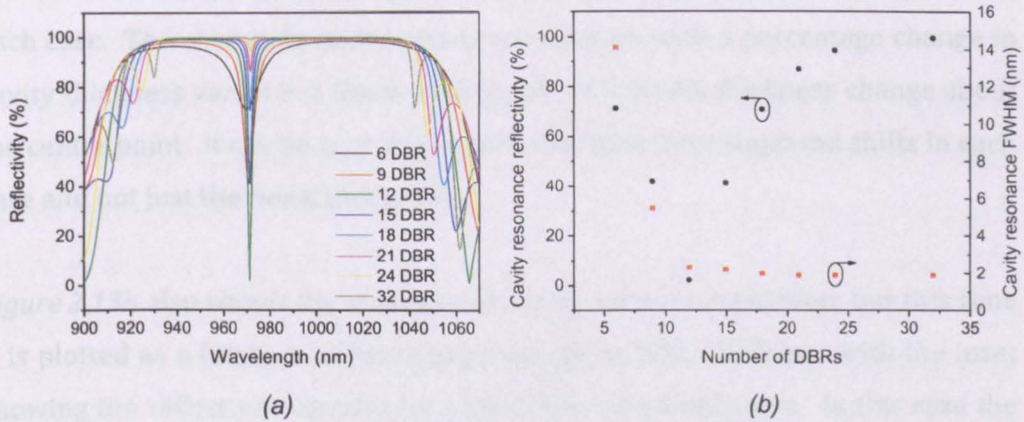

Figure 2.12 (a) Reflectivity spectrum for a cavity placed between two DBRs, where the number of periods of one is varied and the other is fixed at 12 periods (b) Cavity resonance reflectivity and FWHM of the cavity resonance as a function of different numbers of DBR pairs on one side of the cavity

Also of note in *Figure 2.12b* is that the cavity resonance FWHM decreases with an increasing number of DBR periods and above ~20 periods approaches a constant value of 2 nm. A wider cavity resonance FWHM will allow a larger spectral range of light to escape from the cavity, this property can be useful for tunablilty or for RCLEDs where a broad emission bandwidth is desired [20]. Other spectral artefacts shown in *Figure 2.12a* are a decrease in the DBR stopband width with an increasing number of DBRs, a behaviour discussed previously, and the

presence of interference fringes at the edges of the stopband, these are unlikely to cause any problems as their position is well outside the designed laser operating range.

In order to see the affect of a variation in layer thickness on the cavity resonance, another set of simulations were carried out, where the number of DBR periods were kept constant on both side of the cavity at m = 12 (R~90%) and the thickness of the DBRs and the cavity were altered to observe the effect. The initial thickness values for the cavity and DBRs have been described previously. This behaviour is important to understand, as there will always be a deviation from the required layer thickness during epitaxial growth. *Figure 2.13a* shows the variation in cavity resonance position with a percentage change in cavity thickness, with the inset to the figure showing the original reflectivity spectra for each case. The change in cavity resonance position with a percentage change in cavity thickness varies in a linear manner at ~3.2 nm/% thickness change about the centre point. It can be seen in the inset that the entire stopband shifts in each case and not just the resonance point.

Figure 2.13b also shows the variation in cavity resonance position, but this time it is plotted as a function of percentage change in DBR thickness, with the inset showing the reflectivity spectra for each of the simulated cases. In this case the variation in position is also linear with percentage change in DBR thickness, however it varies at twice the rate (6.4 nm/%) of the cavity thickness change, with the whole stopband shifting with the change in thickness. This information is useful as it is desirable to keep the cavity dimensions fixed in order to benefit from resonant periodic gain (described above), so in order to tune laser operation to a specific wavelength a variation in the DBR layer thickness can be applied.

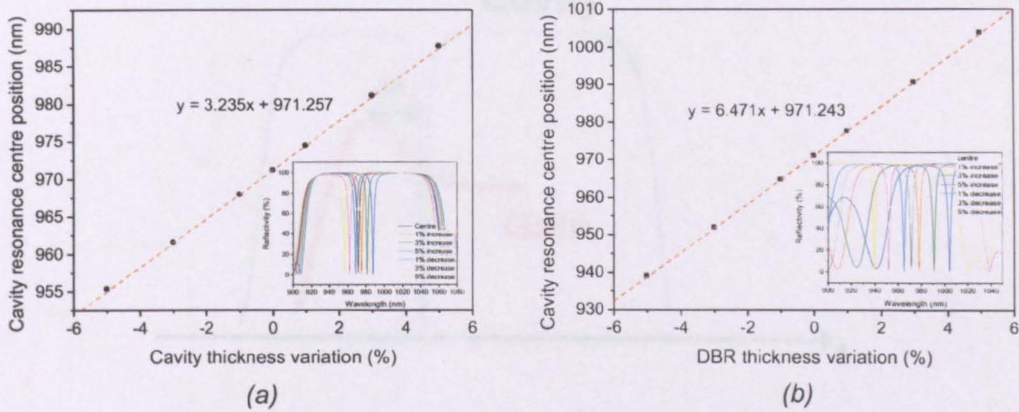

Figure 2.13 (a) Cavity resonance spectral position shift as a function of cavity thickness variation (b) Cavity resonance spectral position shift as a function of DBR thickness variation

2.9 Device Detuning

As mentioned previously in this chapter the resistive nature of DBR gives rise to unwanted joule heating in the device and consequently this negatively affects device performance. To compound this problem the cavity resonance position, which defines the lasing wavelength, has a lower rate of thermal shift, 0.07 nm/K, than that of the gain peak, 0.3 nm/K [21]. So in a device where a large amount of heat is generated this characteristic will exacerbate performance, as the amount of gain at the lasing wavelength will decrease with increasing temperature.

In order to remedy this problem the gain peak can be detuned [22], spectrally blue shifted, from the cavity resonance wavelength. This concept is illustrated in *Figure 2.14*, where $\Delta\lambda$ is the amount of detuning. In this manner it is possible to account for this negative affect when designing the device, however too much detuning will also negatively affect device performance.

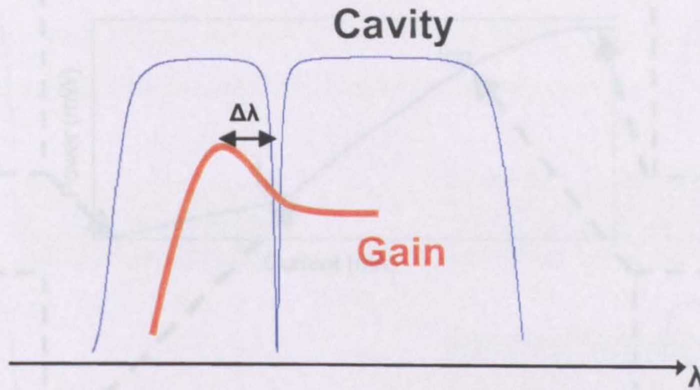

Figure 2.14 Illustration of detuning within a device

Figure 2.15 illustrates how the detuning would be set up in an ideal scenario by showing the position of the gain peak relative to the resonance position at different points along the current power curve. At zero current there is a specified amount of detuning, $\Delta\lambda$, between the gain peak and the resonance position. As the device reaches threshold a given amount of heat will have been generated in the device, shifting the gain peak towards the resonance point, such that the gain seen by the lasing wavelength is increasing. At a user defined operating current, I_{OP}, the gain peak has shifted further and is coincident with the resonance position, providing maximum gain. As the current increases further more heat is generated shifting the gain peak past resonance position decreasing the gain and causing thermal rollover, eventually with further current leading to device turn off. An increase in detuning allows the device to be driven to a high current before the onset of thermal rollover, however this comes at the cost of artificially increasing the threshold current. There will be an optimum amount of detuning to give a suitably low threshold as well as a reasonable range over which the device can be driven before rollover is reached. A change in thermal properties of the device will also change how much detuning is optimal, so it is an iterative design cycle.

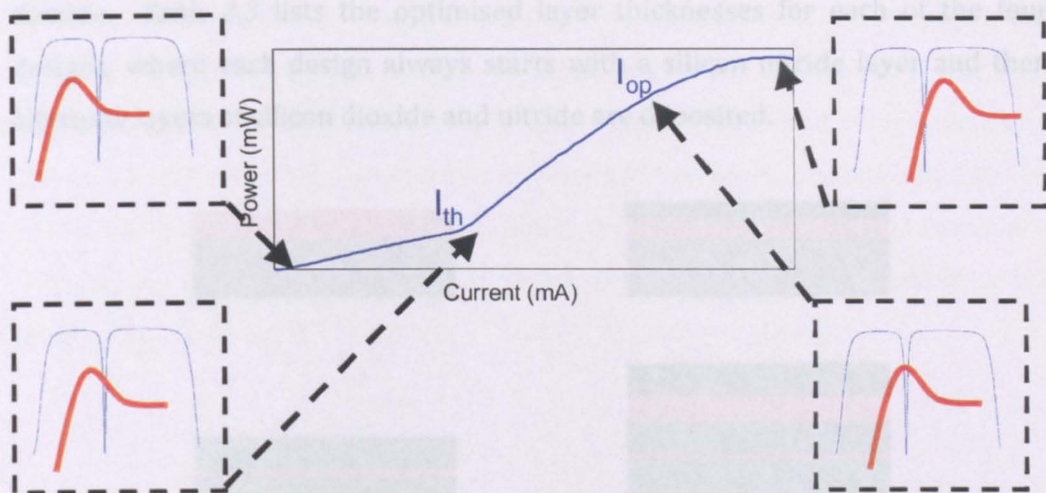

Figure 2.15 Illustration of desired detuning at different points in device operation

2.10 Anti-reflective Coating Design

The final section of this chapter will discuss the optimisation of an anti-reflective region placed on top of the device to reduce the coupling losses experienced by having an external cavity, and hence improving device performance. The introduction of this anti-reflective layer allows more light to couple back into the epitaxial structure from the external cavity in a single pass. This anti-reflective region could be grown epitaxially, however, as a bottom emitting geometry is used this would require the epitaxial growth of a current spreading reason, as a result it was chosen to deposit this region after growth.

The most basic anti-reflective layer is formed by depositing a $\lambda/4$ layer on the sample with a refractive index as close as possible to the square root of the substrate refractive index. More complex coatings can be formed using multiple layers of materials with different refractive indices, using the plasma enhanced chemical vapour deposition (PECVD) equipment layers of silicon dioxide ($n \sim 1.46$) and silicon nitride ($n \sim 1.92$) could be deposited. The Light Machinery Thin Film CAD tool [23] was used to optimize the layer thicknesses for a number of different designs comprised of silicon nitride and silicon dioxide layers. *Figure 2.16* shows the layer structure for the four designs simulated, the first comprised of a single layer, the second having two layers, the third made up of four layers and the fourth design having 6 layers. The pink regions in the figure represent layers of silicon nitride, whereas the green regions are layers of silicon

dioxide. *Table 2.3* lists the optimised layer thicknesses for each of the four designs, where each design always starts with a silicon nitride layer and then alternate layers of silicon dioxide and nitride are deposited.

Figure 2.5 Schematic of different anti-reflective layer coating designs (a) single layer (b) dual layer (c) four layer (d) six layer

	Optimised layer thickness (nm)					
1 layer	127	x	x	x	x	x
2 layers	96	64	x	x	x	x
4 layers	119	164	52	159	x	x
6 layers	154	162	52	159	128	160

Table 2.3 Layer thicknesses for different anti-reflective coating layer designs

Figure 2.17 plots the reflectivity spectrum for each of the four anti-reflective coatings described above. The single and dual layer coatings have similar minimum reflectance value but the dual layer coating maintains a lower value across a larger wavelength range. The four and six layer designs have zero reflectance at their minimum points with the six-layer design having a lower reflectivity over a wider range. The region over which the reflectivity is 1% or

less changes significantly from the one and two layer designs (~200 nm) to the four and six-layer designs (~100 nm). Depending on the application it might be preferred to have a low reflectivity over a wider range than zero reflectivity across a small range and an increased reflectivity in other regions. Due to the lasing wavelength in an EP-VECSEL being controlled by the cavity resonance position and the relatively small shift of this peak with temperature, allows a six-layer design to be used.

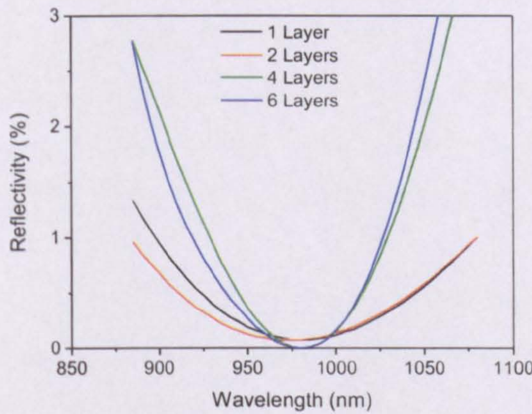

Figure 2.16 Modeled reflectivity spectrum for different anti-reflective layer coating designs

2.11 Conclusion

In this chapter the design of high reflectivity DBRs has been discussed, where the refractive index contrast and layer thickness of the two materials used and the number of DBR periods define the DBR properties. The electrical performance of a DBR can be significantly improved with the introduction of a grading region in between the two DBR materials and if this layer is thin then there is no significant effect on device optical performance. P-doped DBR structures offer a greater design challenge due to the reduced mobility of carriers as well increased free carrier absorption as a result of doping. Of the p-DBR designs grown and tested, the structure with a 10 nm single $Al_{0.47}Ga_{0.53}As$ step produced the lowest resistance as well as highest reflectance over the largest range.

Spectral and spatial positioning of gain is important within the device as correct placement of QWs in the active region can give rise to a factor two gain enhancement. While spectrally detuning the gain from the cavity resonance position allows for a large range of device operation before the onset of thermal rollover, at the cost of increased threshold current. Finally the addition of a multi-layer silicon nitride/silicon dioxide anti-reflective stack can allow for 100% transmission of light into the epitaxial structure in a single pass.

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3 Device Fabrication Development

3.1 Introduction

In this chapter the step-by-step method for device fabrication will be discussed, as well as all the optimisation steps required at each stage of the process. Finally a method for measuring the detuning across the EP-VECSEL epitaxy will be described. *Figure 3.1* shows a schematic of a fabricated EP-VECSEL device, where the pertinent features of the device are labelled. A trench structure is used for the electrical isolation of each device, this is then isolated with silicon dioxide and the trench is filled with gold to aid with heat extraction. The verticality and smoothness of the trench sidewalls are crucial for a low internal loss in the structure and achieving this is covered later in this chapter, where a smooth sidewall profile can be achieved using a hard etch mask and a $SiCl_4$: Ar ICP etch process. Etch depth of the electrical isolation region is also important, whereby etching through the active region can lead to surface recombination effects but too shallow an etch can lead to a large leakage current. These affects will be examined in this chapter.

In order to produce a low resistance device, special attention had to be paid to the resistance of the contacts used in the device, optimisation of the metals used and their optimum annealing temperature will be discussed. An optimum of 360°C is determined for the p-type contact and 400°C the n-type contact. Due to the bottom emitting geometry of the EP-VECSEL the current spreading layer is formed from the substrate, which was thinned to the appropriate thickness. The backside of the wafer required a smooth polished surface to allow for further backside processing as well as reducing surface scattering, the method by which this was achieved will be discussed. Additionally the deposition of the multi-layer AR stack, covered in chapter 2, will be discussed. In realising the multi-

layer designs produced in chapter 2, it is shown that a single layer design is the most repeatable and was hence selected for use.

Finally, a method for the characterisation of the detuning across a wafer will be introduced. By use of this method it is possible to obtain the amount of detuning at any position on the wafer.

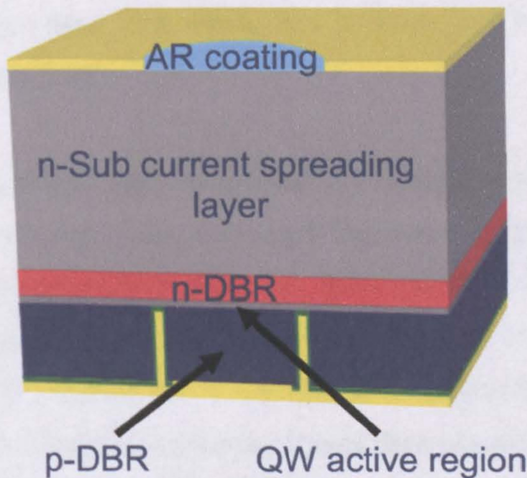


Figure 3.1 Schematic of EP-VECSEL structure

3.2 Device Fabrication Process

Figure 3.2a shows a pictorial representation of the epitaxial structure, with the active region denoted by the red region. The expanded region shows an SEM image of the active region clad with DBR layers on either side. In order to easily depict the device fabrication process only the top few DBR layers will be shown in the figures. All epitaxial growth was carried out by MOVPE on low and high n-doped 2" wafers, with each of the wafers labelled with its position on the susceptor. A process document for the process fabrication can be found in appendix B.

The process began by cleaving ~ $1/6^{th}$ out of the wafer using a diamond tipped hand-scribe tool. This was followed by an inspection of the sample under the microscope to check for areas of dirt and growth defects. A 3 stage clean was then performed on the sample, by firstly placing the sample in warmed n-butyl

acetate, it was then removed and wiped with a cotton bud that been dipped in the n-butyl acetate. This was repeated several times, it was then placed into acetone, followed by isopropyl alcohol (IPA) and then blown dry using a nitrogen gun. All subsequent 3-stage cleaning did not contain the cotton bud step. The whole process was then repeated until the sample was clean, determined by observation of the sample under the microscope. The sample was then placed in the PECVD and 400 nm of silicon dioxide were deposited on the surface to form the basis of the hard etch mask, this is illustrated by the green layer on the sample in *Figure 3.2a*.

Once the deposition was completed the sample was inspected to check the quality of the dielectric and make sure there was no fragments embedded in the dielectric caused by 'drop off' from the chamber. A 3 stage clean was then carried out before beginning the photolithography. The sample was first placed onto a 100 °C hotplate for 1 minute as a dehydration bake, to remove any remnants of the cleaning solvents. It was then placed onto a piece of blue tacky paper to protect the sample's backside and put onto the vacuum chuck of a spinner. The sample was first coated with adhesion promoter, which was then spun at 4000 rpm for 30 seconds. On top of this, a layer of SPR350 was deposited and again spun at 4000 rpm for 30 seconds. The sample was then placed on the hotplate for 1 minute to bake the photoresist; this is represented by the purple layer in *Figure 3.2b*. As a result of thickness non-uniformity in the resist across the sample, known as edge bead, an area of ~2mm around the edge of the sample was removed. This was done by masking the sample using a piece of scrap wafer and then exposing the sample for ~20 seconds (much longer than the actual exposure time for that resist) followed by development for 1 minute in MF26a and finished with a rinse in water before blow drying the sample.

Next, the sample was placed in a mask aligner and positioned under the trench pattern of the trench photolithography mask. The resist was then exposed and the sample was developed in MF26a developer for 1 minute, followed by a rinse in water to stop the development process. This is shown in the bottom right hand part of *Figure 3.2b*, where the black area is the mask and the blue arrows

represent the UV light used to expose the photo resist. The sample was then examined under the microscope to check the quality of the exposure, it was crucial that all the exposed areas were free from photoresist and that a good reproduction of the mask pattern was present. Following this, the sample was oxygen plasma ashed for 1 minute 30 seconds to make sure there were no thin layers of resist present in exposed areas. In the meantime the ICP was set up by running the etch process with an empty chamber for 30 minutes to condition the chamber to the gasses for the process.

The next step was to pattern the silicon dioxide dielectric layer with the photoresist pattern; this was carried out by etching the dielectric using the ICP. This is shown in the bottom left part of *Figure 3.2b* where the red arrows represent the plasma used for etching. The etch recipe was made up of 20 sccm of CHF_3 and 20 sccm of Ar, with a RF power of 200 W and chamber pressure of 35 mT. The sample was placed on the silicon carrier wafer with a little fomblin oil to aid with thermal transfer and moved into the chamber. The Intellimetrics End Point Laser Interferometer was positioned such that the laser was focused on an area of unmasked dielectric. The etch process was then started and the trace from the End point system was used to determine when all the dielectric had been etched through, as the trace would go flat indicating no change in layer thickness. For 400 nm of silicon dioxide the etch time was ~25-30 minutes.

The sample was then removed and inspected under a microscope to make sure all the dielectric had been removed in the unmasked areas and that the fidelity of the pattern was high. If dielectric was still visible the sample would be put back in the ICP and etched further until the dielectric had been removed. If the sample was free from dielectric, then the photoresist would be removed, shown in the top part *Figure 3.2c*. The first stage of this would be a 5 minute oxygen plasma ash to soften the plasma hardened resist. Next the sample would be placed in some Posistrip resist stripper on the 100 °C hotplate for 2 minutes to remove the resist. After removing the sample from the stripper it was rinsed in water followed by IPA and blown dry. The sample was then inspected to see if there was still any residual resist left on the surface, if this was the case the

above steps would be repeated. If the sample was free from resist streaks then a 3 stage clean would be carried out.

The dielectric hard mask would now be used to transfer the trench pattern into the semiconductor, shown in the top right part of *Figure 3.2c*. As with above the ICP was run for 30 minutes with an empty chamber in order to condition the chamber to the process. Initially a test sample was to be used to determine the etch rate of the process, so that the etch depth of the actual sample could be controlled accurately. To determine the etch rate, the relative heights of features on the sample had to be measured before and after the etch; this was carried out using a Dektak Surface Profiler. This equipment drags a cantilevered arm across the surface of the sample to measure the relative heights of the features. Since the trench width (5 μm) was too narrow to be directly probed, the edge of the sample where the dielectric had been etched was measured. Due to a slight thickness variation across the sample, the height at several different points on the sample was measured.

The test sample was loaded into the chamber, this time with no fomblin oil on as the sample was now more thermally stable with no photoresist on it, and the End Point laser was focused on an exposed semiconductor area. In this case the etch recipe was 5 sccm $SiCl_4$ and 2 sccm Ar, with a chamber pressure of 2 mT, a RF coil power of 150 W and an ICP coil power of 250 W. The test sample was etched for 8 minutes, it was then removed and the etch depth was measured using the Dektak. The etch depth was given by the change in the relative heights of the semiconductor area on the sample, this was then divided by the etch time to give the etch rate. Due to the small feature size of the trenches, they will experience a smaller etch rate compared to the measured regions, from SEM measurements the trench is ~800 nm shallower than the measured region. This discrepancy is consistent across the sample as well as from run to run.

The real sample was then placed in the ICP, which was set up in the same way as for the test sample. It was required that the sample be etched through the p-DBR to just above the active region, in this case ~ 5 μm. The typical etch rate for the

semiconductor etch described is ~ 600 nm/min, giving an etch time of approx. 8 min, this was adjusted by the measured etch rate of the system to get the desired etch depth. Once the etch was completed the sample was measured using the Dektak to check the achieved etch depth, it was also inspected under the microscope to ensure that etch profile was as expected. The etching was finished off with a 30 second 20:1 Citric acid, hydrogen peroxide wet etch, to smooth out the etch profile. The sample was then rinsed in water to stop the etching before being blown dry. Another 3 stage clean was then performed before moving on to the next step.

The next process was to remove the dielectric hard mask, as shown in the bottom right part of *Figure 3.2c*. This was done in the same manner as described above, using the same CHF_3: Ar recipe, with a required etch time of ~ 30 minutes to remove all of the silicon dioxide on the surface. The sample was then removed and inspected to make sure no silicon dioxide was left on the surface, any dielectric remaining could result in problems with electrical connections or cause subsequent layers of dielectric to peel off. Once the sample was free from dielectric it was given a 3 stage clean, before it was placed back in the PECVD to have another 400 nm of silicon dioxide deposited on the surface, shown in the bottom left part of *Figure 3.2c*. This step was carried out to passivate the trenches and device surface. While 400 nm of dielectric was deposited on the surface, only ~ 200 nm will be deposited on the trench sidewall. Again the sample was inspected and cleaned before continuing on to the next process step.

The sample was then prepared for the next photolithography step by firstly having a dehydration bake, before being coated with adhesion promoter and SPR350 (as described previously) and baked for one minute, depicted in the top left portion of *Figure 3.2d*. The edge bead process, as described previously, was again carried out. The sample was placed in the mask aligner and positioned so that the pattern on the sample was aligned with that on the mask before being exposed. Next, the sample was developed in MF26a for 1 minute to produce a pattern in the resist, as show in the bottom right of *Figure 3.2d*, before being rinsed in water and blown dry. The quality of the exposure was checked, again

looking for residual resist in exposed areas and the quality of pattern produced; this step was then followed by a 1 minute 30 second oxygen plasma ash.

The next step was to etch the region of dielectric opened up by the photolithography; this was done using the ICP. The same process for etching dielectric, as described previously, was used. The process required ~ 30 minutes to etch through the silicon dioxide layer and is illustrated in the bottom right part of *Figure 3.2d*. Once the etching was complete, the resist could be removed. This was first done by softening the resist using an oxygen plasma for 5 minutes, and then in the Posistrip on the 100 °C hotplate for 2 minutes, and finished with a 3 stage clean. The sample was then inspected to make sure it was clean and free from streaks of resist on the surface or in the trenches, shown in the bottom left part of *Figure 3.2d*. If resist was still present the clean process was repeated, otherwise the sample moved onto the next stage of the process.

The sample was then prepared for photolithography by having BPRS100 photoresist spun onto the sample and then baked for 1 minute; this is shown in the top right part of *Figure 3.2e*. Next, was to place the sample in the mask aligner and position it so that the pattern on the surface aligned with that of the metalisation pattern on the mask. The sample was then exposed and developed in 3:1 H_2O: PLSI for 1 minute, followed by a rinse in DI water and blown dry, this is depicted in the bottom right part of *Figure 3.2e*. The photolithography pattern on the sample was checked and then the sample was given a 1 minute 30 second oxygen plasma ash. Now the sample was ready for the first metalisation stage.

A thermal evaporator was used to deposit an Au/Zn/Au metallic contact onto the device. The evaporator was set up by placing a W coil and a W basket at a position 6 cm above the crystal thickness monitor, the W coil was then filled with a 2 cm length of gold wire folded four times. The W basket was filled with ~ 10 mg of zinc wire. Next, the sample was washed in 19:1 H_2O: Annular Ammonia solution for 30 seconds, to remove the surface oxide, followed by a rinse in water and a blow dry. It was then placed into the evaporator, underneath the coils and close to the crystal thickness monitor. The chamber was then evacuated and

pumped down to a pressure of $1.5x10^{-6}$ T before the evaporation could be carried out, this usually took ~ 2 hours. Once the correct pressure had been reached, a thin layer of gold, ~ 5 nm, was deposited on the surface, this layer helped promote adhesion of the zinc. The thickness of each layer deposited is measured using the crystal thickness monitor. Next the W basket was energized and ~ 10 nm of zinc was deposited on top of the gold layer. Finally, another 200 nm of gold were deposited on top of the sample. Once the deposition was complete the chamber could be pumped back to atmosphere, the sample and the coils could then be removed.

The sample was then placed in a beaker of acetone, in order to break down the photoresist and 'lift off' the gold in the areas it was not required. The 'lift off' was encouraged by spraying additional acetone on to the sample from a squeezy bottle. Once all the unwanted gold had been removed, the sample was inspected for any residual resist. If any resist was present it was removed using the method described previously. When the sample was clean it was placed in the RTA and annealed at 360 °C, where the program had a 30 second ramp time and a 3 second dwell. This allowed for the formation of a low resistance electrical contact in the dielectric window region, as shown in the bottom left part of *Figure 3.2e*.

Next, a layer of Ti/Au was to be sputter deposited over the entire sample, shown in the top right part of *Figure 3.2f*. The sample was placed in the sputter tool, which was then pumped down to low pressure, $2x10^{-6}$ T, taking about 40 minutes. The kit was then set up to deposit 20 nm of titanium on the surface of the sample and the process was carried out, taking ~ 90 seconds. Once this was finished the system was recalibrated and 300 nm of gold was deposited on top of the titanium, taking ~ 900 sec. After this process was finished the chamber was pumped to atmosphere and the sample was removed, the front side processing of the sample was now complete.

The next stage in process was to thin and polish the substrate in order to form the current spreading layer in the device. Firstly, the sample was spun with

SPR350 resist and baked for 1 minute, to form a protective layer on the top surface of the sample. Then, a circular glass block was heated on the 100 °C hotplate for 5 minutes before being covered in a special wax. The wax was allowed to flow for 5 minutes, to become uniform, and then the sample was mounted process side down on the block. Scrap GaAs material of the same thickness was then positioned around the sample. This was then left on the hotplate for 5 minutes to readjust and level out, the glass block was then removed and left to cool until the wax had set firm. The relative height of different point was then measured across the sample; an average deviation of 10 μm across the sample was allowable. However, any larger and the sample had to be removed and the process repeated. The mounted sample is shown in the bottom right part of *Figure 3.2f*.

The glass block was then placed in the vacuum jig of a Logitech LP50 lapper/polisher. The jig was then placed on to the glass lapping wheel, which was set to rotate at 20 RPM. The glass wheel was constantly being covered with a 1:9 mixture of calcined aluminium oxide, with a 3 μm particle size, and water. The jig contained a spring to vary the force on the glass block; this was adjusted to give a lapping rate of 1-2 μm/min. The substrate was then thinned down to ~ 150 μm, at this point the lapping media was changed to aluminium oxide, with a particle size of 0.3 μm, and a further 40 μm of thickness was removed. Once at the desired thickness of 110 μm the glass block was removed from the jig and rinsed with DI water to remove any remaining GaAs slurry on the sample and then blown dry.

Next, the sample, still mounted on the glass block, was placed in a beaker of 1:1:1 etchant for 6 minutes to clean and smooth the backside of the sample, etching ~ 10 μm in thickness. The etchant was made up from 30 ml of each of the following acetic acid, hydrobromic acid, potassium dichromate and DI water. The glass block was then removed, rinsed in water to halt the etching and then blown dry. The backside of the sample was now thinned and had a smooth and shiny appearance, depicted in the bottom left part of *Figure 3.2f*. To remove the sample from the glass block it was placed in a beaker of warm n-butyl acetate,

which broke down the wax allowing the sample to be removed. The sample was then given an inspection on both sides of the sample, to check for contaminants, followed by a 3 stage clean.

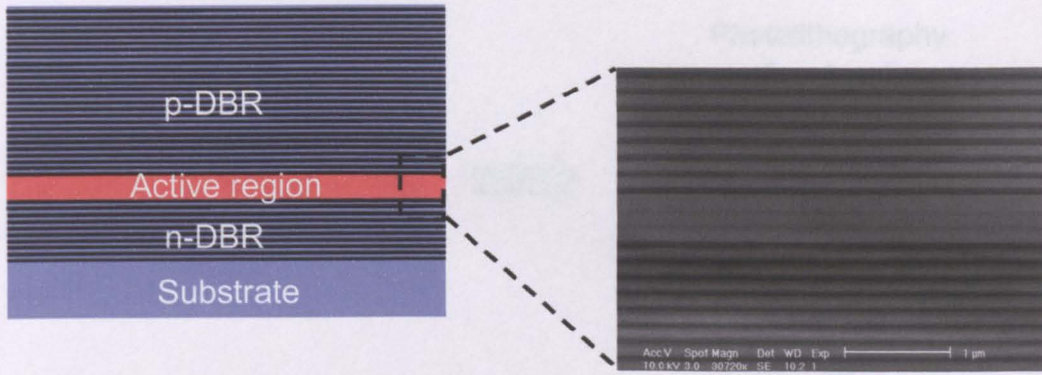
The next stage was to perform front to back lithography on the sample, to allow the front and back features to line up. Firstly, the sample was mounted, epitaxial side down, on a glass cover slip using wax; the whole thing was then spun with adhesion promoter and BPRS100 photoresist and baked for 1 minute. This can be seen in the top left part of *Figure 3.2g*. Next the sample was placed semiconductor side down in the mask aligner. The processed side of the sample could then be viewed through the glass cover slip and aligned to the features on the mask plate. This was then exposed and developed using the 3:1 H_2O: PLSI to produce features on the glass cover slip itself, this is shown in the top right part of *Figure 3.2g*. The sample could then be placed back in the mask aligner; this time cover slip side down, and the mask pattern could be aligned to the pattern on the glass slide itself. This was again exposed and then developed using the 3:1 H_2O: PLSI to produce a pattern on the backside of the wafer that was aligned with the front, this is illustrated in the bottom right part of *Figure 3.2g*.

The sample was now ready for the InGe/Au backside metalisation; again this was carried out using a thermal evaporator. The evaporator was set up by placing a W coil and a W basket at 6 cm from the base of the chamber. The W coil was filled with two 2 cm lengths of gold wire folded 4 times each to fit in the coil, the W basket was filled with a ball of indium and a ball of germanium. The sample was rinsed in 19:1 annular ammonia solution for 30 seconds to remove the surface oxide; this is followed with a rinse in DI water before being blown dry. It was then loaded into the evaporator, which was then pumped down to the required pressure. Once the correct pressure was reached 20 nm of indium/germanium alloy was deposited on the surface, this was then followed by 400 nm of gold. Once the sample was removed from the chamber the 'lift off' process was carried out. The sample was then inspected and any remaining resist was removed before the sample was annealed in the RTA at 360 °C, using the same program as previously described. This produced a low resistance n-

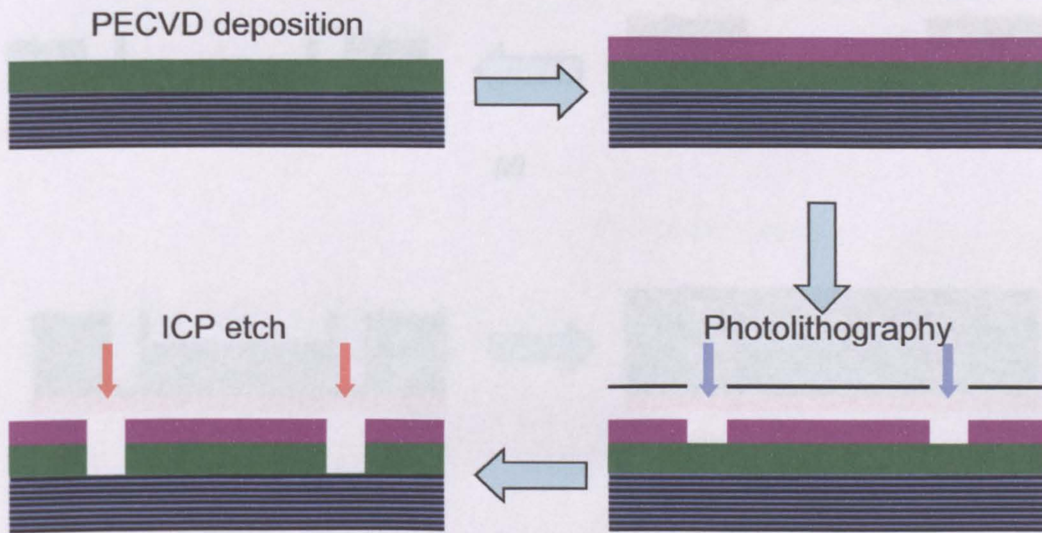
type contact on the backside of the sample, depicted in the bottom left part of *Figure 3.2g*.

Next, was the deposition of the anti-reflective layer, a test piece of silicon was placed in the PECVD and the silicon nitride program was run for 5 minutes. The film thickness of the silicon nitride layer was then measured using an ellipsometer; from this the deposition rate could be calculated. The sample was then placed, epitaxial side down, into the PECVD where a 127 nm layer of silicon nitride was deposited, adjusting the time using the deposition rate measured, this is shown in the top left part of *Figure 3.2h*.

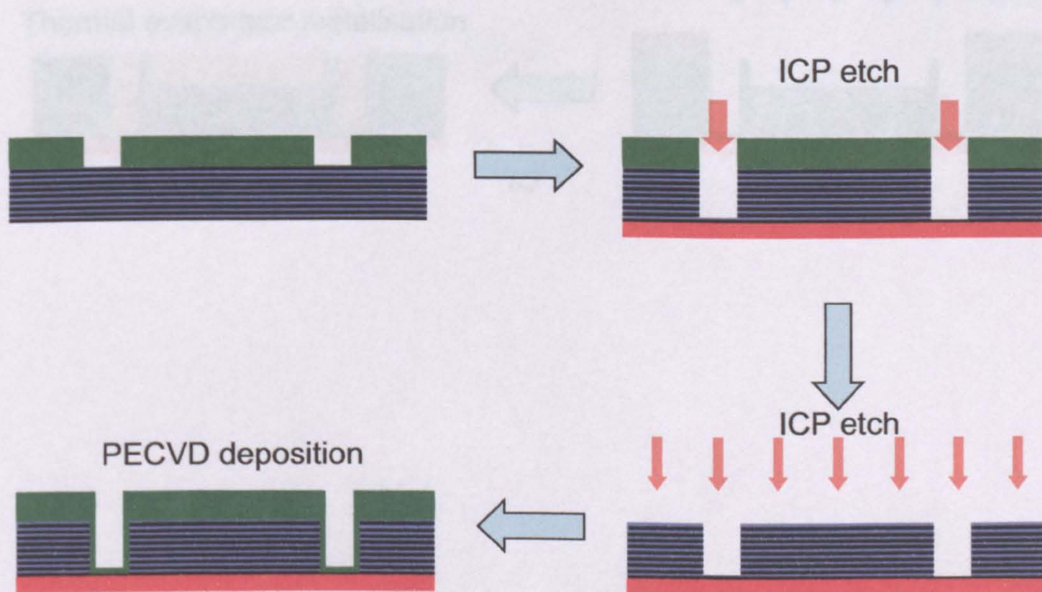
This anti-reflective coating then had to be removed in specific areas; this was done by first masking off those areas using photolithography and then dry etching. The sample was spun with adhesion promoter and SPR350 and baked for 1 minute. It was then aligned and exposed in the mask aligner, before being developed in MF26a for 1 minute. The sample was then inspected and oxygen plasma ashed for 1 minute 30 seconds to produce the alignment pattern shown in the top right of *Figure 3.2h*. The dry etching this time was carried out in the reactive ion etcher (RIE) as the sample surface was covered in gold. As with previous cases the chamber was conditioned by running the recipe for 30 minutes with no sample in the chamber. The etch recipe consisted of 35 sccm of CHF_3 and 5 sccm of O_2, with a chamber pressure of 35 mT and a RF coil power of 80 W. An End point detection system was used to determine when the etch was completed, taking ~ 20 minutes. An illustration of the etched sample is shown in the bottom right of *Figure 3.2h*. The sample was then inspected to see if all the silicon nitride had been removed, if not the sample was placed back in the RIE for further etching. If the window regions were clear, the resist was removed using the oxygen plasma and resist stripper process described previously. Once the sample was clean, as shown in the bottom left part of *Figure 3.2h*, the device processing was completed.



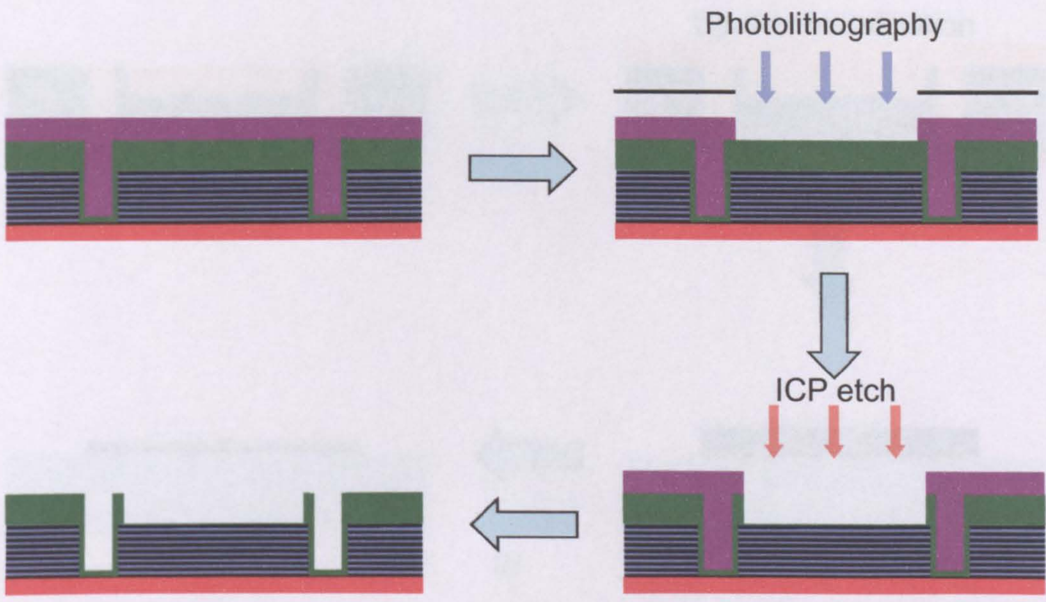
(a)



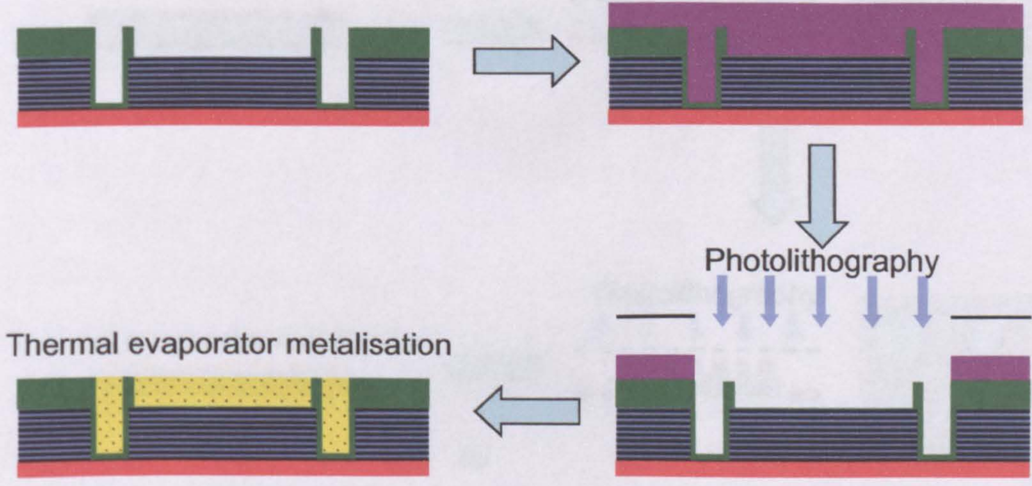
(b)



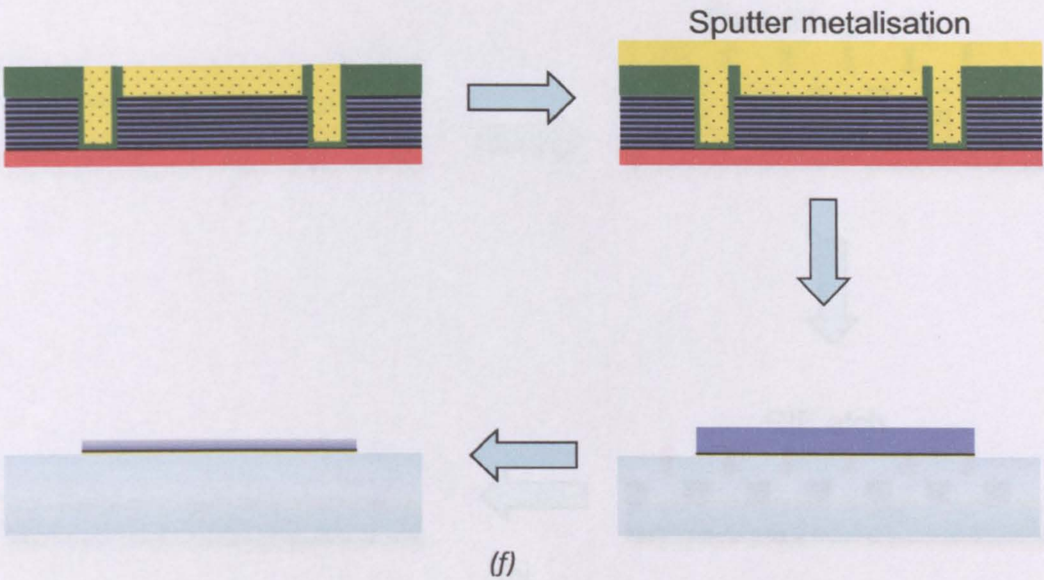
(c)



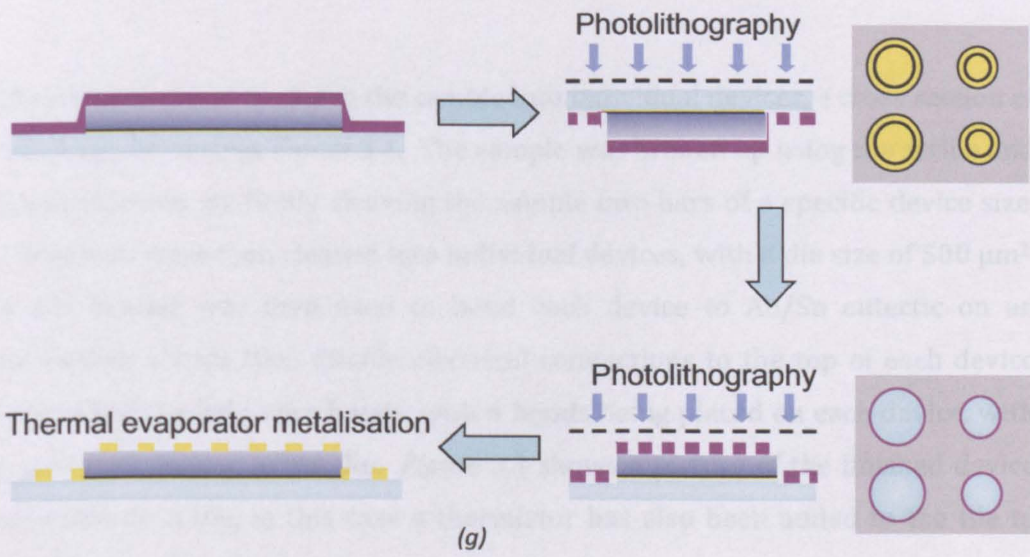
(d)



(e)



(f)



(g)

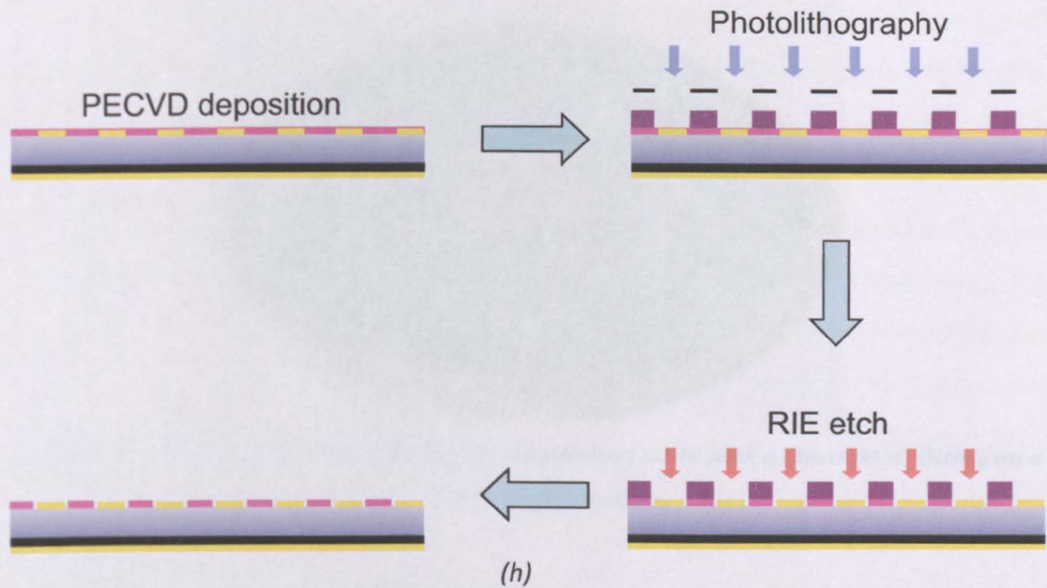


Figure 3.2 (a)-(h) Pictorial representation of EP-VECSEL device fabrication process

The next stage was to cleave the sample into individual devices, a cross section of which can be seen in *Figure 3.1*. The sample was broken up using the scribe and break machine, by firstly cleaving the sample into bars of a specific device size. These bars were then cleaved into individual devices, with a die size of 500 μm². A Die Bonder was then used to bond each device to Au/Sn eutectic on an aluminium nitride tile. Finally electrical connections to the top of each device were added by gold wire bonds, with 4 bonds being placed on each device, with one in each corner of the die. *Figure 3.3* shows a picture of the finished device mounted on a tile, in this case a thermistor has also been added to the tile to monitor the tile temperature.

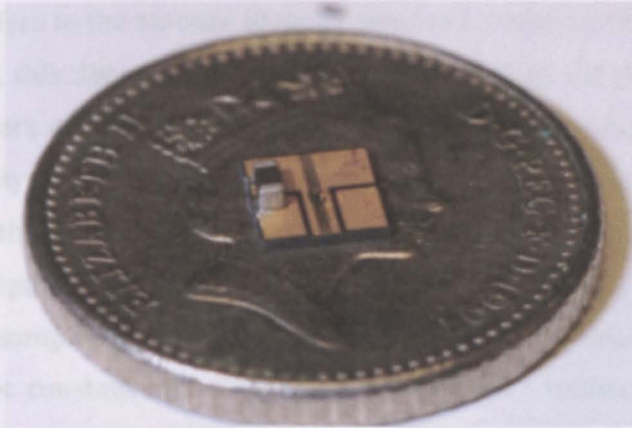


Figure 3.3 Picture of an EP-VECSEL device mounted on a tile with a thermistor, sitting on a 5 pence piece for scale

3.3 Trench Etch Development

The trench etch provides an important function within the device structure, allowing optical and electrical confinement within the device. Crucial to this performance is the verticality and smoothness of the trench sidewalls, which can yield low internal loss. A useful tool in the etching of these devices is the ICP dry etch tool. This has an additional coil that inductively couples to the plasma driving it downward giving the etch plasma much greater directionality, with the more power in the coil the greater the downward force [1]. This etch profile is complicated by the trench shape itself; where semiconductor material has to be removed from a narrow region (5 μm) as opposed to a mesa etch where a large amount of material is removed across the entire sample. The trench geometry is preferred as planar surface is maintained throughout device processing, as well as exhibiting better thermal properties. Another issue that will exacerbate the etch profile is the DBR, as the different materials of the different layers can etch at different rates, producing a corrugated pattern. There are a number of different parameters that can be adjusted when trying to optimise the etch profile, in this section a number of them have been investigated.

The two main problems encountered when using photoresist for etching are thermal loading and etch selectivity. As the resist is a liquid polymer that is set by baking, it is susceptible to deform or burn at high temperature. Etch

selectivity refers to the amount of resist removed relative to that of the material being etched, this depends on chemical composition of the plasma, the RF and ICP coil powers and the type of resist used, a typical selectivity might be 3:1. This selectivity dictates the required resist thickness to etch a given depth. In order to test the suitability of different types of photoresist, samples with the full EP-VECSEL epitaxial structure were patterned with these resists and then etched. The samples were etched in the ICP, with the gas mixture and chamber pressure kept constant and only the ICP coil power varied. The etch recipe consisted of 5 sccm $SiCl_4$, with a chamber pressure of 2 mT, RF coil power of 100 W and the ICP coil power varied between 250, 350 and 500 W. Each of the samples was etched 5 μm, which was roughly the required device etch depth. *Figure 3.4* shows images of the samples after etching for BPRS200 resist. Images *a, c, e* in *Figure 3.4* show the samples prior to the removal of the photoresist, whereas photos *b, d, f* show the surface with the resist removed.

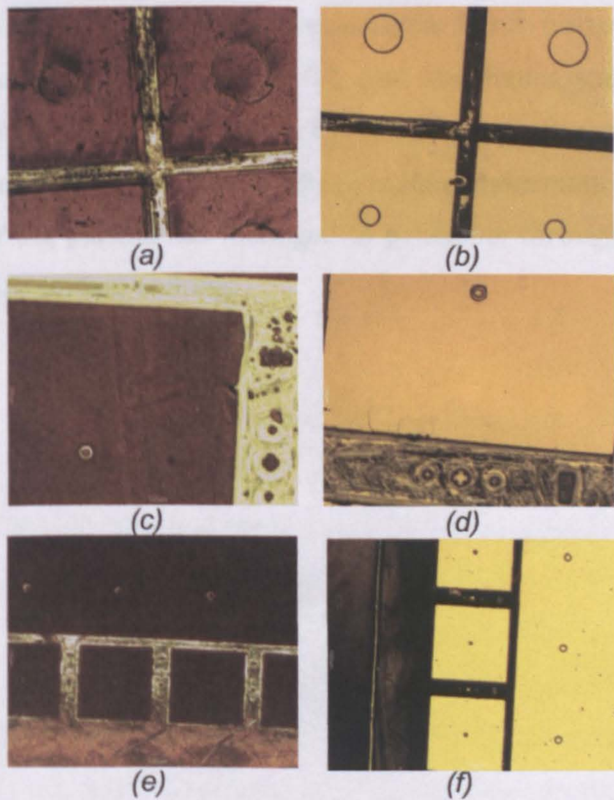


Figure 3.4 Microscope images of ICP etch pattern for BPRS200 resist at different ICP coil powers (a) 250 W (b) 250 W resist removed (c) 350 W (d) 350 W resist removed (e) 500 W (f) 500 W resist removed

The ICP coil power increases from top to bottom in the figure, with the top etch being carried out at 250 W and the bottom etch being done at 500 W. It can been seen from the figure that there is a significant amount of etch damage done in unmasked areas for each of the coil powers, but the severity is increasing with coil power. There is also moderate distortion in the etch profile as a result of resist deformation, which is also increasing with increased ICP coil power. The dark nature of the resist after each etch is due to the thermal stress placed on it, roughening the resist surface, and can be seen to get darker (rougher) with increasing power.

Figure 3.5 shows images of the etch test samples masked using SPR220 resist. The images are arranged in the same manner as previously, left hand image still have photoresist on the surface, whereas in the right hand images it has been removed, and the ICP coil power increases from top to bottom. SPR220 was the thickest resist used in the test (~ 5.2 μm) and hence susceptible to greater thermal loading, this can be seen in the left hand images as a roughening and burning of the surface. In each case there is some deformation of the etch profile and at 500 W the plasma has managed to penetrate through the resist in small areas leading to surface etching.

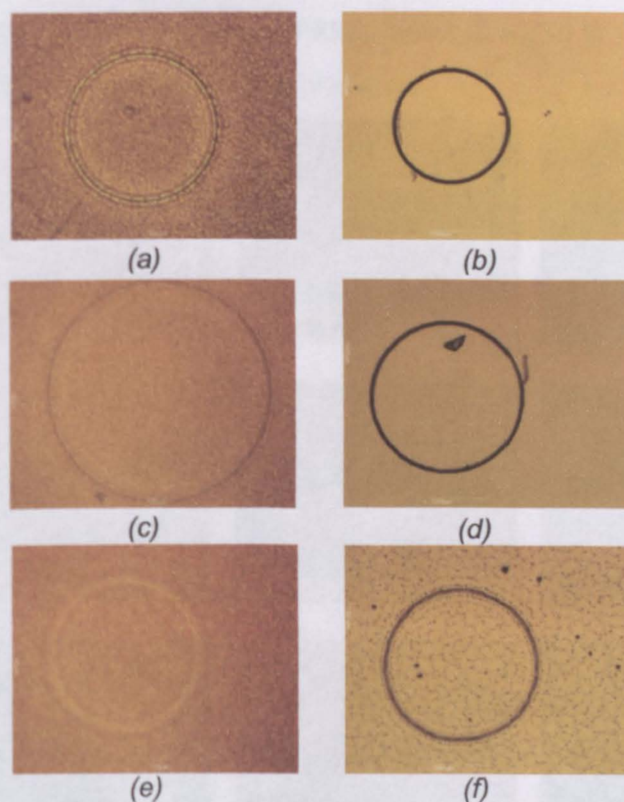


Figure 3.5 Microscope images of ICP etch pattern for SPR220 resist at different ICP coil powers (a) 250 W (b) 250 W resist removed (c) 350 W (d) 350 W resist removed (e) 500 W (f) 500 W resist removed

Figure 3.6 shows the etch profile for samples masked using SPR350 photoresist, the arrangement of the images is the same as in the previous two cases but SEM images of the etch profile are included for each coil power. At 250 W the sample shows no degradation in the resist due to the etching process, and the resulting sidewall profile is vertical with only a small amount of roughness to it. When the power is increased to 350 W, thermal damage to the resist becomes apparent and there is surface damage in unmasked areas. The trench shapes on the microscope image appear not to have deformed, this is backed up by the straight edges of the trench profile in the SEM. However, the sidewall profile is undercut and has both a vertical and a horizontal corrugation. In the case of the 500 W sample, the thermal damage is greatly increased, with the resist now very dark. There is deformation in the resist shape shown by the bevelled edge of the SEM image, as well as surface damage that can be seen in both images *h* and *i*. From

the sets of figures above only the SPR350 resist at a 250 W coil power produces an etch profile suitable for device fabrication.

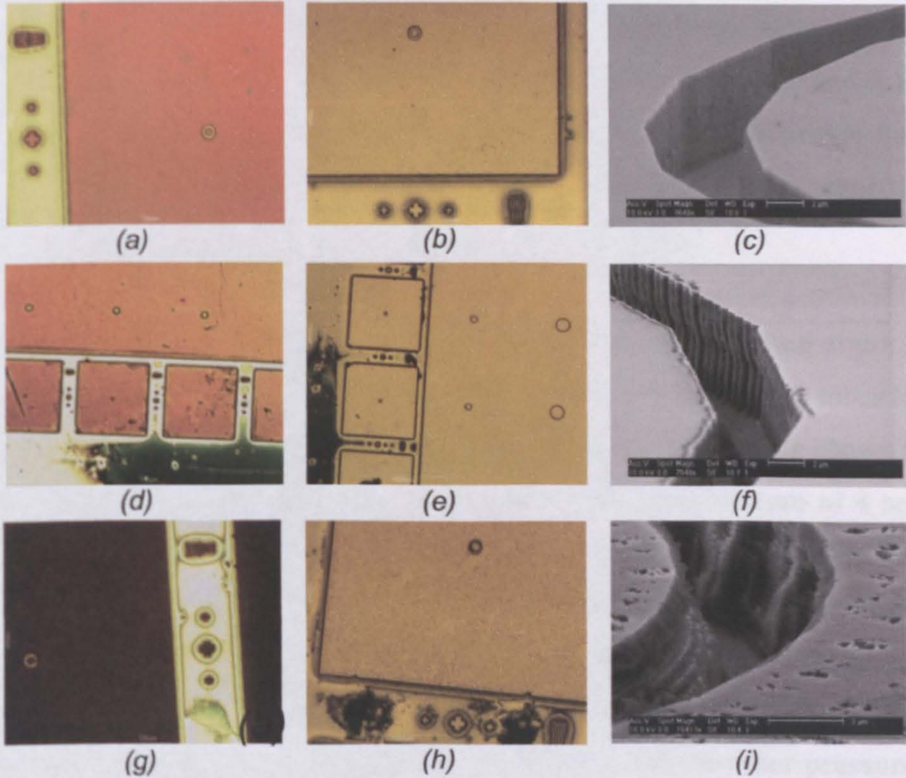


Figure 3.6 Microscope and SEM images of etch pattern and profile for ICP etching at different coil powers using SPR350 resist (a) 250 W (b) 250 W resist removed (c) 250 W SEM trench profile (d) 350 W (e) 350 W resist removed (f) 350 W SEM trench profile (g) 500 W (h) 500 W resist removed (i) 500 W SEM trench profile

Another option to be considered is the use of a hard mask. This is formed by etching the photolithography pattern into a dielectric layer deposited on the surface, and then using this dielectric layer as the semiconductor etch mask. The two main advantages of this are a much higher etch selectivity, allowing deeper etches to be performed, and greater thermal stability meaning no distortion in the etch pattern, with the added ability to use higher ICP coil powers. *Figure 3.7* shows SEM images of the trench profiles for hard mask etches under different etch conditions. Images *a* - *d* use the same etch recipe as for the photoresist etch tests, with a 500 nm silicon dioxide hard mask, and the ICP coil powers increasing from 500 W to 800 W from image *a* - *d*. In each image the hard mask has been removed before imaging in the SEM, residual silicon dioxide can be

seen as blobs on the surface of image *b*. Image *a*, etched at 500 W, has a reasonably smooth sidewall profile, but has a slight undercut in the etch profile. Image *b*, etched at 600 W, has no undercut but there is an increased vertical corrugation in the sidewall profile, which is undesirable. Images *c* and *d*, etched at 700 and 800 W respectively, both have a smooth sidewall profile but also exhibit a barrel like etch profile, where there is a severe undercut near the top and then the profile juts back out in the opposite direction.

Further adjustments to the etch recipe were carried out by adding argon to the gas mixture. The large size of the argon atom makes the etch much more kinetic in nature, compared to $SiCl_4$, which is mainly chemical. *Figure 3.7e* shows a SEM image of the etch profile for a hard mask etch with a gas mixture of 4 sccm of $SiCl_4$ and 2 sccm of Ar, with a chamber pressure of 1 mT, RF power of 150 W and an ICP coil power of 200 W. The etch profile in this case is much smoother than in the previous images and a vertical sidewall is also obtained. *Figure 3.7f* has the same vertical sidewall but with almost no surface roughness, this was achieved by adjusting the amount of $SiCl_4$ to 5 sccm, the chamber pressure to 2 mT and the ICP coil power 250W. Due to the quality of etch produced in *Figure 3.7f* these parameters were selected for use in the device processing.

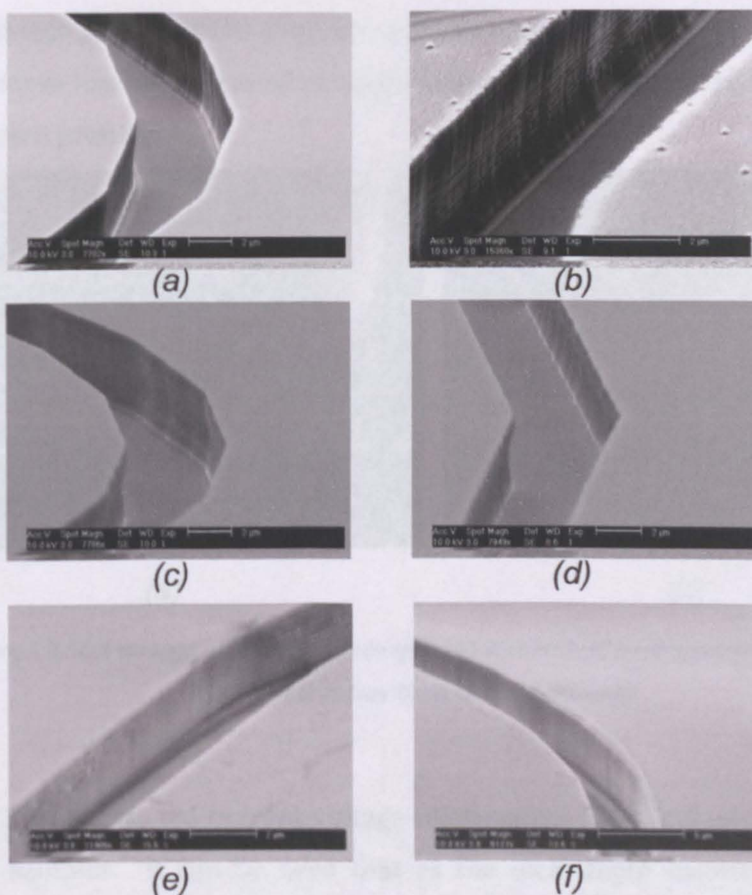


Figure 3.7 SEM images of ICP etch profile using a silicon dioxide hard mask with different etch parameters (a) $SiCl_4$ 500 W (b) $SiCl_4$ 600 W (c) $SiCl_4$ 700 W (d) $SiCl_4$ 800 W (e) $SiCl_4$ + Ar 200 W (f) $SiCl_4$ + Ar 250 W

3.4 Etch Depth

Etch depth is also an important consideration in the fabrication of the device, a shallow etch will allow for better heat dissipation. A deep etch will produce better carrier confinement, but in etching through the active region will result in surface recombination. To determine the optimum etch depth four samples were fabricated, sample A had no trench etch, sample B had a shallow etch of 2.2 µm, sample C had an etch depth of 4 µm and sample D had an etch depth of 6.3 µm. The samples were metalised with an Au/Zn/Au contact and then wet etched using 1:1:1 etchant, which gives a smooth etch profile. An InGe/Au contact was then blanket deposited on the back surface of the samples to finish the devices. *Figure 3.8* shows SEM images of the etch profile produced for sample C, the

smooth etch profile can be seen, but also the non-vertical nature of the etch. Part of the mesa has been cleaved through in this case in order to see a cross section of the etch profile.

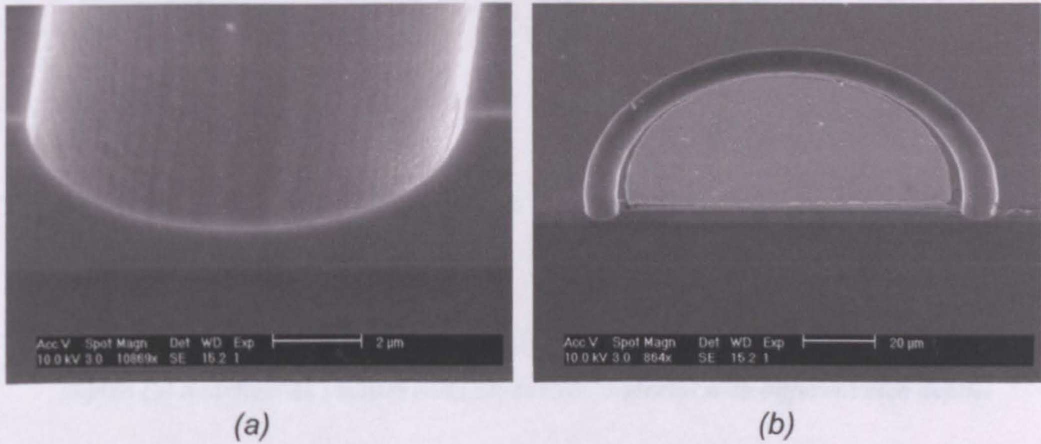


Figure 3.8 SEM images of trench etch profile (a) Wet etched trench profile (b) Contacted mesa that has been cleaved through

Figure 3.9a shows the current voltage relationship for a 300 µm device for each of the samples. It can be seen that as the etch depth increases the turn on current for each of the samples decreases, indicating that an increased device area is involved for the shallow etches and a large amount of current leakage. In the case of samples A and B their performance is almost identical. The slope of the line above turn on for each of the samples is almost the same, indicating very similar device resistances. This indicates that the lateral spreading resistance in the p-DBR is high, meaning the current is well confined under the contact. This is well supported by *Figure 3.9b*, which shows the normalised nearfield electroluminescence (EL) from a cross-section of a 300 µm device for each sample, where the width of EL is very similar in each case. Only the sample A, with no confinement etch has an intensity across a wider range. From the observed behaviour, the desired etch depth is somewhere between that of sample C and D, to a point just above the active region but not through it, ~5 µm.

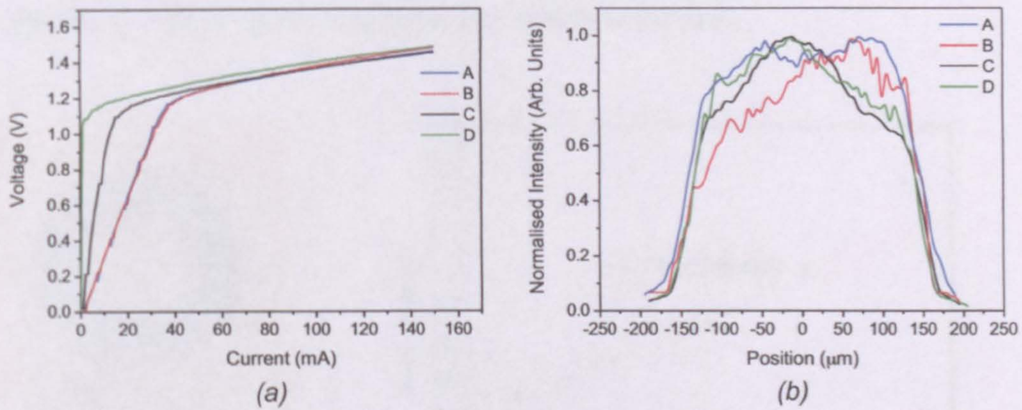


Figure 3.9 (a) Current voltage relationship for EP-VECSEL material with different etch depths (b) Nearfield EL profiles from EP-VECSEL material with different etch depths

3.5 Contact Metalisation

Due to the relatively high resistance nature of the EP-VECSEL devices, anything that could be done to reduce the resistance was carried out. To this end, the type of contact used, as well as its annealing temperature was investigated, in order to reduce the contact resistance. This was done by fabricating circular transmission line measurement (C-TLM) structures to measure the contact resistance [2], [3]. The C-TLM devices were produced using a one step photolithography, followed by metalisation of a specific contact type and a lift off process. The large sample was then split into smaller squares containing six patterns and each was annealed at a different temperature.

Figure 3.10a shows a schematic of the C-TLM structure, where the gap spacing *s* was varied with R_2 constant in each case. The resistance for each of the gap spacings was measured by placing a probe on the inner contact and another on the outside of the ring. The slope of the current voltage relationship in each case was taken to give the resistance; this was done using an HP4145a semiconductor parameter analyser. The lead resistance was also measured by short circuiting the probes, this value was then subtracted off the measured value to give the true resistance. Once all the gap spacings had been measured, their resistance as a function of gap spacing was plotted, shown in *Figure 3.10b* for a Au/Zn/Au

contact annealed at 320 °C. A line was then fit through the points to give the y-intercept, with this value being twice the contact resistance.

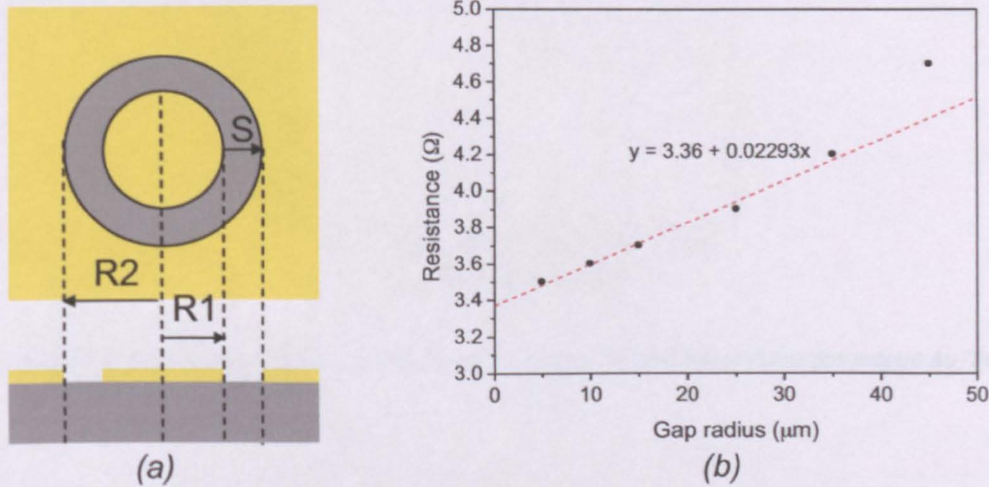


Figure 3.10 (a) Schematic of C-TLM pattern (b) Resistance as a function of gap radius for a Au/Zn/Au contact annealed at 320 °C

Figure 3.11 shows how the contact resistance of an Au/Zn/Au p-type contact varies with annealing temperature. It can be seen that the contact resistance decreases with increasing annealing temperature to minimum 360 °C, at which point a further increase in temperature results in an increase in resistance. This behaviour is attributed to the high mobility of the zinc, which at low temperature does not diffuse far enough through the structure to form a good contact. However at temperatures higher than 360 °C the zinc diffuses too far through the structure, leading to an increase in resistance. It is clear from *Figure 3.11* that a 360 °C annealing temperature is optimum for formation of a low resistance p-type contact.

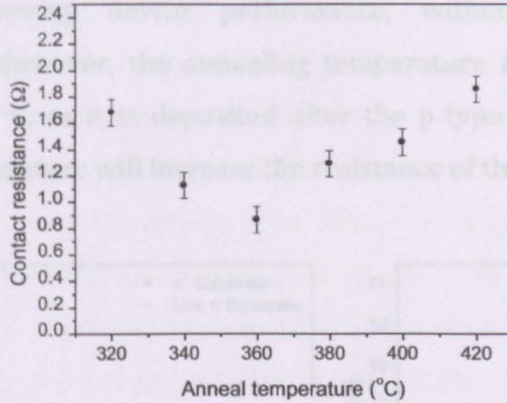


Figure 3.11 Contact resistance as a function of annealing temperature for p-type Au/Zn/Au contact

The same process was carried out for n-type contact resistance, however as EP-VECSELS were made on both n^+ and low n doped substrates; C-TLM patterns were fabricated on both substrates. In addition to that the samples were first lapped and polished, using the same method as described previously, so they had the same surface condition as in the real devices. Furthermore, some samples were deposited with a Ti/Au Schottky contact and the others with an InGe/Au n-type ohmic contact. All the samples were measured using the same method described above, and their contact resistance as a function of annealing temperature can be seen in *Figure 3.12a.*

Only the results for the InGe/Au contacts are shown in *Figure 3.12a*, as the doping level of the low doped substrate lead to the undesirable formation of a Schottky barrier for the Ti/Au contact, as shown in *Figure 3.12b.* It can be seen in *Figure 3.12a* that the contact resistance decreases with increasing annealing temperature for both substrate dopings. Contacts formed on the n^+ doped wafer, as expected, have a lower resistance than those of the low doped wafer, although this difference decreases with increasing annealing temperature, almost converging at high temperature. The absolute value of contact resistance achieved is lower than that of the p-side contact. The ability to form low resistance contacts on the low doped wafer, comparable to that of the n^+ doped

wafer, is important as the lower doping level will reduce the absorption of the substrate improving device performance, without sacrificing electrical performance. However, the annealing temperature for the n-type contact is limited to 360 °C, as it is deposited after the p-type contact, any increase in annealing temperature will increase the resistance of the p-type contact.

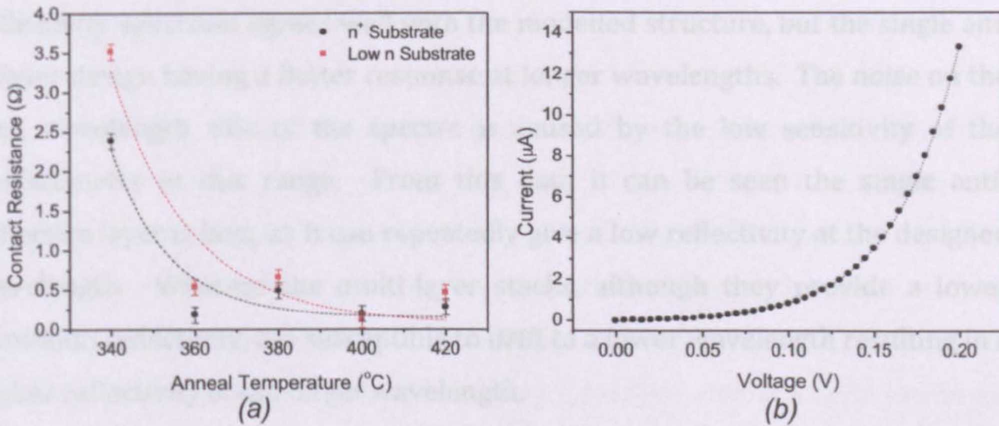


Figure 3.12 (a) Contact resistance as a function of anneal temperature for a n-type InGe/Au contact on n^+ and n doped substrates (b) Current voltage relationship for a Ti/Au contact annealed at 380 °C

3.6 Fabrication of Anti-Reflective Coating

The designs for single and multi-layer anti-reflective coatings proposed in chapter 2 were fabricated to see if their performance matched with that proposed. In order to deposit the correct thicknesses of each material, a piece of silicon substrate was placed in the PECVD and the deposition programs for silicon dioxide and silicon nitride were run for 2 minutes 30 seconds and 5 minutes respectively. The thickness of the layers deposited on each sample was then measured using an ellipsometer, from these measurements the etch rate for each process could be calculated. The single, dual and four layer AR designs were then grown on pieces of silicon substrate. The samples were measured using a white light source and a spectrometer, with their normalised reflectivity spectrums shown in *Figure 3.13a*. The spectrums were normalised, as the spectrometer could not accurately measure such low reflectivity values. The minima for the single layer is positioned as designed at 980 nm, whereas the

multi-layer designs have shifted to shorter wavelengths. This is caused by deposition of layers thicker than specified, due to a drift in chamber temperature during the gas switchover process.

Figure 3.13b shows the modelled reflectivity spectrums produced in chapter 2, to allow comparison to the grown structures. In each case the shape of the reflectivity spectrum agrees well with the modelled structure, but the single and 2-layer design having a flatter response at longer wavelengths. The noise on the long wavelength side of the spectra is caused by the low sensitivity of the spectrometer in this range. From this data it can be seen the single anti-reflective layer is best, as it can repeatedly give a low reflectivity at the designed wavelength. Whereas the multi-layer stacks, although they provide a lower minimum reflectivity, are susceptible to drift to a lower wavelength resulting in a higher reflectivity at the target wavelength.

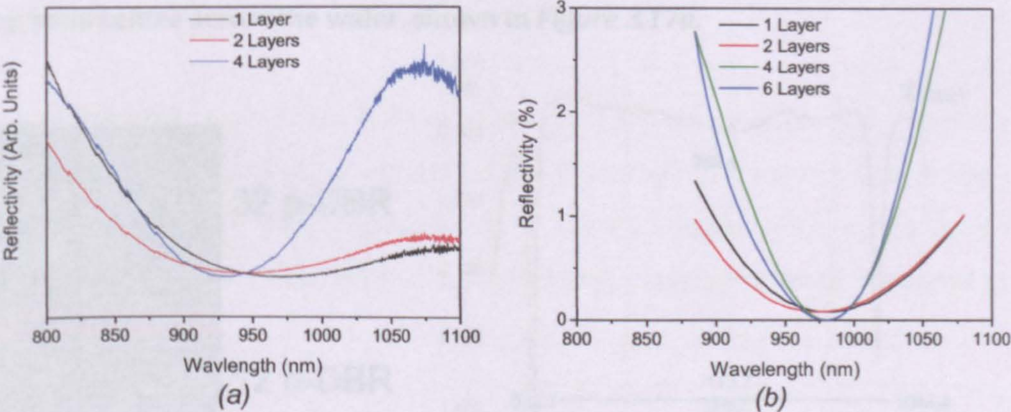


Figure 3.13 (a) Measured reflectivity for different anti-reflective layer coating designs (b) Modeled reflectivity for different anti-reflective layer coating designs

3.7 Characterisation of Detuning

Detuning is the act of blue shifting the gain peak with respect to the cavity resonance position, in order to counteract the thermal shift caused by device self heating, discussed further in chapter 2. The amount of detuning in a device is therefore an important parameter in determining device performance, where a small detuning will result in low threshold operation and a large amount of

detuning will allow for a larger device operating range before thermal rollover[4]. The amount of detuning is fixed by the epitaxial design, however due to variation in layer thicknesses across the wafer during the growth process; the amount of detuning can vary spatially across the wafer. Non-destructive methods such as photo-reflectance [5] have been proposed, but requires cryogenic cooling. Below a method for determining the amount of detuning across the wafer is described.

The first step in the process is to map the DBR reflectivity across the entire wafer; this is carried out by placing the wafer in the RPM 300 reflectivity and photoluminescence kit. *Figure 3.14* shows an illustration on the epitaxial structure measured as well as a snap shot of the reflectivity spectrum measured by the machine. Due to the highly reflective p-DBR the cavity resonance cannot be seen. Computer software on the machine determines the stopband centre for the reflectivity spectrum and uses this to produce a colour map of the variation stop band centre across the wafer, shown in *Figure 3.17a*.

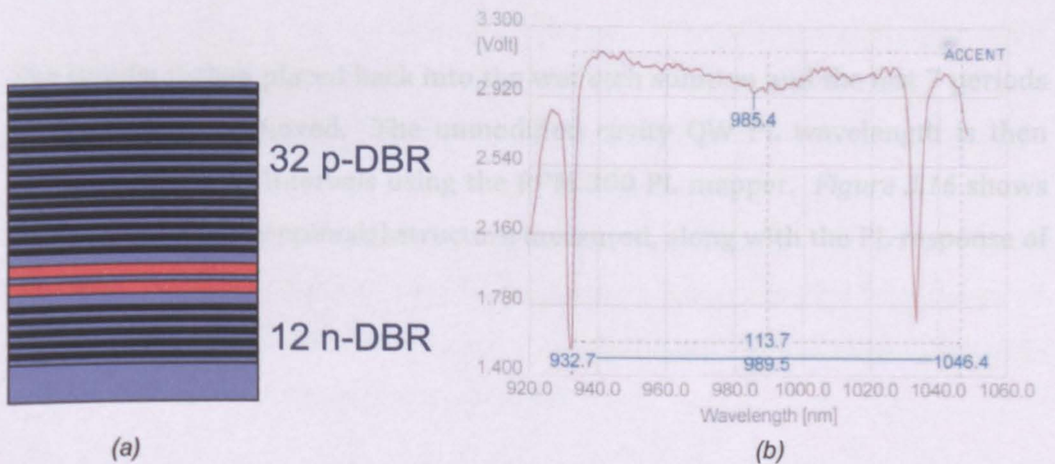


Figure 3.14 (a) Diagram of measured epitaxial structure (b) Reflectivity of unetched EP-VECSEL epitaxial structure

The next step is to cleave a 3 mm wide section out of the middle of the wafer using the scribe and break machine. This sample is then placed into the RPM 300 and the reflectivity band centre is measured at 1 mm intervals along its length. This 3 mm wide strip is then wet etched, using a solution of sulfuric acid and hydrogen peroxide, to remove 25 DBR periods. The etched sample is then

placed back into the RPM 300 and the now visible cavity resonance position is measured at 1 mm intervals along the sample length. *Figure 3.15* illustrates the measured epitaxial structure, along with the reflectivity spectrum at a given position.

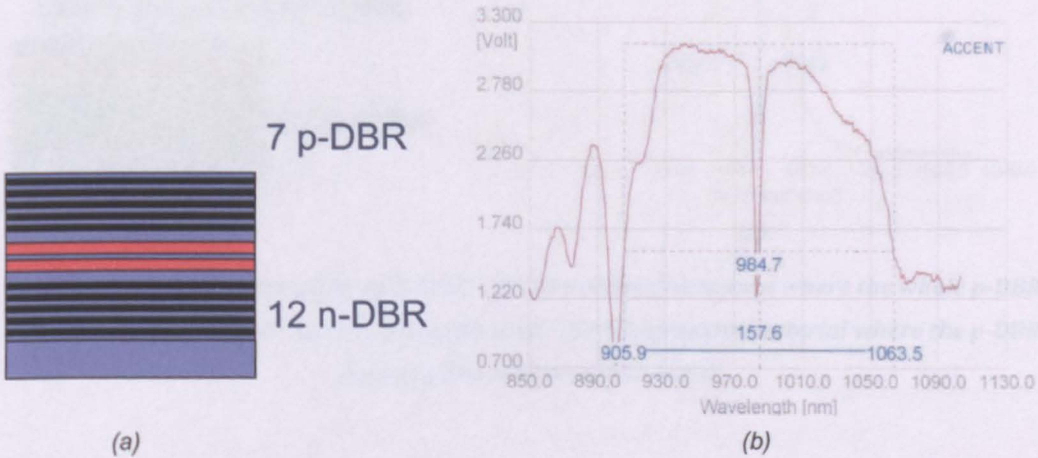
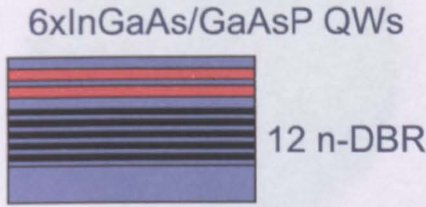
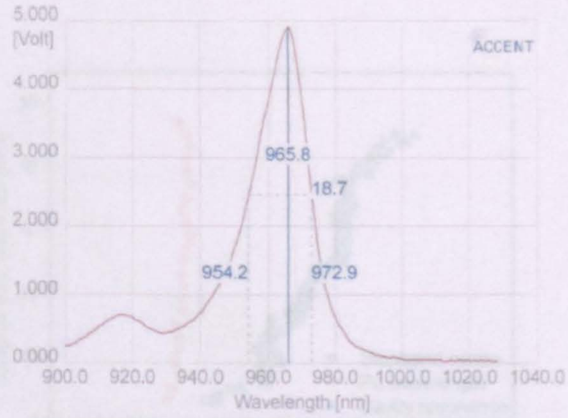


Figure 3.15 (a) Diagram of etched EP-VECSEL epitaxial structure where most of the p-DBR has been removed (b) Measured reflectivity of the etched EP-VECSEL epitaxial structure shown in (a)

The sample is then placed back into the wet etch solution and the last 7 periods of the DBR are removed. The unmodified cavity QW PL wavelength is then measured at 2 mm intervals using the RPM 300 PL mapper. *Figure 3.16* shows an illustration of the epitaxial structure measured, along with the PL response of the QWs.



(a)



(b)

Figure 3.16 (a) Diagram of the etched EP-VECSEL epitaxial structure where the whole p-DBR has been removed (b) PL spectrum of QWs in EP-VECSEL epitaxial material where the p-DBR has been removed as shown in (a)

The reflectivity and PL measurements taken along the length of the strip were then plotted on the same graph as a function of position; this can be seen in *Figure 3.17b*. In the figure it can be seen that the PL wavelength is almost constant across the measured section. Whereas, both the spectral position of the cavity resonance and stopband centre are red shifted with increasing distance from the major flat. The separation between the PL and reflectivity curves give the value of detuning for the relative position on the strip measured. It can also be seen that the reflectivity values can be closely correlated, inferring that the cavity resonance is usually at the stopband centre. Using the data from the graph along with the reflectivity colour map, shown in *Figure 3.17a*, a value of detuning can be obtained for a point across the wafer.

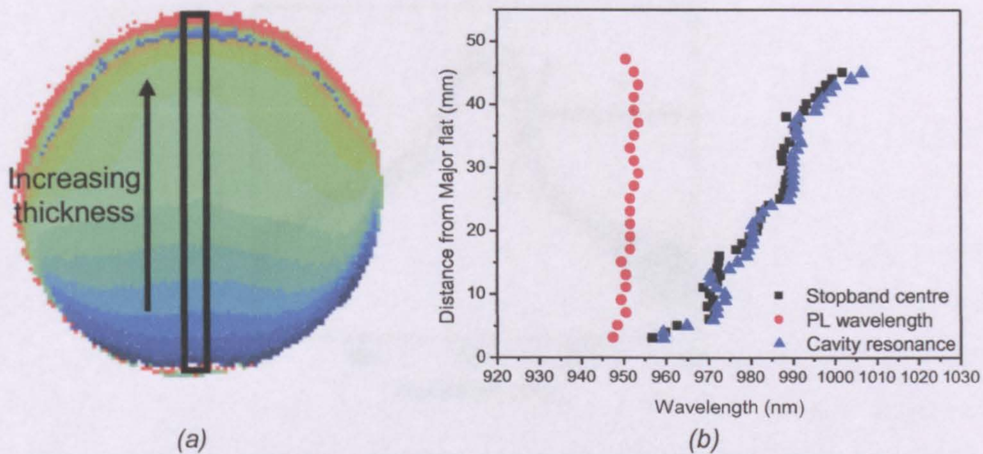


Figure 3.17 (a) Measured reflectivity colour map of an unetched EP-VECSEL wafer with cleaved region marked in black (b) Measured PL, cavity resonance and DBR stopband centre spectral position as a function of distance from the major flat

However, when measuring a 100 µm wide, 1 mm long, broad area laser made from EP-VECSEL material a discrepancy was noted. Under pulsed operation, using an ILX pulsed laser diode driver, with a 5 µs pulse width and a 1% duty cycle, the lasing wavelength was higher than expected. The lasing spectrum can be seen in *Figure 3.18* for a range of different drive currents. The position of the lasing peak is at ~ 971 nm, whereas the measured PL peak for this sample was at 958 nm, resulting in a 13 nm difference. Since broad area lasers always lase from the point of peak gain and the pulsed operation significantly reducing the thermal effects, it is suggested that there is an offset of the gain peak and the PL peak. It is proposed by *Ghosh et al.* [6], that this redshift in the spectrum is a result of reabsorption of the photons as a result of the much larger cavity length in the edge-emitting device. They reported a difference of up to 8 nm for different device designs when comparing VCSELs and edge emitters with the same active region layer structure. In addition, no intentional detuning was used in their VCSEL structures. The length of the edge emitters in the reported case was 5 mm, taking these factors into account, it is suggested that the reabsorption affect explains the red shift in emission wavelength.

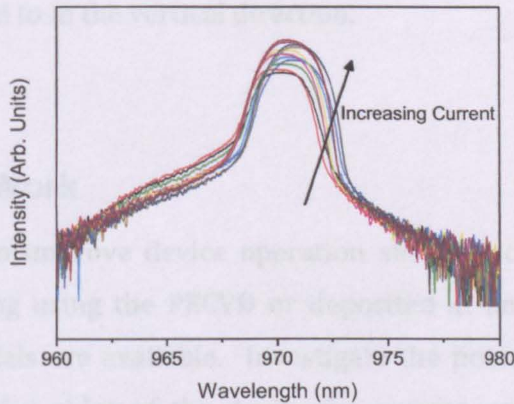


Figure 3.18 Lasing spectra at different pulsed injection currents for a broad area edge emitting laser with a 100 μm ridge with and a 1 mm cavity length

3.8 Conclusion

In this chapter a method by which EP-VECSELs are fabricated has been described, where the use of a silicon dioxide hard mask with an argon: silicon tetrachloride plasma can give a very smooth and straight sidewall etch profile. The desired etch depth was determined to be just above the active region to improve carrier confinement. In order to reduce contact resistance, the optimum annealing temperature was determined to be 360 °C for a p-type Au/Zn/Au ohmic contact, with the n-type InGe/Au contact resistance reducing further with increasing temperature. The annealing temperature for both contacts was limited to 360 °C, as a temperature increase would degrade the performance of the p-type contact.

Tests performed to determine the optimum anti-reflective coating design indicated that a single layer was most suitable, as more complex designs were susceptible to a wavelength shift of the minima. A method for determining the detuning of any point on an EP-VECSEL wafer has been described, with additional experiments showing that there is an offset between the cavity unmodified PL measured in the vertical direction and EL from an edge emitting laser made from the same material of ~ 13 nm, this is attributed to reabsorption

of photons in active region of the edge emitter due to the much larger cavity length compared to in the vertical direction.

3.9 Further Work

Further work to improve device operation should include, an improved anti-reflective coating using the PECVD or deposited at an external facility, where different materials are available. Investigate the potential of ion implantation into both p and n sides of the device for current confinement. Explore the potential of placing an oxide aperture into the device for current confinement. In addition, further work can be carried out on the electrical contacts to reduce their resistance by using different combinations of metals and layer thicknesses.

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4 Device Characterisation

4.1 Introduction

In this chapter experimental device performance will be discussed. Firstly, the epitaxial structure of the devices characterised in this chapter will be described. Then a method for determining the gain-current characteristic will be presented, where the reflectivity of the output coupler was changed, varying the mirror loss in the device altering the threshold current as a result. Using this method the effect of substrate doping on device performance will be presented, where the thinned substrate is used as a current spreading layer and therefore different doping levels will bring about different levels of free carrier absorption. The magnitude of the absorption coefficient will have an affect on device performance, with increased doping levels leading to increased optical absorption in the device. The increased loss will cause an increase in threshold current for the device, resulting in a reduced output power. Furthermore, the electrical properties of the two different substrate dopings will be investigated, where there is negligible difference in carrier transport in the two substrates and only little difference in the resistance. As a result lower doped substrates offer performance advantages over higher doped equivalents. Further discussion of doping induced optical loss in parts of the EP-VECSEL structure is presented in chapter 5. The optical loss resulting from the substrate can be offset by improvements in the gain characteristics of the active region, which are discussed further in chapter 6.

Next, the beam quality of the devices will be examined. Achieving high beam quality (low M^2) simultaneously is desirable for mode locking and second harmonic generation. In the devices measured low M^2 values were obtained only at low output powers (1-5 mW), with multimode behaviour present above these

levels. Additionally, an analysis of the power scaling properties of the devices will be presented. As a high output power is desired from these devices, power scaling is important, as it allows the size of the device to be increased, resulting in an increased output power. However, as the device size increases carrier diffusion becomes much more important, as the carriers are required to move further laterally in order to maintain a Gaussian distribution in the active region. Nearfield profiling of the carrier distribution indicates that a Gaussian profile is not maintained for device diameters greater than 70 µm. A result of this distribution is the non-linear scaling of power and efficiency with device area.

Finally, a method for calculating the thermal resistance of the device will be described. Whereby, the thermal resistance reduces with increasing device diameter. The thermal resistance of the device is crucial, as a lower thermal resistance will allow for a higher injection current to be reached before thermal rollover occurs, enabling a higher output power to be produced. Furthermore, the electrical power density (electrical power- optical power) will be examined, with this value decreasing with increasing device area. A reduction in this value will reduce device self-heating allowing for greater output powers to be obtained.

4.2 Epitaxial Structure

Figure 4.1a shows a schematic of the epi-down, substrate emitting device design. It consists (bottom of figure to top) of a lower metallised region with a circular Au/Zn/Au contact (diameter D), p-DBR, 980nm $InGaAs/GaAs_{0.9}P_{0.1}$ QW active region, n-DBR, substrate current spreading region (thickness T) and a top contact with a Si_3N_4 $\lambda/4$ antireflective window. The fabrication of this device is discussed in chapter 3. The device is of substrate emission geometry with the epitaxial layers being face down in the schematic. Lasing is achieved from the device by aligning a collimating lens and these elements also maintain beam quality in devices greater than a few microns in diameter.

The DBRs consist of alternating layers of $Al_{0.8}Ga_{0.2}As$ and GaAs in order to

achieve high contrast and high reliability and allow future integration of high Al layers for oxide apertures. The $Al_{0.8}Ga_{0.2}As$/GaAs interfaces are graded to reduce series resistance, by using a single 10 nm $Al_{0.47}Ga_{0.53}As$ grading layer [1-3]. A more detailed discussion of DBR grading is given in chapter 5. The epitaxy was started by depositing 400 nm of n+ GaAs on the n-doped substrate, this was followed by a 12 period n-DBR made up from 60 nm GaAs and 74 nm $Al_{0.8}Ga_{0.2}As$ with a 10 nm $Al_{0.47}Ga_{0.53}As$ grading layer in between, this was doped with silicon to a density of $2x10^{18}$ cm^{-3}. The overall reflectivity of this structure was ~ 90 % to allow light to be coupled into the external cavity.

The active region, shown in *Figure 4.1b*, consisted of a 3 λ /2 cavity, with 6 QWs separated into two groups of three, placed at the antinodes of the standing wave for RPG enhancement as described in chapter 2. The active region started with 108 nm of undoped GaAs, followed by 15 nm of $GaAs_{0.9}P_{0.1}$ for strain compensation, then 3 x 8 nm $In_{0.17}Ga_{0.83}As$ quantum wells separated by 9 nm $GaAs_{0.9}P_{0.1}$ barriers. Then an undoped 68 nm GaAs spacer layer sandwiched between two 15 nm $GaAs_{0.9}P_{0.1}$ layers, followed by 3 more 8 nm $In_{0.17}Ga_{0.83}As$ quantum wells separated by 9 nm $GaAs_{0.9}P_{0.1}$ barriers. The active region was finished with another 15 nm $GaAs_{0.9}P_{0.1}$ layer followed by 108 nm of undoped GaAs. The p-DBR structure is identical to the n-DBR but contained 32 mirror pairs (R~ 0.9995) and is carbon doped at a density of $2x10^{18}$ cm^{-3}. The structure was terminated with a 200 nm GaAs cap doped to $1x10^{19}$ cm^{-3} to form a good electrical contact. A layer structure for this growth run (TS522) can be found in appendix A.

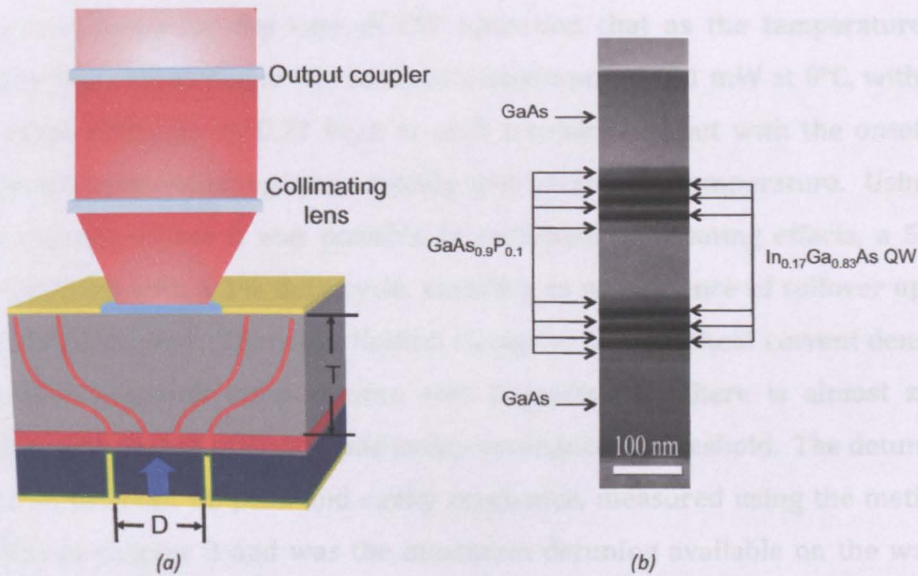

Figure 4.1 (a) Schematic of EP-VECSEL device with external cavity optics (b) TEM of EP-VECSEL device active region with 2 x 3 QWs

4.3 Device Testing

Fabricated devices were mounted onto tiles, as described in chapter 3, and their CW output power and spectra were measured as a function of current, temperature and output coupler. This was done by placing the device on a temperature controlled thermo electric cooler (TEC) and aligning it with a collimating lens, a x-y-z stage was used to adjust the position of the collimating lens until the peak spontaneous emission power was measured on the power meter. Once this was aligned, the output coupler was added to the set up and positioned so that the output spot was incident on the centre of the output coupler mirror. A current close the roll over of the device was injected and the mirror mount for the output coupler was adjusted until lasing was achieved indicated by a large change in the measured power. Further positional adjustments to the set up were made until a maximum power was reached. This process was then repeated for different device diameters and output coupler reflectivities.

Figure 4.2 shows the optical power-current dependence of a 100μm device, with a substrate doping of 4×10^{17} cm^{-3}, discussed in the next section, for a range of temperatures using an 84% reflectivity output coupler mirror. It can clearly be

seen in the figure for the case of CW operation that as the temperature is decreased the output power increases to a maximum of 131 mW at 0°C, with an initial slope efficiency of 0.27 W/A at each temperature but with the onset of thermal roll over occurring more rapidly with increasing temperature. Using a pulsed current source it was possible to minimise self-heating effects, a 5 μs pulse was used with a 1% duty cycle, resulting in no evidence of rollover up to 1A of applied current. There is a limited change in the threshold current density at different heat-sink temperatures, this suggests that there is almost zero detuning between the gain peak and cavity resonance at threshold. The detuning was 12nm between PL peak and cavity resonance, measured using the method described in chapter 3 and was the maximum detuning available on the wafer studied. However, through measurements of the threshold at different temperatures a value of 0 nm of detuning is present in this device. The inset to *Figure 4.2* shows the CW lasing spectra for the same 100 μm device operating at a current of 300 mA and a heatsink temperature of 20°C. The lasing peak is located at 981 nm, which is controlled by the cavity resonance position. This position shifts as the device heats up with increasing drive current. The rate of this shift (~0.07 nm/K) is less than that of PL peak (0.3 nm/K)[4], hence the need for detuning [5]. In addition to the reduction of gain due to the different rates of thermal shift, the optical loss also increases with temperature, further exacerbating the situation.

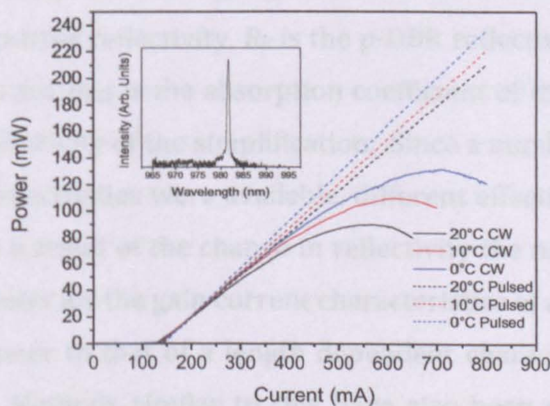

Figure 4.2 Output power as a function of CW (solid lines) and pulsed (dotted lines) current for a 100 μm device with an 84 % reflectivity output coupler mirror at different heatsink temperatures (Inset) Lasing spectrum at 300 mA CW for a 100 μm device operating at room temperature

4.4 Effect of Substrate Doping

The substrate plays an important role in overall device performance, it provides a large area for diffusion of carriers as well as contributing a significant proportion of optical loss to the overall device, and hence substrate doping and thickness are of critical importance. As seen in *Figure 4.1a* the light must pass twice through the substrate for a single cavity round trip, resulting in a large amount of free carrier absorption for a highly doped, thick substrate. This can be ameliorated by performing growth on substrates with a lower doping and reducing the thickness of this current spreading layer. However the reduction of doping level below a certain point can be expected to result in the formation of a poor electrical contact, increasing the overall device resistance. Therefore a study of the trade-off between substrate doping and electrical and optical properties of the device must be carried out. EP-VECSELs with a range of sizes between 30 µm and 150 µm were fabricated on substrates with Si n-type dopant concentrations of $2x10^{18}$ cm^{-3} and $4x10^{17}$ cm^{-3}.

As a VECSEL is a coupled cavity device working in a strong feedback regime [6], it is possible to simplify the system from a coupled cavity to a simple 2 mirror resonator, by combing the effect of the n-DBR and the output coupler mirror. *Figure 4.3* shows a schematic of the EP-VECSEL device with the key areas required for the simplification highlighted. R_n is the n-DBR reflectivity, R_{ext} is the output coupler mirror reflectivity, R_p is the p-DBR reflectivity and is assumed to be unity in this case. α_{sub} is the absorption coefficient of the substrate and R_{eff} is the resultant reflectivity of the simplification. Since a number of output couplers with different reflectivities were available, different effective reflectivities could be achieved. As a result of the change in reflectivity the mirror loss was also be changed, this allows for the gain current characteristics of a device to be derived, in a similar manner to that of a length dependent characterisation in an edge-emitting laser. Methods similar to this have also been carried out on VCSEL devices [7], [8] .

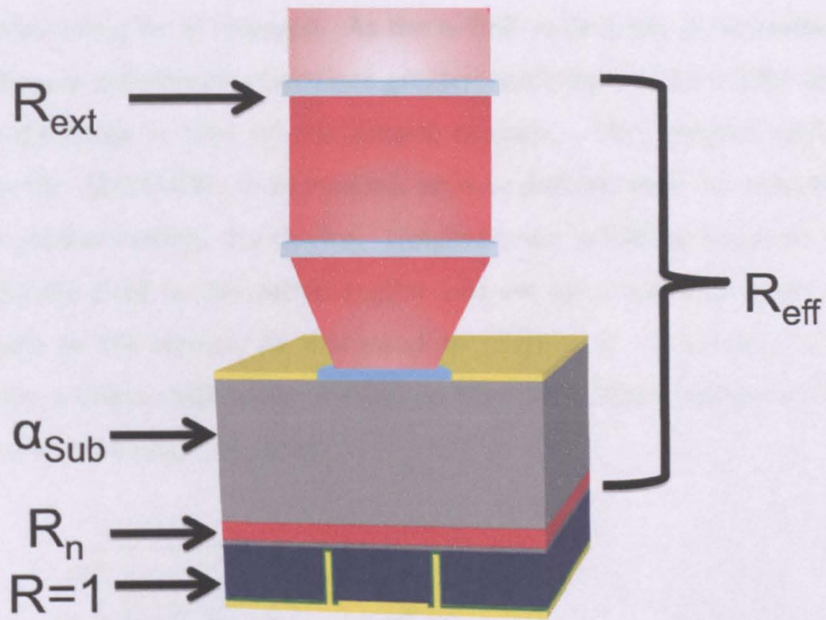

Figure 4.3 Schematic of an EP-VECSEL device with an external cavity, where the optical loss and reflectivities of certain regions are labeled

Equation *(4.1)* describes the calculation of the effective reflectivity, R_{eff}, of the compound mirror [9].

$$R_{eff} = \left(\sqrt{R_n} + \frac{T_n\sqrt{R_{ext}}}{1+\sqrt{R_n R_{ext}}}\right)^2 \tag{4.1}$$

Where R_n is the n-DBR reflectivity, R_{ext} is the output coupler mirror reflectivity and T_n is the n-DBR transmission, which can be adjusted to take into account the loss due to absorption in the substrate. In the analysis presented here, the sum of R_n and T_n is taken as unity, with deviations of the final gain-current density relationships being attributed to differences in substrate absorption, hence substrate absorption is not included in this calculation.

Figure 4.4 plots the effective reflectivity, R_{eff}, as a function of the output coupler reflectivity, R_{ext}, for different n-DBR reflectivities, R_n. As described above, the sum of R_n and T_n is unity in each case. The values of external reflectivity correspond to the reflectivity at 980 nm for the different output couplers used. For high values of n-DBR reflectivity, R_n, the change in the effective reflectivity is

small as the output coupler is changed. As the n-DBR reflectivity is decreased, the range of effective reflectivities becomes greater, until there is no n-DBR and the effective reflectivity is that of the output coupler. The coupled cavity arrangement in the EP-VECSEL is unwanted, as it is desired that the external output coupler mirror control the device. However, the n-DBR is required to enhance the electric field in the active region and set up a standing wave to improve the gain in the device, as discussed in chapter 2. Therefore, it is desirable to have a lower reflectivity n-DBR, so that the output coupler is the dominant element in the coupled cavity.

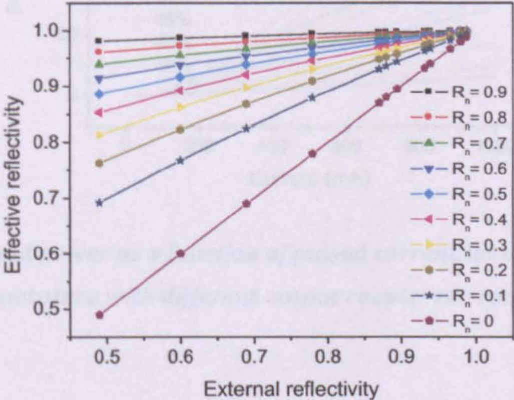

Figure 4.4 Calculated effective reflectivity of the coupled cavity as a function of output coupler reflectivity for different intermediate n-DBR reflectivities

In order to obtain the current-gain characteristic of a device, the output power-current relationship was measured for a number of different output coupler mirrors. *Figure 4.5* shows the output power from a 100μm device for a pulsed current input, with a substrate doping of 4×10^{17} cm^{-3}, operating at room temperature as a function of drive current for a range of different output coupler mirror reflectivities. As the reflectivity of the output coupler mirror reflectivity decreases from an initial value of 99% to 49% the slope efficiency of the device increases from 0.017 W/A to a maximum value 0.24 W/A and then decreases to 0.19 W/A. This increase in slope efficiency coincides with an increase in threshold current, starting at a minimum of 82 mA for a 99% output coupler reflectivity and ending at 290 mA for a 49% output coupler mirror. Additional

mirrors of lower reflectivities were tried, however no lasing was observed. A maximum output power of 227 mW was obtained at 1 A, limited by the pulsed current source, for an output coupler mirror reflectivity of 69%. The kinks in the L-I for the lower reflectivity output couplers are suggestive of mode hopping during device operation.

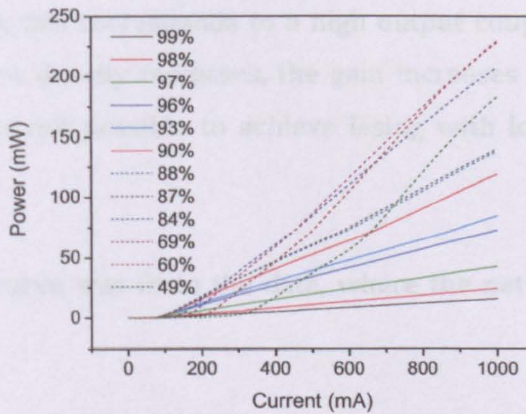

Figure 4.5 Output power as a function of pulsed current for a 100 μm device at room temperature with different output coupler mirror reflectivities

From the data displayed in *Figure 4.5* the threshold current density can be derived for each output coupler mirror. Using the calculated value for effective reflectivity (R_{eff}), along with the threshold current density value for each output coupler a current-gain relationship can be constructed [25], using the relationship described in equation *(4.2)*,

$$g_{sp} = \left(\sqrt{\frac{1}{R_p R_{eff}}} - 1\right) \times 100 \qquad (4.2)$$

Where g_{sp} is the net single pass gain, R_p is the p-DBR reflectivity and R_{eff} is the calculated effective reflectivity from equation *(4.1)*.

In order to examine the affect of different substrate doping levels on the device performance, the output coupler characterisation was carried out on devices with two different substrate dopings. *Figure 4.6* plots the single pass gain

(pulsed) for two 100 μm devices with the same detuning but different substrate dopings of $2x10^{18}$ cm^{-3} (circles) and $4x10^{17}$ cm^{-3} (squares), where it has been assumed that there is no other internal loss in the device and the reflectivity of the p-DBR is unity and that the collimating lens in the external cavity contributes no additional loss to the device. In both cases the current-gain curves have the same shape, but are offset from each other. At low current densities the single pass gain is low, this corresponds to a high output coupler reflectivity. As the threshold current density increases, the gain increases to ~ 3.5 $kAcm^{-2}$, above this point it was not possible to achieve lasing with lower reflectivity output coupler mirrors.

In each case a curve was fit to the data, where the net single pass gain, g_{sp}, is given by:

$$g_{sp} = g_0 \ln\left(\frac{J}{J_0}\right) \tag{4.3}$$

where g_0 is the gain coefficient, J is the current density and J_0 is the transparency current. The fitted curves are empirical fits for a QW gain medium [26], where only the transparency current (J_0), and the current density required to over come internal loss in each device was modified. A constant gain coefficient (g_0) was applied, as the device active region was assumed to be identical in both cases. A good fit to the data was obtained in both cases. As expected, the devices with a lower doped substrate demonstrate lower internal loss. Recasting *Figure 4.6* in terms of a gain coefficient in reciprocal length, an offset of 5±1cm^{-1} for the two sets of devices was obtained. This value for the additional internal loss introduced with the higher substrate doping is in good agreement with absorption measurements for n-doped GaAs [10].

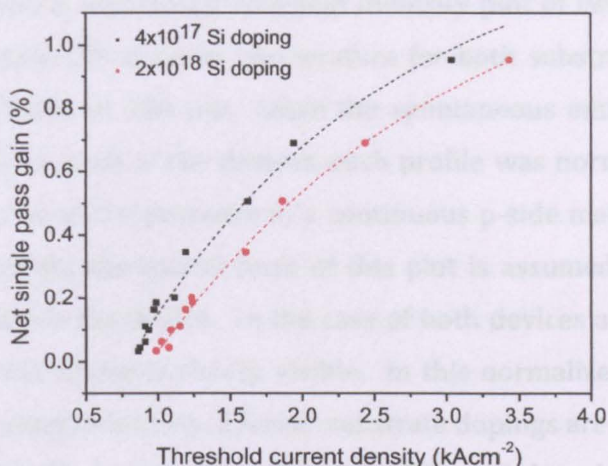

Figure 4.6 Net single pass gain in a 100 µm device with different substrate dopings as a function of threshold current density (pulsed)

In addition to substrate optical loss the electrical operation of the device is of key importance, with the substrate doping level affecting overall device resistance as well as the current spreading performance of the device. Along with examining the optical performance of the devices with different substrate dopings, the electrical performance was also investigated. This was carried out in two ways, firstly by comparison of the near-field profile of EL from the devices with no output coupler mirror, and secondly by comparing device series resistance. Both 150µm devices exhibit similar series resistance of 4.6 Ω for a substrate doping of $4x10^{17}$ cm^{-3} and 4.2 Ω for a substrate doping of $2x10^{18}$ cm^{-3} measured at a current density of 4.5 kA/cm^2 using a two probe measurement.

In order to obtain the nearfield profile from the devices they were placed in a jig and clamped to a stand. A high precision computer controlled x-y-z stage with pitch, yaw and roll was used to scan a lensed optical fibre across the device. The device was driven by a CW current source at a current of 300 mA, with no output coupler mirror in the set up, so only spontaneous emission was captured by the fibre. The intensity of the emission captured at each point was measured by a power meter and logged with the position on the computer. The lensed fibre had a spatial resolution of 2 µm and was scanned across the device at 5 µm intervals.

Figure 4.7 shows a normalized nearfield intensity plot of two 150 µm diameter devices operating CW at room temperature for both substrate dopings, with a substrate thickness of 100 µm. Since the spontaneous emission power levels were different for each of the devices, each profile was normalised to allow for comparison. Due to the presence of a continuous p-side metal contact between the isolated region, the spatial form of this plot is assumed to be the electron distribution within the device. In the case of both devices a dip in EL power at the centre of the device is clearly visible. In this normalized plot, the electron distributions using these two different substrate dopings are very similar, with a slightly greater dip in the case of the $4x10^{17}$ cm^{-3} doped device. This is in keeping with the expected behavior, as the lower doping will result in a greater lateral resistance resulting in fewer electrons diffusing to the centre and hence a lower intensity in the centre of the device. However, this difference is not significant, as there is only ~ 3 % difference in the value of the intensity at the centre and the experimental error in this case is ~ 5 %. The step at the edges shows the position of the window in the top contact, which was 50 µm larger than the p side electrical isolation trench etch. The variation in intensity of this step is attributed to etch depth variations across the wafer, which was exacerbated by the normalization process. The sharp rise in emission indicates that the lateral spreading of holes is negligible due to the trench-etch stopping at the active region. The central dip however, indicates a limit to diffusion of electrons as they pass through the substrate and n-DBR.

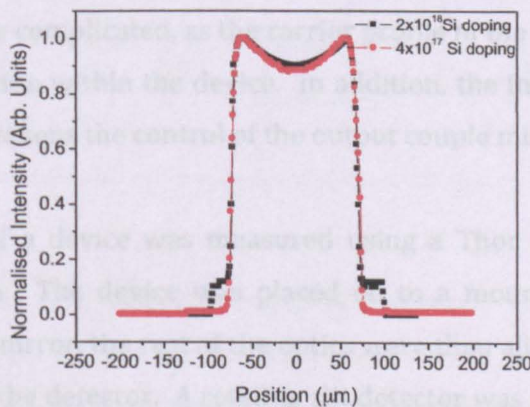

Figure 4.7 Normalised nearfield EL profile for a 100 µm device with different substrate dopings

Since there is no significant difference between the high and mid-doped substrates in terms of spatial EL intensity profile it can be inferred that the diffusion occurs primarily at the many hetero-interfaces in the n-DBR, where the interface barriers promote lateral diffusion, rather than in the substrate. This may cease to be the case when n-DBR pairs are further reduced, for example in mode-locking applications. Considering the similarity of the current spreading properties for the two substrate dopings, no significant increase in device resistance, yet significantly reduced gain at a given current due to increased optical loss, a lower substrate doping is highlighted as beneficial for obtaining improved device performance. A further discussion of current spreading and substrate doping is presented in chapter 5.

4.5 Beam Quality

Beams with a high quality (low M^2) are a highly desirable property for laser devices. A value of M^2 for a particular device indicates how much the beam deviates from an ideal Hermite-Gaussian TEM_{00}, which would have an M^2 of 1. This single mode operation is important because it allows for efficient coupling to single mode optical fibres. In addition, the beam can be tightly focused without the need for expensive optics, with this tight focus enabling efficient non-linear processes to be carried out [11]. In OP-VECSELs, single mode operation is controlled by the output coupler mirror, where the pump spot size is matched to the fundamental transverse mode size [12]. In an EP-VECSEL the situation is more complicated, as the carrier profile in the active region is defined by carrier diffusion within the device. In addition, the intermediate DBR within the structure weakens the control of the output couple mirror on the device.

The M^2 value of a device was measured using a Thor Labs M^2 Beam Quality Analysis System. The device was placed on to a mount and aligned with an output coupler mirror, the rest of the optics were then aligned so that the output was centred on the detector. A rotating slit detector was then moved backwards along a track and a computer logged the beam width as a function of detector

position. Since the final optical element before the detector is a lens of known focal length the system can then calculate the M^2 from the equation below [12]:

$$W_{00} = M^2 \frac{4\lambda f}{\pi W_0} \tag{4.4}$$

where, λ is the emission wavelength, f is the focal length of the lens, W_0 is the measured beam radius and W_{00} is the idealized focused spot diameter. Computer software then fits its model to the measured data and produces an M^2 value.

Figure 4.8 shows the measured beam width as a function of detector position for both the horizontal and vertical directions. The device in this case was a 150 μm in diameter with a 4×10^{17} cm^{-3} doped substrate, emitting 5mW of CW power at room temperature through a 90% output coupler mirror. The measured value of M^2 in this case was 1.2, which is very close to the ideal value of 1.

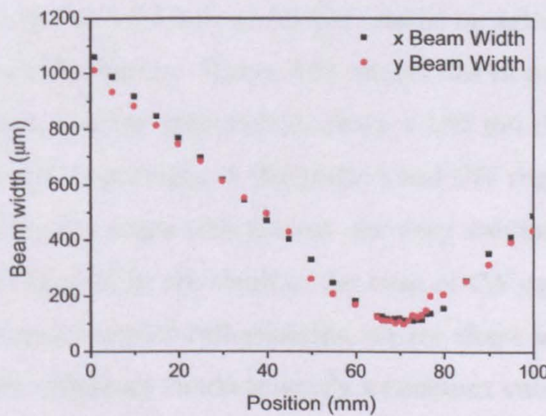

Figure 4.8 Measured beam width as a function of position for a 150 μm device (M^2 =1.2)

The devices were measured at a number of different output powers, with the M^2 increasing dramatically with increasing output power for all the different device diameters measured. Furthermore, changing the distance between the device and the output coupler in the system varied the range of M^2 values obtained. As a result, it was not possible to observe any trends in the devices apart from

degradation in beam quality with increasing output power. It is suggested that high beam quality can be maintained at high output powers by improving the carrier profile within the devices, discussed further in chapter 5, and reducing the reflectivity of the intermediate n-DBR to a value of 80% [13], to allow more control by the output coupler mirror.

4.6 Power Scaling

For many applications, the maximum possible CW output power is a key parameter. In the ideal limit with heat extraction being entirely one dimensional, perfect current spreading, and high optical-electrical conversion efficiency an increase in device size coincides with an increase in power. However, the practical limits of power scaling need to be explored. In this section several device characteristics will be examined as a function of area.

As seen in the previous section the device performance changes depending on the reflectivity of the output coupler used, it was important to understand this behavior so that the correct output coupler could be selected to obtain the best performance from the device. *Figure 4.9a* shows the slope efficiency for a range of different output coupler reflectivities from a 100 μm device with a substrate doping of $4x10^{17}$ cm^{-3} operating in the pulsed and CW regimes. For high output coupler reflectivity the slope efficiencies are very similar, suggesting that self-heating effects at threshold are small in the case of CW operation. In the pulsed case at lower output coupler reflectivities, where there was a higher threshold current, the slope efficiency tends towards a constant value. In the CW case the slope efficiency reduces rapidly beyond the maximum. This was attributed to the effects of self-heating, where the increasingly high threshold current causes heating within the device that drives that gain peak past the cavity resonance position leading to in efficient operation. When operated CW a maximum slope efficiency of ~ 0.26 W/A is achieved using a 70 % reflectivity output coupler mirror, whereas a maximum of ~ 0.28 W/A is obtained for a 60 % reflectivity output coupler in the pulsed case.

Next, the maximum output power was examined as a function of output coupler reflectivity. *Figure 4.9b* plots the output power obtained at 1A (pulsed) and the maximum CW power at thermally induced roll-over as a function of output coupler for the same device as described above. In the case of pulsed operation the power is limited by threshold and internal efficiency of the epitaxial material, whilst self-heating effects play a large role under CW operation. At high output coupler reflectivities the difference in power between the two cases is small, as it is limited by the transmission of the output coupler, as shown in *Figure 4.9a*. However, at lower reflectivities where the transmission is higher, the maximum output in the CW driven devices are inhibited by the thermal rollover. Whereas, in the pulsed case they are not, leading to a much higher maximum power. Additionally, for achieving maximum output power in the CW regime, there is competition between the improved slope efficiency achieved by reducing the output coupler reflectivity and the increased threshold current that it causes. The increased threshold current reduces the amount of current that can be injected before rollover, while the improved slope efficiency allows more output power to be generated per unit current injected. As the main interest of our work is CW device performance, the rest of the figures with regard to lasing were obtained using an 84% output coupler reflectivity, which is the output coupler that allows the highest CW power to be achieved, but does not produce the highest slope efficiency.

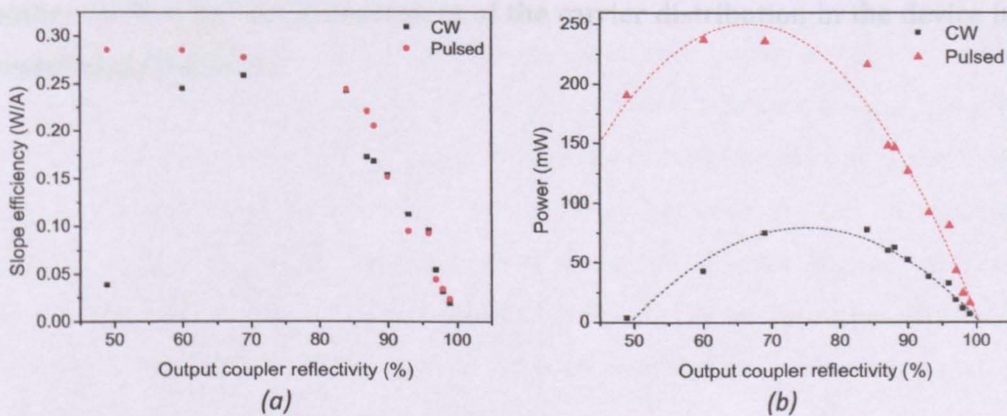

Figure 4.9 (a) Slope efficiency as a function of output coupler reflectivity for a 100 μm device with a substrate doping of 4x10^{17} cm^{-3} for both pulsed and CW operation (b) Output power

as a function of output coupler reflectivity for a 100 μm device with a substrate doping of $4x10^{17}$ cm^{-3} for both pulsed and CW operation

In order to for the devices to uniformly power scale with area the carrier distribution in devices of increasing diameter should be of the same form, deviations from this will result in a degradation in device performance. In order to examine this behavior nearfield profiling, as described previously, was carried out on a range of device diameters. *Figure 4.10* shows the normalised nearfield intensity distribution for a range of different device diameters with $4x10^{17}$ cm^{-3} doped substrates. As with the discussion of *Figure 4.7,* the continuous contact across the p-side mesa means that this was essentially a plot of the electron distribution. For the 30 μm diameter device a roughly Gaussian shaped EL distribution was observed, whilst for the 70 μm diameter device there was a flat topped EL distribution. This was suggestive of a uniform electron distribution across the active region of these devices. Device diameters of 100μm and greater exhibit a reduction in their EL intensity profile as the fibre was moved inwards to the centre of the device, suggesting non-ideal carrier distribution. This was because as the device diameter increases, the thickness of the current spreading layer (100 μm) becomes insufficient to allow electrons to diffuse far enough laterally into the centre of the device. This distribution could be improved in the larger devices by increasing the substrate thickness, however, this would come at the penalty of increasing the free carrier absorption loss. A discussion of another method for the improvement of the carrier distribution in the device is presented in chapter 5.

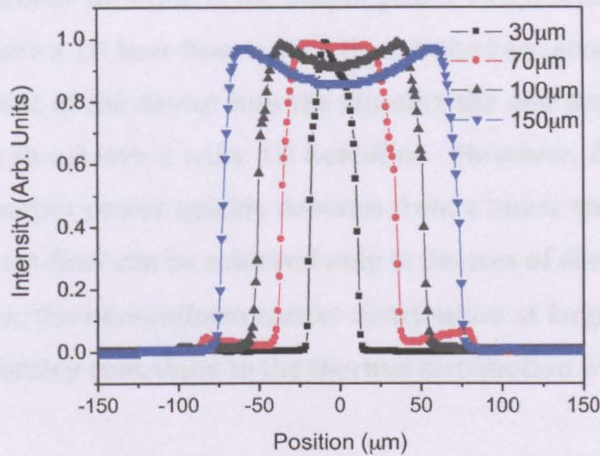

Figure 4.10 Normalised nearfield EL profile for a number of devices of different diameters and substrate doping of $4x10^{17}$ cm^{-3}

Since the carrier distribution deviates from the desired profile at larger device diameters, it was important to investigate how this will affect aspects of device performance. *Figure 4.11a* shows the slope efficiency of CW current driven devices as a function of area for the same devices measured in the previous figure, with an output coupler reflectivity of 84%. It was observed that the slope efficiency decreases as the area increases. If ideal power scaling properties were exhibited in these devices the slope efficiency would be constant for all areas. A deviation from this case further suggests non-uniform carrier distribution as device diameter is increased.

Figure 4.11b shows the scaling of maximum CW output power at roll over with device area, a maximum output power of 133 mW was achieved from a 150 μm diameter device, however a greater power density of 0.0169 mW/μm is obtained from a 100 μm diameter device. The similarity between the output powers obtained from the 100 and 150 μm devices is attributed to the higher roll over point in the 150 μm device, which allows for the deficit in the slope efficiency between the two device to be negated. In each case thermal rollover is a major limiting factor in the CW output of the device.

It is expected that for an idealized 1D heat-flow and optimum carrier

distribution, a linear variation of the output power as a function of area would be produced. Where a 1D heat-flow is such that all the heat generated in the device flows linearly out of the device into the alumina tile and into the heatsink, it is never possible to achieve a truly 1D heat-flow. However, from the figure it is seen that the output power quickly deviates from a linear trend, suggesting that a close to 1D heat-flow can be achieved only in devices of diameter less than 100 μm. In addition, the non-uniform carrier distribution at larger device diameters will also unfavorably contribute to the thermal distribution within the devices.

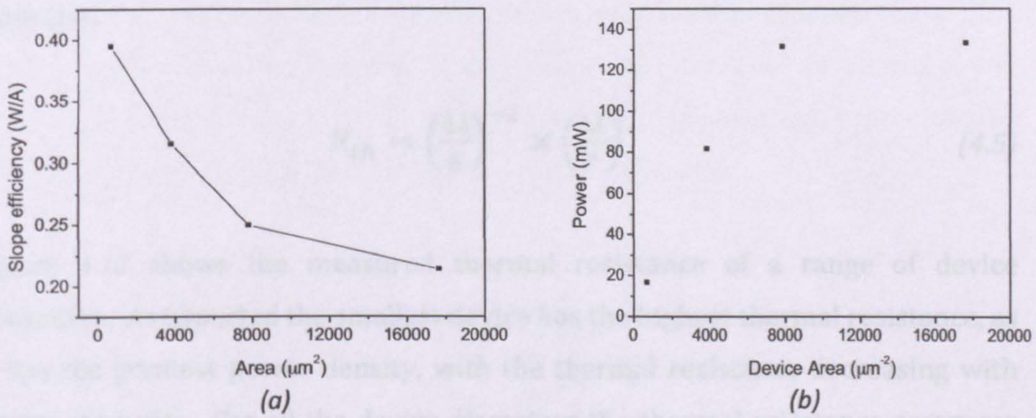

Figure 4.11 (a) CW slope efficiency as a function of device area for devices with a substrate doping of $4x10^{17}$ cm^{-3} at 0 °C (b) CW output power as a function of device area for devices with a substrate doping of $4x10^{17}$ cm^{-3} at 0 °C

4.7 Thermal Properties

As demonstrated in *Figure 4.2,* thermal performance is very important for achieving high device output powers, where being able to drive devices to a higher current before the onset of thermal rollover is a major limiting factor in achieving greater output power. The three main factors that limit this rollover point are device self-heating, gain detuning and heat sinking; a discussion of gain detuning is presented in chapter 2. These factors need to be carefully engineered to achieve optimum performance. The most important of these is self-heating within the device, namely electrical and thermal resistance, which can be controlled by careful design of the DBR by the use of interfacial layers, doping distributions and AlGaAs concentrations, discussed in chapter 5.

In order to measure the thermal resistance, R_{th}, of the devices, the spontaneous emission spectrum of a device with no output coupler was taken at a fixed current for different heatsink temperatures. The peak wavelength of each spectrum was determined for the different temperatures; the peak wavelength was plotted as a function of temperature to yield the peak shift with temperature, Δλ/K. The same process was then carried out at different input currents for a fixed heatsink temperature, the peak wavelength of each spectrum was plotted as a function of input power to yield the wavelength shift with input power, Δλ/P. The thermal resistance can then be obtained using the equation from [14]:

$$R_{th} = \left(\frac{\Delta\lambda}{K}\right)^{-1} \times \left(\frac{\Delta\lambda}{P}\right) \tag{4.5}$$

Figure 4.12 shows the measured thermal resistance of a range of device diameters. As expected the smallest device has the highest thermal resistance, as it has the greatest power density, with the thermal resistance decreasing with device diameter. For all the device diameters the thermal resistance compares favorably to previously quoted values [14-16]. A reduction in the thermal resistance will result in an extension of the point at which thermal rollover occurs allowing for a greater maximum power to be reached.

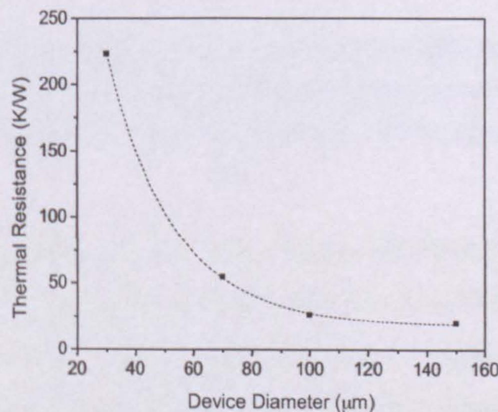

Figure 4.12 Thermal resistance as a function of device diameter for devices with a substrate doping of 4x10¹⁷ cm⁻³

Continuing to look at the affect of electrical power density as a function of area, *Figure 4.13a* shows the IV characteristics of these devices as a function of diameter. Solid square points indicate the point of maximal CW optical power at rollover for each device. The rollover point in each case increases linearly with increasing device diameter at a rate of ~ 5.8 mA/ μm. Using the data from *Figure 4.13a* along with data from *Figure 4.11b* it was possible to calculate the electrical power density in each device. *Figure 4.13b* shows the electrical power density developed in the device at rollover, the power causing Joule heating, which was given by the electrical power developed minus emitted optical power per unit area. Here it was assumed no optical power was emitted through the p-DBR. For the smaller diameter devices, 30 and 70 μm, the calculated developed power per unit area was similar. For the larger diameter devices considerably smaller calculated developed powers at rollover are determined.

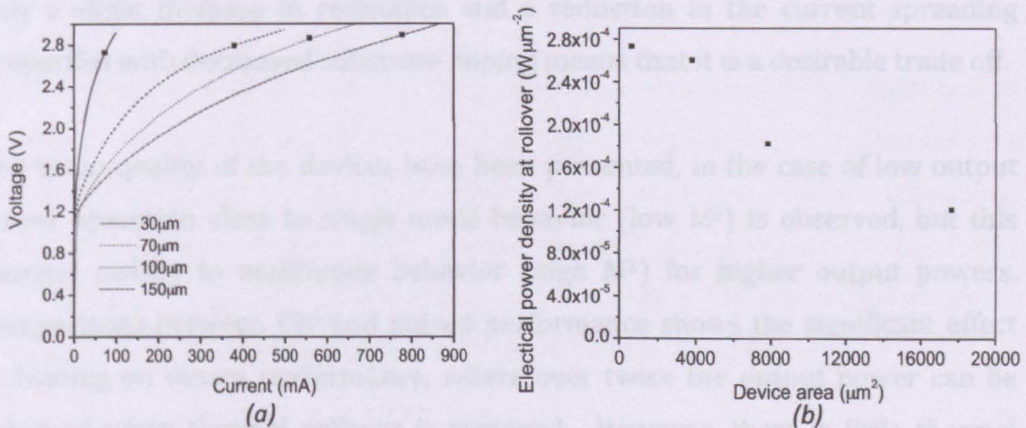

Figure 4.13 (a) Voltage current characteristic for devices of different diameter, where the thermal rollover point is marked with a point (b) Electrical power density at rollover (electrical – optical) as a function of device area for device with a substrate doping of 4x10^{17} cm^{-3}

The apparent performance drop off above 70 μm diameters is attributed to the combination of greatly reduced thermal and electrical resistance with increasing area. This reduction was levied against poorer carrier distribution with increasing area, resulting in reduced overlap with the lasing mode, as evidenced by the reduced slope efficiency. In the case of uniform efficiency, the power density for each of the diameters above 30 μm would decrease due to the

resultant increase in optical power produced, hence the possibility of a linear relationship with power density and area being formed. It is desirable for the electrical power density to be at a minimum for each device, as this will indicate a combination of low electrical resistance as well as high optical output power.

4.8 Conclusion

In this chapter a study of the design trade-offs in substrate emitting EP-VECSELs has been presented. Key areas of design for achieving high power have been highlighted, namely: detuning, device self-heating, current spreading and substrate doping for a substrate emitting EP-VECSEL geometry. An experimental study of the effect of substrate doping on the operating characteristics of substrate emitting electrically pumped VECSELs has been discussed. The reduction in substrate doping from $2x10^{18}$ to $4x10^{17}$ cm^{-3} leads to a reduction in optical loss and therefore enhanced current-gain characteristics. Coupled to this only a slight increase in resistance and a reduction in the current spreading properties with decreased substrate doping means that it is a desirable trade off.

The beam quality of the devices have been presented, in the case of low output power operation close to single mode behavior (low M^2) is observed, but this changes swiftly to multimode behavior (high M^2) for higher output powers. Comparisons between CW and pulsed performance shows the significant effect of heating on device performance, where over twice the output power can be achieved when thermal rollover is removed. However, there is little thermal effect on the slope efficiency until the output coupler reflectivity becomes low as a result of the heating due to the threshold current increase. The output coupler transmittivity ($1-R_{ext}$) controls the maximum output power and hence slope efficiency, with a 70 and a 84 % reflectivity yielding the best results in the pulsed and CW cases respectively.

Spatial carrier distributions, evidenced by near field profiling of devices without external feedback indicate non-uniform carrier distributions for device diameters of greater than 70 μm, with a current spreading layer thickness of 100

μm. Better current spreading may be achieved with the use of a thicker current spreading layer at the cost of a reduced output power, or with a change in the contact arrangement, discussed in chapter 5. As a result of the non-Gaussian carrier distribution in all but the 30 μm device there is a drop in the device efficiency. This in turn is a major contributing factor to the non-uniform power scaling with area exhibited, in addition to the problem of non-idealized heat flow for increasing device area.

Measurement of the device thermal resistance shows that the thermal resistance decreases with device diameter. Reduction in the thermal resistance of the devices by improving heat sinking will result in improved device performance by delaying the onset of thermal roll over. Additionally, a reduction in electrical power density by reducing device resistance will result in less Joule heating and therefore will also extend the operating range of the device, yielding a higher output power.

Overall, improvements in device output power can be achieved by a reduction of threshold current and an increase of slope efficiency, discussed in chapter 6, a reduction in device electrical resistance and improved current spreading, discussed in chapter 5 and better device thermal management. None of this withstanding CW powers of 133 mW at 981 nm with a 150 μm diameter device with 4×10^{17} cm^{-3} substrate doping at 0°C have been demonstrated.

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5 Electrical Performance Optimisation

5.1 Introduction

As discussed previously in chapter 2, the electrical performance of an EP-VECSEL device is critical in defining the overall device performance, where high resistance will lead to significant self-heating. It can be argued that the largest proportion of the overall device resistance is that of the p-DBR, due to the lower hole mobility. The reduction of resistance in this structure is not trivial, as although the incorporation of more dopant into the structure will decrease the resistance, it will also increase the free carrier absorption loss. Due to the requirement for high optical and electrical performance from the DBR structure, this solution is undesirable. It is therefore necessary to produce a design that will yield a low resistance device, without incurring a significant optical loss penalty.

This area has had much attention and many research groups have reported a resistance reduction by the introduction of some sort of grading or interface layer in between the two DBR layers. Simple methods for resistance reduction could be achieved by introducing a single step grading layer [1], interface delta doping [2] or introduction of a superlattice structure [3]. More complicated schemes demonstrated used a continuous linear graded interface [4], [5]. Similarly, the use of a parabolic continuous grading profile can reduce resistance [6], [7]. Later, a uni-parabolic grading profile was suggested as an improvement on the parabolic profile [8]. More recently, it has been shown that the continuously graded profiles can be approximated to a discrete number of steps [9], allowing for easier growth. A different method suggested, is that of intermixing [10], however, although the resistance is reduced, the interfaces are roughened leading to reduced optical quality.

In this chapter the influence of different grading and doping schemes on DBR resistance and optical loss will be investigated, this will first be carried out for p-doped DBRs, as this is where the largest benefits can be gained. The electrical behaviour will be investigated by VCSEL modelling software, where a number of different DBR designs could be simulated. In this case, linear grading provided the lowest resistance but with 3 step discrete composition giving comparable performance. In addition, the analysis of epitaxially grown DBR designs will be presented, where the single step grading exhibited the lowest resistance, where more complex designs exhibited a higher resistance attributed to poor growth interface quality in these structures. The optical loss will be investigated using a simple model using the interaction of the electric field in the DBR profile and the doping level at various positions in the DBR. Coupling the optical and electrical modelling allows the areas where there are benefits to be highlighted; in this case delta doping the interfaces has a significant effect on the resistance for only a modest increase in optical loss.

Following this, the same analysis will be carried out for n-doped DBRs. In this case, due to the transition to an indirect band gap at aluminium concentrations above 45%[11], a single 30% AlGaAs step interface provides the lowest resistance. This is supported by measurements performed on grown structures, where the abrupt interface had a lower resistance than the 50% AlGaAs single step. For the optical performance, the n-DBR behaves similarly to the p-DBR, but the free carrier absorption loss is lower.

Secondary ion mass spectrometry (SIMS) data will be presented for an n-DBR, as well as a full EP-VECSEL structure. This is important, as it shows how doping incorporates into the different materials used and to what level, allowing the real doping levels and distribution within the structure to be understood. For the analysed structures, there is a modulation in the doping incorporation in the DBR, where the doping level is higher in the AlGaAs layers than the GaAs layers, this is much worse for the carbon doped p-DBR. In addition, there is also a large carbon background doping in the n-DBR, which is unfavourable. Finally, a discussion of the top contact geometry and the interplay with the current

spreading layer will be presented, where a simple model will be used to examine the carrier distribution as a function of ring contact width. It shows that a reduced contact width decreases the required thickness of the current spreading layer, allowing for a thinner layer to be used and hence leading to reduced optical loss. In addition, for a fixed contact width of 20 μm the required current spreading layer thickness increases linearly with device radius.

5.2 p-DBR grading design

In order to investigate the affect of different grading layer designs on the DBR resistance, electrical modelling of the DBR structure was carried out. This was done using a program called SimWindows [12] a VCSEL simulation tool, where the layer structure and doping levels were input and the band structure was then calculated. A drift diffusion model was then used to calculate the current at different bias voltage for the structure; this current-voltage relationship was then used to calculate the resistance of the structure. The model was set to operate at 300 K and included models for Fermi-Dirac charge, incomplete dopant ionization, quantum mechanical tunnelling and dopant dependent mobility. The radius of the device simulated was fixed at 50 μm in every case. Although it is very difficult to create a model that accurately matches experimental results, they are very useful for highlighting trends when it comes to optimising device parameters.

Following on from the optical simulations presented in chapter 2, the first step was to simulate the same structure design. In this case a 32 period $Al_{0.9}Ga_{0.1}As/GaAs$ DBR, with a 10 nm grading layer and a uniform doping density of $2x10^{18}$ cm^{-3} was simulated. The aluminium composition of the grading layer was changed and its affect on the device resistance is plotted in *Figure 5.1a*. The DBR resistance decreases in a linear manner with increasing aluminium concentration, reaching a minimum value of 8.34 Ω at 44%, beyond this point the resistance increases again reaching a maximum at 80%. The resistance was plotted on a log scale, showing that there were orders of magnitude difference between the maximum and minimum value. However, these values seem greatly

exaggerated from what would be expected, with maybe only an order of magnitude separating the maxima and minima. This could be attributed the large number of heterointerfaces used in the simulation. Also marked on the figure is the resistance for the same DBR structure with a 10 nm linear grade, as opposed to a single step, the resistance of this design is ~ 8 times less than the best single step grade, with a value of 1.22 Ω.

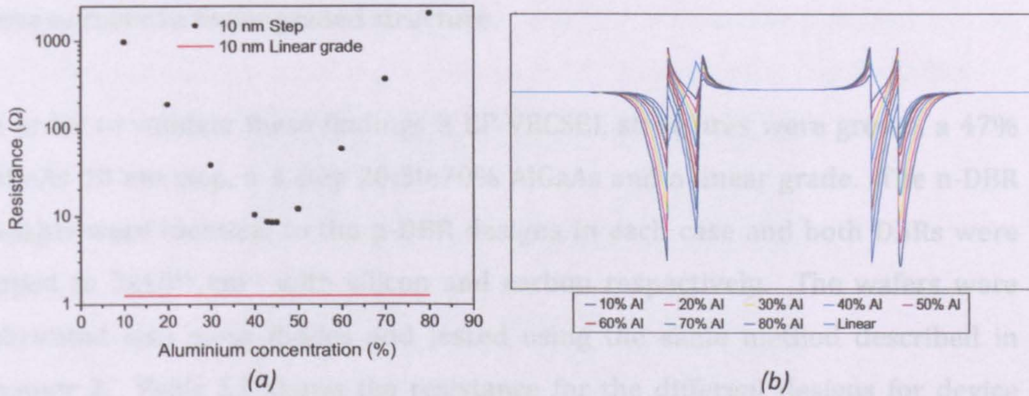

Figure 5.1 (a) Modeled resistance as a function of grading layer aluminium concentrations in the p-DBR (b) Modeled conduction band energy diagram for different grading layer aluminium concentrations in the p-DBR

Figure 5.1b shows a single period the simulated conduction band for each of the different aluminium concentrations, as well as the linear grading. It can be seen that for low aluminium concentrations the first potential spike is large with the second spike being smaller. As the aluminium concentration is increased the size of the first spike decreases, while the second spike increases, to the point where the size of the spikes are almost equal between 40-50% AlGaAs. Beyond this point the second spike becomes greater than the first and grows with increasing aluminium composition while the first spike continues to decrease. The linear graded interface has a further reduced potential spike, while only one peak in present due to the continuous nature of the graded interface. It is the size of this potential peak that determines the resistance, therefore making it as small as possible is very desirable.

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3 step interface with a 3 nm 20% AlGaAs, 4 nm 50% AlGaAs and 3 nm 70% AlGaAs was simulated and is shown by the red line in *Figure 5.2b*. The resistance of this structure is 1.53 Ω, a further reduction in resistance compared to that of the best 2-step design. However, this reduction is much smaller, ~ 0.5 Ω, compared to that gained from going from a single step to a 2 step design, ~ 6.3 Ω. Further to this, the reduction gained moving to a linear grade is smaller again, ~ 0.3 Ω, indicating that 4 or 5 step grading schemes will have a resistance very close to that of a linear graded structure.

In order to validate these findings 3 EP-VECSEL structures were grown, a 47% AlGaAs 10 nm step, a 3 step 20:50:70% AlGaAs and a linear grade. The n-DBR designs were identical to the p-DBR designs in each case and both DBRs were doped to $2x10^{18}$ cm^{-3} with silicon and carbon respectively. The wafers were fabricated into mesa diodes and tested using the same method described in chapter 2. *Table 5.1* shows the resistance for the different designs for device diameters of 100 and 200 μm, with the single step having the lowest resistance, followed by the linear grade and then the 3 step grading.

Interface design	200μm Resistance (Ω)	100μm Resistance (Ω)
Single 47% Al step	2.59	3.34
3 Step	3.53	4.24
Linear	3.13	3.68

Table 5.1 Measured resistance for different EP-VECSEL DBR designs for two mesa sizes

This result is unexpected, but is believed to be due to interface roughness and incorrect aluminium composition. *Figure 5.3* shows a transmission electron microscope image of the DBR for the linear graded sample, the dark region are GaAs and the light regions are AlGaAs, with the intensity signifying composition. It can be seen from the image that the interface between the AlGaAs and GaAs regions are rough and that there is not a smooth increase in intensity from the dark to the light region that would be expected from a linear grade. The grading also does not seem to be same at both interfaces. It is thought that a similar

situation has occurred in the 3 step design due to the additional interfaces and it is this that is causing the increased resistance.

Further to this, the measured resistance for a full EP-VECSEL with single step grading was 3.24 Ω and the simulated resistance for the optimum single step p-DBR alone was 8.34 Ω, indicating that the simulations are a significant over estimate of the actual value. In addition, the benefits of reduced resistance from a design with a more complex grading scheme are counterbalanced by the increased technological challenge, hence, a single step design is still desirable.

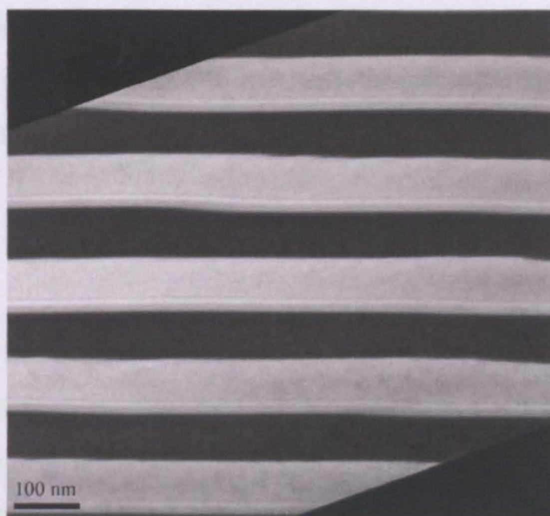

Figure 5.3 TEM of linear grading scheme in p-DBR of EP-VECSEL structure

5.3 p-DBR doping design

The major trade-off in designing EP-VECSELs is that of doping and free carrier absorption loss, with an increase in doping leading to reduced resistance but a greater absorption loss. This is particularly exacerbated in the case of the p-DBR due to its higher resistance and higher absorption loss compared to that of an n-doped structure. Band engineering, as described in a previous section, can be used to decrease the resistance without increasing the doping level. However, it is useful to understand the interplay of resistance and absorption in order to best optimise the overall structure.

The resistance was again obtained through modelling the DBR structure using SimWindows, where the doping level in any region could be defined. The absorption loss was obtained from a simple model, described by *Figure 5.4*. In this model, the electric field in the DBR, seen as the blue line in *Figure 5.4*, obtained from CAMFR modelling, was integrated over the length of the DBR, with its refractive index profile shown in red in *Figure 5.4*. The resultant value was then normalised to a known value of absorption for a given doping level, with the average doping level represented as a dotted line in the figure. There are a number of papers reporting the free carrier absorption as a function of wavelength for different doping levels [13],[14]. However, the values vary slightly in each case at the desired 980 nm wavelength, as it is a basic model the equation described in [15]was used.

$$\propto_{fc} = 3\times10^{-18}n + 7\times10^{-18}p \qquad (5.1)$$

Where n and p are the doping concentrations in cm^{-3}. The green and orange regions in *Figure 5.4* show the low field and high field interface regions respectively, the doping level in the model in these areas could be changed separately to observe the affect. In the case of the p-DBR, the electric field for a single 44% AlGaAs 10 nm step design was used, with the loss normalised to 7 cm^{-1} for a doping of 1×10^{18} cm^{-3}.

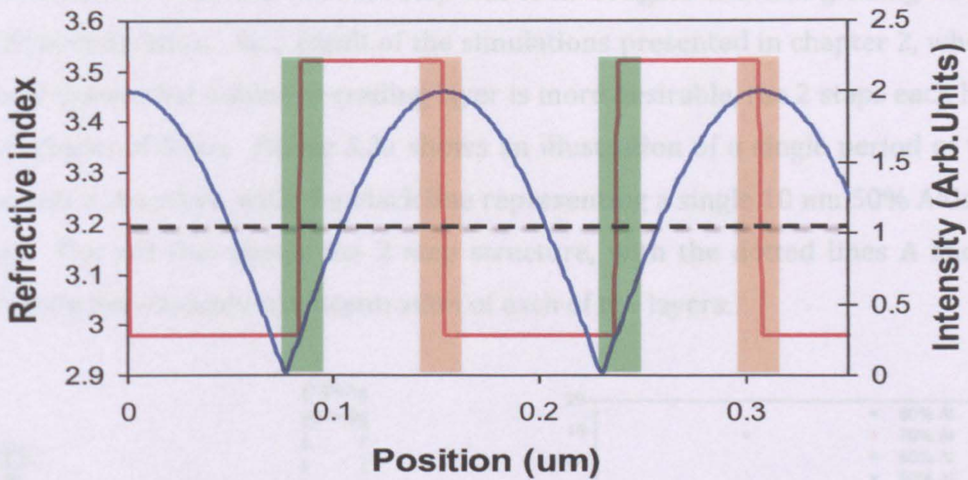

Figure 5.4 Diagram of the interaction of the electric field and the DBR with the average doping level marked with a dotted line and the DBR interface regions marked in green and red

Figure 5.5 shows the resistance for a linear and 44% AlGaAs single 10 nm step designs as a function of constant uniform doping in the structure, as well as the absorption loss as a function of uniform doping. The resistance for each of the two structures varies in a non-linear manner with doping concentration, with linear graded structure having a lower resistance at each point, but the single step experiencing a greater reduction in resistance for an increase in doping. At high doping levels the reduction in resistance for both structures becomes smaller. The absorption loss for a uniform doping variation changes in a linear manner, this indicates it is much better to linear grade the interface and keep the doping level low in order to keep the absorption loss to a minimum.

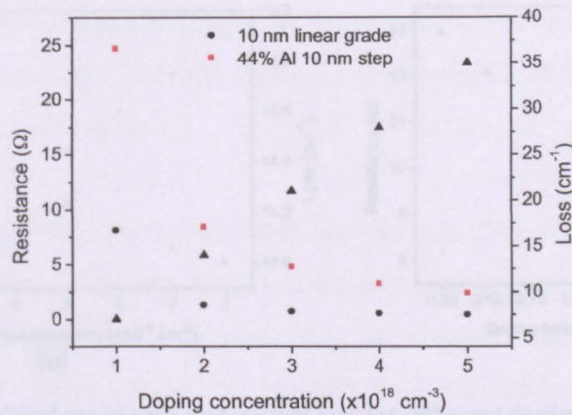

Figure 5.5 Modeled resistance and optical loss for different doping levels in a single step p-DBR and a linear grading scheme

Continuing on from this, the next step was to observe how doping affected the resistance and loss when it was varied in areas where the electric field intensity was at a maximum or a minimum. A single 44% AlGaAs 10 nm step design was used with an average doping of $2x10^{18}$ cm^{-3}, the doping in the low field regions, AlGaAs to GaAs transitions, was then varied with the behaviour shown in *Figure 5.6a*. The resistance varies in a non-linear manner, while the absorption loss varies in a linear manner. For a large increase in doping concentration, the absorption loss only increases by ~ 1 cm^{-1}, indicating there is little interaction with the electric field. However, the resistance reduction with increased doping concentration is also small, with the behaviour of the system still dominated by the average doping level in the device.

Repeating this analysis for the high field regions, GaAs to AlGaAs transitions, but this time reducing the doping level in these regions yields *Figure 5.6b*. Again, the absorption loss varies linearly, while the resistance changes in a non-linear manner. The variation in the absorption loss across the range of doping concentrations is still small, 1.05 cm^{-1}, but the change in resistance is much bigger as the doping is decreased. Similar to above, the average doping still dominates the device behaviour. Therefore, it is undesirable to use this technique to reduce the absorption loss.

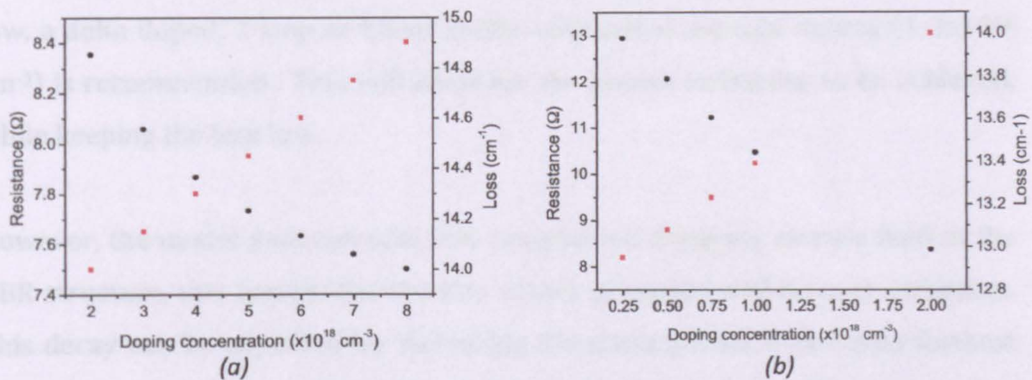

Figure 5.6 (a) Modeled resistance and optical loss for different doping levels at the low field interface in the p-DBR (b) Modeled resistance and optical loss for different doping levels at the high field interface in the p-DBR

Since there is little change in the absorption loss for the high field and low field cases, the behaviour if the doping at both interfaces was increased was investigated, delta doping, this is shown in *Figure 5.7.* In this case there is a larger change in the resistance and loss values for an increase in doping concentration, with a considerable resistance benefit for only a small loss penalty, ~ 3 Ω for only an additional 2 cm^{-1} at a doping level of $5x10^{18}$ cm^{-3}. This result shows that this technique would be of benefit in DBR design.

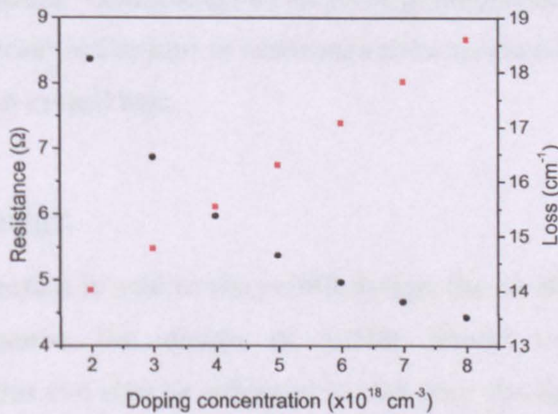

Figure 5.7 Modeled resistance and optical loss for different doping levels in both sides of the p-DBR interface

In order to keep the resistance of the structure low whilst also keeping the loss low, a delta doped, 3 step or linear grade, with a low average doping (1-2x10^{18} cm^{-3}) is recommended. This will allow for the lowest resistance to be achieved, while keeping the loss low.

However, the model does not take into account the decaying electric field in the DBR structure, this means that the loss values proposed will be over estimates. This decay can be exploited by increasing the doping level in the area furthest from the active region where the electric field will be low. The penetration depth, L_{pen}, can be used as a figure of merit for where the doping period can be increased. Where the penetration depth is an approximation for how far the electric field penetrates into the DBR, this is dependent on the number of DBRs in the stack, and can be calculated using methods presented here [16] [17]. For high reflectivities (as in this case), the penetration depth tends towards a fixed value, ~ 495 nm in this case. This allows the doping level to be increased after ~ 5 DBR periods and a weaker affect on the loss to be experienced. As a result, a large portion of the DBR (16-20 periods) can be highly doped (8-10x10^{18} cm^{-3}) without a significant increase to the loss but allowing for a dramatic reduction in resistance, as suggested in [18]. In the region closer to the DBR (5-15 periods) the doping level can be increased, but to lower level, perhaps 4x10^{18} cm^{-3}, to reduce the resistance. Combining this with the grading schemes discussed above will allow significant reductions in resistance to be achieved while incurring only slight penalties in optical loss.

5.4 n-DBR design

While much attention is paid to the p-DBR design, due to the dominant affect on device performance, the design of n-DBR should not be neglected as performance gains can also be achieved in this area through careful design. In the same manner as for the p-DBR the n-DBR was simulated using the SimWindows software. A 12 period single 10 nm step design with a uniform doping concentration of 2x10^{18} cm^{-3} was simulated for different grading step aluminium compositions. *Figure 5.8a* plots the resistance of the n-DBR for

different aluminium grading step concentrations. Increasing from low aluminium concentrations the resistance decreases to a minima at 30% AlGaAs, a further increase in aluminium concentration causes the resistance to increase to a maxima at 50% AlGaAs, above this concentration the again resistance decreases. Also marked on the figure are the resistance for a 10 nm linear grade (blue) and an ungraded abrupt interface (red), the value of resistance for the abrupt interface is significantly lower than that of the linear grade and a lower value than any design with more than 35% aluminium in the grading layer.

This behaviour is very different from that of the p-DBR and can be explained by the change in mobility of the electron at aluminium compositions greater than or equal to 45%, due the change in effective mass caused by to a transition from a direct to an indirect band gap at this composition [11]. *Figure 5.8b* plots that electron and hole mobilities in AlGaAs for varying aluminium concentrations, based on the equations given in [19]. The electron mobility decreases with increasing aluminium concentration to a minimum at 45%, where the transition occurs; above this value the mobility increases until 80% AlGaAs where it begins to decrease again. The behaviour for the light and heavy hole are identical but with different values, the mobility decreases with increasing aluminium fraction to a minimum at 65% AlGaAs, above this concentration the mobility increases again. The mobility of the electrons is greater than that of the holes up to the transition point where the light hole mobility becomes greater than that of the electron.

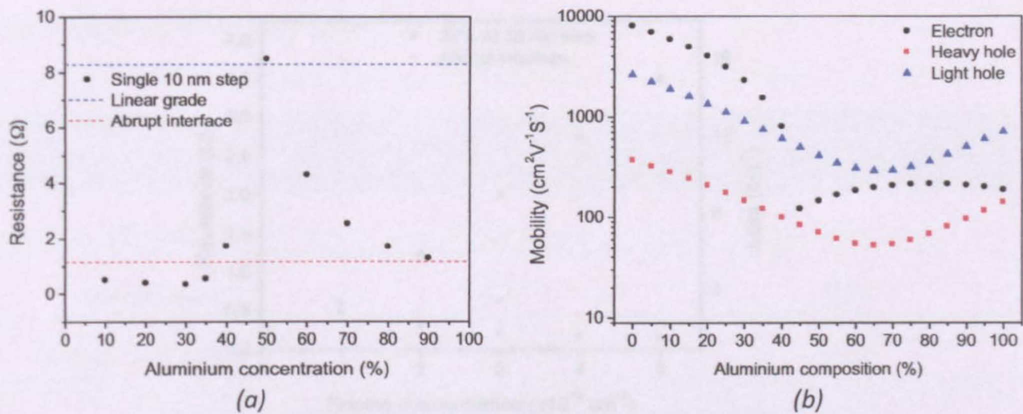

Figure 5.8 (a) Modeled resistance for different aluminium concentrations in a single step grading for the n-DBR (b) Carrier mobility for different aluminum concentrations

This behaviour gives rises to a very different design for a low resistance n-DBR, compared to that of the p-DBR, with a single 30% AlGaAs step giving rise to the lowest resistance and a linear graded design being almost the worst possible. As with the p-DBR previously, the affect of average doping on device resistance and absorption loss was investigated. The electric field for a 30% AlGaAs single step design was used to calculate the loss, using (5.1) to normalise the loss to 3 cm^{-1} for a doping of $1x10^{18}$ cm^{-3}. *Figure 5.9* plots the resistance as a function of doping concentration for an abrupt DBR and a 30% AlGaAs single 10 nm step design on the left axis, and the absorption loss as a function of doping concentration on the right axis. The behaviour is very similar to that of the p-DBR case, with the resistance varying non-linearly and the absorption changing in a linear fashion, but with the magnitude of all the values reduced. The change in resistance for the single step grading, as a function of doping, is much smaller than that of the abrupt case, with the change getting smaller with each further increase in doping concentration.

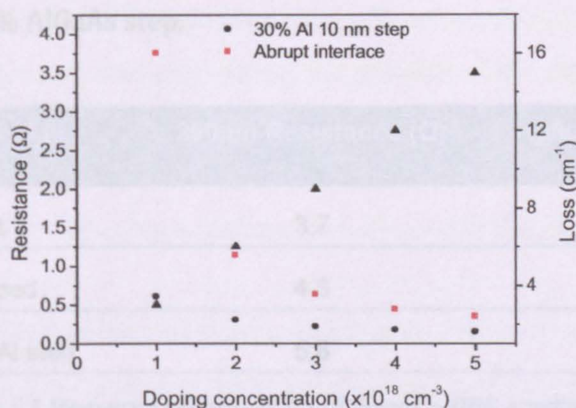

Figure 5.9 Modeled resistance and optical loss for different doping levels in different n-DBR grading designs

As the n-DBR behaviour as a function of doping is similar to that of the p-DBR it is suggested that a delta doped 30% AlGaAs step with an average doping of $1\text{x}10^{18}$ cm^{-3} be used. With this design the resistance will be optimised to a low value whilst not sacrificing too much in terms of absorption loss. In addition, the doping level increase allowed by the penetration depth should not be used in this case, as light is also coupled back through the n-DBR and this would cause an increase in optical loss.

To test the simulation results a number of n-DBR designs were grown, an abrupt interface design, an abrupt interface with delta doping and a 47% AlGaAs 10 nm single step. In each case the structure was 20 periods, the average doping was $1\text{x}10^{18}$ cm^{-3}, for the delta doping and interface doping of $1\text{x}10^{19}$ cm^{-3} was desired. These samples were fabricated into mesas and tested using the same method as described in chapter 2. *Table 5.2* shows the resistance for the 3 different designs for mesas with 100 and 200 μm diameters. The values of resistance in each case seem to be very high, as the resistance of a 200 μm whole EP-VECSEL structure is only 2.59 Ω. The reason for the high resistance is unknown, and the fabrication was repeated but the results were the same. However, the trends in the data are still valid, with the abrupt design having the lowest resistance, followed by the delta doped design and then the 47% AlGaAs

step. This supports the modelling that an abrupt interface has a lower resistance than a single 47% AlGaAs step.

Interface design	200µm Resistance (Ω)	100µm Resistance (Ω)
Abrupt	3.7	9.3
Delta doped	4.3	11.5
Single 47% Al step	5.8	15.9

Table 5.2 Measured resistance for different n-DBR grading designs

5.5 Secondary ion mass spectrometry analysis

Secondary ion mass spectrometry (SIMS) is a technique for analysing the composition of materials and is very helpful in understanding concentrations and incorporation rates in an epitaxially grown structure. The process is carried out by milling a piece of epitaxially grown material using an ion beam, the secondary ions sputtered out by the milling process are collected and sent to a mass spectrometer to determine their elemental and molecular composition. This is a very useful technique for analysing an EP-VECSEL structure as the profile of the aluminium composition, as well as the doping profiles in the n-DBR and p-DBRs can be observed [20].

Figure 5.10 shows the SIMS analysis of the delta-doped abrupt n-DBR design described in the previous section. The milling direction is from left to right indicating the depth into the sample, the black line is the concentration of the silicon dopant as a function of depth through the structure, and the concentration is on a log scale. The blue line is the number of arsenic counts per second as a function of depth, the red line is aluminium counts per second as a function of depth into the structure, and this has not been normalised into a concentration and is on the graph as a reference.

On the left hand side of the graph is the highly doped GaAs cap layer with a doping of 1.3×10^{19} cm^{-3}. Then the first 3 DBR periods with a transition between

the AlGaAs and GaAs layers, shown by the continuous variation of the aluminium concentration. The spiked regions in the silicon profile are the areas of delta doping, which have spread out during the growth. This shows it is difficult to achieve small highly doped regions, meaning the absorption loss for delta doped designs will be higher as the average doping level will be higher over a larger region than specified causing a larger interaction with the electric field.

It is also worth noting that the average doping is ~ 5×10^{18} cm^{-3}, which is 5 times higher than designed. However, this is not a measure of the activated dopant, *i.e.* free carrier concentration, but the atomic incorporation, which is higher than that of the free carrier concentration. Correlating the SIMS data with electrochemical capacitance voltage (ECV) measurements, which measure the free carrier concentration, gives an activated to incorporated ratio of ~ 80%, which is very similar to that reported in [20]. This value is important; as if the ratio is low then this indicates that there are a large number of point defects in the material, resulting in increased non-radiative recombination.

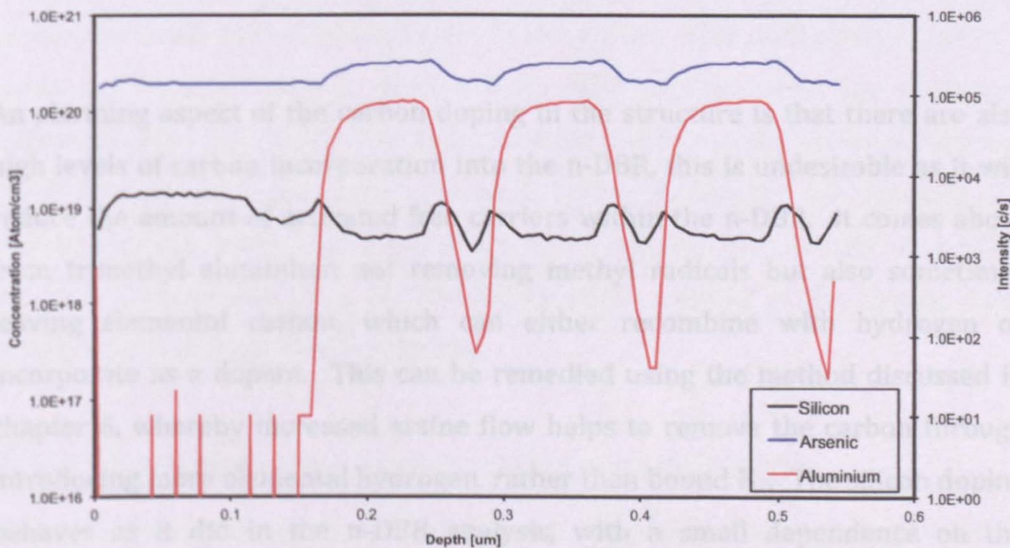

Figure 5.10 SIMS measurement of an n-DBR showing the variation in silicon, aluminium and arsenic concentration

Progressing from this, SIMS analysis was also carried out on the EP-VECSEL material used in chapter 4, with 47% AlGaAs single step grading in both DBRs, 6 QWs and an average doping of $2x10^{18}$ cm^{-3}, shown in *Figure 5.11*. In this case the first few microns of the p-DBR have been left out of the figure for clarity. As with the previous figure, the sample increases in depth from left to right, where the sample has been ion milled. The aluminium (red) and arsenic (blue) are included as a reference to the layers within the structure and are not absolute concentrations. The carbon p doping incorporation within the structure has a strong dependence on AlGaAs composition with a larger incorporation in higher aluminium percentage layers, ~x10 larger for $Al_{0.9}Ga_{0.1}As$ than GaAs. The reason for this is two fold, firstly the carbon precursor carbon tetrachloride causes an etch back reaction due to the presence of chlorine reactants [20], of which $GaCl_3$ is more volatile than $AlCl_3$, as a result as the Al composition increases the etch back process will decrease, resulting in more carbon incorporation into arsenic sites [20]. Secondly, the energy of the Al-C bond is greater than that of the Ga-C bond, making it thermodynamically more favourable to have higher incorporation levels at higher aluminium concentrations [20].

An alarming aspect of the carbon doping in the structure is that there are also high levels of carbon incorporation into the n-DBR, this is undesirable as it will reduce the amount of activated free carriers within the n-DBR. It comes about from trimethyl aluminium not removing methyl radicals but also sometimes leaving elemental carbon, which can either recombine with hydrogen or incorporate as a dopant. This can be remedied using the method discussed in chapter 6, whereby increased arsine flow helps to remove the carbon through introducing more elemental hydrogen, rather than bound H_2. The silicon doping behaves as it did in the n-DBR analysis, with a small dependence on the aluminium concentration and a similar average atomic concentration of $5x10^{18}$ cm^{-3} is also measured. There is also very little silicon incorporation into the p-DBR.

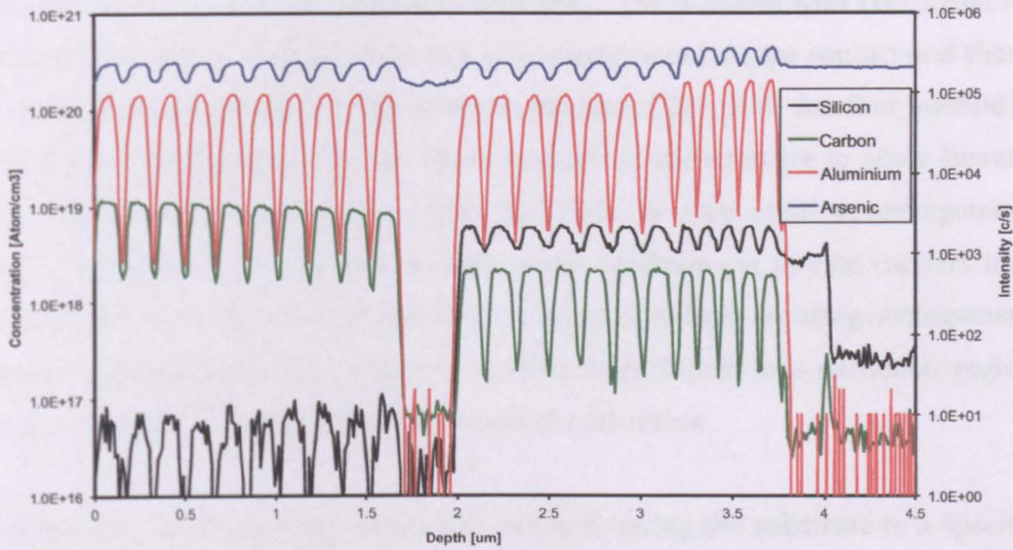

Figure 5.11 SIMS measurement of an EP-VECSEL showing the carbon, silicon, aluminium and arsenic concentrations

In the case of the n and p DBR analysis discussed above, the average free carrier concentration is 2-3 times greater than specified in the designs, with a much greater level still in the AlGaAs layers of the p-DBR. This discrepancy may be a reason as to why there is such a large difference between the resistance calculated from the model data and that measured from the grown structures. These high doping levels, which are good for low resistance, are resulting in a high free carrier absorption loss and are hence undesirable. In order to achieve the best performance from an EP-VECSEL better control of the doping level, incorporation and position is required.

5.6 Contact geometry and current spreading layer

The final element of electrical performance optimisation is that of the current spreading layer (CSL) and contact shape and arrangement. In chapter 4 the importance of the carrier distribution on the device performance is discussed, with devices of greater than 70 μm suffering from a non-uniform carrier distribution, this in turn leads to non-optimal device performance. There are several potential methods for improving the carrier distribution in the device,

such as using a indium tin oxide (ITO) transparent electrical contact to enable current injection over the apertured area [21]. The problem with ITO is that its contact resistance is higher than that of a conventional n-type contact and there will be a certain amount of optical loss in the layer [22], [23]. Another method is to place a thin electrically conductive cross across the aperture to allow current injection in the apertured region [24] [25] [26]. In a top emitting arrangement an oxide aperture can be used to add carrier confinement forcing carriers into the middle of the device [27] [28] [29]. In a top or bottom emitting arrangement proton implantation can be used to confine current flow to a particular region [30], improving the carrier distribution in the structure.

In the realized devices the CSL is formed by thinning the substrate to a specific thickness, in this case 100 μm. Due to the absorption loss associated with the doping density of the CSL, it is desired that the thickness of the CSL be minimized to keep the loss low. The main factors that affect the carrier distribution are the CSL thickness, spreading resistance of the CSL, and the contact geometry. In this section a simple model, described in [31], was used to attempt to optimise the CSL thickness and the contact geometry to yield a uniform carrier distribution.

The model calculates the current distribution at different vertical and radial positions in the CSL for a given device radius and ring contact width, the model was simulated using Matlab; *Figure 5.12a* shows the top view of the model arrangement, R_d is the device radius and R_c is the radius to the outer edge of the contact, with $R_c - R_d$ yielding the width of the contact. *Figure 5.12b* shows a cross-section view through the structure, H denotes the CSL thickness, with the device and outer contact radiuses also marked on, z defines the vertical position within the structure, while r defines the radial position within the structure, I_0 is the injected current. As the device was cylindrically symmetric only half of the device was simulated to reduce computation time.

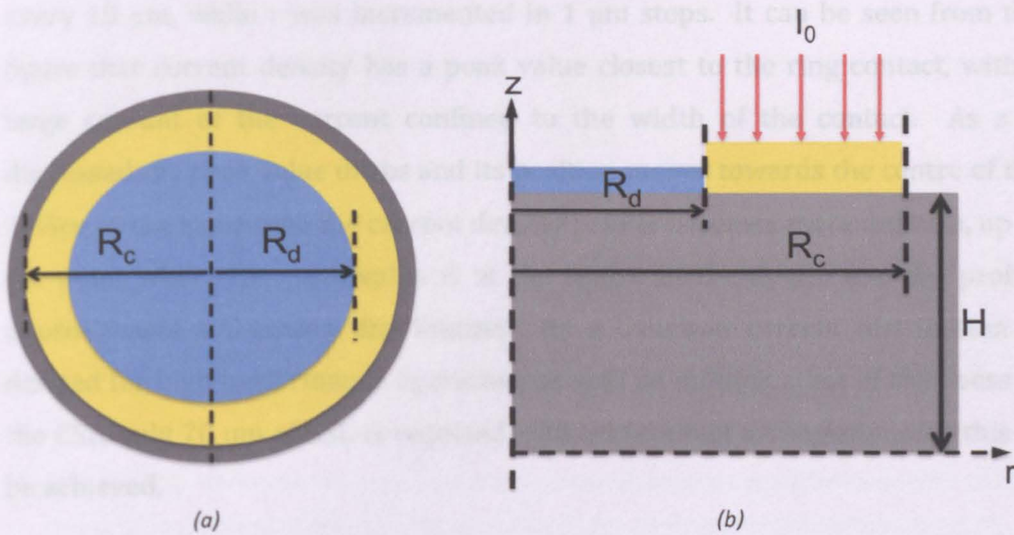

Figure 5.12 (a) Top view of the proposed electrical contact arrangement (b) Cross-section view of current spreading model arrangement

The equations used to calculate the current distribution were:

$$J_z(r,z) = -\frac{I_0(H-z)}{m(R_d+R_c)} \times \sum_{i=1}^{m} \left\{ \frac{R_i}{[(R_i+r)^2+(H-z)^2]^{3/2}} \times \sum_{n=0} \left[\frac{(2n-1)!!}{2n!!}\right]^2 (1+2n)k_i^{2n} \right\} \quad (5.2)$$

where

$$R_i = R_d + (i-1)\frac{R_C - R_d}{m} \quad (5.3)$$

$$i = 1,2,3,\ldots,m$$

and

$$k_i^2 = \frac{4R_i r}{(R_i+r)^2 + (H-z)^2} \quad (5.4)$$

For all the simulations the values of $m=100$, $n=150$ and $I_0=1000$, *Figure 5.13a* shows the current density as a function of device radius at different positions through the CSL (values of z), for a device with radius 50 µm and a ring contact width of 20 µm. The value of $H=100$ µm and the current density was calculated

every 10 μm, while *r* was incremented in 1 μm steps. It can be seen from the figure that current density has a peak value closest to the ring contact, with a large amount of the current confined to the width of the contact. As *z* is decreased the peak value drops and its position moves towards the centre of the device, at the same time the current density profile becomes more uniform, up to the point where the peak value is at the centre of the device and the profile approximates a Gaussian distribution. As a Gaussian current distribution is desired for high performance operation, as well as minimization of thickness of the CSL, only 70 μm of CSL is required with this contact arrangement for this to be achieved.

Extending this concept further, the device radius was fixed to 50 μm and the contact width was varied to investigate the affect on current distribution. *Figure 5.13b* plots the normalised peak current density and the required CSL thickness as a function of contact width. The peak current density in each case was normalised to the peak current density of the 10 μm contact width, while the required CSL thickness is defined as the thickness required in order for the peak value of a given profile to be at the centre of the device. The figure shows that as the contact width increases the normalised peak current density decreases in a non-linear manner, with a large change occurring at small contact widths but as the contact width increases the difference decreases, approaching a constant value above 160 μm. This is logical, as the injected current is fixed but the contact width is increasing, so the current density decreases.

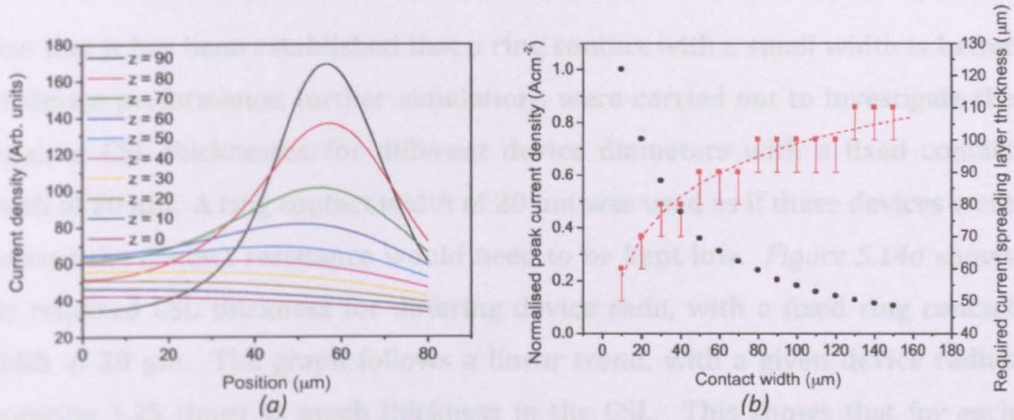

Figure 5.13 (a) Modeled current density as a function of position at different heights in the current spreading layer for a device of radius 50 μm and ring contact width 20 μm (b) Normalised peak current density and required current spreading layer thickness for a 50 μm device with different ring contact widths

In the case of the required CSL thickness, as the contact width is increased the required CSL thickness increases. The tiered behaviour of the graph is due to the fact that the current distribution profiles were only generated at 10 μm intervals through the structure and so could be at the lower or the upper bound of that interval. The increase in required CSL thickness is greater at smaller contact widths and decreases with increasing contact width. This graph indicates that as the contact width is increased the injected current density is reduced, meaning for large contact widths a larger proportion of the current will have a greater distance to diffuse laterally, hence requiring a greater thickness of CSL to achieve a Gaussian distribution.

For the devices described in chapter 4 the top contact can be thought of as a very wide ring contact, extrapolating the required CSL thickness curve to a width of 200 μm gives required CSL thickness of ~ 120 μm. The CSL thickness was 100 μm in the realized devices, below the required thickness for uniform carrier concentration for a device with 100 μm diameter, supporting the non-uniform carrier distribution profiled. Therefore, it is better to have a smaller ring contact width, as this will reduce the required CSL thickness, hence the loss will be reduced and the overall device performance will be boosted.

Now that it has been established that a ring contact with a small width is better for device performance, further simulations were carried out to investigate the required CSL thicknesses for different device diameters with a fixed contact width of 20 μm. A ring contact width of 20 μm was used as if these devices were realized the contact resistance would need to be kept low. *Figure 5.14a* shows the required CSL thickness for differing device radii, with a fixed ring contact width of 20 μm. The graph follows a linear trend, with a given device radius requiring 1.25 times as much thickness in the CSL. This shows that for each device radius there is an optimum thickness of CSL to give a uniform carrier distribution, while keeping the thickness low to reduce loss. Since a number of devices of different radii are made on the same wafer, this optimum value cannot be achieved for each case, requiring the fabrication run to be optimised for a specific device radius. Alternatively a CSL thickness could be selected that provided a uniform carrier distribution for the largest number of different device radii without too much of a penalty for the smaller devices. Using the fit from the graph a 120 μm CSL thickness would allow for uniform carrier distribution in devices up to 200 μm in diameter.

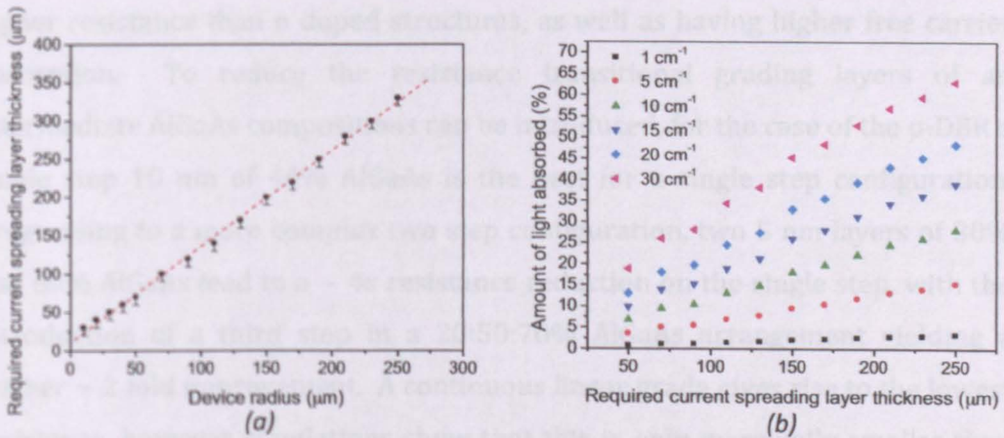

Figure 5.14 (a) Required current spreading layer thickness for different device radii with a fixed ring contact width of 20 μm (b) Modeled absorption as a function of current spreading layer thickness for different optical loss coefficients

Figure 5.14b shows the single pass absorption loss at different thickness of CSL for a number of different absorption coefficients. In each case the relationship is

linear with the minimum value and the gradient of each line increasing with a larger value of absorption coefficient. This graph highlights the importance of having a low doping level in the CSL, as the doping level is the major factor in determining the amount of loss in the device. Secondary to this, by keeping the CSL thickness small the amount of loss can be minimized for a given doping level.

Modelling of the contact geometry has shown that by reducing the ring contact width the required CSL thickness for a uniform carrier distribution can be reduced, and for a fixed contact width the optimum CSL thickness increases at a constant rate with device diameter. However, a decision still has to be made over the thickness of the CSL when realising the devices depending on the device radius required, as this will affect the performance of the devices of different radius manufactured.

5.7 Conclusion

In this chapter electrical and loss modelling of both n and p doped DBR structures has been discussed, as well as measurements of grown structures. Due to the lower mobility of holes within the DBR p doped structures have a higher resistance than n doped structures, as well as having higher free carrier absorption. To reduce the resistance transitional grading layers of an intermediate AlGaAs compositions can be introduced, for the case of the p-DBR a single step 10 nm of 44% AlGaAs is the best for a single step configuration. Progressing to a more complex two step configuration, two 5 nm layers of 30% and 60% AlGaAs lead to a ~ 4x resistance reduction on the single step, with the introduction of a third step in a 20:50:70% AlGaAs arrangement yielding a further ~ 2 fold improvement. A continuous linear grade gives rise to the lowest resistance, however simulations show that this is only marginally smaller than that of the 3 step design, and is significantly more technically challenging than that of the 3 step grade. In the case of the n-DBR, the change in mobility caused by the switch from a direct to an indirect conduction band means that only single step gradings with an AlGaAs composition of less than 35% yield lower resistance than an abrupt interface, with higher AlGaAs compositions negatively

affecting the device resistance. This is supported by measurements of grown n-DBR structures; with the lowest resistance given by a single step AlGaAs composition of 30%.

From the modelling of doping within the DBR structure is has been shown that in order to minimize loss that average doping level must be kept low, and that reduction of doping at the high field interface and increase of doping at the low field interface yield only small reduction in loss. Delta doping of the interfaces has been shown to have a worthwhile improvement in resistance, while only paying a small penalty in absorption loss. However, as seen from the SIMS data, the fixation of high doping levels at specific positions in the DBR structure is quite technologically challenging. Additionally, in order to improve the overall DBR performance, the doping incorporation into the p-DBR must be made more uniform either by adjusting the gas flows for different materials, or by using a different dopant where the incorporation does not vary so much with AlGaAs composition. Furthermore, the level of carbon incorporation into the n-DBR must be reduced as this reduces the free carrier concentration in that part of the structure.

From modelling of the current distribution due to a ring contact, it has been shown that a smaller ring contact width results in a smaller CSL thickness required for a Gaussian carrier distribution. In addition, for a fixed ring contact width of 20 μm, the CSL thickness required for a Gaussian carrier distribution varies linearly with the device radius, with the amount of absorption dominated by the absorption coefficient and hence the doping level of the substrate. In order for improved device performance a n-side ring contact arrangement is required, with a small ring contact width, this will allow a thinner CSL to be used. While the doping level of the substrate used for the CSL should be kept as low as possible, without negatively affecting the device resistance.

5.8 Further Work

Growth of the improved n and p-DBR designs should be carrier out and the material characterised to confirm the information produced from the modelling. Once this has been validated, these designs can be included in a full EP-VECSEL structure. Calibration of dopant incorporation into the different DBR materials should be carried out, so that there is not such a dramatic variation in dopant concentration in the DBR. Devices should be fabricated with different contact geometries so that the affect on the carrier distribution can be observed and hence its affect on device performance.

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6 Quantum Well Performance

6.1 Introduction

In previous chapters the electrical and optical performance optimisation of an EP-VECSEL device has been discussed, the final element to be discussed that requires optimisation is the active region. The active region is made up by a number of quantum wells (QWs) placed at the antinodes of the standing wave of the electric field, discussed in chapter 2. The number of QWs used in the active region as well as their thickness, composition and barrier material have a large effect on the overall device performance. As a high power output is desired from these devices, a number of parameters can be changed to improve performance. Equation *(6.1)* describes the output power (P_o) of an EP-VECSEL device [1]:

$$P_o = F_1 \frac{hv}{q} \eta_d (I - I_{th}) \tag{6.1}$$

where the differential efficiency, η_d, is given by:

$$\eta_d = \eta_i \frac{T_m}{A_i + T_m} \tag{6.2}$$

In equation *(6.1)* F_1 is the fraction of power out of the output coupler mirror, hv is the photon energy, q is the electron charge, I is the injected current and I_{th} is the threshold current. In equation *(6.2)* η_i is the internal efficiency, $T_m = ln(1/R)$ is the mirror loss , where R is the reflectivity and $A_i = \alpha_i L$, where α_i is the internal loss and L is the active region length. The internal efficiency is the ratio of current injected into the QWs that combines radiatively to the total injected current and can then be given by [2]:

$$\eta_i = \frac{J_{stim} + J_{spon}}{J_{stim} + J_{spon} + J_{non-rad} + J_{bar} + J_{leakage}} \quad (6.3)$$

Where J_{stim} is the current density contributing to stimulated emission, J_{spon} is the current density contributing to spontaneous emission, $J_{non-rad}$ is the current lost through non-radiative processes, J_{bar} is current lost to recombination in the barriers and $J_{leakage}$ is the current density that leaks from the active region.

Assuming adjustments to the active region result in no additional loss it can be seen from equation (6.2) that an improvement in the internal efficiency of the QWs, by reducing non-radiative recombination and leakage current, will result in an improved output power. The other parameter controlled by the active region design is the threshold current, I_{th}, where a reduction in its value will result in an increased power at rollover, due to reduced Auger recombination and extended thermal roll-over . These two improvements are illustrated in *Figure 6.1*, which plots the output power current characteristic for 3 different cases. The blue curve is the standard performance, while the red curve shows the behaviour for an improved internal efficiency and the green curve that of a reduced threshold with the same internal efficiency of the standard performance.

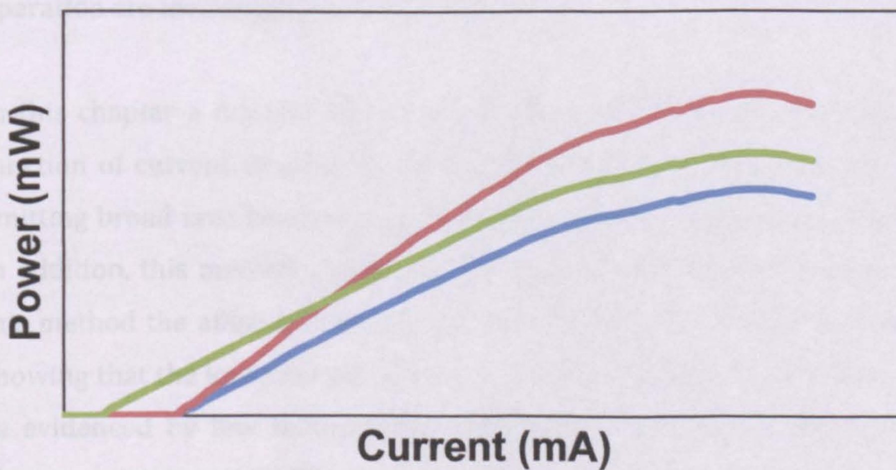

Figure 6.1 Output power as a function of current for different slope efficiencies and threshold currents

In each case the thermal roll over, dominated by the device resistance is assumed to occur at the same point. It should be noted that the maximum output power possible is a result of the interplay of internal efficiency, loss, threshold current, electrical resistance and thermal resistance. Where a reduction in thermal or electrical resistance will extend the point at which thermal rollover occurs, allowing the device to be driven to a higher current and hence a greater output power. As a result, improvements in internal efficiency and threshold current will be compounded by reductions in self-heating, yielding greatly improved performance.

However, it must not be forgotten that in order to achieve lasing in the first instance, the loss within the device must be equalled by the gain produced from the active region. In the case of the EP-VECSEL devices the losses are high due to the thick, doped substrate used for the current spreading layer and the high doping in the DBRs to reduce their resistance, discussed further in chapters 4 and 5. As a result a large gain is required to achieve lasing operation. The requirement for a large gain means that a number of QWs are required, with an increasing number of QWs resulting in an increased threshold current in the device [3]. Due to this trade-off the number of QWs required for lasing operation are investigated in this chapter.

In this chapter a method will be presented to measure the material gain as a function of current density for EP-VECSEL material by fabricating it into edge emitting broad area lasers and performing a length dependent characterisation. In addition, this method also yields the internal efficiency of the device. Using this method the affect QW interface roughness on the gain will be investigated, showing that the low internal efficiency can be attributed to interface roughness as evidenced by low temperature linewidth measurements and transmission electron microscopy (TEM). A method for reducing the roughness described will be proposed, leading to improved internal efficiency and reduced low temperature linewidth. Following on from this, the problems with extrapolating the gain current relationships to higher current densities will be discussed, where there are difficulties in inferring an improvement at current densities

required for EP-VECSEL operation, as measurements were carried out at low current densities. Finally, an analysis of the gain current relationships produced for active regions containing 3, 6 and 9 QWs will be presented, showing that improved gain characteristics can be obtained if 3 QWs are used instead of 6.

6.2 Material Gain Characterisation

Since the amount of time required to make an EP-VECSEL device was approximately 3 weeks, with a large number of fabrication steps that could result in device failure, and the requirement for extensive output coupler characterisation, it would take a long time to provide feedback on the performance, as a result in changes in the growth of a new design. In order to speed up this process and improve feedback on device growth, EP-VECSEL material, grown on n^+ wafers, was fabricated into broad area edge emitting lasers. This is similar to the methods proposed in [4] [5].

This was carried out by first photolithographically defining a top contact, and then an Au/Zn/Au contact was deposited into this region. The contact was rapidly thermal annealed at 360 °C and then a ridge was photolithographically defined. A 1:1:1 mixture of acetic acid, hydrobromic acid and potassium dichromate was used to wet etch the device ridge through the active region, to a depth of ~ 5.6 μm. The substrate of the processed material was then mechanically thinned to a thickness of 200 μm to allow for devices to be easily cleaved. An InGe/Au back contact was then blanket deposited onto the substrate, and was annealed at 340 °C. The processed material was then scribed into different bar lengths; the bars were then mounted on aluminium nitride tiles using an indium paste and the 100 μm wide ridges on each bar were wire bonded to contact pads on the tile.

A schematic of the processed device is shown in *Figure 6.2*, where L was the device length and W is the ridge width, which was 100 μm in this case. The upper region of the ridge is the p-DBR, with the thin grey region denoting the active region, clad on the bottom with the n-DBR (red) and the thinned substrate.

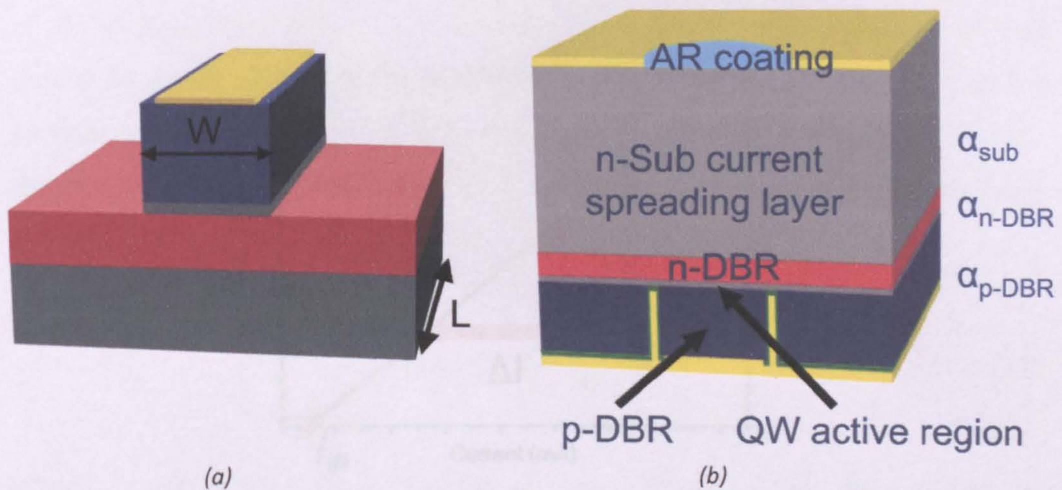

Figure 6.2 (a) Schematic of edge emitting laser with ridge width and cavity length labeled (b) Schematic of EP-VECSEL structure with important device areas labeled

The output power-current characteristic for a number of devices of each length was measured using an ILX pulsed current source and a HP power meter. A pulsed current source was used to minimise self-heating in the device, where a 1 % duty cycle and a 5 μs pulse width were used. A special effort was made to reduce the connector lead length and therefore the capacitance of the device to reduce the ringing that occurred during each pulse. The measurement head of the power meter was aligned in very close proximity to the device under test to collect the maximum amount of power produced.

Figure 6.3 shows an illustration of the power-current relationship measured for single device of a given length. From the graph the slope efficiency, $\Delta P/\Delta I$, can be obtained by measuring the gradient of the curve. Extrapolating the measured gradient back to the point that it intersects the x-axis yields the threshold current, I_{th}. This process was repeated for a number of devices at each different device length. Since the mirror loss is inversely proportional to the cavity length, different lengths yield differing value of mirror loss and therefore devices of different length exhibit different values of $\Delta P/\Delta I$ and I_{th}.

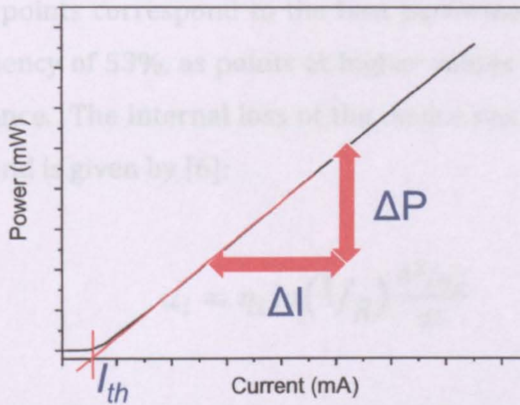

Figure 6.3 Output power as a function of current for an edge-emitting laser with the slope efficiency and threshold current labeled

Using equations *(6.4)* and *(6.5)* [6] these measured values can be transformed into the differential efficiency, η_d, and the threshold current density, J_{th}.

$$\eta_d = 2\frac{dP}{dI}\frac{q\lambda}{hc} \tag{6.4}$$

$$J_{th} = \frac{I_{th}}{W_{ridge}L} \tag{6.5}$$

Where q is the electron charge, h is Plank's constant, c is the speed of light, λ is the wavelength of emission and the 2 is a result of their being two equally reflective mirror facets transmitting light. In equation *(6.5)*, W_{ridge} is the device ridge width and L is the cavity length of the device.

Using the values calculated from equations *(6.4)* and *(6.5)* for different device lengths it was possible to plot these values as a function of length. This analysis was carried out for the EP-VECSEL material described in chapter 4 (TS522). *Figure 6.4a* plots the inverse differential efficiency against the cavity length. The data shows a linear trend with shorter cavity lengths having a smaller value and larger cavity lengths having a larger value. By fitting a straight line to the data it was possible to extract the internal efficiency, η_i, which is given by the intercept

of the straight-line fit to the y-axis. The line was fit to the lowest set of data points, as these points correspond to the best performance in each case, giving an internal efficiency of 53%, as points at higher values are indicative of poorer device performance. The internal loss of the device can also be calculated from the best fit line and is given by [6]:

$$\alpha_i = \eta_i \ln\left(1/_R\right) \frac{d\,1/\eta_d}{dL} \qquad (6.6)$$

Where $R=R_1R_2$ the reflectivities of the as cleaved facets, which were ~ 0.32 per facet.

In a similar manner, the transparency current density, J_0, could be obtained by plotting the inverse cavity length, $1/L$, against the threshold current density, J_{th}; this is shown in *Figure 6.4b.* Again, a linear best fit was applied to the lowest data points, as these were from the best performing devices in each case. The value of the transparency current density is given by the intercept of the best fit line with the y axis, which corresponds to a device with an infinitely long cavity length with no mirror loss from the facets. This value determines how much current is required per cm in order for there to be no absorption loss from the QWs.

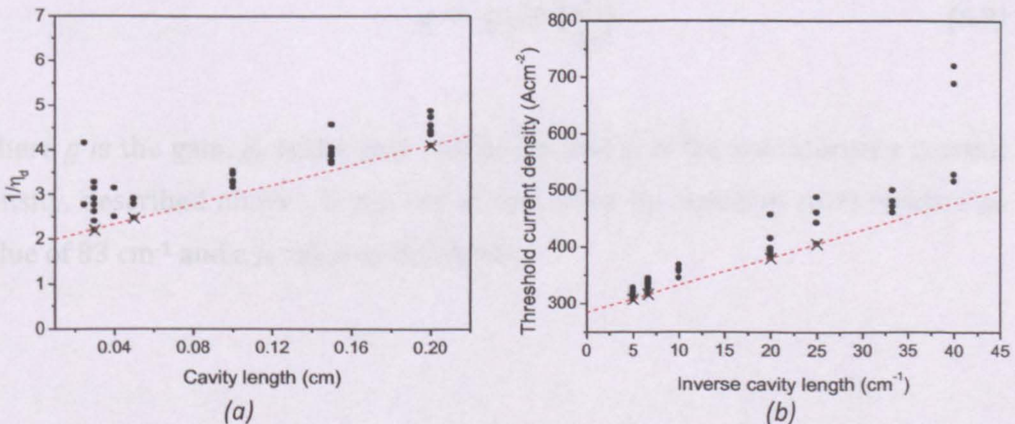

Figure 6.4 (a) Inverse external quantum efficiency as a function of cavity length for an edge emitting laser with a 100 µm wide ridge driven in a pulsed regime (b) Threshold current

density as a function of inverse cavity length for an edge emitting laser with a 100 μm wide ridge driven in a pulsed regime

Once the internal loss had been obtained the mirror loss for the different bar lengths could be calculated using [6]:

$$\alpha_m = \frac{1}{2L}\ln\left(\frac{1}{R_1 R_2}\right) \tag{6.7}$$

Then, using the threshold current density for each length and the relationship described in equation (6.8), a gain-current relationship for the material could be constructed.

$$\Gamma g_{th} = \alpha_i + \alpha_m \tag{6.8}$$

Where Γ is the optical confinement factor for the active region and g_{th} is the threshold gain. *Figure 6.5* plots the net modal gain as a function of current density for the 6 QW material (TS522) described in chapter 4, grown on a n^+ substrate. As described in chapter 4 and an empirical logarithmic relationship can be fitted to the data and takes the form [7]:

$$g = g_0 ln\left(\frac{J}{J_0}\right) \tag{6.9}$$

Where g is the gain, g_0 is the gain coefficient and J_0 is the transparency current density, described above. Using the fit described by equation (6.9) yields a g_0 value of 83 cm^{-1} and a J_0 value of 283 Acm^{-1}.

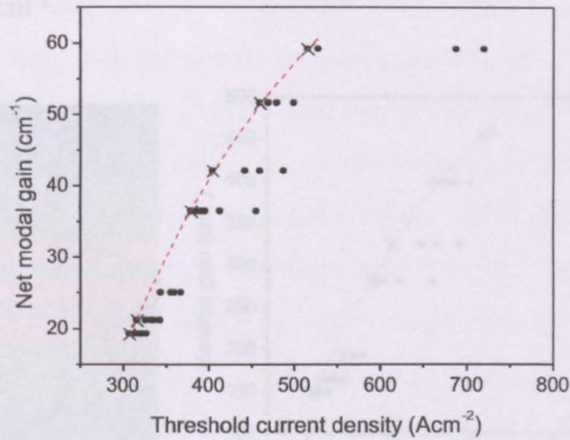

Figure 6.5 Net modal gain as a function of threshold current density for an edge-emitting laser with a 100 µm wide ridge

However, the gain curve shown in *Figure 6.5* cannot be directly compared to data produced through the same analysis for different material, as the interaction between the QWs and the electric field will be slightly different in each case. *Figure 6.6a* shows the overlap of the optical standing wave with the QWs in the active region, the QWs are shown in red, with their barriers in grey. The blue regions are the cladding to the active region into which the electric field will penetrate. By calculating the optical confinement factor for each active region design it was possible to obtain the material gain by dividing the total loss by the confinement factor.

The confinement factor of the structure was calculated by modelling it in the FimmWave optical mode solving modelling software [8]. The epitaxial structure and refractive index of each layer was entered into the software, as well as the etch depth and ridge width of the device. For the 6 QW structure (TS522) described in chapter 4 the calculated value of confinement factor was 0.129. Using this value *Figure 6.6b* was generated, which plots the material gain, for the EP-VECSEL described in chapter 4, as a function of current density. The plot has the same shape as *Figure 6.5* but with the value of gain at each point increased.

The empirical fit can also be applied yielding the same value of J_0 but a larger value of g_0, 683 cm^{-1}.

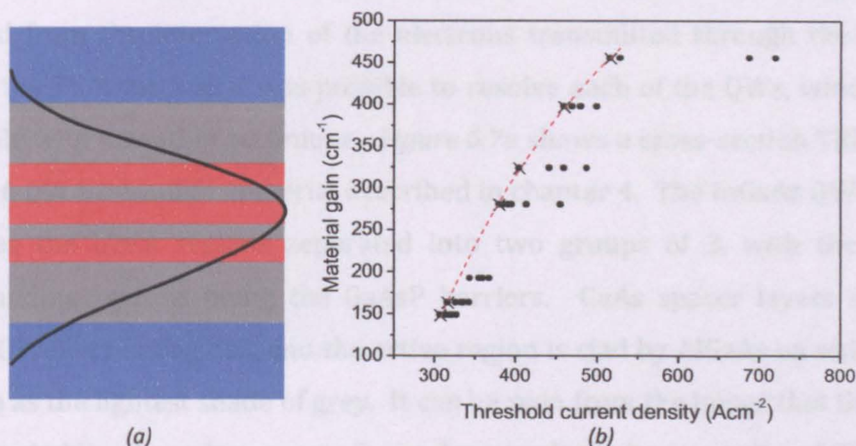

Figure 6.6 (a) Diagram of the interactive between the electric field and the QWs (b) Materials gain as a function of threshold current density for a 6 QW edge emitting laser with a 100 μm wide ridge

Using the method described it is possible to compare epitaxy with different structures, using a number of different figures of merit such as the internal efficiency, transparency current density and internal loss. As well as observe the gain current density behaviour of the material. In this manner is it possible to determine which epitaxial design yields the best device performance.

6.3 Reducing QW Roughness

As discussed in the introduction to this chapter, the internal efficiency of the QWs in the active region plays a large part in the overall output power obtainable for a given epitaxial structure. From the above analysis of the EP-VECSEL material described in chapter 4 (TS522), it was seen that the internal efficiency was quite low η_i = 53 %. As a result of this value, investigations were carried out to determine the interface quality of the QWs with their associated barriers. This was carried out in two ways, firstly by transmission electron microscopy (TEM) and secondly by low temperature electroluminescence (EL) linewidth measurement.

In order for the sample to be imaged using the TEM it must first be thinned to the order of 100 - 200 nm. An electron beam is then shone into the sample with electrons interacting with the media as they pass through it. The image is then formed from the interaction of the electrons transmitted through the sample. Using the TEM method it was possible to resolve each of the QWs, which is not possible with any other technique. *Figure 6.7a* shows a cross-section TEM image of the 6 QW EP-VECSEL material described in chapter 4. The InGaAs QWs can be seen as the black regions separated into two groups of 3, with the darker surrounding regions being the GaAsP barriers. GaAs spacer layers separate these QW/barrier regions, and the active region is clad by AlGaAs on either side, shown as the lightest shade of grey. It can be seen from the image that the lower AlGaAs cladding layer has a wavy form. As a result the lower region of QWs have a modulation in thickness along their length. The upper set of QWs also has a slight modulation in thickness, but to a much lower degree than the lower set. This suggests that the strain induced by the first set of QWs ameliorates the thickness modulation in the above structure. It is suggested that the high level of doping in the n-DBR, as evidenced by the SIMS analysis in Chapter 5, is a factor in the rough layer growth, it is therefore proposed that reducing the doping level will mitigate the rough layer growth.

To carry out the low temperature EL measurements, a 2 mm long broad area laser fabricated for the material characterisation described above, with a 100 μm ridge width, was placed in a closed loop helium cryostat. A thermal paste was used between the tile the device was mounted on and the cold finger in order to ensure good thermal conduction. A large NA lens was used to capture as much of the light as possible produced by the device under test, which was then collimated and another lens then reduced the spot size and focused it into a multimode optical fibre. The device was then cooled down to 20 K and the EL spectra were taken at a number of different CW currents. *Figure 6.7b* shows the 20 K EL spectrum at a current density of 250 Acm^{-2} for the 6 QW EP-VECSEL material (TS522) described in chapter 4. The EL spectrum has a smooth shape with a more pronounced shoulder on the higher energy side. The measured full

width at half maximum (FWHM) linewidth was 13 meV for this sample. This value was ~ 3 times greater than the expected value [9].

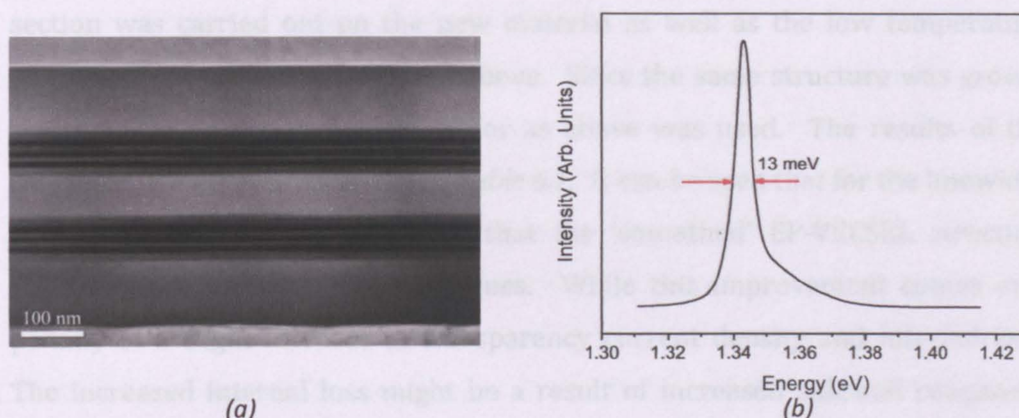

Figure 6.7 (a) TEM image of interface roughness in QW active region (TS522) (b) 20 K EL spectrum for a 6 QW edge emitting laser with a ridge width of 100 μm at a threshold current density of 250 Acm^{-2}, where the linewidth is marked in red

Combining this large EL linewidth with the thickness modulation observed in the TEM image it is clear to see that the broadness of the linewidth is a result of emission from QWs with slight differences in thickness [9] [10]. A consequence of this for device applications could be a reduction of peak gain, but a wider gain bandwidth [10].

Since the thickness modulation in the QWs originates from interface roughness in the n-DBR, which in caused by the introduction of the silicon dopant (Si_2H_6) into the AlGaAs layers, as it promotes inhomogeneous Al-Ga interdiffusion [11]. To remedy this the arsine (AsH_3) flow in the high concentration AlGaAs layers was increased. By doing this the amount of native arsenic atoms on the surface of the wafer are increased, which decreases the surface mobility of the aluminium, as it is now more likely to meet an arsenic atom. This reduction in surface mobility inhibits the coalescing of material due to strain in the material, that leads to wavy layer growth.

Using this new growth technique a new EP-VECSEL structure was grown with identical layer thickness and compositions to that described in chapter 4 (TS797). The material characterisation method described in the previous section was carried out on the new material as well as the low temperature linewidth measurement described above. Since the same structure was grown, the same value of confinement factor as above was used. The results of the measurements are summarized in *Table 6.1*. It can be seen that for the linewidth and the internal efficiency values that the 'smoothed' EP-VECSEL structure (TS797) have greatly improved values. While this improvement comes at a penalty of a slight increase in transparency current density and internal loss. The increased internal loss might be a result of increased sidewall roughness produced by the etch process and not something intrinsically related to the active region.

Device	Linewidth (meV)	η_i (%)	J_o (Acm^{-2})	α_i (cm^{-1})
Rough (TS522)	13 ± 0.1	53 ± 3	283 ± 5	13 ± 2
Flattened (TS797)	7 ± 0.1	71 ± 3	327 ± 5	18 ± 2

Table 6.1 Comparison of laser material parameter for active regions with different interfaces roughness's

Figure 6.8a plots the material gain as a function of current density for the two 6 QW EP-VECSEL structures. The black dots plot the behaviour of the 'rough' QW structure (TS522) analysed in the previous section, while the red dots show the behaviour of the 'smoothed' QW structure (TS797). In each case the dotted lines are the empirical fits to the data described in the previous section. It can be seen from the fits to the data that while the 'rough' QWs have a lower transparency current density than the 'smooth' structure, the 'smooth' structure has a steeper gradient resulting in a g_0 = 925 cm^{-1}, compared to 605 cm^{-1} in the 'rough' QW device. This difference in gradient was important, as it will result in improved gain at higher current densities.

As shown in chapter 4, due to the high losses in the EP-VECSEL structure they operate at much higher current densities, ~ 1 $kAcm^{-2}$, than those of the edge emitting devices used in the characterisation. In order to gain an illustration of the gain at these sorts of current densities the empirical curves fit to the data were extrapolated to these values. *Figure 6.8b* replots the data from *Figure 6.8a* with the empirical fits extrapolated to much higher current densities. Due to the difference in gradients of the two curves, the 'smooth' QW structure achieves a much higher gain at higher current densities, resulting in a difference of ~ 300 cm^{-1} of material gain at 1 $kAcm^{-2}$, with this difference increasing at increased current densities. The improved gain will lead to reduced threshold currents in EP-VECSEL devices as the gain required to satisfy the loss can be obtained at a lower current density.

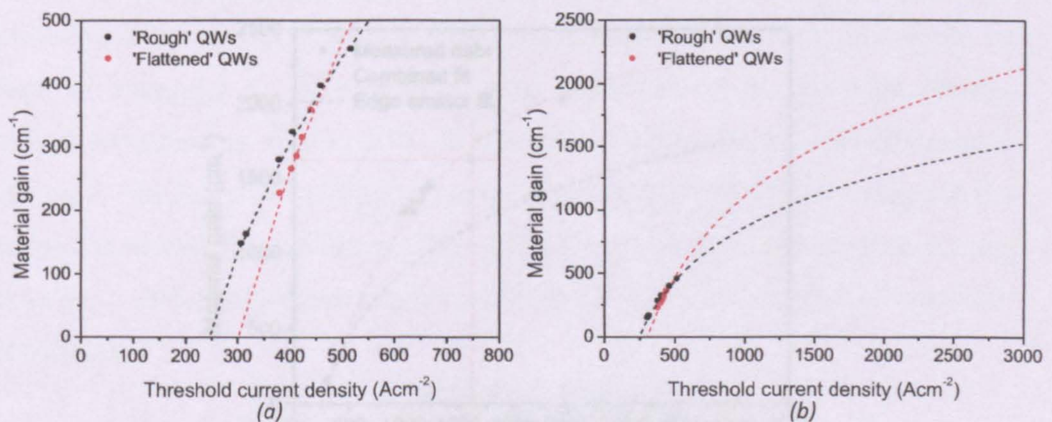

Figure 6.8 (a) Material gain as a function of threshold current density for active regions with different levels of interface roughness (b) Extrapolated material gain as a function of threshold current density for active regions with different levels of interface roughness

However, this extrapolation maybe misleading. By using the gain characterisation method described in chapter 4 it was possible to obtain the gain curve over the EP-VECSEL operating range. Combining this data with the data obtained from the edge emitter characterisation it was possible to fit a different curve to the data. *Figure 6.9* plots the material gain as a function of current density for the combined data from the two characterisation methods. Empirical fits are displayed for a fit to the entire data set (red) and to the data from the edge emitter characterisation (black). The solid red lines in the figure denote the

material gain required for the 84 % output coupler mirror (~ 1650 cm^{-1}), from which the highest output power was achieved, discussed further in chapter 4. The figure shows a large disparity in the measured values and those of the extrapolation, with a difference of ~ 300 cm^{-1} at 1 $kAcm^{-2}$. If the extrapolated fit were true then the amount of gain required for lasing with the 84 % output coupler mirror was only achieved at very high current densities, at this level of injection the self-heating would be large and result in reduced device performance. This suggests that the improvement in gain using the 'smoothing' method indicated by the extrapolation method will be an underestimate of the actual gain in the device. At this time fabrication of the 'smooth' QW material (TS797) into EP-VECSEL devices in order to characterize this behaviour has not been carried out.

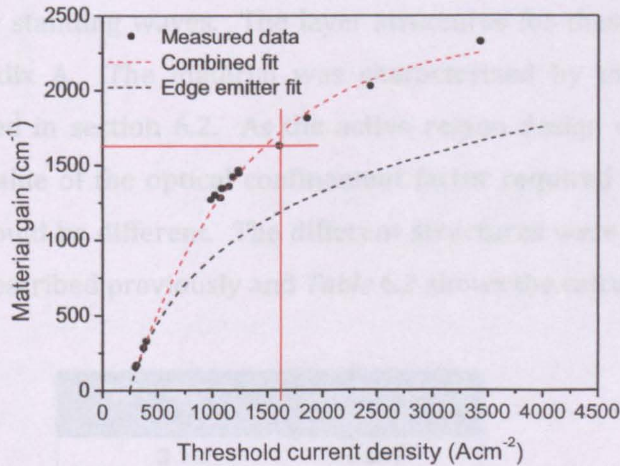

Figure 6.9 Measured material gain as a function of threshold current density for both edge emitter and combined edge emitter EP-VECSEL characterisation techniques, the solid red line shows the gain required for the highest output power achieved in chapter 4

6.4 Number of Quantum Wells

As highlighted previously in the introduction to this chapter, the number of QWs in the active region of a device will have an effect on the threshold current. This is because as the number of QWs is increased a greater number of carriers are required so that each QW becomes transparent, leading to an increased J_0 of the material. Due to the losses in an EP-VECSEL structure being large, a large gain is

required to achieve lasing and hence a number of QWs must be used. However, above the limit required by a given loss in a device, additional QWs will have a negative impact on device performance as well as make growth of the structure more complicated.

In order to test how many QWs are required in an EP-VECSEL device, three different devices were grown with 3, 6 and 9 QW active regions respectively. In each case the DBR design was the same as that of the structure in chapter 4, but the method for reducing n-DBR roughness was included. The 3 QW device (TS838) had a λ active region with the 3 QWs place at the antinode in centre. The 6 QW device (TS797) had the same epitaxial structure as the device described in chapter 4. Finally the 9 QW device (TS830) had a 2λ cavity with three separate groups of 3 QWs separated by GaAs spacer layers centred at antinodes in the standing waves. The layer structures for these devise can be found in appendix A. The material was characterized by the edge emitter method described in section 6.2. As the active region design was different in each case, the value of the optical confinement factor required to compute the material gain would be different. The different structures were modelled using FimmWave as described previously and *Table 6.2* shows the calculated values for each design.

No of QWs	Confinement factor (Γ)
3	0.087
6	0.129
9	0.152

Table 6.2 Modeled confinement factor for active regions with different numbers of QWs

Figure 6.10 plots the material gain as a function of current density for EP-VECSEL material with active regions containing 3, 6 and 9 QWs. In each case a number of empirical fits have been added, with the solid line being the fit and the dashed line being +5 % confidence bound and the dotted line being the -5 % confidence bound, representing a ±5% error in the measurement. These fits were added to

try and compensate for the extrapolation error obtained by not having any data points at high current densities, which is systematic in this case. The horizontal red line in the figure indicates the amount material gain that was required to achieve the highest output power in devices presented in chapter 4. It can be seen from the plot that the 3 QW material (TS838) has the lowest J_0 and the highest g_0, followed by the 6 QW (TS797) and finally the 9 QW material (TS830). The value of J_0 behaves as expected, with its value increasing with an increasing number of QWs. However, the value of g_0 does not behave as expected.

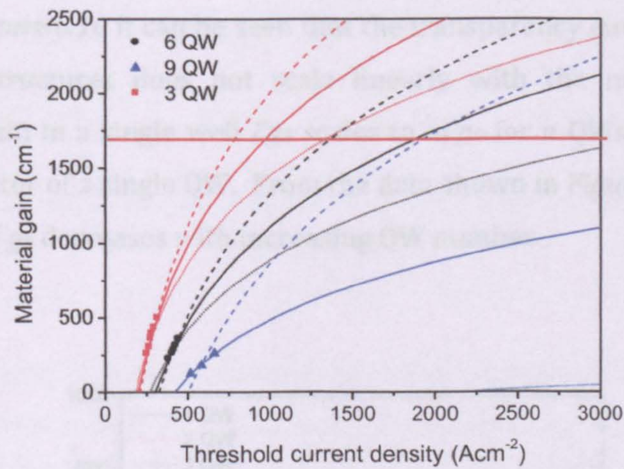

Figure 6.10 Measured material gain as function of threshold current density for edge emitting devices with different numbers of QWs in the active region (solid horizontal red line shows the amount of gain required for the highest output power achieved in an EP-VECSEL device, as shown in chapter 4

Observing the horizontal red line in *Figure 6.10*, switching from a 6 QW device to a 3 QW structure could result in a threshold current density reduction of ~ 1000 Acm^{-2} for the same gain, this could significantly improve device performance. However, as stated in the previous section the extrapolation of the fits to high current density is risky, especially in the case of the 3 QW device as it is unknown at what current injection level the gain will begin to saturate. In this case the amount of gain suggested at this current level would be an overestimate. Nonetheless, material gain values in excess of 2000 cm^{-1} have been reported from 3 QW devices with the same QW material [12], adding strength to the

predicted case. In order to verify the 3 QW performance at high current densities, EP-VECSELs would need to be fabricated and characterised as described in chapter 4.

The behaviour reported in other literature [13], [3] shows a crossing of the gain curves at higher current densities for increasing numbers of wells, indicating that there is a trade off in the number of wells depending on the amount of gain required, this is shown in *Figure 6.11*. However, they use a number of assumptions, firstly, that J_0 for a single QW scales to nJ_0 for n QWs. From the data presented in *Figure 6.10* it can be seen that the transparency current density for the different structures does not scale linearly with the number of QWs. Similarly, the gain in a single well Γg_0 scales to $n\Gamma g_0$ for n QWs, where Γ is the confinement factor of a single QW. From the data shown in *Figure 6.10* it is clear that the value of g_0 decreases with increasing QW number.

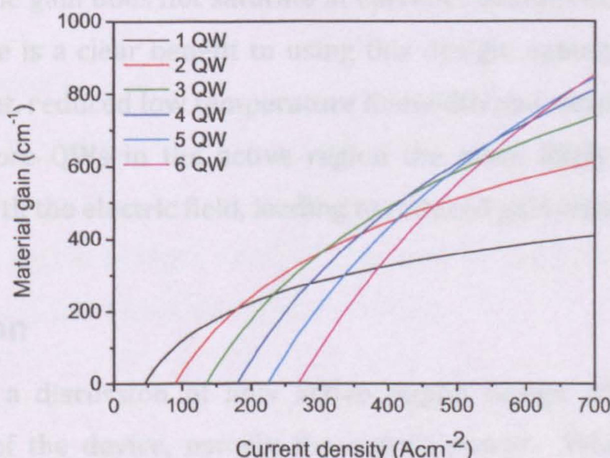

Figure 6.11 Modeled material gain as a function of threshold current density for an active region containing different numbers of QWs

It is proposed that the strain caused by adding QWs to the active region degrades the interface quality, as presented in the previous section. This is supported by the low temperature linewidth measurements presented in *Table 6.3*, taken under the same conditions as mentioned previously, with the 3 QW structure

(TS838) having the lowest linewidth and the 9 QW device (TS830) the highest. Also presented in the table are the internal loss and internal efficiency, it is unknown as to why these values vary in a random manner with the number of QWs, where an increase in the internal loss with an increasing number of QWs would be expected [14].

No of QWs	Linewidth (meV)	η_i (%)	G_o (cm^{-1})	J_o (Acm^{-2})	α_i (cm^{-1})
3	5.8±0.1	61±3	1066±5	227±5	15±2
6	7.2±0.1	71±3	924±5	327±5	18±2
9	10.3±0.1	56±3	557±5	451±5	10±2

Table 6.3 Comparison of laser material values for active regions containing different numbers of QWs

Assuming that the gain does not saturate at current densities of 1 $kAcm^{-2}$ for the 3 QW case, there is a clear benefit to using this design, namely reduced device threshold current, reduced low temperature linewidth and simplified growth. In addition, the more QWs in the active region the more likely there will be a misalignment with the electric field, leading to reduced gain enhancement.

6.5 Conclusion

In this chapter a discussion of how active region design effects the output characteristics of the device, namely the output power. Where, the internal efficiency, transparency current density and threshold gain are critical for obtaining good device performance. A method for characterising the factors mentioned above has been presented, by fabricating edge emitting lasers from EP-VECSEL material and performing a length dependent analysis. Performing this analysis on the material used in chapter 4, showed an undesirably low internal efficiency. TEM analysis coupled with low temperature linewidth measurements showed a broadening in the low temperature EL emission corresponding to a roughening of the QW-barrier interface. A method for

smoothing this interface discontinuity has been presented, where the arsine (AsH_3) pressure was increased in the growth of the AlGaAs layers. Characterisation of this material exhibited improved internal efficiency, reduced low temperature linewidth and increased threshold gain coefficient. However, extrapolation of the data, required to determine the benefit of performance for an EP-VECSEL might be misleading as a fit using only points obtained for low current densities resulted in an under estimation of the gain.

Analysing EP-VECSEL material containing active regions with 3, 6 and 9 QWs showed that it would be beneficial to use a 3 QW based active region (TS838), as it exhibited the highest material gain. However, the gain data presented is not as expected, with a decrease of gain with an increasing number of well as opposed to increasing. It is suggested that the addition of extra QWs to the structure adds additional strain causing roughing of the QW-barrier interface, this is supported by the broadened low temperature linewidth values for the 6 and 9 QW devices.

6.6 Further Work

Fabricate 3, 6 and 9 QW materials into EP-VECSEL devices to determine performance at high current densities. Grow EP-VECSEL structures with improved active region designs, where the carrier confinement is improved by using $Al_{0.2}Ga_{0.8}As$ spacer layers as opposed to GaAs.

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7 Summary and Future Work

In this section the major design aspects of this thesis will be summarized and improvements on the current constituent parts of the designs will be suggested. Chapter 1 gave an introduction into the subject area, with discussions of VCSEL, OP-VECSEL and EP-VECSEL technologies. Chapter 2 introduced the important areas of design in an EP-VECSEL device and methodologies for their optimisation. Chapter 3 described how the EP-VECEL devices were fabricated, providing a discussion for specific areas of process optimisation. Chapter 4 presented measurements from fabricated EP-VECSEL devices, with discussions of device characterisation, the affect of substrate doping, beam quality, power scaling and thermal properties. Chapter 5 investigated methods for improving electrical aspects of device operation, with improved n and p DBR designs proposed. In addition, analysis of SIMS data for an EP-VECSEL and n-DBR were presented, along with an investigation of the top contact geometry. Finally, Chapter 6 provided a discussion of the QW active region, first by analysing the epitaxial material used in chapter 4 and then proposing improvements to the growth process. A comparison of a 3, 6 and 9 QW active region was then presented, where the trade offs been the optimum number of QWs was examined.

Firstly concentrating on the n-DBR design, whose optical properties were discussed in chapter 2 and electrical properties in chapter 5. In chapter 2 it was shown that a high reflectivity could be maintained over a large wavelength range as long as the refractive index contrast between the DBR layers could be kept high, *i.e* by having a thin grading layer. *Figure 7.1a* shows the existing DBR design, with the composition for a single period consisting of a 73.7 nm 80 % AlGaAs layer with a 10 nm 47 % AlGaAs grading layer and a 60 nm GaAs layer, where the grading layer is used to reduce resistance. The doping level in this structure is $2x10^{18}$ cm^{-3}. It was shown in Chapter 5 that the resistance of the n-DBR can be reduced significantly by reducing the concentration of aluminium in

the grading layer from 47 % to 30 %. This is due to the shift from a direct to an indirect band gap in the AlGaAs above 45 %, causing a reduction in mobility.

Taking this into account, *Figure 7.1b* shows the improved design for the n-DBR, where the grading layer thickness is maintained at 10 nm, but the aluminium composition in the AlGaAs layer has been reduced to 30 %. Also discussed in Chapter 5 was the doping level, where an increased doping level will lead to a reduction in resistance but also an increase in loss. Since light is also coupled back into the n-DBR from the external cavity it is important to keep the loss in the n-DBR low as the light will perform a double pass through this structure. As a result, there is little benefit to the complex doping schemes discussed in Chapter 5; hence a doping level of $2x10^{18}$ cm^{-3} would be sufficient. In addition, the reflectivity of the n-DBR with regard to beam quality was discussed in Chapter 4, the discussion suggested that a reduction in the n-DBR reflectivity would allow for stronger control of the mode by the output coupler mirror, leading to improved beam quality. As a result, it is suggested that the number of n-DBRs be reduced from 12 to 9 pairs. This reduction will also beneficial for the decrease of dispersion in a mode locked device.

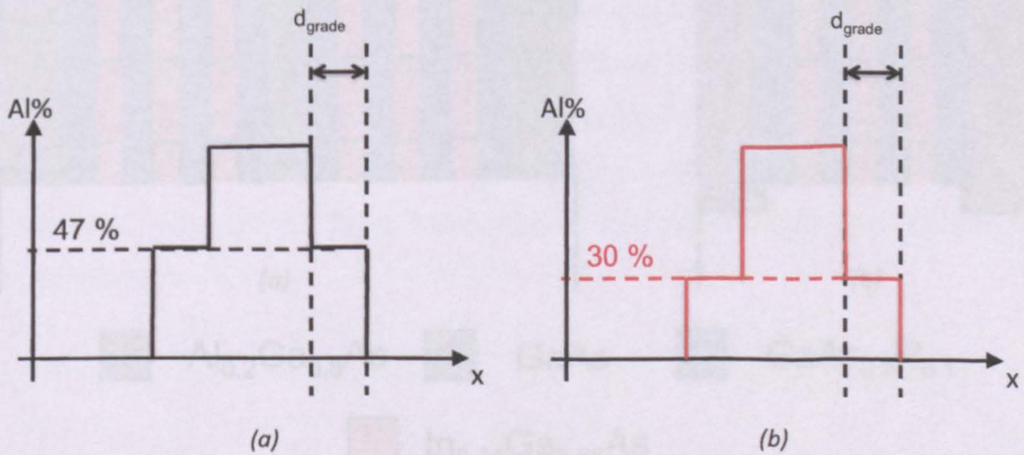


Figure 7.1 (a) Schematic of current n-DBR design (b) Schematic of improved n-DBR design

The performance of active regions with different numbers of QWs was discussed in Chapter 6, where the internal efficiency, gain coefficient, transparency current density and low temperature linewidth were all examined for a number of

different configurations. *Figure 7.2* shows the active region design used to achieve the results presented in Chapter 4, It contains 6 InGaAs QWs separated in two groups of three that are positioned at the antinodes of the standing wave in the electric field. The QWs have $GaAs_{0.9}P_{0.1}$ barriers used for partial strain compensation and GaAs spacer regions to separate the sets of QWs. From the measurements in Chapter 6 it was shown that 3 QWs have an improved gain coefficient and a lower transparency current density, allowing for a reduced threshold current in the device and more tolerance of loss.

Taking this into account, *Figure 7.2b* shows the improved active region design containing 3 QWs placed at a single antinode, as described in Chapter 6. In addition to the reduction in the number of QWs, the spacer regions have been changed from GaAs to 20 % AlGaAs, providing better carrier confinement, and hence increasing the internal efficiency. Another added benefit is a simplified growth allowing for better alignment of the QWs to the electric field standing wave, leading to an improved gain enhancement factor.

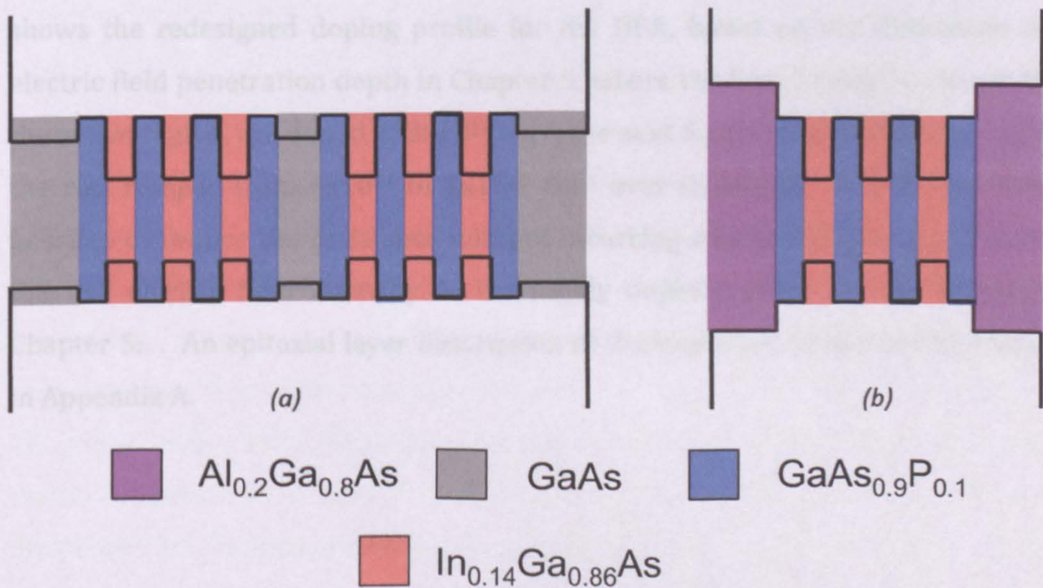


Figure 7.2 (a) Schematic of current EP-VECSEL active region design with 6 QWs (b) Schematic of improved EP-VECSEL active region with 3 QWs and higher barriers

The next region of the structure to be redesigned is the p-DBR, where the most benefits in device performance can be obtained, due to the high resistance and high optical loss nature of the structure. In addition, heat generated in the device

has the biggest negative effect on the output power, reducing the slope efficiency and causing the device to thermally rollover prematurely. *Figure 7.3a* shows the current p-DBR design, with the top region showing the composition for a single DBR period, with a single 47 % AlGaAs 10 nm step, and the bottom region showing the doping level throughout the structure. In Chapter 5 it was shown that the introduction of additional grading layers to DBR interface could reduce the DBR resistance, with 3 discrete steps having a comparable resistance to a linear graded structure.

Using this information the p-DBR could be redesigned, with the top part of *Figure 7.3b* showing the proposed DBR composition of the new structure, where 3 intermediate steps are used. In addition, if linear grading is possible on the growth reactor it should be carried out as further performance gains can be made. The thickness of the grading region should be kept constant at 10 nm to maintain the high reflectivity of the DBR, hence each of the 3 grading regions should have a thickness of 3.3 nm. Further to this, the bottom part of *Figure 7.3b* shows the redesigned doping profile for the DBR, based on the discussion of electric field penetration depth in Chapter 5, where the first 5 periods, closest to the active region, are doped at $2\text{x}10^{18}$ cm^{-3}, the next 5 periods at $4\text{x}10^{18}$ cm^{-3} and the rest ramped from $6\text{x}10^{18}$ to $1\text{x}10^{19}$ cm^{-3} over its length. In this way it is possible to reduce the resistance without incurring a large loss penalty, due to the low electric field intensity in the highly doped regions, as discussed in Chapter 5. . An epitaxial layer description of the improved device can be found in Appendix A.

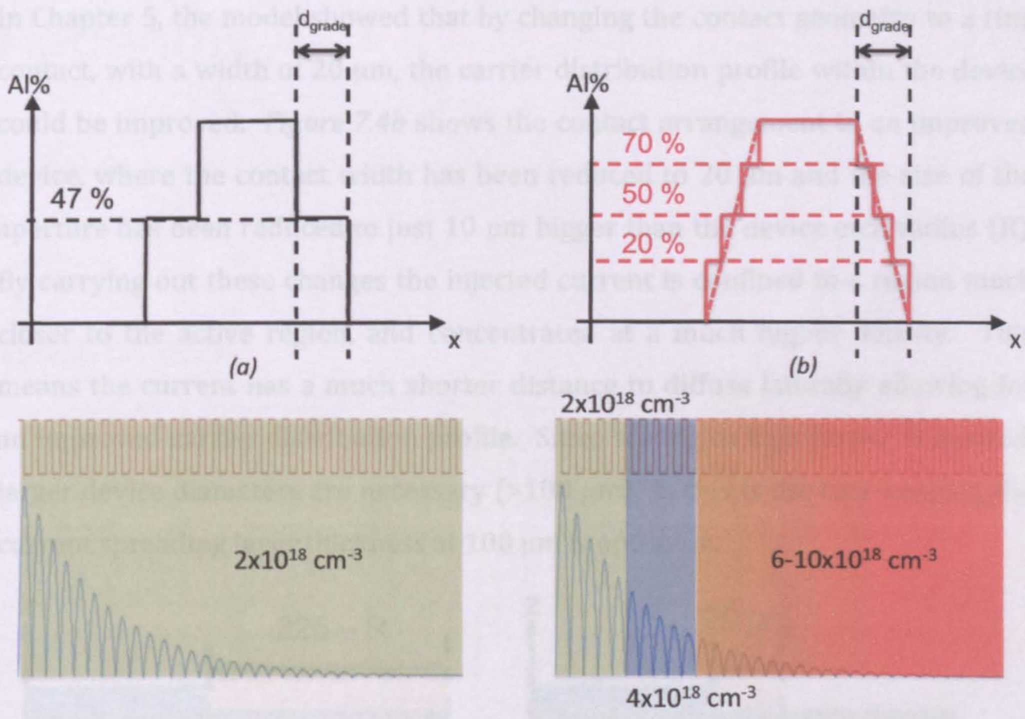


Figure 7.3 (a) Top: Schematic of current p-DBR design Bottom: Schematic of current p-DBR doping profile with index profile (red) and E-field intensity (Blue) (b) Top: Schematic of improved p-DBR design Bottom: Schematic of improved p-DBR doping profile with index profile (red) and E-field intensity (Blue)

Finally, based on the current spreading modelling in Chapter 5, it is proposed that experiments be carried out to verify the results of the modelling. As this would require only a slight alteration to the photolithography masks for processing, but could provide further performance enhancements. *Figure 7.4a* shows the existing contact arrangement in the working EP-VECSELs described in Chapter 4, where the figure shows a cross-section through the device, the gold region is the contact, the grey area is the current spreading region and the blue area is the anti-reflective coating. R denotes the electrical isolation etch radius and H the current spreading layer thickness. In the current device design, each device is cleaved into a chip 500 µm², where the contact extends across the whole area, apart from where the anti-reflective coating is placed. In addition, the current spreading layer thickness is set to 100 µm. In Chapter 4 it was shown that for devices with diameter greater than or equal to 100 µm, the carrier distribution profile is non-uniform, leading to non-ideal device operation.

In Chapter 5, the model showed that by changing the contact geometry to a ring contact, with a width of 20 μm, the carrier distribution profile within the device could be improved. *Figure 7.4b* shows the contact arrangement in an improved device, where the contact width has been reduced to 20 μm and the size of the aperture has been reduced to just 10 μm bigger than the device etch radius (R). By carrying out these changes the injected current is confined to a region much closer to the active region, and concentrated at a much higher density. This means the current has a much shorter distance to diffuse laterally allowing for an improved carrier distribution profile. Since scaling to high power is desired, larger device diameters are necessary (>100 μm), as this is the case keeping the current spreading layer thickness at 100 μm is optimum.

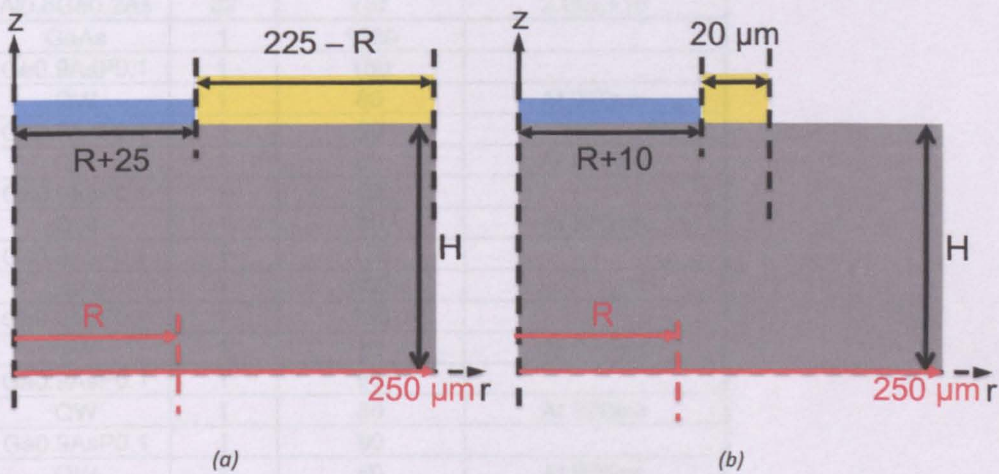


Figure 7.4 (a) Current device contact layout (b) Improved device contact layout with ring contact width reduced to 20 μm

Further improvements can be made to the device by better heat sinking, be this by additional electroplating on the p-side of the device or a water cooled heatsink or a CVD diamond tile. Any or all of these will allow the point at which thermal rollover occurs to be delayed resulting in a greater output power. Adding to this an improved carrier distribution profile, improved internal efficiency, reduced threshold current, reduced optical loss and reduced resistance, will result in significant improvements in device performance

Appendix A

TS522 (6 QWs)

	Repeat	Thickness (A)	Doping
GaAs	1	2000	1.00E+19
Al0.5Ga0.5As		100	2.00E+18
GaAs		600	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
Al0.8Ga0.2As	32	737	2.00E+18
GaAs	1	1080	
Ga0.9AsP0.1	1	150	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	150	
GaAs	1	680	
Ga0.9AsP0.1	1	150	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	150	
GaAs	1	1080	
Al0.8Ga0.2As	12	737	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
GaAs		600	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
GaAs		2000	1.00E+19
n-sub			n+, n

TS797 (6 QWs)

	Repeat	Thickness (A)	Doping
GaAs	1	2000	1.00E+19
Al0.5Ga0.5As		100	2.00E+18
GaAs		600	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
Al0.8Ga0.2As	32	737	2.00E+18
GaAs	1	1080	
Ga0.9AsP0.1	1	150	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	150	
GaAs	1	680	
Ga0.9AsP0.1	1	150	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	150	
GaAs	1	1080	
Al0.8Ga0.2As	12	737	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
GaAs		600	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
GaAs		2000	1.00E+19
n-sub			n+, n

TS830 (9 QWs)

	Repeat	Thickness (A)	Doping
GaAs	1	2000	1.00E+19
Al0.5Ga0.5As		100	2.00E+18
GaAs		600	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
Al0.8Ga0.2As	32	737	2.00E+18
GaAs	1	1020	
Ga0.9AsP0.1	1	150	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	150	
GaAs	1	680	
Ga0.9AsP0.1	1	150	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	150	
GaAs	1	680	
Ga0.9AsP0.1	1	150	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 970nm
Ga0.9AsP0.1	1	150	
GaAs	1	1020	
Al0.8Ga0.2As	12	737	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
GaAs		600	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
GaAs		2000	1.00E+19
n-sub			n

TS838 (3 QWs)

	Repeat	Thickness (A)	Doping
GaAs	1	2000	1.00E+19
Al0.5Ga0.5As	32	100	2.00E+18
GaAs		600	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
Al0.8Ga0.2As		737	2.00E+18
GaAs	1	1040	
Ga0.9AsP0.1	1	150	
QW	1	80	At 950nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 950nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 950nm
Ga0.9AsP0.1	1	150	
GaAs	1	1040	
Al0.8Ga0.2As	12	737	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
GaAs		600	2.00E+18
Al0.5Ga0.5As		100	2.00E+18
GaAs		2000	1.00E+19
n-sub			n

Improved device (Conclusion)

	Repeat	Thickness (A)	Doping
GaAs	1	1000	1.00E+19
Al0.2GaAs		33	6E18-1E19
Al0.5GaAs		33	6E18-1E19
Al0.7GaAs		33	6E18-1E19
GaAs		600	6E18-1E19
Al0.2GaAs		33	6E18-1E19
Al0.5GaAs		33	6E18-1E19
Al0.7GaAs		33	6E18-1E19
Al0.9Ga0.1As	22	737	6E18-1E19
Al0.2GaAs		33	4.00E+18
Al0.5GaAs		33	4.00E+18
Al0.7GaAs		33	4.00E+18
GaAs		600	4.00E+18
Al0.2GaAs		33	4.00E+18
Al0.5GaAs		33	4.00E+18
Al0.7GaAs		33	4.00E+18
Al0.9Ga0.1As	5	737	4.00E+18
Al0.2GaAs		33	4.00E+18
Al0.5GaAs		33	4.00E+18
Al0.7GaAs		33	4.00E+18
GaAs		600	2.00E+18
Al0.2GaAs		33	4.00E+18
Al0.5GaAs		33	4.00E+18
Al0.7GaAs		33	4.00E+18
Al0.9Ga0.1As	5	737	2.00E+18
GaAs	1	1040	
Ga0.9AsP0.1	1	150	
QW	1	80	At 950nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 950nm
Ga0.9AsP0.1	1	90	
QW	1	80	At 950nm
Ga0.9AsP0.1	1	150	
GaAs	1	1040	
Al0.9Ga0.2As		737	2.00E+18
Al0.3Ga0.7As		100	2.00E+18
GaAs		600	2.00E+18
Al0.3Ga0.7As	9	100	2.00E+18
GaAs		2000	1.00E+19
n-sub			n

Appendix B

Prepared by: Jon Orchard Date: 21/11/2011

Title: VCSEL/VECSEL - Batch.......:

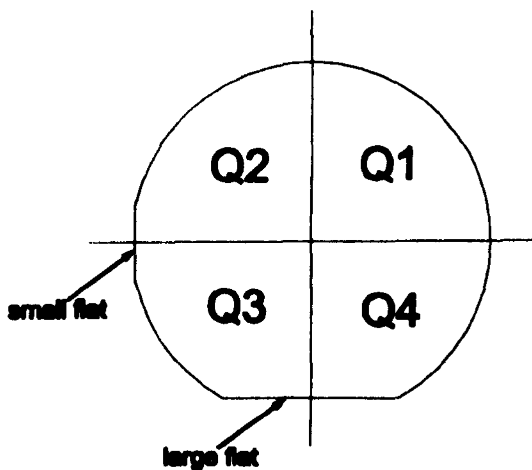
For:

Start date:

Finish date:

Checked:

Mark on area where sample was cleaved from



Process No	Equipment/ Chemicals		Process/ Parameter information	Achieved/ Comments	Sign/Date
1	Scriber 1) n-Butyl 2) Acetone 3) IPA		**CLEAVE and CLEAN** < one particle per field of view on 100 x magnification		
2	PECVD	3 Stage clean and 19:1 Ammonia wash before placeing sample in machine	**OXIDE DEPOSITION** OXIDE program => 400nm		
3	MJB3 mask aligner Resist = SPR350	Remove edge beade prior to exposure	**TRENCH PHOTOLITHOGRAPHY** Mask plate: VECSEL - TRENCH Follow lithography with 1 minute O_2 plasma Ash. Then 1min hard bake 100ºC hotplate		Ken Kris
4	ICP ETCHER	Position end-point on area of sample with no resist	**HARD MASK ETCH** Recipe : 20/20 CHF3/Ar Etch time ~ 25 min		Ken Kris
6	Resist Stripper O2 Asher 1) n-Butyl 2) Acetone 3) IPA		• 5min in O2 asher • Place sample in resist stripper on low temp hotplate for 2min, follow with rinse in IPA. • 3 Stage clean		Ken Kris
5	ICP ETCHER	Position end-point on area of sample with no resist	**SEMICONDUCTOR TRENCH ETCH** Recipe : GaAs etch (SiCl4) T1a Desired etch depth : 5.8um Achieved Etch depth : __________um		Ken Kris
7	ICP ETCHER	Position end-point on area of sample with no resist	**HARD MASK ETCH** Recipe : 20/20 CHF3/Ar Etch time ~ 25 min		Ken Kris

8	PECVD	3 Stage clean and 19:1 Ammonia wash before placeing sample in machine	**OXIDE DEPOSITION** OXIDE program 10 min ~ 400nm		
8	MJB3 mask aligner Resist = SPR350	Use HMDS adhesion promoter	**WINDOW PHOTOLITHOGRAPHY** Mask plate: VECSEL-SHEF1 WINDOW Follow lithography with 1 minute O_2 plasma Ash.		Ken Kris
9	ICP ETCHER	Position end-point on area of sample with no resist	**WINDOW ETCH** Recipe : 20/20 CHF3/Ar Etch time ~ 25 min		Ken Kris
10	Resist Stripper O2 Asher 1) n-Butyl 2) Acetone 3) IPA		• 5min in O2 asher • Place sample in resist stripper on low temp hotplate for 2min, follow with rinse in IPA • 3 Stage clean		
11	MJB3 mask aligner Resist = BPRS200	Use HMDS adhesion promoter	**METAL PHOTOLITHOGRAPHY** Mask plate: VECSEL-SHEF1 TOPCONTACT Follow lithography with 1 minute O_2 plasma Ash.		Ken Kris
12	EVAPORATOR	19:1 Ammonia wash before placeing sample in machine	**TOP CONTACT 1** Au/Zn/Au 5/10/200nm **Au (5nm)** **Zn (10nm)** **Au (200nm)**		Ken Kris
13	1) n-Butyl 2) Acetone 3) IPA		**LIFT OFF IN ACETONE** Followed by 3 stage clean		
14	RTA Prog: Furn360-1		**ANNEAL** Furn360-1 program		

Step	Equipment	Notes	Process		Sign
15	EVAPORATOR		**TOP CONTACT 2** Ti/Au 20/400nm		
			Ti (20nm)		Ken
			Au (400nm)		Kris
16	Logitech lapper/polisher	Mount on glass thinning block, using wax along with small pieces of spacer wafer.	**BACKSIDE THINNING** Be aware of uniformity, and allow for wax in thickness measurement. Followed by good clean (using carriers).		
			Min: 110um Aim: 100um Max: 85um		
			A, B, C, D		Ken Kris
16b	Logitech lapper/polisher		**BACKSIDE POLISHING** 1 hr @ 60rpm using polish solution and polish plate		
17	Wet etch		**WET ETCH** 10ml of each chemical for 1:1:1 etch + 30ml water place samples still mounted on thinning block in solution for 2.5 mins. Then un-mount samples from glass blocks		
18	MJB3 mask aligner Resist = BPRS100	Mount p-side down on glass cover slip, use HMDS adhesion promoter	**BACK CONTACT PHOTOLITHOGRAPHY** Mask plate: VECSEL-SHEF2 BACKCONTACT		Ken Kris
19	EVAPORATOR	19:1 Ammonia wash before placeing sample in machine	**BOTTOM CONTACT** InGe/Au 20/200nm		
			InGe (20nm)		Ken
			Au (400nm)		Kris
20	1) n-Butyl 2) Acetone 3) IPA		**LIFT OFF IN ACETONE** Followed by 3 stage clean		

21	RTA Prog: Furn360-1		**ANNEAL** Furn360-1 program			
22	PECVD	3 Stage clean and 19:1 Ammonia wash before placeing sample in machine	**NITRIDE DEPOSITION** NITRIDE program 127nm desired thickness			
			SiNx (127nm)			Ken
			Ref index (1.93)			Kris
23	MJB3 mask aligner Resist = SPR350	Mount p-side down on glass cover slip, use HMDS adhesion promoter	**AR COATING PHOTOLITHOGRAPHY** Mask plate: VECSEL-SHEF ARETCH Follow lithography with 1 minute O_2 plasma Ash.			
						Ken
						Kris
24	RIE ETCHER	Position end-point on area of sample with no resist	**WINDOW ETCH** Recipe : 35/5 CHF3/O2 80W RF 35mT Etch time ~ 25 min			
						Ken
						Kris