Development of AlGaN/GaN HBTs and HFETs for High Power and High Frequency Operation

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Dedicated to Lucy, Basil, Maxwell and Jasper

Abstract

GaN-based semiconductors show promise for the fabrication of devices capable of operating under high power, high frequency conditions and at elevated temperatures. This has lead to the development of both AlGaN/GaN heterostructure field effect and bipolar junction transistors. In order to increase the efficiency of these devices novel fabrication technologies are examined. Contact resistances to buried p-type layers, exposed using a novel wet etch, were found to be superior when compared to those formed on dry etched structures. Utilising this technology in conjunction with a novel inverted n-p-n AlGaN/GaN HBT is found to increase the emitter-base heterojunction quality and also reduces growth complexity. Replacing the n-type collector region with a Schottky diode was found to significantly reduce leakage in the component and enable normal operation under common emitter bias conditions.

Bulk and surface trapping effects in AlGaN/GaN heterostructures are independently identified. Bulk traps are found to be located close to or at the metal-semiconductor interface which results in a modification to the HFET band structure. Gate leakage current along the AlGaN surface is found to be controlled by injection from the gate and a surface hopping conduction mechanism which dominates at high and low temperature respectively. Passivation of the structure using SiN reduces current flow at the AlGaN surface. Employing a plasma pre-treatment, contamination at the surface of the device can be removed allowing intimate contact between the passivation and AlGaN films. Using a CF_4 plasma treatment is found to remove these contaminants and deposits a thin film of AlF_3 on the AlGaN surface which reduces current collapse in AlGaN/GaN HFETs to negligible levels. GaN capping layers on HFETs can reduce parasitic contact resistances and also reduce current collapse. Methods of selectively etching through the GaN capping layer are presented in order to develop a suitable self-aligned gate recess process.

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List of Publications

Journal Publications

[1] "Surface Leakage Currents in SiNx Passivated AlGaN/GaN HFETs" W.S. Tan, M.J. Uren, P.A. Houston, **R.T. Green**, R.S. Balmer and T. Martin, IEEE Electron Device Letters, Vol. 27, Number 1, pp 1-3, January 2006

[2] "Investigations on Electrode-less Wet Etching of GaN Using Continuous UV Illumination" **R.T. Green**, W.S. Tan, P.A. Houston, T. Wang and P.J. Parbrook, Journal of Electronic Materials, Vol. 36, No. 4, pp 397-402, April 2007

Conference Publications

[1] "Variation in SiNx passivation of AlGaN/GaN HFETs" W.S. Tan, M.W. Low, **R.T. Green**, P.J. Parbrook, P.A. Houston, M.J. Uren, R.S. Balmer, T. Martin, J.L. Glasper, and K.P. Hilton, UKNC '05, University of Manchester, January 2005

[2] "GaN Diodes Fabricated Using A Low Damage Wet Etch Technology" **R.T. Green**, W.S. Tan and P.A. Houston, UKNC '05, University of Manchester, January 2005

[3] "Surface Leakage Effects in AlGaN/GaN-Based Devices" W.S. Tan, **R.T. Green**, P.A. Houston, M.J. Uren, R.S. Balmer and T. Martin, WOCSDICE '05, University of Cardiff, February 2005

[4] "Surface Pre-Treatment Prior to Passivation for AlGaN/GaN HEMTs" **R.T. Green**, W.S. Tan, P.A. Houston, M.J. Uren, R.S. Balmer and T. Martin, UKNC '06, University of Strathclyde, January 2006

[5] "Wet etching for the fabrication of novel HBT structures" **R.T. Green**, W.S. Tan, P.A. Houston, T. Wang and P.J. Parbrook, UKNC '07, University of Cambridge, January 2007

[6] "Leakage Mechanisms in AlGaN/GaN based HFETs" **R.T. Green**, P.A. Houston, I.J. Luxmoore, M.J. Uren, D.J. Wallis, T. Martin, Compound Semiconductors '07, University of Sheffield, July 2007

[7] "Schottky Collector AlGaN/GaN HBTs" **R.T. Green**, I.J. Luxmoore, P.A. Houston, F. Ranali, T. Wang and P.J. Parbrook, UKNC '08, University of Strathclyde, January 2008

[8] "Gate Recessing of GaN/AlGaN/GaN Heterostructures" I.J. Luxmoore, **R.T. Green**, P.A. Houston, F. Ranali, T. Wang and P.J. Parbrook, UKNC '08, University of Strathclyde, January 2008

Contents

1 Introduction

1.1 The GaN-Based Material System

The Si-based semiconductor industry has demonstrated unprecedented growth since its emergence in the mid 20th century. This has been fuelled by the abundance of Si, its material properties and stable oxide layers making it suitable for the fabrication of complimentary metal oxide semiconductor field effect transistors (MOSFETs). However, in the near future the limits for Si based solutions will begin to be realised. With an increasing demand for more advanced solid-state solutions capable of operating at higher frequencies, higher powers and in harsh environments, the development of alternative material systems with superior physical and electrical properties is becoming increasingly important.

The GaN material system has a large direct band gap of 3.39eV making it suitable for high temperature applications. The thermal conductivity of this material is more than four times that for GaAs [1] enabling power devices to operate at elevated temperatures without the need for bulky cooling systems. This large band gap will also allow devices to have increased resilience to radiation exposure, preventing single event effects (SEEs), and enabling devices to be used in satellite and aerospace applications [2]. Furthermore GaN has excellent transport properties including a high saturation velocity and large velocity overshoot. These parameters, coupled with a high breakdown voltage, make GaN-based semiconductors suitable for high power RF applications such as future radar and communication systems. Various material parameters of GaN and AlN are presented in table 1.1 and are compared to other more established semiconductors such as Si and GaAs [1][3]-[6].

Material	E_G (eV)	θ ($WK^{-1}cm^{-1}$)	μ_e ($cm^2V^{-1}s^{-1}$)	E_{BR} (Vcm^{-1})	V_{SAT} (cms^{-1})	V_{PEAK} (cms^{-1})
Si	1.12	1.5	1400	3×10^5	1×10^7	-
GaAs	1.43	0.54	8500	4×10^5	1×10^7	2.1×10^7
GaN	3.4	2.3	900/2000*	3×10^6	2.6×10^7	3.1×10^7
SiC	3.25	4.9	800	3×10^6	2×10^7	-
Diamond	5.5	20-30	4500	$5\text{-}10\times10^6$	2.6×10^7	-

Table 1.1 – Material parameters for Si, GaAs, GaN, SiC and Diamond at room temperature (indicates mobility for electrons in a 2-dimensional electron gas)*

From table 1.1 diamond appears to be the optimum choice for the development of high power semiconductors. However, there are several major technological difficulties which need to be overcome before reliable devices can be realised using this material. These include the need to find an n-type dopant which is suitably shallow [7], reduced ohmic contact resistances, optimisation of growth techniques and device geometries [8].

SiC represents a more mature technology for the fabrication of devices capable of high temperature operation. However, GaN-based materials are more flexible due to the use of heterostructures. In the case of a HFET this leads to greatly enhanced mobility and in the case of HBTs improved emitter injection efficiency and reduced base spreading resistances. Therefore the GaN-based material system shows great promise for the development of solid-state devices capable of operating under high power, high frequency and high temperature conditions.

Initially work on the III-N material system was focused on optical devices developing blue light emitting diodes (LEDs) and laser diodes (LDs) [9][10]. Blue LDs have applications in optical storage where the shorter wavelength enables increased digital memory space. Examples of blue LDs already in use today include the new generation blue-ray digital versatile disk (DVD) players. GaN-based LED devices are currently being investigated for future multicolour displays. However an interesting application

of these LEDs is in future lighting systems. White LEDs have been demonstrated by using a ultra-violet (UV) or blue GaN-based LED in conjunction with an appropriate phosphorous [11][12] for use in domestic and industrial lighting. Incandescent lighting used throughout the world is the largest producer of CO_2 emissions, greatly outweighing that of aviation. The efficiency of the average household bulb is only ≈5% and globally this results in the generation of a massive 1900 MTonnes of CO_2 per year. It has recently been stated in a report by the international energy agency (IEA) that if half of America was to switch to using GaN-based LEDs it would save the equivalent energy of shutting down 41 power stations [13]. Although encouraging progress has been made in the growth and fabrication of GaN-based white LEDs there are still several major problems including, optimisation of efficiency, device lifetime and operating the devices under high power conditions [12].

Despite significant progress in opto-electronic structures, the development of electronic devices is more recent with most of the work concentrated on the development of heterostructure field effect transistors (HFETs) for high power RF applications.

1.2 Growth of GaN and its Alloys

1.2.1 Substrates

Due to extremely high melting temperatures and dissociation pressures, native GaN substrates cannot be produced using standard techniques such as the Czochralski method. Recent work by several groups has demonstrated hydride vapour phase epitaxy (HVPE) can be used to produce free standing GaN crystals due to an extremely high growth rate (10-700μm/h) [14][15]. However, these substrates are only available in small diameters and are extremely expensive, costing approximately $3000 for a 2 inch diameter wafer.

The difficulty of obtaining free standing GaN at low cost and with sufficiently large area has led to the development of epitaxial growth techniques using foreign substrates. SiC and sapphire (Al_2O_3) are the most common substrates of choice for the

growth of GaN. SiC represents the best alternative due to a high thermal conductivity when compared with sapphire ($4.9 WK^{-1}cm^{-1}$ and $0.5\ WK^{-1}cm^{-1}$ respectively) and also a reduced lattice mismatch (≈3% and ≈13% respectively). Unfortunately insulating SiC is only available in small diameter wafers and is very expensive which has lead many research groups to use sapphire since it is significantly cheaper.

Using a foreign substrate to grow material which has a large lattice mismatch can result in a significant number of dislocations. Growth of GaN on SiC can produce approximately 1×10^{5}-$1\times10^{7}cm^{-2}$ threading edge dislocations. Using sapphire, which has an increased lattice mismatch, results in approximately 1×10^{9}-$1\times10^{10}cm^{-2}$ dislocations. With such high dislocation densities it is difficult to imagine that working devices can be fabricated from this material system. This has lead people to believe the dislocations are probably not electrically active.

Si is also emerging as an alternative substrate for the epitaxial growth of GaN and its alloys. Si is cheap and widely available in large diameters making it attractive for use in the development of GaN-based solid-state devices both for research and industrial purposes. Due to the extremely large lattice mismatch, difference in crystal structure and high thermal mismatch, growth on these substrates is technologically demanding. Initial results have shown it possible to grow layers with thicknesses of up to 1μm before cracking of the epitaxial film was observed [16]. To achieve increased thickness, required for the development of electronic devices, appropriate strain management must be employed between the substrate and epilayer. AlN [17] and AlGaN/GaN strained superlattice structures (SLS) [18] have been found effective in increasing the critical thickness of the epitaxially grown GaN. These systems work by partially compensating the tensile strain in the structure which is introduced due to the large lattice mismatch and during cooling of the substrate after growth. Using Si as a substrate can also lead to the problem of wafer bowing due to the large amount of strain in the layers [18]. This can have implications for device lifetime and also create problems in the fabrication process when dealing with large scale manufacture. Furthermore, Si is relatively conducting when compared to GaN (≈10kΩ/□) and therefore an appropriate buffer technology must be employed in order to prevent current leaking through the substrate.

1.2.2 Epitaxial Growth of GaN-Based Semiconductors

Molecular Beam Epitaxy (MBE) can be used to grow epitaxial layers of both elemental and compound semiconductors. Typically growth is performed under an ultra high vacuum (UHV) in order to reduce the incorporation of impurities during deposition. Materials are evaporated by Knudsen effusion ovens which are heated resulting in evaporation of the element or compound. The material then effuses through a small orifice resulting in a molecular beam. The beam is aimed at the semiconductor substrate which is both heated and rotated, resulting in deposition of atomic layers. Using MBE therefore enables precise thicknesses to be deposited and accurate control of dopant species. The surface microstructure of the growing film can also be monitored in-situ using reflection high energy electron diffraction (RHEED).

Due to the inert nature of nitrogen, the growth of III-Nitride materials using the MBE technique requires an energetic nitrogen species which can be produced by RF, electron cyclotron resonance (ECR) or ion sources. Of these approaches the RF method (RF-MBE) is the most attractive since it can operate at high vacuum and provides higher growth rates [19]. However, there are several problems relating to the heterointerface between the substrate and epilayer when using the MBE technique which limit its use when growing on foreign substrates. When growing on sapphire for example the large lattice mismatch results in three dimensional (3D) growth of islands upon the substrate with various orientations. After extended growth this results in material with a rough surface morphology with many dislocations and grain boundaries within the structure [20]. Yoshida et al found when using a low temperature AlN ≈50nm thick buffer layer, crystal quality was noticeably improved [21]. The AlN buffer reduced both lattice mismatch and the difference in thermal expansion coefficients between the two films. However, using this buffer technology still results in relatively poor quality epitaxial layers when compared to material produced using the metal organic chemical vapour deposition (MOCVD) technique.

Further significant improvements in crystal quality when using the MBE method can be achieved when growing on GaN MOCVD produced templates [22]. The growing epilayer reflects the quality of the template resulting in high quality material whilst

taking advantage of the reduced impurity incorporation, in-situ growth monitoring and precise thickness control of the MBE technique. However, this method requires the use of two separate reactors which significantly increases both growth complexity and cost.

With the increasing availability of native GaN substrates with low dislocation densities ($0.5\text{-}1\times10^{6}cm^{-2}$) there has been a recent renewed interest in MBE technology. Using native substrates dramatically reduces the number of dislocations in the material due to reduced strain during growth. The MBE technique in conjunction with a native substrate can therefore lead to high quality material with reduced impurity concentrations and improved growth control. Using this method, high quality AlGaN/GaN heterostructures have been produced with record low temperature 2-dimensional electron gas (2DEG) mobilities higher than $160{,}000cm^{2}V^{-1}s^{-1}$ made possible through reduced dislocation scattering [23]. Furthermore, since MOCVD has many patents due to its popularity, groups in industry look towards MBE as a method of growing structures whilst avoiding copyright infringement. Companies such as Sharp for example are currently producing blue LDs for the next generation blue-ray DVD players using MBE in conjunction with native GaN substrates [24]. However, until the cost of these substrates drops significantly compared to that of sapphire and Si, the MOCVD technique will still remain the most cost effective way of producing high quality epitaxial III-nitride films.

MOCVD has emerged as the dominant method of growth for GaN-based semiconductors due to the superior characteristics of fabricated devices when grown on foreign substrates. MOCVD growth is achieved by passing metal organic precursors over a heated substrate, usually via a hydrogen carrier gas [25]. The precursor decomposes at the substrate resulting in deposition of the volatile component (the semiconductor) whilst the non-volatile component is removed via an exhaust. Growth is usually performed at or reduced atmospheric pressure removing the need for specialist UHV equipment required for MBE growth.

All material discussed in this thesis was produced using the MOCVD technique at either the National Centre for III-V Technologies, Sheffield or at QinetiQ, Malvern

using a Thomas Swan reactor incorporating a close coupled shower head. In the case of GaN deposited upon a sapphire (Al_2O_3) substrate in the c-plane (0001) direction the wafer is first loaded into the reactor via a load lock system. Contamination on the wafer surface which could affect growth and material quality is removed by heating the wafer at ≈1100°C in a flowing H_2 atmosphere. To avoid cracking of the epitaxial film, due to the large lattice mismatch and difference in thermal expansion coefficients between the III-nitride semiconductor and substrate, a nucleation layer must be used similar to that described for the MBE technique. Amano et al [26] was the first to demonstrate AlN nucleation layers for the growth of GaN on sapphire substrates in conjunction with MOCVD. Using the AlN resulted in a vast improvement in material quality. Further improvements in material quality were achieved when employing a thin GaN nucleation layer [27]. Therefore after cleaning, a thin film (≈20nm) of GaN is deposited at low temperature (≈500°C). Initially the deposited material is highly defective and of low quality [20]. The reactor temperature is then raised to ≈1100°C which results in crystallisation of the film leaving small crystallites on the sapphire surface. Upon deposition of subsequent epilayers these crystallites act as growth centres reducing interfacial free energy and promoting lateral two dimensional (2D) growth resulting in high quality, optically smooth epitaxial material. Typically a thick buffer (~1-3μm) is grown on top of the nucleation layer in order to separate the active semiconductor device from the highly defective nucleation region. This buffer reduces the number of dislocations in the material and the background unintentionally doped (UID) n-type conductivity [28].

To transport the metal organic precursors to the substrate hydrogen is passed through a bubbler containing the precursor. The hydrogen carrier gas and precursor is then fed to the shower head via a heated tube to avoid condensation. The group III precursors used were trimethylgallium (TMG) and trimethylaluminium (TMA) and the group V precursor was ammonia (NH_3). N-type and p-type conductivity is controlled by the introduction of silane (SiH_4) and bis-cyclopentadienyl-magnesium (Cp_2Mg) respectively. Upon entering the growth chamber these gasses mix and decompose at the heated substrate. To avoid any build up of pressure within the reactor, gas lines not in use were continuously vented. Prior to venting these gasses were heated to remove the metal organics, passed through catalysts which split them into their

constituent nitrogen and hydrogen components and finally released into the atmosphere.

1.3 AlGaN/GaN Heterostructure Field Effect Transistors (HFETs)

1.3.1 Basic Device Structure and Operation

HFETs consist of two ohmic contacts, the source and drain, and a Schottky contact known as the gate. Figure 1.1 shows an example of an AlGaN/GaN HFET structure. Typically the source is grounded and the drain is forward biased under normal operation. Current is conducted through the channel via a 2DEG which is confined at the lower AlGaN/GaN interface. The electrons are confined to this channel by the energy barriers either side of the quantum well and so can only move laterally. A bias can then be applied to the gate to modulate the current which flows between the two ohmic contacts.

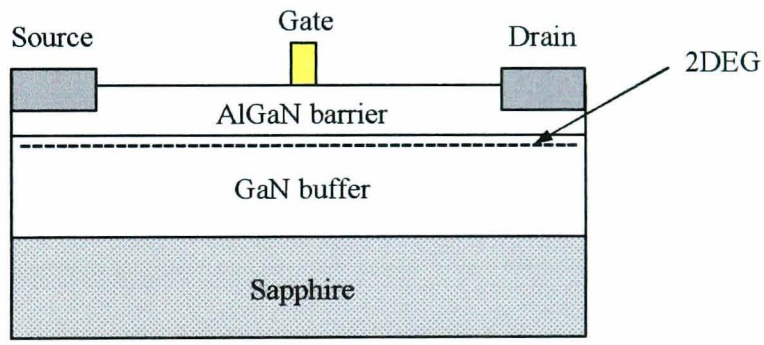


Figure 1.1 – Typical AlGaN/GaN HFET device structure

The ability of the gate to control the output current is governed by the transconductance (g_m) and is defined as the rate of change of channel current with gate voltage (equation 1.1).

$$g_m = \frac{dI_D}{dV_{GS}} \qquad \text{Equation 1.1}$$

Where I_D is the drain output current and V_{GS} is the potential difference applied to the gate with respect to the source.

For real AlGaN/GaN HFETs a potential difference will be induced between the source and gate due to the finite resistance of the channel which will reduce the observed g_m. Analysis of the equivalent circuit for the HFET shows the extrinsic transconductance $g_{m(EXT)}$ is given by equation 1.2, where R_S is the resistance of the channel between the source and gate. Therefore, to maximise $g_{m(EXT)}$ the source-gate separation and parasitic access resistances should be minimised.

$$g_{m(EXT)} = \frac{g_m}{1 + g_m R_S} \qquad \text{Equation 1.2}$$

AlGaN/GaN HFETs will be required to operate at high frequencies (X-band and above) if used in applications such as radar and communication systems. The cut-off frequency (f_t) can be used as an indicator of high frequency performance and is defined as the frequency at which the gain of the FET (i_d/i_g) is equal to unity. It can be shown by considering the equivalent circuit that f_t is given by equation 1.3.

$$f_t = \frac{v}{2\pi L_g} = \frac{g_m}{2\pi C_g} \qquad \text{Equation 1.3}$$

Where v is the velocity of electrons, L_g is the gate length and C_g is the gate capacitance per unit gate width. It can be seen from equation 1.3 that f_t is related to how fast electrons transit across the gate of the HFET which, in a short channel device, is determined by v_{SAT}. Therefore this figure of merit allows important comparisons to be made between the frequency performance of devices fabricated from different material systems. From table 1.1 it can be seen that GaN has a high saturation velocity of $\approx 2.7\times10^7 cms^{-1}$ making it an attractive candidate for the fabrication of high frequency components.

1.3.2 Polarisation Effects in GaN-Based Semiconductors

For AlGaAs/GaAs HFETs the principle of modulation doping is applied. This is where the upper wide band gap material is doped n-type and the lower GaAs layer is semi-insulating (SI). Ionised electrons in the upper layer diffuse and fall into the

lower band gap material and collect near the interface resulting in the formation of a 2DEG. This physical separation of electrons from their donor ions results in greatly reduced columbic scattering yielding a significant increase in mobility [29]. Despite the background impurities in the lower layer the high number of carriers in the 2DEG results in carrier screening which further enhances mobility when compared to bulk films.

The spontaneous and piezoelectric constants in GaN and AlN are ≈10 times higher than that found in other conventional III-V compound semiconductors [30]. Consequently this has a direct influence on band bending at heterointerfaces and for the case of AlGaN/GaN HFETs the 2DEG can form as a result of this polarisation without the need for intentional doping within the barrier layer. A typical HFET band diagram is shown below in figure 1.2.

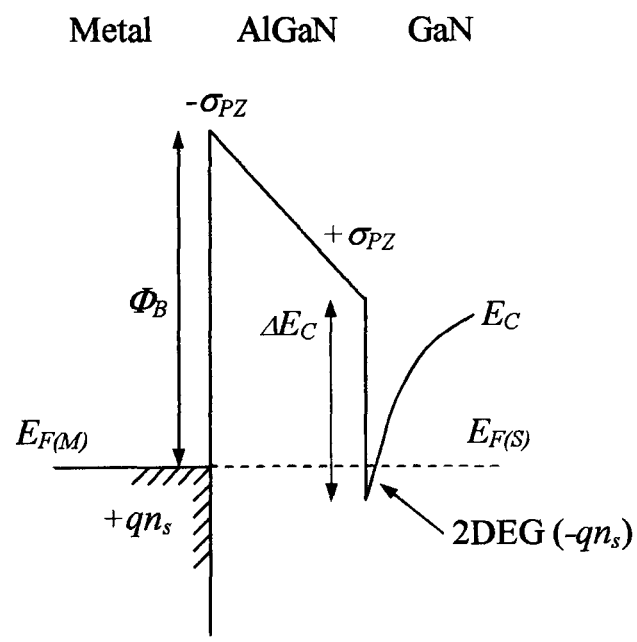


Figure 1.2 –A typical AlGaN/GaN HFET energy band diagram. The polarisation charge is shown as $\pm\sigma_{PZ}$ and the sheet charge from the 2DEG is equal to qn_s.

Spontaneous polarisation (P_{SP}) in GaN-based structures arises from the lack of inversion symmetry in the wurtzite crystal structure [31]. This lack of symmetry gives rise to two possible polarites for (0001) growth, Ga-face or N-face. Ga- and N-face corresponds to the Ga or N atom occupying the top position of the [0001] bi-layer respectively. The direction of polarisation is defined as pointing from the metal

(cation) to the nearest neighbour nitrogen (anion) atom along the c-axis. In the case of MOCVD produced material the termination is of the Ga-face type and therefore the spontaneous polarisation points towards the substrate for both the GaN and AlGaN layers [30]. When growing bulk layers it is believed that re-arrangement of surface charges will nullify these polarisation induced fields. However, for the growth of heterostructures there will be a non-vanishing polarisation field which can dramatically affect the material properties and electrical device behaviour.

If the wurtzite lattice is distorted due to strain, induced by growing a layer on a substrate with a different lattice constant, a piezoelectric polarisation (P_{PZ}) field will result. For the case of AlGaN/GaN HFETs the lower GaN layer is relatively thick and is fully relaxed, therefore the buffer consists of only spontaneous polarisation charges. The upper AlGaN barrier layer is grown pseudomorphically on top of the GaN buffer as shown previously in figure 1.1. Since the lattice constant for AlGaN is smaller than for GaN this will result in the upper barrier layer being under tensile strain. For Ga-face material this acts to reinforce the spontaneous polarisation in the AlGaN layer resulting in a positive polarisation charge at the interface. For such a structure the 2DEG will then be located at the lower AlGaN/GaN interface. As the Al content is increased a more pronounced piezoelectric polarisation charge would be expected since the lattice constant would decrease. The spontaneous and piezoelectric polarisation results in high 2DEG sheet charge concentrations ($>1\times10^{13}cm^{-2}$) which are approximately 5 times more when compared to AlGaAs/GaAs HFETs resulting in greatly reduced on state resistances [32]. If the structure was reversed with a thin strained GaN layer grown on top of a thicker relaxed AlGaN buffer, the piezoelectric polarisation for the GaN would point in the opposite direction to the spontaneous polarisation. Under such conditions a 2DEG will not be formed since the induced polarisation charge will be negative promoting the accumulation of holes.

The piezoelectric and spontaneous polarisation charges result in an electric field produced across the AlGaN layer which is constant irrespective of barrier thickness. The physics behind the formation of the 2DEG as a result of these quasi-electric fields is still not fully understood. Several models have been proposed including piezoelectric doping [33], thermal generation [30] and doping from impurities in the AlGaN [34]. However, the most widely accepted model was proposed by Ibbetson et

al [35]. The author dismissed the concept of piezoelectric doping since the net contribution of polarisation induced charge should be zero. In the absence of an externally applied electric field the structure should remain charge neutral. Therefore, setting the buffer charge (σ_{buffer}) equal to zero and cancelling the polarisation induced dipole gives the following charge balance equation (equation 1.4) [35].

$$\sigma_{surface} + \sigma_{AlGaN} - qn_s = 0 \qquad \text{Equation 1.4}$$

Where $\sigma_{surface}$ corresponds to ionised donor-like surface states, σ_{AlGaN} represents charge in the barrier layer due to ionised donors and qn_s is the sheet charge in the 2DEG. Since the barrier layer is nominally undoped this leads to the conclusion that surface donors are the source of electrons in the 2DEG. Equation 1.4 also shows the spontaneous and piezoelectric polarisation charges are not directly responsible for the 2DEG. The polarisation only determines where in the structure available carriers will collect. The dipole which results from the ionised surface charge and 2DEG partially screens the polarisation induced charges and therefore reduces the overall field across the AlGaN. Assuming the Fermi-level is pinned at the surface by donor-like states at an energy E_P it becomes possible to calculate the theoretical sheet charge concentration for a barrier thickness t using equation 1.5.

$$n_s = \frac{\sigma_{PZ}}{q} - \frac{(E_P - \Delta E_C)\in}{q^2 t} \qquad \text{Equation 1.5}$$

Where σ_{PZ} is the total polarisation induced charge, q is the charge on an electron (1.602×10^{-19}), ΔE_C is the conduction band discontinuity between the GaN and AlGaN and $\in$ is the product of the permittivity of free space and the relative permittivity of the AlGaN barrier.

From equation 1.5 it can be seen that as the aluminium fraction in the barrier layer is increased both σ_{PZ} and ΔE_C will increase resulting in a higher theoretical n_s. Any increase in the thickness of the barrier will result in more electrons transferring across from surface states to the quantum well which will increase the sheet electron concentration. As more electrons transfer the field across the AlGaN film will

decrease and will approach zero for very thick barriers. Under such conditions the sheet charge (qn_s) will be $\approx \sigma_{PZ}$.

1.3.3 HFETs - State of the Art

Since the first demonstration of an AlGaN/GaN HFET in 1993 [36] there has been several novel modifications proposed in the literature to improve device performance. One of the earliest modifications was proposed by Shen [37] whereby a thin AlN layer was placed in between the AlGaN and GaN channel. This increased conduction band discontinuity which resulted in increased 2DEG concentration. Furthermore, due to the binary AlN at the interface, scattering of electrons in the channel was reduced leading to increased mobility. Application of this geometry has lead to high room temperature 2DEG mobilities of greater than $2000cm^2V^{-1}s^{-1}$ and low sheet resistances of $\approx 250\Omega/\square$ [38].

In order to improve the high frequency performance of AlGaN/GaN HFETs it is necessary to reduce the gate of the device to deep-submicron lengths (equation 1.3). However, below ≈200nm short channel effects such as soft pinch-off and increased output conductance degrade both DC and RF device performance [39]. Short channel effects in nitride-based HFETs are a direct result of poor confinement of the 2DEG at these small gate lengths which reduces gate modulation efficiency. Palacios et al [40] proposed an interesting solution which incorporated a thin InGaN back-barrier to the structure (figure 1.3). The induced conduction band discontinuity from the InGaN raises the conduction band in the GaN channel, increasing confinement of the 2DEG and improving high frequency performance.

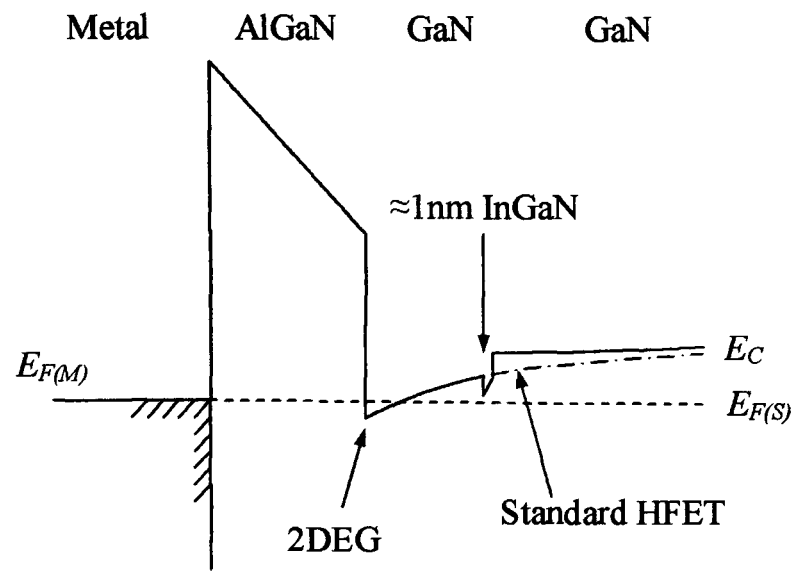


Figure 1.3 – Structure proposed by Palacios et al [39] which incorporates a thin InGaN back-barrier to improve carrier confinement.

Methods used to overcome short channel effects in other compound semiconductor HFETs include using a wide bandgap buffer or doping the buffer p-type. However, these methods cannot be readily applied to AlGaN/GaN devices since they would both introduce trapping states which would degrade high frequency performance. Furthermore a p-type conducting buffer would introduce parasitic capacitive coupling reducing device speed. Consequently, for GaN-based transistors, the conductivity of the buffer must be reduced through the controlled incorporation of deep acceptors which compensate the unintentionally doped film. Iron doping has been found to yield highly insulating material [41] and has been applied to HFETs to produce high quality buffers which improve device performance when using deep-submicron gate lengths.

One of the main limitations for the high frequency performance of AlGaN/GaN HFETs above 20GHz is the high parasitic access resistance which is ≈1 order of magnitude higher than in conventional III-V devices [42]. This resistance is found to increase at high drain currents due to saturation in the velocity of carriers in the channel region [43] degrading g_m and f_T. This adversely affects linearity and leads to reduced power performance. One method to overcome this is to use double channel devices [44]. However, unlike other III-V HFETs the gate is recessed below the first channel. Assuming the barrier between the two channels is sufficiently low, the access resistance will be dramatically reduced for a given drain current. Pei et al [45] used Si

implantation under the source and drain to reduce parasitic resistances associated with the contacts. This method was found to reduce contact resistance significantly, reduce knee voltage and increase output current under both DC and RF conditions.

Zhang et al [46] demonstrated a gate-terminated field plate geometry in order to significantly enhance output power of the device. The field-plate, separated from the semiconductor by a dielectric layer (figure 1.4), works by contributing to the formation of the depletion region in the channel and thus moderates the field at the drain edge of the gate. This spreading of the field enabled, at the time, a record breakdown voltage of 570volts to be obtained. Modulating the field at the drain edge of the gate has also been shown to improve linearity in the device due to a reduction in electron trapping at the surface allowing increased output power at high frequency. Through optimising the field plate geometry record output power densities of >40W/mm have been demonstrated at 4GHz for devices grown on SiC substrates [47]. Some of the drawbacks of using the field-plate geometry are a decrease in gain due to the extension of the depletion region and an increase in gate capacitance which degrades f_t. For the latter case Saito et al [48] proposed a source-terminated field plate which would reduce parasitic capacitances associated with the field plate extension, however this geometry is more complicated to fabricate.

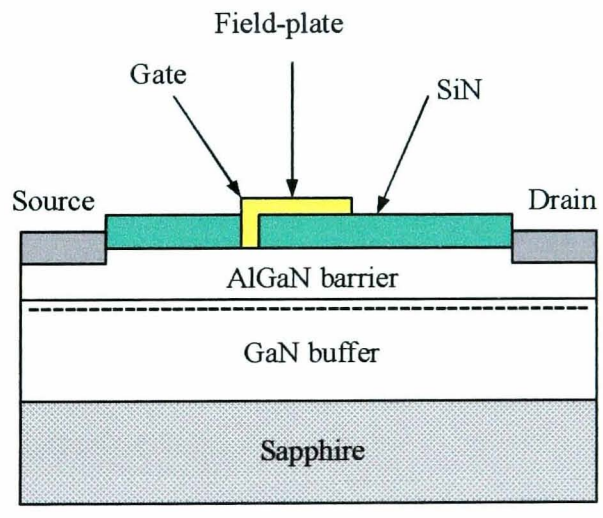


Figure 1.4 – Cross section of gate-terminated field plate.

Despite the addition of field plates, studies have shown that the breakdown voltage for AlGaN/GaN HFETs saturates at ≈400-600 volts at a gate-drain separation of ≈10μm.

Recently Tipirneni et al [49] demonstrated that breakdown occurs due to a flash over effect when testing devices in air. When operating HFETs in a Fluorinert ambient the breakdown voltage was found to scale linearly with gate-drain separation reaching 1.6kV at a separation of 20μm. Using a field plate in conjunction with testing the device in a Fluorinert atmosphere demonstrated a record breakdown voltage of 1.9kV [50].

1.4 Heterostructure Bipolar Transistors (HBTs)

The majority of research on GaN-based electronic devices has focused on HFETs and impressive high power RF performance has been demonstrated. However, AlGaN/GaN HBTs offer several important advantages over HFETs which are summarised in the following points.

- For the HFET structure the thickness of the upper AlGaN barrier layer is critical in controlling the pinch off voltage but in the case of the HBT material parameters determine the emitter-base diode characteristic. Therefore, the threshold voltage is less prone to fluctuations in growth and consequently is more uniform.
- Since current transport is vertical and over a larger area for the HBT as apposed to horizontal transport in a 2DEG, higher output current densities are possible. This use of vertical transport gives better utilisation of wafer area when compared to HFET technology.
- It is expected that HBTs will have higher linearity when compared to HFETs. This will make them extremely useful in applications which require ultra-wide bandwidth such as in military communications and radar systems.
- HBTs are "normally off" devices and so do not require a constant voltage supply to hold them in a pinched-off state.

Despite these advantages there still remain several major technological difficulties which severely hamper the development of this high power microwave component. These issues have lead to a relatively slow development of HBTs when compared to the AlGaN/GaN HFET with only several groups around the world demonstrating

common emitter characteristics. The majority of these problems are related to the thin and electrically sensitive base layer and will be discussed in the preceding sections.

1.4.1 Principle of Operation

For a bipolar junction transistor (BJT) under normal common emitter operation the emitter-base junction is forward biased while the base-collector junction is held under reverse bias. Under such conditions minority carriers are injected into the base from the emitter where they diffuse towards the collector and are swept into this region by the high electric field. This operation is shown schematically in the energy band diagram in figure 1.5a. For the majority of applications an n-p-n structure is adopted since the minority carrier transport of electrons is superior to that of holes and consequently yields superior microwave performance. Therefore, unless otherwise stated, the n-p-n structure will be discussed.

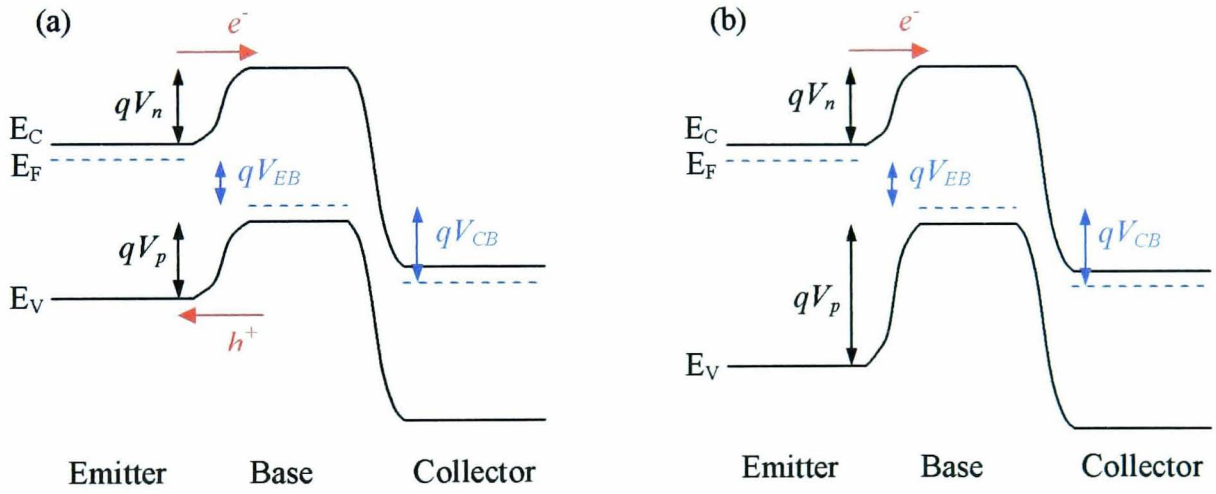


Figure 1.5(a) – Energy band diagram for an n-p-n BJT and (b) HBT under common emitter operating conditions. For the HBT the emitter-base heterojunction is graded to remove the conduction band discontinuity.

In the case of the BJT performance of the emitter-base junction is limited by the parasitic injection of minority holes from the base. In order to maintain a sufficiently high emitter injection efficiency (γ) it therefore becomes necessary to dope the emitter n^+ and the base p^-. This maximises injection from the emitter whist minimising reverse injection from the base. However, the low doping of the base results in an increase in both base access and base spreading resistances degrading device

performance at high frequency and making it unsuitable as a microwave component. Furthermore, a high base resistance will result in emitter crowding potentially leading to secondary breakdown effects and a reduced Early voltage.

The heterostructure bipolar transistor (HBT) was first proposed by Shockley [51] in 1952 and incorporates a wide band gap emitter within the structure. The wide band gap emitter is used in order to selectively prevent parasitic injection of minority carriers from the base (figure 1.5b). Since carrier injection is exponentially dependent on barrier height it becomes possible to greatly increase doping in the base while still maintaining a high emitter injection efficiency and consequently a high gain (β). By doping the base heavily the base spreading resistance will be greatly reduced improving microwave performance and also reducing base width modulation (Early effect and Kirk effect), punch through and secondary breakdown caused by emitter crowding. Furthermore, doping in the emitter can be reduced lowering the base-emitter capacitance and further increasing high frequency performance.

1.4.2 P-type GaN

The majority of problems with n-p-n AlGaN/GaN HBTs are related to the thin and electrically sensitive base layer. Mg is the only known practical p-type dopant for III-nitride semiconductors and forms a deep acceptor in GaN approximately 170meV above the valence band [52]. This deep level means that at room temperature only $\approx$1% of acceptors will be ionised. Therefore the base of an n-p-n HBT will be expected to have a resistivity of approximately 1Ωcm which will result in severe current crowding at the emitter edge.

Growing p-type GaN-based semiconductor material with high hole concentrations at room temperature has proven extremely difficult. It was not until 1989 that the first highly conductive p-type GaN films were demonstrated using MOCVD in conjunction with an appropriate buffer technology [53]. However, after growth no activation of acceptors was observed. A low energy electron beam irradiation (LEEBI) step was found necessary in order to activate acceptors and obtain p-type conductivity. This method of activation was later found to be limited due to the

penetration depth of incident electrons resulting in only thin regions close to the surface being converted to p-type [54]. Soon after this discovery, Nakamura et al [55] showed thermal annealing above 600°C in a nitrogen atmosphere successfully activated acceptors throughout the entire film. The mechanism for acceptor activation in p-GaN during annealing is still not fully understood. The most widely accepted explanation is that hydrogen, which is present during MOCVD growth, passivates the Mg acceptors. Upon annealing the hydrogen escapes from the H-Mg complex, moves through the semiconductor crystal lattice and disassociates from the semiconductor surface [56]. This escape of hydrogen after thermal treatment has been confirmed through the use of secondary ion mass spectrometry (SIMS) [57]. P-type GaN grown using the MBE technique, which does not require a hydrogen carrier gas, demonstrates p-type conduction directly after growth without the need for annealing [58].

Mg has a strong memory effect during growth when using the MOCVD technique. This is attributed to Mg precursor molecules remaining inside the growth chamber and reactor lines after the source has been turned off. Growth of subsequent layers therefore results in residual molecules becoming incorporated into the film. This can alter the electrical properties of the preceding region and cause significant errors in junction placement which has serious implications for bipolar devices. Xing et al [59] further demonstrated surface segregation in MOCVD grown p-GaN resulting in a Mg-rich coating on the growing surface which can incorporate into subsequently grown layers. The problem of Mg memory effect is compounded in AlGaN/GaN HBTs where the wide band gap emitter is grown after the base since the growth rate of AlGaN is lower than GaN. Consequently there is an increase in Mg concentration close to the base-emitter interface in the AlGaN [60]. To reduce memory effect a re-growth step can be introduced. By removing the wafer after growth of the p-type GaN, purging Mg from the reactor and removing the Mg-rich film on the wafer surface by an appropriate acid treatment the decay profiles for the Mg can be improved from ≈100nm/decade to ≈30nm/decade [59]. This improvement in dopant profiles and the accurate placement of the junction has paved the way to BJTs and HBTs with superior device performance.

Etching GaN-based semiconductors using conventional dry techniques can result in damage to the semiconductor due to ion bombardment. This is especially true in the case of p-type GaN since the damage is related to nitrogen vacancies on the surface which act as shallow donors [61], compensating p-type acceptors and reducing the near surface conductivity [62]. This introduces problems when forming ohmic contacts to the etched p-GaN and, in the case of AlGaN/GaN HBTs where etching is used to access the base, forms a surface leakage path between emitter and collector. Furthermore, there is no selectivity between p- and n-type films making it difficult to etch to thin layers such as the base of an AlGaN/GaN HBT.

1.4.3 AlGaN/GaN HBTs – Development and State of the Art

The first AlGaN/GaN HBT structure was demonstrated in 1999 by McCarthy et al [63]. This device was grown on a sapphire substrate using an emitter-up geometry by MOCVD and incorporated a 200nm thick p-type base and an $Al_{0.1}Ga_{0.9}N$ emitter. Dry etching was used to access both the base and sub-collector regions. Common emitter characteristics were achieved by introducing a base re-growth step prior to deposition of the ohmic contacts. This buried the damage caused by the plasma step and resulted in improved contacts to the base. However, contacts were still non-linear and were characteristic of a leaky back-to-back Schottky. The device suffered from several problems which limited its operation. Firstly the gain of the transistor was very low, only 3 at room temperature when measured at a relatively high base-emitter bias of 30 volts. This low gain is primarily due to the relatively thick p-type base, the high resistance of the base layer and the Mg memory effect which can, in the absence of an optimised re-growth step, displace the critical emitter-base heterojunction. Huang et al [64] used a graded interface between the base and emitter heterojunction which removes the spike in the conduction band discontinuity and improves emitter injection efficiency. These devices produced gains of 4-10 at room temperature. Various growth methods have demonstrated varying degrees of reducing the severe Mg memory effect. Some groups have demonstrated MBE growth with very sharp (≈3nm/decade) Mg profiles [59] whilst others have shown conflicting results with inferior Mg doping profiles when compared to MOCVD [65]. These contradictory results potentially reflect the variability in reactor geometries and growth conditions.

Limb et al [66] was the first to fabricate an AlGaN/GaN HBT using a selective emitter re-growth step whereby the growth of the structure was paused after deposition of the base layer as discussed previously. The wafer was removed from the growth chamber and patterned using an inert mask. Following this the sample was placed back into the growth chamber and the final emitter layer was deposited. This had the added advantage that the inert mask could be removed after growth which negated the problems of using a plasma step to etch to the base layer. Since the plasma step was removed the base thickness could be scaled to smaller dimensions resulting in an increase in gain whilst minimising damage to the layer. BJTs fabricated using this method have demonstrated gains of 1.5-3 at room temperature and a greatly improved breakdown voltage of >80 volts [67]. Optimisation of the re-growth step and introducing a heterojunction at the base-emitter diode has resulted in this processing method giving record gains of up to 18 when measured at room temperature and breakdown voltages >330 volts [68]. However, these devices used a large area emitter ($20\times50\mu m^2$) which is not optimised for RF operation. Other groups have reported problems with the re-growth technique when growing small emitter area HBTs for potential high frequency applications [69]. When depositing small emitters ($<10\mu m^2$) the surface morphology was found to become extremely rough and had poor edge acuity. Therefore the selective re-growth method may be limited for the fabrication of large area AlGaN/GaN HBT devices indicating that a selective etch between the emitter and base would be advantageous.

A further problem facing the fabrication of AlGaN/GaN HBTs is due to high leakage currents which flow between the emitter and collector. This leakage has been found to be related to the high number of threading dislocations with run through the material [70]. These dislocations in p-type material act as donors or hole traps and therefore are positively charged. This positive charge runs directly through the base and forms a localised punch through effect between the emitter and collector. Emitter-collector leakage can be reduced by growing low dislocation density material by either a lateral overgrowth (LOG) technique or by growing on native, low defect density substrates.

One of the main limiting factors of AlGaN/GaN HBTs for applications in microwave systems is the highly resistive p-type base. This results in both emitter crowding and also a lateral voltage drop across the width of the base. By heating the transistor more

acceptors in the p-type base can be ionised decreasing the contact and spreading resistances. This leads to an increase in voltage in the active part of the transistor and a corresponding increase in gain. Operating AlGaN/GaN HBTs at elevated temperatures has resulted in moderate increases in gain by a factor of 2-4 [71][72]. Further work has shown that decreasing the operating temperature of the transistor can also directly affect the emitter injection efficiency. Huang et al [73] demonstrated an AlGaN/GaN HBT with a common emitter gain of 31 measured at 175K. This high gain was obtained since the cross-sectional area of defects becomes smaller at reduced temperatures increasing the minority carrier diffusion length. This key result clearly demonstrates the need for improved growth technology so defects associated with the base and at the critical emitter-base heterointerface can be reduced allowing improved emitter injection efficiencies.

Under common emitter operation an offset voltage is typically observed in n-p-n AlGaN/GaN HBT devices. The offset voltage is defined as the collector-emitter bias (V_{CE}) at which the net collector current becomes zero and is normally found to be ≈5volts [66][67][69][70]. For an emitter-up AlGaN/GaN n-p-n HBT there will be a non-linear voltage drop across the base region for a given input current due to the high base spreading resistance. Therefore the voltage directly under the base is greater than under the collector in the intrinsic part of the component. This forms a parasitic base-collector diode (figure 1.6) which will be forward biased until the value of V_{CE} exceeds the potential underneath the base (V_{BE}). This offset increases the knee voltage and results in reduced efficiency in the device. To minimise this effect the conductivity of the base must be maximised and the base contacts should be placed as close to the emitter as possible.

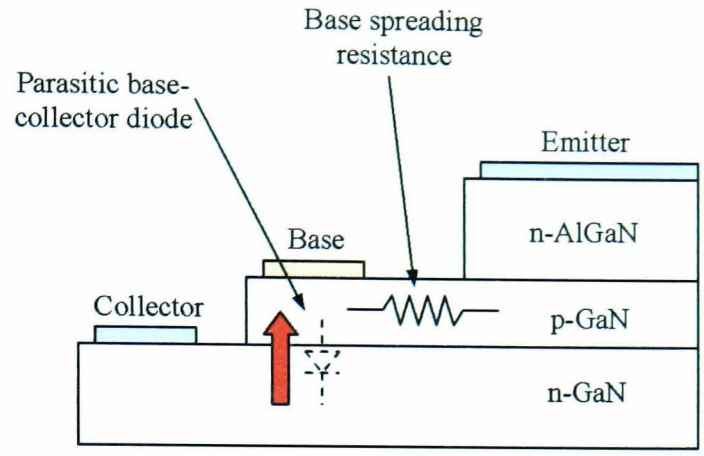


Figure 1.6 – Cross section of an emitter-up AlGaN/GaN HBT showing the formation of a parasitic base-collector diode due to the high base spreading resistance

Due to fabrication issues and the problems associated with the highly resistive base contact and spreading resistances there are limited examples of high frequency measurements made on AlGaN/GaN HBTs. McCarthy et al [74] made the first small signal RF measurements on a 100nm thick base layer which had a short circuit current gain cut off frequency of 2GHz. This value is extremely low when compared to the current state of the art AlGaN/GaN HFETs. These values will be further improved once issues relating to defects and impurities in the base are resolved. Simulation-based studies in the literature suggest that n-p-n HBTs with optimised geometries could have values of f_t and f_{MAX} of up to 44 GHz and 24GHz respectively [75] clearly demonstrating their potential for high-power X- and K-band applications.

1.5 Overview of Thesis

AlGaN/GaN HFETs and HBTs are promising candidates for solid-state microwave power components. The main aim of this research project was to develop fabrication procedures to improve the operation of these devices.

N-p-n HBTs are currently limited by poor ohmic contact to the base and a high base spreading resistance which limits current gain and high frequency performance. The Mg memory effect has been overcome by using a re-growth step. However it is likely interfacial states will be incorporated onto the regrown interface reducing emitter injection efficiency. To overcome some of these difficulties other novel geometries

will be explored to improve device performance. Furthermore, fabrication techniques such as wet etching is investigated in order to improve device characteristics.

Current collapse in AlGaN/GaN HFETs reduces the maximum output power of the device when operated at high frequency. To understand the mechanisms associated with current collapse gate leakage is investigated and trapping centres in the structure are identified. Passivating the surface of the structure using SiN has been found effective in reducing this detrimental effect, however consistency between samples remains a problem. Using I-V characteristics in conjunction with a novel test structure the reasons behind these inconsistencies are investigated. Furthermore, other methods of reducing current collapse such as gate recessing are developed.

Chapter 2 of this thesis outlines the fabrication methods used to realise AlGaN/GaN HBTs, HFETs and the surface leakage test structure. This chapter also describes the measurement techniques used to characterise these devices. Chapter 3 investigates alternative etching techniques which can be used to improve device performance, particularly for accessing the base of an n-p-n HBT and for etching bulk material for the fabrication of other devices such as HFETs. Exploiting the selectivity of the wet etch p-n junctions are fabricated and show this method to be extremely useful for accessing buried p-type and highly insulating layers. Finally, damage to the exposed layers is addressed and is compared to conventional dry etching methods. Chapter 4 discusses the design of novel AlGaN/GaN HBT structures which could potentially overcome some of the difficulties currently described in the literature. Using the wet etch methods developed in the previous chapter, devices are fabricated and I-V characteristics are used to explain device operation. Chapter 5 explores bulk and surface leakage currents in AlGaN/GaN HFET structures using a surface leakage test structure. By operating the device at varying temperatures bulk and surface trapping is investigated and is related to current collapse. The use of a plasma pre-treatment is explored using both DC and pulsed measurements in order to increase the effectiveness of SiN passivation. Chapter 6 develops important fabrication techniques for the development of gate recessed GaN/AlGaN/GaN HFETs. Simple models are shown to describe how device characteristics will be affected by the addition of a GaN capping layer and are compared to experimentally obtained data. Finally in

chapter 7 a summary of all the results presented in this work is given followed by conclusions and recommendations on future development.

1.6 References

[1] *C. Mion, J.F. Muth, E.A. Preble, D. Hanser "Thermal conductivity, dislocation density and GaN device design" Superlattices and Microstructures, Vol. 40, pp 338-342, 2006*

[2] *C.S. Dyer, S.N. Clucas, C. Sanderson, A.D. Frydland, R.T. Green "An experimental study of single-event effects induced in commercial SRAMs by neutrons and protons form thermal energies to 500MeV" IEEE transactions on nuclear science, Vol. 51, No. 5, pp 2817-2824, 2004*

[3] *H. MorkoG, S. Strite,a) G. B. Gao, M. E. Lin, B. Sverdlov, M. Burns "Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies" Journal of Applied Physics, Vol. 76, No. 3, pp 1363-1398, 1994*

[4] *W. Liu "Fundamentals of III-V devices" Appendices, Wiley, New York, 1999*

[5] *B.G. Streetman, S. Banerjee "Solid state electronics" Appendices, Prentice Hall, New Jersey, 2000*

[6] *J. Isberg, J. Hammersberg, E. Johansson, T. Wikström, D.J. Twitchen, A.J. Whitehead, S.E. Coe, G.A. Scarsbrook "High carrier mobility in single-crystal plasma-deposited diamond" Science, Vol. 297, pp 1670-1672, 2002*

[7] *R. Kalish "Doping of Diamond" Carbon 37, pp 781-785, 1999*

[8] *A. Aleksov, M. Kubovic, N. Kaeb, U. Spitzberg, A. Bergmaier, G. Dollinger, Th. Bauer, M. Schreck, B. Stritzker, E. Kohn "Diamond field effect transistors – concepts and challenges" Diamond and Related Materials, Vol. 12, pp 391-398, 2003*

[9] *S. Nakamura M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, Y. Sugimoto "InGaN-based multi-quantum well structure laser diodes" Japanese Journal of Applied Physics, Vol. 35, pp L74-L76, 1996*

[10] *I. Akasaki "Key inventions in the history of nitride-based blue LED and LD" Journal of Crystal Growth, Vol. 300, pp 2-10, 2007*

[11] *X. Sun, J. Zhang, X. Zhang, S. Lu, X. Wang "A white light phosphor suitable for near ultraviolet excitation" Journal of Luminescence, Vol. 122-123, pp 955-957, 2007*

[12] *D.A. Steigerwald, J.C. Bhat, D. Collins, R.M. Fletcher, M.O. Holcomb, M.J. Ludowise, P.S. Martin, S.L. Rudaz "Illumination with solid state lighting*

technology" IEEE journal on selected topics in quantum electronics, Vol. 8, No. 2, pp 310-320, 2002

[13] C.J. Humphreys, L.X. Zhao, C. McAleese, M.J. Kappers, A. Phillips, E.J. Thrush "Progress and challenges in solid state lighting" UKNC '07, University of Cambridge, January 2007

[14] A.D. Williams, T.D. Moustakas "Formation of large-area freestanding gallium nitride substrates by natural stress-induced separation of GaN and sapphire" Journal of Crystal Growth, Vol. 300, pp 37-41, 2007

[15] C. Hemmingsson, P.P. Paskov, G. Pozina, M. Heuken, B. Schineller, B. Monemar "Hydride vapour phase epitaxy growth and characterisation of thick GaN using a vertical HVPE reactor" Journal of Crystal Growth, Vol. 300, pp 32-36, 2007

[16] A. Reiher, J. Bläsing, A. Dadgar, A. Diez, A. Krost "Efficient stress relief in GaN heteroepitaxy on Si(111) using low-temperature AlN interlayers" Journal of Crystal Growth, Vol. 248, pp 563-567, 2003

[17] A. Dadgar, J. Bläsing, A. Diez, A. Alam, M. Heuken, A. Krost "Metalorganic chemical vapor phase epitaxy of crack-free GaN on Si(111) exceeding 1μm in thickness" Japeneese. Journal of Applied Physics, Vol. 39 pp L1183-L1185, 2000

[18] A. Ubukata, K. Ikenaga, N. Akutsu, A. Yamaguchi, K. Matsumoto, T. Yamazaki, T. Egawa "GaN growth on 150-mm-diameter (111) Si substrates" Journal of Crystal Growth, Vol. 298, pp 198-201, 2007

[19] J.M. Van Hove, G.J. Cosimini, E. Nelson, A.M. Wowchak, P.P. Chow "GaN growth by a controllable RF-excited nitrogen source" Journal of Crystal Growth, Vol. 150, pp 908-911, 1995

[20] I. Akasaki, H. Amano, Y. Koide, K. Hiramatsu, N. Sawaki "Effects of AlN buffer layer on crystallographic structure and on electrical and optical properties of GaN and $Ga_{1-x}Al_xN$ ($0<x\leq0.4$) films grown on sapphire" Journal of Crystal Growth, Vol. 98, pp 209-219, 1989

[21] S. Yoshida, S. Misawa, S. Gonda "Epitaxial growth of GaN/AlN heterostructures" Journal of Vacuum Science and Technology B, Vol. 2, pp 250-253, 1983

[22] *S. Kubo, S. Kurai, T. Taguchi "Homoepitaxial growth of GaN thin layer by molecular beam epitaxy with an RF nitrogen plasma" Vacuum, Vol. 59, pp 277-283, 2000*

[23] *M.J. Manfra, K.W. Baldwin, A.M. Sergent, K.W. West, R.J. Molnar, J. Caissie "Electron mobility exceeding 160 000cm2/Vs in AlGaN/GaN heterostructures grown by molecular-beam epitaxy" Applied Physics Letters, Vol. 85, No.22, pp 5394-5396, 2004*

[24] *S.E. Hooper, M. Kauer, V. Bousquet, K. Johnson, C. Zellweger, J. Heffernan "InGaN laser diodes and high brightness light emitting diodes grown by molecular beam epitaxy" Journal of Crystal Growth, Vol. 278, pp 361-366, 2005*

[25] *O. Schön, B. Schineller, M. Heuken, R. Beccard "Comparison of hydrogen and nitrogen as carrier gas for MOVPE growth of GaN" Journal of Crystal Growth, Vol. 189/190, pp 335-339, 1998*

[26] *H. Amano, N. Sawaki, I. Akasaki "Metalorganic vapour phase epitaxial growth of a high quality GaN film using an AlN buffer layer" Applied Physics Letters, Vol. 48, No. 3, pp 353-355, 1986*

[27] *S. Nakamura "GaN growth using GaN buffer layer" Japanese Journal of Applied Physics, Vol.30, No. 10A, pp L1705-L1707, 1991*

[28] *H. Xing, P.M. Chavarkar, S. Keller, S.P. DenBaars, U.K. Mishra "Very High Voltage Operation (>330V) with high current gain of AlGaN/GaN HBTs" IEEE Electron Device Letters, Vol. 24, No. 3, pp 141-143, 2003*

[29] *C. Y. Chang, F. Kai "GaAs High Speed Devices Physics, Technology and Circuit Applications" John Wiley & Sons, New York*

[30] *O. Ambacher, J. Smart, J.R. Shealy, N.G. Weimann, K. Chu, M. Murphy, W.J. Schaff, L.F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, J. Hilsenbeck "Two-dimensional electron gases induced by spontaneous and piezoelectric polarisation charges in N- and Ga-face AlGaN/GaN heterostructures" Journal of Applied Physics, Vol. 85, No. 6, pp 3222-3233, 1999*

[31] *F. Bernardini, V. Fiorentini, D. Vanderbilt, "Spontaneous polarisation and piezoelectric constants of III-V nitrides" Physical Review B, Vol. 52, No. 16, pp 10024-10027, 1997*

[32] *W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, T. Ogura "Design optimisation of high breakdown voltage AlGaN-GaN power HEMT on an insulating substrate for $R_{ON}A$-V_B tradeoff characteristics" IEEE Transactions on Electron Devices, Vol. 52, No. 1, pp 106-111, 2005*

[33] *P. M. Asbeck, E. T. Yu, S. S. Lau, G. J. Sullivan, J. Van Hove, and J. Redwing "Piezoelectric charge densities in AlGaN/GaN HFETs" Electronics Letters, Vol. 33, No. 14, pp 1230-1231, 1997*

[34] *L. Hsu and W. Walukiewicz, "Effects of piezoelectric field on defect formation, charge transfer, and electron transport at GaN/$Al_xGa_{1-x}N$ interfaces" Applied Physics Letters, Vol. 73, No. 3, pp 339-341 1998*

[35] *J.P. Ibbetson, P.T. Fini, K.D. Ness, S.P. DenBaars, J.S. Speck, U.K. Mishra "Polarisation effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors" Applied Physics Letters, Vol. 77, No. 2, pp 250-252, 2000*

[36] *M. Asif Khan, A. Bhattarai, J.N. Kuznia, D.T. Olson "High electron mobility transistor based on a GaN-$Al_xGa_{1-x}N$ heterojunction" Applied Physics Letters, Vol. 63, No. 9, pp 1214-1215, 1993*

[37] *L. Shen, S. Heikman, B. Moran, R. Coffie, N.Q. Zhang, D. Buttari, I.P. Smorchkova, S. Keller, S.P. DenBaars, U.K. Mishra "AlGaN/AlN/GaN high power microwave HEMT" IEEE Electron Device Letters, Vol. 22, No. 10, pp 457-459 , 2001*

[38] *X.L. Wang, T.S. Cheng, Z.Y. Ma, G.X. Hu, H.L. Xiao, J.X. Ran, C.M. Wang, W.J. Luo "1-mm gate periphery AlGaN/AlN/GaN HEMTs on SiC with output power of 9.39W at 8GHz" Solid-State Electronics, Vol. 51, pp 428-432, 2007*

[39] *M.J. Uren, K.J. Nash, R.S. Balmer, T. Martin, E. Morvan, N. Caillas, S.L. Delage, D. Ducatteau, B. Grimbert, J.C. De Jaeger "Punch-through in short-channel AlGaN/GaN HFETs" IEEE Transactions on Electron Devices, Vol. 53, No. 2, pp 395-398, 2006*

[40] *T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S.P. DenBaars, U.K. Mishra "AlGaN/GaN high electron mobility transistors with InGaN back-barriers" IEEE Electron Device Letters, Vol. 27, No. 1, pp13-15, 2006*

[41] *S. Heikman, S. Keller, S.P. DenBaars, U.K. Mishra "Growth of Fe doped semi-insulating GaN by metalorganic chemical vapour deposition" Applied Physics Letters, Vol. 81, No. 3, pp 439-441, 2002*

[42] *Nidhi, T. Palacios, A. Chakraborty, S. Keller, U.K. Mishra "Study of impact of access resistance on high-frequency performance of AlGaN/GaN HEMTs by measurement at low temperature" IEEE Electron Device Letters, Vol. 27, No. 11, pp 877-880, 2006*

[43] *T. Palacios, S. Rajan, A. Chakraborty, S. Heikman, S. Keller, S.P. DenBaars, U.K. Mishra "Influence of the dynamic access resistance in the g_m and f_T linearity of AlGaN/GaN HEMTs" IEEE Transactions on Electron Devices, Vol. 52, No. 10, pp 2117-2123, 2005*

[44] *T. Palacios, A. Chini, D. Buttari, S. Heikman, A. Chakraborty, S. Keller, S. DenBaars, U.K. Mishra "Use of double channel heterostructures to improve the access resistance and linearity in GaN-based HEMTs" IEEE Transactions on Electron Devices, Vol. 53, No. 3, pp 562-565, 2006*

[45] *Y. Pei, F. Recht, N. Fichtenbaum, S. Keller, S.P. DenBaars, U.K. Mishra "Deep submicron AlGaN/GaN HEMTs with ion implanted source/drain regions and non-alloyed ohmic contacts" Electronics Letters, Vol. 43, No. 25, pp 1466-1467, 2007*

[46] *N.Q. Zhang, S. Keller, G. Parish, S. Heikman, S.P. DenBaars, U.K. Mishra "High breakdown GaN HEMT with overlapping gate structure" IEEE Electron Device Letters, Vol. 21, No. 9, 2000*

[47] *Y.F. Wu, M. Moore, A. Saxler, T. Wisleder, P. Parikh "40-W/mm double field-plated GaN HEMTs" IEEE 64th Device Research Conference, pp 151-152, 2006*

[48] *W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, H. Ohashi "High breakdown voltage AlGaN-GaN power-HEMT design and high current density switching behavior" IEEE Transactions on Electron Devices, Vol. 50, No. 12, pp 2528-2531, 2003*

[49] *N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, M. Asif Khan "The 1.6-kV AlGaN/GaN HFETs" IEEE Electron Device Letters, Vol. 27, No.9, pp 716-718, 2006*

[50] *Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S.P. DenBaars, U.K. Mishra "High breakdown voltage achieved on AlGaN/GaN HEMTs with intergrated slant field plates" IEEE Electron Device Letters, Vol. 27, No.9, pp 713-715, 2006*

[51] *W. Shockley, U.S. Patent 2 569 347, 1951*

[52] *W.Götz, N.M. Johnson, J. Walker, D.P. Bour, R.A. Street "Activation of acceptors in Mg-doped GaN grown by metalorganic chemical vapour deposition" Applied Physics Letters, Vol. 68, No. 5, pp 667-669, 1996*

[53] *H. Amano, M. Kito, K. Hiramatsu, I. Akasaki "P-type Conduction in Mg-Doped GaN Treated with Low Energy Electron Beam Irradiation (LEEBI)" Japanese Journal of Applied Physics, Vol. 28, No. 12, pp 2112-2114, 1989*

[54] *S. Nakamura, M. Senoh, T. Mukai "Highly p-typed Mg-Doped GaN Films Grown with GaN Buffer Layers" Japanese Journal of Applied Physics, Vol. 30, No. 10A, pp 1708-1711, 1991*

[55] *S. Nakamura, T. Mukai, M. Senoh, N. Iwasa "Thermal Annealing Effects on P-Type Mg-Doped GaN Films" Japanese Journal of Applied Physics, Vol. 31, Part 2, No. 2B, pp 139-142, 1992*

[56] *S. Nakamura, N. Iwasa, M. Senoh, T. Mukai "Hole Compensation Mechanism of P-Type GaN Films" Japanese Journal of Applied Physics, Vol. 31, Part 1, No. 5A, pp 1258-1266, 1992*

[57] *"GaN and Related Materials II" Gordon and Breach Publishers, Vol. 7, pp 93-171, 2000*

[58] *W. Kim, A. Salvador, A.E. Botchkarev, O. Aktas, S.N. Mohammad, H. Morcoç "Mg-doped p-type GaN grown by reactive molecular beam epitaxy" Applied Physics Letters, Vol. 69, No. 4, pp 559-561, 1996*

[59] *H. Xing, D.S. Green, H. Yu, T. Mates, P. Kozodoy, S. Keller, S.P. Denbaars, U.K. Mishra "Memory effect and redistribution of Mg into sequentially regrown GaN layer by metalorganic chemical vapour deposition" Japanese Journal of Applied Physics, Vol. 42, No. 1, pp 50-53, 2003*

[60] *J. Han, A.G. Baca, R.J. Shul, C.G. Willison, L. Zhang, F. Ren, A.P. Zhang, G.T. Dang, S.M. Donovan, X.A. Cao, H. Cho, K.B. Jung, C.R. Abernathy, S.J. Pearton R.G. Wilson "Growth and fabrication of GaN/AlGaN heterostructure bipolar transistor" Applied Physics Letters, Vol. 74, No. 18, pp 2702-2704, 1999*

[61] *D.C. Look, G.C. Farlow, P.J. Drevinsky, D.F. Bliss, J.R. Sizelove "On the nitrogen vacancy in GaN" Applied Physics Letters, Vol. 83, No. 17, pp 3525-3527, 2003*

[62] *X.A. Cao, S.J. Pearton, A.P. Zhang, G.T. Dang, F. Ren, R.J. Shul, L. Zhang, R. Hickman, J.M. Van Hove "Electrical effects of plasma damage in p-GaN" Applied Physics Letters, Vol. 75, No. 17, pp 2569-2571, 1999*

[63] *L.S. McCarthy, P. Kozodoy, M.J.W. Rodwell, S.P. DenBaars, U.K. Mishra "AlGaN/GaN Heterojunction Bipolar Transistor" IEEE Electron Device Letters, Vol. 20, No. 6, pp 277-279, 1999*

[64] *J.J. Huang, M. Hattendorf, M. Feng, D.J.H. Lambert, B.S. Shelton, M.W. Wong, U. Chowdhury, T.G. Zhu, H.K. Kwon, R.D. Dupuis "Graded-emitter AlGaN/GaN heterojunction bipolar transistors" Electronics Letters, Vol. 36, No. 14, pp 1239-1241, 2000*

[65] *F. Ren, J. Han, R. Hickman, J.M. Van Hove, P.P. Chow, J.J. Klaasen, J.R. LaRoche, K.B. Jung, H. Cho, X.A. Cao, S.M. Donovan, R.F. Kopf, R.G. Wilson, A.G. Baca, R.J. Shul, L. Zhang, C.G. Willison, C.R. Abernathy, S.J. Pearton "GaN/AlGaN HBT fabrication" Solid-State Electronics, Vol. 44, pp 239-244, 2000*

[66] *J.B. Limb, L. McCarthy, P. Zozodoy, H. Xing, J. Ibbetson, Y. Smorchkova, S.P. DenBaars, U.K. Mishra "AlGaN/GaN HBTs using regrown emitter" Electronics Letters, Vol.35, No. 19, pp 1671-1673 , 1999*

[67] *J.B. Limb, H. Xing, B. Moran, L. McCarthy, S.P. DenBaars, U.K. Mishra "High voltage operation (>80 V) of GaN bipolar junction transistors" Applied Physics Letters, Vol. 76, No. 17, 2000*

[68] *H. Xing, P.M. Chavarkar, S. Keller, S.P. DenBaars, U.K. Mishra "Very high voltage operation (>330 V) with high current gain of AlGaN/GaN HBTs" IEEE Electron Device Letters" Vol. 24, No. 3, 2003*

[69] *K.P. Lee, A.P. Zhang, G. Dang, F. Ren, J. Han, S.N.G. Chu, W.S. Hobson, J. Lopata, C.R. Abernathy, S.J. Pearton, J.W. Lee "Self-aligned process for emitter- and base-regrowth GaN HBTs and BJTs" Solid-State Electronics, Vol. 45, pp 243-247, 2001*

[70] *L. McCarthy, I. Smorchkova, H. Xing, P. Fini, S. Keller, J. Speck, S.P. DenBaars, M.J.W. Rodwell, U.K. Mishra "Effect of threading dislocations on AlGaN/GaN heterojunction bipolar transistors" Applied Physics Letters, Vol. 78, No. 15, pp 2235-2237 , 2001*

[71] *F. Ren, C.R. Abernathy, J.M. Van Hove, P.P. Chow, R. Hickman, J.J. Klaassen, R.F. Kopf, H. Cho, K.B. Jung, J.R. Laroche, R.G. Wilson, J. Han, R.J. Shul, A.G.*

Baca, S.J. Pearton "300°C GaN/AlGaN heterostructure bipolar transistor" MRS Internet Journal of Nitride Semiconductor Research, Vol. 3, No 41, pp 1-4. 1998

[72] C. Monier, S.J. Pearton, P.C. Chang, A.G. Baca, F. Ren, "Effect of Mg ionisation efficiency on performance of Npn AlGaN/GaN heterojunction bipolar transistors" Applied Physics Letters, Vol. 76, No. 21, pp3115, 3117, 2000

[73] J.J. Huang, M. Hattendorf, M. Feng, D.J.H. Lambert, B.S. Shelton, M.M. Wong, U. Chowdhury, T.G. Zhu, H.K. Kwon, R.D. Dupuis "Temperature dependent common emitter current gain and collector-emitter offset voltage study in AlGaN/GaN heterojunction bipolar transistors" IEEE Electron Device Letters, Vol. 22, No. 4, pp 157-159, 2001

[74] L.S. McCarthy, I.P. Smorchkova, P. Fini, M.J.W. Rodwell, J. Speck, S.P. DenBaars, U.K. Mishra "Small signal RF performance of AlGaN/GaN heterojunction bipolar transistors" Electronics Letters, Vol. 38, No. 2, pp 144-145, 2002

[75] E. Alekseev, D. Pavlidis "DC and high-frequency performance of AlGaN/GaN heterostructure bipolar transistors" Solid-State Electronics, Vol. 44, pp 245-252, 2000

2 Fabrication and Measurement Techniques

2.1 Introduction

This chapter describes the fabrication of Heterostructure Field Effect Transistors (HFETs), Heterojunction Bipolar Transistors (HBTs) and other devices relating to this work. The material used in the fabrication of these devices was grown at either the National Centre for III-V Technologies, Sheffield and at QinetiQ, Malvern using the Metal Organic Chemical Vapour Deposition (MOCVD) growth technique which has been described earlier (chapter 1). Fabrication of all the devices used in this work was performed in a class 10,000 departmental clean room facility at Sheffield University.

2.2 Basic Fabrication Steps

2.2.1 Sample Cleaving

Many semiconductors, such as Si and GaAs for example, are grown on native substrates resulting in an alignment of atomic planes. Therefore, placing a small scratch at the edge of the epitaxial layer and applying a small amount of force results in a predictable and straight cleave. However, due to a lack of a native substrate, epitaxial GaN-based layers are grown pseudomorphically on foreign substrates with closely matching lattice constants. This mismatch between the substrate and epitaxial layers results in misalignment of atomic planes and the inability to easily cleave the sample.

To cleave GaN-based semiconductors a diamond tipped scriber is used. For the work produced in this thesis, samples were cleaved into pieces which measured approximately 1 to 2cm^2. Initially a line is scribed using a straight edge along the desired cleave line. GaN-based samples grown on foreign substrates require a considerable amount of force in order to produce a scribed line which will result in a predictable cleave. Therefore, the scribe is performed on the back of the substrate to mitigate any damage to the epitaxial layers. After the scribe line has been draw the sample is placed between two glass slides with the cleaved line running along the edge of the glass forming a cantilever. To reduce damage to the epitaxial layers the glass slides are wrapped in filter paper. Finally, holding the two slides firmly, a downward force is applied to the back of the sample, usually in the form of a sharp

tap from the hilt of a pair of tweezers. If the scribed line is sufficiently deep and straight, the semiconductor should break at this point. These procedures are repeated in order to produce a number of samples with the appropriate size and shape.

2.2.2 Sample Cleaning

The cleanliness of the sample is of paramount importance throughout the fabrication process. Small particles of dust can have a significant affect on device performance, especially in the case of AlGaN/GaN HFETs where the surface has been shown to be extremely sensitive to processing [1][2]. Therefore, after each fabrication procedure is completed the sample is thoroughly cleaned.

Initially the cleaved sample is boiled in n-butyl for approximately 1 minute. The sample is removed from the solvent and the surface is wiped using a cotton wool bud dipped in the hot n-butyl. It is important to note the sample can only be wiped with a cotton bud at the very first stage of processing. Once features, such as mesas or contacts, have been placed on the surface this process would result in significant damage to the semiconductor. Therefore after the first clean, subsequent cleaning is performed with this step omitted. After wiping the sample it is rinsed again in n-butyl and placed in warm acetone for approximately 30 seconds. The sample is rinsed in hot isopropyl alcohol (IPA) and then blown dry with a nitrogen gun to avoid drying stains on the semiconductor surface. Finally the sample is inspected using an optical microscope. As a rule of thumb, using a magnification of 100 there should be less than 1 particle of dust visible on the surface within the field of view. If this criterion is not met the sample is cleaned again using the same procedure.

2.3 HFET Fabrication Procedures

2.3.1 Layer Sequence for AlGaN/GaN HFETs

The main principles of the AlGaN/GaN heterostructure were covered in the introduction section. In designing the appropriate layer structure the minimum Al content in the buffer layer is restricted by the confinement of the two-dimensional electron gas (2DEG). At Al concentrations less than 15% the conduction band offset

is too small resulting in poor confinement of the 2DEG [3]. A HFET fabricated in this manner would experience considerable leakage making it un-suitable for noise sensitive applications. As the Al fraction is raised the confinement of the 2DEG improves and the sheet charge concentration increases due to the corresponding increase in polarisation induced fields. However, a high aluminium content in the barrier will reduce the critical thickness (defined as the AlGaN thickness after which strain relaxation will occur) [4] potentially resulting in the formation of cracks and relaxation of the AlGaN. This loss in strain will affect piezoelectric polarisation resulting in a significant reduction in the 2DEG concentration. Therefore, the standard structure given in table 2.1 was used in the fabrication of all HFET devices used in this work.

Layer	Material	Thickness	Doping Concentration
Barrier	$Al_{0.25}Ga_{0.75}N$	25nm	-
Buffer	GaN	1200nm	-

Table 2.1 – Layer sequence used for the AlGaN/GaN HFETs.

2.3.2 Defining the Mesa for Device Isolation

Photolithography is a process used to define patterns on the surface of semiconductors before metals are deposited or etching is performed. After cleaning, the sample is placed on a glass slide using a small amount of molten wax. This makes the sample much easier to handle and makes it possible to use the spin coater. After mounting the sample the cover slip is placed on a hot plate and baked at 100°C for 1 minute. This bake ensures there is a negligible amount of solvent or moisture on the surface which may affect the photoresist. After baking, the sample is removed, placed on a Electronic Micro Systems Model 4000 photo resist spinner and blown with N_2. This enables the correct speed of the spinner to be checked and to remove any further contamination which may have occurred after the sample was cleaned. The sample is then coated with BPRS100 photoresist and spun at ≈4000 rpm for 30 seconds. Once the spin is complete the sample is placed back onto the hot plate and baked for a

period of 30 seconds at 100°C. Not accounting for the edge bead, the average thickness of the resist spun under these conditions was found to be ≈900nm, measured using a Dektak 3030 ST profiler.

A chromium mask was used in conjunction with a Karl Suss mask aligner to define the appropriate pattern on the semiconductor surface. Before exposing, the mask is thoroughly cleaned by scrubbing with hot decon solution using a toothbrush then rinsed in water, acetone and IPA. Finally the mask is blown dry with N_2. The mask aligners use either a UV-300 or UV-400 optic system to expose the pattern onto the sample. Samples patterned using the UV-300 optics can define features down to ≈500nm compared to ≈800nm for the conventional UV-400 system.

After exposing, the sample was immersed and agitated in a PLSI: deionised (DI) water (1:3) developer solution, rinsed in water and finally blown dry in N_2. Finally the sample was placed under the microscope to check the exposure. It is important the correct exposure time is used giving a sharp, anisotropic resist profile. Poor resist profiles will lead to problems with both lift-off and edge acuity for deposition of contacts or in the case of etching, may lead to inadequate definition of sidewalls. In order to determine optimum exposure time special features were placed on the mask which can be checked using an optical microscope. If the sample was not correctly exposed the resist was removed in acetone, rinsed in IPA and blown dry in N_2. After removal of the resist the sample was then re-patterned by following the same steps as discussed previously.

2.3.3 Inductively Coupled Plasma (ICP) Etching

Inductively Coupled Plasma (ICP) etching is used to isolate the HFET and allows bond-pads to be placed upon the high resistivity buffer layer, away from the active device. ICP technology relies on the formation of a reactive plasma in the centre of the etch chamber through a surrounding inductive coil. The plasma is transferred to the wafer by an electric field resulting in ion energy and plasma density being independent. This enables high and uniform plasma intensities to be transferred to the sample while keeping incident ion energy low. The sample is etched by the chemical

and physical interactions of the accelerated ions on the exposed semiconductor surface. Due to the strong bonding strength of III-nitrides dry etching is generally ion driven which results in excellent sidewall anisotropy but poor selectivity between materials. For the devices fabricated in this thesis an Oxford Instruments Plasmalab ICP System 100 was used.

For the HFET a $SiCl_4$, Ar, Cl_2 recipe is used with flow rates of 1.5, 4 and 15 standard cubic centimetres per minute (sccm) respectively. The RF power was set to 150W, the ICP power used was 450W and the pressure was set to 4mTorr. Samples were etched using a photoresist mask for a period of 35 seconds. The etch rate under these conditions is approximately ≈150-210nm/min and the mesa is etched down to the high resistivity GaN buffer layer. The mesa height is kept to a minimum in order to reduce mesa leakage whist being deep enough to allow alignment for subsequent photolithography stages. In order to monitor the etch rate in-situ, a laser inferometer is used and after etching the etch depth is verified using a Dektak 3030 ST profiler.

Bombarding the sample with high energy ions results in the surface of the resist becoming hard which makes it difficult to fully remove using acetone. Therefore, the sample is placed in hot resist stripper (Posis-strip EKC 830) and subjected to a 10 minute ultrasonic treatment. Afterwards the sample is rinsed in DI water and washed using the n-butyl, acetone and IPA as outlined previously.

2.3.4 The Source and Drain Ohmic Contacts

To define the ohmic contacts, which make up the source and drain of the HFET, photolithography is used in a similar manner as outlined in section 2.3.2. Previous alignment marks formed in the first mesa isolation step enable alignment to an accuracy of $\approx \pm 1\,\mu m$ in either the x or y plane.

Before any ohmic contacts are deposited onto the semiconductor the sample is immersed in a NH_4OH: DI water (1:9) solution for a period of 5 minutes in order to reduce native oxide on the semiconductor surface. After 5 minutes the sample is rinsed in DI water and blown dry with N_2. The sample is then placed in the

evaporation chamber as soon as possible after the treatment to minimise any re-growth of the oxide.

Ohmic contact metals were thermally evaporated using an Edwards Coating System E306A Evaporator. The metallization scheme used for the HFET devices was Ti (20nm)/Al (100nm)/Ti (45nm)/Au (50nm). All metals were weighed and washed thoroughly in n-butyl for approximately 1 minute before using. Metals are then positioned in degreased tungsten (W) coils or baskets and placed inside the evaporation chamber between two available electrodes. Depending upon the evaporation temperature of the metal, the coil or boat is placed at a different height from the sample which is located at the bottom of the chamber. Metals with melting points below 1100°C are placed at a source to sample distance of 6cm, metals with higher melting points (up to ~1700°C) are placed at a distance of 12cm. This ensures the sample is not excessively thermally stressed during evaporation which may result in hardening of the resist leading to problems such as re-flow and could, in the worst case, result in a failure of the metal to lift-off from the surface. Before deposition of the metals the evaporation chamber is pumped down to a pressure of $\approx 1\text{-}5\times10^{-6}$ Torr. The Precise thickness of deposited metals is monitored in-situ using an Intellemetrics IL200 Thin Film Monitoring Unit. Finally, once the metals have been deposited, the samples are removed from the chamber and soaked in acetone. This removes the un-exposed photoresist underneath the metal, resulting in lift-off and leaving behind the metal in contact with the semiconductor surface.

2.3.5 Annealing Ohmic Contacts

After deposition, the source and drain contacts are found to exhibit rectifying behaviour. An annealing step is required in order to alloy the contacts and make them ohmic. In order to perform this processing step a Mattson rapid thermal anneal (RTA) system was used. This device is able to heat samples to extremely high temperatures (up to 1200°C) in several seconds.

To determine optimum conditions for the HFET a small test piece from each wafer was annealed for various periods of time and at progressively higher temperatures

until the optimum was found. The optimum annealing conditions for the source and drain contacts was found to range from between 800°C for 30 seconds, 800°C for 1 minute or 850°C for 30 seconds depending upon the wafer used. This spread of values demonstrates that differences in growth and subsequent processing can have significant affects upon optimum alloying conditions. After annealing, transmission line modelling (TLM) was used in order to assess the ohmic contacts. Generally contact resistances were found to vary between 0.2Ωmm to 1Ωmm and the sheet resistance of the two dimensional electron gas 2DEG was found to vary from 550Ω/□ to 650Ω/□.

2.3.6 Depositing Bond Pads

Bond pads are necessary to enable the device to be electrically probed or bonded to a header. The bond pads are defined using optical lithography similar to the process outlined in section 1.3.2. For the HFETs the bond pads run down the size of the mesa, away from the active part of the device onto the high resistivity GaN buffer. To achieve good contact the bond pads are made ≈230nm thick. The metals are thermally evaporated using the same process defined in section 1.3.4. The source and drain bond pads are Ti (30nm)/Au (200nm) and sit on top of the ohmic contacts. Ti is used as it is found to adhere well to the semiconductor surface. Since the gate bond pad needs to run up the side of the mesa and sit on the active part of the device, it is necessary to use a metallization scheme which has a higher work function than Ti and consequently Ni is used (Ni (30nm)/Au (200nm)). Therefore in defining the bond pads two photolithography and two evaporation steps are required. It is important to note that Ni does not adhere to the GaN surface very well when compared to Ti, which can result in problems when bonding samples.

2.3.7 Defining the Gate

The gate metals form a Schottky contact to the semiconductor surface so, when a voltage is applied, the depletion region under the gate changes and modulates the carriers in the 2DEG channel. For all HFETs produced in this work Ni/Au gates were used and the thicknesses were changed depending upon the type of resist used. For the

larger gate lengths ($L_G \geq 700$nm) where it was possible to use optical lithography, the standard methods of defining the gate and depositing the metals were used (outlined in sections 1.3.2 and 1.3.4). To maximise f_T and f_{MAX} the gate length must be scaled to smaller, sub-micron lengths. To achieve these smaller features the gates were written using electron beam lithography (EBL). For EBL patterned devices the samples were pre-baked at 100°C for 1 minute to remove any solvent or moisture from the surface. Following this the samples were placed on the spinner and blown with N_2 to remove any contamination from the surface. A PMMA (950K A7) resist, diluted with a thinner (2:1), was spun on the surface at 4000rpm and then soft-baked at 180°C for 4 minutes. The thickness of the resist spun under these conditions was found to be ≈300nm.

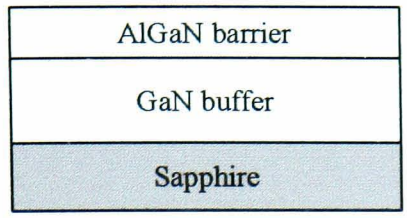
A Raith 150 EBL system was used to define gates with feature sizes <0.7μm. Sapphire is extremely insulating and consequently devices grown using this as a substrate can experience drift when placed in the chamber. This is due to electrons being injected into the semiconductor from the e-beam. Since these charges cannot escape due to the insulating substrate a negative charge accumulates and deflects the impinging beam resulting in a significant reduction in resolution. To overcome this problem, devices grown with sapphire substrates were coated with a thin 20nm thick layer of Al after depositing the resist. The sample is then clamped in the EBL chamber forming an electrical connection which would discharge the semiconductor during writing of the gates. Devices grown on Si substrates did not require the Al layer and consequently this stage was omitted. For all devices with EBL defined gates the gate length, unless otherwise stated, was set to 250nm.

Once the devices were exposed the Al coating was removed in 1:10 decon: DI water, rinsed in DI water and blown dry with N_2. To develop the resist the sample was placed in an MBIK: IPA 3: 1 solution heated to a temperature of 23°C and gently agitated for 30 seconds, then rinsed in IPA and blown dry with N_2. For feature sizes of ≥200nm it was possible to check the development using an optical microscope. Ni (20nm)/Au (90nm) metals were then deposited to form the gate of the HFET.

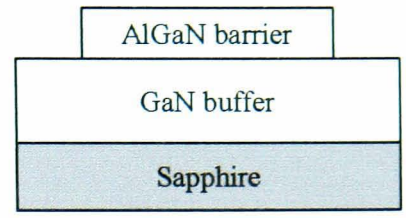
2.3.8 Deposition of Dielectrics

As discussed in chapter 5, AlGaN/GaN HFETs are extremely sensitive to surface conditions. Traps on the surface of the AlGaN can degrade high frequency performance and lead to a reduction in output current commonly referred to as current collapse. Passivating the surface with a deposited dielectric layer can reduce this detrimental effect and greatly improve the RF operating characteristics [1]. Therefore devices were, unless otherwise stated, passivated with Si_3N_4 deposited using a Plasma-Therm 790 Series plasma enhanced chemical vapour deposition (PECVD) system. SiH_4, NH_3 and N_2 were used as precursors to produce the deposited dielectric at flow rates of 100sccm, 5sccm and 900sccm respectively at a pressure of 900mTorr. The base plate temperature was held constant at 60°C and the chamber wall temperature was set to 300°C. Using a Philips Ellipsometer, the deposition rate for standard Si_3N_4 was found to be ≈10nm/min.

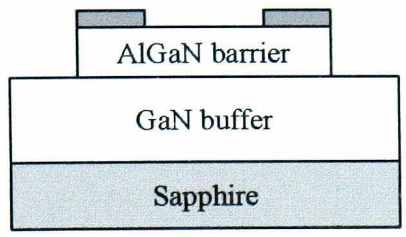
A summary of all the processing steps in chronological order for the AlGaN/GaN HFET is shown in figure 2.1.



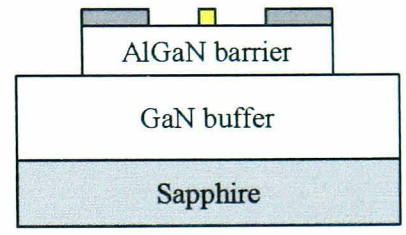
a) HFET structure



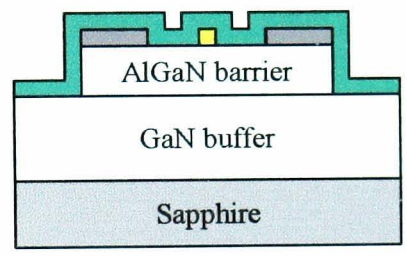
b) Device isolation



c) Depoistion of ohmic contacts



d) Depoistion of rectifying contacts



e) Depoistion of SiN passivation

Figure 2.1 – The fabrication steps required to produce the AlGaN/GaN HFETs used in this work.

2.4 Surface Leakage Test Structure Fabrication

The operation of the surface leakage test structure is discussed in chapter 5 and is fabricated using HFET material. Initially the wafer is cleaved and cleaned as outlined previously. Following this photolithography is used in conjunction with ICP etching to define the mesas. After stripping residual resist, the ohmic contacts (Ti/Al/Ti/Au) are defined, deposited and annealed using the RTA. The Schottky contacts are then defined by photolithography and Ni (20nm)/Au (200nm) is deposited by thermal evaporation. Finally Ti (20nm)/Au (200nm) bondpads are deposited. A summary of

all the processing steps required to fabricate the surface leakage test structure is shown in figure 2.2.

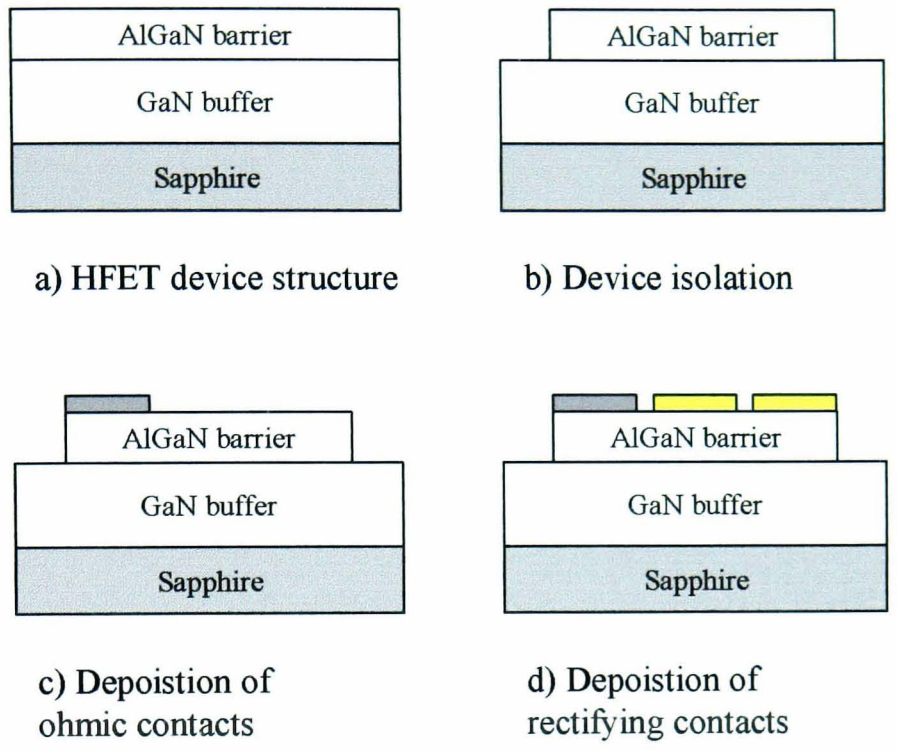


Figure 2.2 – The fabrication steps required to produce the surface leakage test structure.

2.5 HBT Fabrication Procedures

2.5.1 Layer Sequence for AlGaN/GaN HBTs

The main principles of AlGaN/GaN heterostructure bipolar transistors (HBTs) was covered in chapter 1. The design of the layer sequences for both the collector-up geometry and also the Schottky collector are discussed subsequently in chapter 4. The layer sequences for both geometries are summarised in tables 2.2 and 2.3 respectively. All material relating to the HBT was grown using the MOCVD reactor based at the centre for III-V technologies, Sheffield.

Layer	Material	Thickness	Dopant	Type	Doping Concentration
Collector	GaN	700 nm	Si	n	$\sim 1\times10^{17}cm^{-3}$
Base	GaN	100 nm	Mg	p	$\sim 1\times10^{20}cm^{-3}$
Emitter	$Al_{0.05}Ga_{0.95}N$	150 nm	Si	n	$\sim 1\times10^{18}cm^{-3}$
Sub-Emitter	GaN	2000 nm	Si	n	$\sim 1\times10^{19}cm^{-3}$
Buffer	GaN	1000 nm	-	i	-

Table 2.2 – Layer sequence for inverted, collector-up AlGaN/GaN n-p-n HBT

Layer	Material	Thickness	Dopant	Type	Doping Concentration
Base	GaN	T_1, T_2, T_3	Mg	p	$\sim 1\times10^{20}cm^{-3}$
Emitter	$Al_{0.05}Ga_{0.95}N$	150 nm	Si	n	$\sim 1\times10^{18}cm^{-3}$
Sub-Emitter	GaN	2000 nm	Si	n	$\sim 1\times10^{19}cm^{-3}$
Buffer	GaN	1000 nm	-	i	-

Table 2.3 – Layer sequence for Schottky collector AlGaN/GaN HBT. Three layers were grown with base thicknesses of T_1 = 100nm, T_2 = 160nm and T_3 = 200nm.

2.5.2 Defining the Collector Mesa

In order to mitigate damage to the exposed base layer of the HBT the collector was wet etched down to the p-type GaN (section 3.5). Wet etching was performed using an unfiltered Hamamatsu 500W Mg-Xe lamp. The spectrum of this lamp (figure 2.3) was measured by displacing the light through a 50cm single monochrometer and collected into a photomultiplier tube (PMT). As can be seen from the spectrum there is sufficient power in the lower wavelengths below the bandgap of GaN (≤365nm) to create electron hole pairs necessary for etching.

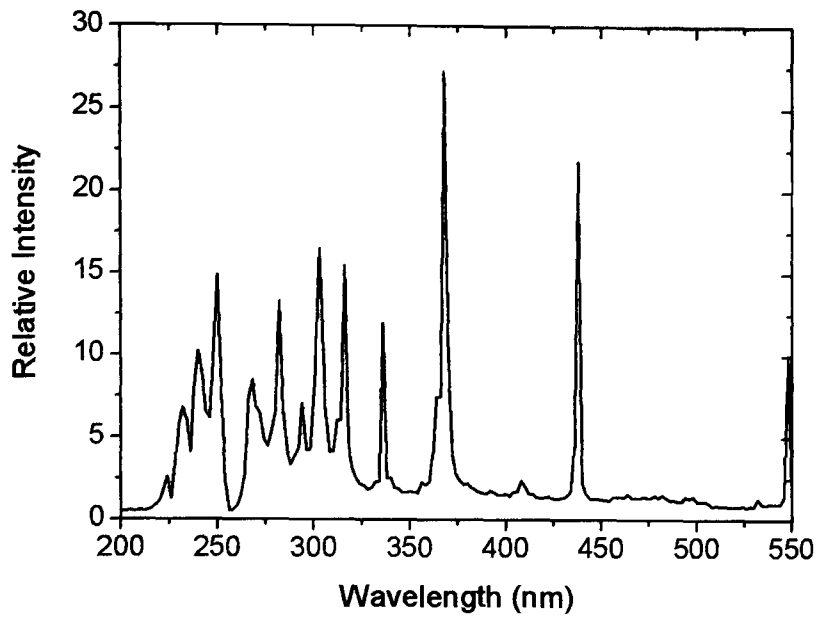


Figure 2.3 – Output spectrum for the 500W Mg-Xe lamp used for etching experiments.

The collector area was defined using photolithography and Ni was used as a catalytic metal mask. The solution concentrations used were 0.3M KOH and 0.1M $K_2S_2O_8$. All solutions were freshly mixed in DI water. The light intensity incident on the sample was ≈70mWcm^{-2}, measured with a Coherent UV laser power meter using the 365nm calibration point. Under these conditions the etch mechanism is selective to the un-activated p-type base layer due to its high resistance. Consequently once the layer is exposed the etch rate will reduce to a negligible level using this light intensity.

Once etching was complete the Ni mask was removed in hydrochloric acid: nitric acid 1: 3 rinsed in deionised water and thoroughly cleaned.

2.5.3 Defining the Base Mesa

Once the collector mesa was etched and the Ni mask removed, the base mesa could then be defined. A BPRS 100 photoresist mask was used in conjunction with ICP etching. The same etching parameters were used as discussed previously. Since the

geometry is inverted the device only needs to be etched through the wide bandgap emitter to the contact layer below, limiting damage to the structure [5].

2.5.4 Activation of the p-type Layer

Once the base is exposed the p-type layer can be activated using a high temperature anneal step. With a significant fraction of the upper n-type collector removed the thermal process can allow the hydrogen to break free from the hydrogen-magnesium complex, diffuse through the material and finally disassociate from the semiconductor surface [6]. A Vecstar furnace was used to activate the p-type layer at 650°C for a period of 30 minutes under an N_2 atmosphere. The anneal time of 30 minutes was defined as the point at which the furnace reaches ±10°C of the desired temperature.

2.5.5 Defining Collector, Emitter and Base Ohmic Contacts

Both the emitter and collector contacts used were the same as for the source and drain ohmic contacts of the HFET. Since the ohmics were deposited onto a highly conductive n-type layer excellent, low resistance contacts were realised. The p-type ohmic contacts were defined by initially mounting the sample on a glass cover slide and pre-baking at 100°C for 1 minute. Following this, the sample was spun and blown with N_2 to remove any contamination from the surface. The sample is coated with BPRS200 photoresist and spun at ≈4000 rpm for 30 seconds. Once the spin is complete the sample is placed back onto the hot plate and baked for a period of 1 minute at 100°C. Not accounting for the edge bead, the average thickness of the resist spun under these conditions was found to be ≈1800nm.

A Pt (10nm)/ Au (150nm) p-type ohmic metallization scheme was employed for the base contacts. Since Pt has a high melting point (1772°C) it is difficult to evaporate using the thermal technique. Consequently an Edwards AUTO 306 e-beam evaporator was used at the centre for III-V Technologies, Sheffield. This system works by using an electron beam, directed using a magnet, to heat material held in a crucible. The sample is held above the crucible on a water cooled mount to minimise any heating. Despite the reduction in temperature during e-beam evaporation, significant heating

still occurs which can affect the resist and make lift-off extremely difficult. Using the thicker BPRS200 photoresist was found to overcome this problem.

A summary of all the processing steps in chronological order for the AlGaN/GaN HBT is shown in figure 2.4.

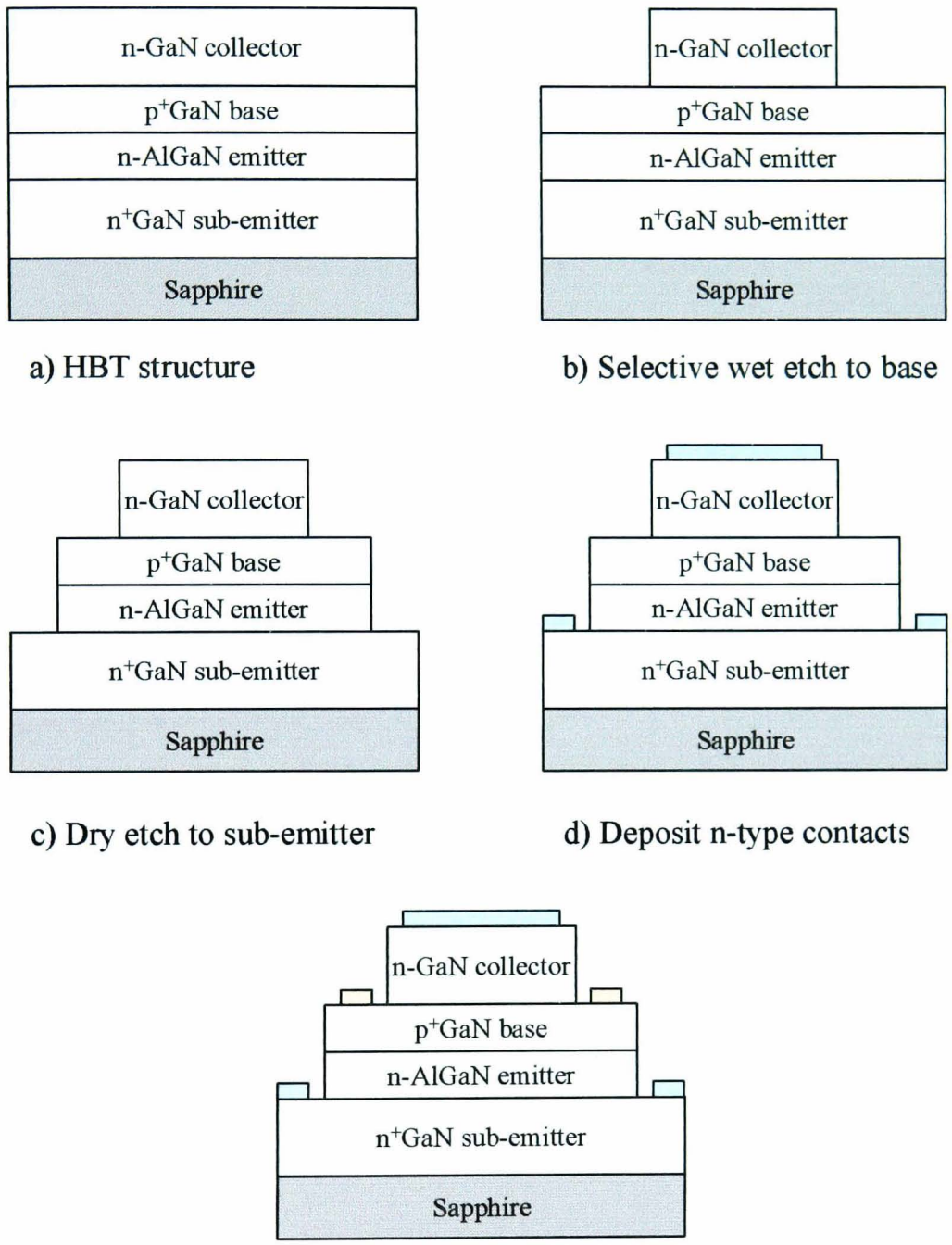


Figure 2.4 – The fabrication steps required to produce the AlGaN/GaN HBTs used in this work.

2.6 Measurement Techniques

2.6.1 Current-Voltage (I-V) Measurement

I-V measurements are the most common methods employed for characterising the AlGaN/GaN HFETs, surface leakage structures and HBTs. Two Keithley source measure units (SMUs) were used in conjunction with a Keithley 2361 trigger controller unit. The setup was controlled by a PC running the appropriate Keithley software to bias the devices and record the resulting current or voltage signal from the SMUs. A schematic of the setup is shown below in figure 2.5.

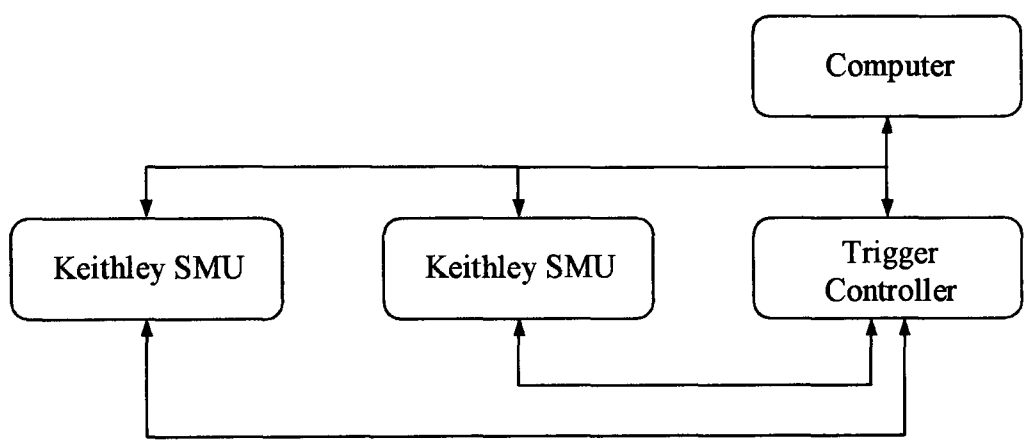


Figure 2.5 – Configuration of Keithley setup to measure the AlGaN/GaN HBTs, HFETs and the surface leakage structure.

The AlGaN/GaN HBTs were measured in the common emitter configuration whereby the output collector current (I_C) is measured with respect to the voltage across the collector and emitter (V_{CE}) with the base current (I_B) held constant. The value for I_B is then changed to build up a family of curves for the HBT. For the HBT no pulse biasing was employed.

The AlGaN/GaN HFETs were biased in the common source configuration whereby the output drain current (I_D) is recorded with respect to a voltage applied across the drain-source (V_{DS}) with the gate-source voltage (V_{GS}) held constant. The measurements are repeated for varying values of V_{GS} to build up the full direct current (DC) HFET characteristic. Since the sapphire substrate is a bad thermal conductor,

significant heating will occur in the channel resulting in a reduction in mobility and consequently a reduction in drain current. Therefore, when measuring the HFET devices, V_{DS} was pulsed to minimise self heating. The minimum pulse width using the Keithley setup of 1ms was used in conjunction with an off time of 25ms.

In order to detect the presence of electrical traps within the HFETs significantly shorter pulse widths are required. To detect these trapping centres a pulse generator is used in conjunction with the circuit shown in figure 2.6. The gate lag measurements work by initially holding the device at a V_{DS} bias above the knee voltage with the device pinched off ($V_{GS} \geq V_{PINCH}$). V_{GS} is then pulsed to a value greater than V_{PINCH} and the corresponding output drain current is measured across a 50Ω resister. The pulse widths used in this experiment were 400ns and the mark space ratio was kept as small as possible to minimise heating of the component.

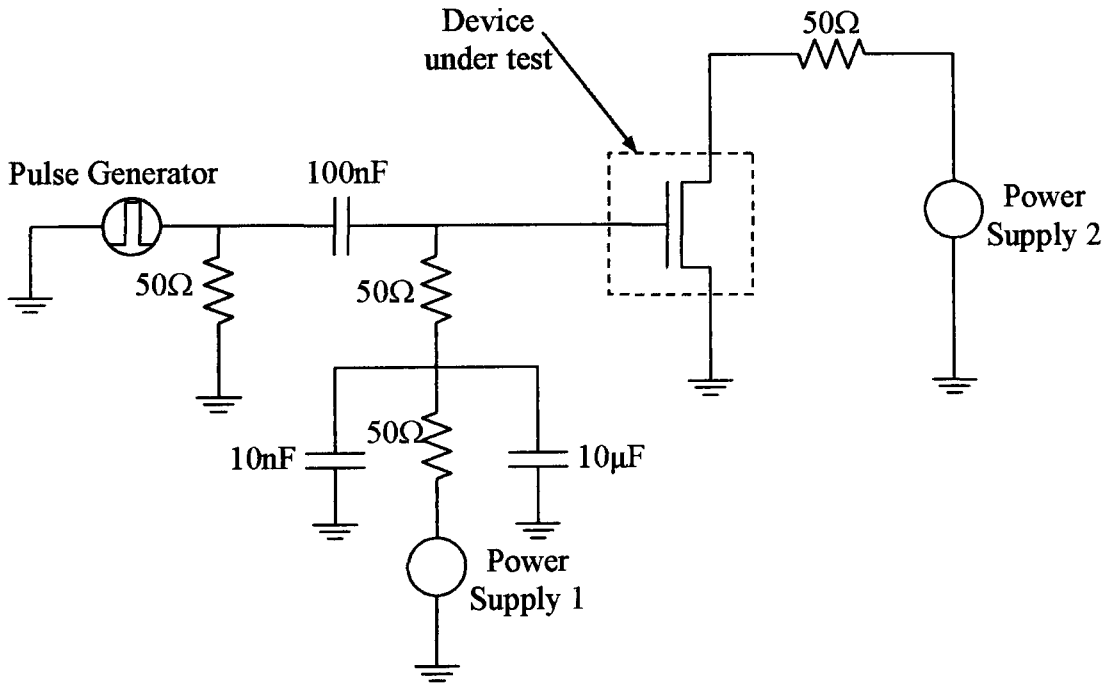


Figure 2.6 – Circuit diagram for the gate lag measurements

2.6.2 Capacitance-Voltage (C-V) Measurement

The Capacitance-Voltage (C-V) technique can be used to determine depletion depth, built in voltage, barrier height and doping concentrations in p-n and Schottky diodes.

The C-V setup is primarily used in this work to determine the doping concentration close to the surface for p-type GaN Schottky diodes.

The C-V setup is shown schematically in figure 2.7 and consists of a probe station to verify the operation of the device, a Hewlett Packard HP4275A inductor capacitor resistor (LCR) impedance meter and a computer to read the capacitance for a given voltage. To ensure an accurate measurement for the capacitance, the phase angle for the impedance should be as close to 90° as possible.

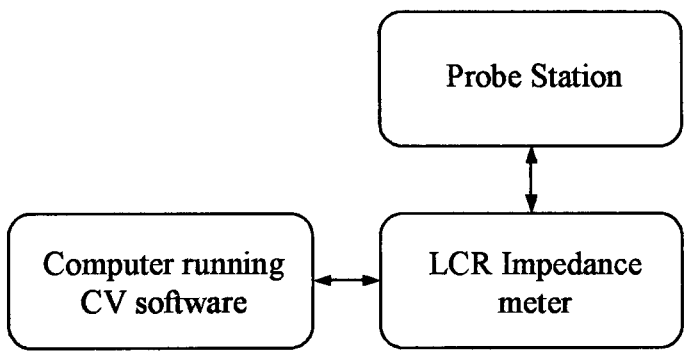


Figure 2.7 – Block diagram showing C-V measurement system

2.6.3 Richardson Plot

The C-V technique cannot always be used to obtain the barrier height for Schottky diodes if the doping concentration in the semiconductor is not constant as in the case of the AlGaN/GaN HFETs (chapter 5) and the p-type Schottky diodes (chapter 4). The I-V characteristics of a Schottky diode can be described by equation 2.1.

$$I = I_S\left(e^{\frac{qV}{nkT}} - 1\right) \qquad \text{Equation 2.1}$$

Where I is the output current, q is the charge on an electron ($1.602\times10^{-19}C$), V is the applied bias, n is the ideality factor for the diode, k is the Boltzmann constant ($8.617\times10^{-5}eVK^{-1}$), T is the temperature in Kelvin and I_S is the saturation current (equation 2.2).

$$I_S = A_e A^* T^2 e^{\frac{-q\phi_B}{kT}} \qquad \text{Equation 2.2}$$

Where A_e is the area of the diode, A^* is the Richardson constant and ϕ_B is the barrier height of the diode.

From the temperature dependent I-V analysis a Richardson plot of $ln(I_S/A_eA^*T^2)$ verses $1/T$ can be obtained. According to equation 2.2 this will result in a straight line allowing the barrier height and the Richardson constant to be determined independently.

2.6.4 TLM Measurement

Transmission line modelling (TLM) is an important tool which enables contact resistance and sheet resistances to be obtained [7]. This method is used in this work to optimise contacts and characterise semiconducting films for both the HFETs and also HBTs. This method works by measuring the resistance between various contacts of equal size as a function of gap spacing. A graph of this data produces a straight line which, when extrapolated to zero spacing, reveals the sum of the contact resistance between the two probed pads. Therefore, this method can be used to determine optimum annealing conditions for ohmic contacts which is important to improve high frequency performance and maximise output power of the devices. Linear TLM is used in conjunction with the HFETs to characterise n-type ohmics and works by placing contacts of equal size onto the semiconductor which is isolated by a mesa etch to prevent current spreading (figure 2.8). This method is advantageous since it does not require significant chip area.

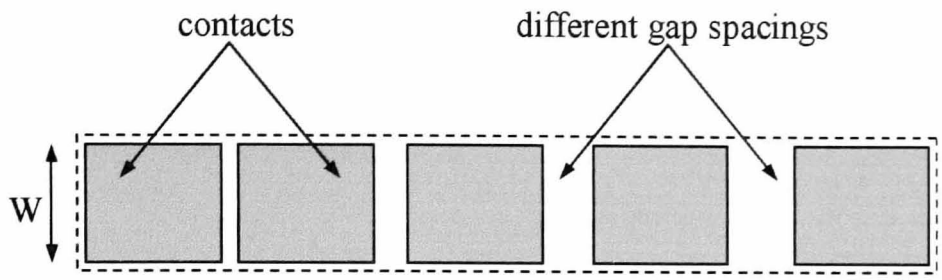


Figure 2.8 – Typical layout for Linear TLM with the dotted line representing the mesa edge.

By plotting a graph of resistance against gap spacing for each of the contacts and assuming the sheet resistance is not affected by the metallization, the total resistance R_T is given by equation 2.3.

$$R_T = 2R_C + \frac{R_{SH}L}{W} \qquad \text{Equation 2.3}$$

Where R_C is the contact resistance, R_{SH} is the sheet resistance, L is the gap spacing and W is the width of the contact pads. The sheet resistance, contact resistance, transfer length (L_T) and specific contact resistance (ρ_C) is then calculated from equations 2.4, 2.5, 2.6 and 2.7 respectively. Typically R_C is normailised to Ωmm by multiplying the obtained value by the width of the contact pad W. Therefore the quoted figure represents the resistance for a 1mm wide contact.

$$R_{SH} = \frac{dy}{dx}W \qquad \text{Equation 2.4}$$

$$R_C = \frac{\text{y - axis intercept}}{2} \qquad \text{Equation 2.5}$$

$$L_T = \frac{x\text{ - axis intercept}}{2} \qquad \text{Equation 2.6}$$

$$\rho_C = \frac{R_C{}^2 W^2}{R_{SH}} \qquad \text{Equation 2.7}$$

To characterise the p-type contacts circular-TLM (CTLM) is used [8]. This reduces processing complexity and also minimises errors due to current spreading effects.

This technique uses a circular contact geometry similar to that shown in figure 2.9. Typically for CTLM $d_2 >> d$ which means more chip area is consumed when compared to the linear TLM method.

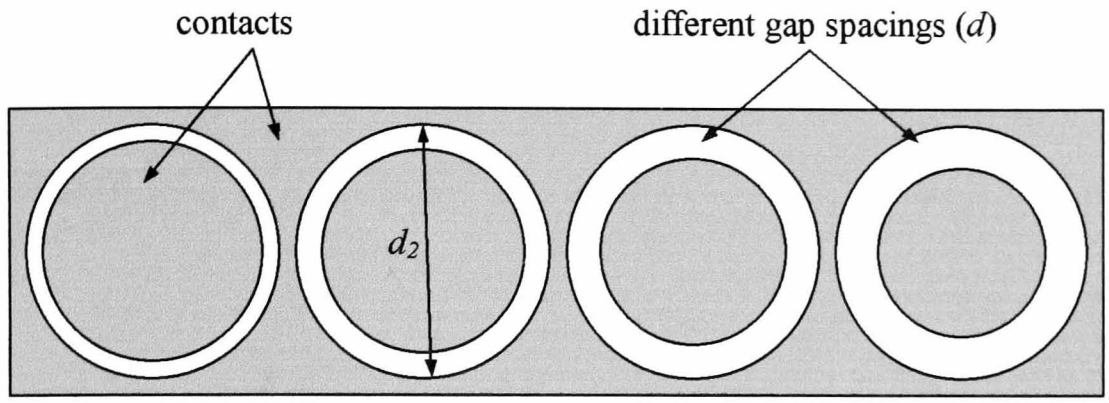


Figure 2.9 – Typical layout for CTLM geometry. Since the contacts are circular there is no need to perform any isolation etching.

The total resistance can then be approximated by applying equation 2.8, where r_2 is the radius of the outer ring [9].

$$R_T = \frac{R_{SH}}{2\pi}\left[\ln\frac{r_2}{r_2 - d} + L_T\left(\frac{1}{r_2 - d} + \frac{1}{r_2}\right)\right] \qquad \text{Equation 2.8}$$

As d increases the graph of resistance verses contact spacing deviates from a straight line and a small correction factor is required to fit the data [8]. The correction factor α, which must be multiplied to the obtained resistance, can be found by applying equation 2.9 for a given gap d [10].

$$\alpha = \frac{r_2\left[\ln\frac{r_2}{r_2 - d} + L_T\left(\frac{1}{r_2 - d} + \frac{1}{r_2}\right)\right]}{2L_T + d} \qquad \text{Equation 2.9}$$

The sheet resistance (with W equal to the circumference of the outer ring) and contact resistance is calculated as before. The transfer length and specific contact resistance is found from equations 2.10 and 2.11 respectively.

$$L_T = \frac{R_C W}{R_{SH}}$$ Equation 2.10

$$\rho_C = L_T{}^2 R_{SH}$$ Equation 2.11

2.7 References

[1] *S. Keller, Yi-Feng, G. Parish, N. Ziang, J.J. Xu, B.P. Keller, S. DenBaars, U.K. Mishra "Gallium nitride based high power heterojunction field effect transistors: process development and present status at UCSB" IEEE Transactions on Electron Devices, Vol. 48, No. 3, pp 552-559, 2001*

[2] *T.R. Prunty, J.A. Smart, E.M. Chumbes, B.K. Ridley, L.F. Eastman, J.R. Shealy "Passivation of AlGaN/GaN heterostructure with silicon nitride for insulated gate transistors" Proceedings of the 2000 IEEE/Cornell Conference on High Performance Devices, Ithaca, New York, pp 208, 2000*

[3] *O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman "Two-dimensional electron gasses induced by spontaneous and piezoelectric polarisation charges in N- and Ga-face AlGaN/GaN heterostructures" Journal of Applied Physics, Vol. 85, No. 6, pp 3222-3233, 1999*

[4] *J.W. Matthews and E. Klolholm "Fracture of brittle epitaxial films under the influence of misfit stress" Materials Research Bulletin, Vol. 7, No. 3, pp 213-221, 1972*

[5] *H. Xing, P. M. Chavarkar, S. Keller, S. P. DenBaars, U. K. Mishra "Very High Voltage Operation (>330V) With High Current Gain of AlGaN/GaN HBTs" IEEE Electron Device Letters, Vol. 24, No. 3, pp 141-143, March 2003.*

[6] *S. Nakamura, T. Mukai, M. Senoh, N. Iwasa "Thermal Annealing Effects on P-Type Mg-Doped GaN Films" Japanese Journal of Applied Physics, Vol. 31, Part 2, No. 2B, pp 139-142, 1992*

[7] *W. Schockley, Report No. Al-TOR-64-207, Air Force Atomic Laboratory, Wright Patterson Air Force Base, Ohio, 1964*

[8] *G.S. Marlow, M.B. Das "The effects of contact size and non-zero metal resistance on the determination of specific contact resistance" Solid State Electronics, Vol. 25, No. 2, pp 91-94, 1982*

[9] *S.S. Cohen, G.S. Gildenblat "Metal-Semiconductor contacts and devices" Academic Press, Orlando FL, 1986*

[10] *L.F. Lester, J.M. Brown, J.C. Ramer, L. Zhang, S.D. Hersee "Nonalloyed Ti/Al ohmic contacts to n-type GaN using high-temperature premetallization anneal" Applied Physics Letters, Vol. 69, No. 18, pp 2737-2739 , 1996*

3 Wet Etching of GaN

3.1 Introduction

Etching of GaN-based devices is commonly performed using dry etch techniques such as reactive ion etching (RIE). This relies on the formation of a plasma which is generated by placing a reactive gas between two Radio Frequency (RF) electrodes. GaN-based samples are positioned on one of the electrodes and are etched by the chemical and physical interactions of the high-energy ions incident on the surface. In order to achieve smooth and anisotropic etching the plasma density, and therefore ion energy, must be high. This energetic bombardment of the surface can lead to damage of the sample resulting in degradation of electrical and optical properties. This problem can be partially alleviated by using inductively coupled plasma (ICP) etching (chapter 2).

Dry etching of GaN-based materials has been shown to create damage on the exposed semiconductor surface [1][2]. It is believed the bombardment of reactive ions on the semiconductor results in point defects which take the form of nitrogen vacancies. Nitrogen vacancies in GaN introduce shallow states into the bandgap below the conduction band edge and hence act as donors [3]. Damage of the exposed surface forms a highly conductive leakage path which degrades device performance. This is especially true in the etching of p-type GaN where ion-induced damage causes compensation at the surface resulting in poor quality ohmic contacts [4].

Photo-electrical chemical (PEC) etching has been shown to be successful in etching GaN-based semiconductors. Conditions required to obtain smoothly etched surface morphologies using the PEC technique have been extensively investigated. However, to date no studies showing how light intensity and solution concentration affect etch rate and final surface morphology in electrode-less etching have been presented. The work presented in this chapter investigates these aspects and also explores the effects upon the etch mechanism of changing the geometry and type of catalytic mask used on the semiconductor surface. Damage to the semiconductor surface is investigated by analysing the I-V characteristics for both wet and dry etched rectifying diodes. Furthermore the etch selectivity is investigated showing that it is possible to fabricate devices with buried p-type layers such as AlGaN/GaN heterostructure bipolar transistors (HBTs).

3.2 Photo-Electro Chemical Etching of GaN

A wet etch for unintentionally doped (UID) and n-type GaN has been demonstrated using the PEC technique [5]-[7]. This involves immersing a sample, which is electrically connected to a remote Pt counter electrode, in an electrolyte solution and illuminating the surface with ultra-violet (UV) light. In order for etching to occur the semiconductor must be illuminated with above bandgap light (≤365nm for GaN, corresponding to the UV part of the spectrum). Photo-generated holes travel to the surface due to an electric field induced by band bending where they react with hydroxide ions in the electrolyte to form gallium oxide (equation 3.1). The surface oxide then dissolves in the alkaline solution (equation 3.2).

$$2GaN + 6h^+ + 6OH^- \rightarrow Ga_2O_3 + 3H_2O + N_2 \qquad \text{Equation 3.1}$$

$$Ga_2O_3 + 6OH^- \rightarrow 2GaO_3^{3-} + 3H_2O \qquad \text{Equation 3.2}$$

The rate of etching is heavily dependent on conditions at the semiconductor-electrolyte interface. Surface potential at this boundary results in band bending revealing a thin layer of depleted material. For n-type GaN positive donor ions in the crystal structure are revealed which attracts both holes and negatively charged hydroxide ions to the semiconductor-electrolyte interface (figure 3.1a). In p-type material band bending at the surface is reversed repelling holes and reactive ions therefore preventing the etch mechanism (figure 3.1b).

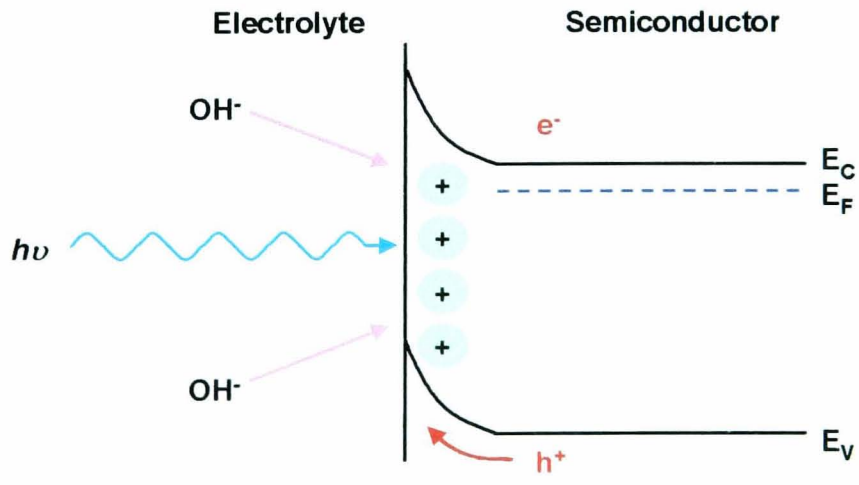


Figure 3.1a – Band bending at the surface of an n-type GaN layer

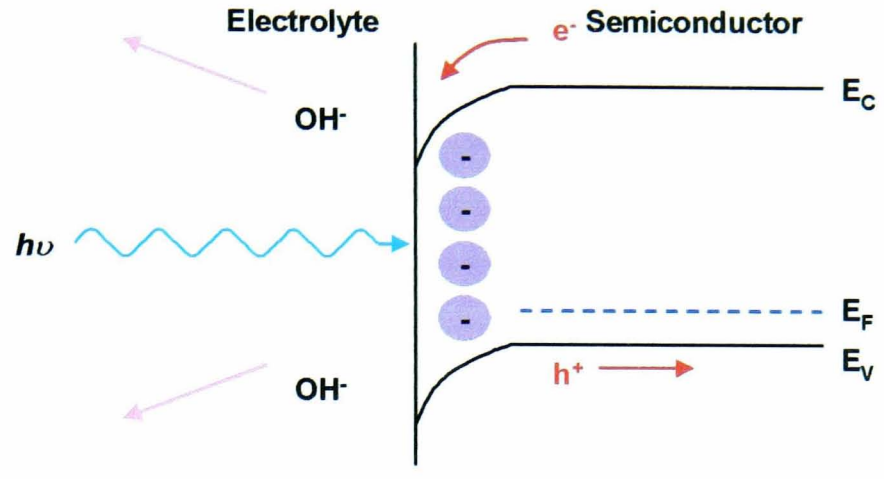


Figure 3.1b – Band bending at the surface of a p-type GaN layer

Morphologies of etched surfaces were shown to be dependent on both solution concentration and UV light intensity. C. Youtsey et al [7] showed by increasing UV power incident on the sample a linear increase in etch rate was initially observed for all solution concentrations. This indicates the reaction is limited by the creation of electron hole pairs (EHP) at the surface of the semiconductor. With further increase in light intensity the etch rate became constant signifying the diffusion of reactants in the solution limited the etching mechanism. Under diffusion limited conditions the PEC etch was found to give very smooth surface morphologies. Diffusion limited etching was observed for high light intensities and low solution concentrations. Using this information PEC etching of GaN was demonstrated with a root mean square (RMS) surface roughness of 1.5nm using a 0.01M KOH solution and 10mWcm^{-2} UV light intensity measured at 365nm [5]. However, under diffusion limited conditions the etch rate is sensitive to geometry with etching occurring faster at the sidewalls of the mask.

Using low light intensities in conjunction with high solution concentrations resulted in rough surface morphologies. Under these conditions tiny stems or whiskers were observed which are orientated perpendicular to the etched surface. These whiskers usually extend up to the original surface and can be removed in a hot KOH solution after etching or by an ultrasonic treatment. It is believed each whisker represents the site of a threading dislocation (TD) within the original GaN material [6]. TDs are

thought to act as recombination centres and hence at these points there are fewer EHP to participate in the reaction given by equation 3.1.

PEC etching requires an electrical contact to the semiconductor which is impractical for fabrication. This contact means only devices grown on a conducting substrate (such as 6H-SiC) or which have a fully interconnected mask can be etched using this technique.

3.3 Electrode-Less Chemical Etching of GaN-Based Material

Recently a wet etch for GaN was demonstrated by Bardwell et al [8] which eliminated the need for the Pt counter electrode by adding an oxidising agent to locally consume electrons from the semiconductor surface (equation 3.3). This allows processing of GaN grown on insulating substrates such as sapphire. The oxidising agent used was $K_2S_2O_8$ due to its stability in the alkaline solution and soluble reaction products. In this work etching unintentionally doped (UID) material using a Pt catalytic mask produced etch rates of 30nm/min and surfaces with 20nm RMS roughness [9]. The use of a high work function metal such as Pt on the surface can speed up the reaction due to the creation of electrons when exposed to UV light. The photo-generated electrons are consumed at the semiconductor interface resulting in an increase in current and therefore a corresponding increase in etch rate.

$$S_2O_8^{2-} + 2e^- \rightarrow SO_4^{2-} \qquad \text{Equation 3.3}$$

3.4 Wet Etching of Bulk GaN Layers

To investigate the wet etch, bulk UID GaN was grown using metalorganic chemical vapour deposition (MOCVD) with a thickness of 2.5μm on a sapphire substrate. The layer structure exhibited a smooth surface morphology after growth. Optical lithography was used to pattern the samples with a ≈50nm thick catalytic Ni or non-catalytic Ti mask. Prior to deposition of the metals the samples were treated in 9:1 ammonia: DI water for 5 minutes to remove native oxide from the surface to prevent the metals from lifting off during etching (equation 3.2). In order to determine how the quantity of catalytic metal present on the surface affected etch rate, samples were

patterned using separate masks. One set of samples were patterned using a light-field mask which coated the majority of the surface with Ni. The second set of samples were patterned with an inverted dark-field version of the first mask which left the majority of the semiconductor surface exposed.

Wet etching was carried out using an unfiltered 500W Hg-Xe lamp which served as the UV source. The light intensity incident on the sample was estimated with a Coherent UV laser power meter using the 365nm calibration point. All solutions were freshly mixed in deionised (DI) water. In order to reduce heating effects caused by the bulb, etch times were kept to a minimum with the longest etch period before changing the solution being 10 minutes.

Using samples patterned with the light-field Ni mask the effect of lowering the KOH concentration was investigated while keeping light intensities and the $K_2S_2O_8$ concentration constant at 70mWcm^{-2} and 0.1M respectively. Measured etch depths were seen to increase linearly with increasing KOH concentration (figure 3.2). The line of best fit passes through the origin which indicates the 9:1 ammonia: DI water treatment was successful in removing native oxide from the surface of the sample prior to metallization. For samples patterned using a dark-field Ni mask etch rates decreased by over an order of magnitude, making it unsuitable for device fabrication (≈1nm/min using 0.1M KOH). This is due to less catalytic metal on the surface which results in a limited amount of photo-generated electrons consumed by the solution and therefore a reduction in etch rate [10]. Etching using a non-catalytic Ti mask also produced extremely slow etch rates similar to those obtained using the dark-field Ni mask. This clearly shows etch rate is strongly affected by not only the type of mask used, but also by the area of catalyst present on the semiconductor surface when using the electrode-less wet etching technique.

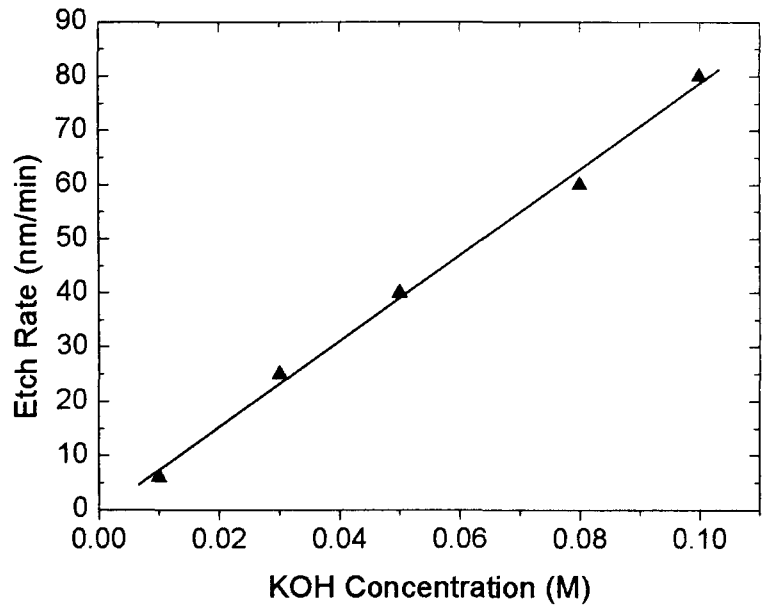


Figure 3.2 – Etching of bulk GaN using varying KOH concentrations with the amount of $K_2S_2O_8$ kept constant at 0.1M. A 500W Hg-Xe bulb was used as the UV source.

Using a light-field Ni mask and high KOH solution concentrations (>0.06M), the resulting etched morphology became extremely rough as shown in figure 3.3. Under these conditions many tiny stems or whiskers could be seen extending from the surface. Previous investigations have shown these whiskers originate from threading dislocations (TDs) within the material [11]. These defects act as recombination centres resulting in a localised reduction of holes and a decrease of etch rate at these points. Therefore the crystalline GaN surrounding the TD is removed first, revealing the location of the dislocation.

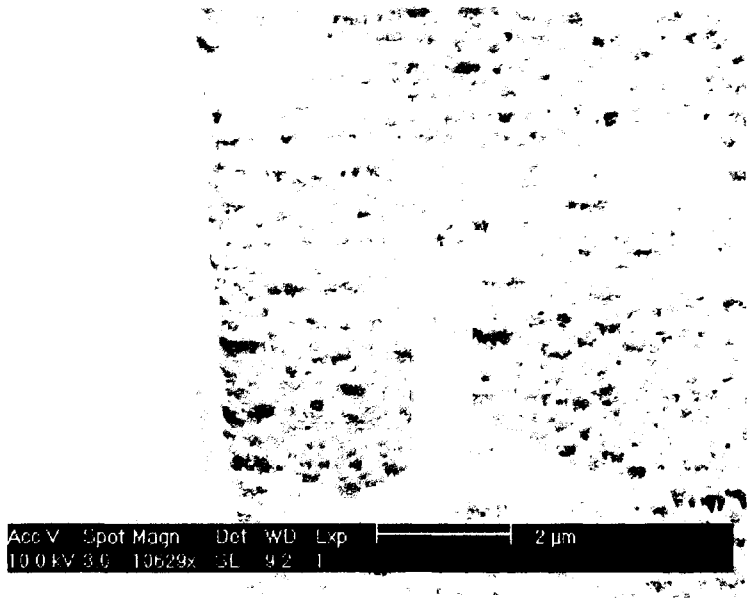


Figure 3.3 – Bulk GaN etched using 0.05M KOH and 0.1M $K_2S_2O_8$ in conjunction with a UV light intensity of 70mWcm^{-2} (measured at 365nm).

Figure 3.4 shows the variation of root mean squared (RMS) surface roughness as a function of KOH concentration, using 0.1M $K_2S_2O_8$ and a light intensity of 70mWcm^{-2}. For all these samples the etch time was adjusted to give an approximate etch depth of 400nm. At concentrations of 0.04M or less the etch mechanism became diffusion limited with etching occurring faster at the edge of the mask due to local variations in solution concentration. Therefore, the reaction is limited by how fast hydroxide ions within the solution can diffuse to the semiconductor surface and not by the rate at which electron-hole pairs are generated within the material by exposure to the UV light. The surface morphology became significantly smoother under these conditions (figure 3.5). Stirring of the solution in conjunction with low KOH concentrations and high light intensities caused surfaces to become extremely rough, similar to that shown in Figure 3. It was also observed the etch mechanism was no longer diffusion limited due to the faster transport of reactants to the semiconductor surface. This result agrees with previous work on PEC and electrode-less wet etching which showed that surface roughness increased under stirred conditions [6][7].

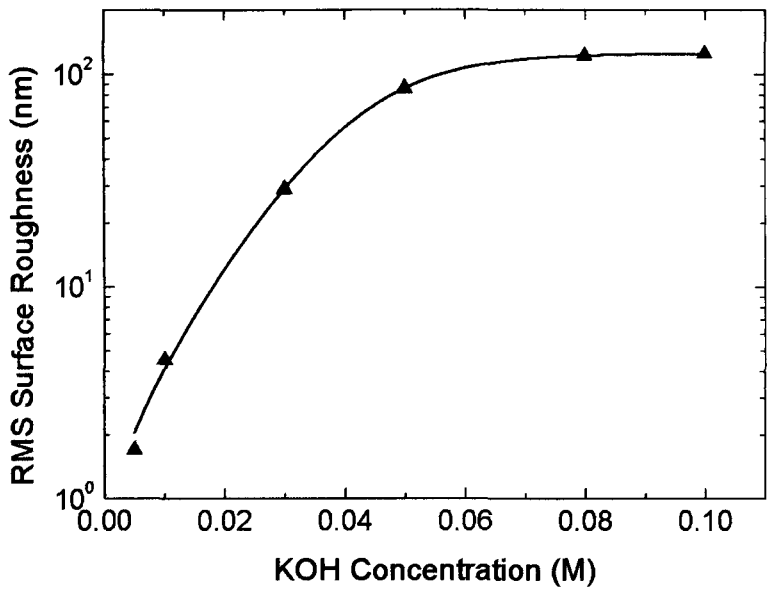


Figure 3.4 – RMS surface roughness of bulk GaN using varying KOH concentrations with the amount of $K_2S_2O_8$ kept constant at 0.1M. A 500W Hg-Xe bulb was used as the UV source. The RMS roughness of the un-etched surface was measured to be 0.16nm.

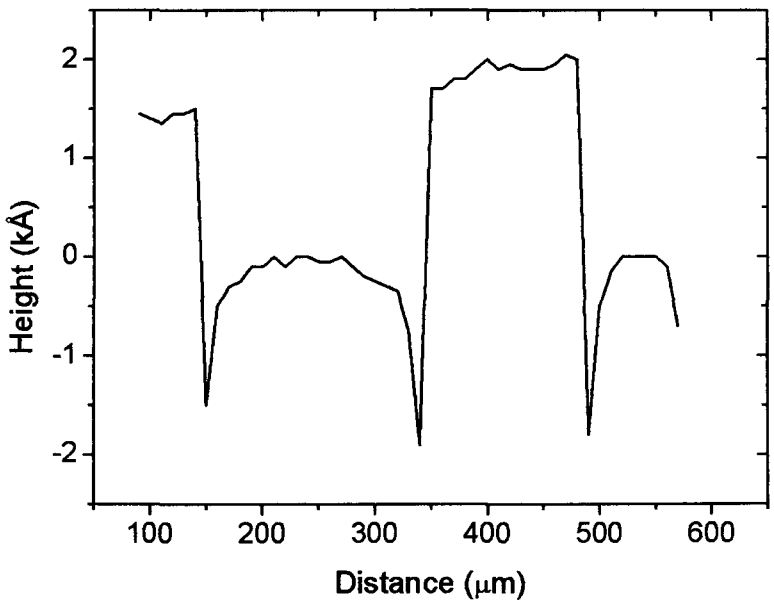


Figure 3.5 – Etch profile for GaN using the wet etch technique under diffusion limited conditions. The solution concentrations used were 0.3M KOH and 0.1M $K_2S_2O_8$.

The effect on etch rate of lowering the light intensity on the sample, while keeping the KOH concentration constant, is shown in figure 3.6. Initially etch rates increase approximately linearly with UV light intensity for a fixed amount of KOH, indicating etching is limited by electron-hole generation. At sufficiently high UV power the etch rate becomes relatively constant, signifying the onset of diffusion limited conditions. This means the rate of electron-hole generation at the semiconductor surface due to the UV light exceeds the rate at which hydroxide ions diffuse towards the semiconductor surface. It was noted under these conditions the surface morphologies became significantly smoother. For higher KOH concentrations higher intensity light is required to achieve diffusion limited etching. These results are consistent with those for the PEC technique [7]. However, for electrode-less etching significantly higher light intensities are required in order to obtain diffusion limited conditions. This can be explained by considering the amount of catalyst used in the two different methods. For the PEC technique the catalyst is located away from the sample and can therefore have a sufficiently increased area to maintain a large photocurrent and increase the rate of the reaction. However, the electrode-less method is limited by the area of catalyst which can be used on the surface in the form of the mask, resulting in the observed reduction in etch rate. Therefore to obtain smoothly etched surfaces using the electrode-less method requires not only high light intensities and low solution concentrations but also a catalytic mask which covers the majority of the surface.

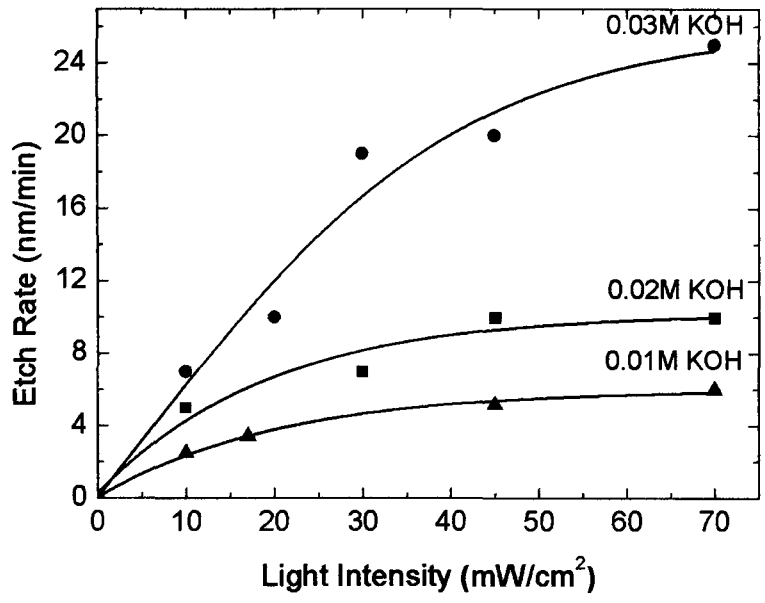


Figure 3.6 – Etch Etch rates as a function of UV light intensity (measured at 365nm) for 0.01 (▲), 0.02 (■) and 0.03M (●) KOH. The amount of $K_2S_2O_8$ was kept constant at 0.1M.

Bardwell et al [9] reported that to obtain smoothly etched surfaces the etch rate should be limited to <30nm/min. This was achieved through reducing UV light intensity on the sample while maintaining a relatively high solution concentration. It was believed etching at this slow rate was necessary in order to allow defects within the material to etch at the same rate as the GaN. This is contrary to the results presented in this work where a reduction in the light intensity incident on the sample would actually result in an increase in surface roughness. This reason for this discrepancy is unclear, however it should be noted that Bardwell used material grown by molecular beam epitaxy whereas in this work the MOCVD technique is used. In addition to this, differences in the mask, material quality and experimental setup may have also impacted on the observed inconsistency between results. Fang et al [12] reported extremely smooth etched surfaces, although the etch rate was <1nm/min making it unsuitable for device fabrication. Our investigation has shown smooth morphologies are dependent on solution concentration, UV intensity and the area of catalyst present on the surface. Therefore using an appropriate geometry, with a sufficiently large area catalytic mask

and high light intensity, it becomes possible to obtain smooth surfaces at an increased etch rate, making the technique more suitable for the fabrication of electronic devices. Using these results smooth etching of bulk UID GaN was demonstrated using solution concentrations of 0.005M KOH and 0.1M $K_2S_2O_8$ in conjunction with a continuous light intensity of 70mWcm^{-2} which had an RMS surface roughness of 1.7nm (Figure 3.7). It is evident from the SEM image shown in figure 3.7 that the surface roughness is higher at the edge of the mask compared to the surface several microns away. This is due to the diffusion limited effect. At the edge of the mask there are more hydroxide ions which are diffusing to the semiconductor surface since they do not react with the Ni. This results in a localised increase in the etch rate close to the mask and, since light intensity is constant across the semiconductor surface the surface roughness close to the edge of the sidewall will increase (figure 3.4). These results should be taken into account when etching feature sizes less than approximately 1μm.

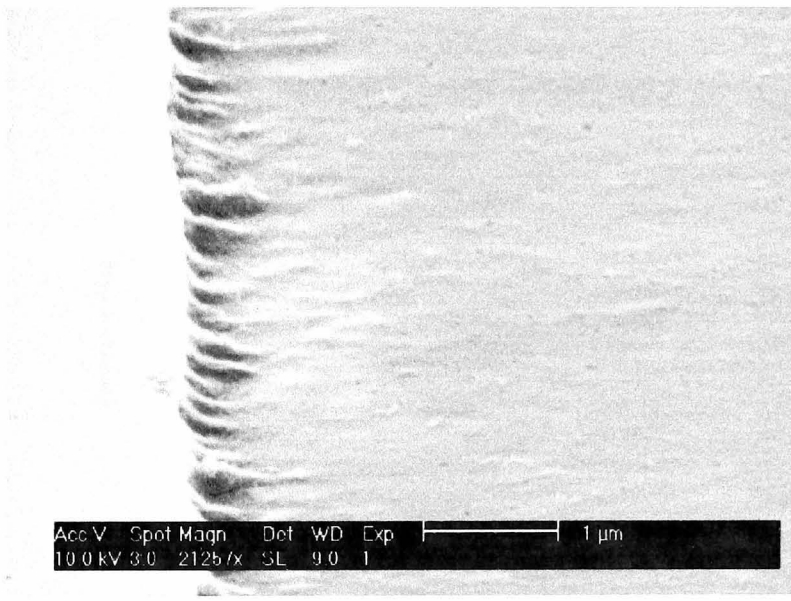


Figure 3.7 – Bulk GaN etched using solution concentrations of 0.005M KOH and 0.1M $K_2S_2O_8$ in conjunction with a 500W Hg-Xe bulb.

3.5 Selectivity of the Wet Etch

To compare the properties of wet and dry etching an n-p structure was grown on sapphire by MOCVD. After the standard nucleation a 2μm thick Mg doped (1×10^{20}cm^{-3}) p-type layer was deposited. Using non-selective re-growth, to prevent the Mg memory effect [13], an upper Si doped (1×10^{18}cm^{-3}) 750nm thick n-type

region was subsequently grown. For both structures the group III precursors used were trimethylgallium (TMG) and trimethylaluminium (TMA) and the group V precursor was ammonia (NH_3). N-type and p-type doping was achieved through the introduction of silane (SiH_4) and bis-cyclopentadienyl-magnesium (Cp_2Mg) respectively.

From the previous section the conditions required to produce rapid etching of n-GaN were determined. Since the selectivity naturally achieves smooth p-surfaces, etch conditions were chosen for rapidity rather than smoothness. It should be noted that since etching is performed with the p-type layer un-activated, the etch mechanism is not truly selective. However, since the p-GaN is highly resistive before the thermal treatment the etch rate will reduce to a negligible level once the layer is exposed. The n-p sample was etched using the same experimental setup as previously described. The concentrations used were 0.3M KOH, 0.1M $K_2S_2O_8$ and the light intensity incident on the sample was $\approx$70mWcm^{-2} (measured at 365nm). Under these conditions the etch mechanism was found to be selective to the un-activated p-type layer due to its high resistance. Consequently once the layer is exposed the etch rate will reduce to a negligible level using this light intensity. Employing higher light intensity by using a 325nm HeCd 25mW laser resulted in etching of the un-activated p-type material. However, following activation it was found that no etching occurred under any conditions. After uncovering the underlying region, the sample was placed in an ultrasonic bath for 10 minutes to remove whiskers originating from the etched surface. A SEM image of a mesa formed on a typical re-gown n-p structure is shown in figure 3.8. This demonstrates the selectivity of the wet etch and shows it could be useful in the fabrication of devices such as N-p-n HBTs where the thin buried p-type layers are difficult to access using dry etch techniques.

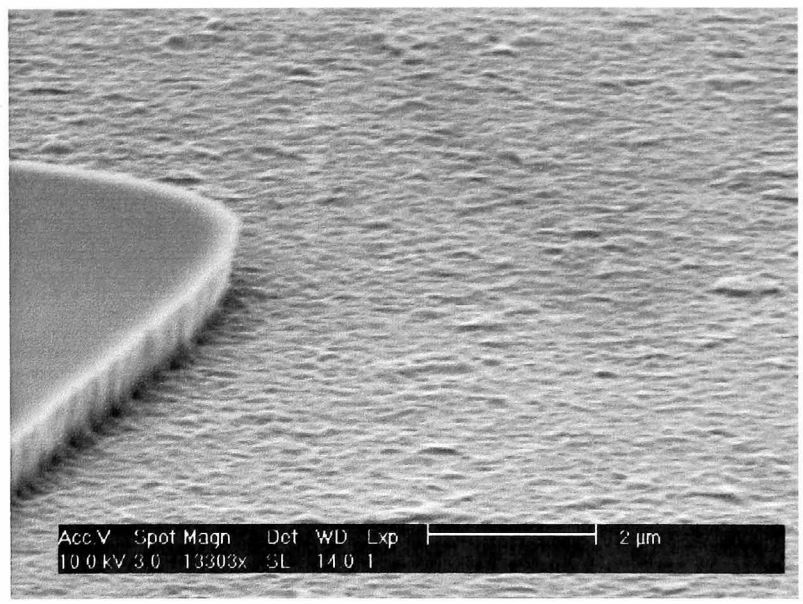


Figure 3.8 – Formation of an n-type mesa on a re-grown n-p structure using a 0.3M KOH, 0.1M $K_2S_2O_8$ solution in conjunction with a 500W Hg-Xe bulb.

Current state-of-the-art AlGaN/GaN n-p-n HBT devices are fabricated by employing a selective re-growth to form the emitter. This mitigates the need to etch to the thin and electrically sensitive p-type base layer [14][15]. This method has resulted in devices with gains of up to 18 at room temperature [16]. However, the size of the emitter area for re-growth is limited and for areas of $\leq 10\mu m^2$ the edge acuity and surface morphology of the emitter is very poor [17]. Therefore the re-growth technique can only produce large area emitters which are not suitable for high frequency applications. Since the wet etch is highly anisotropic, as the UV light will not penetrate the Ni mask, this technology could be used to form the emitter of a HBT, removing the need to re-grow the emitter selectively and allowing emitter areas of $\leq 10\mu m^2$ to be realised. Furthermore, due to the high selectivity between the n- and p-type layers this process could be easily applied to a manufactures' fabrication line.

It was possible to increase the UV light intensity incident on the sample to $\approx 160 mWcm^{-2}$ (measured at 325nm) by using the collimated output of a 325nm He-Cd laser. Employing the laser in conjunction with high KOH concentrations ($\geq 0.3M$) resulted in a significant increase in etch rate of the un-activated p-type material. However, the etched surfaces were found to be extremely rough, similar to that shown in figure 3.3. After the activation anneal, p-type conduction is obtained resulting in band bending at the GaN surface which repels the hydroxide ions resulting in true

selectivity. Therefore, under these conditions for activated p-GaN wet etching will not occur under any circumstances.

It is widely believed that hydrogen, which is present during growth of the MOCVD produced material, passivates Mg doped GaN acceptors [18]. Upon annealing, the hydrogen gains sufficient energy to break free from the H-Mg complex, allowing it to move through the crystal lattice and disassociate from the GaN surface. Activation of the p-type layer was attempted using an un-etched sample (i.e. with the p-type layer buried beneath the upper n-type region). Therefore the un-etched samples were annealed in flowing N_2 using the temperatures listed in table 3.1. The surface morphology of the epitaxial film was found to alter when annealing at 1050°C. Using an optical microscope, small dark circles (~100μm diameter) were observed on the surface of the material. GaN gown by metal organic chemical vapour deposition (MOCVD) on sapphire substrates has been shown to be stable up to temperatures of ≈800°C before decomposition occurs [19]. In the temperature range from 800°C to 1000°C degradation of the semiconductor is limited to the N-sublattice. N is preferentially removed, leaving behind a Ga rich surface [20]. Nitrogen vacancies have been shown to act as shallow donors in GaN-based materials and therefore increase the surface n-type conductivity [3]. Damage to the Ga-sublattice only becomes significant at temperatures exceeding ≈1000°C. At these excessively high temperatures significant damage occurs within the bulk of the semiconductor and material is evaporated from the surface [21]. Therefore this change in surface morphology is attributed to evaporation of material from the sample and a corresponding significant reduction in material quality. To prevent this damage an AlN encapsulation layer could be used, which acts as a diffusion barrier [22], or annealing the device under high pressure [23].

Temperature	Anneal time
700°C	20 minutes
950°C	15 minutes
1050°C	30 seconds
1050°C	1 minute
1050°C	10 minutes

Table 3.1 – Temperatures used in an attempt to activate p-type GaN layers prior to formation of the mesa. All activations were performed in a flowing N_2 atmosphere.

After the high temperature treatment the samples were patterned with a Ni mask as before and etched using solution concentrations of 0.3M KOH and 0.1M $K_2S_2O_8$. After exposing the p-type region it was discovered that no activation of acceptors had occurred for any of the samples. This agrees with theoretical predictions [24] and other experimental results [25] which show hydrogen rapidly diffuses in p-GaN but not in n-type material. Therefore it was necessary to expose the underlying p-type region before thermal activation. Once the p-type region had been uncovered the layer was activated at 650°C for 30 minutes in an N_2 atmosphere.

To ensure p-type activation occurs for the entire layer (i.e. under n-type mesa) and not just for the exposed p-GaN surface, a sample was patterned with a Ni mask and etched as described previously. The Ni mask was removed in 3:1 $HCl:HNO_3$ and the material activated. Finally the sample was re-etched using a high KOH concentration in conjunction with the 25mW He-Cd laser. The etch removed the mesas but failed to attack the underlying material, indicating p-type conductivity. The size of the mesas used in this experiment was 200μm×200μm implying that the escaping hydrogen has diffused a maximum of 100μm during the high temperature treatment. This gives a minimum diffusion coefficient of $\geq 125 \mu m^2 min^{-1}$. It should be noted, while an accurate diffusion coefficient was not obtained, the true value is believed to be significantly higher than the above figure.

3.6 Damage in Wet and Dry Etched Structures

In order to assess the viability of the wet etch for device fabrication GaN Schottky and p-n junctions were produced. For the Schottky diodes the bulk nominally undoped GaN was etched to a depth of ≈400nm using wet and ICP dry etching. The wet etched devices were fabricated using a 0.005M KOH, 0.1M $K_2S_2O_8$ solution at a UV light intensity of 75mWcm^{-2} (measured at 365nm). The dry etch structures were fabricated using an Oxford Instruments Plasmalab system 100 ICP etching machine with a $SiCl_4/Ar/Cl_2$ recipe with flow rates of 1.5, 4 and 15 standard cubic centimetres per minute (sccm) respectively. The pressure was set to 4mTorr and the ICP power was 450W. For the dry etched diodes the RF power used was varied from 150W to 10W. Following etching, Ti (20nm) /Al (100nm) /Ti (45nm) /Au (55nm) ohmic contacts were deposited and annealed at 850°C for 1 minute in an N_2 atmosphere. Finally a Ni (20nm) /Au (200nm) rectifying contact was deposited onto the recessed surface. To compare damage for wet and dry etching a Schottky diode was fabricated with no recess.

For the p-n junction diodes the n-type mesas were formed using the techniques described previously and once exposed, the p-type GaN was activated at 650°C in flowing N_2 for a period of 30 minutes. A second set of diodes were produced using conventional ICP dry etch techniques. For the dry etch a BPRS 100 resist mask was used in conjunction with the conventional $SiCl_4$-based plasma. The RF power used was 100W and the ICP power was set at 150W. The Ti (20nm) /Al (100nm) /Ti (45nm) /Au (55nm) and Pt (10nm) /Au (150nm) metallization schemes were used for n-type and p-type contacts respectively. Both contacts were alloyed simultaneously at 800°C for a period of 1 minute in flowing N_2.

The forward and reverse I-V characteristics of the Schottky diodes are shown in figure 3.9a. The reverse leakage current for the diodes measured at -2 volts is shown in Figure 3.9b. For all dry etched diodes the leakage current was found to be extremely high when compared to the control sample. For RF powers greater than 10W the leakage current stays relatively constant. At 10W there is a significant reduction in leakage current. However, the leakage current is still ≈3 orders of magnitude greater than the un-etched diode. This reduction is attributed to a reduction in incident ion

energy which limits damage to the GaN surface. Reducing the RF power below 10W was found to be problematic as the plasma failed to strike. As mentioned previously the damage to the GaN is likely to take the form of nitrogen vacancies which introduce shallow states into the band gap below the conduction band edge. These states will reduce the Schottky diode barrier width resulting in an increase in tunnelling. This increase in leakage has been observed by others in the literature [26] and some have taken advantage of it for reducing n-type contact resistances [27].

For the wet etched diodes it can be seen from figures 3.9a and 3.9b that the leakage is comparable to the control sample indicating minimal damage to the exposed surface.

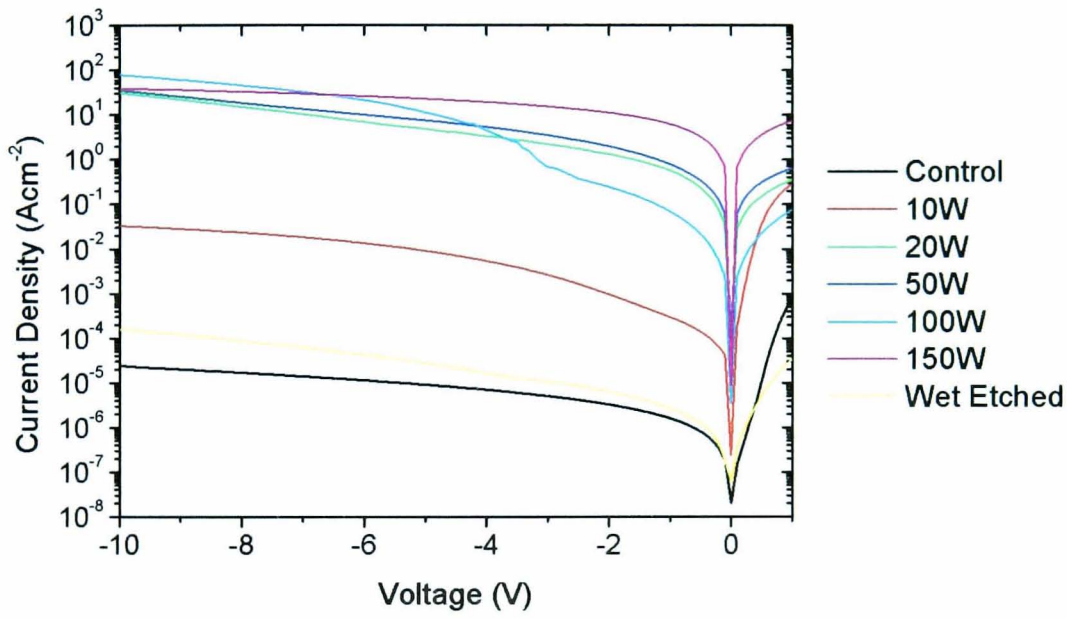


Figure 3.9a – I-V characteristics for dry and wet etched Schottky diodes.

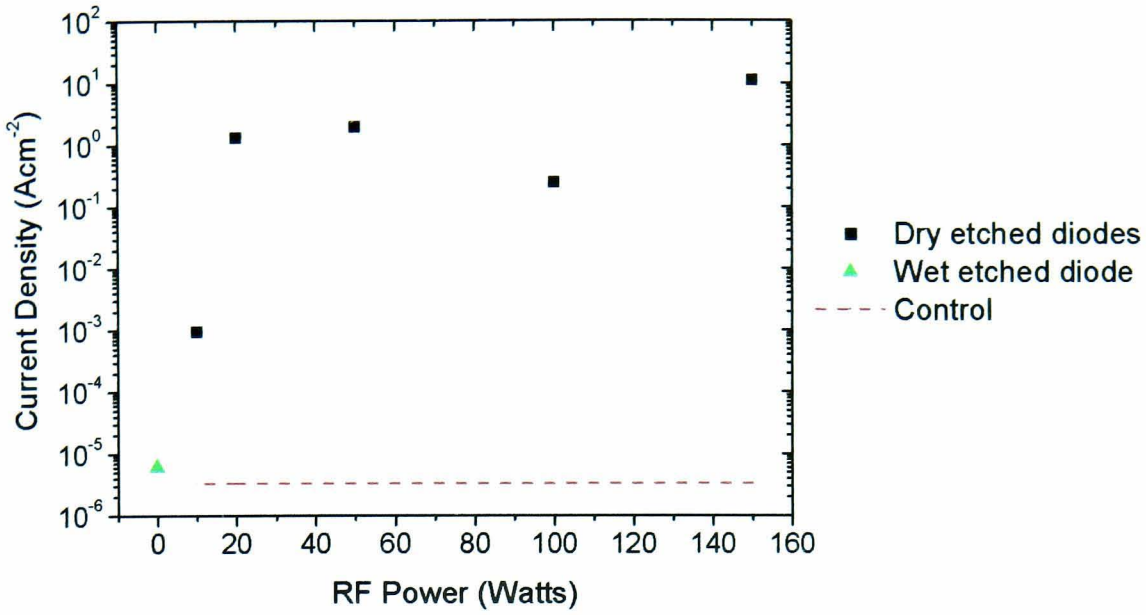


Figure 3.9b – Leakage current for wet and dry etched rectifying diodes compared to an un-etched diode measured at 2 volts reverse bias.

For the p-n junction diodes both n- and p-type contacts were shown to exhibit ohmic behaviour. However, the p-type contacts formed on dry etched surfaces show higher resistance which is due to the introduction of ion-induced plasma damage on the surface of the exposed p-type layer. This compensates the p-type acceptors at the surface resulting in increased resistance. In contrast, the wet etch has mitigated this detrimental effect by transferring minimal damage to the exposed layer (figure 3.10). The forward I-V characteristics for diodes fabricated using the wet etch show an ideality factor of 1.6 and a saturation current density (J_o) of $\approx$6nAcm^{-2} (figure 3.11). For dry etched diodes the ideality factor was >2 indicating highly resistive ohmic contacts.

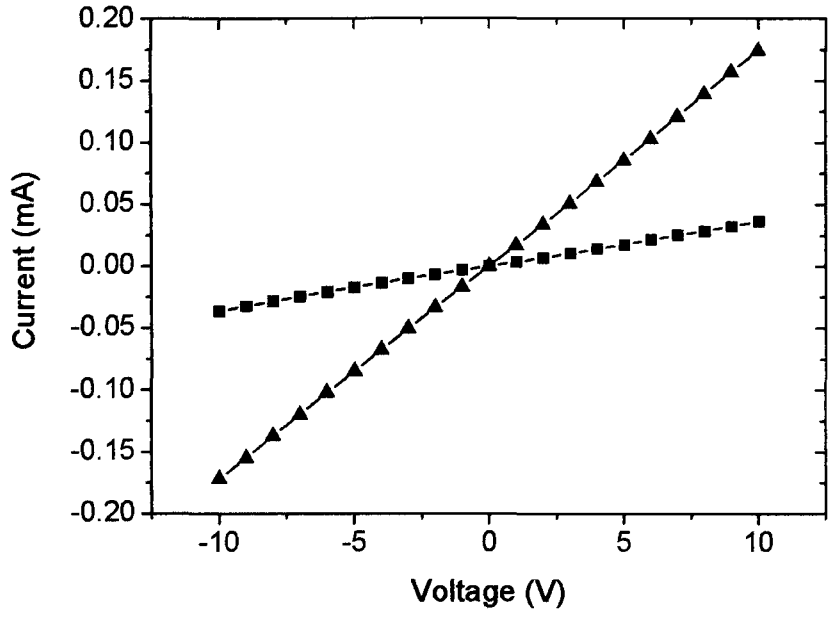


Figure 3.10 – Comparison of I-V characteristics for Pt/Au contacts deposited on p-GaN layers exposed by dry (■) and wet (▲) etching. The gap spacing between contacts was 30μm.

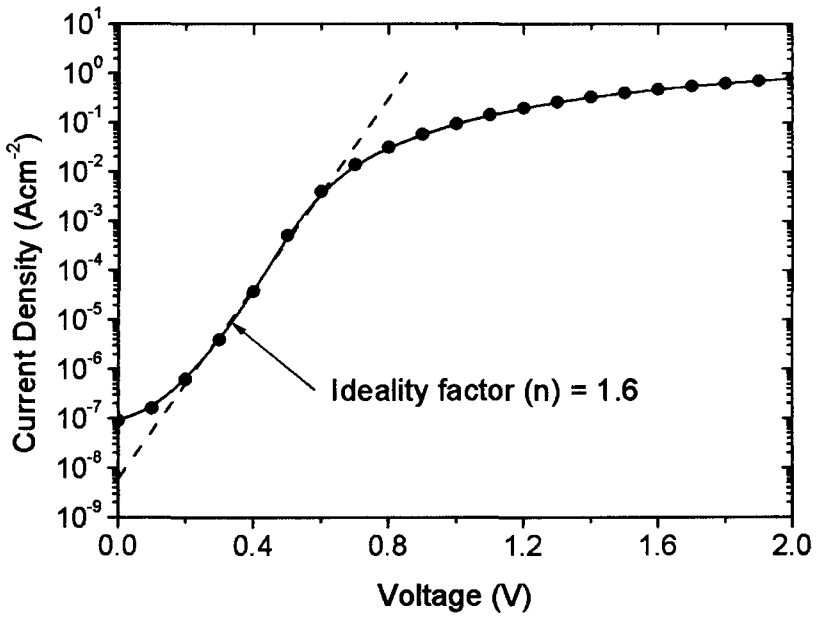


Figure 3.11 – Forward I-V characteristic for a p-n diode fabricated using the wet etch technique. The dotted line is a guide to the eye to show where the gradient of the I-V characteristic was taken.

3.7 Conclusions

Wet etching of GaN-based semiconductors using $KOH/K_2S_2O_8$ solutions has been shown to be an effective method of fabricating electronic devices. However, catalytic masks which cover the majority of the sample surface are needed for the electrode-less method to achieve sufficiently high etch rates. It has been shown experimentally that etching under diffusion limited conditions is necessary to produce smoothly etched GaN surfaces. To obtain these conditions high light intensities, low KOH solution concentrations and a catalytic mask which covers the majority of the surface are required. Due to the limited amount of catalyst on the semiconductor surface the amount of light intensity required to obtain diffusion limited conditions is higher than when compared to PEC etching. In this work etching of bulk GaN grown on a sapphire substrate has been demonstrated with a surface roughness of 1.7nm RMS using solution concentrations of 0.005M KOH and 0.1M $K_2S_2O_8$ in conjunction with a UV light intensity of $70mWcm^{-2}$ (measured at 365nm). This represents the smoothest surface demonstrated using this technique with continuous UV illumination.

Bulk GaN Schottky diodes were demonstrated using both wet and conventional dry etch techniques. Comparison of output I-V characteristics show the wet etch has transferred minimal damage to the semiconductor surface and leakage currents were approximately equal to an un-etched diode. The leakage currents for the rectifier formed on the wet etched surface was ≈5 orders of magnitude greater when compared to dry etched diodes fabricated at RF powers greater than 10W. The Schottky contact formed at 10W RF power exhibited ≈3 orders of magnitude more leakage.

The etch selectivity has been exploited to create n-type mesas on a re-grown n-p structure. Excellent ohmic contacts to the uncovered p-type surface were obtained when compared to those formed on dry etched surfaces. This further demonstrates that the wet etch has transferred minimal damage to the semiconductor surface and may be useful in the fabrication of devices with buried p-type layers such as AlGaN/GaN N-p-n HBTs. Due to the high selectivity, minimal undercut and low damage the wet etch represents a method of producing small area mesas ($\leq 10\mu m^2$) which is useful for the

fabrication of high frequency AlGaN/GaN HBTs. Furthermore, since the process is highly selective this technology could be easily applied to a manufacturing line.

3.8 References

[1] *J.M. Lee, K.M. Chang, S.W. Kim, C. Huh, I.H. Lee, S.J. Park "Dry Etch Damage in n-type GaN and its Recovery by Treatment with N_2 plasma" Journal of Applied Physics, Vol. 87, No. 11, pp 7667-7670, 2000*

[2] *X.A. Cao, S.J. Pearton, A.P. Zhang, G.T. Dang F. Ren, R.J. Shul L. Zhang, R. Hickman, J.M. Van Hove "Electrical effects of plasma damage in p-GaN" Applied Physics Letters, Vol. 75, No. 17, pp 2569-2571, 1999*

[3] *D.C. Look, G.C. Farlow, P.J. Drevinsky, D.F. Bliss, J.R. Sizelove "On the nitrogen vacancy in GaN" Applied Physics Letters, Vol. 83, No. 17, pp 3525-3527, 2003*

[4] *L.S. McCarthy, P. Kozodoy, M.J.W. Rodwell, S.P. DenBaars, U.K. Mishra "AlGaN/GaN Heterojunction Bipolar Transistor" IEEE Electron Device Letters, Vol. 20, No. 6, pp 277-279, 1999*

[5] *L. H. Peng, C. W. Chuang, J. K. Ho, C. N. Huang, C. Y. Chen "Deep Ultraviolet Enhnaced Wet Chemical Etching of Gallium Nitride" Applied Physics Letters, Vol. 75, No. 8, pp 939-941, 1998*

[6] *J. Škriniarová, A. Van Der Hart, H.P. Bochem, A. Fox, P. Kordoš "Photoenhanced Wet Chemical Etching of n^+-doped GaN" Materials and Engineering, Vol. B91-92, pp 298-302, 2002*

[7] *C. Youtsey, I. Adesida, L. T. Romano, G. Bulman "Smooth n-type GaN Surfaces by Photoenhanced Wet Etching" Applied Physics Letters, Vol. 72, No. 5, pp 560-562, 1998*

[8] *J. A. Bardwell, I. E. Foulds, J. B. Webb, H. Tang, J. Fraser, S. Moisa, S. J. Rolfe "A Simple Wet Etch for GaN" Journal of Electronic Materials, Vol. 28, No. 10, pp 24-26, 1999*

[9] *J. A. Bardwell, J. B. Webb, H. Tang, J. Fraser, S. Moisa "Ultraviolet Photoenhanced Wet Etching of GaN in $K_2S_2O_8$ Solution" Journal of Applied Physics, Vol. 89, No. 7, pp 4142-4149, 2001*

[10] *J. M. Hwang, K. Y. Ho, Z. H. Hwang, W. H. Hung, Kei May Lau, H. L. Hwang "Efficient Wet Etching of GaN and p-GaN Assisted with Chopped UV Source" Superlattices and Microstructures, Vol. 35, pp 45-47, 2004*

[11] C. Youtsey, L.T. Romano, I. Adesida "Gallium Nitride Whiskers Formed by Photoenhanced Wet Etching of Dislocations" Applied Physics Letters, Vol. 73, No. 6, pp 797-799, 1998

[12] C. Y. Fang, W. J Huang, E. Y. Chang, C. F. Lin, M. S. Feng "Etching Damages on AlGaN, GaN and InGaN Caused by Hybrid Inductively Coupled Plasma Etch and Photoenhanced Chemical Wet Etch by Schottky Contact Characterizations" Japanese Journal of Applied Physics, Vol. 43, Part 1, No. 7A, pp 4207-4212, 2003

[13] H. Xing D. S. Green, H. Yu, T. Mates, P. Kozodoy, S. Keller, S. P. Denbaars, U. K. Mishra "Memory Effect and Redistribution of Mg into Sequentially Regrown GaN Layer by Metalorganic Chemical Vapor Deposition" Japanese Journal of Applied Physics, Vol. 42, Part 1, No. 1, pp 50-53, 2003

[14] J.B. Limb, L. McCarthy, P. Kozodoy, H. Xing, J. Ibbetson, Y. Smorchkova, S.P. DenBaars, U.K. Mishra "AlGaN/GaN HBTs using a regrown emitter" Electronics Letters, Vol. 35, No. 19, pp 1671-1673, 1999

[15] J.B. Limb, H. Xing, B. Moran, L. McCarthy, S.P. DenBaars, U.K. Mishra "High voltage operation (>80 V) of GaN bipolar junction transistors with low leakage" Applied Physics Letters, Vol. 76, No. 17, pp 2457-2459, 2000

[16] H. Xing, P. M. Chavarkar, S. Keller, S.P. DenBaars, U.K. Mishra "Very high voltage operation (>330 V) with high current gain of AlGaN/GaN HBTs" IEEE Electron Device Letters, Vol. 24, No. 3, pp 141-143, 2003

[17] K.P. Lee, A.P. Zhang, G. Dang, F. Ren, J. Han, S.N.G. Chu, W.S. Hobson, J. Lopata, C.R. Abernathy, S.J. Pearton, J.W. Lee "Self-aligned process for emitter- and base regrowth GaN HBTs and BJTs" Solid-State Electronics, Vol. 45, pp 243-247, 2001

[18] S. Nakamura, N. Iwasa, M. Senoh, T. Mukai "Hole Compensation Mechanism of P-Type GaN Films" Japanese Journal of Applied Physics, Vol. 31, Part 1, No. 5A, pp 1258-1266, 1992

[19] A. Pisch, R. Schmid-Fetzer "In situ decomposition study of GaN thin films" Journal of Crystal Growth, Vol. 187, pp 329-332, 1998

[20] H.W. Choi, M.A. Rana, S.J. Chua, T. Osipowicz, J.S. Pan "Surface analysis of GaN decomposition" Semiconductor Science and Technology, Vol. 17, pp 1223-1225, 2002

[21] M.A. Rana, T. Osipowicz, H.W. Choi, M.B.H. Breese, S.J. Chua "A study of the material loss and other processes involved during annealing of GaN at growth temperatures" Chemical Physics Letters, Vol. 380, pp 105-110, 2003

[22] J. C. Zolper, D. J. Rieger, A. G. Baca, S. J. Pearton, J. W. Lee, R. A. Stall "Sputtered AlN Encapsulant for High-Temperature Annealing of GaN" Applied Physics Letters, Vol. 69, No. 4, pp 538-540, 1996

[23] S. Porowski, J. Jun, S. Krukowski, I. Grzegory, M. Leszczynski, T. Suski, H. Teisseyre, C.T. Foxon, D. Korakakis "Annealing of gallium nitride under high-N_2 pressure" Physica B, Vol. 265, pp 295-299, 1999

[24] J. Neugebauer, C.G. Van de Walle "Role of hydrogen in doping of GaN" Applied Physics Letters, Vol. 68, No. 13, pp 1829-1831, 1996

[25] A. Y. Polyakov, N. B. Smirnov, S. J. Pearton, F. Ren, B. Theys, F. Jomard, Z. Teukam, V. A. Dmitriev, A. E. Nikolaev, A. S. Usikov, I. P. Nikitina "Fermi Level Dependence of Hydrogen Diffusivity in GaN" Applied Physics Letters, Vol. 79, No. 12, pp 1834-1836, 2001

[26] D.G. Kent, K.P. Lee, A.P. Zhang, B. Luo, M.E. Overberg, C.R. Abernathy, F. Ren, K.D. Mackenzie, S.J. Pearton, Y. Nakagawa "Electrical effects of N2 plasma exposure on dry-etch damage in p- and n-GaN Schottky diodes" Solid-State Electronics, Vol. 45, pp 1837-1842, 2001

[27] J. Yan, M.J. Kappers, Z.H. Barber, C.J. Humphreys "Effects of oxygen plasma treatments on the formation of ohmic contacts to GaN" Applied Surface Science, Vol. 234, pp 328-332, 2004

4 AlGaN/GaN Heterostructure Bipolar Transistors

4.1 Introduction

HBTs offer several important advantages over HFETs including a more uniform threshold voltage, improved linearity and greater power density. These make AlGaN/GaN HBTs attractive candidates for RF applications such as airborne radar, cellular base station power amplifiers and general electronics for high temperature environments.

There are several major aspects relating to the growth and subsequent processing of these devices which have hampered the development of n-p-n AlGaN/GaN HBTs. These include poor placement of the critical base-emitter heterojunction, a high base spreading resistance, poor ohmic contacts to the p-type layer and high leakage currents. As a result of these difficulties there are only a handful of groups which are able to produce working devices. Several of these aspects are addressed within this chapter and various device geometries are investigated in order to overcome some of the key limitations.

4.2 Discussion of Inverted Geometry AlGaN/GaN HBT

Progress in the development of AlGaN/GaN HBTs has been severely hampered by low hole mobilities in the base and the deep acceptor level associated with the only known practical p-dopant, magnesium. Mg suffers from a strong memory effect which results in carry over when growing subsequent junctions [1]-[4]. In the case of the n-p-n AlGaN/GaN HBT this can displace the critical emitter-base heterojunction resulting in a severe decrease in both emitter injection efficiency and gain. Several groups have attempted to overcome the problem of carry over by re-growing the emitter [5]. Further work has concentrated on re-growing the emitter selectively using an inert mask which overcomes the problems of etching to the extremely thin and electrically sensitive base layer [6]-[9]. However, using this method of re-growth is complicated and will undoubtedly lead to the incorporation of interfacial defects which will result in a decrease in the emitter injection efficiency (γ).

To overcome these problems an inverted structure is suggested whereby the device is grown using a collector-up geometry. Since the incorporation of Mg into the growing film occurs rapidly after the Cp_2Mg source is turned on, the lower emitter-base heterojunction can be grown without interruption and with negligible displacement, thereby improving the quality of the interface. The memory effect will be transferred to the less critical base-collector homojunction enabling the device structure to be deposited without interruption greatly simplifying growth. Using the inverted geometry will allow quasi-electric fields across the base to be produced which aid electron transport resulting in reduced transit time and improved gain. Typical Mg decay profiles show a decrease of ≈100nm/decade [2][4][10] which would result in a field of ≈6kVcm^{-1}.

Employing an inverted structure with dissimilar junction areas will result in parasitic injection of electrons underneath the base contacts. These minority carriers will be unable to reach the collector and will recombine in the base resulting in reduced gain (figure 4.1). In the case of AlGaN/GaN bipolar devices where the p-type resistance is high there will be a non-linear voltage drop across the length of the base. Since carrier injection is exponentially dependent on bias this will compound the problem, leading to preferential injection away from the collector in the extrinsic part of the component. To reduce parasitic injection of minority carriers underneath the base contact a p-type implantation will be used which will locally displace the heterojunction channelling current into the centre of the device (figure 4.2). This implantation step, which will not penetrate into the sub-emitter, may also increase near-surface p-type conductivity leading to greatly improved ohmic contacts.

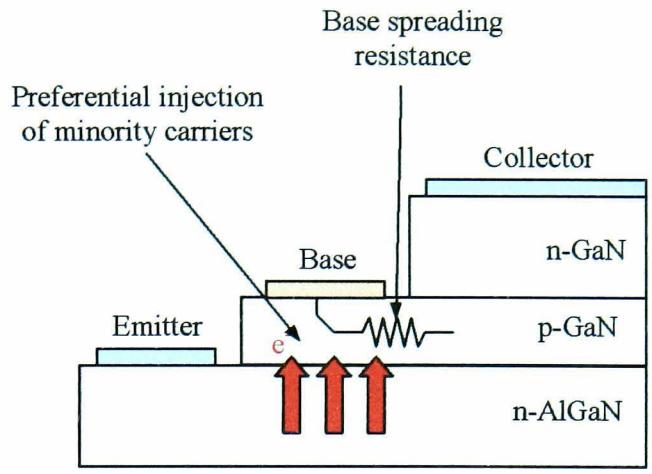


Figure 4.1 – Simple cross section of an inverted AlGaN/GaN HBT showing preferential injection away from the active part of the device underneath the base contacts.

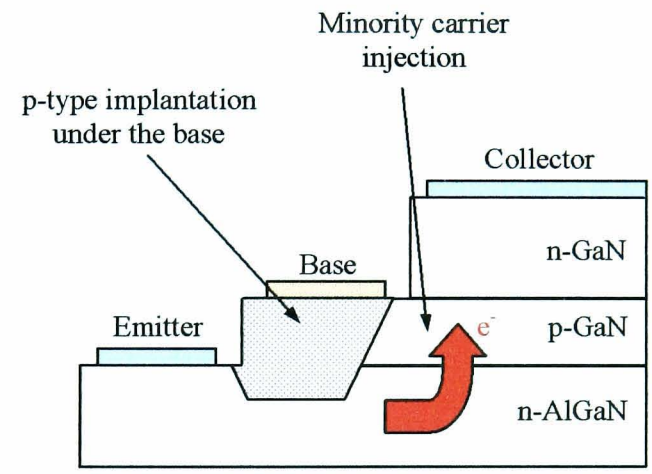


Figure 4.2 – Proposed structure for the inverted AlGaN/GaN HBT showing implantation under the base contacts which will channel injected current into the centre of the component.

Ion implantation in III-nitride semiconductors is still in its infancy, however reports in the literature have shown Si implantation into nominally undoped and p-type GaN to form n-type regions is relatively straightforward. Using this technique several working devices have already been demonstrated including a Junction Field Effect Transistor (JFET) [11] and n-p diodes [12]. P-type implantation into GaN has proven more difficult to realise. Simple Mg implantation followed by annealing does not result in p-type conduction. Pearton et al [13] observed p-type conduction using a co-

implantation of Mg and P. The role of the P was to increase vacancy concentration and promote substitutional Mg incorporation upon annealing. In order to activate the implanted species and remove ion-induced damage temperatures in excess of 1000°C are necessary. J. Keckes et al [14] showed radiation damage causes modification of stress within the material. By monitoring the stress in conjunction with in-plane lattice parameters it was possible to observe how annealing after ion implantation affected the crystal structure in GaN. From this data it was possible to extrapolate an optimum anneal temperature of approximately 1600°C which compares well to other estimates made in the literature [15][16].

For the HBT under development the implantation will be used to form a p-type region extending into the wide bandgap emitter. There have been very few reports in the literature of ion implantation into AlGaN structures. Polyakov et al [17] implanted Si and Mg/P into semi-insulating $Al_{0.12}Ga_{0.88}N$. Activation of the Si occurred only after annealing at 1140°C, however annealing of Mg/P resulted in highly resistive layers with no evidence of p-type conduction. This data suggests radiation induced damage in the AlGaN becomes increasingly stable due to the incorporation of aluminium. Consequently even higher temperatures are required to electrically activate the implanted species and remove damage in the crystal lattice. For the inverted HBT a localised highly insulating region in the AlGaN emitter underneath the base contacts will reduce parasitic injection of minority carriers similar to a p-type region. Consequently, providing p-type conduction in the base is maintained, excessive post-implant anneal temperatures (>1200°C) will not be required.

Implantation simulation packages such as TRIM can be used in order to determine the fluence and energy of ions required to penetrate the base of the HBT. Comparison of the simulated depth profiles to those obtained in the literature show reasonable agreement [18]. For the HBT layer structure defined in table 2.2 of chapter 2, a Mg^+ implantation energy of 100keV at a dose of $\approx 1\times10^{15}cm^2$ performed at an angle of 7° is required to form the localised p-type or highly insulating region.

Unfortunately, during the course of this work it was not possible to perform any implantation studies. Therefore, all the HBTs were produced with the implantation

stage omitted. As shown earlier, this will result in a significant reduction in the base transport factor. Despite this the benefits of using the inverted structure should still be observed and subsequent work will focus on implantation under the base contacts to produce more efficient transistors with high gains.

4.3 Growth of Inverted Geometry AlGaN/GaN HBT

Several attempts were made to grow the n-p-n structure without interruption. Initial trial runs resulted in poor quality epitaxial layers with significant surface roughness and large pits present across the film as shown in the scanning electron microscope (SEM) image of figure 4.3. These pits were approximately 500nm deep, 300nm in diameter and there were approximately $5\times10^{8}cm^{-2}$ on the collector surface. Cleaving through the structure also revealed voids within the epilayers. Wet etching of the sample, using the same conditions as outlined in section 3.5 of chapter 3, did not terminate on the base indicating insufficient p-type doping.

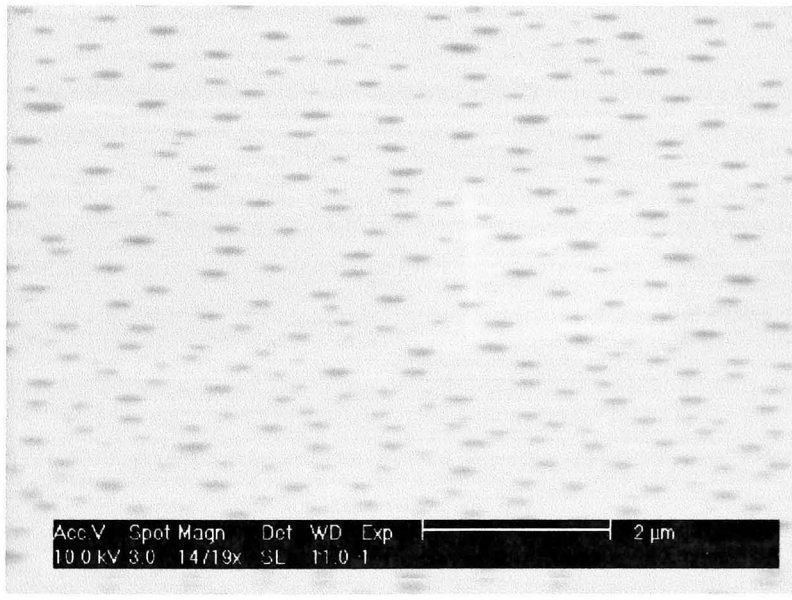


Figure 4.3 – Example of the collector surface of the inverted AlGaN/GaN HBT grown using the MOCVD technique without interruption.

It was not possible to perform secondary ion mass spectrometry (SIMS) on any of the HBT structures in order to determine carrier profiles and optimise growth as this facility is not available at Sheffield. Although other groups in the literature have demonstrated n-p-n structures without interruption between the base and upper emitter

layer [19]-[21] all the wafers produced at Sheffield were found to be of low quality. Therefore, initial trials on the HBT were performed with the collector layer re-grown. To achieve this, after deposition of the lower emitter-base heterojunction, the wafer was transferred into a second chamber via a load lock system and held under vacuum to minimise contamination on top of the base. The growth reactor was baked at high temperature in a H_2 atmosphere to purge any remaining Mg. Following this the wafer was re-loaded and, after deposition of a thin nucleation layer, the collector was grown. Despite having to use the re-growth technique it was still possible to prove the underlying concept of the inverted geometry. Furthermore, any contamination from the re-growth will be present at the less critical base-collector junction, resulting in improved emitter injection efficiency. Using re-growth to deposit the collector resulted in a significant improvement in material quality and wet etching could be used to selectively access the un-activated p-type base.

4.4 Characterisation of the AlGaN/GaN HBT

The layer structure (table 2.2) and fabrication steps for the AlGaN/GaN n-p-n HBTs grown using the collector-up geometry were outlined in chapter 2. The selectivity of the wet etch (demonstrated in chapter 3) was employed to access the 100nm thick p-type base. All devices were tested at room temperature in the common emitter configuration. For the inverted geometry, without any implantation under the base contacts, normal operation was not achieved for the majority of devices (figure 4.4). I-V characteristics for both emitter-base and collector-base junctions demonstrated ideality factors >2 (figures 4.5a and 4.5b respectively). Therefore, information regarding transport mechanisms and quality of the junctions could not be obtained. The resistivity of the p-type layer was measured using circular transmission line modelling (CTLM) and found to be $\approx 3\Omega$cm.

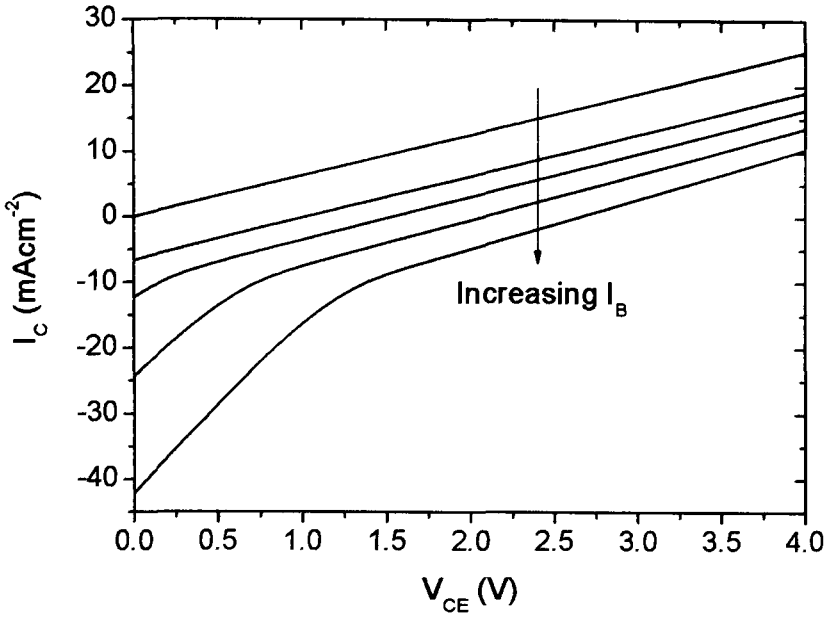


Figure 4.4 – Common emitter characteristics for the inverted geometry AlGaN/GaN HBT with base current (I_B) set to 0mA to 20mA in steps of 5mA.

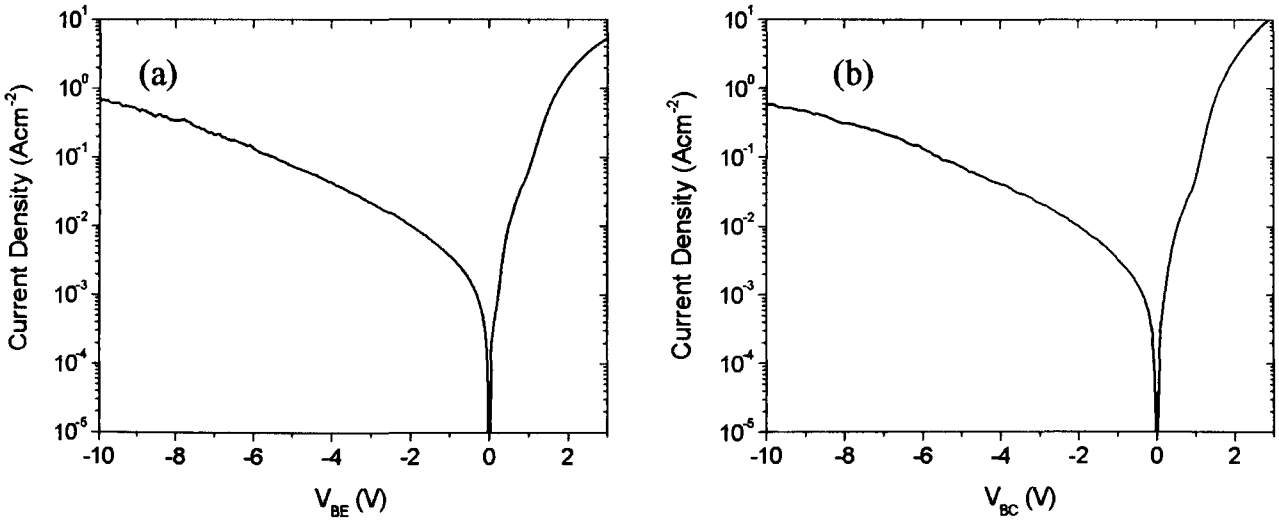


Figure 4.5 – Diode characteristics for the emitter-base (a) and base collector (b) junctions of the n-p-n AlGaN/GaN HBT.

The failure to obtain common-emitter characteristics can be explained by considering the large leakage currents in the base-collector junction (I_{CB0}) coupled with the series resistance of the p-type GaN. If the simple cross section of the HBT is considered

(figure 4.6a) with base current (I_B) set to 0mA there will be no minority carrier injection from the emitter. As the collector-emitter voltage (V_{CE}) is increased the resulting I-V curve is dominated by the reverse biased characteristic of the base-collector junction. If I_B is increased (I_B > 0mA) a lateral voltage drop is induced across the length of the base. A change in potential difference between the base and collector (ΔV_{BC}) in the intrinsic part of the device, as a result of an applied base current, will therefore decrease the leakage across the junction (figure 4.6b). Since minority carrier injection from the emitter underneath the collector is negligible, the reverse base-collector leakage current dominates and the total output current drops (ΔI_C). The origin of the excessive junction leakage is believed to be due to a large number of point defects within the material. These defects, which act as recombination centres, result in carrier generation within the junction depletion region when under reverse bias.

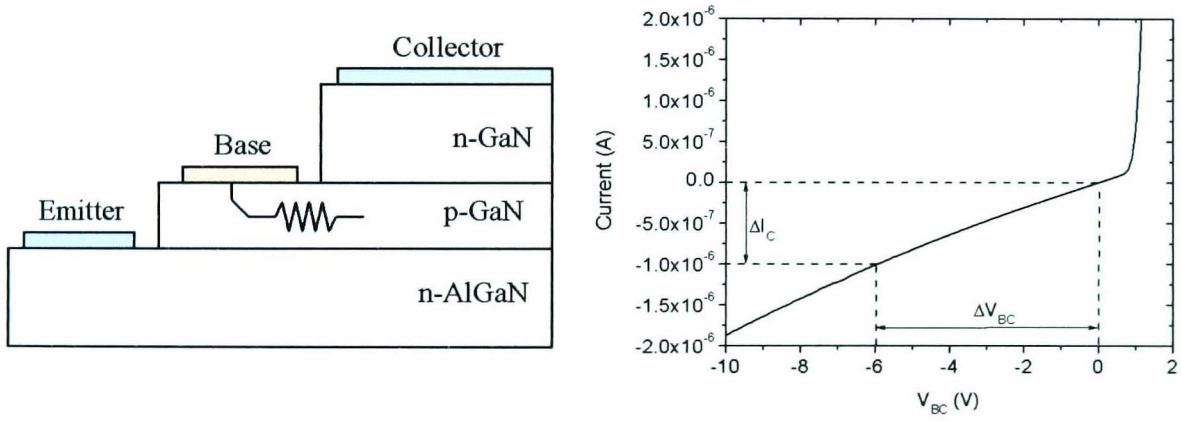


Figure 4.6a – Simple cross section of AlGaN/GaN HBT and (b) reverse leakage characteristic of the base-collector junction.

Despite the problems in obtaining common-emitter characteristics a working HBT was demonstrated (figure 4.7). This was a circular device with a collector radius of 25μm and a base radius of 78μm. This is the first AlGaN/GaN HBT in the UK and the first ever demonstration of the collector-up geometry. From the characteristic a gain of ≈0.13 was observed. This low value was expected due to the high base spreading resistance in conjunction with the difference in areas between the two p-n junctions which results in parasitic injection of electrons under the p-type contacts. Once the

implantation is performed a significant proportion of the injected minority carriers will be channelled into the active device region greatly increasing the base transport factor. Ignoring the lateral voltage drop across the base of the device gives a worst case estimate of ≈1.3 for the gain of a similar transistor with symmetrical junction areas. The value of 1.3 for the gain of a symmetrical device assumes the voltage drop across the base is negligible. The resistivity of the p-GaN material is very high which will lead to a significant voltage drop across the base and preferential injection of minority carriers under the contacts. Therefore the quoted value is expected to be significantly higher once these issues are accounted for.

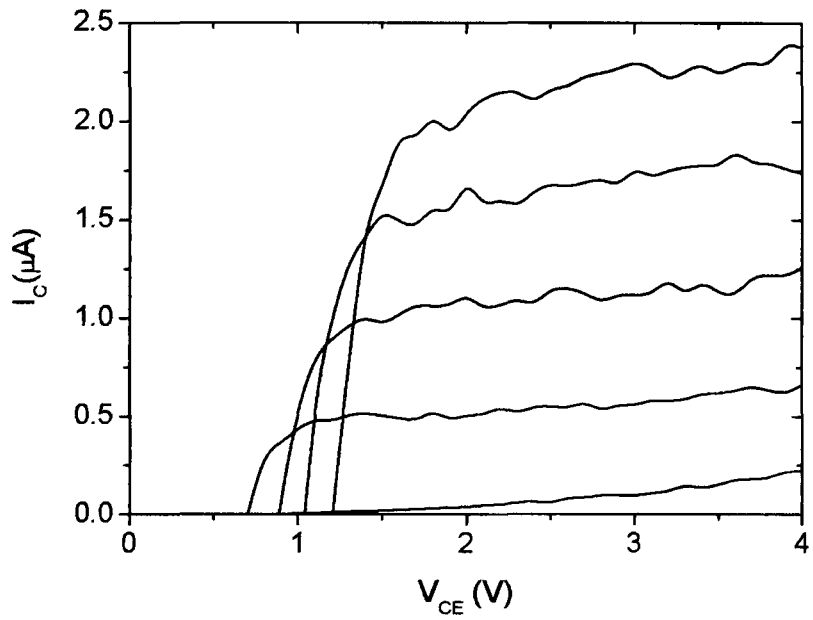


Figure 4.7 – Common emitter characteristic for working AlGaN/GaN HBT. The device was biased with I_B = 0 to 20μA in 5μA steps.

Operating the transistor in reverse with the collector acting as the emitter resulted in a gain of 0.05. Since the geometry of the device should result in an increase in gain when compared to the emitter-down approach it is therefore believed the quality of the re-grown interface is inferior to the lower junction deposited without interruption. Consequently, the upper junction has interfacial states between the collector and base which act as recombination centres as predicted earlier. This shows the advantages of

the inverted geometry over the standard emitter-up approach and the benefits of depositing the critical emitter-base heterojunction without pausing growth.

The common-emitter I-V characteristics show an offset voltage of ≈1 volt which is dependent on input base current. This offset voltage is undesirable in switching applications due to unnecessary power consumption. In standard AlGaN/GaN HBT structures which use an emitter-up geometry the offset voltage is related to a parasitic base-collector diode located underneath the p-type contacts [22]. Due to the high base spreading resistance this diode in the extrinsic part of the component can become forward biased at low voltage, resulting in a negative collector current. In the case of the inverted AlGaN/GaN HBT this parasitic element has been eliminated. Therefore the offset voltage is attributed to the difference in turn-on characteristics between the base-emitter and base-collector diodes [23]. This difference in the characteristics is related to the conduction band spike at the heterojunction interface and can be eliminated using a graded heterostructure or by making both junctions symmetrical by forming a double-HBT (DHBT).

Typically, for a geometrically symmetrical structure with near unity ideality factors the collector-emitter offset voltage (ΔV_{CE}) can be expressed using equation 4.1.

$$\Delta V_{CE} = \frac{kT}{q}\ln\left(\frac{J_{CS}}{\alpha_F J_{ES}}\right) + I_B R_E \qquad \text{Equation 4.1}$$

Where k is the Boltzmann constant, T is the temperature in Kelvin, q is the charge on an electron ($1.602\times10^{-19}C$) α_F is the forward common base current gain, R_E is the emitter resistance and J_{CS} and J_{ES} are the saturation current densities for thermionic currents appearing in the opposite contact from the base-emitter forward bias and collector-base forward bias respectively.

As can be seen from equation 4.1 the voltage dropped across the emitter resistance causes ΔV_{CE} to be dependant on base current. However, in the case of the inverted AlGaN/GaN HBT the emitter resistance can be assumed to be negligible and therefore it is proposed that the dependence of offset voltage on base current is related to the

high resistance of the p-type layer. As base current is increased the potential difference underneath the collector is raised and a correspondingly higher voltage is then required to place the base-collector diode under reverse bias resulting in the observed shift in ΔV_{CE}.

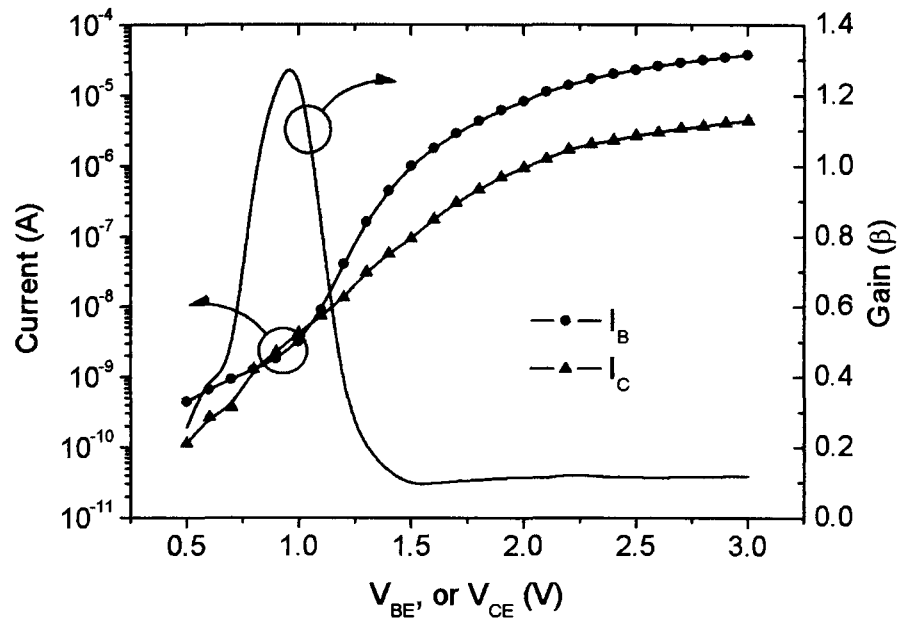


Figure 4.8 – Gummel plot for the working AlGaN/GaN HBT with collector-up geometry. An intrinsic current gain of 0.12 was demonstrated.

The Gummel plot for the working AlGaN/GaN HBT (figure 4.8) reveals a high gain of 1.28 at a low bias of 0.95 volts. As the bias is increased the gain drops and saturates at a value of ≈0.12. This high gain at low voltage is commonly observed in AlGaN/GaN HBTs [5][20][24] and can be explained by considering the high leakage currents in conjunction with the high series resistance of the base [25]. A simplified equivalent circuit for the above HBT with the base and collector junctions biased simultaneously is shown in figure 4.9. In this figure the p-type series and contact resistances are modelled as an extrinsic resistance (R_B), the collector and emitter resistances are assumed to be negligible and the base-collector leakage current is modelled as a variable resistor (R_{ICB0}) [25].

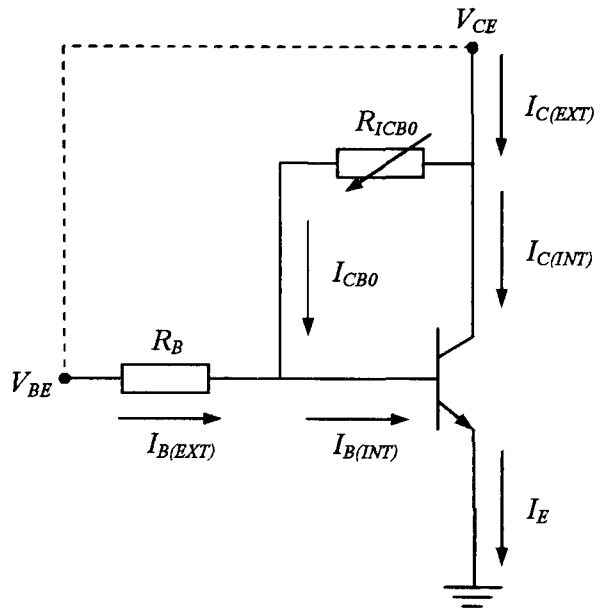


Figure 4.9 – Equivalent circuit for bipolar transistor with a high base contact resistance [25]. The extrinsic and intrinsic base and collector currents are defined as $I_{B(EXT)}$, $I_{B(INT)}$, $I_{C(EXT)}$ *and* $I_{C(INT)}$ *respectively.*

As the device is biased the extrinsic base current gives rise to a potential difference across R_B. Consequently the base-collector junction will become reverse biased producing a leakage current which will increase with increasing input current. Analysis of the equivalent circuit shown in figure 4.9 shows the extrinsically observed gain (β_{EXT}) is equal to equation 4.2.

$$\beta_{EXT} = \frac{I_{C(INT)} + I_{CB0}}{I_{B(INT)} - I_{CB0}} \qquad \text{Equation 4.2}$$

At low V_{CE} or V_{BE} where the induced base current is small, the leakage at the junction will cause $\beta_{(EXT)}$ to increase and reach a peak as $I_{B(INT)} - I_{CB0} \rightarrow 0$. As the voltage increases, more base current will flow and at high bias $I_{B(INT)} >> I_{CB0}$ and $\beta_{EXT} \rightarrow \beta_{INT}$. Therefore, the true gain of the HBT from the Gummel plot shown in figure 4.8 is 0.12 which compares well with the value extracted from the common emitter characteristic of 0.13.

Gummel plots for failed devices of identical dimensions reveal a similar intrinsic gain for the transistor of 0.12 (figure 4.10). However, while I_B is almost identical to the

previous characteristic for the working device, I_C shows a significant difference at low voltage, leading to a high peak in β_{EXT} which is more than 3 orders of magnitude greater than the intrinsic gain. This variation in I_C for the failed devices is attributed to a lower contact and/or base series resistance when compared to the working HBT. The increased p-type conduction in the failed HBT leads to a reduced voltage drop across the base. Consequently at low voltages the relative magnitude of I_{CB0} is increased and the peak in extrinsic gain is significantly greater. However, the intrinsic gain at higher voltage is almost identical. This decrease in p-type conduction for the device was confirmed when comparing I-V characteristics for the two diodes at high forward bias where the series and contact resistances of the base dominate. Although this explains the difference in Gummel plots a reasonable explanation as to why common emitter operation was obtained for the device shown in figures 4.7 and 4.8 compared to failed HBTs cannot be given. It is believed that despite the observed similarities for the emitter-base and base-collector diodes between the two devices there is an increase in junction quality for the working HBT which cannot be observed since it is masked in the I-V characteristic by the high contact and series resistance of the p-type layer. Therefore a localised fluctuation in material quality, which may have reduced the number of point defects in the neutral base or improved minority carrier injection, resulted in normal transistor action.

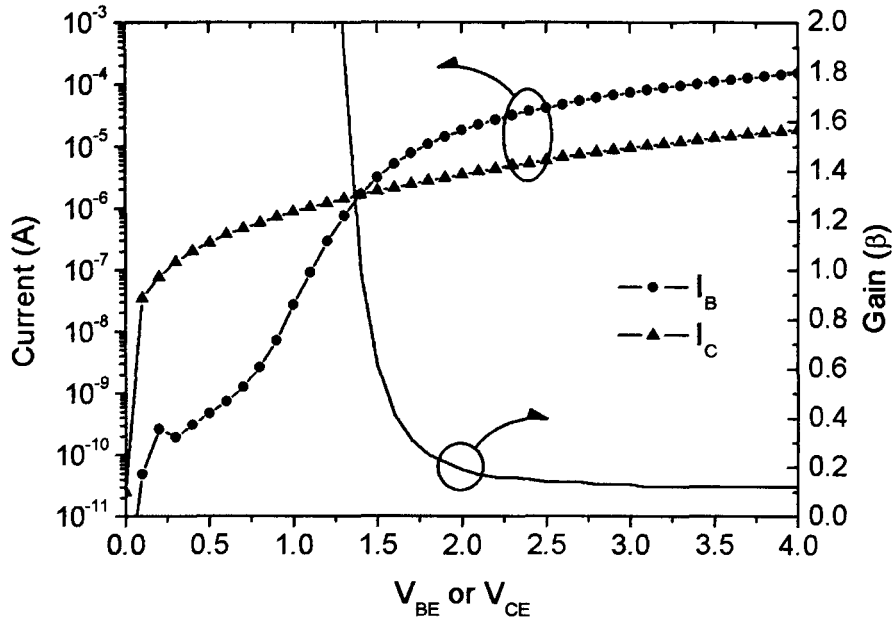


Figure 4.10 – A typical Gummel plot for a failed HBT with the same dimensions as that shown in figure 4.5

4.5 Schottky Collector HBT

To create a working HBT leakage from the base-collector region must be significantly reduced. To achieve this various other geometries based on the collector-up technique were considered. One of the most promising approaches found was to replace the collector with a Schottky diode. Adopting the collector-up structure ensures the quality of the emitter-base heterojunction is maintained due to elimination of the Mg memory effect. Furthermore, growth and device fabrication is considerably simplified since only a p-n junction is required and no etching is needed in order to access the p-type region. The device will still need an implantation step to prevent parasitic injection of electrons underneath the base contacts (figure 4.11).

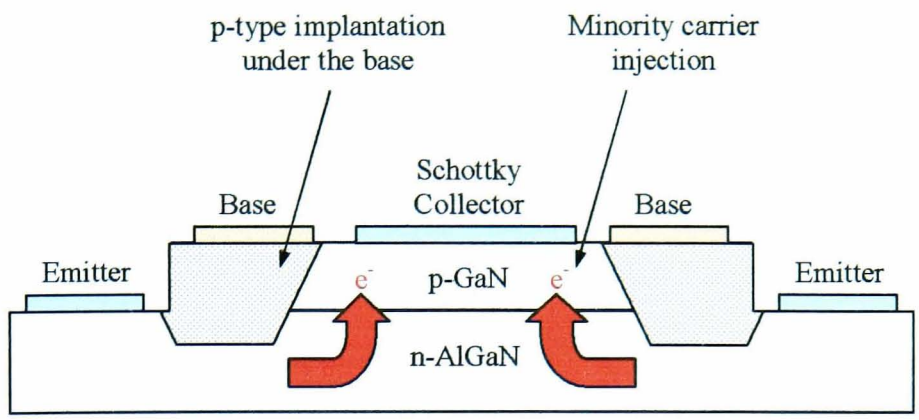


Figure 4.11 – Cross section showing proposed Schottky collector HBT geometry

Schottky collector HBTs have been demonstrated previously using other material systems incorporating a transferred substrate approach. Typically the cut off frequencies for HBT devices are considerably reduced when compared to HFETs. By employing a transferred substrate approach in conjunction with a Schottky collector, it becomes possible to significantly increase the frequency response for these components [26]. The transferred substrate method involves fabricating devices with narrow emitter and collector stripes aligned on opposite sides of the base epitaxial layer. By utilising a Schottky collector, the device dimensions can be scaled to deep sub micron lengths and collector series resistance is correspondingly eliminated. The base resistance and collector capacitance product becomes proportional to the process minimum feature size and f_{MAX} increases rapidly with scaling. The use of this technique in conjunction with GaAs- [27] and InP-based material systems [28] has yielded HBTs with $f_{MAX} > 400$ GHz, clearly demonstrating their potential for RF applications.

The following sections discuss both the fabrication and operation of p-type rectifying diodes and also the Schottky collector HBT. In these preliminary results no effort was made to scale the size of the collector to deep sub micron lengths and also no implantation under the base contacts was performed. Consequently, the gain for these initial transistors will be correspondingly low, similar to the n-p-n structures discussed in the previous sections. Future work will therefore concentrate on developing suitable implantation technologies to enable the fabrication of HBT devices with increased gain.

4.5.1 P-type Schottky Diodes

In order to investigate p-type Schottky diodes a bulk 2μm thick Mg-doped ($\approx 1\times10^{20}$ cm^{-3}) GaN film was grown on a sapphire substrate at the National Centre for III-V Technologies using the MOCVD technique. After deposition and annealing of Pt (10nm)/Au (150nm) ohmic contacts, Ti (30nm)/Au (150nm) or Al (30nm)/Au (150nm) metals were deposited onto the highly doped p-type GaN. The forward and reverse I-V characteristics for the two sets of diodes are shown in figure 4.12 and are compared to the base-collector junction for the n-p-n HBT. Both Schottky characteristics are almost symmetric and reverse leakage currents are ≈2-3 orders of magnitude higher than the conventional p-n junction. The Al/Au metallization scheme shows a lower leakage when compared to the Ti/Au due to the reduced work function of aluminium. Consequently, in all further experiments Al/Au was used as the rectifying contact.

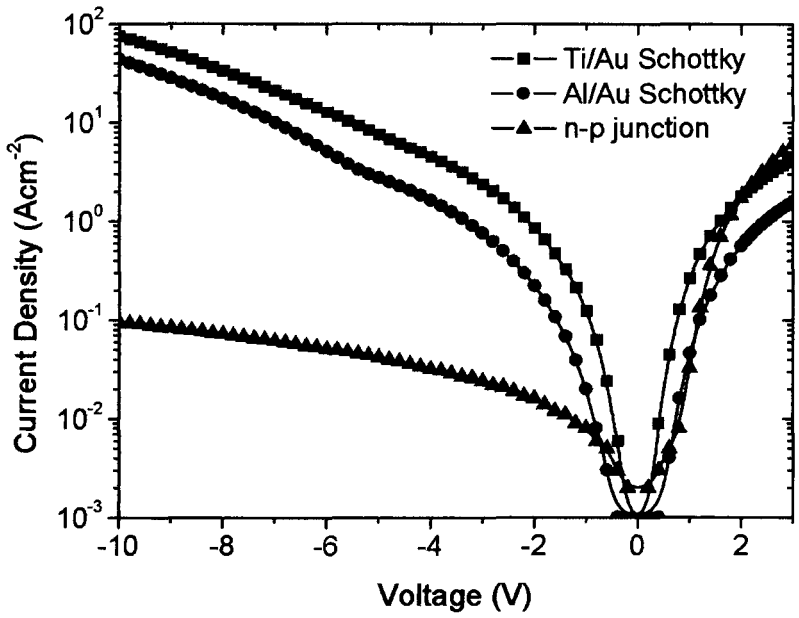


Figure 4.12 – I-V characteristics for Al/Au and Ti/Au Schottky contacts on p-GaN compared to a p-n junction diode.

Despite the relatively low free hole concentration at room temperature for p-GaN the width of the depletion layer below the rectifying contact is related to the concentration

of dopants which are capable of supplying a hole to the semiconductor lattice. The material used in this experiment is doped $\approx 1\times10^{20}cm^{-3}$ (the same as the base of the HBT) to maximise conductivity. Consequently, for both Schottky contacts there will be an extremely small depletion width leading to high leakage currents due to tunnelling (figure 4.13).

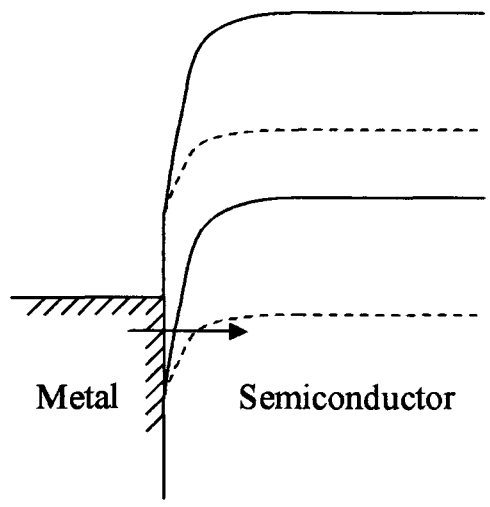


Figure 4.13 – Representation of tunnelling component (arrow) for a Schottky diode with a thin tunnelling region shown under equilibrium (dashed line) and under reverse bias (solid line).

There are few reports in the literature on p-GaN Schottky diodes, however plasma pre-treatments have been found effective in improving rectifying characteristics [29][30]. The plasma step introduces donor-like states into the bandgap in the form of nitrogen vacancies which compensate acceptors [31] resulting in a localised decrease in doping concentration at the surface. Introducing extremely high levels of surface damage has been found to result in a type conversion at the surface from p- to n-type material [29]. To investigate the plasma pre-treated Schottky contacts, diodes were fabricated in a similar manner to that described previously but a self aligning 1 minute Ar^+ ion plasma step was introduced prior to depositing the rectifying metals. This step was performed using the inductively coupled plasma (ICP) setup at an Ar flow rate of 20 standard cubic centimetres per minute (sccm), a pressure of 4 mTorr, an ICP power of 450W and an RF power of 50 W, 100 W or 150 W with BPRS100 photoresist used as a mask. Finally Al (100nm)/ Au (150nm) was deposited onto the damaged surface

using thermal evaporation. For all fabricated diodes no etching of the p-GaN surface was observed under any of the pre-treatment conditions.

Diodes fabricated using different RF powers exhibited almost identical I-V characteristics. A Schottky rectifier formed using a 50W Ar^+ pre-treatment is shown in figure 4.14 and is compared to the base collector junction of a working HBT. For the plasma pre-treated devices the quality of the rectifying contact has been significantly improved. The reverse bias leakage current has been reduced by ≈2-3 orders of magnitude when compared to the n-p junction of the HBT. At low forward bias (>2-2.5 volts) the ideality factor was ≈2. At higher voltages this value increased and became >2 due to the high resistance of the base dominating over junction resistance. The increase in diode quality compared to un-treated rectifiers is due to the localised reduction in p-type conductivity underneath the Al contact which increases the barrier width and prevents tunnelling. The breakdown voltage for the diodes was found to be ≈20 volts and was independent of RF power. Analysis of circular devices showed leakage to have a linear dependence on radius indicating injection at the periphery of the rectifying contact (figure 4.15).

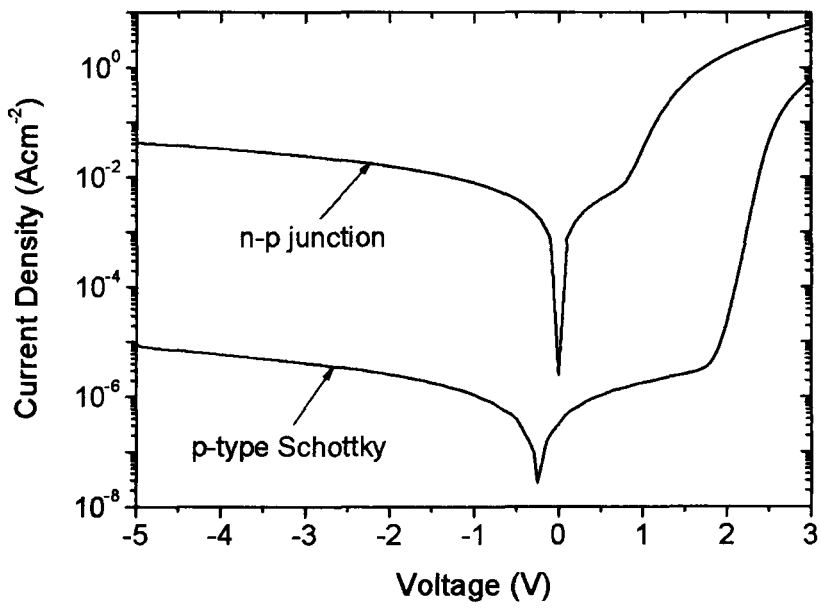


Figure 4.14 – I-V characteristics for p-type Schottky diodes fabricated using a 50W Ar^+ ion plasma step before deposition of an Al/Au rectifying contact.

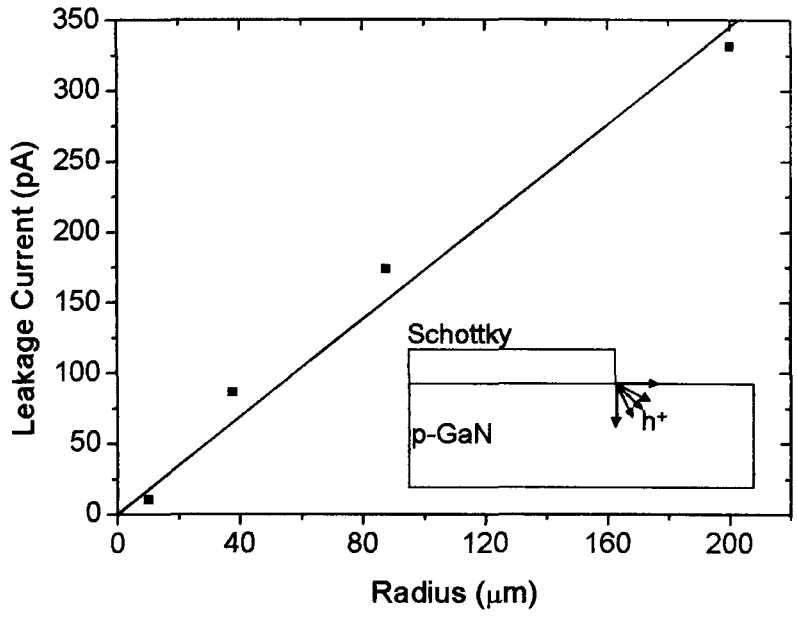


Figure 4.15 – Reverse leakage currents for p-type GaN Schottky diodes with varying radius formed using a 50W Ar^+ plasma step. The inset shows the likely injection at the edge of the rectifying contact.

Capacitance-Voltage (C-V) profiling can be used to determine carrier concentrations, built-in voltages and depletion depths for bulk and p-n junction semiconductors. Figure 4.16 shows the acceptor profiles for Ar^+ pre-treated diodes determined using the C-V technique. A 10 kHz measurement frequency was used to ensure accurate measurement of all activated carriers. As can be seen from figure 4.16, the Ar^+ ion step has been successful in reducing acceptor concentrations close to the surface, which extends the depletion depth and reduces tunnelling current to negligible levels. Increasing the ion energy results in the Ar penetrating further into the semiconductor increasing the barrier width. The acceptor concentration was found to be exponentially dependent on distance from the surface. For the case of the inverted AlGaN/GaN HBT this could be used to create a quasi-electric field across the base region. This will result in a decrease in minority carrier transit time across the p-GaN layer. The resulting field, estimated from figure 4.16, would be equal to $15kVcm^{-1}$, $13kVcm^{-1}$ and $10kVcm^{-1}$ for pre-treatments of 50, 100 and 150W respectively.

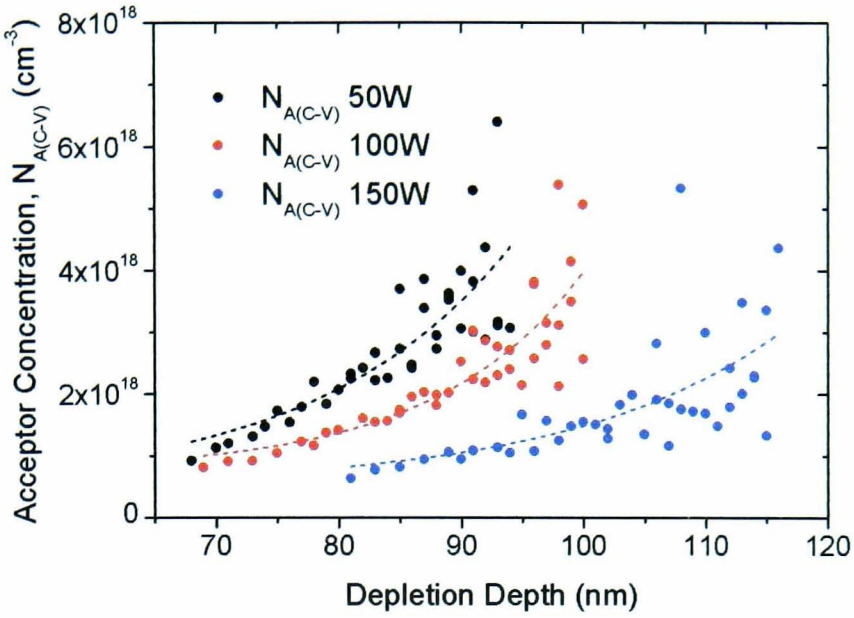


Figure 4.16 – Acceptor concentrations measured for the plasma treated p-type Al/Au Schottky diodes using the C-V technique at a measurement frequency of 10 kHz.

Since the effective doping concentration is changing at the surface, C-V cannot be used to determine the barrier height of the rectifying Al/Au contact and consequently an Arrhenius plot must be employed [32]. Figure 4.17 shows the Richardson plots for diodes fabricated with a 50W Ar^+ pre-treatment. From these results the barrier height and the Richardson constant for the plasma pre-treated Schottky diode was measured as 1.6eV and 1.4$Acm^{-2}K^{-2}$ respectively. This value of barrier height is close to the 1.4eV measured for Ti rectifying contacts on lightly doped p-type material [33]. This is the first measurement for the barrier height and Richardson constant for Al rectifiers deposited on p-GaN.

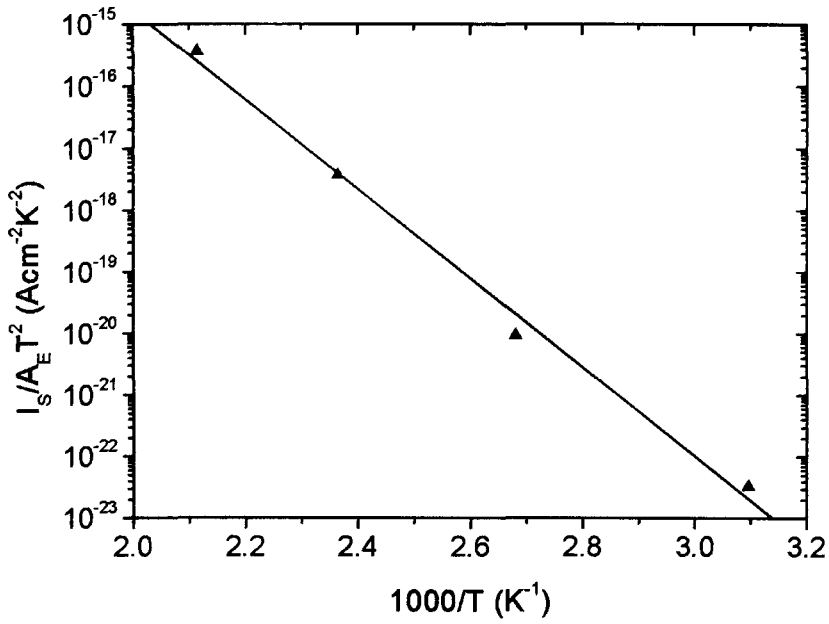


Figure 4.17 – Arrhenius plot for p-type Schottky diodes used to determine barrier height and Richardson constant independently.

4.5.2 Characterising the Schottky Collector HBT

Using the results obtained in the previous section for p-type Schottky diodes it was possible to specify a layer structure using the emitter-down geometry but replacing the 700nm thick n-type collector with a rectifying contact (table 2.3 of chapter 2). The Schottky collector was formed using an Ar^+ plasma pre-treatment step at a RF power of 50W. The areas of the collector-base and emitter-base junctions were 20×50μm and 48×66μm respectively. For all devices with a base thickness of 100nm, 160nm and 250nm, common emitter characteristics were obtained (figure 4.18a, b and c). Gummel plots (figure 4.18d, e and f) were used to verify the intrinsic gain of the HBTs and were found to be approximately 2×10^{-3}, 2×10^{-5} and 1×10^{-5} for a base thickness of 100nm, 160nm and 250nm respectively. Despite the low gain this is the first example of AlGaN/GaN HBTs using a rectifying contact as the collector junction and, for the 100nm device, the first device to employ a graded base to aid minority carrier transport.

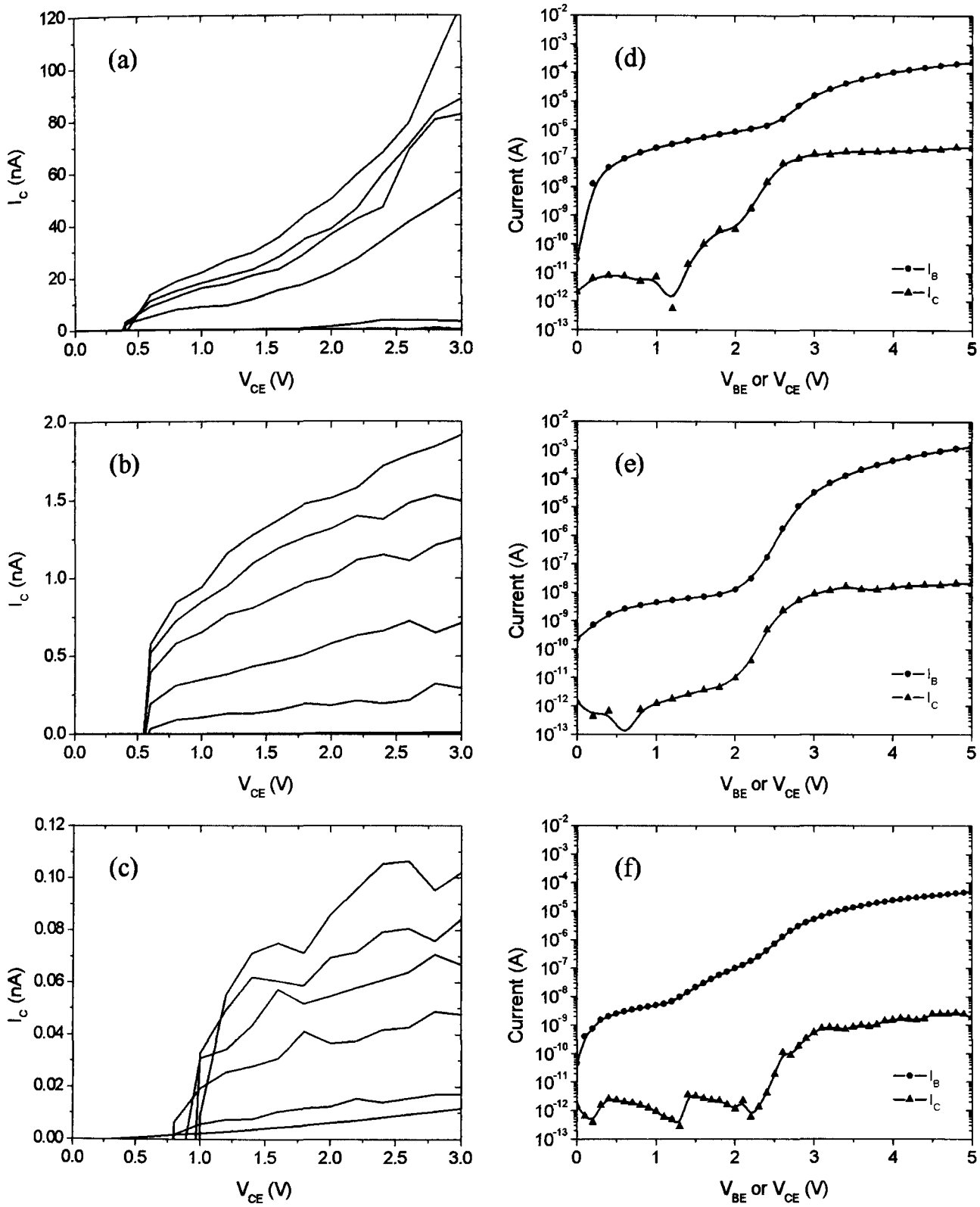


Figure 4.18 – Common emitter plots for Ar^+ pre-treated Schottky-collector HBTs with (a) 100nm, (b) 160nm and (c) 250nm thick p-type base regions. Gummel plots for Ar^+ pre-treated Schottky-collector HBT with (d) 100nm, (e) 160nm and (f) 250nm thick p-type base regions.

The offset voltage for the Schottky collector HBTs was found to be ≈0.5 volts with the thickest base showing a base current dependence on offset voltage. The base resitivity was found to be 3, 6 and 12Ωcm for a base thickness of 100, 160 and 250nm respectively. Therefore the input current dependence on offset voltage for the thickest base is believed to be related to an increased base spreading resistance. This results in an increased voltage underneath the collector for a given base current which consequently requires a larger base-collector bias in order to reverse bias the junction. The reason for the decrease in base conductivity for increasing base thickness is unclear but may be related to a shift in the optimum post-growth activation anneal of acceptors.

The Schottky collector HBTs suffered from several major problems which limited their operation. Firstly the output conductance was very high resulting in a low Early voltage. This is attributed to the reduction in majority hole concentration across the p-GaN leading to an increase in base width modulation. The severity of this effect is most prominent in the 100nm base HBT. For these devices the ion damage has penetrated the majority of the p-type region forming a punch through effect. This was confirmed from both C-V measurements and the I-V characteristic for the emitter-base diode which showed extremely high leakage under reverse bias. Apart from this junction both the Schottky collector and emitter-base diodes exhibited ideality factors of ≈2 (Figure 4.19a and b). The high ideality factor for the p-n junction indicates that under normal common emitter operation minority carriers are recombining at the interface and therefore do not transit the base. These carriers will be unable to reach the collector and therefore contribute to the low gain observed for all three transistor structures.

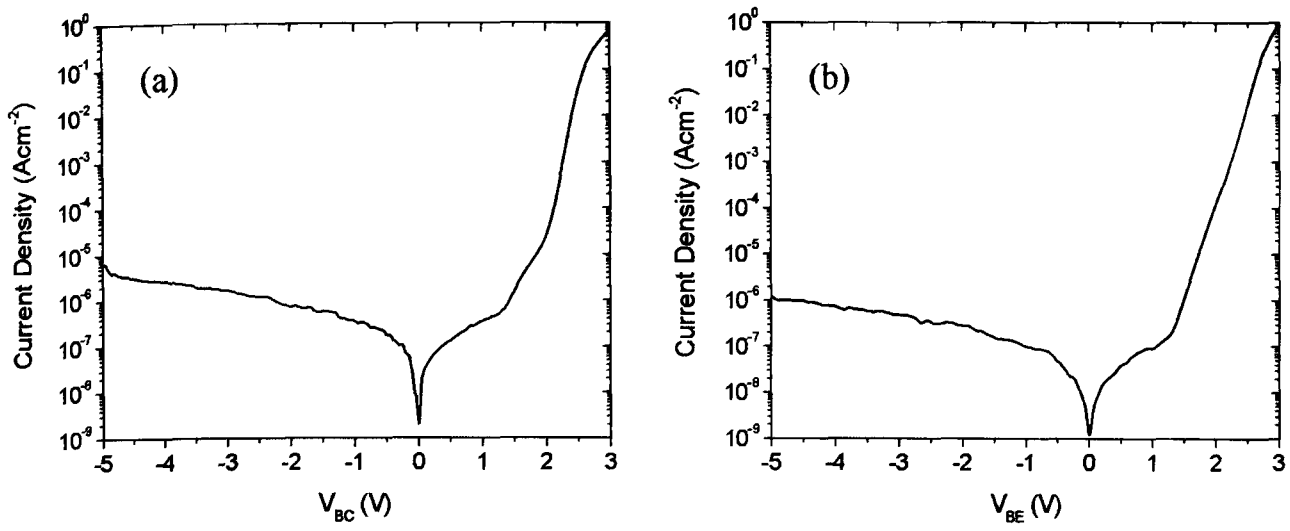


Figure 4.19 – (a) emitter-base and (b) Schottky collector I-V characteristics for the 160nm base AlGaN/GaN HBT.

A comparison of the intrinsic gain for pre-treated and non-pre-treated Schottky collector HBTs is shown in figure 4.20 for various base thicknesses. For HBTs fabricated without the plasma pre-treatment, common emitter operation was not achieved and I-V characteristics were similar to that shown in figure 4.4. This was attributed to the poor quality of the collector-base rectifying diode coupled with the high resistance of the p-GaN. It is interesting to note the gain for the 100nm base width device (0.08) is similar to the n-p-n HBTs demonstrated in section 4.6. The gain of Ar^+ pre-treated structures was observed to be very low and for both the 100nm and 160nm devices the gain was reduced when compared to the non-pre-treated HBTs. This is due to the introduction of shallow donor states into the bandgap which reduces the conductivity of the p-type base layer underneath the Schottky contact. As the resistivity under the collector is increased the corresponding voltage drop across the length of the p-type region will also increase. Consequently there is a reduction in minority carrier injection under the collector and a decrease in gain. For the 250nm thick base HBT the ion damage only penetrates ≈100nm. Consequently the conductivity under the collector is not significantly compromised and the gain is increased compared to the un-pre-treated device. For the non-pre-treated transistors there is an exponential dependence of gain on base thickness. This is related to the diffusion length of minority carrier electrons in the p-doped region. For the 250nm

thick device the majority of injected electrons will recombine with holes in the base since the width of the p-type region is approximately the same as the diffusion length (≈300nm). As the width of the base is reduced more electrons will reach the collector and the gain will increase. From the data shown in figure 4.20 it can be seen that for the non-pre-treated HBTs a base width of ≤50nm is required to give a gain ≥1. To improve gain for pre-treated devices the depth of compensation for the p-type layer prior to deposition of the collector must be reduced. To achieve this RF power for the Ar^+ plasma step must be correspondingly decreased.

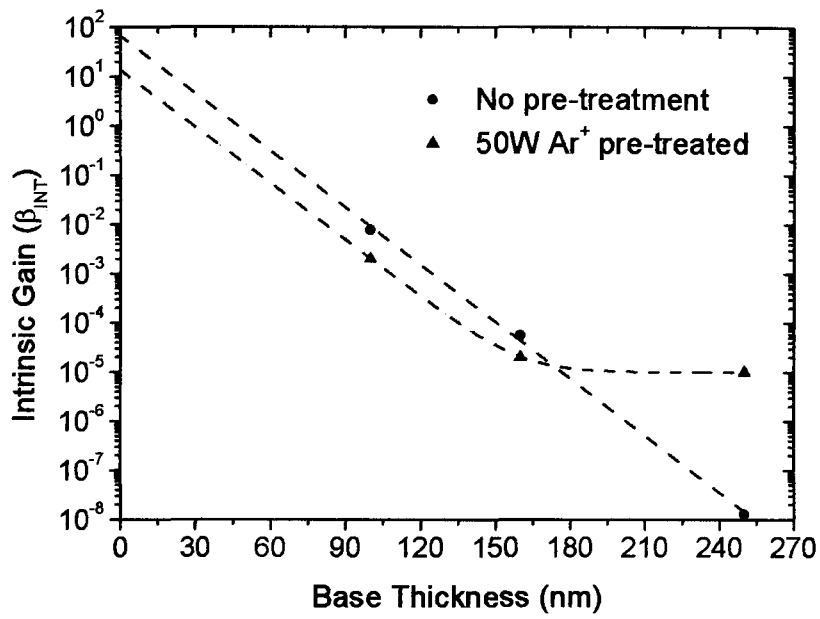


Figure 4.20 – Intrinsic gains extracted from Gummel plots for non pre-treated and pre-treated Schottky collector AlGaN/GaN HBTs.

The high emitter-collector leakage currents in AlGaN/GaN n-p-n HBTs increases noise in the component and limits common emitter operation. Emitter-collector leakage for the Schottky HBTs is presented in figure 4.21 and is compared to the previously fabricated n-p-n devices. It can be seen that as the base thickness is reduced the leakage current correspondingly decreases. Whilst the decrease in leakage between the 160nm and 250nm thick p-type layers is marginal, the emitter-collector currents for the 100nm base are relatively high. This is due to the plasma induced donor states extending across the length of the base, causing a punch through effect.

Reducing the Ar^+ plasma RF power to 5-10W will decrease the ion penetration depth to ≈50nm. It is predicted using these low powers to form the Schottky contact will reduce emitter-collector leakage to values close to those obtained on thicker p-GaN layers. Despite this the 100nm thick Schottky collector HBT shows reduced leakage when compared to the standard n-p-n devices. For HBTs with thicker base layers the leakage current has been reduced by ≈5 orders of magnitude when compared to n-p-n HBTs. These leakage currents are similar to those obtained for HBTs fabricated on dislocation free material [34] clearly demonstrating the advantages of the Schottky collector geometry.

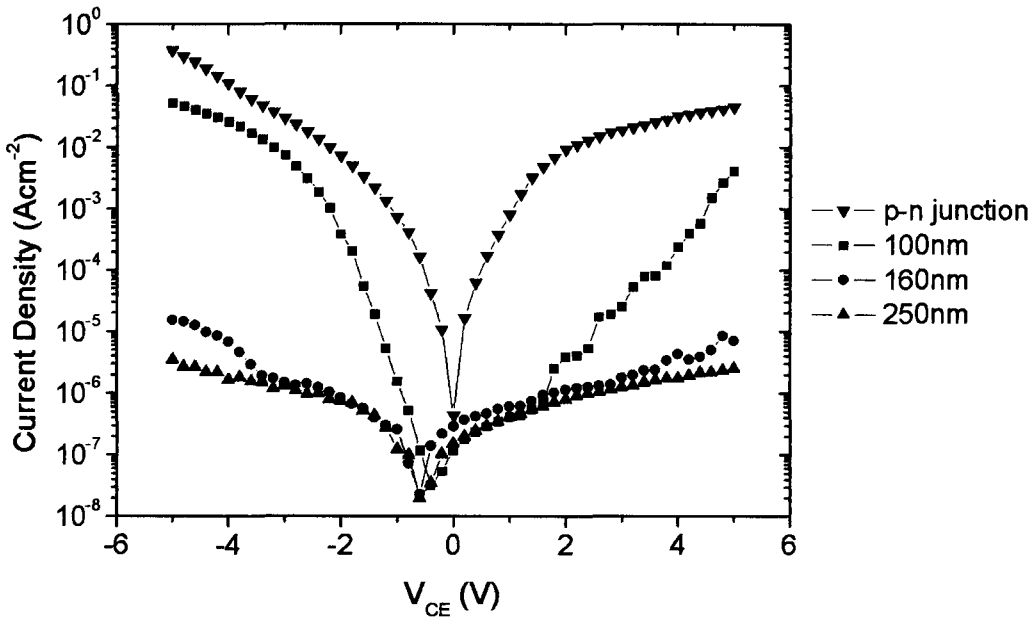


Figure 4.21 – Emitter-collector leakage currents for plasma pre-treated AlGaN/GaN Schottky collector HBTs compared to emitter-collector leakage in the p-n junction.

4.6 Conclusions

A new n-p-n AlGaN/GaN HBT geometry based on a collector-up approach has been presented. This structure will improve the quality of the critical emitter-base heterojunction improving the gain of the transistor. Furthermore, the Mg memory effect will be transferred to the less critical base-collector homojunction, potentially eliminating the need for two separate growth stages. However, for initial fabrication

trials the collector was deposited using a re-growth technique to achieve material of suitably high quality. Obtaining common emitter characteristics for initial devices using the n-p-n structure was found to be problematic. This was directly attributed to leakage currents at the collector-base diode in conjunction with the large base spreading resistance. Despite these difficulties a working device was demonstrated with a common emitter current gain of ≈0.13. This low gain was due to the lack of an appropriate implantation under the p-type contacts which lead to preferential injection away from the collector. After implantation to form a device with symmetrical junction areas it has been estimated the gain should increase to values >1. This is the first n-p-n AlGaN/GaN HBT grown and fabricated in the UK and the first ever demonstration of the collector-up geometry.

To reduce leakage in the structure the collector of the inverted HBT was replaced with a Schottky rectifier. This greatly simplified growth since only a single p-n junction was required. To improve the quality of the Schottky diode an Ar^+ plasma pre-treatment was employed. Introducing this processing step reduced reverse bias leakage currents by ≈3 orders of magnitude when compared to the base-collector p-n junction. The barrier height and Richardson constant for Al rectifiers on p-GaN was found to be 1.6eV and 1.4$Acm^{-2}K^{-2}$ respectively. Using the Ar^+ plasma step before deposition of the collector resulted in the demonstration of common emitter characteristics. For HBTs with base thicknesses of 100nm, 160nm and 250nm the intrinsic gains of the devices were found to be 2×10^{-3}, 2×10^{-5} and 1×10^{-5} respectively. Unfortunately gains for the transistors with base thicknesses of 100nm and 160nm were not improved compared to non pre-treated devices due to the reduction in conductivity under the collector contact which reduced minority carrier injection. Furthermore, emitter-base diode characteristics demonstrated an ideality factor of ≈2 indicating minority carriers were recombining at the junction interface resulting in a reduced gain. For the 100nm thick base HBT the Ar plasma treatment penetrated the width of the base, greatly increasing emitter-collector leakage. For transistors using a 160nm and 250nm base the emitter-collector leakage current was reduced by ≈5 orders of magnitude, similar to HBTs grown on dislocation free material. This is the first demonstration of an AlGaN/GaN HBT using a rectifying contact as the collector. It is predicted that using a lower RF plasma power before deposition of the Schottky contact will greatly improve the characteristics for transistors with thinner base layers.

4.7 References

[1] *Y. L. Chang, M. Ludowise, D. Lefforge, B. Perez "Study of Mg diffusion during metalorganic chemical vapour deposition of GaN and AlGaN" Applied Physics Letters, Vol. 74, No. 5, pp 688-690, 1999*

[2] *J. Han, A. G. Baca, R. J. Shul, C. G. Willison, L. Zhang "Growth and fabrication of GaN/AlGaN heterojunction bipolar transistor" Applied Physics Letters, Vol. 74, No. 18, pp 2702-2704, 1999*

[3] *F. Ren, J. Han, R. Hickman, J. M. Van Hove, P. P. Chow, J. J. Klaassen, J. R. LaRoche, K. B. Jung, H. Cho, X. A. Cao, S. M. Donovan, R. F. Kopf, R. G. Wilson, A. G. Baca, R. J. Shul, L. Zhang, C. G. Willison, C. R. Abernathy, S. J. Pearton "GaN/AlGaN HBT fabrication" Solid-State Electronics, Vol. 44, No. 2, pp 239-244, 2000*

[4] *L. McCarthy, I. Smorchkova, H. Xing, P. Kozodoy, P. Fini, J. Limb, D. Pulfrey, J. Speck, M. J. W. Rodwell, S. P. DenBaars, U. K. Mishra "GaN HBT: Towards an RF device" IEEE Transactions on Electron Devices, Vol. 48, No. 3, pp 543-551, 2001*

[5] *D. J. H. Lambert, J. J. Huang, B. S. Shelton, M. M. Wong, U. Chowdhury, T. G. Zhu, H. K. Kwon, Z. Liliental-Weber, M. Benarama, M. Feng, R. D. Dupuis "The growth of AlGaN/GaN heterojunction bipolar transistors by metalorganic chemical vapour deposition" Journal of Crystal Growth, Vol. 221, pp 730-733, 2000*

[6] *J. B. Limb, L. McCarthy, P. Kozodoy, H. Xing, J. Ibbetson, Y. Smorchkova, S. P. DenBaars, U. K. Mishra "AlGaN/GaN HBTs using a regrown emitter" Electronics Letters, Vol. 35, No. 19, pp 1671-1673, 1999*

[7] *J. B. Limb, H. Xing, B. Moran, L. McCarthy, S. P. DenBaars, U. K. Mishra "High voltage operation (>80V) of GaN bipolar junction transistors with low leakage" Applied Physics Letters, Vol. 76, No. 17, pp 2457-2459, 2000*

[8] *K. P. Lee, A. P. Zhang, G. Dang, F. Ren, J. Han, S. N. G. Chu, W. S. Hobson, J. Lopata, C. R. Abernathy, S. J. Pearton, J. W. Lee "Self-aligned process for emitter- and base-regrowth GaN HBTs and BJTs" Solid-State Electronics, Vol. 45, No. 2, pp 243-247, 2001*

[9] *H. Xing, P. M. Chavarkar, S. Keller, S. P. DenBaars, U. K. Mishra "Very High Voltage Operation (>330V) With High Current Gain of AlGaN/GaN HBTs" IEEE Electron Device Letters, Vol. 24, No. 3, pp 141-143, 2003*

[10] *H. Xing, D.S. Green, H. Yu, T. Mates, P. Kozodoy, S. Keller, S.P. Denbaars, U.K. Mishra "Memory effect and redistribution of Mg into sequentially regrown GaN layer by metalorganic chemical vapour deposition" Japanese Journal of Applied Physics, Vol. 42, No. 1, pp 50-53, 2003*

[11] *X. A. Cao, J. R. LaRoche, F. Ren, S. J. Pearton, J. R. Lothian, R. K. Singh, R. G. Wilson, H. J. Guo, S. J. Pennycook "Implanted p-n Junctions in GaN" Solid-State Electronics, Vol. 43, No. 7, pp 1235-1238, 1999*

[12] *J. C. Zolper, R. G. Wilson, S. J. Pearton, R. A. Stall "Ion-Implanted GaN Junction Field Effect Transistor" Applied Physics Letters, Vol. 68, No. 16, pp 2273-2274, 1996*

[13] *S. J. Pearton, C. B. Vartuli, J. C. Zolper, C. Yuan, R. A. Stall "Ion Implantation Doping and Isolation of GaN" Applied Physics Letters, Vol. 67, No. 10, pp 1435-1437, 1995*

[14] *J. Keckes, A. Wenzel, J. W. Gerlach, B. Rauschenbach "Annealing of the Radiation Damage in Mg-Implanted GaN thin films: Temperature development of Lattice Parameters and Stresses" Nuclear Instruments and Methods in Physics Research B, Vol. 211, No. 4, pp 519-523, 2003*

[15] *C. Liu, A. Wenzel, J.W. Gerlach, X.F. Fan, B. Rauschenbach "Annealing Study of Ion Implanted GaN" Surface and Coatings Technology, Vol. 128-129, pp 455-460, 2000*

[16] *J. C. Zolper "Ion Implantation in Group III-Nitride Semiconductors: A Tool for Doping and Defect Studies" Journal of Crystal Growth, Vol. 178, pp 157-167, 1997*

[17] *A. Y. Polyakov, M. Shin, M. Skowronski, R. G. Wilson, D. W. Greve, S. J. Pearton "Ion Implantation of Si, Mg and C into $Al_{0.12}Ga_{0.88}N$" Solid State Electronics, Vol. 41, No. 5, pp 703-706, 1997*

[18] *R.G. Wilson, C.B. Vartuli, C.R. Abernathy, S.J. Pearton, J.M. Zavada "Implantation and redistribution of dopants and isolation species in GaN and related compounds" Solid-State Electronics, Vol. 38, No. 7, pp 1329-1333, 1995*

[19] L.S. McCarthy, P. Zozodoy, M.J.W. Rodwell, S.P. DenBaars, U.K. Mishra "AlGaN/GaN Heterojunction Bipolar Transistor" IEEE Electron Device Letters, Vol. 20, No. 6, pp 277-279, 1999

[20] J.J. Huang, M. Hattendorf, M. Feng, D.J.H. Lambert, B.S. Shelton, M.W. Wong, U. Chowdhury, T.G. Zhu, H.K. Kwon, R.D. Dupuis "Graded-emitter AlGaN/GaN heterojunction bipolar transistors" Electronics Letters, Vol. 36, No. 14, pp 1239-1241, 2000

[21] J.J. Huang, M. Hattendorf, M. Feng, D.J.H. Lambert, B.S. Shelton, M.M. Wong, U. Chowdhury, T.G. Zhu, H.K. Kwon, R.D. Dupuis "Temperature dependent common emitter current gain and collector-emitter offset voltage study in AlGaN/GaN heterojunction bipolar transistors" IEEE Electron Device Letters, Vol. 22, No. 4, pp 157-159, 2001

[22] L.S. McCarthy, I.P. Smorchkova, H. Xing, P. Kozodoy, P. Fini, J. Limb, D.L. Pulfrey, J.S. Speck, M.J.W. Rodwell, S.P. DenBaars, U.K. Mishra "GaN HBT: Towards an RF device" IEEE Transactions on Electron Devices, Vol. 48, No. 3, pp 543-551, 2001

[23] S.C. Lee, J.N. Kau, H.H. Lin "Origin of high offset voltage in an AlGaAs/GaAs heterojunction bipolar transistor" Applied Physics Letters, Vol. 45, No. 10, pp 1114-1116, 1984

[24] H. Xing, P.M. Chavarkar, S. Keller, S.P. DenBaars, U.K. Mishra "Very high voltage operation (>330 V) with high current gain of AlGaN/GaN HBTs" IEEE Electron Device Letters, Vol. 24, No. 3, pp 141-143, 2003

[25] H. Xing, D. Jena, M.J.W. Rodwell, U.K. Mishra "Explanation of anomalously high current gain observed in GaN based bipolar transistors" IEEE Electron Device Letters, Vol. 24, No. 1, pp 4-6, 2003

[26] U. Bhattacharya, M.J. Mondry, G. Hurtz, I.H. Tan, R. Pullela, M. Reddy, J. Guthrine, M.J.W. Rodwell, J.E Bowers "Transferred substrate Schottky-collector HBTs: First results and scaling laws for high f_{max}" IEEE Electron Device Letters, Vol. 16, No. 8, pp 357-359, 1995

[27] Q. Lee, B. Agarwal, D. Mensa, R. Pullela, J. Guthrie, L. Samoska, M.J.W. Rodwell "A > 400 GHz f_{max} transferred-substrate heterojunction bipolar transistor IC technology" IEEE Electron Device Letters, Vol. 19, No. 3, pp 77-79, 1998

[28] *S. Lee, H.J. Kim, M. Urteaga, S. Krishnan, Y. Wei, M. Dahlström M. Rodwell "Transferred-substrate InP/InGaAs/InP double heterojunction bipolar transistors with f_{max} = 425 GHz" Electronics Letters, Vol. 37, No. 17, pp 1096-1098, 2001*

[29] *X.A. Cao, S.J. Pearton, A.P. Zhang, G.T. Dang, F. Ren, R.J. Shul, L. Zhang, R. Hickman, J.M. Van Hove "Electrical effects of plasma damage in p-GaN" Applied Physics Letters, Vol. 75, No. 17, pp 2569-2571, 1999*

[30] *D.G. Kent, K.P. Lee, A.P. Zhang, B. Luo, M.E. Overberg, C.R. Abernathy, F. Ren, K.D. Mackenzie, S.J. Pearton, Y. Nakagawa "Electrical effects of N_2 plasma exposure on dry-etch damage in p- and n-GaN Schottky diodes" Solid-State Electronics, Vol. 45, No. 10, pp 1837-1842, 2001*

[31] *D.C. Look, G. C. Farlow, P. J. Drevinsky, D. F. Bliss, J.R. Sizelove "On the nitrogen vacancy in GaN" Applied Physics Letters, Vol. 83, No. 17, pp 3525-3527, 2003*

[32] *L.S. Yu, Q.Z. Liu, Q.J. Xing, D.J. Qiao, S.S. Lau, J. Redwing "The role of the tunnelling component in the current-voltage characteristics of metal-GaN Schottky diodes" Journal of Applied Physics, Vol. 84, No. 4, pp 2099-2104*

[33] *J.W. Kim, J.W. Lee "Ti/Al p-GaN Schottky barrier height determined by C-V measurements" Applied Surface Science, Vol. 250, pp 247-251, 2005*

[34] *L. McCarthy, I. Smorchkova, H. Xing, P. Fini, S. Keller, J. Speck, S.P. DenBaars, M.J.W. Rodwell, U.K. Mishra "Effect of threading dislocations on AlGaN/GaN heterojunction bipolar transistors" Applied Physics Letters, Vol. 78, No. 15, pp 2235-2237, 2001*

5 Passivation of AlGaN/GaN Heterostructure Field Effect Transistors

5.1 Introduction

Devices such as $Al_xGa_{1-x}N$/GaN heterostructure field effect transistors (HFETs) with impressive power densities continue to be reported [1][2]. However, these devices suffer from an undesirable reduction in output current in conjunction with an increase in knee voltage when operated at microwave frequencies which significantly reduces the theoretically predicted maximum output power. This phenomenon is referred to as current slump and is attributed to deep level traps located both within the structure and on the AlGaN barrier surface [3]. Passivating the HFET surface, usually with SiN, has been found effective in reducing this effect [4], however consistency between samples remains a problem.

In this chapter a novel test structure is employed to analyse both bulk and surface leakage components in AlGaN/GaN devices. Using this same test structure, bulk and surface related traps are investigated independently. Furthermore, the reasons behind inconsistencies when passivating the HFET surface using SiN is explained and a plasma pre-treatment step is introduced before deposition of the dielectric layer which greatly reduces current collapse under pulse biased conditions.

5.2 Current Collapse in AlGaN/GaN HFETs

In AlGaN/GaN HFETs the 2 dimensional electron gas (2DEG) is formed as a result of the spontaneous and piezoelectric polarisation charges present within the structure. According to Ibbetson's model [5], electrons which form the 2DEG are supplied by surface states on the AlGaN barrier. These states are generally associated with traps formed from dangling bonds and threading dislocations. In order for the system to remain charge neutral, the positive states on the free AlGaN surface exactly balance the sheet charge contained within the 2DEG.

Under typical device operating conditions a high electric field is present at the drain edge of the gate. These high fields cause electrons, in the form of leakage current from the gate, to be injected onto the AlGaN barrier surface. The tunnelling electrons are subsequently trapped by positively charged surface states resulting in compensation. To maintain overall space charge neutrality in the system electrons

from the 2DEG channel are removed causing the depletion region to extend out beyond the gate electrode (figure 5.1). As the depletion region expands and the 2DEG density is reduced the output drain current drops. This modulation of charge contained within the channel in the un-gated region of the device forms a second "virtual gate" which is in series with the physical gate [2]. The output current then becomes dependent on how fast charge is transferred to and removed from these states which comprise the virtual gate. Under large signal RF operation the relatively long time constants associated with trapping states on the surface results in a significantly reduced current swing and consequently a corresponding reduction in output power. As the reduction in channel conductivity in the un-gated region between the gate and drain increases the knee voltage will correspondingly rise leading to a "walk out" effect in the characteristic. This frequency dependent slump in output drain current is one of the main factors which currently limit the efficiency of AlGaN/GaN HFETs for RF applications.

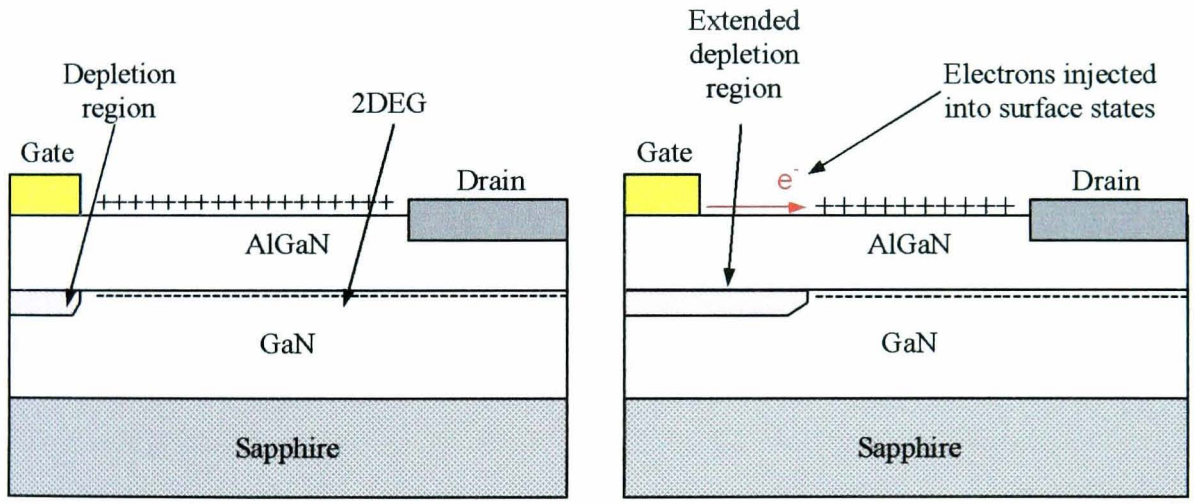


Figure 5.1 – Schematic showing electrons injected into surface states onto the AlGaN resulting in depletion of the 2DEG channel in the un-gated source-drain region.

The collapse in drain current and increase in knee voltage severely reduces the output power (P_{OUT}) of AlGaN/GaN HFETs when operated at RF frequencies. For a field effect transistor it can be shown the maximum AC output power which can be delivered to a load without clipping is given by equation 5.1.

$$P_{OUT} = \frac{(V_{BR} - V_{KNEE})I_{ds(MAX)}}{8} \qquad \text{Equation 5.1}$$

Where V_{BR} is the breakdown voltage of the device and $I_{DS(MAX)}$ is the maximum output drain current.

From equation 5.1 it is observed output power is proportional to both the knee voltage and maximum output current. Therefore, when operating AlGaN/GaN HFETs under large signal RF conditions current collapse results in significantly reduced P_{OUT} when compared to theoretically predicted values.

Figure 5.2a shows a typical DC output characteristic for a 100μm wide AlGaN/GaN HFET with a gate length of 250nm. Operating the device under these conditions revealed a drain current measured at 0 volts V_{GS} (I_{DSS0}) of 860mA/mm and an extrinsic transconductance of 190mS/mm. The negative output conductance observed in the characteristic was due to the poor thermal conductivity of the sapphire substrate. The same device was then biased under pulsed conditions in order to simulate large signal switching at RF frequencies (figure 5.2b). The initial bias points for V_{GS} and V_{DS} were set to pinch off (-6 volts) and 30 volts respectively. The gate and drain voltages were then pulsed for a period of 1μs to each point on the characteristic with a pulse separation of 1ms. Under such operating conditions the high field at the drain edge of the gate will result in electrons tunnelling from the Schottky contact into surface states on the AlGaN barrier depleting electrons in the channel. Consequently there is a significant drop in output current and also a large shift in the knee voltage. From the characteristic shown in figure 5.2b I_{DSS0} drops to ≈148mA/mm and the extrinsic transconductance is reduced to ≈26mS/mm. This clearly illustrates current collapse is a serious problem in unpassivated AlGaN/GaN HFETs which significantly degrades output performance at high frequencies. It is important to note the field at the source edge of the gate will also inject electrons into surface states at the un-gated source-gate region. However, this field is smaller when compared to the drain edge of the gate and so fewer electrons are injected onto the surface.

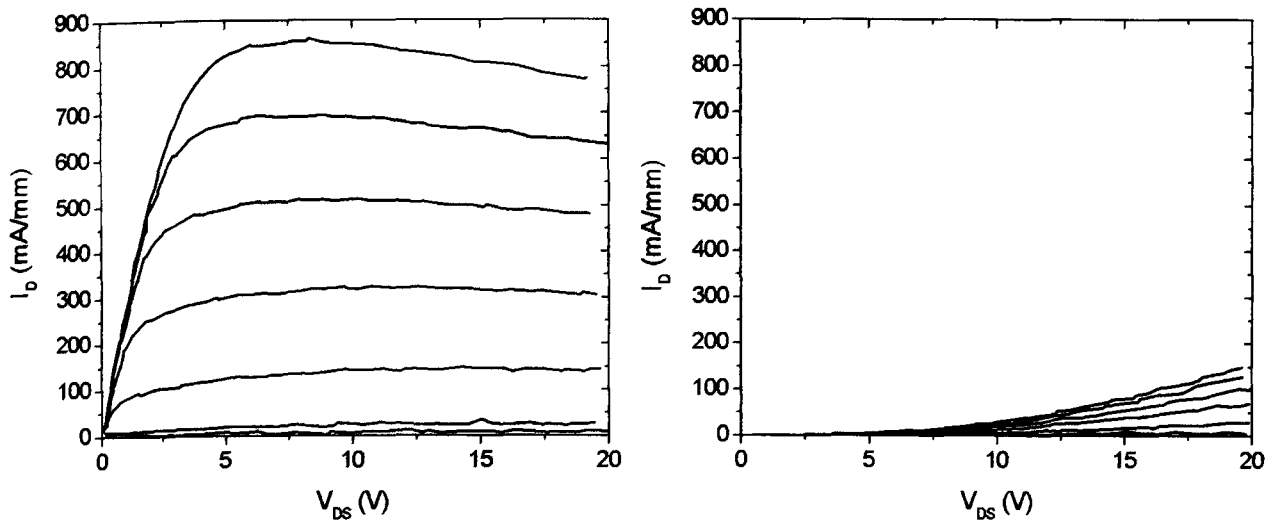


Figure 5.2 – (a) HFET characteristic under DC conditions for a 100μm wide device with a gate length of 250nm. (b) The same device under pulsed operation with the HFET initially biased at V_{GS} = -6 volts and V_{DS} = 20 volts, the pulse length was 1μs and the pulse separation was 1ms. The device was biased from V_{GS} = 0 volts to -6 volts in steps of 1 volt.

5.3 The Surface Leakage Test Structure

The surface leakage test structure was developed through a partnership between the University of Sheffield and QinetiQ Ltd. and was first introduced by Tan et al [6]. The device consists of two Schottky contacts and an ohmic (figure 5.3). Under normal operation the gate is reverse biased with respect to the ohmic and the guard is held at zero volts. Assuming the induced current does not result in a significant voltage drop underneath the guard terminal, which would result in the contact becoming forward biased, surface and bulk leakage components can be reliably separated. Under appropriate bias conditions electrons from the reversed biased Schottky gate will flow towards the guard. Any charge flowing along the AlGaN surface will be intercepted by the guard and therefore represents surface leakage (I_{SURF}). Current flowing into the ohmic contact must pass through either the AlGaN or GaN layers and hence denotes bulk current (I_{BULK}). Depending upon the geometry of the gate and guard contacts, mesa contributions to the leakage current (I_{MESA}) can also be separated. However in all the following experiments the rectifying metals were placed with no mesa edge

crossing to eliminate this component. An image of a completed surface leakage test structure taken using a scanning electron microscope (SEM) is shown in figure 5.4.

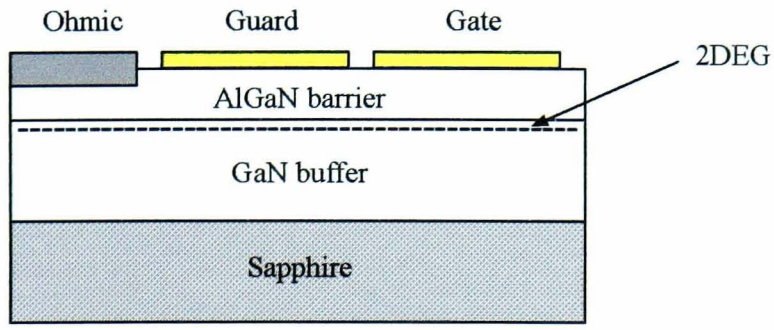


Figure 5.3 – A schematic diagram of the surface leakage test structure used on an AlGaN/GaN HFET structure.

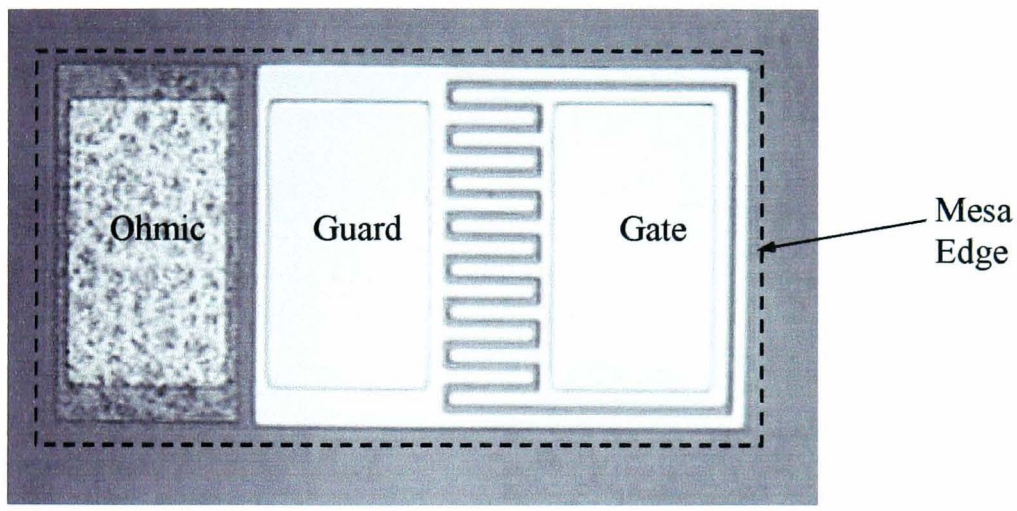


Figure 5.4 – An SEM image of the surface leakage test structure. The guard completely surrounds the gate to eliminate surface leakage current from reaching the ohmic contact.

A typical output from the surface leakage structure is shown in figure 5.5. As can be seen I_{BULK} dominates over I_{SURF} and increases rapidly until pinch-off after which the leakage component appears to saturate. This saturation occurs at voltages ≥ pinch-off since the vertical field underneath the gate electrode becomes constant at or above this bias and any further increase in the gate potential is dropped laterally in the gate-drain access region [7]. The lateral electric field on the AlGaN surface will continue to increase beyond pinch-off resulting in a continual rise in I_{SURF} with no apparent

saturation until breakdown. For these diodes the breakdown was found to be ≈330 volts. Unfortunately, at breakdown there was no clear evidence to suggest the mechanism was related to a surface or bulk effect.

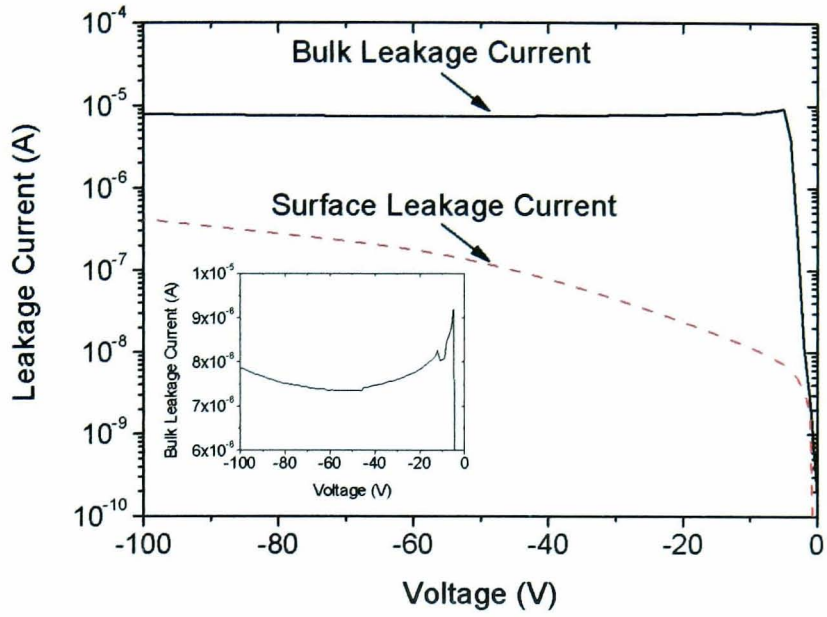


Figure 5.5 – Output from the test structure showing both bulk and surface leakage components. Inset shows the same bulk leakage current but using a linear scale.

To determine the different components which comprise the bulk and surface leakage currents both circular and interdigitated structures were employed. From analysis of circular devices with varying radius it was shown the total current was dominated by injection at the periphery of the rectifying contact with a small area term contributing to leakage (figure 5.6). The surface leakage component was found to scale roughly linearly with increasing radius, consistent with the model for electrons tunnelling onto the AlGaN surface from the Schottky metal. Therefore, three separate leakage paths can be deduced, including injection underneath the gate and at the edge which forms both bulk and surface leakage components (inset in figure 5.6).

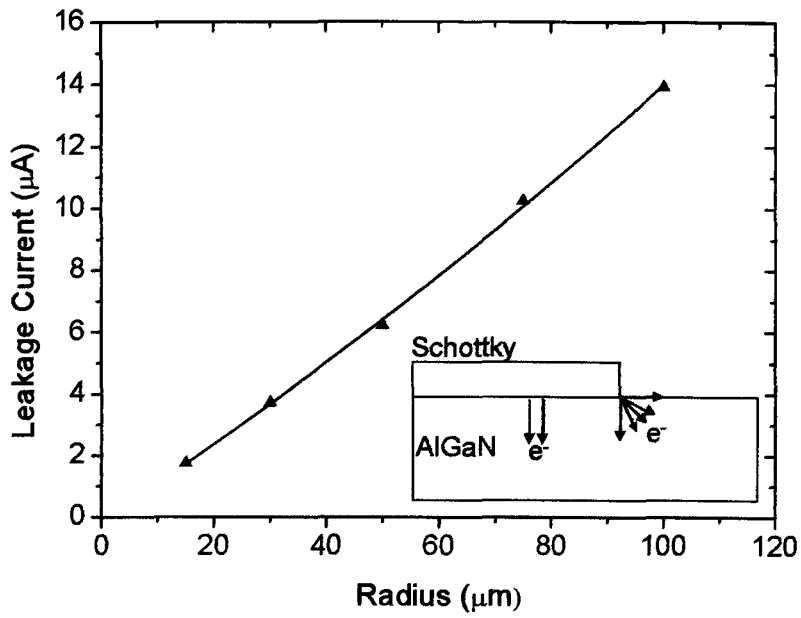


Figure 5.6 – Leakage current for Schottky diodes of varying radius. Inset shows the likely current injection under reverse bias which comprises injection from underneath the rectifying contact and injection at the periphery.

An interesting observation in the bulk leakage characteristic shown in figure 5.5, which is more clearly seen in the linear scaled inset, is an apparent reduction in reverse leakage current after pinch off which reaches a minimum at ≈50-60 volts and then begins to increase. This effect is contrary to leakage models proposed in the literature which suggest this component should saturate at pinch off and then increase slowly as the lateral field on the un-gated surface extends [7]. The degree of this effect was noted to vary from wafer to wafer but was present on both samples grown at Sheffield and QinetiQ. Generally this effect was more severe for samples showing reduced leakage currents under reverse bias.

To further investigate this phenomena temperature dependent I-V characteristics were taken of the bulk leakage component. The leakage current after pinch off is plotted against temperature in figure 5.7 and shows an unexpected negative dependence. The characteristic was found to pass through a minimum at 400-420K after which it began to rise. This characteristic, although not commonly reported in the literature, has been found to be present in both material grown at Sheffield and QinetiQ. For devices with

relatively high bulk leakage currents temperature dependent I-V curves revealed an exponential dependence on temperature which is consistent with models proposed in the literature. In the temperature regime from 25°C to 160°C the activation energy for these devices was found to be 50meV which is related to bulk traps in the AlGaN barrier layer.

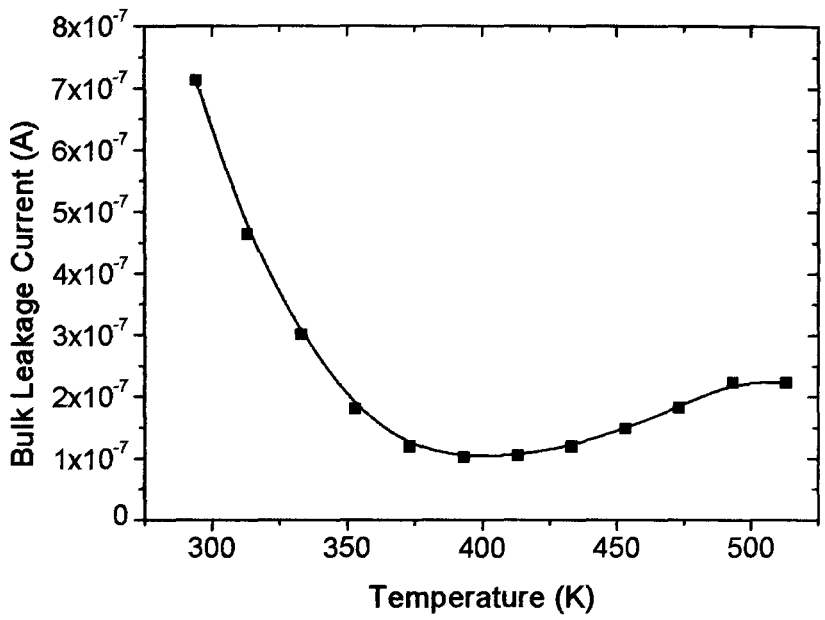


Figure 5.7 – Bulk leakage current plotted as a function of temperature from 295K to 373K.

To explain this negative temperature dependence a model of the barrier is proposed whereby the AlGaN layer is sparsely populated with traps which are donor like and are located close to or at the Schottky-semiconductor interface over a range of energies. This results in a modification to the band structure of the device with a reduced barrier width in the conduction band (E_C) close to this interface. As a reverse bias is applied electrons are able to directly tunnel through the spike, similar to a Fowler-Nordheim mechanism, resulting in leakage. However, electrons will also be able to tunnel into the interfacial traps. Since there are few traps contained within the AlGaN layer these electrons become stuck and can only move through the barrier by either a tunnelling, hopping or Poole-Frankel conduction mechanism [8]. Consequently, the width of the spike in the conduction band at the metal-

semiconductor interface is reduced preventing further leakage electrons from tunnelling directly through the barrier by thermionic field emission. As the temperature is increased the thermal energy of electrons in the metal is raised and more carriers are able to tunnel into these traps which are spread over a range of energies resulting in the observed reduction of bulk leakage. At sufficiently high temperature electrons in the gate metal have enough thermal energy to tunnel directly through the AlGaN by thermionic field emission or electrons contained within traps in the barrier may be able to pass through the layer via a hopping conduction. A schematic representation of this mechanism is shown in figure 5.8. It is observed that samples which exhibit these effects to a lesser degree generally have increased levels of bulk leakage. For these samples it is believed an increased number of traps are present throughout the entire AlGaN layer. Electrons are then able to tunnel through the barrier either via direct or a trap assisted tunnelling mechanism resulting in increased levels of bulk leakage within the structure consistent with theories regarding the origin of leakage in AlGaN/GaN structures [9][10].

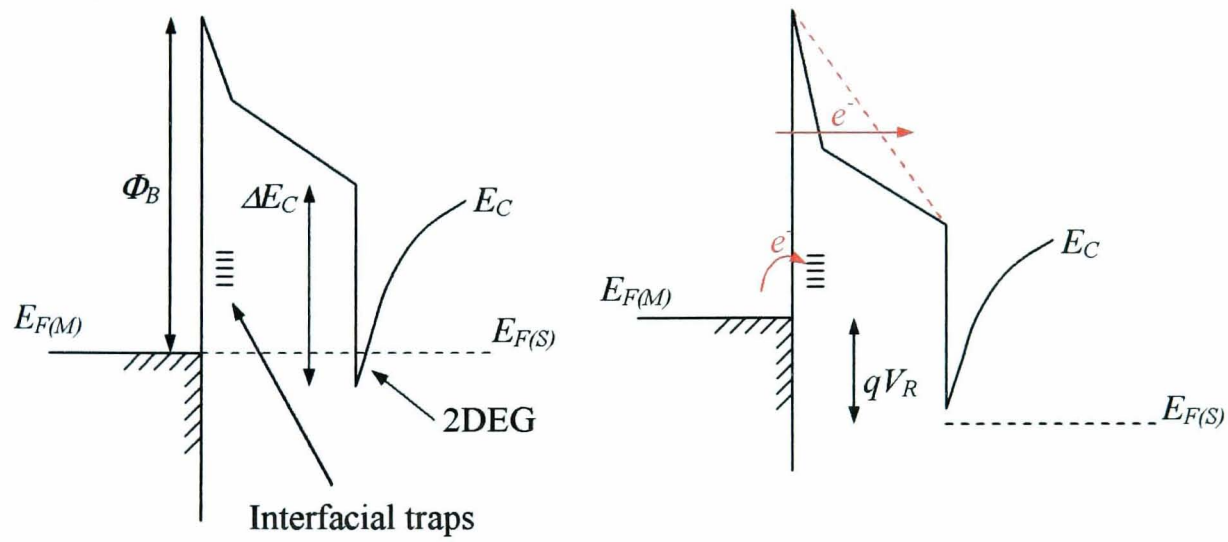


Figure 5.8 – A schematic representation of the proposed model for bulk leakage current in AlGaN/GaN heterostructures at equilibrium and under a reverse bias (V_R).

The surface leakage current was found to increase exponentially with increasing temperature. An activation plot of surface leakage is shown in figure 5.9 and shows two distinct regions, illustrating two separate mechanisms which each dominate under

different temperature regimes. It has been proposed in the literature that current flowing at the AlGaN surface occurs via a hopping conduction mechanism [11]. This process will be limited by either how many electrons can be injected into barrier states or by how fast electrons are transported across the surface, depending on which mechanism is slowest. Using the novel test structure it is demonstrated that in the lower temperature regime (20°C to 160°C) the mechanism is dominated by how fast the electrons hop across the surface. As the temperature is raised the electrons gain more energy and can therefore move across the surface faster. At a temperature of approximately 160°C electrons on the surface have enough energy to move freely and the rate becomes limited by how fast electrons can be injected onto the surface from the gate (figure 5.10). The activation energy for the lower temperature range which relates to the trap depth of surface states is found to be equal to 200meV. The activation energy for the higher temperatures is found to be 1.1eV which is the expected barrier height for a Ni/Au rectifying contact on an AlGaN surface [12] and is therefore consistent with the proposed model.

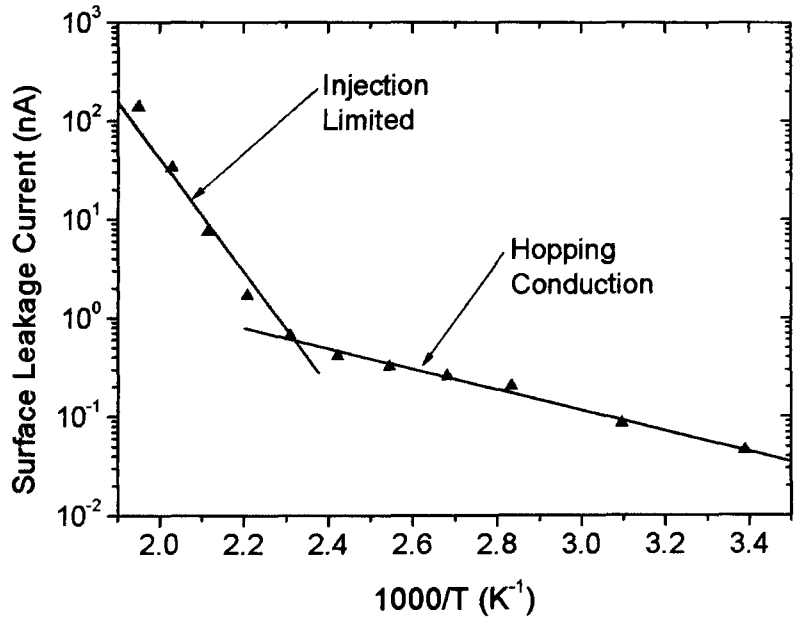


Figure 5.9 – Surface leakage current measured at varying temperatures. The activation energies for the two regions are 200meV for temperatures between 20°C to 140°C and 1.1eV from 140°C to 340°C.

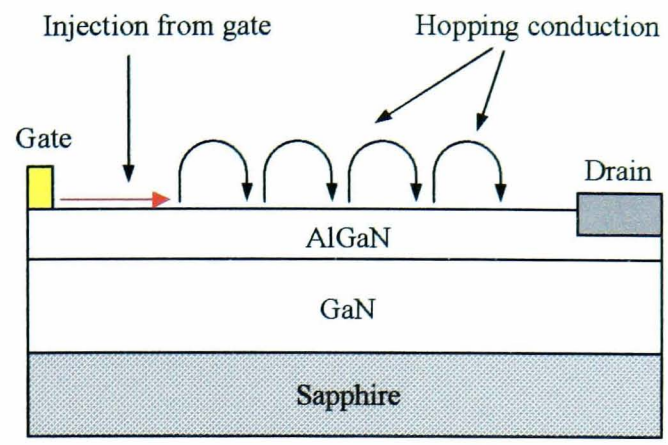


Figure 5.10 – Mechanism for surface leakage showing two separate processes including injection from the gate and subsequent hopping along the AlGaN surface.

5.4 Passivation and Surface Pre-Treatment

Passivation, usually using SiN deposited by plasma enhanced chemical vapour deposition (PECVD), has been found successful in reducing current collapse in AlGaN/GaN HFETs [2][3]. Deposition of a dielectric layer is often accompanied by a detrimental increase in the gate leakage current which has consequences for noise sensitive applications and is difficult to reconcile using conventional models. Although the mechanism for the removal of current collapse is not fully understood, it is widely believed that the dielectric layer buries states on the AlGaN surface making them inaccessible to electrons injected from the gate and therefore suppresses current flow at the surface. This decrease in surface leakage after passivation has recently been confirmed using the novel surface leakage test structure [6]. However, passivation of the AlGaN is not always completely successful in reducing current collapse to negligible levels and variation in effectiveness is widely observed.

Figure 5.11 shows the I-V behaviour for both I_{BULK} and I_{SURF} before and after passivation with ≈50nm of standard Si_3N_4. As can be seen from figure 5.16, a small increase in the bulk leakage current occurs after deposition of the SiN layer. This has been observed previously by other groups [13][14], however, using the test structure reveals that this increase is related to a bulk effect. More significantly the surface leakage component is found to drop by ≈1 order of magnitude. Previous work by our group demonstrated for the first time, using this novel test structure, that leakage

current at the AlGaN surface is indeed suppressed by the deposition of a passivating SiN film, consistent with models proposed in the literature. Furthermore, this drop in I_{SURF} at the un-gated region relates directly to a reduction in current collapse in passivated AlGaN/GaN HFETs [6].

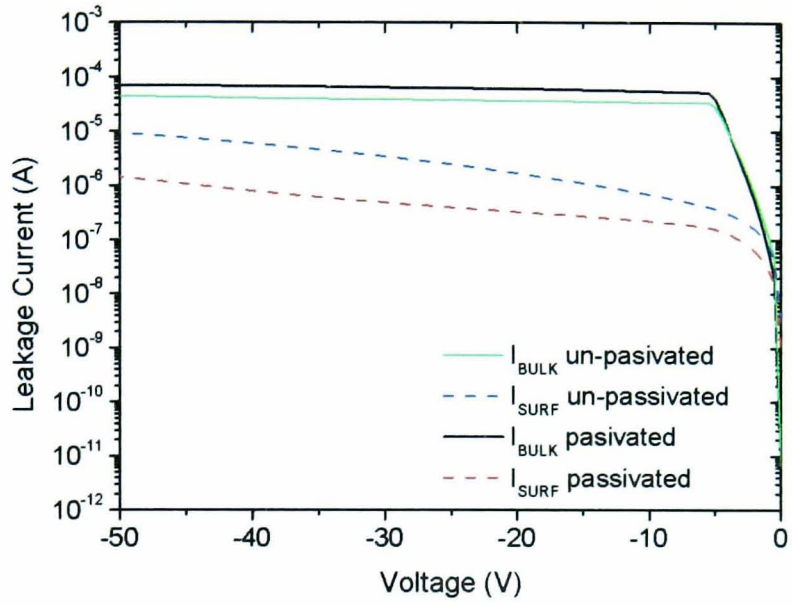


Figure 5.11 – I-V characteristic for the surface leakage structure fabricated on HFET material grown on a sapphire substrate. The solid green line represents bulk leakage before passivation and the black line after passivation. The blue and red dashed lines represent the surface leakage current before and after passivation respectively.

Depositing varying SiN film thicknesses from 50nm to 150nm on top of the AlGaN/GaN HFET was found to have negligible effect upon the output characteristics with all devices showing a similar reduction in surface leakage current after passivation. This provides direct evidence to suggest that the thickness of the film has no direct link with current collapse and only the first few mono-layers which are in contact with the barrier layer of the HFET bury states on the AlGaN preventing current flow. This would suggest these two layers must be in intimate contact in order for the passivating film to be effective. Contaminants on the HFET surface such as oxide and resist which is left over from device processing can prevent this intimate contact between the two layers which therefore leads to the observed inconsistencies

in results. Preliminary studies in the literature have shown plasma pre-treatments prior to passivation are effective in removing these contaminants from the semiconductor surface [15][16]. These studies do not attempt to find optimum conditions in terms of plasma power and exposure time. Furthermore, damage to the AlGaN layer is not considered which may affect breakdown voltage.

The recently introduced surface leakage test structure is used to investigate the effects of varying CF_4 pre-treatments prior to passivation with standard Si_3N_4. Measuring bulk and surface leakage currents directly will enable optimum conditions to be determined, reducing current slump to negligible levels and maximising device efficiency. Using the test structure to monitor breakdown voltage and leakage components it will be possible to quantify damage introduced by exposure to the plasma.

HFET material used in this work was grown at both the National Centre for III-V Technologies, Sheffield and QinetiQ Ltd, Malvern. After fabrication of the surface leakage test structure samples were loaded into a PECVD system and exposed to various CF_4 plasma pre-treatments. During the pre-treatment the pressure was held constant at 900mTorr and the corresponding flow rate for the gas was set at 90 standard cubic centimetres per second (sccm). 50nm of Si_3N_4 was deposited onto the surface directly after exposure, maintaining a constant vacuum over the sample to minimise exposure of the AlGaN to contaminants present in the atmosphere.

Figure 5.12 shows the affect of incorporating a 40W plasma pre-treatment for a period of 1.5 minutes directly prior to passivation. After deposition of the dielectric film a significant drop in the surface leakage component by 2-3 orders of magnitude is observed. This demonstrates a 1-2 order of magnitude reduction in current flow at the surface compared to the non-pre-treated passivated test structure (figure 5.11) indicating the surface contamination has been effectively removed by the plasma allowing intimate contact between the AlGaN and dielectric layers. For this relatively long exposure it was observed a soft breakdown was introduced into the structure at 30-40 volts. This limits the maximum operating voltage of the HFET and decreases maximum output power (equation 5.1).

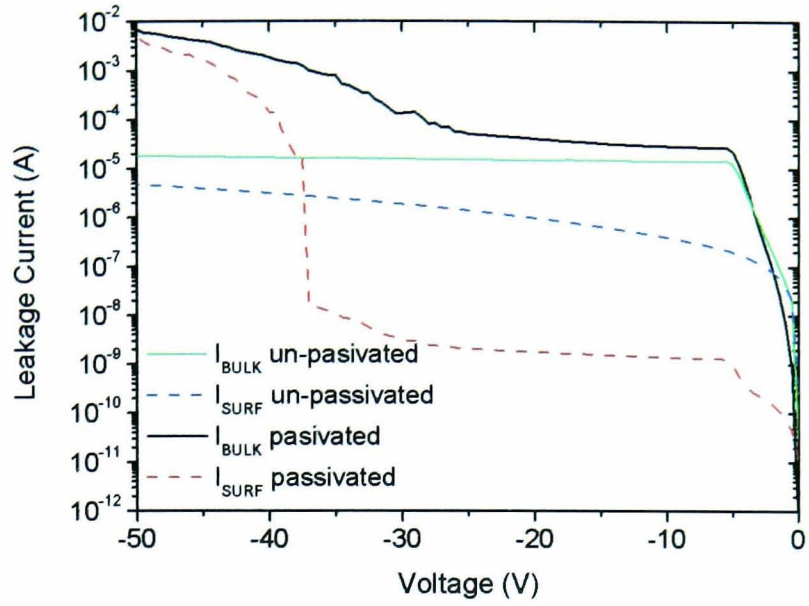


Figure 5.12 – Bulk and surface leakage components for a device exposed to a CF_4 plasma pre-treatment of 40W for 1.5 minutes before deposition of ≈50nm of standard SiN. The solid green line represents bulk leakage current before passivation and the black line after passivation. The blue and red dashed lines represent the surface leakage before and after passivation respectively.

Decreasing the exposure time of the CF_4 plasma to 1 minute prior to passivation maintained roughly the same 2-3 orders of magnitude reduction in surface current. However, the breakdown voltage was found to increase to ≈80 volts (figure 5.13). Reducing the exposure time further to 30 seconds (figure 5.14) resulted in minimal reduction in the surface leakage when compared to non pre-treated samples. Using the optimum exposure time of 1 minute the power of the CF_4 plasma was varied in an effort to further reduce surface leakage current and maximise breakdown voltage. It was found that increasing the power to higher levels resulted in an unacceptably low breakdown voltage, similar to that shown in figure 5.12. Reducing RF power to levels <40W was found to be ineffective in removing surface contamination, resulting in negligible reduction of surface leakage. This is the first optimisation of a plasma pre-treatment exposure prior to passivation in AlGaN/GaN HFETs in order to maximise the efficiency of the deposited dielectric film.

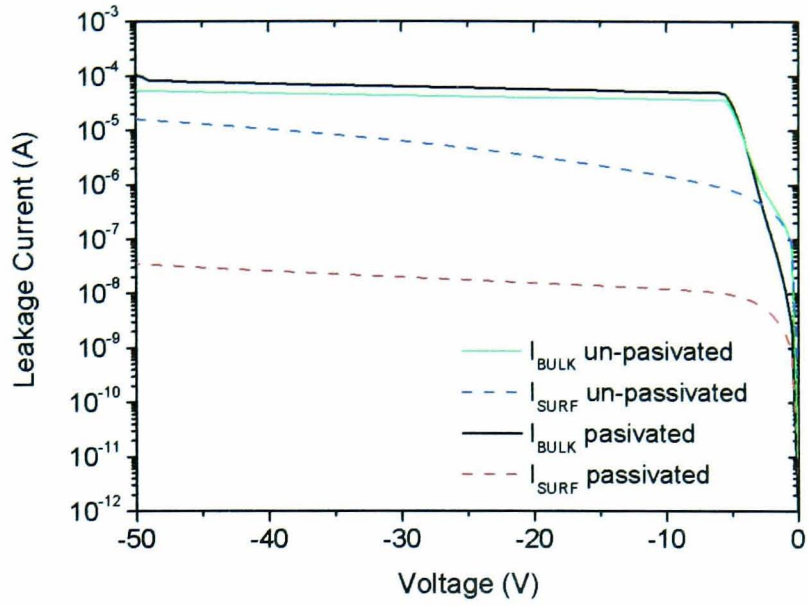


Figure 5.13 – Bulk and surface leakage components for a device exposed to a CF_4 plasma pre-treatment of 40W for 1 minute before deposition of ≈50nm of standard SiN. The solid green line represents bulk leakage current before passivation and the black line after passivation. The blue and red dashed lines represent the surface leakage current before and after passivation respectively.

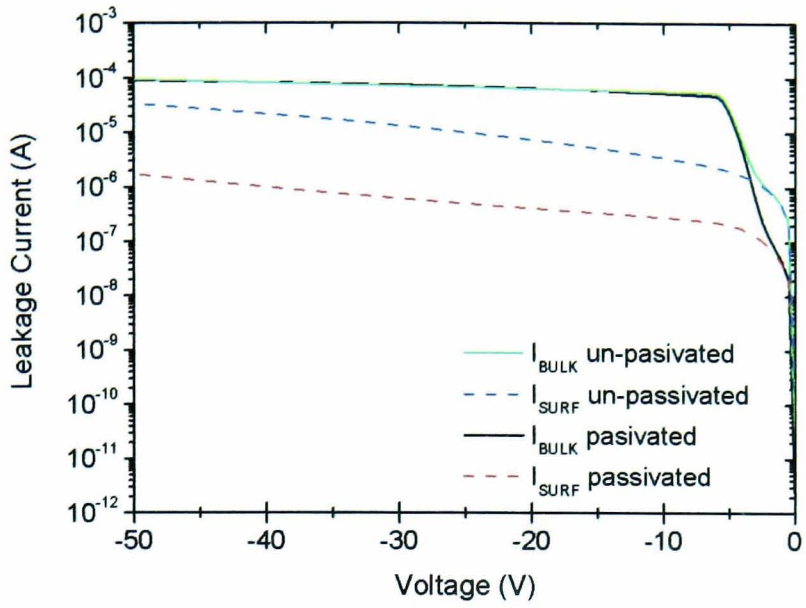


Figure 5.14 – Bulk and surface leakage components for a device exposed to a CF_4 plasma pre-treatment of 40W for 0.5 minutes before deposition of ≈50nm of standard SiN. The solid green line represents bulk leakage current before passivation and the black line after passivation. The blue and red dashed lines represent the surface leakage current before and after passivation respectively.

5.5 HFET Devices Using the Optimised CF_4 Plasma Pre-Treatment

The surface leakage current can be used as a quantitative factor in the assessment of current collapse in AlGaN/GaN HFETs. From the results presented in section 5.4.1 this would indicate that for passivated CF_4 exposed samples large signal RF performance should be significantly enhanced. Since no microwave characterisation facilities are available at Sheffield pulse measurements are used to simulate the high frequency response of the component. The experimental setup for the gate lag measurement and fabrication of devices is described in detail in sections 2.6 and 2.3 of chapter 2 respectively. Gates were defined using optical lithography with lengths ranging from 0.7-1.5μm. For passivated devices 50nm of Si_3N_4 was subsequently deposited using PECVD. Pulsed measurements were performed at a constant V_{DS} potential above the saturation point at (6 volts). V_{GS} is then kept at or below pinch off (-6 volts) and the gate pulsed to the full channel current (I_{DSS0}). For these experiments

the pulse length used was 400ns with a low repetition rate in order to minimise self heating. The output drain current is then normalised to the DC value giving the gate lag ratio (GLR). A GLR of 1 represents the ideal response and a ratio of 0 indicates massive current collapse in the structure. The pulsed gate lag measurements were performed on un-passivated and passivated HFETs and also devices using various pre-treatments prior to deposition of the dielectric layer.

A typical output response for an AlGaN/GaN HFET with no passivation showed a ratio of ≈0.40 indicating a significant level of current collapse. After deposition of the Si_3N_4 layer with no pre-treatment the gate lag ratio was found to vary from sample to sample with devices demonstrating an average GLR of 0.79. This illustrates the problems in consistency when passivating the AlGaN surface and the variability in results. A simple wet treatment using 9:1 Ammonia: deionised (DI) water for 5 minutes prior to passivation was also included. This treatment, which is used extensively at Sheffield prior to deposition of n-type ohmic contacts, reduces native oxide on the semiconductor surface, enabling reduced source and drain parasitic resistances. By utilising this treatment surface oxide which may prevent the intimate contact between the passivating SiN layer and AlGaN barrier can be eliminated. However, using this treatment also resulted in a large variation in the measured GLR with an average value of 0.8 which is similar to non-pre-treated values. Finally using SiN passivation in conjunction with the optimised CF_4 pre-treatment resulted in a dramatic increase in the gate lag ratio to ≈1 with only a 3% variation between the wide range of samples tested. These results are summarised in the bar chart shown in figure 5.15. These ratios were found to exhibit negligible deviation from the quoted values for drain biases ranging from 6 to 15 volts.

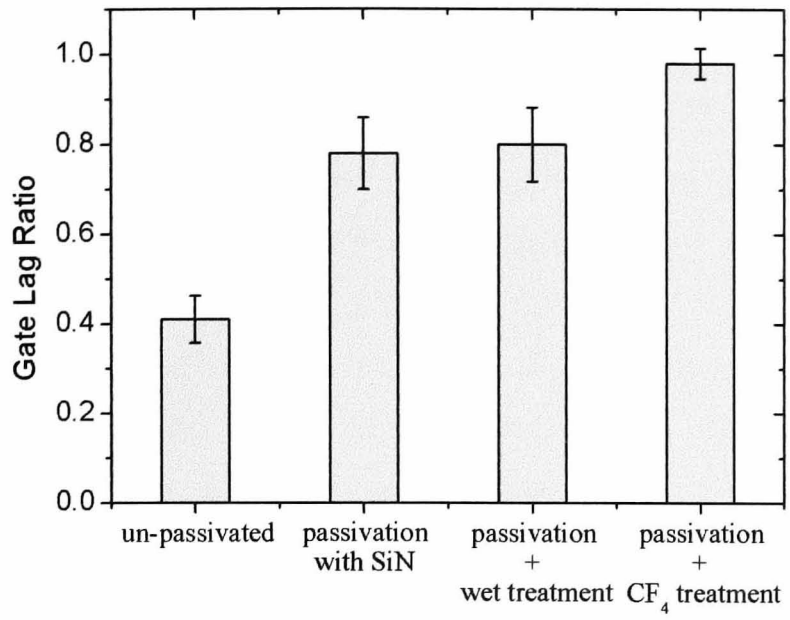


Figure 5.15 – Gate lag ratio for HFETs fabricated on Si substrates with no passivation, passivation with SiN and passivation with a CF_4 pre-treatment for 1 minute.

This gives further direct evidence the reduction in surface leakage relates directly with a reduction in current collapse in AlGaN/GaN HFETs. Omitting the plasma pre-treatment step does not result in intimate contact between the dielectric and semiconductor layer, with a consequent reduction in efficiency. Furthermore, reduction in the native oxide present on the AlGaN surface was not effective in significantly improving current collapse in AlGaN/GaN HFETs. However, it is important to note that completely removing oxides from AlGaN surfaces is extremely difficult using wet treatments [17] and therefore it is likely some interfacial layer is still present which prevents intimate contact between the dielectric and semiconductor. It is also suggested that other contaminants on the AlGaN are present such as resist and/or other impurities left over from the fabrication process. The plasma pre-treatment has been effective in removing both these contaminants and the oxide from the AlGaN surface, allowing intimate contact with the deposited dielectric and the barrier layer. This enabled current collapse to be reduced to negligible levels and with minimal variation between samples.

5.6 Mechanism of Soft Breakdown in Plasma Pre-Treated HFETs

The surface leakage structure was used to assess the effects of plasma exposure without any passivation on the AlGaN surface. The results of this experiment are presented in figure 5.16. After a 40W CF_4 plasma treatment for 1 minute the bulk leakage current is relatively unaffected when compared to the un-pre-treated device. However, the surface leakage current is found to reduce by a similar degree to that of pre-treated devices which are passivated with Si_3N_4. This unexpected result indicates that either the contaminants present on the AlGaN surface may play a role in the severity of current collapse or the CF_4 pre-treatment results in the formation of a thin layer which acts to bury states present on the surface. Furthermore the breakdown voltage of the component is identical to un-passivated devices. Depositing SiN on top of the test structure shown in figure 5.16 resulted in a soft-breakdown similar to that shown previously.

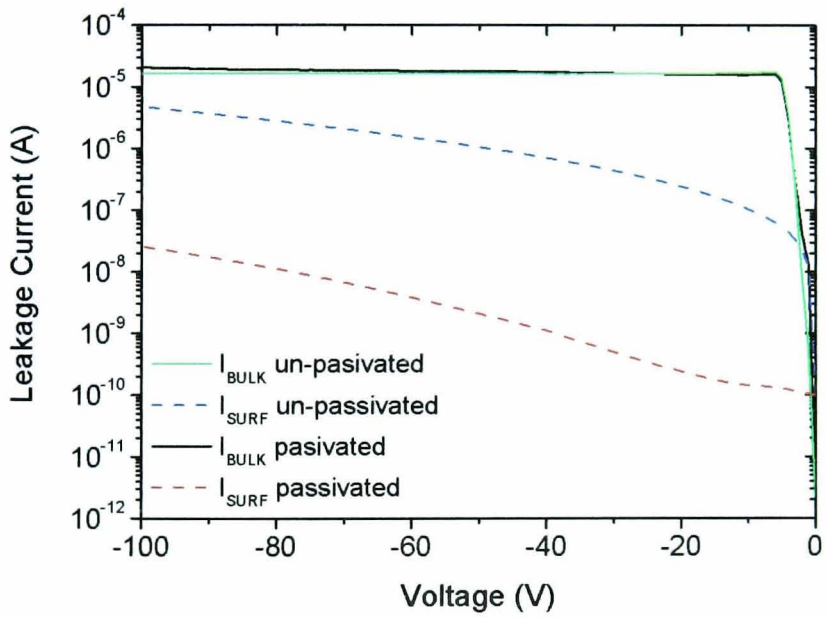


Figure 5.16 – I-V characteristic for the surface leakage structure when exposed to a 40W CF_4 plasma for a period of 1.5 minutes. The solid green line represents bulk leakage current before passivation and the black line after passivation. The red and blue dashed lines represent the surface leakage current before and after passivation respectively.

In order to determine if a thin passivation layer is formed on the surface prior to deposition of the SiN, energy dispersive x-ray (EDX) analysis in conjunction with an SEM was employed. The results of this experiment were inconclusive due to the relatively large penetration depth of incident electrons compared to a thin film on the AlGaN surface. However, it is believed the fluorine in the CF_4 pre-treatment has reacted with the aluminium in the barrier layer to form a thin film of AlF_3 on the surface [18][19]. For the case of the AlGaN/GaN structure shown in figure 5.16 this thin film acts as a passivant, significantly reducing current flow at the surface of the HFET. Testing the CF_4 pre-treatment on four different wafers without subsequent SiN passivation revealed identical results, with the plasma treatment significantly reducing surface leakage when compared to SiN passivated samples with no pre-treatment. Consequently, despite the creation of a thin interfacial layer at the AlGaN surface, the pre-treatment is still effective in removing contaminants from the barrier layer, and the surface leakage current is significantly reduced, with negligible variation between results. Performing gate lag measurements on these devices demonstrated a GLR of $\approx$1 with negligible variation between samples indicating no measurable current collapse. Therefore CF_4 pre-treated HFETs with no subsequent SiN passivation will exhibit greatly increased P_{OUT} since current collapse is significantly reduced while not affecting breakdown. This is the first AlGaN/GaN HFET passivated using an AlF_3 film.

To further investigate the effects of exposing the CF_4 plasma to the AlGaN surface circular Schottky diodes were fabricated from the HFET material. One set of samples was fabricated by depositing the standard Ti/Al/Ti/Au ohmic contact followed by Ni/Au rectifying metals. A second set was fabricated in the same way. However, prior to deposition of the Schottky metals, the sample was exposed to a CF_4 plasma pre-treatment of 40W for a period of 1.5 minutes. Both sets of devices were characterised using temperature dependant I-V. An Arrhenius plot can be used to determine the barrier height and Richardson constant for the Schottky diodes independently [20]. Figure 5.17 shows the Richardson plots for diodes fabricated both with and without exposure to the plasma. For the standard diodes a value of 0.45eV and $2.85 Acm^{-2}K^{-2}$ was found for the barrier height and Richardson constant respectively. Ideality factors for these devices where found to be in the range 1.2-1.5. For the second set of Schottky diodes, which were exposed to the CF_4 plasma prior to depositing the

rectifying contacts, the barrier height was found to be significantly reduced to ≈0.26eV and the Richardson constant has increased to ≈3.1Acm^{-2}K^{-2}. The ideality factor for the plasma damaged diodes was found to be ≈2-3.

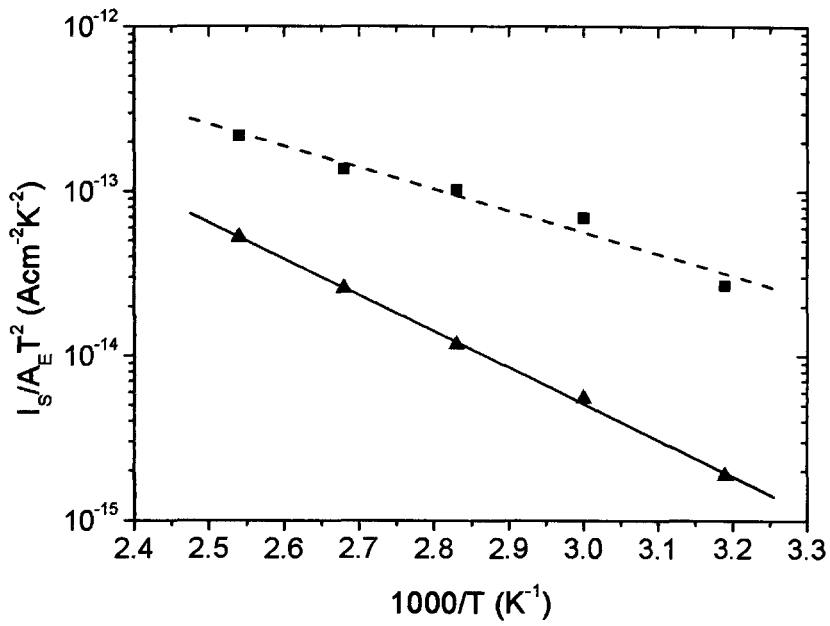


Figure 5.17 – Richardson plot for Schottky diodes fabricated on HFET material with (▲) measured for a diode with no pre-treatment and (■) for a device fabricated using a 40W CF_4 plasma pre-treatment prior to depositing the rectifying contact. I_S represents the saturation current, A_E is the area of the diode and T is the temperature in Kelvin.

For the pre-treated devices this suggests donor-like pinning states are introduced at the AlGaN surface which reduce the barrier height in the un-gated region. CF_4-based plasma treatments have recently been used to create enhancement mode HFETs which have state of the art performance [21][22][23]. The CF_4 is believed to be implanted into the structure creating acceptor like states in the AlGaN. However, these pre-treatments are typically performed at high RF powers and for relatively long periods of time. For the devices shown in this study it is believed the RF power is too low to implant the plasma species, however the energy of the ions may be sufficient to displace nitrogen atoms in the AlGaN crystal lattice forming vacancies. Nitrogen vacancies are thought to introduce shallow states into the bandgap near the conduction

band edge and hence act as donors [24]. It is therefore proposed that during the CF_4 pre-treatment these states are introduced at the surface which lowers the barrier height for the AlGaN in the un-gated region between the source and drain. Current flowing at the surface is then suppressed by the passivating AlF_3 film and no soft-breakdown occurs since electrons are unable to access these regions of reduced barrier height. After depositing SiN on the HFET surface electrons are able to flow to these areas of low barrier height at sufficiently high electric fields by a Poole-Frankel conduction mechanism [8]. These electrons result in the creation of further states at the surface [25] and a further reduction in barrier height. This leads to a runaway effect resulting in the observed soft breakdown at reduced voltage.

It is interesting to note the same soft-breakdown effect could be induced when annealing the sample prior to deposition of the rectifying contact. When alloying the ohmic contacts several samples were subjected to increased temperatures. This was shown to have negligible effects on the quality of the ohmic contacts and prior to passivation the breakdown for the devices was unaffected. After depositing 50nm of Si_3N_4 and re-testing the devices the bulk leakage current was found to increase as shown previously but a soft breakdown was also observed at a considerably reduced voltage similar to pre-treated passivated devices (figure 5.18). Annealing of GaN-based devices at temperatures in excess of ≈800-1000°C is found to result in a loss of N from the surface [26][27]. For these devices the bulk leakage current was found to be reduced with excessive annealing while the surface leakage current was found to increase consistent with the creation of donor like states at the AlGaN surface. This further supports the proposed mechanism for soft-breakdown whereby electrons reach an area of low barrier height, caused by nitrogen vacancies on the surface of the un-gated region, through the passivating SiN film.

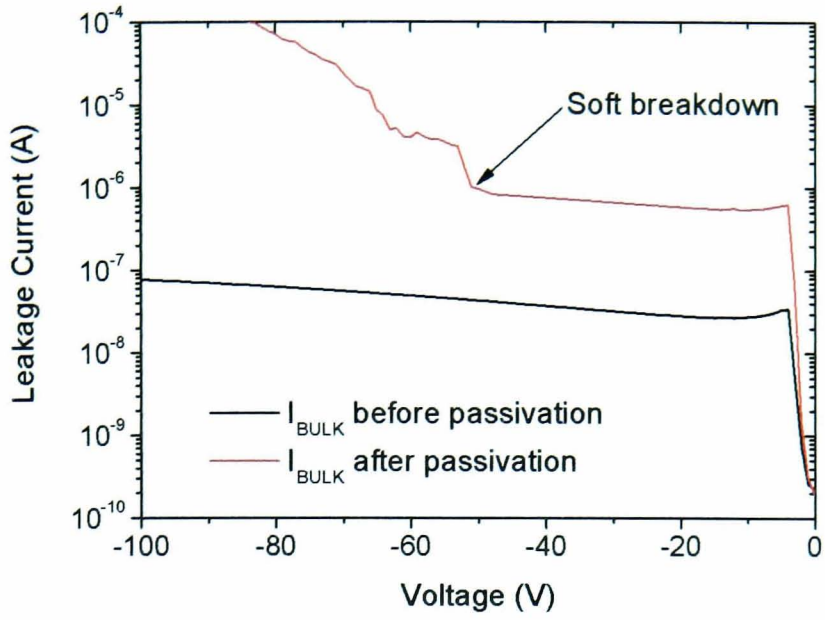


Figure 5.18 – Example of a sample which was subjected to an anneal temperature and time which was greater than that of the optimum.

5.7 Conclusions

Using the novel surface leakage test structure, bulk and surface leakage components in AlGaN/GaN structures have been investigated. DC characteristics taken at both room and elevated temperatures revealed the presence of bulk traps at the Schottky/AlGaN interface. Temperature dependent I-V showed surface traps to have a depth of ≈200meV. When operating at temperatures below 160°C it was found that surface leakage current was dominated by a hopping conduction mechanism at the AlGaN surface. At temperatures in excess of 160°C electrons contained within surface states are able to move freely and surface leakage current becomes dependent on the rate of electron injection from the gate. This is the first experimental study of bulk and surface related traps in AlGaN/GaN HFETs investigated independently using the novel surface leakage test structure.

Passivation of AlGaN/GaN structures is found to impede leakage at the AlGaN surface which is fully consistent with models of current collapse proposed in the literature. Introducing a CF_4 pre-treatment prior to passivation further reduces surface

leakage current. Using the test structure enabled, for the first time, this step to be optimised. Employing CF_4 pre-treatments was found to create a thin layer of AlF_3 on the HFET surface which acted as a passivating layer. However, due to the negligible variation in results between samples, the CF_4 pre-treatment was also effective in removing surface contamination allowing intimate contact between the dielectric and barrier surface. Applying optimised CF_4 exposure conditions for devices that were both passivated and un-passivated with SiN resulted in negligible current collapse with little variation between samples. This is the first example of a AlGaN/GaN HFETs passivated using a AlF_3 film.

Depositing SiN on pre-treated devices resulted in a soft-breakdown at reduced voltage. This was attributed to a reduced barrier height at the pre-treated un-gated regions. Upon deposition of a SiN layer and at sufficiently high electric fields electrons from the gate are able to access these regions of low barrier height through the dielectric layer.

5.8 References

[1] *Y.F. Wu, A.Saxler, M. Moore, R.P. Smith, S. Sheppard, P.M. Chavarkar, T. Wisleder, U.K. Mishra, P. Parikh "30-W/mm GaN HEMTs by field plate optimization" IEEE Electron Device Letters, Vol. 25, No. 3, pp 117-119, 2004*

[2] *Y.F. Wu, M. Moore, A. Saxler, T. Wisleder, P. Parikh "40W/mm double field-plated GaN HEMTs" Proceedings Digital Device Research Conference, pp 151-152, 2006*

[3] *R. Vetury, N.Q. Zhang, S. Keller, U.K. Mishra "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs" IEEE Transactions on Electron Devices, Vol. 48, No. 3, pp 560-566, 2001*

[4] *B.M. Green, K.K. Chu, E.M. Chumbers, J.A. Smart, J.R. Shealy, L.F. Eastman "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs" IEEE Electron Device Letters, Vol. 21, No. 6, pp 268-270, 2000*

[5] *J.P. Ibbetson, P.T. Fini, K.D. Ness, S.P. DenBaars, J.S. Speck, U.K. Mishra "Polarisation effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors" Applied Physics Letters, Vol. 77, No. 2, pp 250-252, 2000*

[6] *W.S. Tan, M.J. Uren, P.A. Houston, R.T. Green, R.S. Balmer, T. Martin "Surface leakage currents in SiN_x passivated AlGaN/GaN HFETs" IEEE Electron Device Letters, Vol. 27, No. 1, pp 1-3 , 2006*

[7] *E.J. Miller, X.Z. Dang, E.T. Yu "Gate leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors" Journal of Applied Physics, Vol. 88, No. 10, pp 5951-5958*

[8] *S.M. Sze "Physics of semiconductor devices 2nd edition" New York, Wiley, pp 402, 1981*

[9] *S. Karmalkar, D.M. Sathaiya, M.S. Shur "Mechanism of the reverse gate leakage in AlGaN/GaN high electron mobility transistors" Applied Physics Letters, Vol. 82, No. 22, pp 3976-3978, 2003*

[10] *D.M. Sathaiya, S. Karmalkar "Thermionic trap-assisted tunnelling model and its application to leakage current in nitrided oxides and AlGaN/GaN high electron mobility transistors" Journal of Applied Physics, Vol. 99, No. 9, 2006*

[11] W.S.Tan, P.A. Houston, P.J. Parbrook, D.A. Wood, G. Hill C.R. Whitehouse "Gate leakage effects and breakdown voltage in metalorganic vapour phase epitaxy AlGaN-GaN heterostructure field-effect transistors" Applied Physics Letters, Vol. 80, No. 17, pp 3207-3209, 2002

[12] M.W. Low "An experimental study of AlGaN/GaN Schottky diodes" MPhil Thesis, Sheffield University, 2006

[13] W.S. Tan, P.A. Houston, P.J. Parbrook, G. Hill R.J. Airey "Comparison of different surface passivation dielectrics in AlGaN/GaN heterostructure field-effect transistors" Journal of Physics D: Applied Physics, Vol. 35, No. 7, pp 595-598, 2002

[14] J.S. Lee, A. Vescan, A. Wieszt, R. Dietrich, H. Leier, Y.S. Kwon "Small signal and power measurements of AlGaN/GaN HEMT with SiN passivation" Electronics Letters, Vol. 37, No. 2, pp 130-132, 2001

[15] A.P. Edwards, J.A. Mittereder, S.C. Binari, D.S. Katzer, D.F. Strom, J.A. Roussos "Improved reliability of AlGaN-GaN HEMTs using an NH_3 plasma treatment prior to SiN passivation" IEEE Electron Device Letters, Vol. 26, No. 4, pp 225-227, 2005

[16] Y.Guhel, B. Boudart, N. Vellas, C. Gaquière, E. Delos, D. Ducatteau, Z. Bougrioua, M. Germain "Impact of plasma pre-treatment before SiN_x passivation on AlGaN/GaN HFETs electrical traps" Solid-State Electronics, Vol. 49, No. 10, pp 1589-1594, 2005

[17] D. Buttari, A. Chini, T. Palacios, R. Coffie, L. Shen, H. Xing, S. Heikman, L. McCarthy "Origin of etch delay time in Cl_2 dry etching of AlGaN/GaN structures" Applied Physics Letters, Vol. 83, No. 23, pp 4779-4781, 2003

[18] S. Salimian, C.B. Cooper, R. Norton, J. Bacon "Reactive ion etch process with highly controllable GaAs-to-AlGaAs selectivity using SF_6 and $SiCl_4$" Applied Physics Letters, Vol. 51, No. 14, pp 1083-1085, 1987

[19] R. Chu, C.S. Suh, M.H. Wong, N. Fichtenbaum, D. Brown, L. McCarthy, S. Keller, F. Wu, J.S. Speck, U.K. Mishra "Impact of CF_4 plasma treatment on GaN" IEEE Electron Device Letters, Vol. 28, No. 9, pp 781-783, 2007

[20] L.S. Yu, Q.Z. Liu, Q.J. Xing, D.J. Qiao, S.S. Lau, R. Redwing "The role of the tunnelling component in the current-voltage characteristics of metal-GaN Schottky diodes" Journal of Applied Physics, Vol. 84, No. 4, pp 2099-2104, 1998

[21] Y. Cai, Y. Zhou, K.J. Chen, K.M. Lau "High-performance enhancement-mode AlGaN-GaN HEMTs using fluoride-based plasma treatment" IEEE Electron Device Letters, Vol. 26, No. 7, pp 435-437, 2005

[22] T. Palacios, C.S. Suh, A. Chakraborty, S. Keller, S.P. DenBaars, U.K. Mishra "High-performance E-mode AlGaN/GaN HEMTs" IEEE Electron Device Letters, Vol. 27, No. 6, pp 428-430, 2006

[23] S. Jia, Y. Cai, D. Wang, B. Zhang, K.M. Lau, K.J. Chen "Enhancement-mode AlGaN/GaN HEMTs on silicon substrates" IEEE Transactions on Electron Devices, Vol. 53, No. 6. pp 1474-1477, 2006

[24] D.C. Look, G.C. Farlow, P.J. Drevinsky, D.F. Bliss, J.R. Sizelove "On the nitrogen vacancy in GaN" Applied Physics Letters, Vol. 83, No. 17, pp 3525-3527, 2003

[25] H Kim, R.M. Thompson, V. Tilak, T.R. Prunty, J.R. Shealy, L.F. Eastman "Effects of SiN passivation and high-electric field on AlGaN-GaN HFET degradation" IEEE Electron Device Letters, Vol. 24, No. 7, pp 421-423, 2003

[26] H.W. Choi, M.A. Rana, S.J. Chua, T. Osipowicz, J.S. Pan "Surface analysis of GaN decomposition" Semiconductor Science and Technology, Vol. 17, No. 12, pp 1223-1225, 2002

[27] M.A. Rana, T. Osipowicz, H.W. Choi, M.B.H. Breese, S.J. Chua "A study of the material loss and other processes involved during annealing of GaN at growth temperatures" Chemical Physical Letters, Vol. 380, pp 105-110, 2003

6 Gate Recessing of AlGaN/GaN HFETs

6.1 Introduction

In this chapter gate recessing of AlGaN/GaN HFETs is investigated using GaN capping layers. According to simulated results the recess will reduce the field on the surface of the device and could therefore potentially reduce current collapse and improve high frequency performance. A simple model is developed to describe how the sheet charge concentration will be affected by GaN capping thickness and is compared to experimentally obtained data.

Dry etching techniques are subsequently developed which can selectively remove the GaN capping layer on top of the HFET structure to enable a self-aligned gate recess process. Furthermore, damage to the exposed AlGaN barrier layer is investigated through Schottky diode I-V characteristics in order to quantify damage to the exposed semiconductor film.

6.2 Gate Recessing of AlGaN/GaN HFETs

The use of gate recessing in field effect devices has been widely exploited in GaAs technologies [1]. For AlGaN/GaN devices the use of the recess is also important as it acts to improve the source and drain ohmic contacts enabling reduced parasitic access resistance leading to improved performance under high frequency operation [2][3]. Through correct design the electric field at the surface of the semiconductor can be suppressed, preventing injection of electrons into surface states and reducing current collapse. Using DESSIS, a commercially available device simulation suite, it is possible to show how fields present at the surface will be modified by the recessed structure. Figure 6.1 shows the electric field profile underneath the gate at the drain edge side for an AlGaN/GaN HFET under typical operating conditions. It can be observed from the simulation that the high field at the Schottky can only extend laterally across the recessed surface preventing it from reaching the un-etched cap. Since this field is drawn away from the surface there will be less injection of electrons from the gate into surface states (chapter 5) and the large signal RF performance is consequently enhanced.

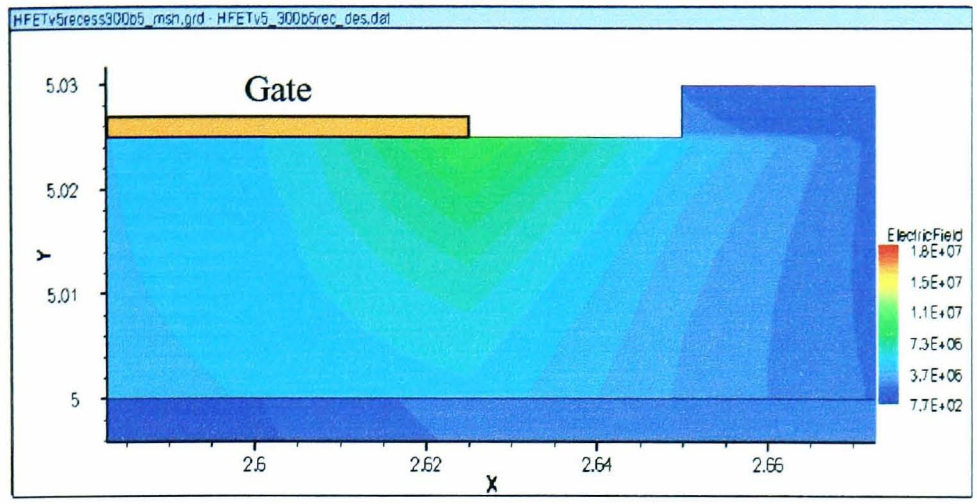


Figure 6.1 – DESSIS simulations performed by P. Vines showing the electric field profile of an $Al_{0.3}Ga_{0.7}N$/GaN HFET with a 30nm barrier layer and a 5nm recess. The length of the recess is 290nm and the gate length is 250nm. The gate-source and drain-source voltage is set to 0V and 30V respectively.

After recessing, an increase in transconductance and reduction in pinch-off voltage is generally observed [4][5] due to the decrease in distance between the gate metal and 2DEG channel. Kuliev et al [6] investigated the DC and RF performance of AlGaN/GaN HFETs with varying recess lengths from 0.5-1μm and showed very little dependence on RF performance. This agrees with DESSIS simulations performed at Sheffield which indicates a recess length of ≈20nm is sufficient to suppress the electric field on the un-recessed surface.

The use of thick capping layers has been found to greatly increase the large signal high frequency performance of devices without the need for passivation [7]. By spatially separating surface traps from the channel their effects are diminished allowing improved performance at RF frequencies. However, using thick capping layers requires appropriate strain management to prevent cracking in the epilayers and can also reduce conductivity in the channel. The incorporation of a field plate into AlGaN/GaN HFETs has been shown to increase breakdown voltage, reduce current collapse and improve linearity [8]. The extension of the plate over the gate increases parasitic capacitances and reduces gain in the component [9]. By incorporating a recessed gate into the field-plated structure the gain for the transistor can be

improved, leading to greatly enhanced power performance under high frequency operating conditions [10][11].

6.3 Capping Layers and its Affect on the 2DEG

For AlGaN/GaN HFETs it becomes advantageous to use a GaN capping layer for the recess which is heavily doped n-type. This will act to reduce the contact resistance of the source and drain, through both a reduction in barrier height and width. However, the use of a GaN capped layer will reduce the sheet charge in the 2DEG since the GaN cap will modify the spontaneous and piezoelectric polarisation charge distribution in the structure. For GaN/AlGaN/GaN structures a negative polarisation charge will be induced at the upper GaN/AlGaN heterointerface which will increase the electric field across the AlGaN and reduce the number of electrons in the 2DEG. This is shown schematically in figure 6.2 [12].

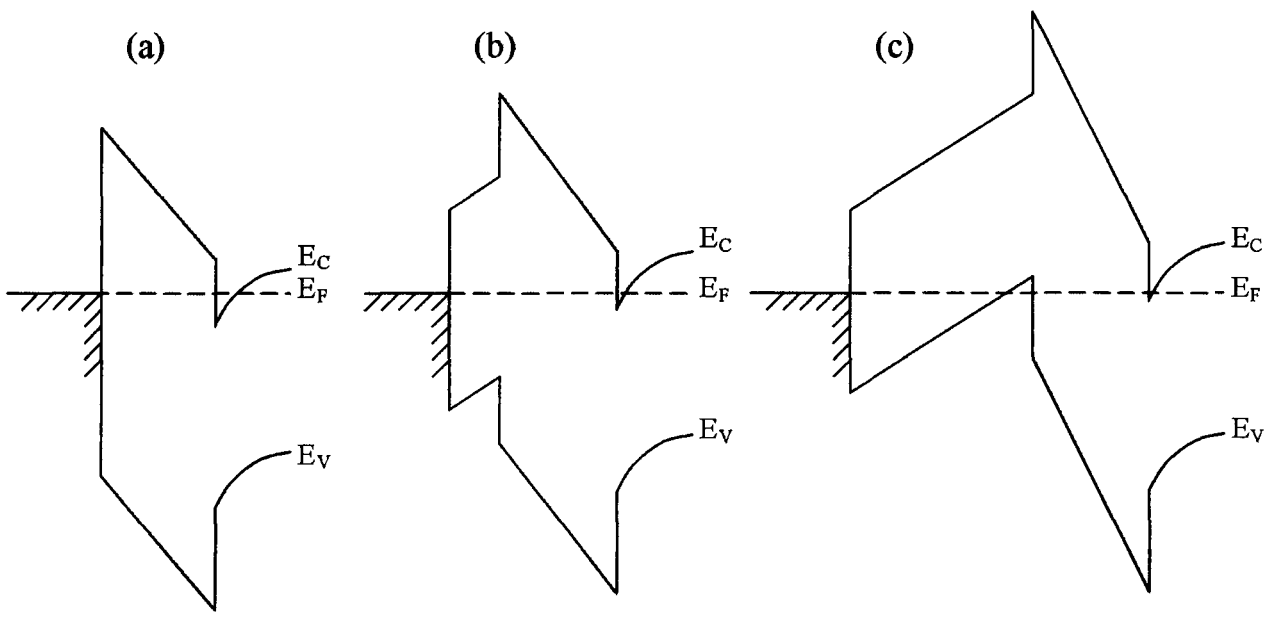


Figure 6.2 – Schematic representation of band structure for an AlGaN/GaN HFET using various thicknesses of GaN capping layer; (a) shows no cap, (b) shows a thin GaN cap and (c) shows a thick GaN cap and a resultant 2DHG [12]. Note the reduction in 2DEG concentration with increasing cap thickness.

As the capping layer thickness is increased the valence band will approach the Fermi level. Once the valence band meets the Fermi level it can be assumed the bands will

then become effectively pinned and any increase in field due to further increases in cap thickness is compensated by the formation of a two-dimensional hole gas (2DHG). Taking this assumption as valid, once this critical thickness is reached the sheet carrier concentration in the 2DEG will remain constant. Since the polarisation resulting from the upper GaN layer ($\sigma_{PZ(cap)}$) is uncompensated, the thickness at which the capping layer creates a 2DHG can be described by equation 6.1.

$$t_{CHG} = \frac{\left(E_{g(AlGaN)} - \phi_B - \Delta E_V\right)\in_{cap}}{\sigma_{PZ(cap)}} \qquad \text{Equation 6.1}$$

Where t_{CHG} is the thickness of GaN required to form a 2DHG, $E_{g(AlGaN)}$ is the band gap of the AlGaN barrier layer, ϕ_B is the metal-semiconductor barrier height, ΔE_V is the valance band discontinuity and $\in_{cap}$ is the product of the permittivity of free space and the relative permittivity of the GaN cap.

In order to develop a model to describe how the number of charge carriers in the 2DEG (n_s) is affected by capping thickness (t_{cap}) it will be assumed the additional field across the barrier layer due to a GaN cap is directly equivalent to applying a bias to the AlGaN layer. The extra capacitance associated with the addition of the GaN cap can be added in series with the AlGaN barrier layer and the amount of charge removed from the 2DEG calculated (equation 6.2). Furthermore, once the thickness of the cap exceeds t_{CHG}, the number of holes in the 2DHG (h_s) can be calculated using equation 6.3.

$$n_s = \left[\frac{\sigma_{PZ(HFET)}}{q} - \frac{\left(\phi_B - \Delta E_C\right)\in_{AlGaN}}{q t_{AlGaN}}\right] - \frac{\sigma_{PZ(cap)}}{q}\left(\frac{t_{cap}\in_{AlGaN}}{t_{AlGaN}\in_{cap}}\right) \qquad \text{for} \quad 0 \geq t_{cap} \leq t_{CHG} \qquad \text{Equation 6.2}$$

$$h_s = \frac{\sigma_{PZ(cap)}}{q} - \frac{\left(E_{g(AlGaN)} - \phi_B - \Delta E_V\right)\in_{cap}}{q t_{cap}} \qquad \text{for} \quad 0 \geq t_{cap} \leq t_{CHG} \qquad \text{Equation 6.3}$$

Where $\sigma_{PZ(HFET)}$ represents the polarisation charge in the uncapped structure, q is the charge on an electron ($1.602\times10^{-19}C$), ΔE_C is the conduction band discontinuity, ϵ_{AlGaN} is the product of the permittivity of free space and the relative permittivity of the AlGaN and t_{AlGaN} is the thickness of the AlGaN layer.

Using this model the number of electrons contained in the 2DEG can be determined for varying GaN cap thickness, AlGaN thickness and Al concentrations in the barrier. Figure 6.3 shows the results of applying equation 6.2 for a GaN/$Al_{0.32}Ga_{0.68}$N/GaN heterostructure with a 20nm thick barrier. The barrier height between metal and semiconductor was assumed to be constant at 1 eV, the conduction band discontinuity was 0.45 eV and the relative permittivity of the GaN and AlGaN was 9.5 and 9.34 respectively [13]. The polarisation charge for the AlGaN and GaN cap was calculated to be -2.88×10^{-6} Ccm^{-2} and 2.88×10^{-6} Ccm^{-2} respectively [14]. Experimental data presented by Heikman et al [12] was used to test the validity of the presented models and are compared in figure 6.3. Both sets of results show reasonable agreement with a decreasing number of electrons in the channel for increasing cap thickness which saturates for thicker GaN layers. For these thicker caps a small difference between calculated and experimental values is observed. The reason for the discrepancy is believed to be related to the unintentional background doping in the GaN cap which will undoubtedly lead to an increase in the position of the Fermi level at the upper GaN/AlGaN interface, reducing the field across the barrier layer and increasing the concentration of electrons in the 2DEG.

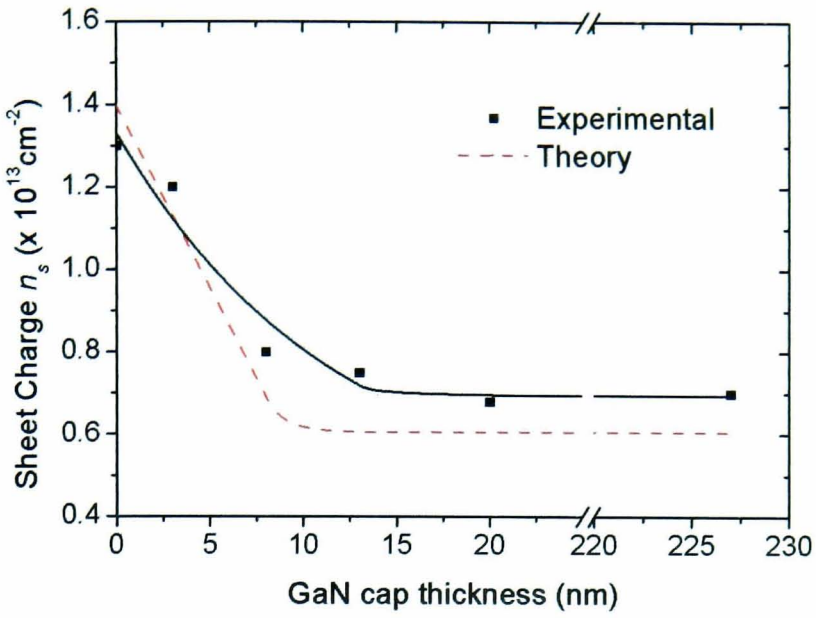


Figure 6.3 – Simulated 2DEG concentration for varying GaN cap thicknesses on a GaN/$Al_{0.32}Ga_{0.68}$N/GaN heterostructure using a 20nm thick AlGaN barrier compared to experimental results in [12].

6.4 Etching GaN/AlGaN Heterostructures

In order to produce gate recessed devices within a production setting it is important to have an etching process which is highly selective between the GaN cap and AlGaN barrier layer. Using a selective etch will remove the need for a timed procedure and the problems which this might cause due to process drift. The wet etch developed in chapter 3 could be used to form the gate recess for the HFET. Employing this method will result in an extremely high selectivity since the ultraviolet (UV) light can be tailored to produce electron hole pairs in the GaN and not the AlGaN [15]. However, the photoresist used as an etch mask does not absorb UV light and consequently no control over the lateral etch will be possible, resulting in a timed process which is susceptible to drift. Consequently this technology is not directly applicable to the fabrication of gate recessed devices and alternative techniques must be investigated.

In the following sections different dry etch recipes are investigated in order to assess their suitability for the fabrication of gate recessed devices. All experiments were

carried out using an inductively coupled plasma (ICP) system which incorporated a vacuum load lock to prevent atmospheric contaminants from affecting the etch. All etching was carried out on a 4 inch Si carrier wafer which was maintained at a constant table temperature of 20°C. Etch depths were measured using a Dektak 3030 ST surface profiler which has a resolution of ±5nm.

6.4.1 Standard $SiCl_4/Cl_2/Ar$ Recipe

Chlorine-based gasses including BCl_3 [16] $SiCl_4$ [17], and Cl_2 [18] have been used extensively to etch GaN-based semiconductors using both ICP and reactive ion etch (RIE) methods. Etching is achieved through the reaction of Cl radicals with Ga to form a $GaCl_x$ species. This volatile component is then sputtered from the surface by ions in a separate step, typically achieved by adding Ar into the plasma. Vartuli et al [19] demonstrated a selectivity of 4:1 between GaN and AlGaN and 10:1 between GaN and AlN using a Cl_2/Ar plasma chemistry in conjunction with ICP etching. Optimisation of the recipe by Smith et al [20] lead to an even higher selectivity of 10:1 between GaN and AlGaN and 38:1 for GaN and AlN. This dissimilarity in etch rates between the two layers was attributed to the difference in bond energies between Ga-N and Al-N which have been shown to be equal to 8.92 and 11.52 eV/atom respectively [21]. These results have recently been questioned by Buttari et al [22] who has proven the existence of oxide layers on the AlGaN surface which are difficult to remove and form a barrier on the semiconductor surface leading to an initial dead time in etching. Accounting for these dead times resulted in no observable differences in etch rates up to aluminium fractions of 35%.

Etching of GaN-based semiconductors at Sheffield is performed using the ICP technique in conjunction with a $SiCl_4/Cl_2/Ar$ recipe at flow rates of 1.5, 15 and 4 standard cubic centimetres per minute (sccm) respectively. The introduction of the $SiCl_4$ into the conventional Cl_2/Ar plasma chemistry acts to attack oxide layers on the surface of the semiconductor and therefore minimises dead time [23]. The ICP power is kept constant at 450W and the chamber is held at a pressure of 4mTorr.

In order to investigate this recipe for the potential fabrication of gate recessed AlGaN/GaN HFETs, bulk 1μm thick GaN and $Al_{0.25}Ga_{0.75}N$ was grown by metal organic chemical vapour deposition (MOCVD) on sapphire substrates. All samples used in the following experiments were patterned with photoresist which acted as an etch mask. The $Cl_2/Ar/SiCl_4$ recipe was used to etch GaN and $Al_{0.25}Ga_{0.75}N$ samples with varying RF powers from 10W to 150W (figure 6.4).

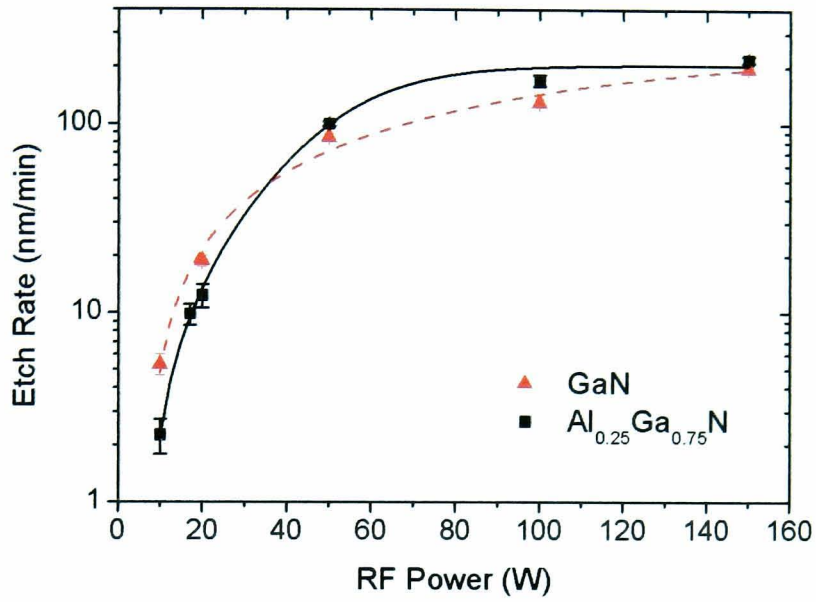


Figure 6.4 – Etch rates for GaN, $Al_{0.25}Ga_{0.75}N$ and AlN using the standard dry etch recipe at Sheffield with varying RF power.

Using the conventional dry etch recipe results in minimal selectivity between GaN and $Al_{0.25}Ga_{0.75}N$ films (1.3:1). By incorporating $SiCl_4$ into the plasma chemistry, oxides present on the semiconductor surface have been eliminated allowing true etch rates for samples to be obtained. The extremely low selectivity observed agrees with the findings of Buttari et al [22] who showed negligible differences in etch rate between the GaN and AlGaN films when using a Cl_2/Ar plasma. Consequently this recipe is not suitable for the fabrication of gate recessed AlGaN/GaN HFETs.

6.4.2 $Ar/Cl_2/O_2$ Recipe

Introducing oxygen into the Cl_2/Ar plasma chemistry has been found to greatly increase selectivity between GaN and AlGaN epilayers [21][4]. During etching of AlGaN the O_2 species reacts with the aluminium to create a thin layer of oxide on the semiconductor surface which is not formed on GaN. The bond strength for aluminium oxide (21.2 eV/atom) is significantly higher when compared to the III-nitrides, resulting in the formation of an etch resistant barrier. Employing this technique has lead to selectivities in the range of 16:1 – 32:1 between GaN and AlGaN samples. Han et al [24] was able to further improve selectivity by introducing N_2 into the recipe which acts as a catalyst for the reaction of oxygen resulting in the highest reported selectivity of 60:1 between GaN and $Al_{0.28}Ga_{0.73}N$.

In order to investigate the use of O_2 containing plasmas the conventional etch recipe was modified to $Cl_2/Ar/O_2$ at flow rates of 30, 10 and 2 sccm respectively with a pressure of 10mTorr [21]. The ICP power was 450W and the RF power was varied from 10W to 100W. While etch rates for the GaN were readily obtained (figure 6.5), exposing $Al_{0.25}Ga_{0.75}N$ samples to the chemistry resulted in no observable etching taking place under any conditions, indicating an extremely high selectivity (>20:1). In order to obtain the true selectivity a ≈500nm thick SiO_2 mask was deposited onto the AlGaN layer and patterned using photoresist in conjunction with a O_2/CHF_3 reactive ion etch (RIE) at flow rates of 5 and 35 sccm, a pressure of 35 mTorr and an RF power of 100 W. Upon ICP etching using the same conditions as employed previously the selectivity was found to be dramatically reduced to ≈10:1 (figure 6.5). This drop in selectivity is attributed to sputtered Si from the SiO_2 mask which getters O_2 contained within the plasma and consequently results in a decrease in selectivity between samples. It is important to note that for $Cl_2/Ar/O_2$-based plasmas investigated in the literature a SiO_2 mask is extensively used in order to enable an accurate figure for selectivity to be obtained. It is therefore proposed that, by using a resist mask, the quoted selectivity between GaN and AlGaN would be dramatically improved.

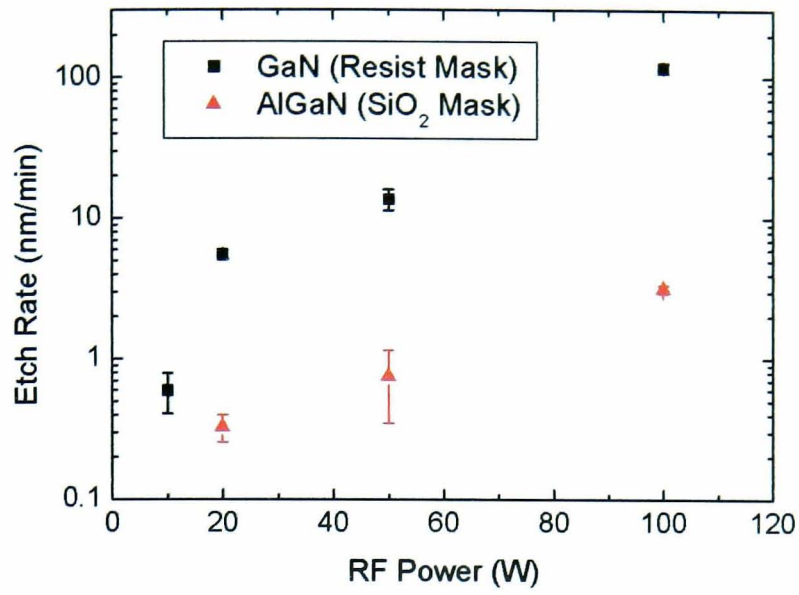


Figure 6.5 – Etch rate for GaN and AlGaN using a $Cl_2/Ar/O_2$ plasma with a resist and SiO_2 mask respectively.

In order to form a gate recess in AlGaN/GaN HFETs it is important that a single self-aligned step is developed. Therefore the plasma must not introduce significant levels of damage into the semiconductor and also must not remove a significant amount of the resist used as an etch mask. Furthermore, to achieve a recess length greater than the length of the gate the resist profile must also be maintained during etching. Since PMMA resist is typically used in the fabrication of sub-micron gates in AlGaN/GaN HFETs the etch rate for the PMMA using the $Cl_2/Ar/O_2$ recipe was investigated using a range of RF powers and is compared to the etch rates for GaN (figure 6.6).

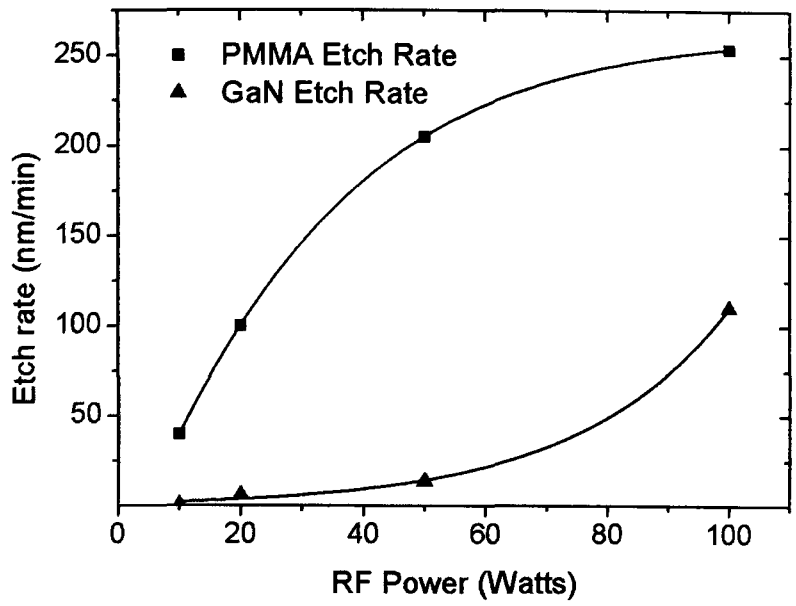


Figure 6.6 – Etch rates for PMMA and GaN using the $Cl_2/Ar/O_2$ recipe.

The selectivity of PMMA:GaN is found to increase with increasing RF power with the highest value of 0.43:1 at 100W. Typically the GaN capping layer is made thin to minimise the loss of sheet charge concentration in the 2DEG and therefore the corresponding recess depth will also be small. At these high RF powers the etch rate for both the GaN and PMMA are high, resulting in an impractically small etch time making it unsuitable for a gate recessed device. Therefore, the use of lower RF powers where the etch rate for the GaN is reduced giving a more controllable rate is advantageous. Under these conditions the selectivity between PMMA and GaN is extremely small. Since a self-aligned process is required the profile of the PMMA is of great importance and loss of this layer will degrade the efficiency of the HFET when operated under large signal high frequency operation. Consequently the O_2-based recipe is not suitable for the fabrication of the self-aligned gate recessed device.

6.4.3 $SiCl_4/SF_6$ Recipe

Employing both Ar and O_2 in the plasma chemistry will lead to the rapid consumption of the resist mask which is unsuitable for the fabrication of a self-aligned gate recess HFET. Alternative recipes which do not include these components must be

considered. The $SiCl_4/SF_6$ recipe has been used extensively in the AlGaAs/GaAs material system [25] however, a comprehensive study of etching using AlGaN/GaN structures has yet to be presented. By incorporating SF_6 into the plasma recipe the obtained selectivity between GaAs and AlGaAs is achieved through the reaction of fluorine with aluminium contained within the AlGaAs material which forms a layer of AlF_3 on the surface and acts as an etch resistant barrier.

In order to investigate the use of this recipe for gate recessed devices bulk GaN and $Al_{0.25}Ga_{0.75}N$ samples were etched using $SiCl_4$ and SF_6 at flow rates of 20 and 5sccm respectively at an ICP power of 450W. Both the RF power and pressure was varied from 50 to 100W and 20 to 50mTorr respectively. Etch rates for both GaN and AlGaN samples are shown in figure 6.7a and b respectively. The corresponding selectivity between samples is shown in figure 6.8. Using energy dispersive x-ray (EDX) analysis in conjunction with a scanning electron microscope (SEM) to confirm the formation of the AlF_3 layer was found to be problematic. The penetration depth of electrons into the semiconductor when using the SEM will be significantly greater when compared to the thin interfacial layer of AlF_3 which is expected to be only a few mono-layers thick. Therefore any fluoride signal from the EDX analysis will be masked by noise in the instrument.

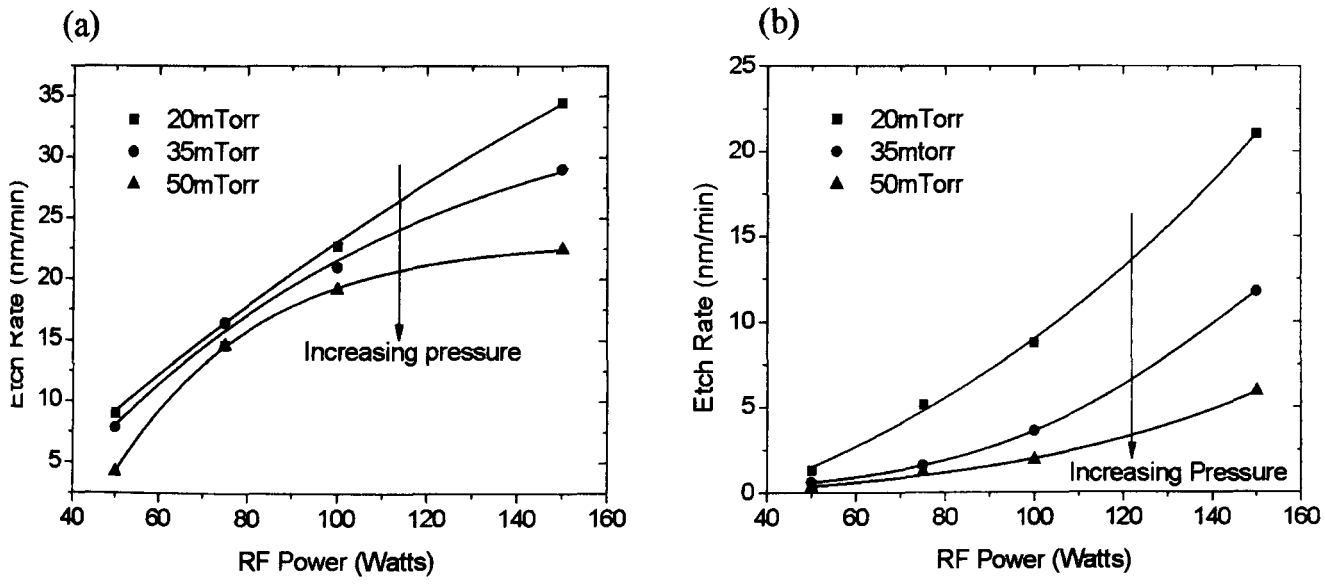


Figure 6.7 – Etch rates for (a) GaN and (b) AlGaN using a $SiCl_4/SF_6$ recipe

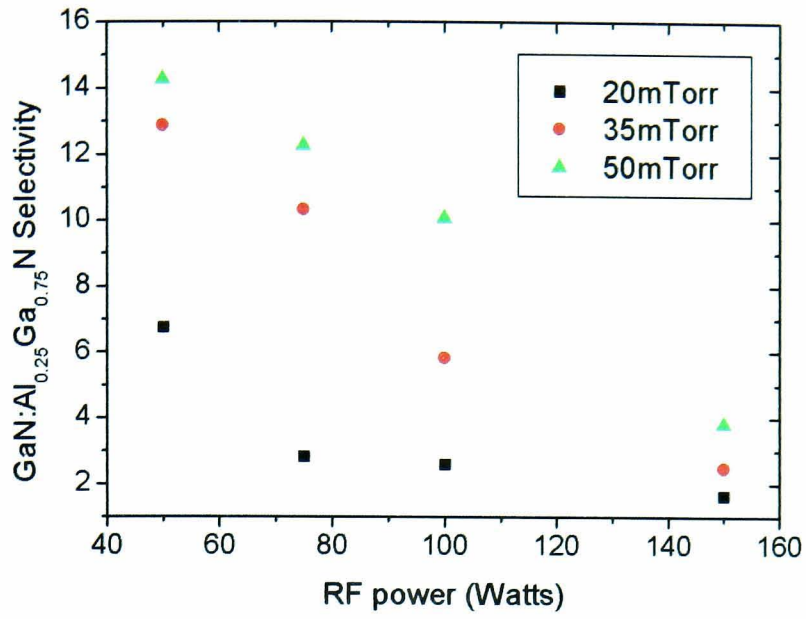


Figure 6.8 - GaN:AlGaN selectivity using the $SiCl_4/SF_6$ recipe

The GaN:AlGaN selectivity was found to be relatively low when compared to the $Cl_2/Ar/O_2$ recipe with the maximum found to be 14:1 when etching at an RF power of 50W and a pressure of 50mTorr. The reduction in selectivity for increasing RF power is attributed to enhanced sputtering of the induced Al-F film at the surface of the AlGaN layer. Under these high power RF conditions it is believed the etch mechanism is dominated by physical ion bombardment. As the RF power is reduced the selectivity improves, indicating a transition to a more chemical etching mechanism. From figure 6.8 it can be seen that in addition to reducing the RF power, the selectivity can also be controlled by altering the pressure in the ICP chamber. As the pressure is increased the mean free path of incident ions in the plasma is reduced and as a result their mobility is also decreased. Therefore, incident ions impinging on the AlGaN surface have less energy, preventing the removal of the etch resistant barrier layer. Consequently, etching under high pressure conditions and at reduced RF powers will lead to increased selectivity between GaN and AlGaN films.

The etch rate for PMMA compared to GaN is shown in figure 6.9. The removal of the etch mask at low RF power is considerably reduced. When etching at 50W the selectivity between the PMMA and GaN has been increased by a factor of 4 when

compared to the $Cl_2/Ar/O_2$ recipe making it more suitable for the fabrication of gate recessed AlGaN/GaN HFETs.

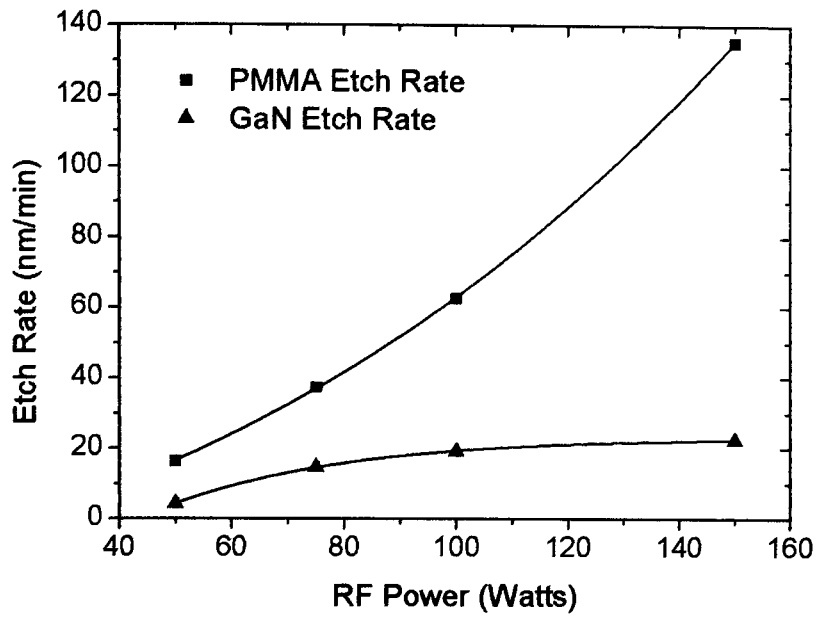


Figure 6.9 – Etch rates for PMMA and GaN using the $SiCl_4/SF_6$ recipe.

In order to quantify the damage induced from the recess etch and also confirm the selectivity between the GaN and AlGaN films, Schottky diodes were fabricated using HFET material with a 50nm undoped GaN cap. After depositing ohmic contacts on top of the GaN a recess was formed using the optimised $SiCl_4/SF_6$ recipe with flow rates of 20 and 5 sccm respectively at a pressure of 50mTorr. The ICP and RF powers used were 450 and 50W respectively. Samples were pre-treated using ammonia:deionised (DI) water (1:9) for a period of 5 minutes prior to etching to remove native oxide on the semiconductor surface which may result in dead times. The rectifiers were then etched for a period of 30 to 60 minutes using ICP which would result in a 200-600% over-etch time. Finally Ni/Au was deposited onto the recessed surface. The results for these experiments are compared to a rectifier formed without employing a recess and also a Schottky diode fabricated on a standard un-capped AlGaN/GaN structure (figure 6.10).

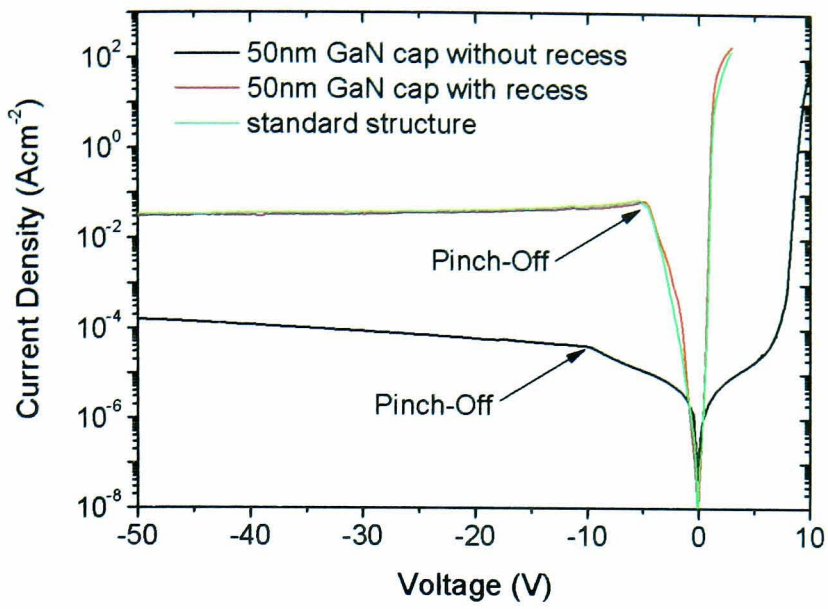


Figure 6.10 – I-V characteristics for a recessed GaN/AlGaN/GaN Schottky diode compared to a conventional AlGaN/GaN rectifier.

Schottky diodes formed on the 50nm GaN capped HFET material without recessing exhibited extremely low leakage currents when compared to conventional devices. Using a GaN cap is found to modify the piezoelectric and spontaneous polarisation in the structure which increases the effective barrier height for the material (figure 6.2) leading to a reduction in leakage current. This is confirmed when observing the diode in the corresponding forward direction which shows a greatly reduced current for a given voltage when compared to the standard structure. Furthermore, the pinch-off voltage for the un-etched capped device is found to be relatively high at ≈10 volts and is attributed to an increase in the distance between the Schottky and channel. Etching through the 50nm GaN cap using the optimised selective etch recipe was found to reduce the pinch-off voltage to ≈6 volts which is consistent with a reduced distance between the rectifying metal and channel. This value is found to coincide with the pinch-off for the standard HFET structure. Both I-V characteristics for recessed and non-recessed devices were almost coincident. This shows the etch was successful in uncovering the AlGaN film and the plasma chemistry introduced minimal damage into the device. It is believed the formation of the AlF_3 layer on the AlGaN surface acted not only as an etch resistant barrier but also formed a protective covering on the

surface of the semiconductor which prevented ion induced damage once the barrier layer was exposed. In the forward direction both etched and standard diodes showed almost identical characteristics demonstrating the Schottky barrier height on the semiconductor surface is unaffected by the plasma etch. Breakdown voltages for the un-recessed 50nm GaN capped material were measured at ≈430 volts. After etching, the breakdown reduced only very slightly to ≈410 volts. It is important to note a flash-over effect has been observed when operating devices at these high bias voltages and consequently these values may not reflect the true breakdown of the component [26]. This provides further evidence the plasma chemistry used to form the recessed structure has introduced minimal damage on the semiconductor surface. The results of these experiments consequently show the $SiCl_4/SF_6$ etch recipe will be extremely useful in the fabrication of self-aligned gate recessed AlGaN/GaN HFETs.

6.5 Conclusions

Using simulations it is shown that a gate recessed AlGaN/GaN HFET will exhibit reduced current collapse and knee walkout effects when operated under high power RF conditions due to the reduction in electric field at the un-recessed surface. A GaN capping layer is advantageous since it will lead to reduced parasitic resistances associated with the drain and source, however the sheet charge density in the 2DEG will be reduced. For the first time a simple model has been presented to illustrate how the thickness of the GaN cap will affect the 2DEG concentration. Comparison of the developed model to experimental results is found to give reasonably good agreement. For relatively thick caps, where the charge in the 2DEG saturated, the model was found to be less accurate. This was attributed to the background n-type doping in the GaN layer.

In order to fabricate a self-aligned gate recessed device different dry etch recipes have been investigated. O_2-based recipes were found to have the highest selectivity between GaN and AlGaN films (>20:1) however, the mask was found to have a significant affect on the etch rate. Using a SiO_2 mask resulted in significantly reduced selectivity due to the gettering of O_2 by sputtered Si from the mask. This has yet to be identified in the literature and may lead to increased selectivities between GaN and AlGaN films. Despite the high selectivity, the use of O_2 and Ar in the plasma lead to

the rapid removal of the PMMA resist making it un-suitable in the fabrication of gate recessed devices. An alternative $SiCl_4/SF_6$ recipe was subsequently developed which had a reduced selectivity of 14:1 however, etching of the PMMA mask was reduced by a factor of 4 when compared to the O_2-based recipe making it more appropriate for the fabrication of a self-aligned gate recessed device. Diodes fabricated using the $SiCl_4/SF_6$ recipe showed minimal differences in characteristics when compared to rectifying diodes fabricated on standard AlGaN/GaN material. This showed negligible damage is introduced on the AlGaN surface and is attributed to the formation of the AlF_3 layer which may prevent ion induced damage on the barrier surface. This is the first systematic development of a $SiCl_4/SF_6$ based recipe for the AlGaN/GaN material system.

6.6 References

[1] *F. Ali, A. Gupta "HEMTs & HBTs: Devices, fabrication and circuits" Boston, Artech House, pp 3-4, 1991*

[2] *Nidhi, T. Palacios, A. Chakraborty, S. Keller, U.K. Mishra "Study of impact of access resistance on high-frequency performance of AlGaN/GaN HEMTs by measurement at low temperature" IEEE Electron Device Letters, Vol. 27, No. 11, pp 877-880, 2006*

[3] *T. Palacios, S. Rajan, A. Chakraborty, S. Heikman, S. Keller, S.P. DenBaars, U.K. Mishra "Influence of the dynamic access resistance in the g_m and f_T linearity of AlGaN/GaN HEMTs" IEEE Transactions on Electron Devices, Vol. 52, No. 10, pp 2117-2123, 2005*

[4] *W.K. Wang, Y.J. Li, C.K. Lin, Y.J. Jen, G.T. Chen, J.I. Chyi "Low damage, Cl_2-based gate recess Etching for 0.3-μm gate-length AlGaN/GaN HEMT fabrication" IEEE Electron Device Letters, Vol. 25, No. 2, pp 52-54, 2004*

[5] *J. Burm, W.J. Schaff, G.H. Martin, L.F. Eastman, H. Amano, I. Akasaki "Recessed gate GaN MODFETs" Solid-State Electronics, Vol. 41, No. 2, pp 247-250, 1997*

[6] *A. Kuliev, V. Kumar, R. Schwindt, D. Selvanathan, A.M. Dabiran, P. Chow, I. Adesida "0.15 μm gate-length AlGaN/GaN HEMTs with varying gate recess length" Solid-State Electronics, Vol. 47, No. 1, pp 117-122, 2003*

[7] *L. Shen, T. Palacios, C. Poblenz, A. Corrion, A. Chakraborty, N. Fichtenbaum, S. Keller, S.P. DenBaars, J.S. Speck, U.K. Mishra "Unpassivated high power deeply recessed GaN HEMTs with a fluorine-plasma surface treatment" IEEE Electron Device Letters, Vol. 27, No. 4, pp 214-216, 2006*

[8] *Y.F. Wu, A. Saxler, M. Moore, R.P. Smith, S. Sheppard, P.M. Chavarkar, T. Wisleder, U.K. Mishra, P. Parikh "30-W/mm GaN HEMTs by field plate optimization" IEEE Electron Device Letters, Vol. 25, No. 3, pp 117-119, 2004*

[9] *S. Karmalkar, U.K. Mishra "Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate" IEEE Transactions on Electron Devices, Vol. 48, No. 8, pp 1515-1512, 2001*

[10] *Y. Okamoto, Y. Ando, T. Nakayama, K. Hataya, H. Miyamoto, T. Inoue, M. Senda, K. Hirata, M. Kosaki, N. Shibata, M. Kuzuhara "High power recessed-*

gate AlGaN-GaN HFET with field-modulating plate" IEEE Transactions on Electron Devices, Vol. 51, No. 12, pp 2217-2222, 2004

[11] J.S. Moon, S. Wu, D. Wong, I. Milosavljevic, A. Conway, P. Hashimoto, M. Hu, M. Antcliffe, M. Micovic "Gate-recessed AlGaN-GaN HEMTs for high-performance millimetre-wave applications" IEEE Electron Device Letters, Vol. 26, No. 6, pp 348-350, 2005

[12] S. Heikman, S. Keller, Y. Wu, J.S. Speck, S.P. DenBaars, U.K. Mishra "Polarisation effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures" Journal of Applied Physics, Vol. 93, No. 12, pp 10114-10118, 2003

[13] O. Ambacher, J. Smart, J.R. Shealy, N.G. Weimann, K. Chu, M. Murphy, W.J. Schaff, L.F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, J. Hilsenbeck "Two-dimensional electron gases induced by spontaneous and piezoelectric polarisation charges in N- and Ga-face, AlGaN/GaN heterostructures" Journal of Applied Physics, Vol. 85, No. 6, pp 3222-3233, 1999

[14] F. Bernardini, V. Fiorentini, D. Vanderbilt "Spontaneous polarisation and piezoelectric constants of III-V nitrides" Physical Review B, Vol. 56, No. 16, pp R10024-R10027, 1997

[15] R.T. Green, W.S. Tan, P.A. Houston, T. Wang, P.J. Parbrook "Investigations on electrode-less wet etching of GaN using continuous ultraviolet illumination" Journal of Electronic Materials, Vol. 36, No. 4, 2007

[16] M.E. Lin, Z.F. Fan, Z. Ma, L.H. Allen, H. Morkoç "Reactive ion etching of GaN using BCl_3" Applied Physics Letters, Vol. 64, No. 7, pp 887-888, 1994

[17] I. Adesida, A. Mahajan, E. Andideh, M. Asif Khan, D.T. Olsen, J.N. Kuznia "Reactive ion etching of gallium nitride in silicon tetrachloride plasmas" Applied Physics Letters, Vol. 63, No. 20, pp 2777-2779, 1993

[18] H. Cho, C.B. Vartuli, C.R. Abernathy, S.M. Donovan, S.J. Pearton, R.J. Shul, J. Han "Cl_2-based dry etching of the AlGaInN system in inductively coupled plasmas" Solid-State Electronics, Vol. 42, No. 12, pp 2277-2281, 1998

[19] C.B. Vartuli, S.J. Pearton, J.W. Lee, A.Y. Polyakov, M. Shin, D.W. Greve, M. Skronowski, R.J. Shul, "Electron cyclotron resonance plasma etching of AlGaN in Cl_2/Ar and BCl_3/Ar plasmas" Electrochemical Society Interface, Vol. 144, No. 6, pp 2146-2149, 1997

[20] S.A. Smith, C.A. Wolden, M.D. Bremser, A.D. Hanser, R.F. Davis, W.V. Lampert "High rate and selective etching of GaN, AlGaN, and AlN using inductively coupled plasma" Applied Physics Letters, Vol. 25, No. 22, pp 3631-3633, 1997

[21] J.M. Lee, K.M. Chang, I.H. Lee, S.J. Park "Highly selective dry etching of III nitrides using an inductively coupled $Cl_2/Ar/O_2$ plasma" Journal of Vacuum Science and Technology B, Vol. 18, No. 3, pp 1409-1411, 2000

[22] D. Buttari, A. Chini, T. Palacios, R. Coffie, L. Shen, H. Xing, S. Heikman, L. McCarthy, A. Chakraborty, S. Keller, U.K. Mishra "Origin of etch delay time in Cl_2 dry etching of AlGaN/GaN structures" Applied Physics Letters, Vol. 83, No. 23, pp 4779-4781, 2003

[23] E. Zhirnov, S. Strpanov, W.N. Wang, Y.G. Shreter, D.V. Takhin, N.I. Bochkareva "Influence of cathode material and $SiCl_4$ gas on inductively coupled plasma etching of AlGAN layers with Cl_2/Ar plasma" Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films, Vol. 22, No. 6, pp 2336-2341, 2004

[24] Y. Han, S. Xue, W. Guo, Y. Luo, Z. Hao, C. Sun "Highly selective dry etching of GaN over AlGaN using inductively coupled $Cl_2/N_2/O_2$ plasmas" Japanese Journal of Applied Physics, Vol. 42, No. 10A, pp L1139-L1141, 2003

[25] S. Salimian, C.B. Cooper, R. Norton, J. Bacon "Reactive ion etch process with highly controllable GaAs-to-AlGaAs selectivity using SF_6 and $SiCl_4$" Applied Physics Letters, Vol. 51, No. 14, pp 1083-1085, 1987

[26] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, M. Asif Khan "The 1.6-kV AlGaN/GaN HFETs" IEEE Electron Device Letters, Vol. 27, No. 9, pp 716-718, 2006

7 Conclusions and Recommendations for Future Work

Conclusions

Fabrication techniques for both AlGaN/GaN heterostructure bipolar transistors (HBTs) and heterostructure field effect transistors (HFETs) have been developed. Wet etching of GaN has been exploited in bulk material and can be used to produce smooth surface morphologies when etching under conditions of high ultra-violet (UV) light intensity and low KOH solution concentrations. In order to obtain sufficiently high etch rates catalytic masks which cover the majority of the sample surface are required. Etching bulk material with solution concentrations of 0.005M KOH and 0.1M $K_2S_2O_8$ in conjunction with a UV light intensity of 70mWcm^{-2} produced surfaces with 1.7nm root mean square (RMS) roughness. Fabricating Schottky diodes from this material showed significantly reduced damage when compared to conventionally dry etched diodes. The selectivity of the wet etch was exploited to access buried p-type layers and form p-n diodes. Due to the significant reduction in damage at the semiconductor surface excellent p-type ohmic contacts were obtained which were superior to those formed on dry etched surfaces. Diodes fabricated using the wet etch technique exhibited ideallity factors of ≈1.6 demonstrating the value of this technology for the fabrication of devices such as n-p-n AlGaN/GaN HBTs.

Novel AlGaN/GaN HBT structures based on a collector-up approach have been investigated. By inverting the standard collector-down devices the critical emitter-base junction can be grown without interruption reducing the incorporation of

interfacial states at the interface and improving the quality of the junction leading to transistors with higher gains. The majority of n-p-n transistors did not show common emitter characteristics due to the high leakage currents at the base-collector junction. However a working device was demonstrated which exhibited a gain of 0.13. Operating the device in reverse with the collector acting as the emitter resulted in a decrease in gain indicating the quality of the re-grown interface was inferior to the lower emitter-base junction which was grown without interruption proving the presence of recombination states at the re-growth interface.

To reduce the large leakage currents present in the HBT device a novel Schottky collector HBT was investigated. P-type rectifying contacts formed on an Ar^+ pre-treated surface exhibited ≈3 orders of magnitude reduction in leakage current when compared to an equivalent p-n junction. Using temperature dependent current voltage (I-V) analysis the Schottky barrier height for aluminium deposited on the pre-treated p-GaN was found to be 1.6eV. Fabricating HBTs using this technology resulted in gains of 2×10^{-3}, 2×10^{-5} and 1×10^{-5} for devices with a base thickness of 100, 160 and 250nm respectively. The relatively low gain observed for transistors with a 100nm thick base when compared to the n-p-n devices was attributed to the reduction in conductivity in the p-GaN which resulted in reduced minority carrier injection underneath the collector. Furthermore the idealitly factors for the emitter-base junction were found to be ≈2 indicating recombination at the junction interface which results in a decrease in transistor gain. The novel structure was successful in reducing leakage in the component enabling the observation of common emitter characteristics. Furthermore, emitter-collector leakage for a base thickness of 160 or 250nm was found to be similar to those obtained on dislocation free material.

Using a recently introduced novel test structure bulk and surface leakage components in AlGaN/GaN heterostructures were examined for the first time independently. Temperature dependent I-V characteristics revealed surface traps to have a depth of 200meV below the conduction band. Samples grown at both Sheffield and QinetiQ were found to have bulk trapping states in the AlGaN layer and for devices which exhibited low leakage these states were localised at the Schottky-semiconductor interface. Passivation of the structure with SiN was found to reduce the surface leakage current which is consistent with models of current collapse in the literature for

AlGaN/GaN HFETs. Introducing a CF_4 plasma pre-treatment prior to deposition of a dielectric layer resulted in the removal of contaminants from the surface and the deposition of a thin layer of AlF_3 which acted as a passivating film and reduced surface leakage current. This is the first example of AlF_3 used as a passivation layer in AlGaN/GaN HFETs. Using the pre-treatment resulted in a reduction in barrier height at the un-gated region from 0.45eV to 0.26eV. Upon depositing SiN on top of the pre-treated devices a soft-breakdown was introduced at low voltage which reduced the maximum output power of the component. This was attributed to current flowing through the SiN film at high electric fields which then flowed to areas of reduced barrier height on the AlGaN barrier surface. Using the test structure an optimised CF_4 pre-treatment performed at 40W for a period of 1 minute prior to deposition of SiN was required to maximise the detrimental soft-breakdown.

GaN capping layers can be employed on top of AlGaN/GaN HFETs to reduce parasitic resistances which currently limit device operation at high frequencies. A simple model was presented and showed the 2-dimensional electron gas 2DEG concentration can be substantially reduced by incorporating a cap into the structure. For thicker caps, the sheet charge (n_s) contained within the channel was found to saturate. Comparison of theoretically obtained results to those found in the literature showed good agreement. For thicker caps a small difference between the two results were observed which was attributed to background doping in the cap which pushes the Fermi level closer to the conduction band and opposes the polarisation-induced interface charge. Dry etching techniques were investigated in order to develop a self-aligned gate recess fabrication process. The conventional Cl_2/Ar based process was found to have negligible selectivity between GaN and AlGaN samples. The addition of O_2 into the plasma recipe was found to greatly increase selectivity. Selectivity was found to be heavily dependent on the mask used with a photoresist mask yielding the highest selectivity of >20:1 whist using a SiO_2 mask reduced this figure to ≈10:1. The reason for this is believed to be due to the gettering of O_2 in the plasma by sputtered Si in the mask. Despite the high selectivity the use of O_2 and Ar in the plasma consumed PMMA resist at a high rate making it unsuitable for the fabrication of a self-aligned gate recessed HFET. Consequently a novel $SiCl_4/SF_6$ recipe was developed which showed a reduced selectivity of 14:1 when compared to the O_2-

based recipe. However, the removal of Ar and O_2 from the plasma reduced the etch rate of the PMMA mask making it more suitable for a self-aligned gate recess. Using a 50nm GaN capped AlGaN/GaN HFET structure Schottky diodes were formed using the optimised recipe. Upon comparing devices to rectifying contacts on standard HFET material minimal damage was observed and both I-V characteristics were found to be coincident. It is believed that the formation of the AlF_3 barrier on the AlGaN after the GaN cap was removed prevented ion bombardment and consequently reduced damage on the semiconductor surface.

Recommendations for future development

Recently a method for etching GaN using periodic illumination by UV light has been demonstrated [1]. By shortening the interval of UV irradiation recombination of electron-hole pairs was reduced enabling etching at higher rates when compared to continuous illumination. By incorporating a pulsed UV light source may enable increased etch rates, reduced surface roughness and less dependence on the area of catalytic mask used on the semiconductor surface. Consequently, wet etching experiments using various solution concentrations and UV light intensities should be investigated in conjunction with a chopped UV source with varying frequencies to determine optimum etching conditions for bulk GaN material.

For the n-p-n AlGaN/GaN HBT structures leakage in the component must be minimised in order to produce working devices. To achieve this junction quality must be significantly improved. Using secondary ion mass spectrometry (SIMS) in conjunction with varying growth conditions will enable devices to be grown in the inverted geometry eliminating the need for a re-growth step in the base-collector junction. This has been shown experimentally in this work to greatly increase junction quality. In addition molecular beam epitaxy (MBE) could be used in parallel with metal organic chemical vapour deposition (MOCVD) to determine the optimum growth technology. Further work must concentrate upon improving p-type conduction in the base to reduce base spreading resistance. This could be investigated through the use of co-doping in the base, novel super lattice structures and improved activation efficiencies during post growth annealing to improve hole concentration at room temperature.

For both the n-p-n and Schottky collector HBT structures which take advantage of the inverted geometry a p-type implantation is required underneath the base contacts which extends into the emitter. Devices with this step omitted have been found to suffer from low gains of 0.12 and 2×10^{-3} depending upon the geometry of the device. To assess the effects of ion implantation to form the p-type region through both the base and emitter of the HBT bulk p-type GaN and n-type AlGaN layers will be implanted using both Mg and Mg + P. In order to prevent the degradation of the epitaxial layers during activation of the implanted species different methods of preventing preferential nitrogen loss from the surface will be considered. This will include encapsulating the sample in AlN, wafer-to-wafer annealing and finally annealing the implanted devices under high pressure. Once these studies are completed Hall measurements will be used to assess how carrier concentrations are affected by the implantation. Furthermore Rutherford backscattering (RBS) will be employed to determine how the material quality has been affected by ion implantation and to what degree the activation anneal has restored uniformity in the crystal lattice. Finally once these studies are complete the optimised ion-implantation process can be applied to the HBT geometry developed previously in chapter 4 of this thesis. Using I-V characteristics it will then be possible to show how the implantation step affects gain in the component.

In order to increase gain in the Schottky collector AlGaN/GaN HBT the RF power during the Ar plasma pre-treatment step must be reduced. Preliminary work suggests reducing the RF power to ≈5-10W will reduce the penetration depth of compensating states to ≈30 to 50 nm. This will not compromise the quality of the Schottky diode but will increase conduction in the base in the active part of the component leading to greatly increased gain. The Schottky collector HBT is limited by reduced breakdown voltages when compared to p-n junctions. To improve the devices a new geometry is proposed whereby the Ar pre-treatment is replaced by a second ion implantation step to implant the collector region (figure 7.1). Employing this geometry will allow the base contact region to be made relatively thick reducing the access resistance and decreasing the lateral voltage drop between the extrinsic and active part of the base region. Implanting the collector region to form a p-n junction will result in a greatly enhanced breakdown voltage for the component which will yield superior output powers when compared to the Schottky collector HBT. In order to fabricate this

structure an n-type region must be formed using a Si-implantation into the upper p-type layer. Although this has already been performed in the literature this technology must also be developed at Sheffield. Therefore it is proposed that a series of experiments are performed using Si-implantation into bulk highly doped Mg^+ films. Optimum post implant anneal conditions using an appropriate method to preserve material quality must then be determined. Electrical measurements such as I-V and C-V characteristics can be used in conjunction with transmission electron microscopy (TEM) and SIMS analysis to determine the quality of the junction. The results of this study can be used to specify the appropriate implantation parameters to form the necessary collector region for the inverted HBT. Furthermore the results of this study can also be applied to HFET technology in order to form a localised highly n-type region prior to deposition of the source and drain ohmic contacts which will reduce parasitic access resistances and consequently improve high frequency performance.

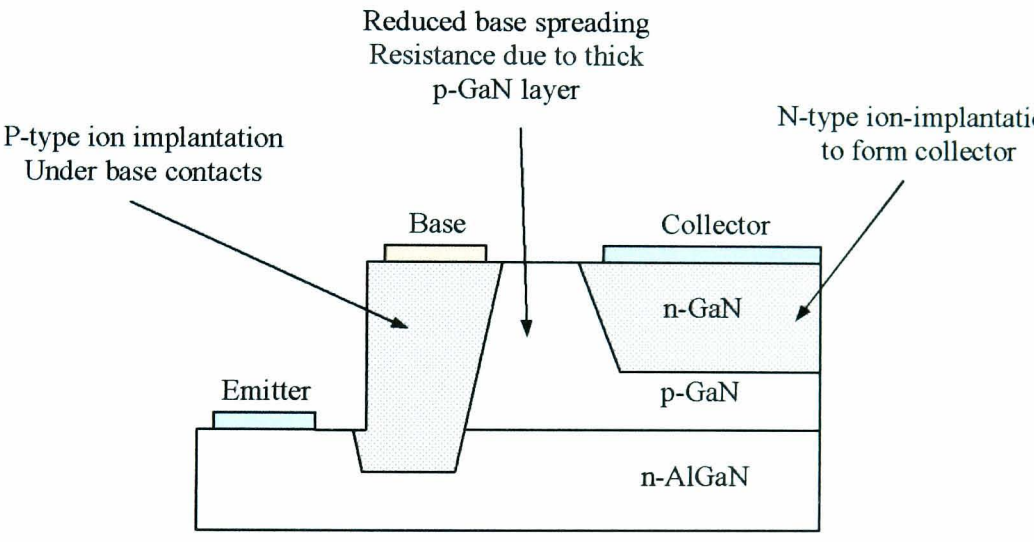


Figure 7.1 – Improved HBT geometry based on the collector-up approach with the collector region formed using a Si-implantation step.

Ultimately however a transferred substrate approach is suggested whereby the layer structure for the HBT is similar to that shown in figure 7.1 and the device is grown using the emitter-down approach to maintain a high quality junction. The collector can then be formed by ion-implantation followed by deposition of metal contacts in a self-aligned step. The feature size for the collector can then be made very small in order to increase high frequency performance. If the sample is grown using a thick

AlN buffer layer to improve material quality [2] the sapphire substrate could be removed using a KOH-based solution and the devices inverted and transferred to a second substrate. Following this the emitter layer can be formed by depositing the appropriate metallization scheme and the previously developed wet etched can then be employed access the p-type base. Employing this step will therefore eliminate the need for a second implantation step underneath the base contacts. The wet etch has been shown to be very anisotropic since the UV light cannot penetrate the metal mask and therefore this process will enable the emitter to be scaled to similar dimensions used for the collector allowing the high frequency performance of the component to potentially rival those of AlGaN/GaN HFETs.

Although the CF_4 pre-treatment has been shown to dramatically reduce current flow at the surface of AlGaN/GaN structures which has consequently significantly reduced current collapse in HFETs, a soft breakdown is introduced when subsequently depositing SiN. In order to incorporate field-plates into the structure to increase breakdown, linearity and maximise output power a dielectric layer must be deposited onto the HFET surface without degrading breakdown voltage. Initially other dielectric layers such as SiO, SiO_2, strontium-fluoride and oxide resists which can be spun onto the sample will be tested to investigate effects on breakdown voltage. Since the soft-breakdown is related to nitrogen vacancies at the AlGaN surface methods of restoring the surface stoichiometry must be investigated. It has been shown in the literature that a nitrogen plasma treatment can restore the chemistry of GaN-based semiconductors. This can be incorporated after the CF_4 exposure and then followed by deposition of the dielectric layer.

The dry etching of GaN/AlGaN/GaN structures has been optimised using a $SiCl_4/SF_6$ plasma recipe. This has been shown not to attack PMMA resist at a high rate when compared to O_2- and Ar-based recipes. However, using the $SiCl_4/SF_6$ recipe developed in chapter 6 other etching parameters should also be investigated. This includes altering the $SiCl_4/SF_6$ ratios and also varying the ICP power during etching. The results of such a study may lead to an increase in both GaN:AlGaN and GaN:PMMA selectivity.

The conditions required to obtain an undercut to create a self-aligned recess whereby the length of the recess is greater than the length of the gate have not been determined. Preliminary results when exposing the PMMA shows the profile can be modified by overexposing the resist to give undercuts of 0 to 200nm. To obtain these undercuts the current recipe must be tested using these resist profiles. Employing TEM and atomic force microscopy (AFM) will enable the correct etching conditions to be obtained. This will enable GaN capped AlGaN/GaN HFETs to be fabricated which have improved performance under large signal RF operation. Once these studies have been completed varying recess depths and lengths can be investigated on HFET devices to optimise high frequency operation using load pull measurements in conjunction with dual pulse biasing to simulate the device performance under RF conditions.

References

[1] J.M. Hwang, K.Y. Ho, Z.H. Hwang, W.H. Hung, Kei May Lau and H.L. Hwang, Superlattices and Microstructures, Vol. 35, pp 45-57, 2004

[2] J. Bai, T. Wang, P. Comming, P.J. Parbrook, J.P.R. David, A.G. Cullis "Optical properties of AlGaN/GaN multiple quantum well structure by using a high-temperature AlN buffer on sapphire substrate" Journal of Applied Physics, Vol. 99, No. 2, pp 023513 1-4, 2006