New processing techniques for large-area electronics

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ABSTRACT

Recent advancements in the semiconductor industry have been driven by the extreme down-scaling of device dimensions enabled by innovative photolithography methods. However, such nano-scale patterning technologies are impractical for large-area electronics primarily due to extremely high cost and incompatibility with large-area processing. Therefore, alternative techniques that are simpler, more scalable and compatible with large-area manufacturing are required. This thesis explores the technological potential of two recently developed patterning techniques namely interlayer lithography (IL) and adhesion-lithography (a-Lith) for application in the field of large-area nano/electronics. The IL method relies on the use of a pre-patterned metal electrode that acts as the mask during back illumination of a photoresist layer followed by a conventional lift-off process step. On the other hand in the a-Lith approach, the surface energy of a patterned metal electrode is modified through the use of surface energy modifiers such as organic self-assembling monolayer (SAM). Following, a second metal is evaporated on the entire substrate. However, because of the present of the SAM, regions of metal-2 overlapping with metal-1 can easily be peeled off with the aid of a adhesive layer (e.g. sticky tape) leaving behind the two metal electrodes in close proximity to each other. Analysis of the resulting structures reveals that inter-electrode distances <20 nm can easily be achieved. The method was then used to develop innovative process protocols for the fabrication of functional self-aligned gate (SAG) transistor architectures. Best performing devices exhibited charge carrier mobility in the range of 0.5-1 cm2/Vs, high current on-off ratio ($\sim 10^4$), negligible operating hysteresis and excellent switching speed. Using the same a-Lith process protocol, low-voltage organic ferroelectric tunnel junction memory devices were also developed by combining the metal-1/metal-2 nanogap electrodes with a ferroelectric copolymer deposited in-between them. Controllable ferroelectric tunnelling was observed enabling the devices' conductivity to be programmed using low biases and hence been used as a non-volatile memory cell. The alternative and highly scalable patterning methods described in this thesis may one day play a significant role on how large-area electronics of the future would be manufactured.

DECLARATION

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I declare that contents of this thesis are my own work, and that contributions from other sources are appropriately acknowledged and referenced.

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CHAPTER 1

Introduction

1.1 Motivation

The "Internet of Things (IoT)" has been receiving increasing attention in recent years due to its huge potential for impacting our daily life in areas spanning from personal health, home appliances, communication and personal entertainment to transportation and energy.[1,2] The IoT is defined as "*A dynamic global network infrastructure with self-configuring capabilities based on standard and interoperable communication protocols where physical and virtual "things" have identities.*" by IoT European Research Cluster, IERC[3] (Figure 1.1). For this reason, significant research activities have been inspired across the world (Figure 1.2). For instance, within the European Union the IoT technology has been developed through programs such as Coordination and Support Action for Global RFID-related Activities and Standardization (CASAGRAS) under 7th Framework Program (FP7)[4], and more recently within the nano electronic research program ENIAC under Horizon 2020[5,6]. In the United States, six main technologies related with IOT were selected and several research programs were financially supported by US research agencies.[7] Similarly, in Asia numerous government driven research programs have recently been initiatted.[8,9] These worldwide activities indicate the momentum IoT has created and hence reflecting its potential.

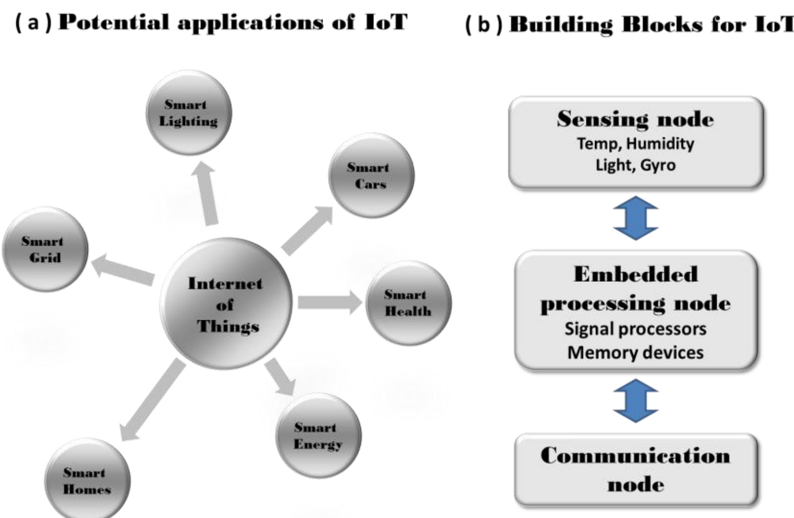
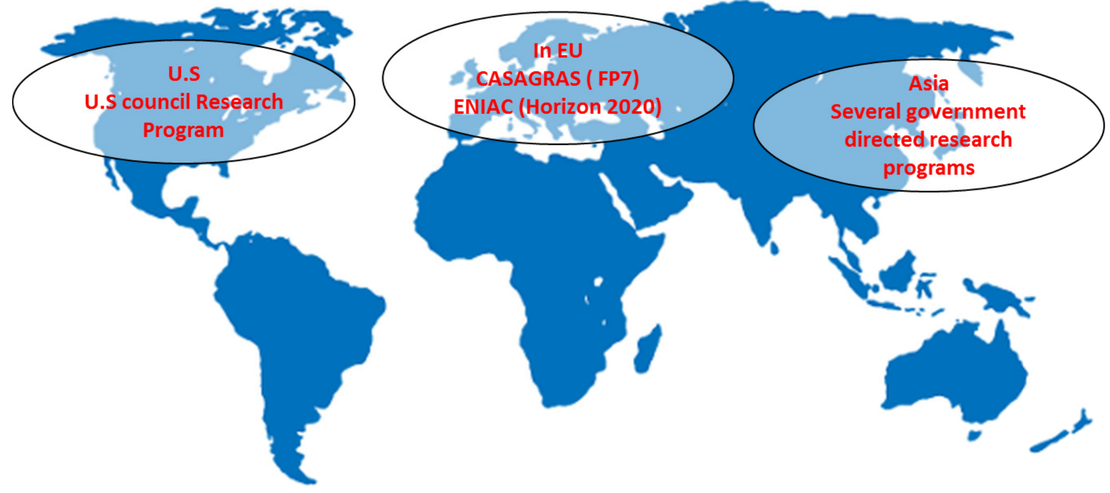


Fig.1.1. (a) Schematic illustration of potential applications of IoT.[1,2] (b) Concept of building blocks of IOT. [10]

The building blocks of IoT are shown in Figure 1.1 and include several units: a sensing node for collecting the information from physical “things”, an embedded processing node for processing the gathered information and transforming into the signal form of internet “things” and a communicating node for transmitting and receiving signals with central controlling units [10,11].



World wide movements for “ Internet of Things ”

Fig.1.2. Global research programs on IoT. [4-9]

For realizing the IoT and successfully implementing it in our everyday life, a low-cost, energy-efficient embedded processing node is required with self-configuring capabilities.[3] Solution-processed semiconducting, insulating and conducting materials have been widely studied and proposed in the past few decades as possible building blocks for the manufacturing of such processing nodes. For example, numerous families of chemically stable organic semiconducting materials have been developed and their electrical performances has been improving steadily.[12,13] Metal oxides semiconducting materials such as zinc oxide, indium oxide and gallium oxide have also emerged with their electrical performances now in par with that of state-of-the-art low-temperature poly silicon transistors[14,15]. Similarly, complementary organics as well as inorganic insulating materials have also been developed and used in numerous large-area electronic applications.[16–19] Electrically conducting materials based on solution-processable metal nanowires and nanoparticle are also being developed as alternatives to conventional vacuum processed electrode materials.[20–24] As a result there is now a consensus that solution-processed materials

poses a number of advantages over vacuum-processed systems in terms of manufacturing cost and could one day enable the much sought widespread adoption of electronic devices and sensors for realising the IoT.[25,26]

In the area of patterning techniques for the manufacturing of active opto/electronic devices, non-photolithographic based pattering methods such as nano-imprint lithography[27,28], inkjet-printing[29–31] and gravure printing[32–34] appear to be the most favourable processes. However, numerous issues associated with these methods have been identified over the years. For example, although spatial resolution down to a few nanometre scales is indeed possible via nano-imprint lithography[27], the cost for fabricating the master itself is very high while the durability of the master remains unproven. Similarly, in the case of inkjet printing, the resolution of the pattern is known to be limited typically in the order of 10 micrometre, while the uniformity of the printed layers suffers from unwanted effects such as coffee stain effect. Therefore, development of alternative patterning methods that are scalable, inexpensive and at the same time compatible with large-area electronics manufacturing, are urgently required.

1.2 Objectives and thesis layout

The key motivation and aim of this study is the development of new processing methodologies and their implementation in large-area electronics and ultimately the IoT. In order to achieve this goal, a modified photo-lithographic patterning method namely Interlayer Lithography (IL) was firstly explored. After establishing the basic process steps of IL, other processing steps such as spin casting of the photoresist and light exposure conditions, were optimized for the manufacturing of reproducible metal patterns. Following, a non-photolithographic method called Adhesion Lithography (a-Lith) was explored for the development of different metal patterns with unique features. These activities are summarized in Chapter 2. In Chapter 3, the new patterning processes were applied for the development of high performance solution-processed self-aligned gate (SAG) thin-film transistors (TFTs). Solution-processed metal oxides semiconductors, namely zinc oxide and indium oxides were combined with high capacitance (high-*k*) dielectric materials such as ion-gel dielectrics and hybrid metal oxide/self-assembled monolayer (SAM) dielectric system to produce low operating voltage TFTs. Fabrication of SAG TFT structure was also attempted via a-Lith in combination with various passive and active materials. Chapter 4 is the last experimental chapter and discusses the development of organic ferroelectric memory device using the pre-

patterned metal electrode nanogap structures developed via a-Lith. Because of their unique nanogap electrode architecture, the devices are able to operate as non-volatile tunnel junction memories rather than conventional ferroelectric capacitors i.e. often seen in devices with nano-gaps >>10 nm. The measured current-voltage characteristics were analysed within the framework of various carrier transport mechanisms, and key conclusions were drawn. Finally, Chapter 5 provides a summary of the work and future outlook.

CHAPTER 2

Background

2.1 Lithography

A variety of patterning methods have been developed within the microelectronics industry for the fabrication of electrode and device nano/microstructures. Among these methods shadow mask lithography is the simplest process. The latter relies on attaching the mask directly on the substrate and depositing the materials though the mask followed by removal of the mask from the substrate (Figure 2.1.1).[38–40] Although, shadow masking suffers from a lot of limitations such as low resolution, alignment inaccuracy and shadow effects, it is widely used in organic electronics because of its simplicity. Additionally, no solvents are involved during patterning, unlike photolithographic methods, hence avoiding issues related to the orthogonalilty of solvents used.[41–43]

Compared to shadow mask, photolithography process consists of several steps.[44–46] Firstly, the pattern is transferred to light-sensitive materials called the *photoresist* (PR) by exposure to light. Next, the deposited layer is etched by wet or dry etching methods using the PR as a protective film. Finally, the residual PR is removed with a liquid resist stripper. The process is illustrated in Figure 2.1.2.

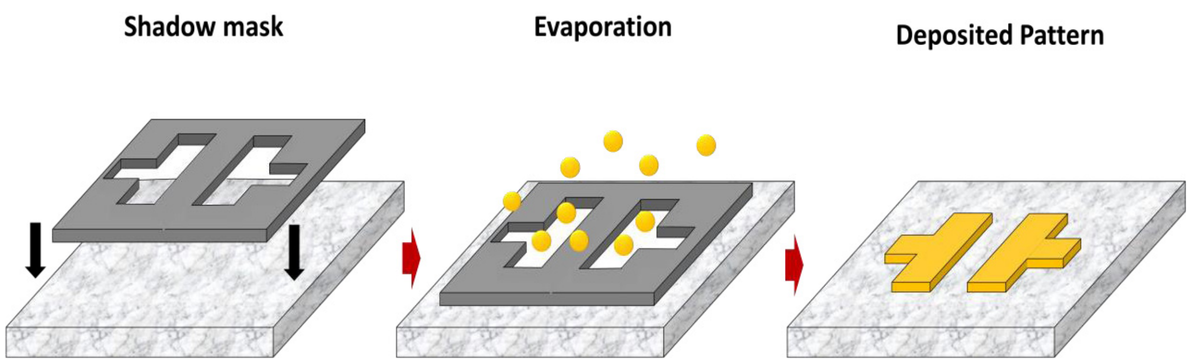


Fig.2.1.1. Schematic process diagrams of shadow mask lithography.

There are two kinds of photoresist; one is a positive-tone PR and the other a negative-tone PR. A photoresist is classed as a positive tone if it becomes more soluble to the developer liquid when exposed to light. Common positive-tone photoresists are based on mixtures of diazonaphthoquinone (DNQ) and novolac resin i.e. a phenol formaldehyde resin. On the other hand, if the photoresist is cross-linked by the exposure of light and becomes

insoluble to the developer, it is classed as a negative tone photoresist. In a negative tone photoresist, cross-linking agents in the PR are activated through exposure to light. The polymers are then cross-linked by a baking step, referred to as a post exposure bake (PEB). Hence, the PR becomes resistant to the developer and the patterned area is obtained. The process parameter of the PEB step such as temperature and time is crucial for the adhesion and resolution of a negative tone PR since the pattern is formed though the cross-linking process. A very common negative photoresist is the epoxy-based photoresist *SU-8,* from *Microchem* and this photoresist was used for IL here. [47,48]

In order to transfer the pattern to the PR layers, the layer is required to be exposed to suitable light. The basic principle of an exposure system is to focus the incoherent and uncollimated light from the source into a uniform and collimated beam on the substrate. Thus, the system is classified by the methods of focusing and irradiating. In the case of a contact system, which is the most primitive exposure system, one lens is used for focusing the light and the photo mask is attached to the substrate. During this step there is a probability of damaging the surface and the mask due to direct attachment of the two. Despite this risk however the contact method can deliver very high resolution patterning. A proximity system uses the same systems as a contact printing, but the mask does not make contact with the substrate. Because of this, the resolution limit of a proximity printing is not as high as the contact printing, so the method is often used for low resolution applications. A projection system uses a multi lens system and is operated in scan and repeat mode. Such systems are widely used in large-area electronics manufacturing. Figure 2.1.3 shows schematics of the contact, proximity and projection systems.[44]

The minimum feature size, *F,* of a device produced by photoresists is dependent on the wave length used during exposure and expressed as:

$$F = 0.5 \ \frac{\lambda}{NA} \tag{2.1}$$

where NA is the numerical aperture of the lens and λ is the wavelength of the light used. Thus higher definition patterns can be obtained by using light sources with shorter wavelength.

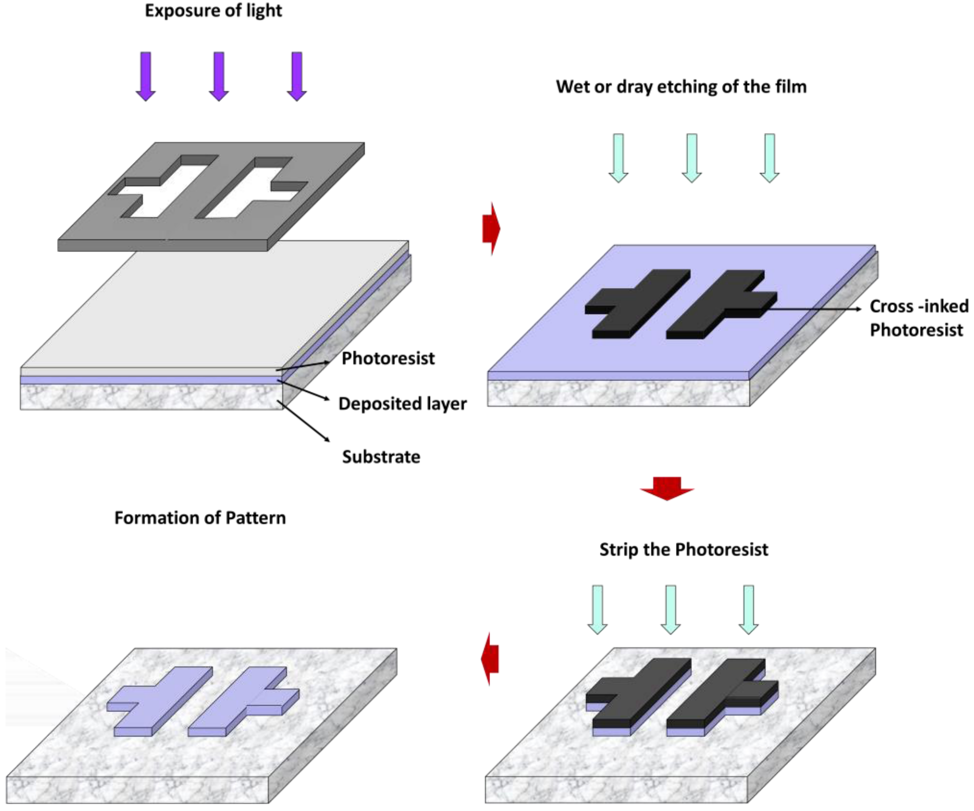


Fig.2.1.2. Schematic diagrams of photolithography based on the negative photoresist.

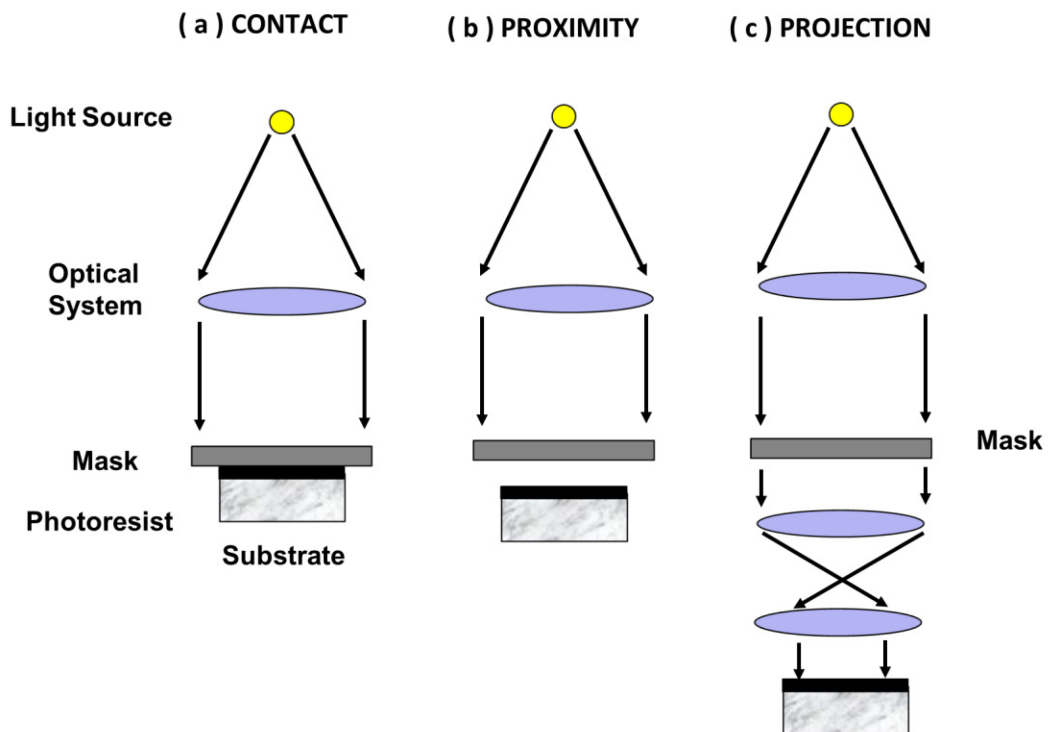


Fig.2.1.3. Schematic diagrams of exposure systems. (a) Contact system. (b) Proximity system. (c) Projection system.

2.2 Device physics of thin-film transistors

A thin-film transistor (TFT) consists of three main components: a semiconductor, an insulator and three metal electrodes.[77–80] The semiconductor is isolated from the metal *gate* (G) electrode by the insulator. Two additional metal electrodes, namely *the source* (S) and *the drain* (D) are in contact with semiconductor. The distance between the S and D electrodes is the so-called channel length (L) while the length of the S-D electrodes defines the so-called channel width (W). Figure 2.2.1 shows several different TFT architectures according to the location of electrodes, an insulator and a semiconductor: (a) bottom-gate bottom-contact, (b) bottom-gate top-contact, (c) top-gate bottom-contact, and (d) top-gate/top-contact.[79] Despite the dramatic differences between the various TFT architectures, their operation is governed by exactly the same principles because charges accumulate at the semiconducting layer near the dielectric layer when biased thorough the gate electrode.

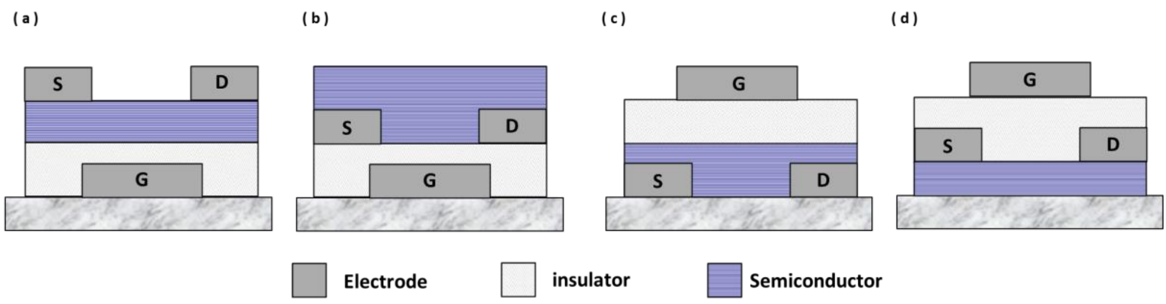


Fig.2.2.1. Schematic representations of field-effect transistor architectures. (a) bottom-gate top-contact. (b) bottom-gate bottom-contact. (c) top-gate bottom-contact. (d) top-gate top-contact.

The amount of charge will depend on the dielectric's properties and its geometry and the electrical potential applied. Under suitable conditions a conducting layer of mobile charge carriers, i.e. the conducting channel, is formed in the semiconductor/dielectric interface. Electrons or holes enter the channel from the source and leave at the drain if a voltage is applied also between the source and drain. In this way, the conductance of the channel (i.e. the amount of current) is modulated by the electric field applied at the gate terminal. The ability to modulate large currents through the application of electrostatic gate fields enables use of the TFT as low-power switches in numerous electronic applications.

The current equation for the TFT at low drain-source voltages, V_D, ($V_D \ll V_G - V_T$) is described by the time-dependant model, often called *the charge-control model*.[77–80] The

threshold voltage, V_T is defined as the gate voltage at which current between the source and drain terminals starts to flow. The drain-source current I_D is represented by Equation 2.2, which is related to the total charge in the channel Q_N by the transit time T_{tr}. Assuming the current is dominated by a drift flow and the charge per unit area Q_n regarded as constant with the channel dimension *WL,* the transit time becomes the channel length divided by the drift velocity of the carriers. The drift velocity can be expressed as $\upsilon_d = -\mu_n(V_D - V_S) / L = -\mu_n V_{DS} / L$. Therefore, the drain current at low drain voltages, Equation 2.5, is obtained by substituting Equations 2.3 and 2.4 into Equation 2.2. As a result, for $V_D \ll V_G - V_T$, the drain current is expected to vary linearly with the drain-source voltage V_{DS}[77]:

$$I_D = \frac{-Q_N}{T_{tr}} \tag{2.2}$$

$$T_{tr} = \frac{L^2}{\mu_n V_{DS}} \tag{2.3}$$

$$Q_N = Q_n \mathrm{WL} = \mathrm{C}_i \left[V_G - V_T \right] WL \tag{2.4}$$

$$I_D = \mu_n C_i \frac{W}{L} \left[(V_G - V_T) V_{DS} \right] \tag{2.5}$$

However, if the drain voltage increases, the analysis becomes invalid since the charge per unit area Q_n is affected by the drain-source voltage and becomes variable. The square-law model based on the gradual-channel approximation considers this variability and describes the behaviour using a differential equation.[77] According to this approximation, the distribution of the induced charge, Q_n, can be expressed linearly with channel voltage $V_C(y)$ [Equation 2.6]. Additionally, assuming that drain current only flows along the channel length direction and the channel length is longer than the depletion region at the drain, the incremental channel voltage, dV_C, can be expressed as the product of the drain-source current and incremental resistance *dR* [Equation 2.7] .

$$Q_n = \mathrm{C}_i \left[V_G - V_T - (V_C - V_S) \right] \tag{2.6}$$

$$dV_C = I_D dR = - \frac{I_D dy}{W \mu_n Q_n(y)} \tag{2.7}$$

Then the drain current is obtained by integrating from the source to the drain where V_{DS} is equal to $V_D - V_S$ [Equations of 2.8 and 2.9]:

$$I_D = \frac{-\mu_n W}{L} \int_{V_s}^{V_D} Q_n(V_C) dV_C \tag{2.8}$$

$$I_D = \mu_n C_i \frac{W}{L} \left[(V_G - V_T)V_{DS} - \frac{V_{DS}2}{2}\right] \tag{2.9}$$

Equations 2.8 and 2.9 describe the evolution of channel current with drain voltage in the so-called linear regime. If the drain voltage $V_{DS} > V_G - V_T$, the induced charge becomes negative which is physically unreasonable. In that condition, the drain current starts to pinch off at the end of the channel, which means the end of channel is no longer at y = L but rather at y = L' (where L' is smaller than L). Thus the voltage at which $Q_n \rightarrow 0$ is $V_{DSAT} = V_G - V_T + V_S$ and the drain current is calculated by applying this relation of V_{DSAT} into the Equation 2.9 and expressed as:

$$I_{Dsat} = \mu_n C_i \frac{W}{2L} (V_G - V_T)^2 \tag{2.10}$$

The drain current now becomes independent of the drain voltage, in other words it saturates. This condition, i.e. $V_D \geq V_G - V_T$, is known as the saturation regime.

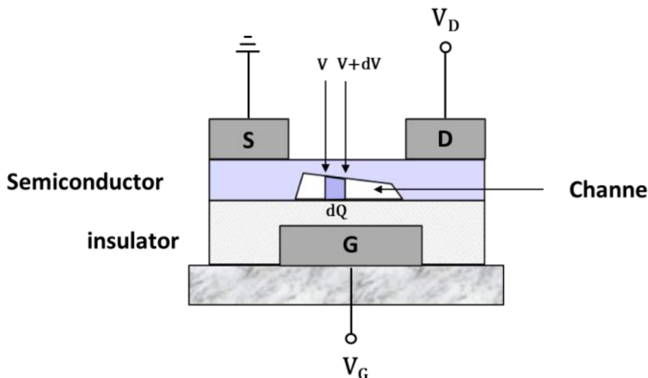


Fig.2.2.2. Cross-sectional view of a bottom-gate, top-contact staggered thin-film transistor.

Typical transfer (I_D versus V_G) and an output (I_D versus V_D) curves measured for an ion-gel gated transistor is shown in Figure 2.2.3. Several important parameters can be extracted from these characteristics. From the transfer curve, the on/off ratio can be deduced by comparing the on and off currents and the hysteresis characteristics is also investigated by comparing the current loops between forward (off to on) and reverse (on to off) sweeps. In addition, the threshold voltages can be identified from the plot of $\sqrt{I_D}$ versus V_G, which should be linear in the saturation regime. The equation is expressed simply by modifying

Equation 2.11 and is given as:

$$\sqrt{I_{Dsat}} = \sqrt{\mu_n C_i \frac{W}{2L}}\ (V_G - V_T) \tag{2.11}$$

The value of carrier mobility can also be deduced from both the linear and saturation regimes using Equations 2.5 and 2.10, respectively:

$$\mu_{LIN} = \frac{1}{C_i V_D} \frac{L}{W} \frac{\partial I_D}{\partial V_G} \tag{2.12}$$

$$\mu_{SAT} = \frac{2}{C_i} \frac{L}{W} \left(\frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \tag{2.13}$$

In general, the performance of the transistor is evaluated by the magnitude of the charge carrier mobility, the on/off channel current ratio, the threshold voltage (the closer to 0 V, the better) and the operating hysteresis (measured between forward and reverse V_G sweeps). Here, these values will also be used as the main figures of merit for investigating the performance characteristics of various TFTs developed.

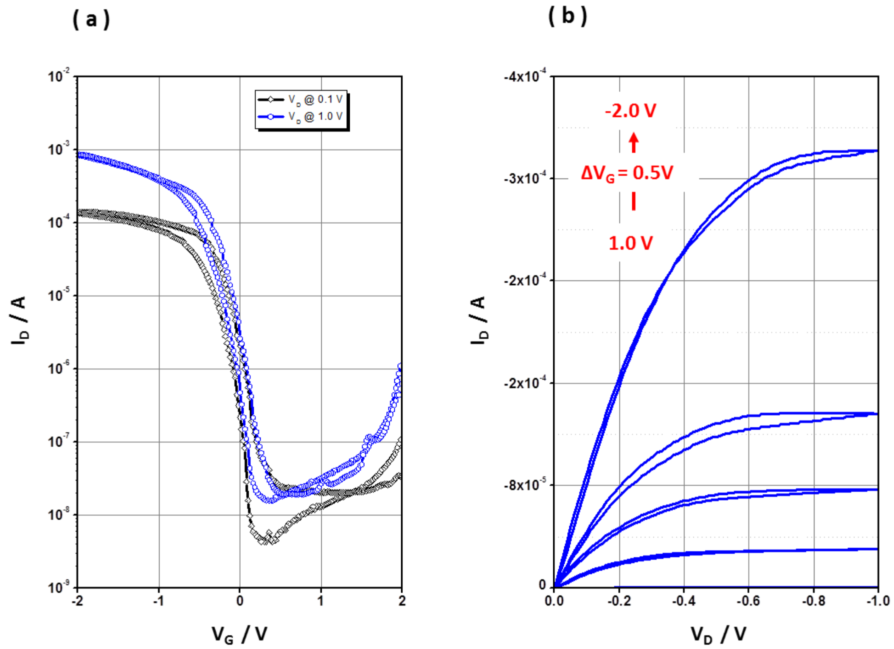


Fig.2.2.3. (a) Linear (V_D = 0.1 V) and saturated (V_D = 1.0 V) transfer characteristics of a top-gate, top-contact TFT with channel width W =1000 µm and channel length L = 100 µm, fabricated with poly 3-hexylthiophene (P3HT) films on ion-gel dielectric. (b) Output characteristics of the ion-gel gated poly 3-hexylthiophene (P3HT) transistor.

One of the most important figures of merits for any transistor technology is the *cut-off frequency*, f_T, of operation. This is because f_T determines the maximum switching speed that the unit device (i.e. the transistor) can be operated and used for designing the logic circuitry. In MOSFET technology, f_T is derived from the small-signal model of the device and experimentally determined by measuring the frequency at which the current-gain of the device decreases to one.[77] In this section, the small-signal model of a MOSFET was modified for a thin-film transistor and the cut-off frequency of the device is introduced. When a DC and a small-signal AC bias are applied to the transistor through the gate electrode, each voltage and current in the circuit has both a DC and small-signal component as illustrated in the Figure 2.2.4. Because the small-signal is considered to be a small perturbation, hence, non-linear components become linear, where superposition can be applied to determine the circuit response. On the basis of this assumption, the total gate-source voltage and total drain-source current can be written as:

$$v_{GS} = V_{GS} + v_{gs},\ i_D = I_D + i_d \tag{2.14}$$

where small letters with large subscripts are total responses, large letters with large subscripts denote DC components and small letters with small subscripts represent the small-signal response.

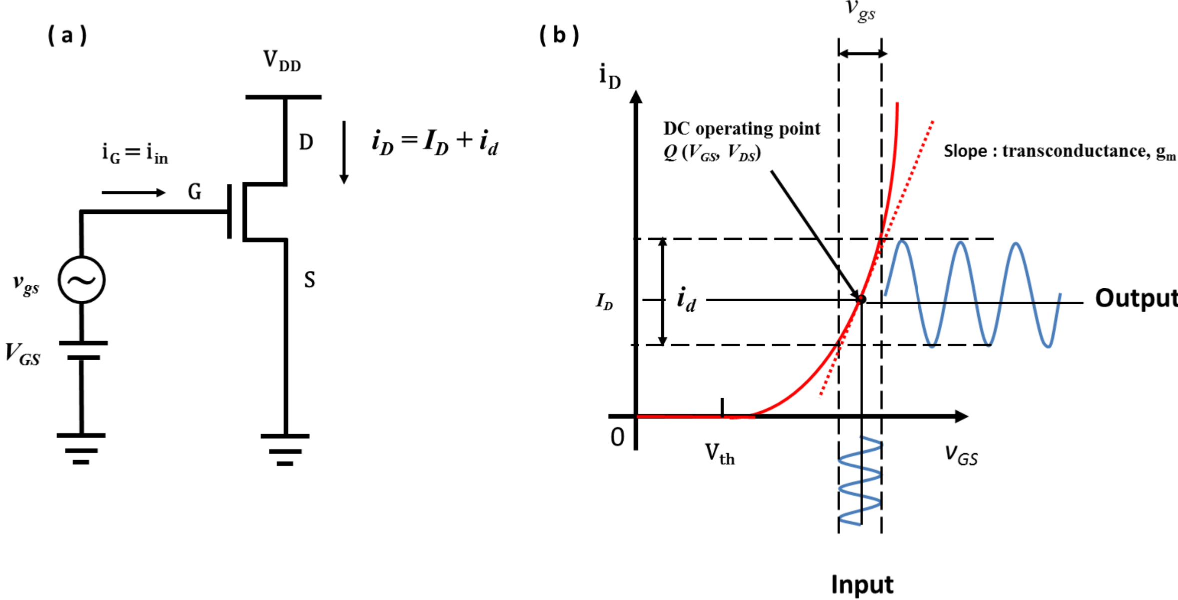


Figure.2.2.4. (a) Schematic of the transistors and the various voltage and current components. (b) DC and small-signal AC components of the transistors.

The relationship of the increment in drain current (i_d) due to an increment in gate-source voltage (v_{gs}) or drain-source voltage (v_{ds}) can be obtained from the first terms of Taylor expansion of the total drain current around the DC operating point, Q (V_{GS}, V_{DS}) and is expressed as:

$$i_D\left(V_{GS} + v_{gs}, V_{DS} + v_{ds}\right) = i_D(V_{GS}, V_{DS}) + \left.\frac{\partial i_D}{\partial V_{GS}}\right|_Q (v_{gs}) + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_Q (v_{ds}) \qquad (2.15)$$

where $i_D(V_{GS}, V_{DS})$ becomes $I_D(V_{GS}, V_{DS})$ because it is a DC component. Therefore, the small-signal response of circuit can be written as:

$$i_d\left(v_{gs}, v_{ds}\right) = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_Q \left(v_{gs}\right) + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_Q (v_{ds}) = g_m v_{gs} + g_0 v_{ds} \qquad (2.16)$$

The first term in Equation 2.16, the small-signal current due to v_{gs}, is defined as the **transconductance, g_m** and the second term relating to v_{ds} as the outputconductance, g_o ($1/r_0$).

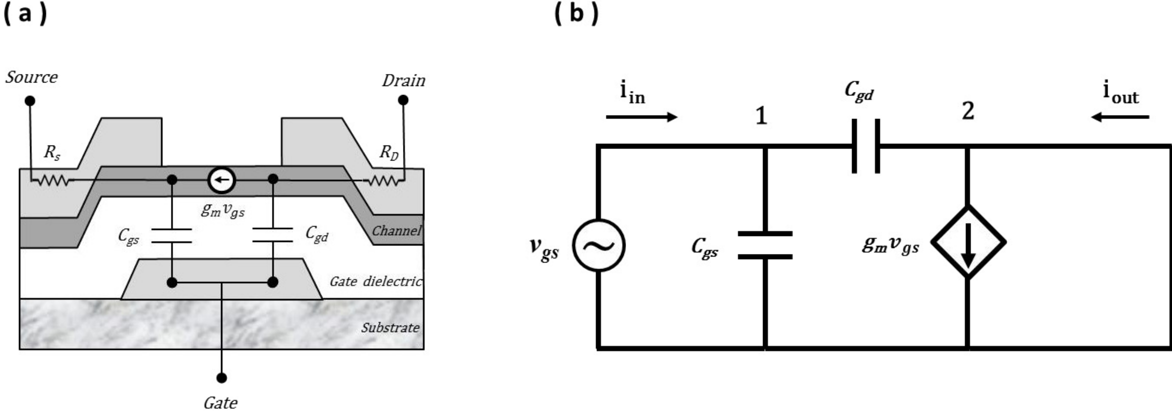


Figure.2.2.5.(a) Device Schematic illustration of a thin-film transistor. (b) Simplified small-signal model of a thin-film transistor.

As shown in the simplified small-signal model of a thin-film transistor in Figure 2.2.5, the input (i_{in}) and output (i_{out}) currents of the circuit can be extracted when considering the circuit at nodes 1 and 2 using:

$$\text{node 1}: i_{in} - v_{gs}j\omega C_{gs} - v_{gs}j\omega C_{gd} = 0 \quad \rightarrow \quad i_{in} = v_{gs}j\omega(C_{gs} + C_{gd}) \qquad (2.17\text{ a})$$

$$\text{node 2}: i_{out} - g_m v_{gs} + v_{gs}j\omega C_{gd} = 0 \quad \rightarrow \quad i_{out} = v_{gs}(g_m - j\omega C_{gd}) \qquad (2.17\text{ b})$$

where C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance and ω is the angular frequency. Then, the current gain (h_{21}) and its magnitude can be written as:

$$h_{21} = \frac{i_{out}}{i_{in}} = \frac{g_m - j\omega C_{gd}}{j\omega\,(C_{gs} + C_{gd})} \tag{2.18 a}$$

$$|h_{21}| = \frac{\sqrt{g^2{}_m + \omega^2 C^2{}_{gd}}}{\omega(C_{gs} + C_{gd})} \tag{2.18 b}$$

According to the operating frequency, the magnitude can be expressed in a simpler form as:

$$|h_{21}| \approx \frac{g_m}{\omega(C_{gs} + C_{gd})} \quad at\ low\ frequency\,(\,\omega \ll g_m\,/\,C_{gd}\,) \tag{2.19 a}$$

$$|h_{21}| \approx \frac{C_{gd}}{(C_{gs} + C_{gd})} \quad at\ high\ frequency\,(\omega \gg g_m\,/\,C_{gd}\,) \tag{2.19 b}$$

When the magnitude of h_{21} becomes unity, the frequency can be written as.

$$\frac{g_m}{\omega_T\,(C_{gs} + C_{gd})} = 1 \tag{2.20 a}$$

$$\omega_T = 2\pi f_T = \frac{g_m}{(C_{gs} + C_{gd})} \tag{2.21 b}$$

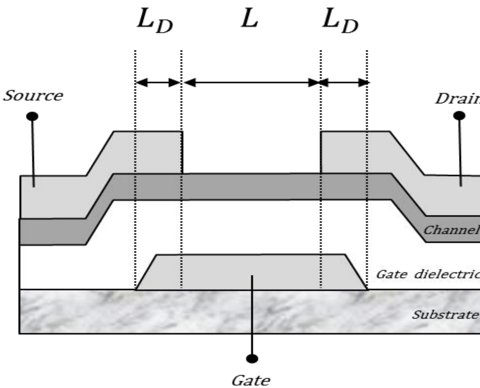
$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.22 C}$$

The higher the value of f_T is, the faster the thin film transistor can operate. Furthermore, the cut-off frequency can be physically interpreted when combined with the capacitances (C_{gs}, C_{gd}) and its transconductance. The capacitances contain not only intrinsic elements but also parasitic elements due to the overlap of the gate and the source and drain electrodes (L_D) as shown in Figure 2.2.6. In the linear regime, the channel is considered to be uniform from the source and drain, so the C_{gs} and C_{gd} is a same value as $1/2C_{ox}WL + C_{ox}WL_D$. In the saturation regime, the channel starts to be pinched off near the drain electrode and it is not assumed to be uniform. Thus, the C_{gs} becomes approximately $2/3C_{ox}WL + C_{ox}WL_D$, while C_{gd} contains only the remaining parasitic capacitance component of $C_{ox}WL_D$. The transconductance is found by differentiating the drain current with respect to V_{GS} and it can be expressed as $\mu_n C_{OX}(W/L)V_{DS}$ in the linear regime and $\mu_n C_{OX}(W/L)(\,V_{gs} - V_{th})$ in the saturation regime, respectively. Therefore, the cut-off frequency in the linear and saturation regime can be written as:

$$f_T = \frac{\mu_n V_{DS}}{2\pi L^2(1 + 2L_D/L)} \quad \text{linear regime} \qquad (2.23\ \text{a})$$

$$f_T = \frac{3\,\mu_n(V_{gs} - V_{th})}{4\pi L^2\,(1 + 3L_D/L)} \quad \text{saturation regime} \qquad (2.23\ \text{b})$$

From Equation 2.23 it is evident that f_T can be increased by: (i) reducing the channel length (L) of the transistor, (ii) reducing the electrode overlap length (L_D), (iii) increasing the charge carrier mobility of the semiconductor. In the next section, significant effort was focused on minimizing L_D by fabricating self-aligned gate transistors developed via new-processing method, adhesion lithography.



Figur.2.2.6. Thin-film transistor schematic showing the parasitic overlaps between the various electrode terminals.

2.3 Ferroelectricity in solid-state materials

In an isotropic dielectric material, the bound charge is slightly separated by an applied electric field, **E**. This partial charge separation induces a local electric dipole moment in the material, and the vector sum of these dipole moments per unit volume is defined as polarization, **P**. This polarization is dependent on the material property and can be expressed as:

$$\mathbf{P} = \varepsilon_0 \chi \boldsymbol{E} \tag{2.24}$$

where ε_0 is the vacuum permittivity and χ is the responsivity to an applied field, susceptibility. Then the total polarization can be expressed by combining the polarization of dielectric material with free space effect. This physical quantity is called as the electric displacement field, given by the equation:

$$\mathbf{D} = \varepsilon_0 \mathbf{E} + \mathbf{P} \tag{2.25}$$

However, there are specific dielectric materials that show spontaneous polarization due to the incongruity of crystal structure. In the crystal structure of barium titanate, for example, the centre of positive charge does not correspond with the centre of negative charge. This causes the dielectric material exhibits inherent, spontaneous polarization. This polarization can be switched by a specific applied electric field in the opposite direction, coercive field. This directed polarization is sustained even in the absence of an external electric field, yielding a hysteresis loop. This bistable and hysteric characteristic is called ferroelectricity[120,121]. When ferroelectric materials are heated above a certain temperature, ferroelectricity disappears. The temperature at which this phenomenon occurs is the so-called Curie temperature and is attributed to thermal disordering of the crystal structure.

Ferroelectricity has been found in numerous materials and includes inorganics such as $SrBi_2Ta_2O_9$ (SBT), $Pb[Zr_xTi_{1-x}]O_3$ (PZT) as well as organics such as ferroelectric nylons, a polyvinylidene fluoride, P(VDF) and P(VDF) based copolymers. Representative ferroelectric materials and its properties are summarized in the table 2.1. Among these materials, the organic ferroelectric material, P(VDF-TrFE) will be further discussed due to its relatively high ferroelectricity and the potential for cost processing from solution phase.

	Inorganic Based NVM	Organic Based NVM
Technology Readiness Level	Already in Market	Close to Market
Material	$SrBi_2Ta_2O_9$ (SBT), $Pb[Zr_xTi_{1-x}]O_3$ (PZT)	Ferroelectric nylons , P(VDF)
Energy Efficient	Excellent	Low
Ec (MV/m)	< 5	> 50
Process Temperature	> 900 °C	< 150 °C
Cost	Moderate	Ultra low-cost attainable

Table.2.1. Representative ferroelectric materials and its properties.

Polyvinylidene fluoride, P(VDF) is a linear fluorinated hydrocarbon polymer, based on the monomer CH_2CF_2. The dielectric properties of P(VDF) are significantly dependant on the molecular orientation of this monomer and its crystal structures[122,123]. The monomer itself shows polar characteristics because there is a difference in the electronegativity between the hydrogen and the fluorine atoms, which induces a dipole moment. During polymerization and crystallization, if the monomers are unaligned, the net polarization of the polymer becomes a neutralized state and there is no permanent electric dipole. This kind of P(VDF) such as trans-gauche $TG\overline{TG}$, α-phase display paraelectricity. However, if the monomers are aligned such as the all-trans (TTTT) β-phase, the polymer crystal shows polar characteristics and this polarization can be switched according to the external electric field, hence manifested as ferroelectricity. The chemical structure of the monomer and the different crystal structures of P(VDF) are depicted in Figure 2.3.1.

The β-phase of P(VDF) is useful for applications such as a non-volatile memory devices and additional post-treatment is often required to obtain it. To this end, there are several methods one can employ to obtain the β-phase including: mechanical extension followed by electrical poling from the α–phase, high pressure crystallization, ultra-fast cooling, addition of nucleating fillers such as $BaTiO_3$ and copolymerization with other

polymer such as trifluoroethylene, hexafluoropropene and chloride trifluoride ethylene [124,122]. Among these methods, the most well established method is copolymerization with trifluoroethylene, P(TrFE), resulting P(VDF-TrFE). The addition of the third fluoride in the TrFE enhances the β-phase formation due to a large steric hindrance. Additionally, the β-phase of P(VDF-TrFE) is easily processed directly from the solution states, thus P(VDF-TrFE) has been studied extensively.[123,125] Usually the molar ratios of VDF to TrFE are between 50:50 mol% and 80:20 mol%. A schematic chemical structure of P(VDF-TrFE), together with the ferroelectric behaviour of a capacitor under operation and its structure are illustrated in Figure 2.3.2.

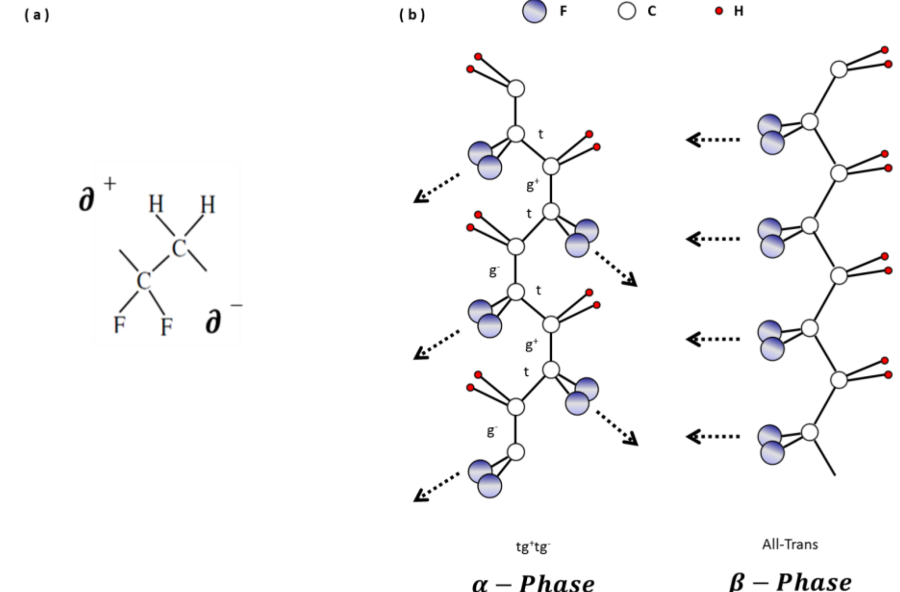


Fig.2.3.1.(a) Chemical structure of the VDF monomer. (b) Crystal structures of P(VDF).

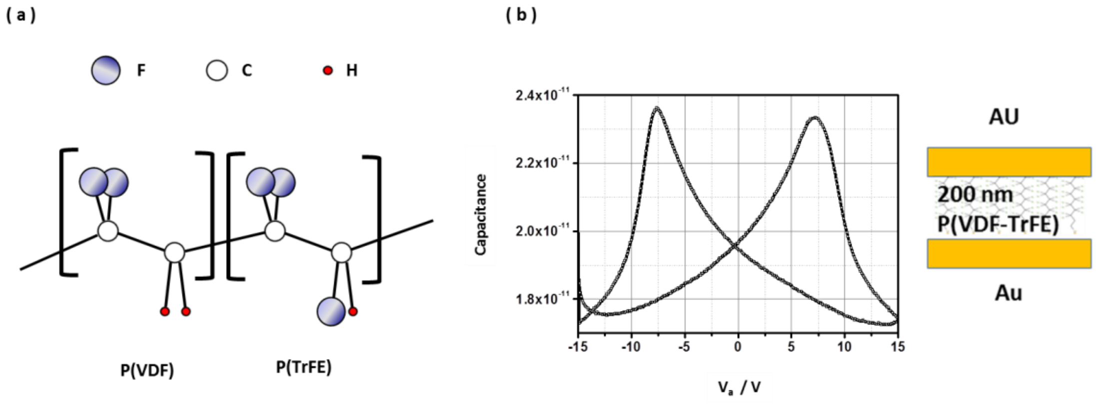


Fig.2.3.2.(a) Schematic chemical structure of P(VDF-TrFE). (b) Typical hysteresis loop of 200-nm-thickness of organic ferroelectric materials, P(VDF-TrFE). Device structures was 200 nm thick P(VDF-TrFE) MIM Capacitors.

One of main research directions in the field of P(VDF-TrFE) based memory capacitors is achieving low-voltage operation. When compared to inorganic ferroelectric materials and devices, organic ferroelectric devices require a relatively high operating voltage due to high coercive field (~ 50 MV/m). For example, the coercive field of $Pb[Zr_xTi_{1-x}]O_3$ (PZT) is below 5 MV/m, which translates to an operating voltage of 1 V for a 200 nm-thick active layer. For an equivalent thickness P(VDF-TrFE) layer the operating voltage of the capacitor would have been 10 V i.e. five times higher. There have been numerous attempts to reduce the voltage operation of organic ferroelectric memories with relatively little success. The simplest way for achieving low-voltage operation is by decreasing the ferroelectric film thickness. Bune *et al*. showed that low voltage operation (< 1 V) was attainable with Langmuir–Blodgett (LB) deposited ultrathin film (~1 nm)[119]. Fujisaki *et al*. also reported that low-voltage operation with the film thickness of 65 nm by spin casting[126]. Kliem *et al.*, however, experimentally figured out that the thinner the film is, the higher the coercive field becomes. This dependence was expressed in a power law given as $Ec \sim d^{-\alpha}$, where $\alpha = 0.64$ and d is film thickness[127]. This dependency was attributed to the reduction in the crystallinity within the layer and the non-ferroelectric "dead" layer present on the aluminium electrodes. Naber *et al.* proposed that introducing of the organic conductive doped polymer PEDOT:PSS layer instead of aluminium suppressed this scaling effect and achieved an operation voltage of 5.2 V[128]. Recently, a noteworthy result was reported by Hu *et al*, which showed that low voltage operation of <0.8 V was achievable by confining the grain boundary of P(VDF-TrFE) films using nano imprint method (NIL)[118].

An alternative approach for reducing the operating voltage of organic ferroelectric is by simplifying the device structure. Device layouts of 1 TFT with 1 Capacitor or 2 TFTs with 2 Capacitors is required when implementing the ferroelectric materials into memory devices[125]. However, if devices can be fabricated in a simpler form, may also provide significant advantages. For example, Asadi *el al.* developed non-volatile bistable resistive memory devices by blending P(VDF-TrFE) with semiconducting poly(3-hexylthiophene), P3HT[129]. Charge transport through the semiconducting phase could be controlled by external ferroelectric polarization of polymer. Similarly, Khan *el al.* reported that this blending method can be extended to n-type organic semiconductor, [6,6]-phenyl-C61-butyric acid methyl ester (PCBM) [130]. In addition, Breemen *el al.* developed similar organic blend system in a more controlled way by surface directed phase separation with patterned SAMs[131]. Moreover, the possibility of fabrication of array devices on plastic film in simpler forms of

1D or 1D1R was also demonstrated. These various research directions relevant to organic memory devices based on P(VDF-TrFE) are summarized in the Table 2.2.

	Low-voltage capacitors	Resistive memory
Methods	- Decreasing the film Thickness By Langmuir–Blodgett (LB),Spin casting	- non-volatile bistable resistive memory By blending with semiconductor, P3HT (P-type), PCBM (n-type)
	- Minimizing "deadlayer effect " By introducing the PEDOT:PSS layer	- Controlled blending By patterned SAM
	- Refining crystal structure By nano imprint method(NIL)	- Fabrication of array devices on plastic film in a simpler form (1D or 1D1R)
Limitation	Thickness Below 50 nm in vertical structure often displayed degradation	Still high operating voltage

Table.2.2. Research directions of organic memory devices based on P(VDF-TrFE).

One interesting device architecture that to date has received relatively little attention is organic ferroelectric tunnel junctions. This is primarily due to the extreme difficulty in fabricating such devices since the ferroelectric polymer layer thickness is required to be <<10 nm. To the best of our knowledge, to date, there are only a handful of studies describing the development of inorganic ferroelectric tunnel junction memories and only one on organic ferroelectric junction memory[133-136].

CHAPTER 3

New processing techniques for large-area electronics

3.1 Interlayer Lithography

3.1.1 Introduction

Recently, a modified version of the lift-off process called Interlayer Lithography (IL) was reported for the patterning of conductive electrodes.[35–37] In the latter study, a few layer (4 nm-thick) chemically exfoliated graphene oxide was transferred to the surface of the pre-exposed yet undeveloped negative tone photoresist namely *SU-8*. During the developing step of the photoresist, the graphene oxide layer was removed with the un-exposed areas of the photoresist and ultra-thin graphene electrodes were formed on the negative tone photoresist.[37] This early work demonstrated that IL could indeed be used in large-area microelectronics especially for the patterning ultra-thin conductive layers at low temperatures. Here, the IL method was studied in more detail and exploited for the patterning of metal electrodes where the first electrode acted as a photo-mask when back illuminated.

3.1.2 Experimental Methods

For the purpose of this work the IL method was further developed and explored for application in large-area electronics. As schematically illustrated in the Figure 3.1.1, a 40 nm-thick Al electrode acting was deposited by thermal evaporation on pre-cleaned glass substrate through a shadow mask. Then a negative tone photoresist (*SU-8,* 2000.5 *Microchem*) was spin-cast on top at 4000 rpm for 60 seconds and soft-baked on a hot plate at 95 °C for 60 seconds. Next, the photoresist was cross-linked through back exposure using a hand-made cross-linking system for 3 to 5 minutes. In this configuration, the first deposited Al electrode acted as a mask. Next, the sample was annealed again at 135°C for 3 minutes. A second 40 nm-thick Al electrode was deposited on the soft-cured substrate and the photoresist was developed by sonication for 3 to 5 minutes in the *SU-8* developer. During developing step of the photoresist, the second deposited electrode was patterned with the unexposed photoresist which was defined by the overlapping area with the first Al electrode. Finally, the sample was annealed at 200°C for 10 minutes for hardening the photoresist. During these process steps,

the thickness of the photoresist at each step was measured with a surface profiler.

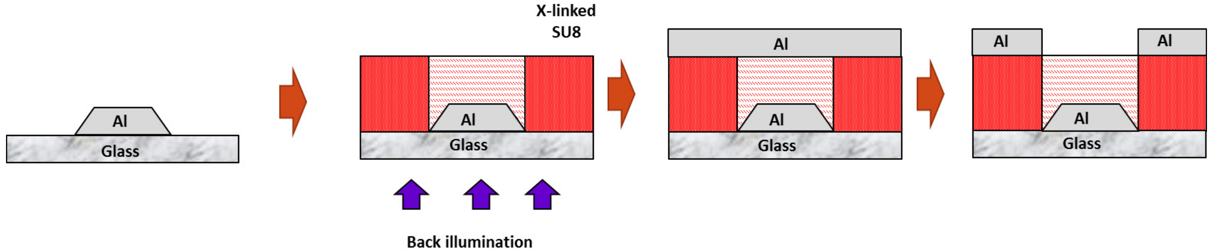


Fig.3.1.1.Schematic representation of the IL process.

3.1.3 Results and discussions

Firstly, the temperature profiles of the hot plate and the thickness variations of the *SU-8* layer as a function of the spin coating conditions were investigated in order to ensure stable and reproducible results. As discussed earlier, the negative photoresist is cross-linked during the post exposure bake (PEB) through the heat assisted diffusion of the activated cross-linker by light. Thus accurate control of the process parameters, such as temperature and time, was essential. As shown in the Figure 3.1.2, the measured temperature at the surface of a hotplate was consistently lower than the programmed temperature. The higher the setting temperature was, the larger the deviation was from that setting temperature. The deviation at the setting temperature of 100°C was approximately 10°C, but increased gradually at the elevated temperatures and reached 40°C at the setting temperature of 260°C. Moreover, the temperature of the glass (borosilicate) was always lower than that of a silicon wafer. This is most likely due to the lower thermal conductivity of glass (1.1 W/ m K) as compared to that of silicon (148 W/ m K)[49]. Hence, a higher setting temperature was used when glass was employed as the substrate. For example, if a annealing temperature of 100 °C was required on the glass substrate, the hotplate temperature was set to 120 °C in order to reach the targeted 100 °C. In every case, the temperature profiles were measured using a thermocouple (testo 925).

The photoresist thickness per spin speed (in revolutions per minute) curve is shown in Figure 3.1.3. The 4000 rpm for 60 seconds was considered to be an ideal spin speed since the changes at the spin rate caused only small changes in the thickness. Below 2000 rpm, the thickness of the *SU-8* was strongly dependant on the rate, implying that small deviations in the spin speed would cause large changes in the layer thickness. The initial thickness at 4000 rpm was about 0.64 μm, but it decreased during post processing. The total layer thickness

was decreased by 3% of the initial thickness after the post exposure bake step at 135°C for 3 minutes and the hard bake caused it to fall by a further 3%. Total shrinkage of the photoresist was about 0.3 μm.

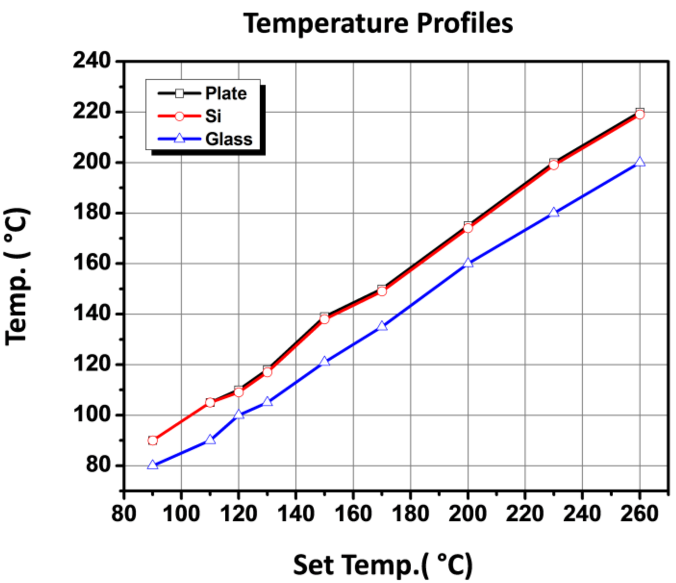


Fig.3.1.2. Measured surface temperatures (black) versus hotplate set temperatures for a Si wafer (red) and a glass substrate (blue) from 90 °C to 260 °C.

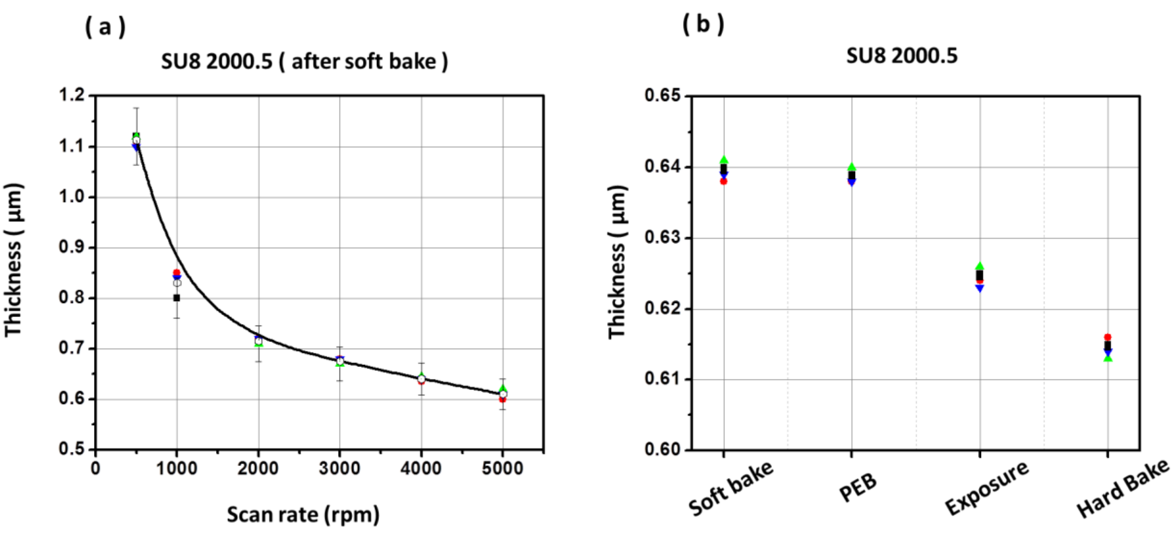


Fig.3.1.3. (a) TPR curve of *SU-8* according to the spin rate from 500 rpm to 5000 rpm. (b) Thickness changes of spin-coated SU-8 during the post-processes.

Although the condition of post exposure bake was given as 95°C for 2 minutes from the datasheet of *Microchem,* several temperatures from 95°C to 135°C for the PEB step were

investigated. As shown in Figure 3.1.4, the PEB condition of 135°C for 3 minutes produced optimum patterns. Processing below 135°C, formation of bubbles was observed indicating damage to the *SU-8* layer.

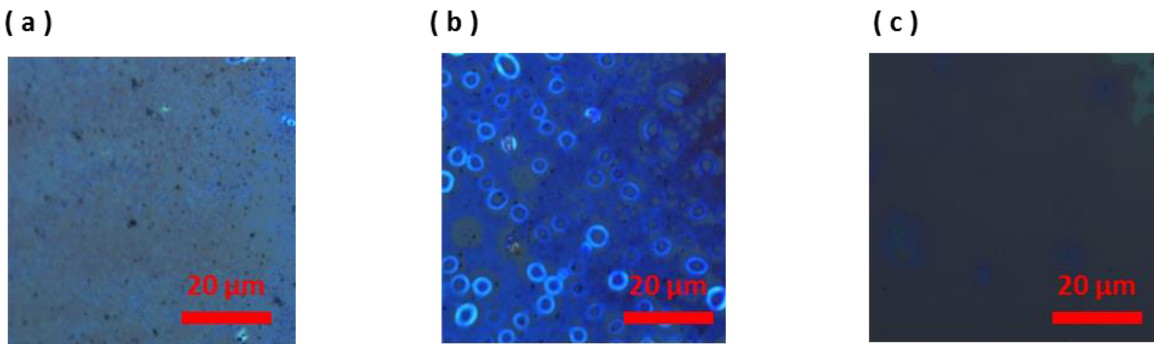


Fig.3.1.4. Surface images of spin-casted *SU-8* at various PEB temperatures. (a) 95°C, 3 min. (b) 115°C, 3 min. (c) 135°C, 3 min.

After setting up the basic spin-casting and baking condition of SU-8, patterning by the back-exposure with the light source of cross-linking system was investigated with an optical microscope. Unfortunately, obtained patterns were found to be not well-defined. The latter feature was attributed to the use of the hand-made exposure system for cross-linking the photoresist. In an effort to address this issue the system was modified (collimated system) and well-defined patterns were obtained. As illustrated in Figure 3.1.5, guides of 2 cm height were installed on the system assuming the resolution limit of *SU-8* was in the range of 1 to 2 μm. The patterning was tested with and without the guide and inspected with an optical microscope. A finer pattern was obtained with the guide since it would block the light from the side, reducing the shadowing effect. Figure 3.1.6 showed the patterned images with the guide and without the guide. Without the guide, the *SU-8* was not clearly defined and the patterned edge resolution was over 25 μm. With the guide, however, the *SU-8* was well-defined and a resolution of 1 to 2 μm at the edges was achieved. The required exposure time for patterning was in the range of 3 minutes to 5 minutes, if the exposure time is below 3 minutes, the pattern was easily removed by the developer. On the other hand, if the exposure time was over 5 minutes, the PR was not well developed (i.e. difficult to remove).

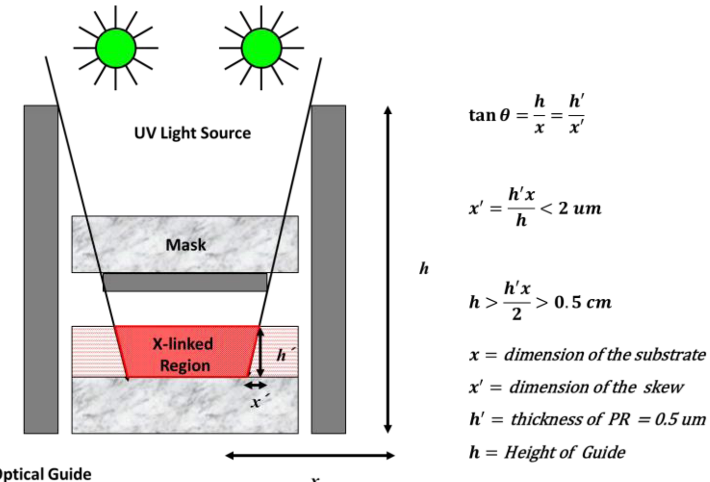


Fig.3.1.5. Schematic illustration of the hand-made exposure system. From the geometrical considerations, guides of 2 cm height were installed on the system for enhancing the patterning resolution.

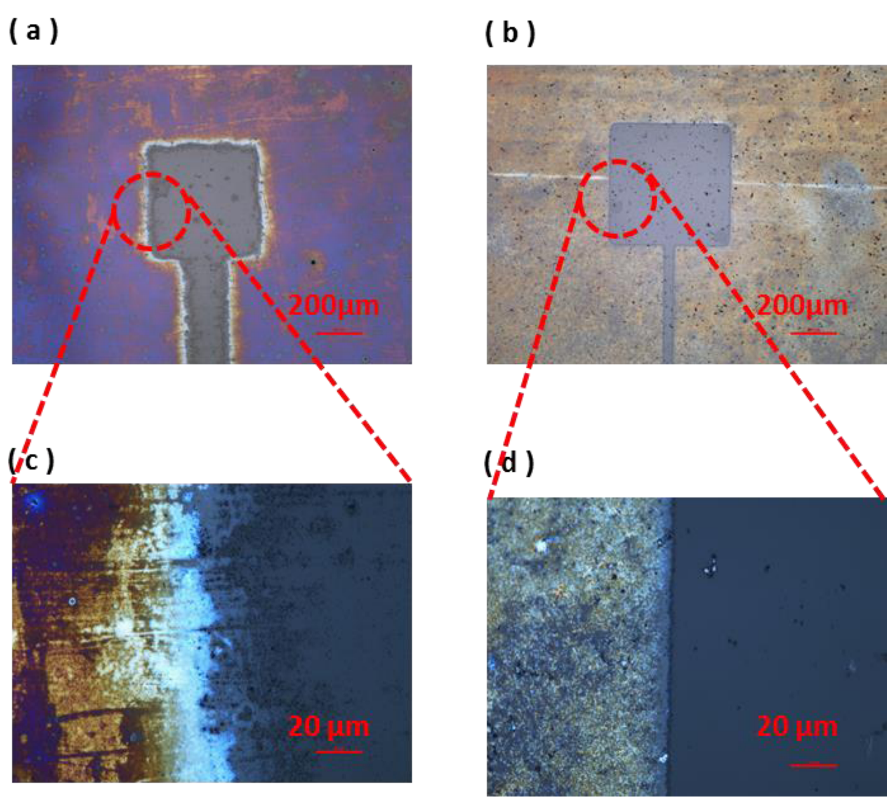


Fig.3.1.6.Pattern images without guide at low (a) and high resolution (c), Pattern images with guide at low (b) and high resolution (d) for IL.

There are two possible routes that can be used to pattern the electrodes as illustrated in the Figure 3.17. The first one is the “cross-linking after deposition” route and the other one

the “deposition after cross linking”. Since *SU-8* shrinks during cross-linking, it was necessary to evaluate the impact of shrinkage to the metal electrodes. These results were used for deciding on the optimal patterning route to be adopted for electrode processing.

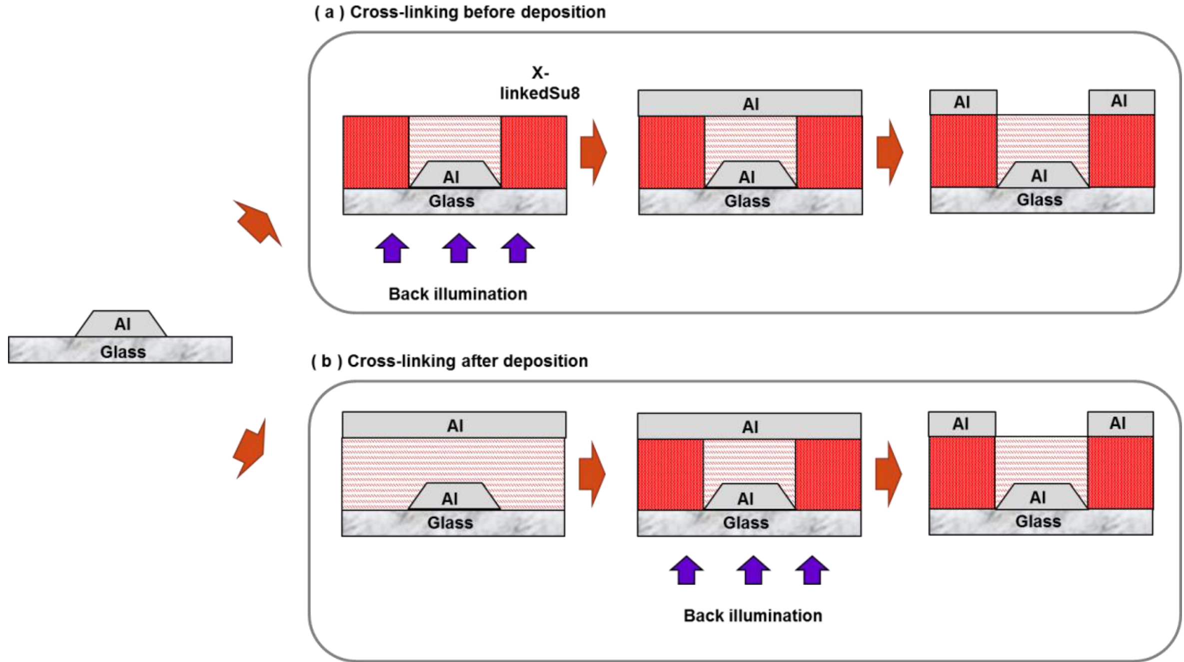


Fig.3.1.7.Two possible process routes for IL. (a) Cross-linking before deposition. (b) Cross-linking after deposition.

Electrodes patterned using both processing routes were inspected with an optical microscope. In the case of the “cross-linking after deposition” route, wrinkles in the metal electrodes were observed before the developing step and the pattern was not well-defined as shown in Figure 3.1.8. These wrinkles were attributed to the stress relaxation of the films.[50–52] During cross-linking the photoresist shrinks resulting in stress between the metal and the photoresist layers. To minimize the stress, the metal deforms leading to the micro-wrinkles observed. Due to these micro-wrinkles, there was no selectivity between the exposed and unexposed regions during the developing step with the resulting pattern appearing not well-defined. However, this issue was rectified by removing the unexposed region during developing using the “deposition after cross linking” route. Using the latter process route, different dimensions of patterned electrodes were possible as shown in the Figure 3.1.9. On the basis of these results, we conclude that *SU-8* should be cross-linked in advance of the metal deposition in order to achieve high resolution patterning of the metallic electrodes via IL.

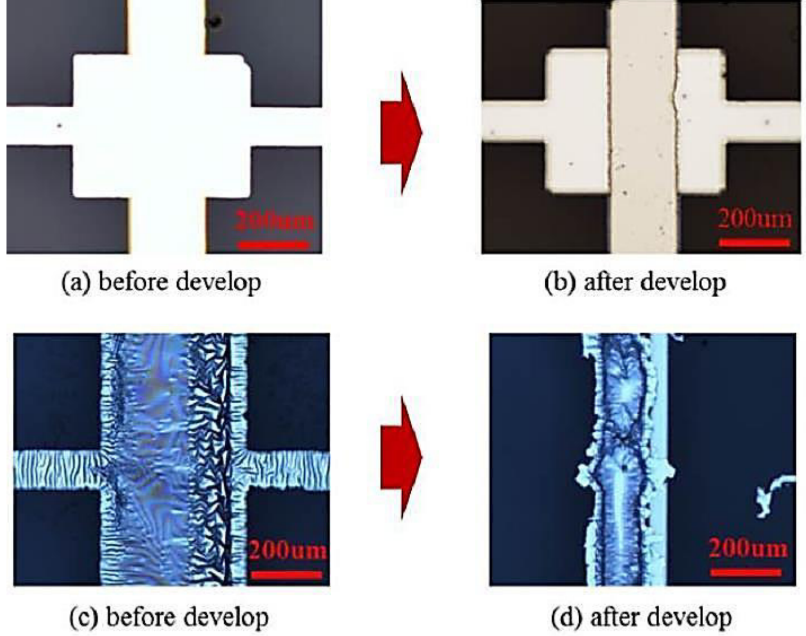


Fig.3.1.8. Pattern images of the “deposition after cross linking” route. before (a) and after (b) develop. Pattern images of the “cross-linking after deposition” route before (c) and after (d) develop.

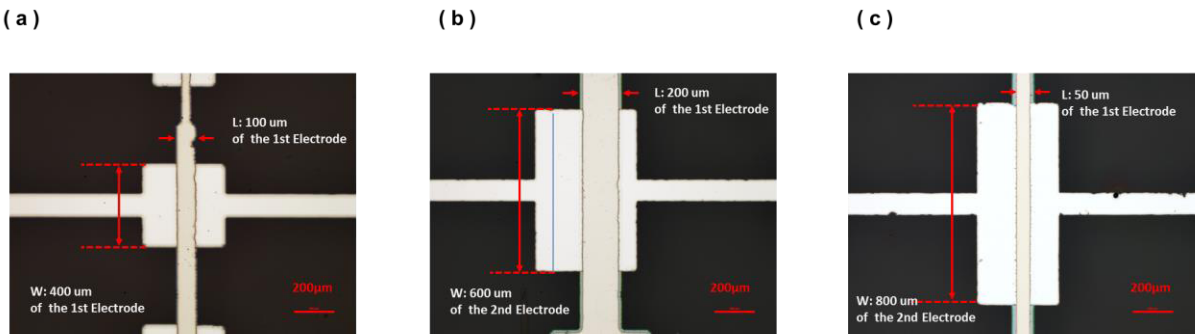


Fig.3.1.9. Electrode patterns with different dimensions produced by IL. (a) W/L = 400/100 μm. (b)W/L = 600/200 μm. (c) (b)W/L = 800/50 μm.

3.1.4 Summary and Conclusions

A modified version of photolithographic lift-off process called IL was demonstrated using a negative-tone photoresist. Following systematic process steps optimization, reliable patterning of metal electrodes with micrometer accuracy, was demonstrated. Despite the success, however, an important limitation associated with the method, was identified. Specifically, since IL relies on the use of micrometer-thick photoresist layer, a significant thickness discontinuity between the first and the second metallization layers exist. The latter

was found to limit the applicability of the method to soft semiconducting materials (Figure 3.1.10). A new patterning method was needed.

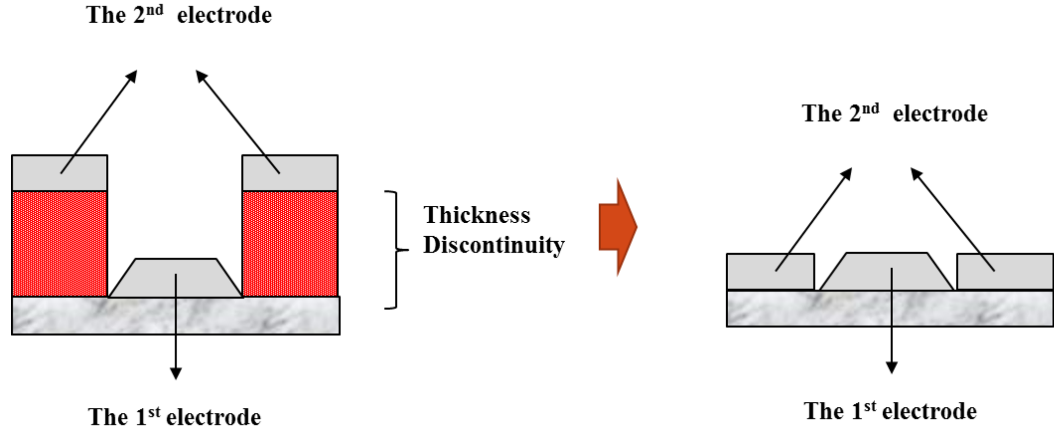


Fig.3.1.10 Schematic demonstrating the fundamental limitation of IL, thickness discontinuity between electrodes.

3.2 Adhesion lithography

3.2.1 Introduction

Several non-conventional patterning methods have been proposed and studied over the years including nano-skiving [53,54] and nano-imprint lithography.[27] Although these processes have their own distinctive advantages and disadvantages, self-assembled monolayers (SAMs) based processes were widely studied due to their bottom-up self-assembly nature.[55,56] Hatzor *et al.* proposed SAMs as a molecular ruler for the pattering in nano scale[57]. After placing the metal electrodes on the substrate with ~ 100 nm spacing by conventional e-beam lithography, a mercaptohexadecanic acid was functionalised on the surface of the first metal electrode. By controlling the thickness of the SAMs via repeated SAM treatment, ~100 nm spacing between the 1st metal electrodes became shorter by a few nanometre each time with the isolated region remaining in the centre. After deposition of the second metal, the unwanted second metal was chemically lifted off in HCl/DMF solution while the isolated centre metal electrode remained between the first metal electrodes. In this manner, they reported the formation of sub-30 nm nanogaps between metallic electrodes. Negishi *et al.* suggested a nanogap fabricating method in a more direct way[58]. After depositing the first metal electrode, the metal was functionalized with SAMs, 16-mercaptohexadecanic acid. Next, the second metal electrode was deposited on the surface and SAMs were chemically removed by

immersion in a photoresist stripper. By using a single SAM treatment step, they reported the possibility of direct nanogap patterning. Beesley *et al.* also demonstrated nanogap fabrication using the SAMs as the surface energy modifier[59]. After the formation of the first metal electrode, the metal was functionalized with a hydrophobic SAM. In their study, the workers used octadecylphosphonic acid (ODPA) for oxides and octadecanethiol (ODT) for Au electrodes. Next, the second metal electrode was deposited by thermal evaporation through a shadow mask. Finally, mechanical exfoliation using an adhesive was performed for forming the nanogap. The second metal on the SAM treated region was removed easily due to the hydrophobic SAMs treatment and the in-plane nano metal structures with sub-15 nm gaps were fabricated. The process was called Adhesion Lithography (a-Lith) and has since been explored for numerous device applications[139]. Negishi *et al.* used SAMs as a separator between metal electrodes while Beesley *et al.* utilized the SAMs for modifying the adhesion forces of the first metal's surface. The a-Lith is considered to have huge potentials since it can be easily applied to large-area substrates even via roll-to-roll processes. Here, we explored the use of a-Lith as an alternative patterning method to IL discussed earlier.

The fundamental concept that underpins a-Lith is the patterning of layers by mechanical exfoliation by controlling the surface adhesion force between the first and second metal electrodes. As illustrated in Figure 3.2.1, if the adhesion of one surface is weaker than adjacent surface(s), the layer on the weak adhesion surface will be easily peeled off through the use of an adhesive medium such as tape and/or glue. This surface energy modification could be attained using a variety of hydrophobic/hydrophilic organic SAMs.

Amongst the vast library of organic SAMs, octadecylphosphonic acid (ODPA) has been known as a stable hydrophobic SAM suitable for attaching onto metal oxide surface such as AlO_x, TiO_x and SiO_x.[60] One side of the ODPA molecule is terminated with phosphonic group, which anchors to the surface of the native metal oxide and acts as a head group. The other side of ODPA is terminated with methyl group (CH_3), thus the SAM functionalized surface often shows a highly hydrophobic character. This is why ODPA was also considered for this work as well as used extensively in the literature.[59] Gouzman *et al.* reported the surface chemistry of ODPA with an X-ray photoelectron spectroscopy study.[61] The phosphonic acid molecules in the unheated state simply attached to the substrates in the form of hydrogen-bonding, but it transformed to strongly chemically bonding in the form of a tri-dentate phosphonate by additional sufficient annealing. In addition, they showed the bond strength in the form of hydrogen-bonding was weak, thus ODPA became defective by simple

rinsing, while stabilized one by thermal annealing was quietly strong. Based on these early results, SAM functionalization in this study was implemented using the following steps: immersing the sample in the SAM solution followed by rinsing with IPA and thermal annealing.

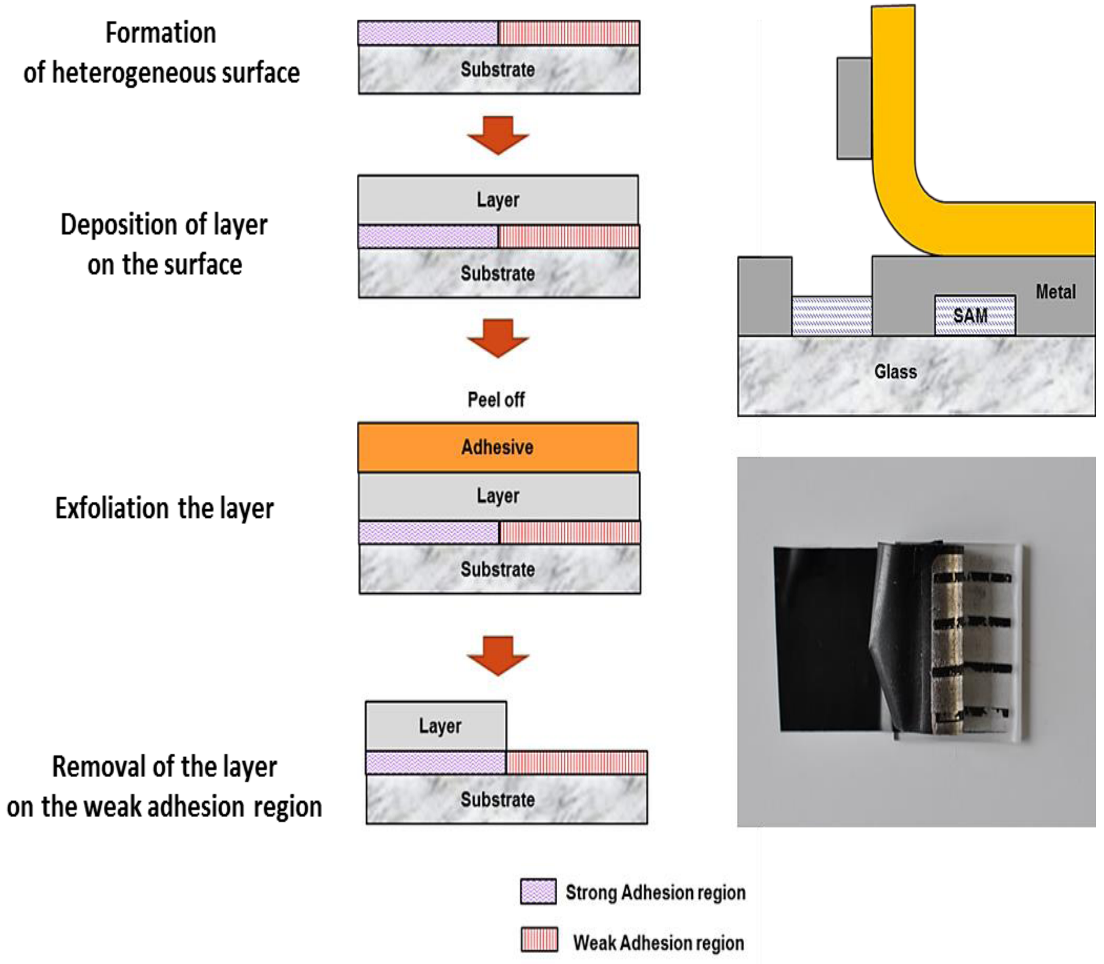


Fig.3.2.1. Basic process flow chart of a-Lith.

3.2.2 Experimental Methods

The organic interlayer for selective surface treatment, *Benzocyclobutene photoresist* (*CYCLOTENE3000, Dow Chemical*) was spin-casted at 4000 rpm for 60 s and cured on a hot plate at 300°C for 1 hour in N_2. Then, a 40-nm-thick Al layer acting as the first electrode was deposited by thermal evaporation on the substrate through a shadow mask and thermally annealed at 200 °C for 10 minutes in ambient air in order to form a native oxide layer (alumina). SAM treatment was performed by immersing the sample in the SAM solution

(5mM Octadecylphosphonic acid, ODPA in IPA or Ethanol) for 12 hours, followed by thermal annealing at 150 °C for 30 minutes. After rinsing the sample with IPA several times and dried with nitrogen gas, a 35 nm-thick Au with 5 nm-thick Al (the latter acting as an adhesion layer) as the second electrode were vacuum-deposited by thermal evaporation on the substrate through a shadow mask. Next, the patterning was completed by peeling off the unwanted metal with adhesive tapes manually or with a tensile tester, Linkam TST 350. The resulting structures were inspected with an optical and atomic force microscope while the electrical properties were investigated using an Agilent 4155C semiconductor parameter analyzer.

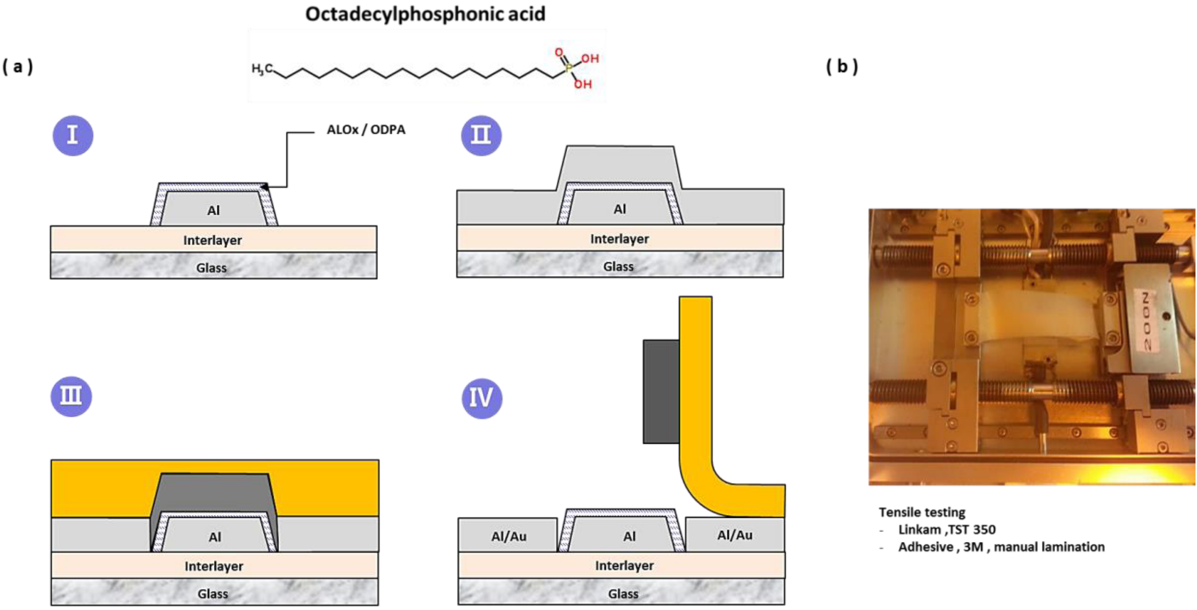


Fig.3.2.2. (a) Schematic illustrations of the process, a-Lith. (b) Peeling process with a tensile tester, Linkam TST 350.

3.2.3 Results and discussions

Firstly, the hydrophobicity of the various SAM-treated substrates was investigated by measuring the contact angle of D.I. water in an effort to ensure heterogeneous characteristics. As shown in the Figure 3.2.3, the surface of UV- ozone treated aluminum becomes hydrophobic after SAMs treatment using octadecylphosphonic acid. As can be seen, the contact angle of D.I water of the as cleaned surface was ~10 °, but it changes to ~100 ° upon SAM treatment, indicating the presence of the phosphonic SAM. On the other hand, the surface tension of glass substrate was also found to change since the contact angle of as-cleaned glass changes from ~10 °, to about 70 ° following SAM functionalization. As Hanson

et al. reported, this might due to be fact that phosphonic acid SAMs could be attached on the native SiO_2 [62]. This SiO_2 is a main component of glass and Takeda *et al.* reported that density of hydroxyl group of the surface of glass were in the range of 20 to 30 percent, dependent on their compositions [63]. To this end, Afzali *et al*. has also reported that the surface of glass was also functionalized by ODPA SAMs, hence further supporting our proposed expnalation[64].

In order to confirm whether the surface of glass was functionalized by ODPA SAMs or not, dropping test using D.I water and peeling tests were performed on the partial SAM treated glass. The SAM layer on the glass was partially removed by a brief UV-ozone treatment using a metal shadow mask as shown in the Figure 3.2.4(a).

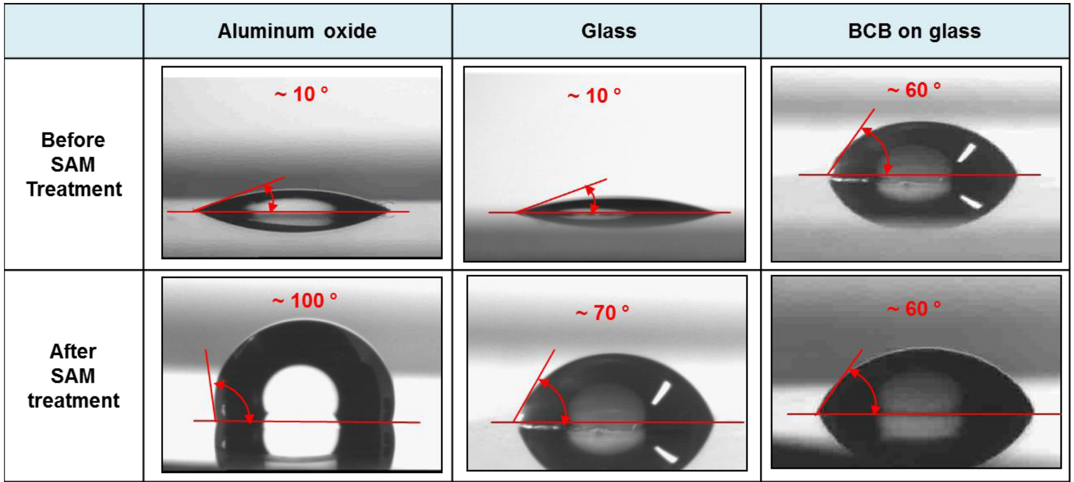


Figure.3.2.3. D.I water contact angle measurement on various substrates.

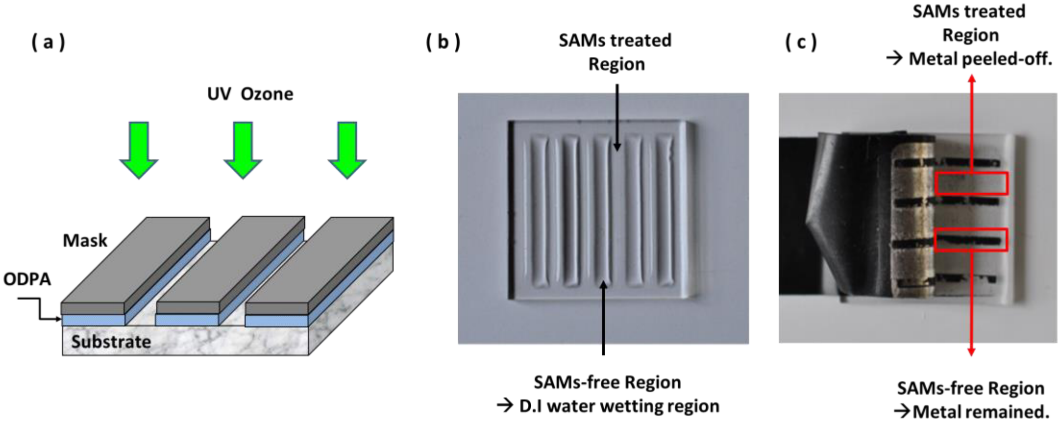


Fig.3.2.4. (a) Removal of SAMs by UV-ozone treatment with a metal mask. (b) D.I water dropping test on the substrates. D.I water was spreading only on the SAM-free region. (c) Peeling test on glass. Metal on the SAMs treated region was peeled-off, while remained on the SAM-free region.

As shown in the Figure 3.2.4 (b), D.I water spreads only on the SAM-free regions, which indicates that the surface of glass is functionalized with the hydrophobic SAM. In addition, we identified that the metal deposited on the SAMs treated glass areas was easily peeled off using a sticky tape. Although the surface of the glass substrate might be less reactive as compared to aluminum oxide surface as evident from the lower contact angle, it can be concluded that the glass substrate is not ideal substrate for a-Lith and a chemically inactive interlayer is required. To this end, benzocyclobutene (BCB) was found to provide an excellent option as a passive interlayer because it is known to consist of a hydroxyl group-free surface[65]. As a result, the ODPA SAM was assumed not to react with the surface of BCB and heterogeneous surfaces with well defines surface energetics were anticipated.

Following deposition of the organic interlayer (BCB) on glass, the contact angle of D.I. water on the BCB coated areas was ~60 °, with the value remaining almost the same after SAM treatment, indicating that the BCB surface was chemically stable. To confirm this, liquid droplet test using D.I. water was performed as shown in the Figure 3.2.5(a). Here D.I. water is seen to spread only when in contact with BCB coated glass regions. This indicates that the surface of the ODPA-treated Al-AlO_X appears significantly more hydrophobic than the surface of the BCB coated glass. The adhesion force of the surfaces were also investigated by measuring the force and distance curve using an AFM (Agilent 5500) and checking the equilibrium point between the adhesion force and an elastic force of the cantilever. The spring constant of the AFM tip employed for the measurements was 46 N/m. The calculated adhesion force of SAMs treated aluminum oxide surface was ~ 7nN, but that of the BCB coated glass was ~ 400 nN. As expected, the SAM-treated Al-AlO_X surface shows very weak adhesion to the AFM tip as compared to BCB surface. Thus metal layers deposited on the SAM treated surface are expected to be easily peeled off using adhesive tape/layer. To be noted that the adhesion force of cleaned BCB and Al-AlO_X surfaces were ~400-500 nN and ~2000 nN, respectively.

Previously, Hanson *et al.* reported that complete monolayer of ODPA was attainable by sonication of the SAM functionalised substrate in 0.5 M K_2CO_3 in 2:1 ethanol/water (carbonate rinse). However, this result was difficult to be reproduced in this study[62] as our experimental findings indicate that the ODPA layer thickness was ~10 nm. We attribute this to the different SAM functionalization process employed. The apparent thicker ODPA layer formed indicates the presence of a multi-layered SAM since the molecular length of ODPA is about 2.3 nm. The SAM thickness was studied by depositing a 40 nm-thick metal on the

substrate though a shadow mask, and removing the SAM via UV exposure. The structure's height profile was then studied using high resolution AFM. Figure 3.2.6 shows the height profile of the complete stack (SAM + metal electrode) to be on the order of 60 nm. Since the metal accounts for the 40 nm, and has been verified independently, we conclude that the remaining 20 nm is due to the formation of ODPA multilayer structure.

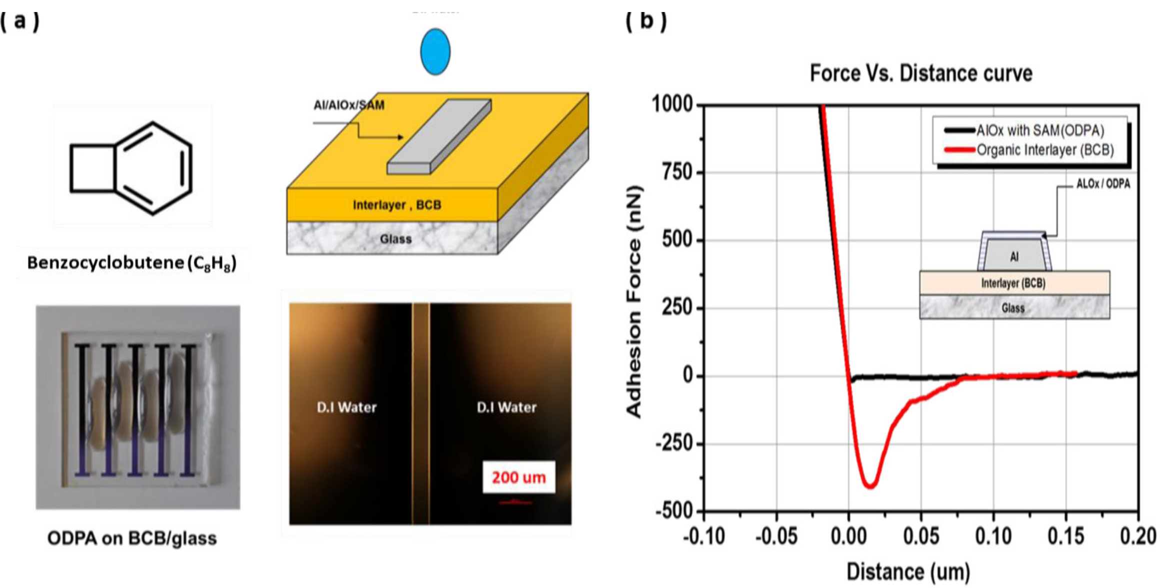


Fig.3.2.5. (a) Selective SAM treatment on the BCB coated glass. (b) Force and distance curves of the SAM treat aluminum oxide and BCB coated glass.

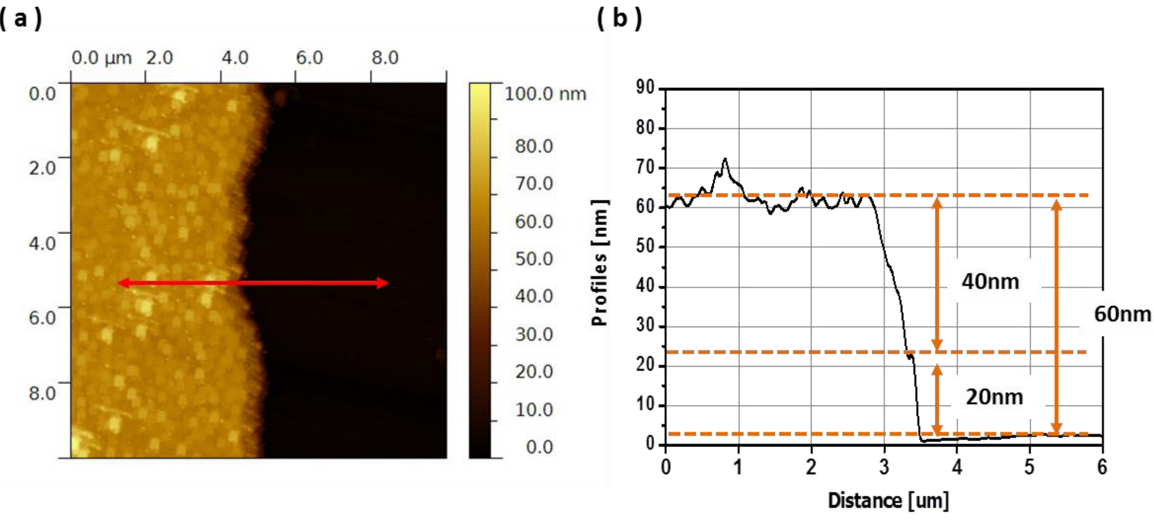


Fig.3.2.6. Multilayer ODPA film. (a) AFM topography image. (b) Depth profiles of the line (red). Total measured thickness of the layers is 60 nm, where 40 nm for the deposited metal on the SAMs. Remaining 20 nm is due to the formation of ODPA multilayer structures.

To improve the monolayer nature of the SAM, a new deposition route was developed. The latter relies on mechanical exfoliation method of the unwanted upper layers of ODPA that self-assemble to form the apparent organic multilayer. Since the chemical bonding between the substrate and head group of ODPA is expected to be very strong and the bonding between multilayer SAMs to be relatively weak (due to Van der Waals bonding), we expected that the upper ODPA layers would be easily removed through mechanical exfoliation - a process often used to exfoliate 2-D layers of MoS_2, WS_2 or graphene from bulk crystals using adhesive tape.[66–68]

Figure 3.2.7 shows the obtained results where a clear image contrast between exfoliated regions and non-exfoliated regions can be observed. The contact angle of D.I. water droplet was ~100 ° on the exfoliated region, which indicates that the SAM is still present. Following gentle scratching with a sharp tip, the thickness of the SAM was investigated via AFM. As shown in the Figure 3.2.8, the extracted depth profile was now just below 2 nm, providing evidence of the formation of monolayer ODPA SAM (if one accounts for the tilt angle of the molecules once functionalised on the surface). Guided by these results, the modified version for the formation of the SAM was adopted. Figure 3.2.8 illustrates the steps for the formation of ODPA SAMs.

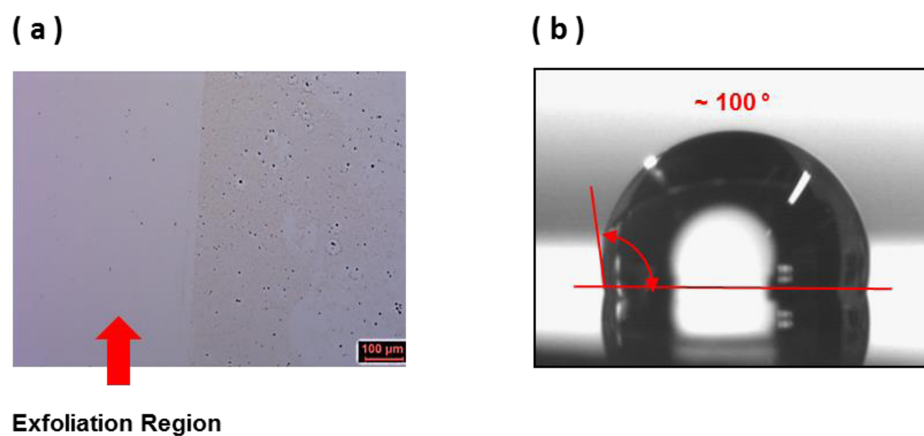


Fig.3.2.7. (a) Optical image of ODPA SAMs by mechanical Exfoliation. (b) Contact angle of D.I water on the exfoliated region (~100 °).

Using the modified SAM formation protocol, a-Lith patterning was performed using a 35-nm-thick Au electrode with a 5 nm-thick Al interlayer acting as the adhesion layer for gold on glass. The top metal was then peeled off manually using an adhesive tape or using an

automated tensile tester (Linkam TST 350). As shown in the Figure 3.2.9, the second Au metal was successfully patterned with high resolution. Analysis of the formed nanogap using AFM reveals that the average value of the nanogap separating the two electrodes was <20 nm, while the gap was found to form along the grain boundaries of aluminum electrode, clearly highlighting the importance of the metal microstructure on the formed metal nanogap.

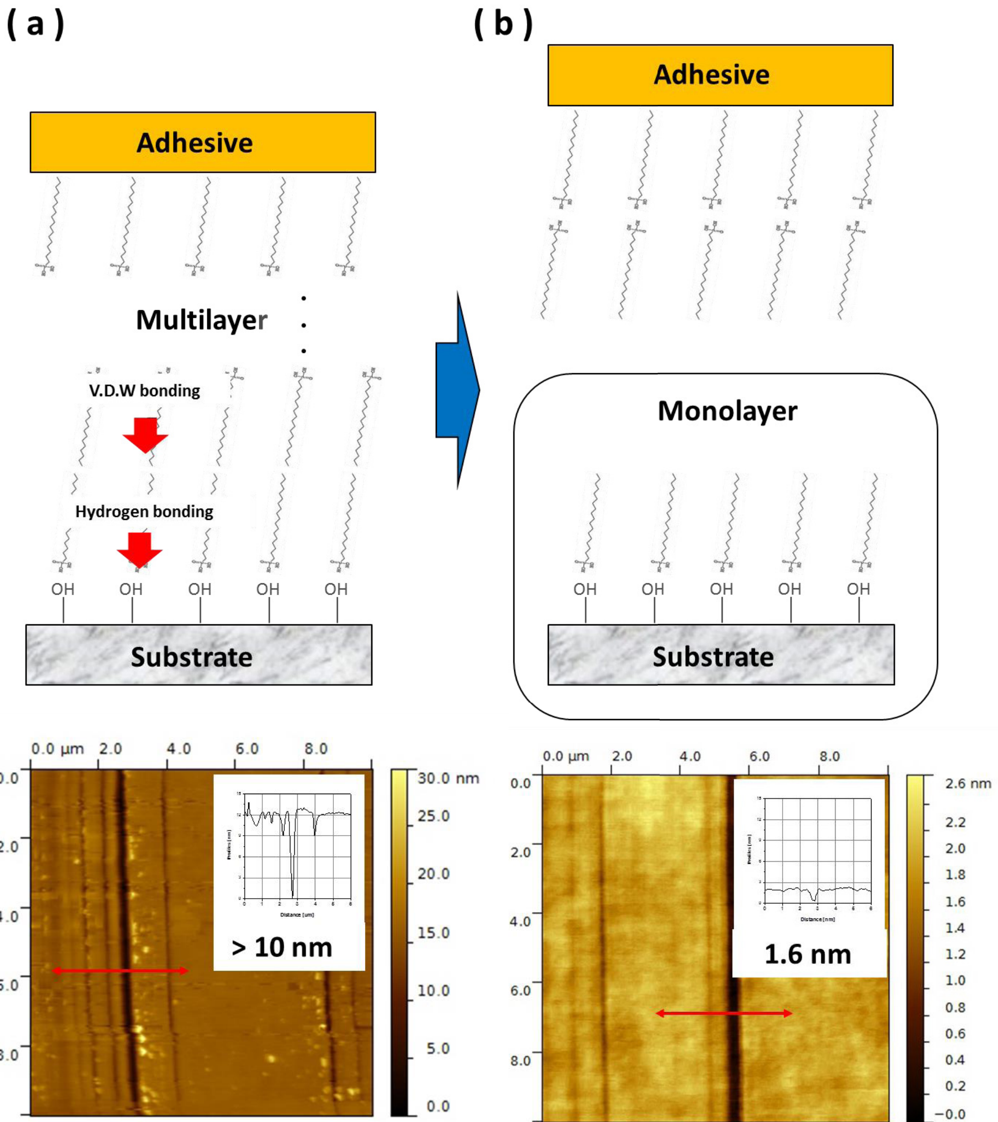


Fig.3.2.8. (a) Schematic illustration of the chemical bonding nature of multi-layered ODPA. (b) Formation of Monolayer of ODPA SAMs by mechanical exfoliation. During the exfoliation, the relatively week Van der Waals bonding between the multi-layered ODPA molecules was broken, hence only chemically bounded- monolayer ODPA remained on the surface.

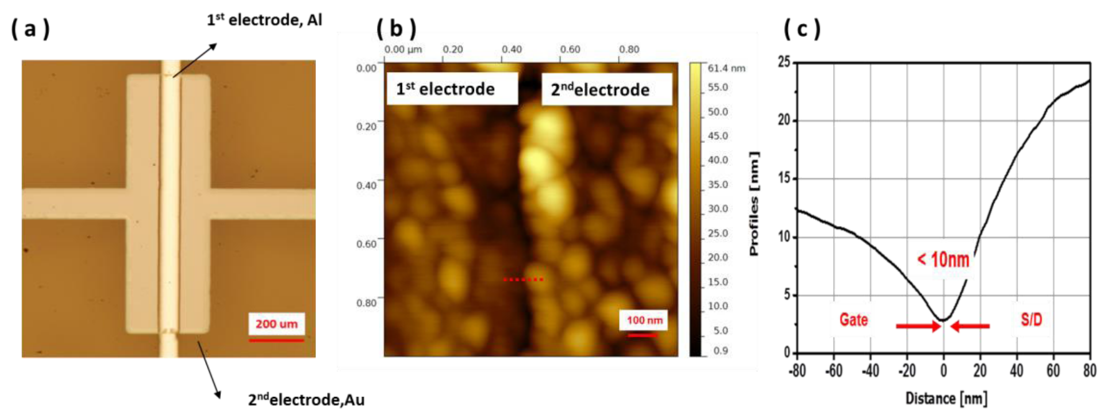


Fig.3.2.9. (a) Optical image of the in-plane nanostructures. (b) Atomic force topography image of the gap between the 1st and 2nd electrodes. (c) The profiles of the gap and the values were sub 20 nm.

3.3 Summary and concussions

Two new patterning techniques suitable for the manufacturing of large-area electronics were developed. The first method was a modified version of the lift-off process called Interlayer Lithography (IL). Patterning of metal electrodes was demonstrated in large-area substrates following systematic process optimization. In particular, spin casting conditions of the negative-tone photoresist was optimized while the exposure system was modified for collimating the light and hence minimizing the shadow effect. The development of the "deposition after cross linking" route ensured patterning of metal electrodes with excellent quality and reproducibility. However, the IL method exhibit inherent limitation in resolution due to the thickness discontinuity between the first and the second electrode/metallization layers. In an effort to address this issue a modified version of an alternative patterning technic called Adhesion Lithography (or a-Lith), was developed. The latter method relies on the modulation of the surface adhesion forces through the use of appropriate SAMs, and a mechanical exfoliation lift-off step. Once optimised the method was able to reliably produce pairs of electrodes with nanogap dimensions <20 nm. Because of its unprecedented performance and simplicity, a-Lith was considered to be dramatically more versatile than IL. Use of a-Lith for the fabrication of various devices is discussed in the following chapters.

CHAPTER 4

Low operating voltage, self-aligned gate transistors

4.1 Introduction

Efforts for the development of high-performance thin-film transistors (TFTs) have been inte nsifying in recent years due to their commercially-relevant applications in driving backplanes for flat-panel displays such as ultra-high definition displays (UHD) and organic light-emitting displays.[69,70] High performance TFTs are often achieved through optimisation of the device geometry as well as through improvements in the charge carrier mobility of the semiconductor employed.[71] To this end, a self-aligned gate (SAG) transistor offers numerous advantages since the switching speed of the device can be enhanced by minimizing parasitic capacitance elements (i.e. C_{gs}, C_{gd}, in Fig. 3.1.1.).[72,73] When the SAG architecture is combined with high performance semiconductors, TFTs' and ultimately system' performance, is expected to be dramatically improved.

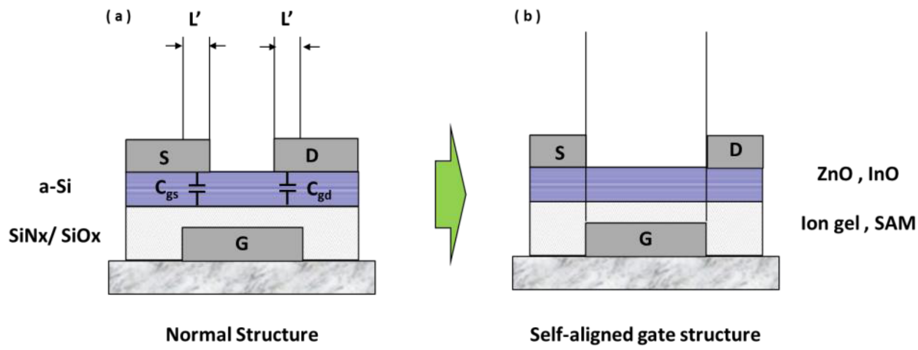


Fig.4.1.1. Strategies for high performance and low-voltage thin-film transistors. (a) shows a conventional TFT structure while (b) an aligned gate TFT architecture where the parasitic capacitances due to electrode overlaps are minimized.

Controlling of the parasitic overlap areas between the gate and source and drain electrodes through conventional photolithography is problematic due to the spatial resolution limitations associated with the photolithography systems. As a result, conventional photolithography for large-area electronics is limited to about a few micrometres[74,75]. For finer dimensions/patterns, advanced lithography techniques could be used, but it is impractical, costly and not scalable. This is primarily attributed to the exponentially increasing cost of the process equipment with increasing resolution and the associated

reduction in the throughput which in turn render these processes unsuitable for large-volume manufacturing.[76] Therefore, alternative nanoscale fabrication methods that are simple and compatible with large-area electronics manufacturing, are urgently required.

In this chapter the modified version of the a-Lith method described earlier was used for the development of SAG transistors. Solution processable semiconductors such as zinc oxide and indium oxide (ZnO, InO_X) were used as the active layers rather than commonly used amorphous silicon (a-Si) in conventional TFTs. As the gate dielectrics, an ion-gel dielectric and a SAM-based dielectric were investigated and evaluated in low operating voltage TFTs based on ZnO and InO_X. The obtained results will be introduced in following sections after reviewing the operating principles of the thin-film transistor.

4.2 Solution-processed metal oxides semiconductors

4.2.1 Introduction

Solution-processed metal oxide transistors have been studied extensively since the first report by Ohya *et al*. in 2001[81]. The interest is primarily attributed to the high performance achieved in TFTs based on a diverse range of metal-oxide semiconducting materials[82]. Furthermore, low-cost process can be achieved by changing the deposition process from vacuum-based to non-vacuum processes such as solution-based ones. To this end, various candidate solution processable materials have been reported and can be classified into two main categories: (i) nano-particle type[83] and (ii) precursor type material systems. Between the two approaches, precursor type materials have attracted most attention due to their superior performance as compared to that of nano-particle based devices. As Adachi *et al.* pointed out [84], in the case of nano-particle system, high density of the voids between the nano-particles in the semiconducting channel layer and rough interface between the gate dielectric and the semiconducting channel layer can severely limit carrier transport. For these reasons, to date, precursor type solution-processed metal oxide thin-film transistors have attracted most attention. Despite this, precursor based oxide system also exhibit some disadvantages. First of all, the transformation of precursors into a high-performance oxide semiconductor requires high temperature annealing (> 400 °C).[71] This is a severe bottleneck for transferring the technology on plastic substrates or even glass because such substrate materials cannot endure these high process temperatures. The glass transition temperature of glass for display is roughly 500 °C, thus conventional process temperatures for display are less than 400 °C. In

addition, the glass transition temperature of common plastic substrate such PEN and PET, is less than 200 °C.[85] This high temperature process stems from the fact that the metal oxide raw materials such as nitrates and acetates are chemically stable and removing the unwanted ligands is mostly achievable via high temperature annealing.[86,87] Without this annealing step, the performance of the resulting device remains low because of the presence of remnant ligands and hydroxyl groups in the solid film.[88] These features impact the stoichiometry of the resulting metal oxide layers which is known to be crucial for the device performance.[89,90] The latter property however is not easily controlled in metal oxides materials processed from solution process. This is why in recent years many researchers focused on the development of materials and processes that are compatible with low-temperature processing without compromising the device stability and performance.

For low-temperature process materials, there have been two main research directions. One is the development of materials that can be processed at low temperature. Banger *et al.* suggested that soluble metal alkoxide precursors provide a new route for low-temperature processing of metal oxides.[91] They showed that when the precursors incorporated organic bonded hybrid structures such as indium oxo cluster, zinc-*bis*-methoxyethoxide and gallium-*tris*-isopropoxide, raher than acetates or nitrates, metal oxide semiconducting layers could be grown by hydrolysis at relatively low-temperature (<250 °C). High performance indium zinc oxide (IZO) and indium gallium zinc oxide (InGaZnO) thin-film transistors were demonstrated with electron mobilities of ~10 cm^2/V.s and high on-off ratio ($>10^7$). Kim *et al.* proposed another material design approach called “self-energy generating combusting method.”[92] The workers showed that the addition of acetyl-acetonate or urea as a source of fuel in the metal nitrate precursor solution enabled the solution to be locally heated and transformed the precursors to stable metal oxide semiconductors at relatively low temperature of 250 °C. Based on this chemistry they demonstrated high performance indium oxide, zinc tin oxide and indium tin oxide thin-film transistors that can be fabricated on aluminum oxide gate dielectrics with electron mobility values up to ~40 cm^2/v.s and high on-off current ratios ($>10^5$).

A more recent approach for low-temperature processing of metal oxides was through post conversion of the precursor solid layer using light. Specifically, Kim *et al.* proposed a UV-assisted photo annealing method that can be used to lower the process temperature.[93] They showed that alkoxy group in the spin-casted film from the precursor was easily

decomposed and transformed to metal-oxide-metal frame by deep UV treatment at 150 °C. They demonstrated that this proposed methods can indeed be successfully applied to plastic substrates, due to the exceptional low-temperature process, by fabricating indium gallium zinc oxide (IGZO) TFTs with electron mobility of 7 cm^2/V.s. Similarly, Yoo *et al.* showed that the UV-processing time also could be minimized up to sub-second level by using intensely pulsed white light as a photo-annealing source.[94] Similarly, Jun *et al*., used microwave annealing as the conversion method of ZnO. Here the semiconducting films could be formed very efficiently when microwaves were focused to the nitrate precursor.[88] They showed that the performance of microwave annealed devices at 140 °C was comparable to that of hot plate annealed devices at 320 °C. Their reported value of mobility was 1.7 cm^2/V.s.

Generally speaking, the device performance of solution-processed devices was until recently considered to be inferior to vacuum-processed device mainly because the solution-processed films often contain high density of defects and pinholes. In order to solve these problems and enhance the device performance, various approaches have been developed and evaluated. One of these approaches is based on intentional chemical doping. By adding metal ions such as Li or Al into a semiconducting metal oxide layer, the film quality can be improved as electrical performances. Adamopoulos *et al.* suggested Li-doping of ZnO and their transistors and proved that the extreme high mobility of 85 cm^2/V.s could be achieved.[14] In their study, the workers simply added lithium acetates into a ZnO precursor and the doped film was formed by spray-pyrolysis at 400 °C. Their obtained value of mobility is considered to be very high and comparable to that of poly-Si TFTs.

The other proposed method is a heterogeneous oxide films method remonstrated by Rim *et al.* The workers demonstrated this concept by forming the heterogeneous channel layers.[95] They constructed these layers with indium-tin-zinc oxide layer (ITZO) as the first bottom layer and indium-gallium-zinc oxide layer(IGZO) as the second top layer. Due to the work function difference of these layers, the Schottky barrier is formed between these two semiconducting layers, which suppressed the carrier flow from ITZO layer to IGZO layer. In this way, the carrier transport could be confined in the interface between the dielectric and ITZO channel layer and the device performance could be enhanced significantly compared to that of single layer TFTs. The workers reported electron mobility values of 22.16 cm^2/V.s for these devices up from 1.56 cm^2/V.s for single layer TFTs. In addition, resulting device exhibited turn on voltages ~0 V and high on/off ratios of 10^7. These previously reported

results are summarized in the Table 4.1. Using this early work as our starting point, solution-processed ZnO and InO_X were investigated as the semiconductor materials and combined with the new-patterning techniques to demonstrate high performance TFTs.

			Semiconductor	Precursors	Process condition		Electron mobility, (cm2/V^{-1}S^{-1})	Year	ref
					Deposition Methods	Process Temp. (°C)			
Material system	binary		ZnO	Zinc acetate	chemical bath	900	N.A	2001	81
				Zinc acetate	Spray pyrolysis	400	15	2009	96
				ZnO-nanoparticle	Spin casting	100	2.5	2009	83
	Tern ary		ZnSnO	Zinc acetate / tin chloride	Spin casting	500	14	2009	97
	Quarterl y		InZnSnO	Zinc chloride Tin chloride Indium chloride	Spin casting	600	4	2011	98
Low Temp process	Material Design	Nitrates precursors	InGaZnO	Zinc acetate Indium nitrate Gallium nitrate	Spin casting	250 ~ 400	1.5	2010	99
			ZnO	Zinc nitrate	Inkjet Spin casting	150	0.4 ~ 1.8	2008	86
		alkoxide precursors	InZnO	Indium oxo cluster Zinc-bis methoxyethoxide Gallium-tris-isopropoxide	Spin casting	230	7	2010	91
		Combustion	InO, ZnSnO,InSnO	Indium nitrate Zinc nitrate Tn chloride	Inkjet printing Spin casting	200	6 ~ 40	2011	92
	Process development	Deep UV	InGaZnO	Indium nitrate Galium nitrate Zinc acetate	Spin casting	< 150	7	2012	93
		Microw ave	ZnO	Zinc hydroxide	Spin casting	< 150	1.7	2011	88
High perform	Dopi ng		Li-Doped ZnO	Zinc acetate Lithium acetate	Spray pyrolysis	400	85	2010	14.15
	Bilayer		ITZO/IGZO	Indium nitrate Gallium nitrate Zinc acetate	Spin casting	450	22	2014	95

Table.4.1. Recent progresses of solution processed metal oxide semiconductors.

4.2.2 Solution-processed zinc oxide transistors

Experimental

Solution–processed ZnO transistors with a bottom gate top contact configuration were fabricated. The solution of ZnO was prepared by dissolving ZnO hydrate (0.1 M, ZnO•xH_2O, 97% Sigma-Aldrich) in ammonium hydroxide (28–30%, Sigma-Aldrich) and stirring for 3 to 6 hour, yielding a clear transparent Zn amine complex based precursor solution. The solution was then spin casted at 4000 rpm for 60 seconds onto 200 nm-thick Si^{++}/SiO_2 substrates and subsequently annealed at various temperatures/conditions. Finally, 40 nm-thick Al for source and drain electrodes were evaporated through a shadow mask under high vacuum (10^{-6} mbar). The channel length and width of the resulting TFTs were 50 μm and 1000 μm respectively. All devices were electrically characterized using a semiconductor parameter analyzer (AgilentB2900A).

Results and Discussion

First the performance of solution-processed ZnO TFTs frown from ZnO-hydrate in ammonium hydroxide was investigated. Stable and high performance ZnO transistors were obtained by thermal annealing of the precursor layer at 300 °C in nitrogen atmosphere (Figure 4.2.1). The extracted value of mobility of the device in saturation regime was in the range of 0.5- 5 cm^2/V.s. In addition, the devices showed high current on-off ratio (>10^5) with negligible hysteresis and a turn-on voltage of almost 0 V.

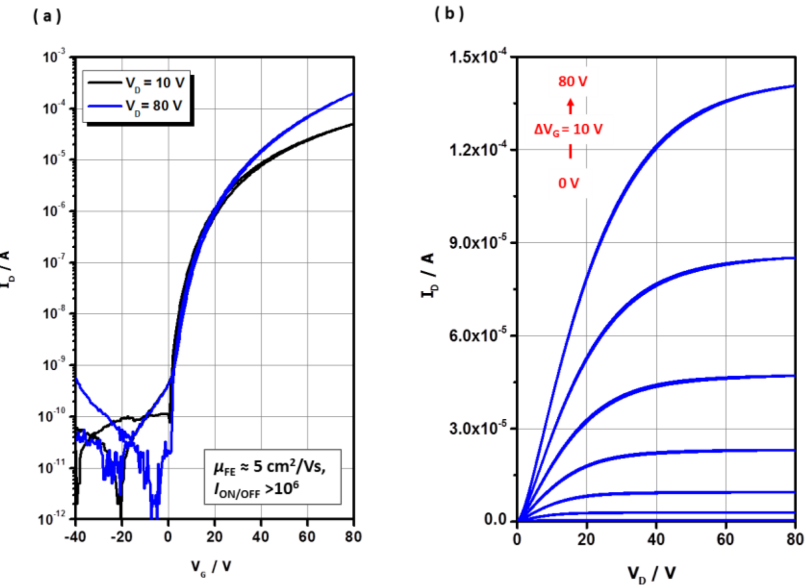


Fig.4.2.1. (a) Linear (V_D = 10 V) and saturated (V_D = 80 V) transfer characteristics of

bottom-gate, top-contact TFTs with channel width W =1000 μm and channel length L = 50 μm, fabricated with ZnO films on 200 nm-thick SiO_2 dielectric by spin casting. (b) Output characteristics of the ZnO based TFT.

As mentioned in the earlier section, thermal annealing at ~300 °C was essential for realising stable and high performance ZnO TFTs. As shown in the Figure 4.2.2, the operating hysteresis in these devices was minimized after thermal annealing at the elevated temperature. Specifically, the value of hysteresis was decreased from 6.5 V at 190 °C to 3 V at 240 °C and minimized to below 1.5 V at 300 °C. In an effort to understand the evolution in device performance with annealing temperature, several workers devoted significant efforts. For example, Jun et al. reported that two kinds of chemical reactions were required for the formation of stable ZnO layers deposited from ammonium hydroxide solution.[88] One was dehydroxylation which was occurred at the temperature of 134 °C and the other was decomposition of Zn-amine complex which was happened at 240 °C. If films were annealed < 240°C, the hydroxyl group in the form of $Zn(NH_3)_xOH_y$ or Zn-amine complex, $Zn(NH_3)_x$ remained in the film. These hydroxyl and amine groups acted as trap sites which hinder the transport of free electrons induced by the gate field resulting in the observed hysteresis of the devices. However, when the films were annealed > 240°C, the amine group in the film decomposed and the precursor became metal-oxygen-metal, Zn−O frame. Hence, the value of hysteresis was minimized below 1.5 V. On the basis of these results, we conclude that thermal annealing at 300 °C was crucial for achieving stable and high performance ZnO transistors.

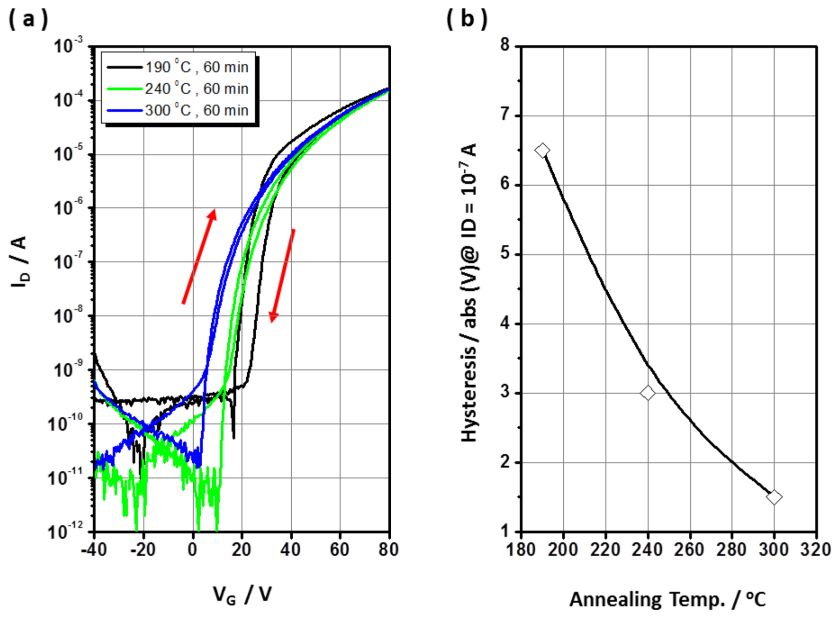


Fig.4.2.2. (a) Saturated (V_D = 80 V) transfer characteristics of bottom-gate, top-contact TFTs

with channel width W =1000 μm and channel length L = 50 μm, fabricated with ZnO films at various annealing temperatures. (b) The value of hysteresis of the devices, which was deduced the voltage differences at the drain current of 1.0×10^{-7} A.

4.2.3 Solution-processed indium oxide transistors

Experimental Sections

Bottom-gate, top-contact TFTs based on solution–processed InO were fabricated and electrically characterised. The indium oxide precursor solution was prepared by dissolving indium (III) nitrate hydrate (0.5M, $In(NO_3)_3$•$x(H_2O)$ (Sigma-Aldrich) in deionized water and stirred at room temperature for 6 hour. The resulting precursor solution was then spin casted at 4000 rpm for 60 seconds onto pre-cleaned Si^{++}/SiO_2(200 nm) substrates and subsequently annealed at various temperatures. Next, sets of 40-nm-thick Al S-D electrodes were evaporated through a shadow mask under high vacuum (10^{-6} mbar). The channel length and width were 50 μm and 1000 μm respectively. Performance of device was characterized using a semiconductor parameter analyzer (AgilentB2900A).

Results and Discussion

The performance of solution-processed InO transistors was first investigated. Indium oxide is known to be an n-type semiconductor with high electron mobility of 55.26 cm^2/V.s.[100] Additionally, deionized water may also be used as solvent when the precursor materials such as indium nitrate hydrate [$In(NO_3)_3$•$x(H_2O)$] is used. Such water based solutions are desirable because of their chemically friendly to the organic interlayer for fabricating the SAG TFT structure via a-Lith. In this study, stable and high performance InO transistors were obtained by thermal annealing of the spin casted precursor layers at 350 °C in air. Devices annealed at lower temperatures often showed significant operating hysteresis. To this end, Park *et al.* reported that nitrate groups in the precursor was gradually decomposed with increasing temperatures and pure In−O bonds formed in the solid films annealed at 320 °C, in good agreement with our observations.[101]

Initially, the TFTs were annealed at 240 °C for 1 hour and the devices showed the hysteresis (Figure 4.2.3(a)). This hysteresis was probably due to the presence of the indium nitrate groups $In(NO_3)_3$ from the indium nitrate hydrate [$In(NO_3)_3$•$x(H_2O)$] precursors. In an effort to remove the operating hysteresis from our devices, the TFTs were annealed at more

high temperature at 350 °C for 1 hour. Unfortunately this step resulted in highly conductive transistor characteristics (Figure 4.2.3(b)). The latter was considered to be due to the formation of indium hydrate $In(OH)_3$ or non-stoichiometric i.e. metal ion rich-phase, of indium oxide films. Thus additional thermal annealing at higher temperature of 350 °C in ambient for 2 hours was applied for complete conversion of the precursor film to indium oxide (Figure 4.2.3(c)). As illustrated in Figure 4.2.4, stable and high performance InO_X TFTs were obtained via this post-processing high temperature-annealing step. The extracted value of the electron mobility in the saturation regime was in the range of 2-5 cm^2/V.s with the TFTs exhibiting high on-off current ratio (>10^5).

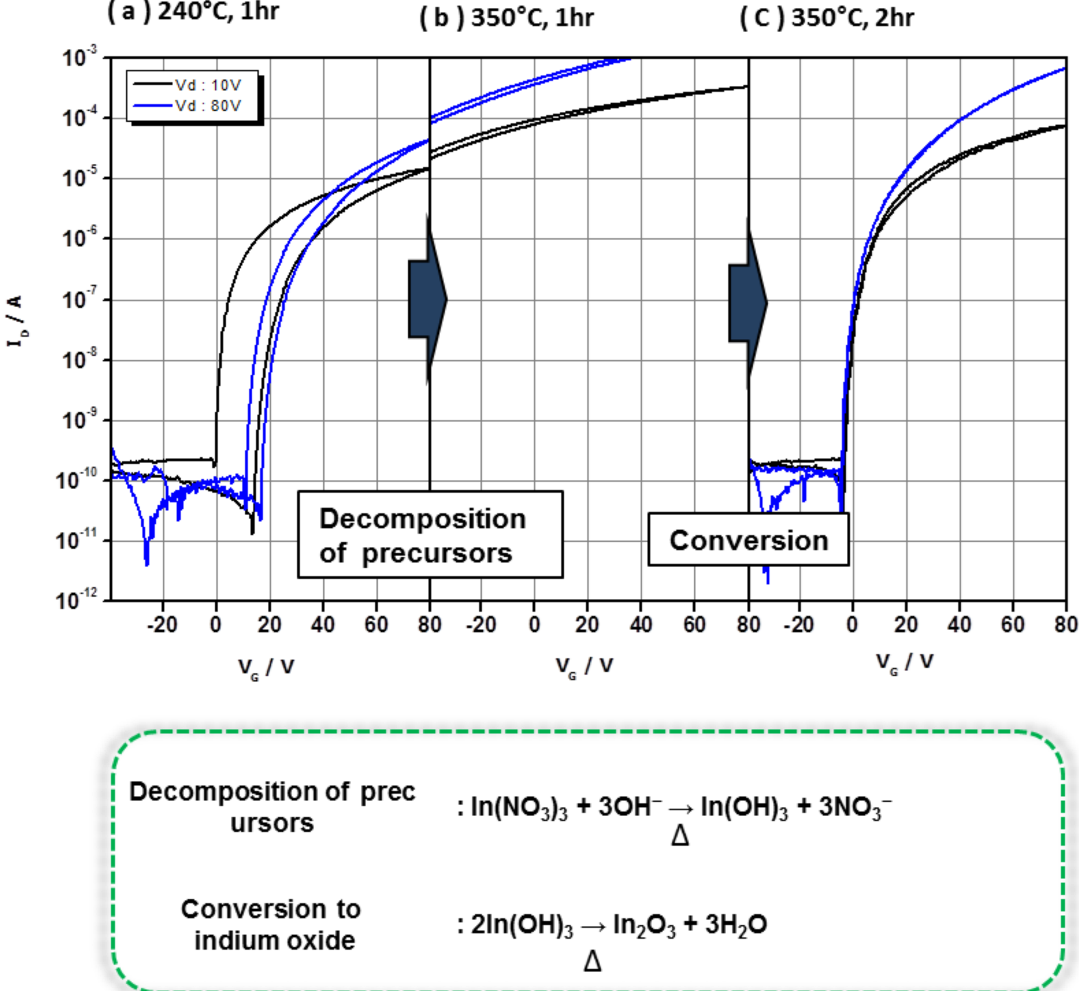


Fig.4.2.3. The evolution of saturated (V_D = 80 V) transfer characteristics of bottom-gate, top-contact InO TFTs according to the increasing annealing temperature and time. (a) 240 °C, 1h. (b) 350 °C, 1h. (c) 350 °C, 2h. Decomposition of the indium nitrate groups took place through the annealing the InO films at 350 °C, 1h. But, only conductive films were formed. For the semiconducting films of InO, additional thermal annealing at 350 °C, 2h was applied.

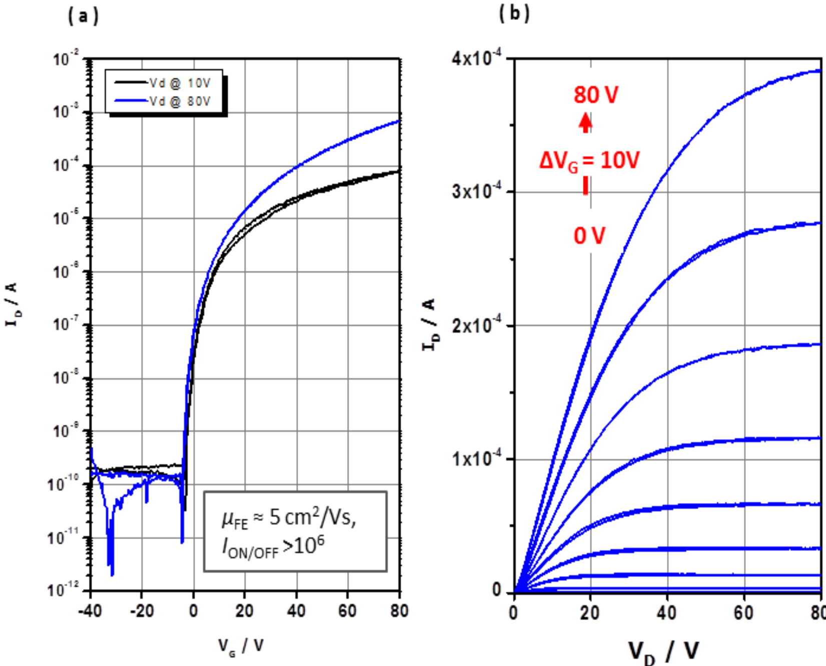


Fig.4.2.4. (a) Linear (V_D = 10 V) and saturated (V_D = 80 V) transfer characteristics of a bottom-gate, top-contact TFT with channel width W =1000 µm and channel length L = 50 µm, fabricated with InO films on 200 nm-thick SiO_2 dielectric by spin casting. (b) Output characteristics of the InO based TFT.

If the solution-processed oxide semiconductor films according to the various annealing conditions were investigated with X-ray photoelectron spectroscopy and Fourier transform infrared spectroscopy etc, the evolution of the transistor characteristics could be understood in more detail.[93]

4.2.4 Summary and Conclusions

In summary, stable and high-performance solution-processed n-channel ZnO and InO transistors were successfully demonstrated. For both types of devices, the extracted electron mobility values were almost identical and in the range of 0.5-5 cm^2/V.s. As-prepared devices showed high current on-off ratios (>10^5) and turn-on voltages close to 0 V. The relatively high performance was attained in devices annealed at temperatures in excess of 300 °C due to complete decomposition of the precursor materials. Annealing of the devices below the decomposition temperature resulted in TFTs with significant operating hysteresis and lower electron mobility values. In the case of indium oxide semiconductor, an additional oxidation step was required for converting the conducting state of the channel layer to an intrinsic-like semiconducting state. Corrosive ammonia solution was required for dissolving the zinc oxide,

while deionized water was chosen for the preparation of the indium oxide precursor formulations. Therefore, indium oxide was selected as the standard semiconducting material for fabricating the SAG transistors via a-Lith, which will be discussed in the next chapter.

	Zinc oxide (ZnO)	Indium oxide (InO)
Mobility [cm^2/Vs]	1 ~ 5	1 ~ 5
On/off ratio *	> 10^5	> 10^5
Process Temperature *	~ 300 °C	~ 350 °C
Solvent	Ammonia	D.I water
Orthogonality*	Corrosive	Proper

- Orthogonality to electrode and organic interlayer
- on/off ratio from the devices on 200 nm-thick SiO_2 dielectric

Aluminum in ammonia

Table.4.2. Comparisons between ZnO and InO transistors.

4.3 Dielectric materials for low-voltage transistor operation

4.3.1 Introduction

In an effort to lower the operating voltage of the thin-film transistors, the use of high permittivity (high-*k*) dielectric materials was investigated. The value of capacitance of the dielectric layer is expressed as:

$$C = \frac{\kappa \epsilon_0 A}{t} \tag{4.1}$$

where κ is a relative dielectric constant, ϵ_0 is a dielectric constant in vacuum, A is a geometrical area of the dielectric layer and t is the thickness of the dielectric layer. In addition, the value of the capacitance of the dielectric materials is calculated from the first terms of Taylor expansion of the total charge around the applied operating point, $V = V_S$ and is expressed as:

$$Q = f(V_S + v_s) \approx f(V_S) + \left.\frac{\partial f(V)}{\partial V}\right|_{V=Vs} (v_s) \tag{4.2}$$

$$f(V_S) : constant\ charge\ , \left.\frac{\partial f(V)}{\partial V}\right|_{V=Vs} (v_s) = incremental\ charge$$

$$q = \left.\frac{\partial f(V)}{\partial V}\right|_{V=Vs} (v_s) = Cv_s \tag{4.3a}$$

$$C = \left.\frac{\partial f(V)}{\partial V}\right|_{V=Vs} \tag{4.3b}$$

On the basis of these equations high geometrical capacitance can be achieved through the use of high-κ dielectric materials and/or by decreasing the thickness of the dielectric layer. Historically, high- κ dielectric materials such as zirconium oxide ($\epsilon_r = 20-40$), hafnium oxide ($\epsilon_r = 20-30$) and aluminium oxide ($\epsilon_r = 9.5$) have been developed for Si-technology. [102] As the channel length of state-of-the-art MOSFETs has been scaled down, the thickness of gate oxide would be decreased accordingly in order to avoid adverse effects associated with the short transistor channel. Although silicon dioxide ($\epsilon_r = 3.9$) is a stable insulator, the decrease of its thickness below 2 nm results to high gate leakage current - a problem that is impossible to overcome due to physical limitations. Use of high-κ dielectric materials enables the use of thicker gate dielectric layers while preserving the strong capacitive coupling of the gate to the channel. For thin-film transistors, these high-κ dielectric materials have been studied not only for the purpose of lowering the operating voltage but also for improving the performance of devices, especially in metal oxide thin-film transistors and circuits. For instance, there have been numerous reports on the enhancement of metal oxide TFT performance when high capacitive dielectric materials were employed[15].

In this chapter two recently proposed gate dielectric materials, namely ion-gel dielectrics[103–107] and SAM dielectrics have been studied.[60,108–113] The former family of materials is known as ultra-high capacitive materials due to the formation of the electrical double layer, while the latter is known for its nano-metre layer thicknesses due to closely packed self-assembly of the molecules on the surface of suitably treated gate electrodes. Resulting TFTs were studied in terms of operating voltage characteristics as well as charge carrier mobility since both properties are of critical importance for any practical application in the field of large-area electronics.

4.3.2 Ion-gel gate dielectric material

Experimental

An ion-gel gated transistor with a top gate top contact configuration was fabricated as shown in Figure 4.3.1. First a 50-nm-thick Au source/drain electrodes were deposited by thermal evaporation on cleaned Si/SiO_2 substrate through a shadow mask. The channel length and width of the devices were 100 μm and 1000 μm respectively. As a reference semiconducting material for evaluating the ion-gel gate dielectric material, poly 3-hexylthiophene (P3HT) was employed. The molecular weight of P3HT was 69K /mol with PDI=1.65 and RR>97%. P3HT was dissolved in chlorobenzene (5mg/ml) and was spin-casted onto the substrate at 1000 rpm for 60 s and subsequently annealed on a hot plate at 120°C for 20 min in nitrogen ambient. The thickness of the resulting semiconductor layer was ~20 nm. The ion-gel material was prepared by gelation of a triblock copolymer, poly (styrene-block-ethylene oxide-block-styrene) (PS-PEO-PS) with an ionic liquid, 1-ethyl-3-methylimidazoliumbis (trifluoromethylsulfonyl) imide ([EMIM][TFSI]) in acetonitrile. The mixing ratio was 9 wt% ionic liquid, 1wt% polymer and 90 wt% solvent. The resulting solution was drop-casted on to the isolated semiconducting region and kept under vacuum at 10^{-2} torr for 1 hour in order to dry. Device performance was characterized using drop cast silver-paste electrodes acting as the gate terminal. For capacitance measurements, following deposition of the bottom Au electrode (50 nm) the ion-gel material was drop-casted and dried followed by the deposition of the solution processed silver-paste top electrode. The values of capacitance were measure using a LCR meter from 20 Hz to 10^5 Hz. Electrical characterisation of the devices was carried entirely inside a N_2 glove box.

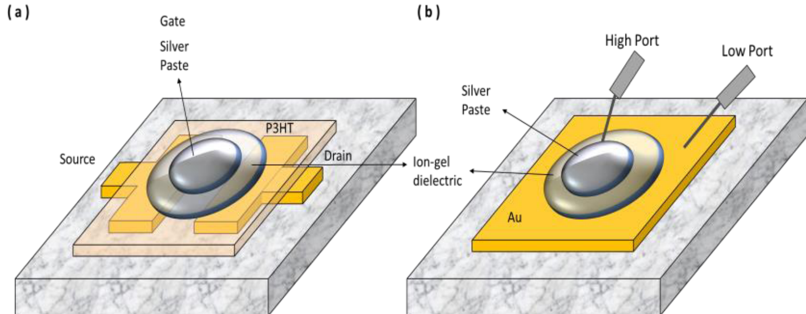


Fig.4.3.1. (a) Schematic diagrams of devices for measuring the performance characteristics of ion-gel gated transistors. (b) Illustration for the measurement for the values of the capacitance of the ion-gel dielectric.

Results and Discussion

The geometric capacitance of an ion-gel dielectric material was first measured. As shown in Figure 4.3.2, the value of capacitance was extremely high and higher than any other commonly known high capacitance dielectric material. Maximum values of over 10 $\mu F/cm^2$ were typically obtained. This value however decreased from 11.4 $\mu F/cm^2$ to 3.4 $\mu F/cm^2$ as the operating frequency increased from 20 Hz to 10^5 Hz. As previously shown, this frequency dependent characteristic can be explained in terms of ion-movement in the dielectric layer as in the Figure 4.3.3[106]. When the electric field is applied on the layer, positive and negative ions move according to the bias/electric field direction. This displacement induces the electric double layer and enables exceptional high capacitance values to be achieved. However, for this polarization to occur certain amount of time is required for aligning and saturating the electric-double layer. This is the reason for the frequency dependent capacitance characteristics in all ion-gel gate dielectric materials. Due to the low limit of frequency of impedance measurement system, measuring the values of capacitance in the range of the operating frequency could not be conducted (<1 Hz). The typical operating frequency of the ion-gel gated transistor was below 0.1 Hz, which will be discussed in the following section in more detail. Thus, the values were deduced from the fitting with a Debye relaxation model (exponential decay model). The assumed values were higher than the measure value of 11.4 $\mu F/cm^2$ at 20 Hz, but it was saturated and the values remained almost constant at 13.45 $\mu F/cm^2$ (<0.1Hz).

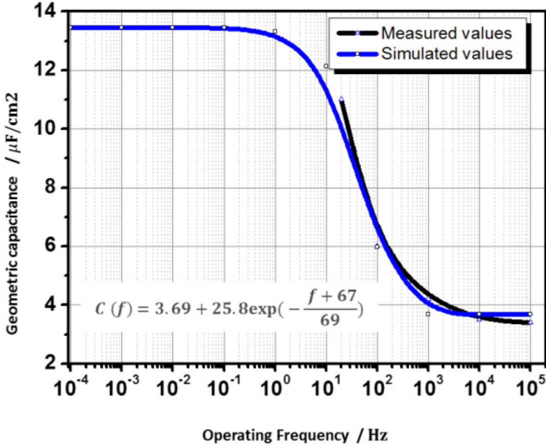


Fig.4.3.2. The frequent dependent geometric capacitance of an ion-gel dielectric material from 20 Hz to 10^5 Hz. Measured values were depicted in black line and simulated values were depicted in blue line. Inset: The fitting model according to the Debye relaxation model.

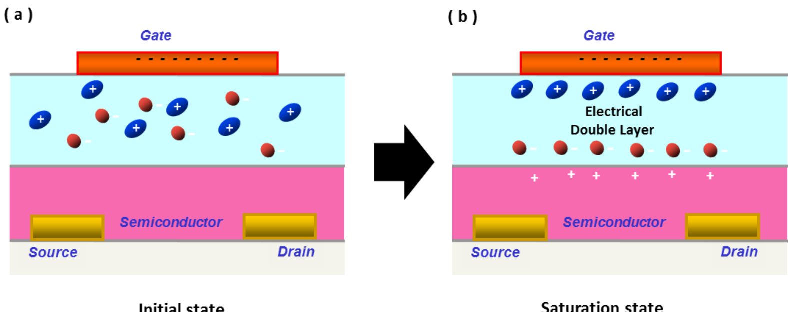


Fig.4.3.3. Schematic illustrations of the frequent dependent movement of the ion-gel dielectric material. (a) Initial state, randomly distributed state. (b) Saturation state for the formation of the electrical double layer in the ion-gel dielectric.

Next, the device performance of conventional poly 3-hexylthiophene (P3HT) transistors was investigated, prior to characterizing the ion-gel dielectric-based TFTs. Although high operating voltage was required due to the low geometric capacitance of the 400 nm-thick SiO_2 (8.63 nF/cm^2), the device exhibit good operation as shown in Figure 4.3.4. The on-current level of the TFT was over 10^{-6}A at the applied gate bias of -80 V with almost zero hysteresis. The extracted values of hole mobility were 0.003 cm^2/V.s and 0.005 cm^2/V.s in the linear and saturation regimes, respectively. These values are comparable with mobility values published previously (~ 10^{-3} cm^2/V.s). [26,110,111,114]

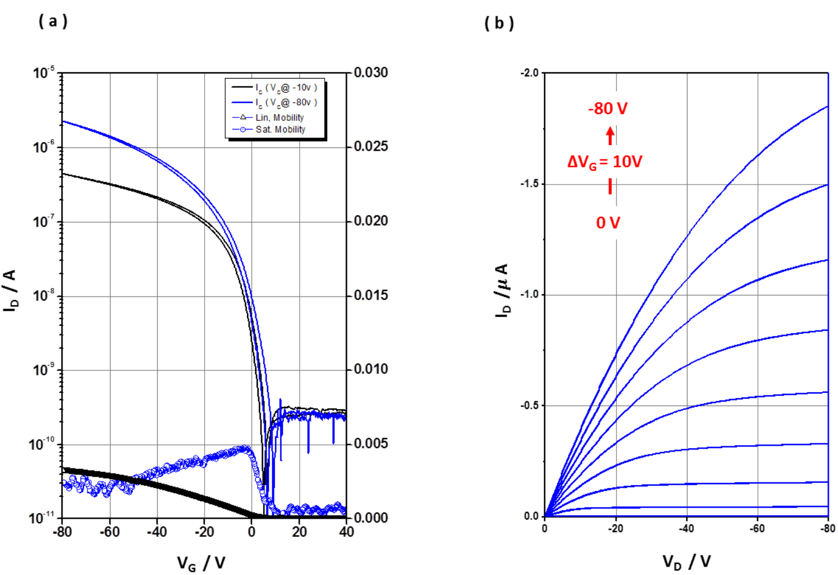


Fig 4.3.4. (a) Linear (V_D = 10 V) and saturated (V_D = 80 V) transfer characteristics of a bottom-gate, top-contact TFT with channel width W =1000 μm and channel length L = 50 μm, fabricated with P3HT on 400 nm-thick SiO_2 dielectric by spin casting. (b) Output characteristics of the P3HT TFT.

Following the deposition of the ion-gel gate dielectric onto the P3HT, the TFT performance was studied. As shown in Figure 4.3.5, low-voltage transistor operation can indeed be achieved. As can be seen, the operating voltage reduces to a few volts due to the high geometric capacitance of the ion-gel dielectric. The on-current level at the applied gate bias of -3 V reaches values of over 10^{-4} A, while the off-level is kept near 10^{-8}A. This behaviour results in high current on-off ratio (>10^{4}), which is highly desirable for many electronic applications. Furthermore, the turn-on voltage remains low and close to 0 V with negligible hysteresis.

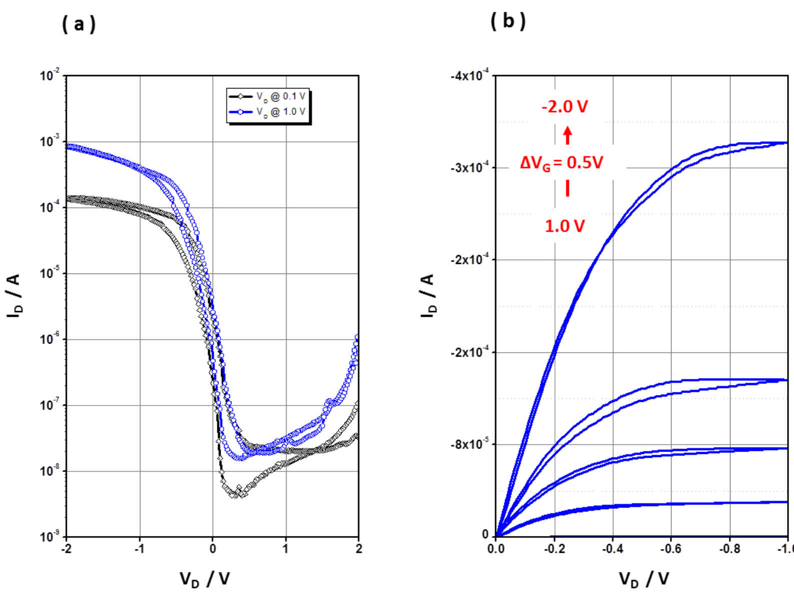


Fig.4.3.5. (a) Linear (V_D = 0.1 V) and saturated (V_D = 1.0 V) transfer characteristics of a top-gate, top-contact TFT with channel width W =1000 μm and channel length L = 100 μm, fabricated with P3HT films on ion-gel dielectric. (b) Output characteristics of the ion-gel gated P3HT transistor.

However, we do stress that in order to achieve this operating characteristics the device needs to be operated at slow voltage scanning rates (ΔV_G = 1 mV/s). When the device is operated at higher sweep rate, the performance of devices is found degrade significantly as illustrated in Figure 4.3.6. Here, the on-current is seen to decrease by over 100 times from 1.6 × 10^{-4} A to 1.4 × 10^{-6} A as the gate voltage sweep rate increased from 1 mV/s to 1000 mV/s. The value of hysteresis was also increased significantly from 0.2 V to 2.1 V. The scan range of 5 V in the direction of forward and reverse bias at the sweep rate of 1 mV/s requires 1000 s, thus, the sweep rate in Hz would be approximately 10^{-4} Hz. Similarly, the sweep rate at 10 mV/s, 100 mV/s and 1000 mV/s was approximately equal to an operating frequency of 10^{-3}

Hz, 10^{-2} Hz and 10^{-1} Hz, respectively. The extracted values of mobility with the value of capacitance of 13.45 μF/cm^2(<0.1Hz) were also dependent on the operating frequency. The value of mobility was 23 cm^2/V.s at 1 mV/s, 6 cm^2/V.s at 10 mV/s, 0.5 cm^2/V.s at 100 mV/s and 0.06 cm^2/V.s at 1000 mV/s. This frequency dependent performance of device can be understood by considering electrochemical doping effect in the organic semiconductor by the migrated ions and has been discussed extensively in the literature.[106,115]

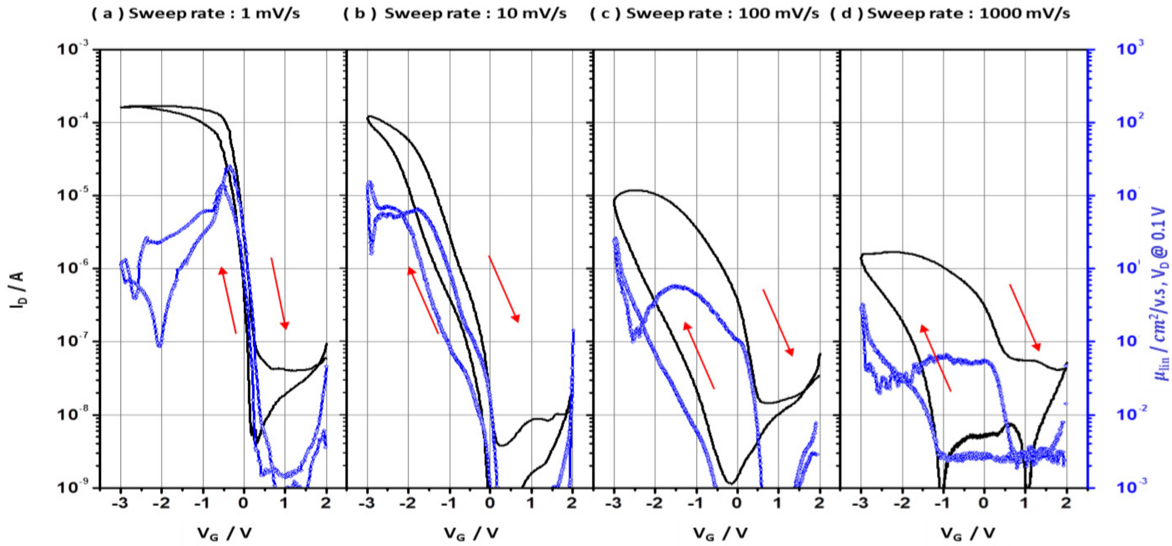
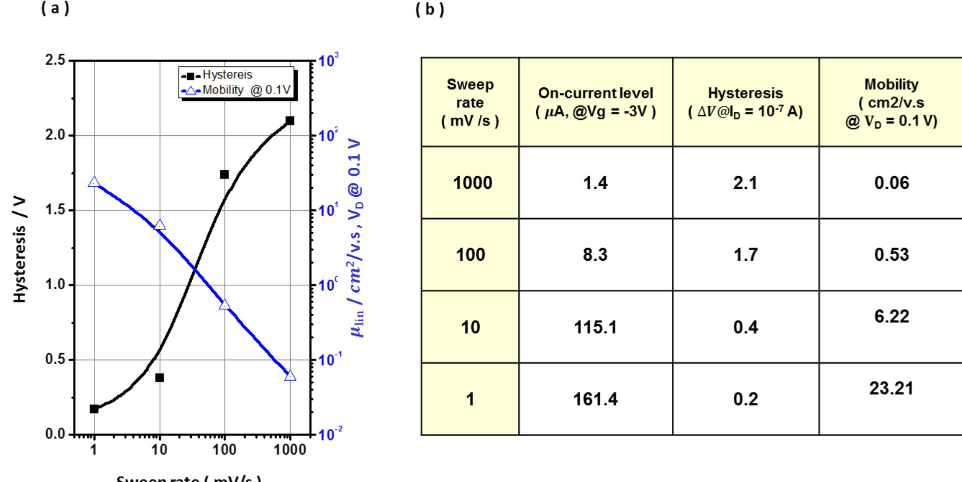


Fig 4.3.6. The degradation of linear (V_D = 0.1 V) transfer characteristics of the ion-gel gated P3HT transistor as increaing the sweep rate.(S/R) (a) At S/R = 1 mV/s. (b) At S/R = 10 mV/s. (c) At S/R = 100 mV/s. (d) At S/R = 1000 mV/s.

When a permeable semiconducting material, such as P3HT, is used as the semiconducting layer, the ions in the ion-gel material can penetrate into the semiconductor and enhance its conductance as illustrated in Figure 4.3.8. This enhancement reduces the density of traps in the interface between the semiconductor and the insulator, through deactivation, and the transport of carriers appears less scattered, thus the hole mobility value increases. Additionally, the doping effect can improve the charge injection rate from the source/drain electrodes by lowering the Schottky barrier between the electrode and the semiconductor, due to narrowing of the depletion region width, thus the performance is enhanced. However, this electrochemical doping process is time-dependent. If the device is operated at high frequency, the doping process cannot follow the high frequency field, thus the mobility enhancement cannot be saturated. This gives rise to a strong frequency dependent performance. Similarly, the hysteresis of the device may also be attributed to the

same electrochemical doping effect. As shown in Figure 4.3.6, the channel current in the reverse bias sweep appears higher than in the forward bias sweep.



Sweep rate (mV /s)	On-current level (μA, @Vg = -3V)	Hysteresis (ΔV@I_D = 10^{-7} A)	Mobility (cm2/v.s @ V_D = 0.1 V)
1000	1.4	2.1	0.06
100	8.3	1.7	0.53
10	115.1	0.4	6.22
1	161.4	0.2	23.21

Fig 4.3.7 (a) Evolution of the operating hysteresis and hole mobility with gate voltage sweep rate measured for an ion-gel gated P3HT transistor. (b) Summary of key transistor parameters extracted from TFTs measured at different gate voltage sweep rates.

If the frequency dependent conductance and trap density of the semiconductor were investigated in more detail, these TFT characteristics could potentially be understood and adequately addressed. However, this is beyond the scope of the work described in this thesis. Instead, our work was focused in using this interesting dielectric material as a versatile tool for the manufacturing of short channel SAG TFTs.

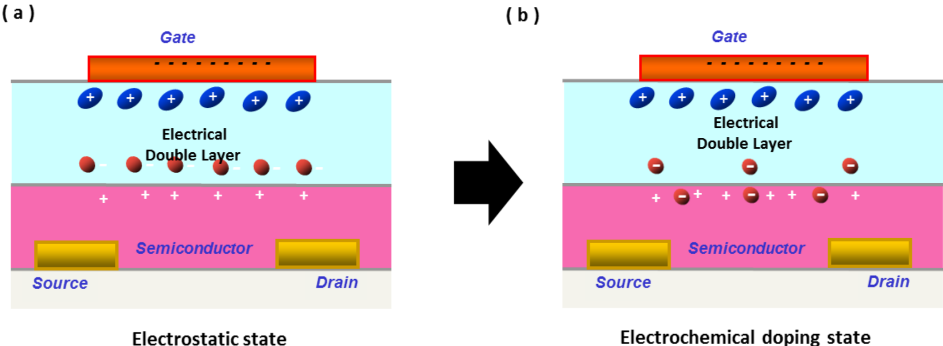


Fig 4.3.8 Schematic illustrations of the electrochemical doping effect of the ion-gel dielectric on the P3HT semiconductor. (a) Electrostatic state when it biased at faster rate. (b) Electrochemical doping state when it biased at slow rate. Mobile ions in the ion-gel dielectric could be penetrated onto the semiconductor layer, resulting the channel conductance might be enhanced significantly.

4.3.2 Self-assembled monolayers dielectric materials for metal oxide TFTs

Experimental

The SAM dielectric layer was developed and used in solution-processed metal oxide semiconductor TFTs based on the bottom-gate, top-contact configuration. As shown in Figure 4.3.9, a 50 nm-thick Al gate electrode was deposited by thermal evaporation onto Si/SiO_2 substrate through a shadow mask. Next, the surface of aluminium was oxidized by exposing it to UV ozone treatment for 1 hour or thermal annealing at 200 °C for 10 minutes in ambient air. Following, the SAM treatment was performed by immersing the substrates in the SAM solution (2 mM 16-Phosphonohexadecanoic acid, PHPA, in IPA or Ethanol) for 12 hours and anneal them at 150 °C for 30 minutes in air. After rinsing the sample with IPA several times and dried with nitrogen gas, an indium oxide semiconducting layer was formed by spin casting an indium (III) nitrate hydrate [0.5M $In(NO_3)_3{\cdot}x(H_2O)$] D.I. water solution at 4000 rpm for 60 seconds followed by thermal annealing at 350 °C for 3 hours in ambient air. Lastly, 50 nm-thick Al for a source-drain electrodes were deposited via thermal evaporation through a shadow mask. The channel length and width of the TFTs were 50 μm and 1000 μm, respectively. Measurements of the geometric capacitance and the leakage current were performed using the conventional metal-insulator-metal structure. Capacitance-voltage characteristics were acquired using a LCR meter in the frequency range 100-10^7 Hz. All measurements were performed in a N_2 glovebox.

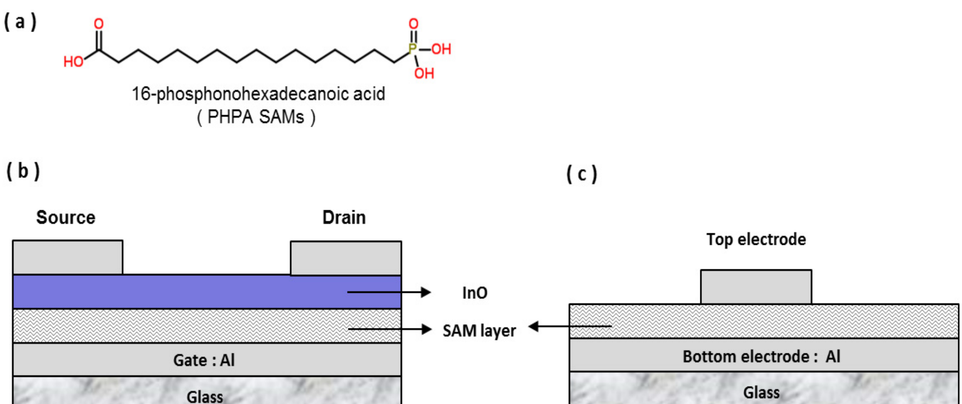
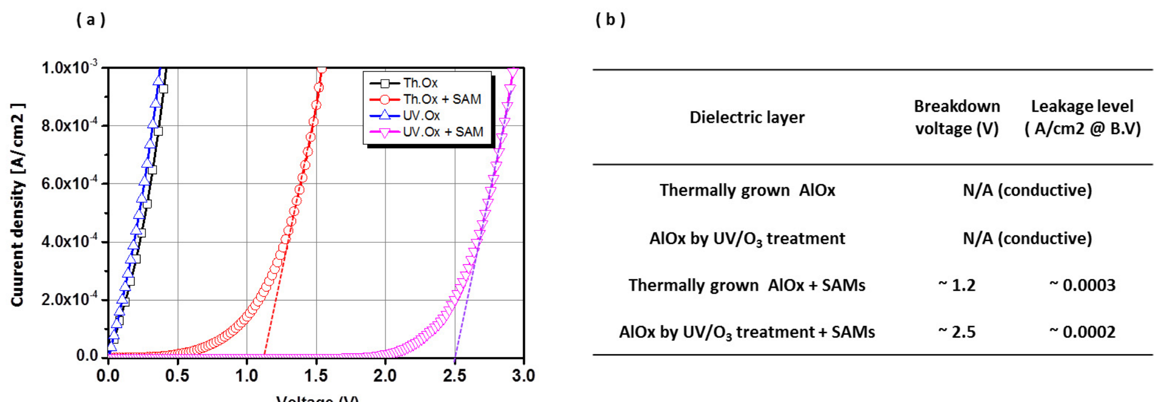


Fig 4.3.9 (a) Chemical structure of 16-Phosphonohexadecanoic acid. (b) Schematic diagrams of devices for measuring the performance characteristics of the transistor on the SAMs based dielectric. (c) Illustration for the measurement for the values of the capacitance of the SAMs based dielectric.

Results and Discussion

Firstly, the insulating properties of the SAM dielectric were investigated. Although aluminum oxide is a frequently used and stable dielectric material, here the native alumina appears conductive and unable to deliver good insulating characteristics. Specifically, the current level was over 1.0×10^{-3} A/cm^2 at an applied bias of 0.5 V without any rectifying characteristics. We attribute this to the ultra-thin nature of the native alumina and/or non-stoichiometric aluminum oxide. However, when the self-assembled monolayers were applied/functionalized on the surface of the Al-AlO_X electrode, there were dramatic changes in the current-voltage characteristics of the devices. Specifically, all resulting devices appear to be highly insulating with excellent reproducibility. Some of the devices also exhibited rectifying characteristics at applied voltages of <1 V. In addition, the breakdown voltage, which it is here defined as the bias potential where the current starts increasing exponentially, was identified as 1.2 V with the leakage current level of 3.0×10^{-4} A/cm^2. This insulating characteristics were further improved if the aluminum oxide layer was grown by UV ozone treatment with the breakdown voltage increasing to 2.5 V while the leakage current decreased to $<2.0\times10^{-4}$ A/cm^2. Unlike the ion-gel dielectric layer, the hybrid SAM dielectric grown on UV ozone treated aluminum gate electrodes showed a stable operation up to 10^5 Hz. The geometric capacitance of the layer was in the range of 500-600 nF/cm^2 as depicted in Figure 4.3.11. This value was comparable with the precious reported values of 500-800 nF/cm^2.



Dielectric layer	Breakdown voltage (V)	Leakage level (A/cm2 @ B.V)
Thermally grown AlOx	N/A (conductive)	
AlOx by UV/O_3 treatment	N/A (conductive)	
Thermally grown AlOx + SAMs	~ 1.2	~ 0.0003
AlOx by UV/O_3 treatment + SAMs	~ 2.5	~ 0.0002

Fig 4.3.10 (a) Current density versus applied bias and extraction of the break down voltage in devices based on differently processed alumina and alumina/SAM dielectric layers. (b) Summary of the extracted device parameters.

The existence of imperfections, such as pinholes, in the dielectric layer is commonly considered to be the source for the measured leakage current.[116] Pinholes or crevices in the

film create current pathways thought the insulating layer, leading to leakage current. In the past increasing the dielectric thickness and/or thermal annealing at higher temperature has been attempted. Here, SAM treatment appears to provide a simple solution for the formation of stable dielectric layers. As illustrated in the Figure 4.3.12, even aluminum oxide grown via UV ozone treatment or thermal annealing, still exhibits a high density of pinhole defects. These lead to high current and dielectric breakdown at relatively low electric fields. SAM treatment appears to be able to effectively passivate these pinholes and dramatically supress the leakage current. On the basis of these results it is clear that SAM functionalization provides a viable route to ultra-thin gate dielectrics.

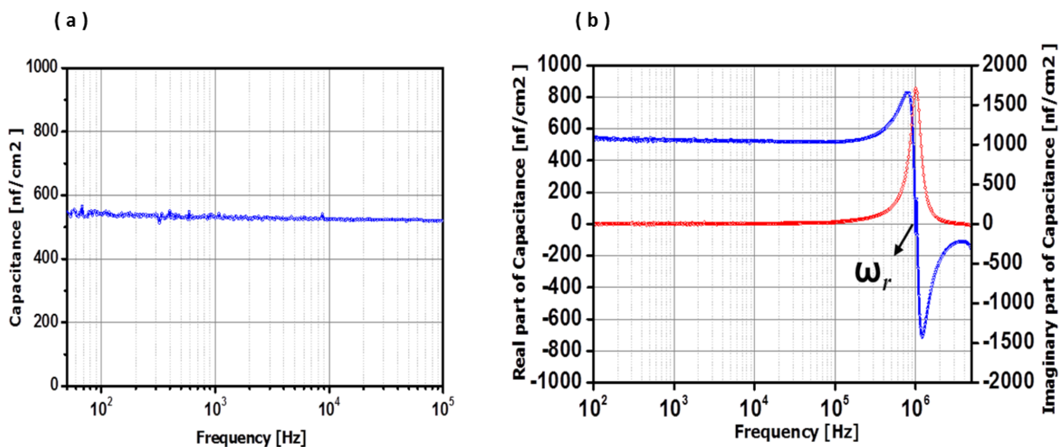


Fig 4.3.11 Values of the geometric capacitance of the hybrid SAMs dielectric layer for frequency signals. (a) Up to 10^5 Hz. (b) Up to 10^7 Hz. Resonance frequency of the hybrid SAMs dielectric layer, ω_r was near 10^6 Hz, where the maximum operation frequency of the device with the hybrid SAMs dielectric can be determined by this frequency.

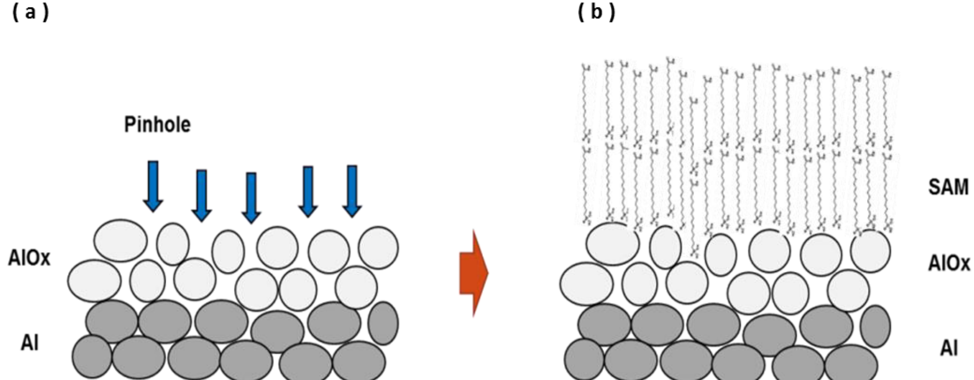


Fig 4.3.12 Schematic illustration of the passivation process occurring on the native oxide by SAMs treatment. (a) Native aluminum oxide dielectric. (b) SAMs treated aluminum oxide dielectric. A lot of density of pinhole and crevices could be passivated by the SAMs molecules.

Following the optimization of the hybrid SAM dielectric, low operating voltage TFTs were fabricated using solution-processed indium oxide layers acting as the channel material. The particular SAM dielectric used here was the 16-Phosphonohexadecanoic acid, which is terminated with hydroxyls group. The resulting hydroxyl terminated surface exhibits hydrophilic surface characteristics and as such enables solution deposition of water based precursor formulations including that of the indium nitrate used here. Due to its high value of geometric capacitance (500-600 nF/cm^2), low-voltage operating TFTs were successfully demonstrated. As shown in the Figure 4.3.14, the on-current level of the device was over 10^{-6} A at the applied gate bias of 1.5 V, while the off-level was kept near 10^{-9} A, resulting in a high current on-off ratio of >10^3. The extracted value of the electron mobility was ~1 cm^2/V.s. On the other hand, the off-current state of the SAMs-based TFTs with thermally grown aluminum oxide was not well-defined and fluctuated significantly due to severe leakage currents (Figure 4.3.13). This result illustrates the practical problem of using unstable aluminum oxide layers formed by simple thermal annealing and was avoided in all subsequent experiment with the remaining of the work focusing on the use of UV ozone treated Al gate electrodes.

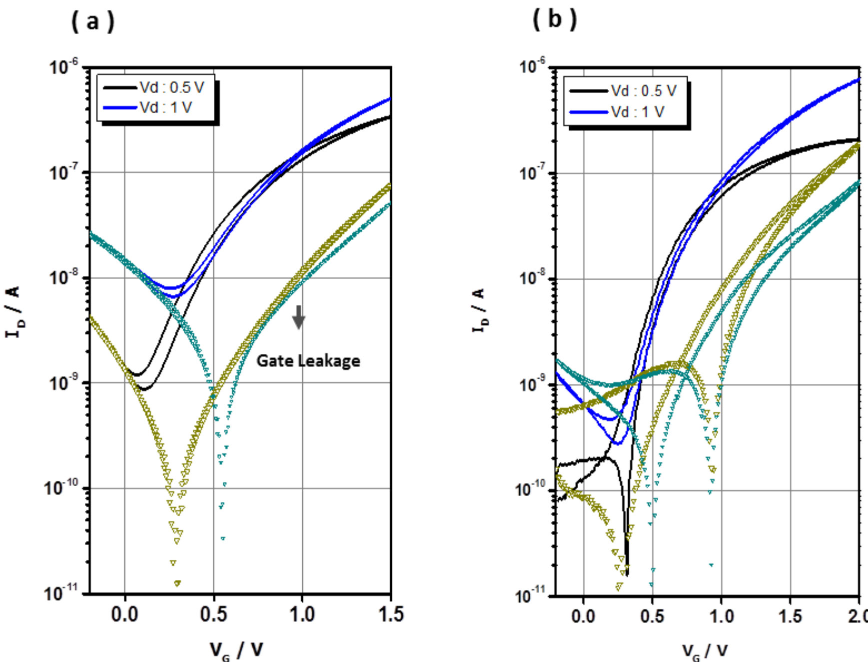


Fig 4.3.13 Linear (V_D = 0.5 V) and saturated (V_D = 1 V) transfer characteristics of a bottom-gate, top-contact TFT with channel width W =1000 μm and channel length L = 50 μm, fabricated with InO films. (a) On the thermally grown alumina prior to SAM functionalization. (b) On the UV ozone treated alumina prior to SAM functionalization.

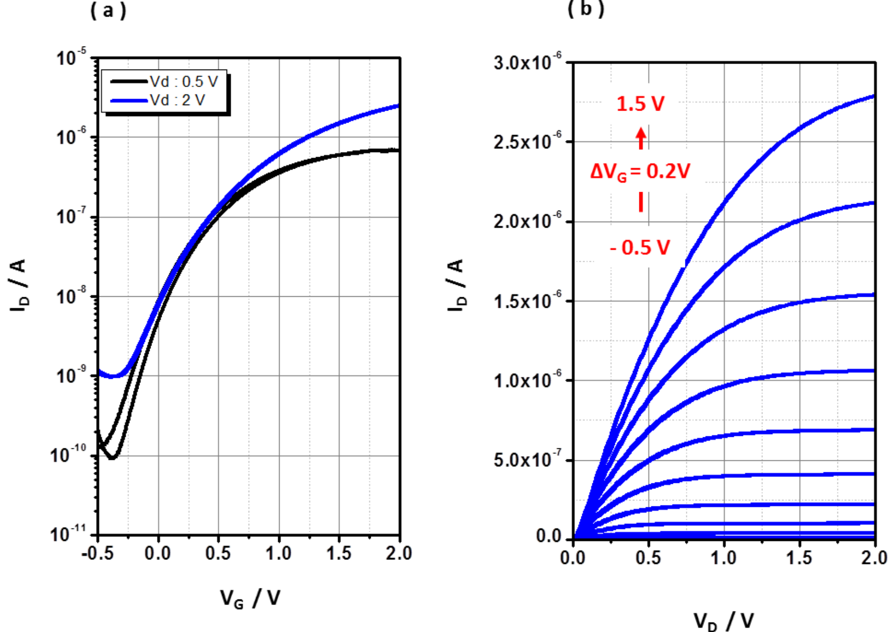


Fig.4.3.14 (a) Linear (V_D = 0.5 V) and saturated (V_D = 2.0 V) transfer characteristics of a top-gate, top-contact TFT with channel width W =1000 μm and channel length L = 50 μm, fabricated with solution-processed indium oxide on the hybrid alumina/SAM dielectric. (b) Output characteristics of the solution-processed indium oxide transistor.

4.3.3 Summary and Conclusions

In summary, two different types of solution processed high geometrical capacitance gate dielectric materials, namely ion-gel and SAMs, were developed and evaluated. In the case of the ion-gel materials, the ultra-high geometrical capacitance (~ $\mu F/cm^2$) allowed the fabrication of organic TFTs with operating voltages in the range of a few Volts. However, the performance of these devices was found to degrade significantly as the operating frequency increased. The deduced value of the hole mobility changed from 23 $cm^2/V.s$ to 0.06 $cm^2/V.s$ as the operating frequency increased from 10^{-4} Hz to 10^{-1} Hz. This ultra-low limit of operating frequency was considered to be a serious bottleneck for implementing the technology into real-life electronics. Hence, another dielectric material, which also allows for low-voltage operation, was developed. Specifically, a hybrid alumina-SAM dielectric layer was developed and applied in low-voltage indium oxide TFTs processed from solution. Using the native aluminium oxide layer that was grown by UV-ozone treatment of the Al gate electrodes at room temperature, a phosphonic SAM was functionalized from solution resulting in the formation of stable and high geometric capacitance (500-600 nF/cm^2) dielectric layers. The breakdown voltage of the resulting layers was typically ~2.5 V with a

leakage current density of 2.0×10^{-4} A/cm^2. When combined with solution processed indium oxide semiconducting layers, low voltage (<1.5 V) TFTs with electron mobility of ~1 cm^2/V.s and high on-off ratio (>10^3) were demonstrated, clearly highlighting the tremendous potential of this interesting and simple to implement dielectric technology.

4.4 Process architecture of self-aligned gate transistors by a-Lith

Experimental

The a-Lith technic was applied for fabricating the self-aligned gate TFT architecture shown in Figure 4.4.1. In brief, the organic interlayer *Benzocyclobutene photoresist* (*CYCLOTENE3000, Dow Chemical*) was spin-casted at 4000 rpm for 60 s and cured on a hot plate at 300°C for 1 hour in a N_2 filled-glove box. Following, a 50-nm-thick Aluminium gate electrode was deposited by thermal evaporation through a shadow. The Al electrodes were then thermally annealed at 200 °C for 10 minutes in ambient air in order to form a thin layer of native alumina. Next, SAM functionalization was performed by immersing the samples in a SAM solution of 5 mM Octadecylphosphonic acid (ODPA) in IPA for 12 hours. Samples were then removed, dried and annealed at 150 °C for 30 minutes in air. After rinsing the sample with IPA and dried with nitrogen gas, an 80 nm-thick aluminium electrode, which will be used to form the discrete source and drain electrodes via a-Lith, was deposited by thermal evaporation in high vacuum through a shadow mask. Overlap regions between the top Al electrode and the bottom SAM treated Al gate electrode was subsequently removed via a-Lith using an adhesive tape. This step resulted in the formation of the separated source and drain electrode along the gate electrode as shown in Figure 4.4.1 step (V).

For the formation of the hybrid SAM dielectrics, samples were treated with UV-ozone for 1 hour again and then immersed in the SAM solution of 2 mM 16-Phosphonohexadecanoic acid, PHPA in IPA or Ethanol for 12 hours and annealed at 150 °C for 30 minutes. After rinsing the sample an indium oxide semiconducting layer was deposited via spin casting of the Indium (III) nitrate hydrate solution [0.5M $In(NO_3)_3 \cdot x(H_2O)$ in D.I. water] at 4000 rpm for 60 seconds and subsequent thermally annealed at 350 °C for 3 hours in ambient air. The resulting transistor channel length and width were 1000 μm and 50 μm, respectively. Electrical characterization of the devices was performed using a semiconductor parameter analyzer (Agilent B2900A). For measuring the operating frequency of the device, a common drain amplifier configuration was employed. Here a square wave input signal from a

function generator (Agilent 33220A) was applied to the gate electrode of the transistor, while a fixed voltage was applied to the drain electrode. A 100 Ohms resistor was connected in the source node and the output signal in the resistor was transformed with a current amplifier (Stanford research system SR570) and measured with an oscilloscope (Agilent DSO6014A). A schematic of the measurement set up is shown in Figure 4.4.2.

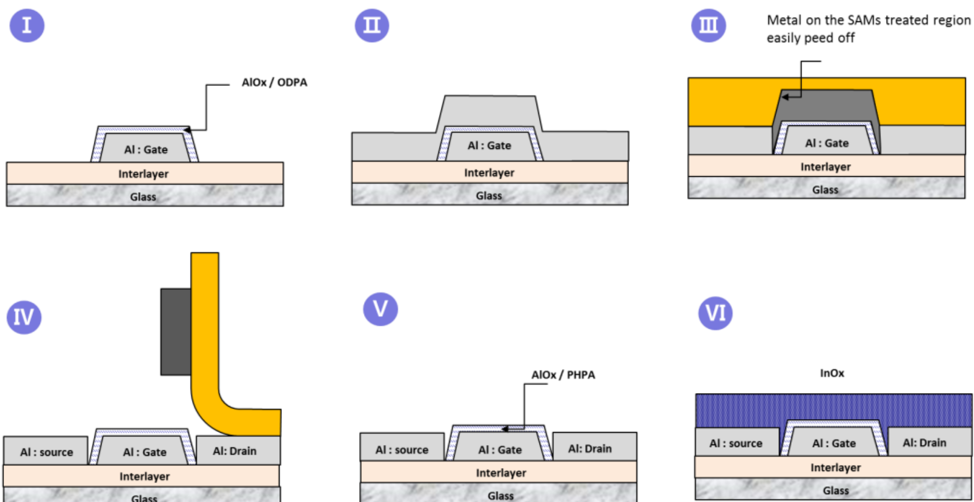


Fig 4.4.1 Schematic illustration of the process steps used to fabricate the SAGs TFTs by a-Lith.

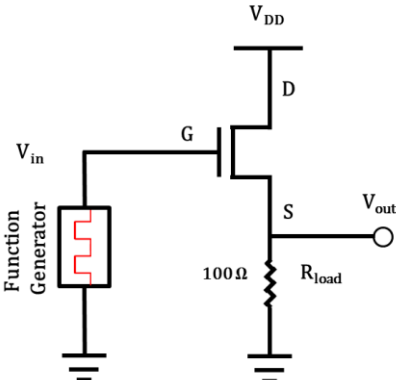


Fig 4.4.2 Common-drain amplifier circuit configuration for measuring the operating speed of the TFTs.

Results and Discussion

The resulting SAG TFT architecture developed by a-Lith was initially examined with an optical and atomic force microscope. Figure 4.4.3 shows the measured optical and AFM images of a representative TFT structure. The extracted value of the electron mobility for these SAG indium oxide based TFTs was in the range of 0.5-1 $cm^2/V.s$ with high current on-off ratios ($\sim 10^3$) (Figure 4.4.4). Both values are comparable to those extracted from

conventional TFT architectures, further demonstrating the applicability of the a-Lith method for the development of this rather demanding transistor configuration.

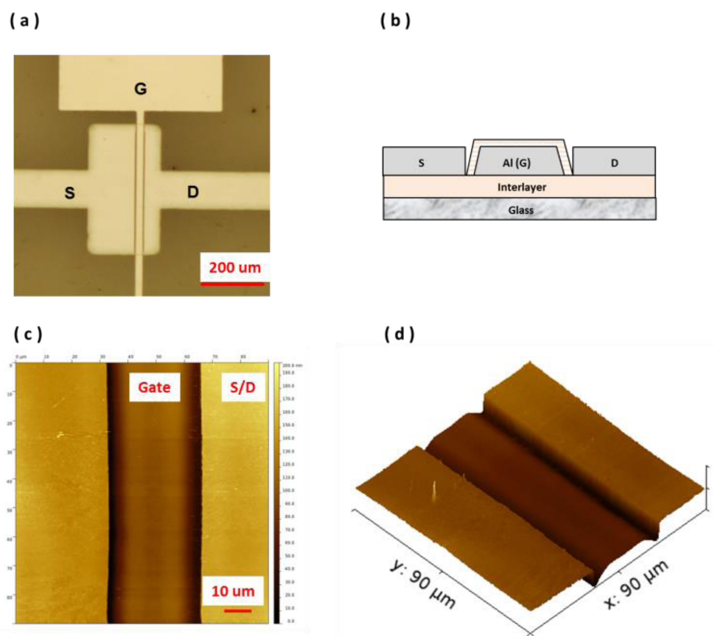


Fig 4.4.3 (a) Optical image of the SAG TFT structure. (b) Schematic cross-sectional view of the illustration of the SAG TFT structure. (c) Two-dimensional AFM image of the self-aligned gate sturcture. (d) Three-dimensional AFM image of the self-aligned gate sturcture.

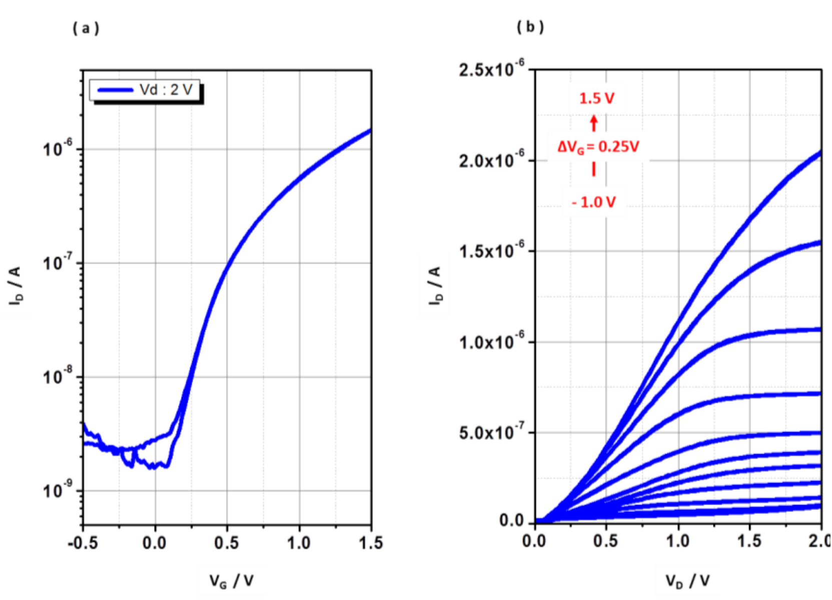


Fig.4.4.4 (a) Saturated (V_D = 2.0 V) transfer characteristics of the self-align bottom-gate, bottom-contact TFT with channel width W =1000 μm and channel length L = 50 μm, fabricated with solution-processed indium oxide on the hybrid alumina/SAM dielectric. (b) Output characteristics of the solution-processed indium oxide transistor.

Next, the cut-off frequency of the devices was simulated according to the Equation of 2.2.3. To this end a value for the electron mobility of 1 $cm^2/V.s$ was employed with an assumed value for effective gate bias ($V_{gs} - V_{th}$) of 1.5 V (Figure 4.4.5). Using these parameters a cut-off frequency for the conventional TFT structure (i.e. non-aligned gate) was calculated to be on the range of 3×10^3 Hz. This relatively low value is attributed to the significant S-D/G overlap length of 50 μm, which is comparable to the channel length of the transistor (50 μm). Performing the same calculations for the self-aligned TFT structure now, yields a maximum operating frequency of 1.4×10^4 Hz – nearly one order of magnitude higher than the non-aligned gate TFT. In both cases, the transistor channel length used was 50 μm. These calculations demonstrate the importance of the parasitic overlap length and how the SAG architecture can help to enhance the device performance

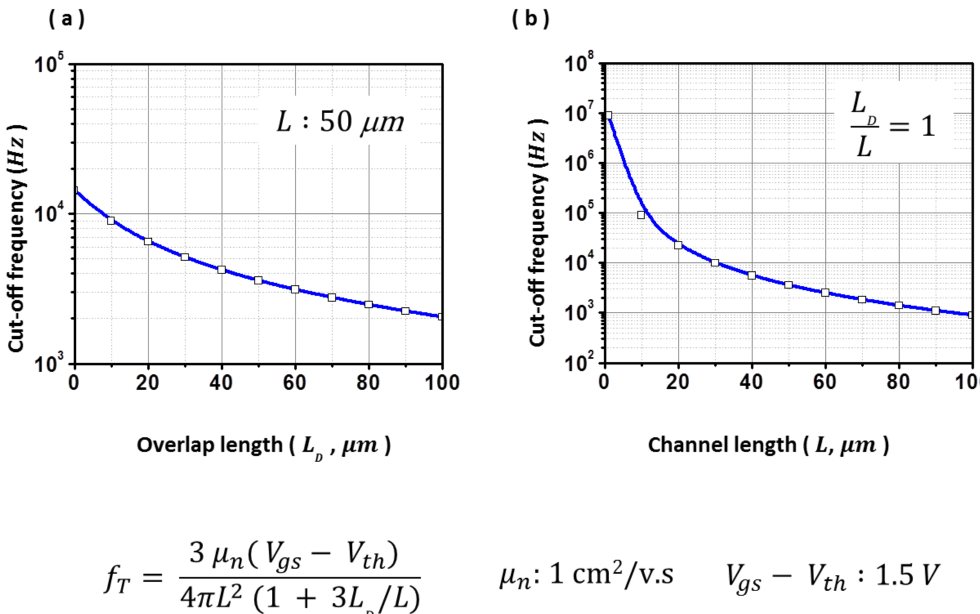


Fig 4.4.5 (a) Simulation results of the values of the cutt-off frequency according to the overlap length from 0 μm to 100 μm at the fixed channel length of 50 μm. (a) Simulation results of the values of the cutt-off frequency according to the channle length from 0 μm to 100 μm at the fixed ratio of unity between the channel length and the overlap length.

To investigate the operating speed of the SAG TFTs developed here, the common-drain amplifier configuration (Figure 4.4.2) was used for measuring the dynamic response of the devices. In this measurement configuration it is expected that when the gate bias (V_{in}) is low, the resistance of the channel is far larger than the load resistance of 100 Ohm. Thus, the V_{out} across the load resistance will be small. However, when a high gate bias (V_{in}) is applied to the device, the resistance of channel becomes small, and the V_{out} measured across the load

resistance increases according to the voltage-dividing rule between the TFT's channel and the load resistor. Hence, this common-drain circuit geometry is fundamentally non-inverting circuit, but a signal lag between the input and the output signal due to the RC network in the circuit. Therefore, by measuring the rise time of the output signal in this circuit (from 10 % to 90 % of the output voltage), the intrinsic cut-off frequency of the transistor can be deduced. The measured rise time of the SAG TFTs with the overlap length of 0 μm was measured to be about 20 μs for an applied input signal of 1 KHz, while that of a conventional TFT structure with a channel overlap length of 50 μm was 30 μs. (Figure 4.4.7) These results demonstrate the effectiveness of the new a-Lith based approach demonstrated here for the development of metal oxide TFTs with improved operating characteristics.

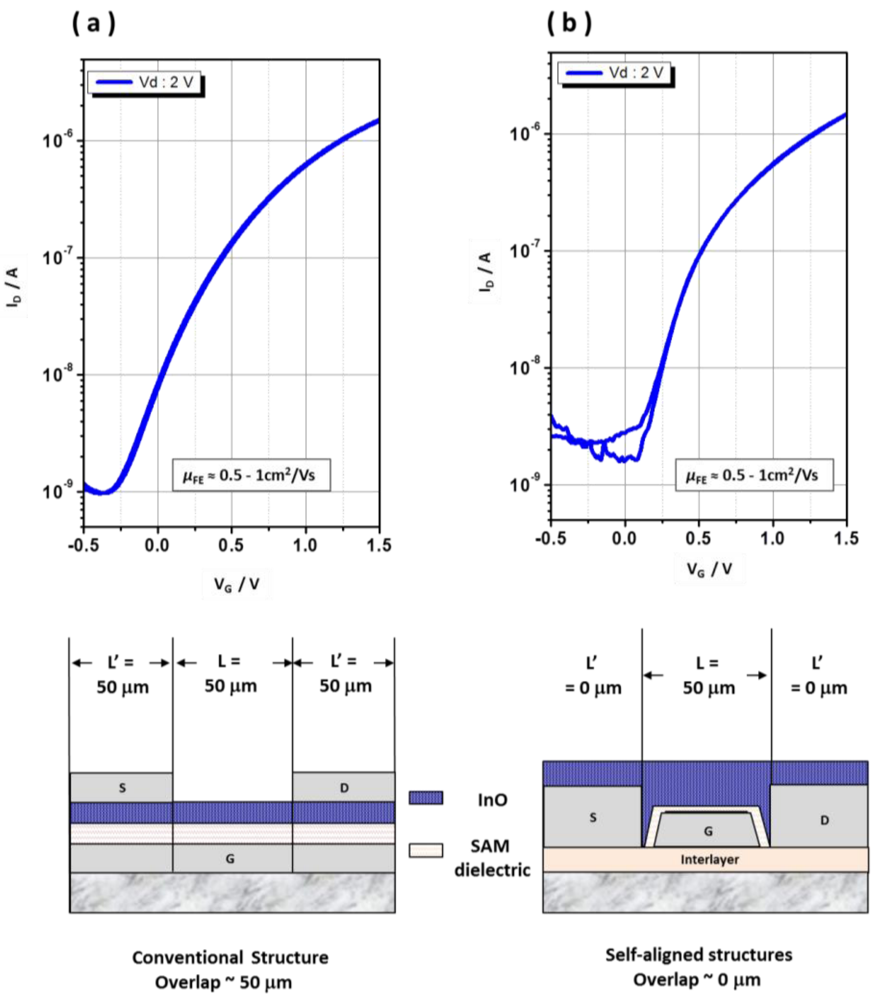


Fig.4.4.6 Saturated (V_D = 2.0 V) transfer characteristics of InO transistors with channel width W =1000 μm and channel length L = 50 μm. (a) A conventional structures with overlap length of 50 μm. (b) A self-aligned gate structure with the ovelap length of close to 0 μm.

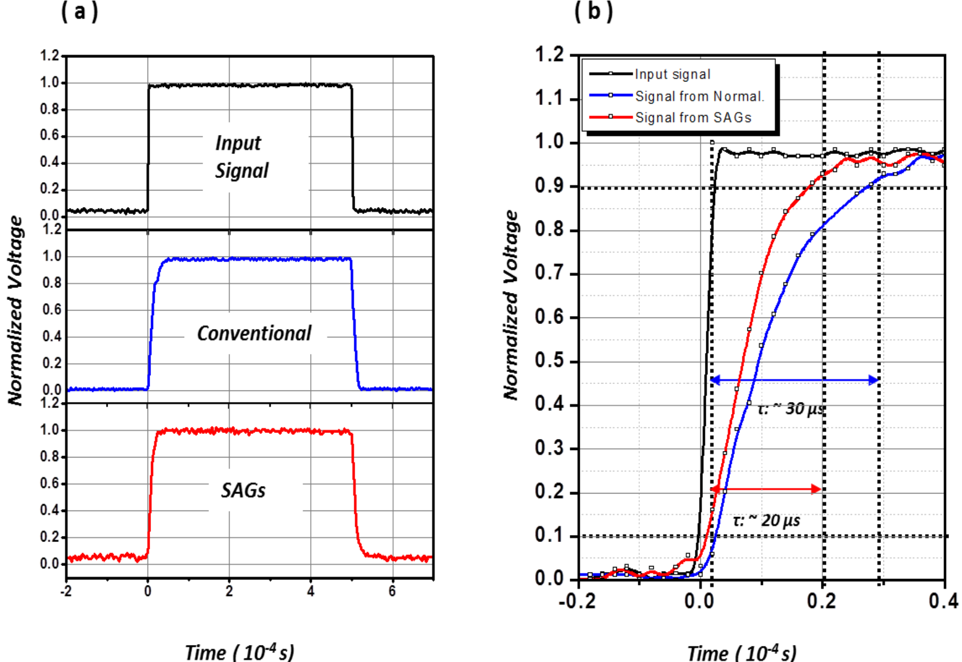


Fig 4.4.7 Dynamic response of transistors. (a) One cycle of the input signal (black), the output signal of the conventional structures with overlap length of 50 µm (blue) and the self-aligned gate structures with overlap length of 0 µm (red). (c) Determination of the rise time, required time for rising from 10 % to 90 % of the signal. The measured rise time of the SAG TFTs with the overlap length of 0 µm was about 20 µs (blue arrow), while that of a conventional TFT structure with a channel overlap length of 50 µm was 30 µs (red arrow).

The differences between the conventional and SAG TFT architectures become even more pronounced when the channel length of the device is reduced to 1 µm. This difference is nicely illustrated in Figure 4.4.5 where the operating frequency for the SAG TFT (b) approaches a maximum value close to 10 MHz, whilst the value for the non-aligned TFT (a) (conventional) remains only at ~14 KHz. From these calculations it can be concluded that both the SAG architecture combined with the downscaling of the channel length can yield TFTs with dramatically increased operating frequencies. Use of semiconducting materials with higher electron mobilities can help to further increase this value significantly. However, the latter is beyond the scope of this work and will be addressed in future studies.

4.5 Summary and conclusions

A new patterning technic for the development of self-aligned gate (SAG) TFTs has been developed and its effectiveness demonstrated. Initially, solution-processed indium oxide transistors were processed at 300 °C in air using the previously described formulation. The extracted values of the electron motility for these TFTs were in the range of 0.5-5 $cm^2/V.s$ and the devices exhibited high current on-off ratio of $>10^5$. In an effort to reduce the operating voltage of the TFTs, high capacitance hybrid SAM dielectric layer were employed and indium oxide TFTs with low operating voltage (1.5 V) were successfully demonstrated. Resulting devices exhibited electron mobility values of about 1 $cm^2/V.s$ with high current on-off ratio values of $>10^3$. Next, SAG indium oxide-based TFT were developed using a combination of the a-Lith method and the hybrid SAM dielectric. The proposed modified lift-off process allows facile development of SAG TFTs on arbitrary substrates since the entire development steps can be performed at low temperatures. Using the SAG architecture, indium oxide TFTs with improved switching speed were successfully demonstrated. In particular, SAG TFTs showed rise time of 20 μs, while for TFTs based on the conventional device structure (with overlap length of 50 μm) this value was >30 μs. The work described in this section represents an important development towards simple to implement, and hence inexpensive, patterning technique for SAG TFTs and should be applicable to any solution-processable semiconductor material.

CHAPTER 5

Organic ferroelectric tunnel junction memories

5.1 Introduction

The "*Internet of Things* (IOT)" concept has received considerable attention in recent years due to its huge technological potential for application in every form of future electronics.[4] Since one of the most important building blocks of the IOT is the embedded processing node, a low- voltage reprogrammable memory device is also required for data processing and recording the signals from the various input devices/elements. In the field of solid-state memory devices, there are many inorganic technologies including the widely used Si memories, phase-change memories (PRAM), magneto resistive memories (MRAM), ferroelectric memories (FeRAM)[117] and recently reported organic ferroelectric memory devices[123]. Among these candidates, organic ferroelectric memory devices offer numerous advantages, including reprogramability and processing versatility, which is important for low-cost manufacturing. However, organic ferroelectric memory devices hare characterised by a major drawback, namely the relatively high operating voltage attributed to its high coercive field (~50 MV/m). Although there have been numerous attempts to lower the operating voltage of organic ferroelectric materials by downscaling of key device dimensions (e.g. material thickness, device dimensions) through the use of sophisticated fabrication techniques such as nano imprint lithography (NIL)[118] and Langmuir–Blodgett (LB) methods,[119] these approaches are incompatible with large-area manufacturing while metal deposition on thin organic ferroelectric materials with thicknesses <50 nm has proven extremely challenging due to metal diffusion into the organic layer during deposition (Figure 5.1).

The primary aim of this work was to explore the potential of a-Lith for the development of organic ferroelectric memory devices and particularly, ferroelectric tunnel junctions. As described in an earlier section, formation of electrode nanogaps on large area substrates has now become possible via a-Lith. As such, nanogap electrodes combined with organic ferroelectric materials that can be deposited at the end should yields coplanar diodes without electrical shorts – the main problem conventional sandwich type devices suffer from. To achieve this, however, well-defined nanogaps with critical lateral dimensions down to a few nm, are required. Additionally, the organic ferroelectric material needs to penetrate into the nanogap and form well-ordered domains. To test this hypothesis, we developed and tested

a number of devices, the experimental results of which are discussed next, while we review ferroelectric tunnel junction memories and charge transport mechanisms in metal-insulator-metal junctions.

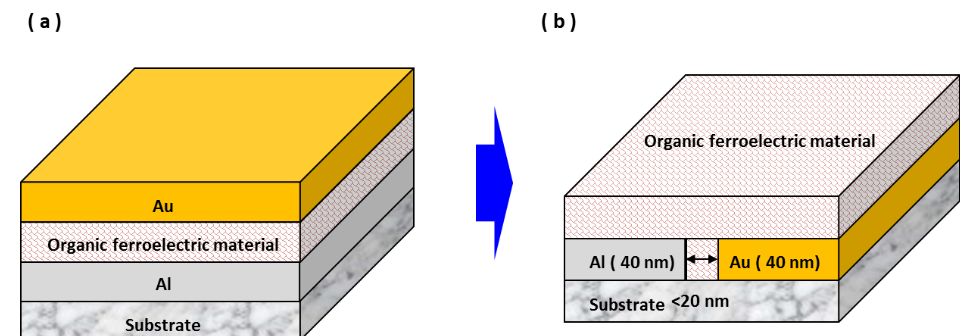


Fig 5.1 Strategies for a low-voltage organic memory device by a-Lith. (a) Conventional vertical structure. (b) In-plane nanogap structure.

5.2 Charge transport in Ferroelectric tunnel junction memories

In 1971, Esaki *el al.* proposed the concept of the ferroelectric tunnel junctions (FTJs)[132], but only recently the first experimental results on FTJs were reported [134]. This was due to the fundamental thickness limit of ferroelectricity and the practical difficulties in fabricating such devices[133]. In 2009, Garcia *el al.* demonstrated the giant tunnel electroesistance of the a few nano meter ferroelectric $BaTiO_3$ film. They investigated the resistance of the film according to the polarization direction and the contrast was up to ~75,000% [134]. Chanthbouala *el al.* also proved that this inorganic $BaTiO_3$ FTJs memory operated with power of 1×10^4 A/ cm^2, at least two orders of magnitude lower than the value required for MRAMs[133]. Contrary to these results, Maksymovych *el al.* showed that the polarization control of electron transport of the relatively thick, 30 nm ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$, PZT films and insisted that a Fowler-Norheim tunnelling conductance could be drastically reduced when the polarization vector was antiparallel to the applied electric field[135]. These dissimilar current-voltage characteristics of FTJs might be due to the difference between direct tunnelling and Fowler-Norheim tunnelling, which are strongly dependent on the thickness of the ferroelectric materials. Kusuma *el al.* reported organic ferroelectric tunnel junction devices based on vinylidene fluoride (VDF) oligomer[136]. They argued that the device showed memory characteristics when the ferroelectric materials were biased above 1 V, which was believed to be the coercive field. These early results demonstrated the feasibility in fabricating organic tunnel junction memories and their enormous technological potential.

Even though dielectric materials are insulating, electrical currents can still be measured in a capacitor. This current however is not attributed to direct conduction though the insulating layer, but due to induced currents from the changing of displacement field, and this is why it is often called a displacement current given by Equation 5.1 in the absence of magnetic field [120]:

$$\mathbf{J_D} = \frac{\partial \mathbf{D}}{\partial t} \qquad [\mathrm{A}/m^2] \tag{5.1}$$

Although the displacement current is important especially for high frequency devices, actual conduction of charges though the insulator was more relevant in this study for understanding the tunnel junction memory devices operated under DC bias.

The charge carrier transport mechanisms though an insulator can be classified into two main processes: (i) an electrode-limited conduction mechanism, and (ii) a bulk-limited conduction mechanism[120,137,138]. In the electrode-limited conduction mechanism, there are also several detailed models such as Schottky emission, Fowler-Nordheim tunnelling, direct tunnelling and thermionic-field emission. In the bulk-limited conduction mechanism, carrier transport phenomena is explained in more detail with Poole-Frenkel emission, hopping conduction, Ohmic conduction, space-charge-limited conduction, ionic conduction and grain-boundary-limited conduction models. Here we discuss the following models:

- Schottky emission
- Poole-Frenkel emission
- direct tunnelling, and
- Fowler–Nordheim tunnelling

In a metal-insulator-metal junction, the difference between the work function of the metal and the electron affinity of the insulator induces the potential barrier at metal-insulator interfaces, the so-called Schottky barrier. Carrier transport thorough the insulator is blocked by this potential barrier, however, when thermally activated enough to overcome the potential barrier, the charge carrier transport over the barrier increases. This kind of transport mechanism is called as Schottky emission or thermionic emission. The current equation of Schottky emission is given by:

$$J_{S.E} = \mathrm{A}^* T^2 \exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}}{kT}\right] \qquad \mathrm{A}^* = \frac{4\pi q k^2 m^*}{h^3} \tag{5.2}$$

where J is the current density, A^* is the effective Richardson constant, $m*$ is the effective electron mass in the dielectric layer, T is the absolute temperature, q is the electronic charge,

$q\phi_B$ is the Schottky barrier height, E is the electric field, k is the Boltzmann's constant, h is the Planck's constant, ε_0 is the permittivity in vacuum, and ε_r is the optical dielectric constant.

Conventional insulator materials such as SiNx, SiOx etc, are not perfect crystals and as such contain several defects. These defects form several additional energy states in the insulator, which tend to lower the potential barrier. Thus, even under the application of a relatively high electric field, significant amount of charge carriers are transported across the dielectric. This trap-assisted mechanism is called as Poole-Frenkel emission and the current density is expressed as:

$$J_{P.F} = q\mu N_c E\, exp\left[\frac{-\,q(\phi_T - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}}{kT}\right] \tag{5.3}$$

where μ is the drift mobility, N_C is the density of states in the conduction band and ϕ_T is the trap energy level.

Charge carriers may also be transported across the dielectric via quantum mechanical tunnelling provided the thickness of the insulator is small enough (<<10 nm). Interestingly, the latter process can occur even at low applied bias with the current density given as:

$$J_{D.T} \propto \mathrm{E}exp(-\frac{4\pi d}{h}\sqrt{2m^*\phi_B}) \tag{5.4}$$

where m^* is the effective mass of the tunnelling electron in the dielectric layer.

At high applied bias, band bending in the insulator occurs and the carrier can be transported though the triangular barrier. This process is known as Fowler-Norheim Tunnelling and the current density is expressed as:

$$J_{FN} = \frac{q^2\mathrm{E}^2}{8\pi h\phi_B} exp(-\frac{8\pi\sqrt{2m^*(q\phi_B)^3}}{3qh\mathrm{E}}) \tag{5.5}$$

where m^* is the effective mass of the tunnelling electron in the dielectric. In Figure 5.2, schematic band diagrams of these models are illustrated and simplified version of current equations are summarised in the table 5.1.

Conduction Mechanism	Characteristic Behavior	Temperature Dependence	Field Dependence
Direct Tunneling	$J \propto \mathrm{E}exp(-\frac{4\pi d}{h}\sqrt{2m^{*}\phi_B})$	none	$J \propto \mathrm{E}$
Fowler − Nordheim Tunneling	$J = \frac{q^2\mathrm{E}^2}{8\pi h\phi_B}exp(-\frac{8\pi\sqrt{2m^{*}(q\phi_B)^3}}{3qh\mathrm{E}})$	none	$\ln(J/E^2) \propto \mathrm{E}^{-1}$
Schottky Emission	$J = \frac{4\pi qm^{*}k^2T^2}{h^3}exp(-\frac{q\phi_B - \sqrt{q^3\mathrm{E}/4\pi\varepsilon}}{kT})$	$\ln(J/T^2) \propto T^{-1}$	$\ln(J) \propto \sqrt{\mathrm{E}}$
Poole − Frenkel Emission	$J = q\mu N_c\mathrm{E}exp(-\frac{q\phi_t - \sqrt{q\mathrm{E}/\pi\varepsilon}}{kT})$	$\ln(J/\mathrm{E}) \propto T^{-1}$	$J \propto \mathrm{E}$

Table 5.1 Summary of the charge-transport mechanisms though an insulator.

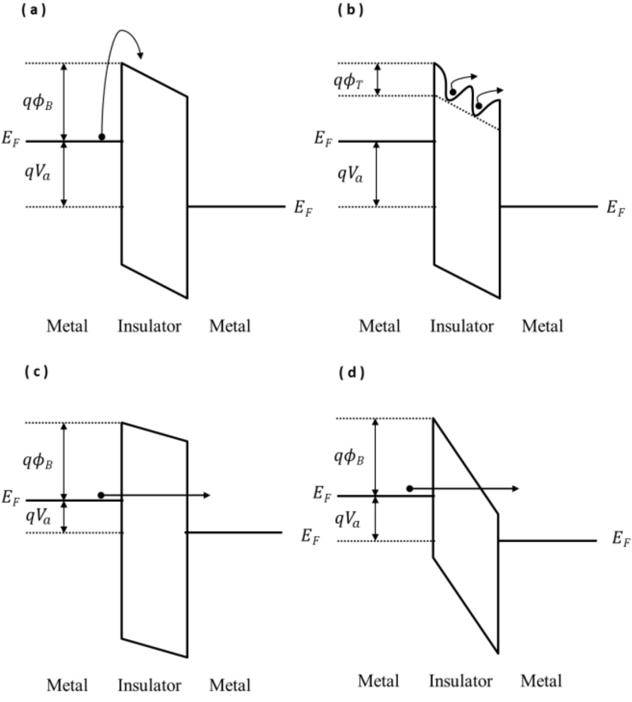


Fig 5.2 Schematic illustrations of the charge-transport mechanisms though an insulator. (a) Schottky emission. (b) Poole-Frenkel emission. (c) Direct Tunneling. (d) Fowler–Nordheim tunnelling.

5.3 Experimental Methods

The previously described a-Lith based patterning technic was employed for fabricating the electrode nanogaps and subsequently the organic ferroelectric tunnel junction. Figure 5.3

shows the various process steps employed. In brief, a 50 nm-thick Aluminum (1st electrode) was deposited by thermal evaporation and thermally oxidized to form the native alumina. Following, SAM treatment was performed by immersing the samples in a 5 mM octadecylphosphonic acid (ODPA) IPA or Ethanol solution for 12 hours. Samples were then rinsed and thermally annealed at 150 °C for 30 minutes in nitrogen ambient. After rinsing the samples with IPA and dried with nitrogen gas, a 40 nm-thick Au (2nd electrode) layer was deposited onto a pre-deposited 10 nm-thick Al interlayer acting as the adhesion layer for Au on glass. Electrode overlaps between the 1st and 2nd electrodes were then removed by a-Lith, forming the inter-electrode nanogap as shown in Figure 5.3(IV). P(VDF-TrFE) was then deposited via additive inkjet printing from a 1 wt % cyclopentanone solution using a Dimatix material printer (DMP-2831) onto the in-plane nanogap electrodes (Figure 5.3(V)). The samples were then annealed at 135°C for 1 hour in order to obtain the ferroelectric β-phase, the presence of which was verified via polarized optical microscopy measurements. Figure 5.4 shows optical images of the ferroelectric material during printing and a lower and a higher magnification image of the device and the nanogap respectively. As-prepared devices were electrically characterized using an Agilent 4155C semiconductor parameter analyzer. Capacitance-voltage measurements were performed with an Agilent LCR analyzer (HP4284A) using a four-probe method.

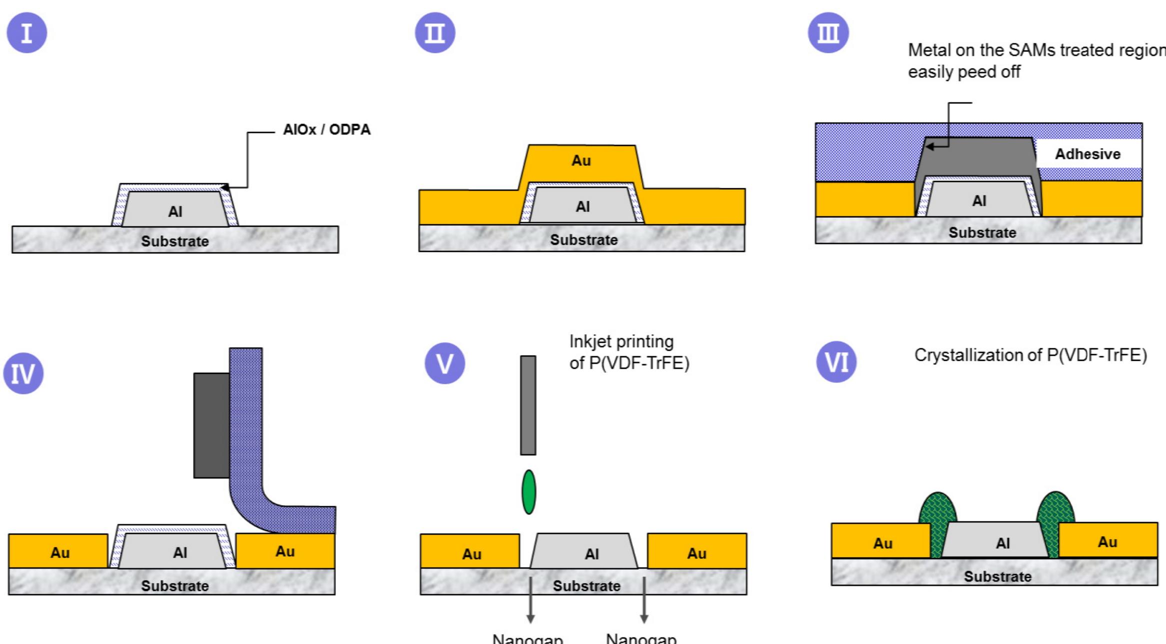


Fig.5.3. Schematic of the process steps used to manufacture an organic ferroelectric tunnel juntion memory by a-Lith. Before inkjetting the P(VDF-TrFE) on to the nanogap, the samples were treated with UV-ozone for 10 minutes for removal of SAM layer.

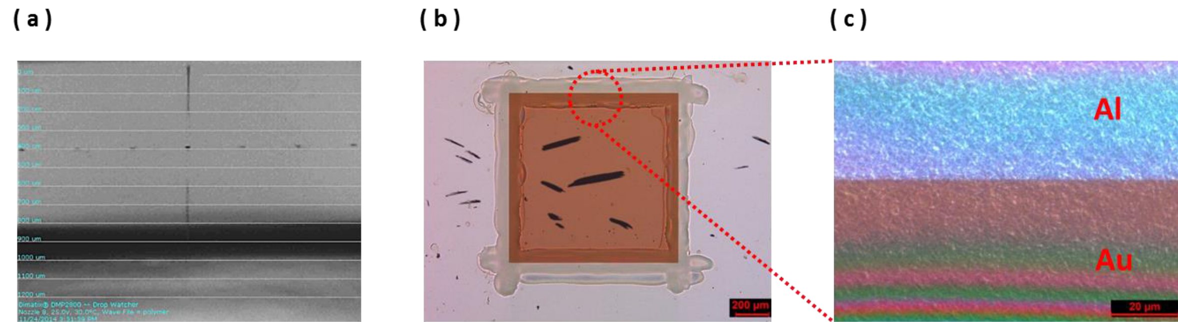


Fig.5.4. Printed organic ferroelectric devices. (a) Printing image. (b) Low magnification non-polarized optical image of the whole device consisting of a square middle Al electrode surrounded by a global Au electrode. Scratches in the electrodes were from the electrical measurement. (c) Higher magnification polarized optical image of the nanogap region. Organic ferroelectric of P(VDF-TrFE) was printed in the nanogap region. The polarized image was yellowish in Au region. Birefringence of the film in polarized mode was observed, which indicate the formation of crystal structure of P(VDF-TrFE) film.

5.4 Results and Discussion

First, the physical integrity of all as-fabricated coplanar nano-gap devices was inspected. Figure 5.5(a) shows an optical image where the 2nd Au metal electrode surrounds the central squared shaped SAM-treated Al electrode and separated by the nanogap. I-V measurements taken from this empty nanogap devices [Figure 5.5(b)] verify that the gap between the two electrodes is indeed empty and highly insulating with the measured current close to the measurement system's detection limit of $\sim 10^{-12}$ A. The circumference of the nanogap for this particular device was 4 mm. Analysis of the nanogap [Figure 5.6] by AFM reveals that the average nanogap present between Al and Au electrodes was indeed very small and consistently below 20 nm. Importantly, we find evidence that show that the nanogap dimensions depend heavily on the crystallinity of the metals and particular the grain size of the crystalline domains [see AFM image in Figure 5.6]. These values for the nanogap are consistent with the previously reported values and observations. [59]

Once the physical integrity, low-dimensionality and insulating nature of the nanogap electrodes has been verified, fabrication of the complete coplanar ferroelectric capacitors was completed to form devices similar to the ones shown in Figure 5.7(a). Following, devices were electrically characterised using the equipment described above. Assuming that as-prepared coplanar structures do indeed behave as ferroelectric capacitors, a nanogap of <20

nm is expected to yield devices that operate at voltages in the range of 1-2 V if one assumes an *Ec* of 50-100 MV/m. Furthermore, additional decrease of the operating voltage to sub-1 V could be possible by refining the quality and orientation of ferroelectric material in the nanogap. For example, Hu *et al*. reported previously that the value of *Ec* can indeed be reduced to 10 MV/m by using nano-embossed imprint methods for the ferroelectric material leading to low-voltage operation devices (<2 V). Therefore, combination of the co-planar nanogap architecture proposed here and advanced processing methods could indeed prove highly effective in device optimization. For the present coplanar nanogap capacitors, displacement currents are expected to dominate conduction at the coercive field [Figure 5.7 (a)]. Another possibility would be the appearance of low voltage memristor-like behaviour [Figure 5.7(b)]. Because of the sub-20 nm dimension of the critical nanogap, charge carrier tunnelling could also occur. Interestingly, in the latter case charge carrier tunnelling is expected to depend on the polarization direction of the ferroelectric film domains also resulting in I-V behaviour closely resembling that depicted in Figure 5.7(b). Furthermore, the current density in such ferroelectric tunnel junction would be significantly higher than that of the current density due to displacement current.

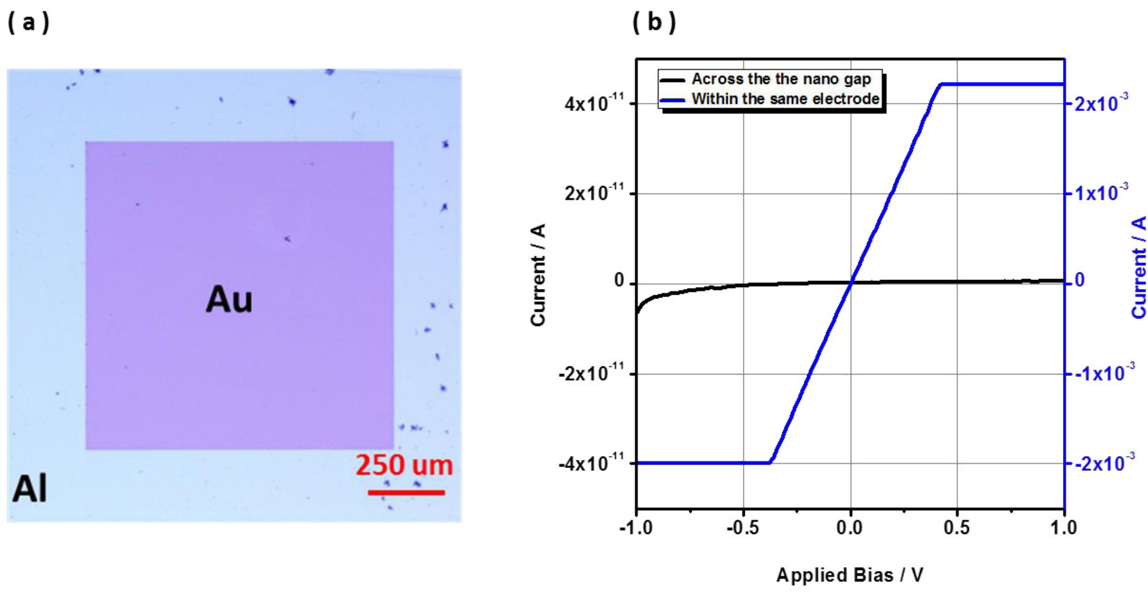


Fig.5.5. (a) Optical image of the as-fabricated Al-Au nanogap. (b) I-V characteristics measured across the nanogap (black line) and in contact with the same electrode (i.e. both probes touching the same electrode).

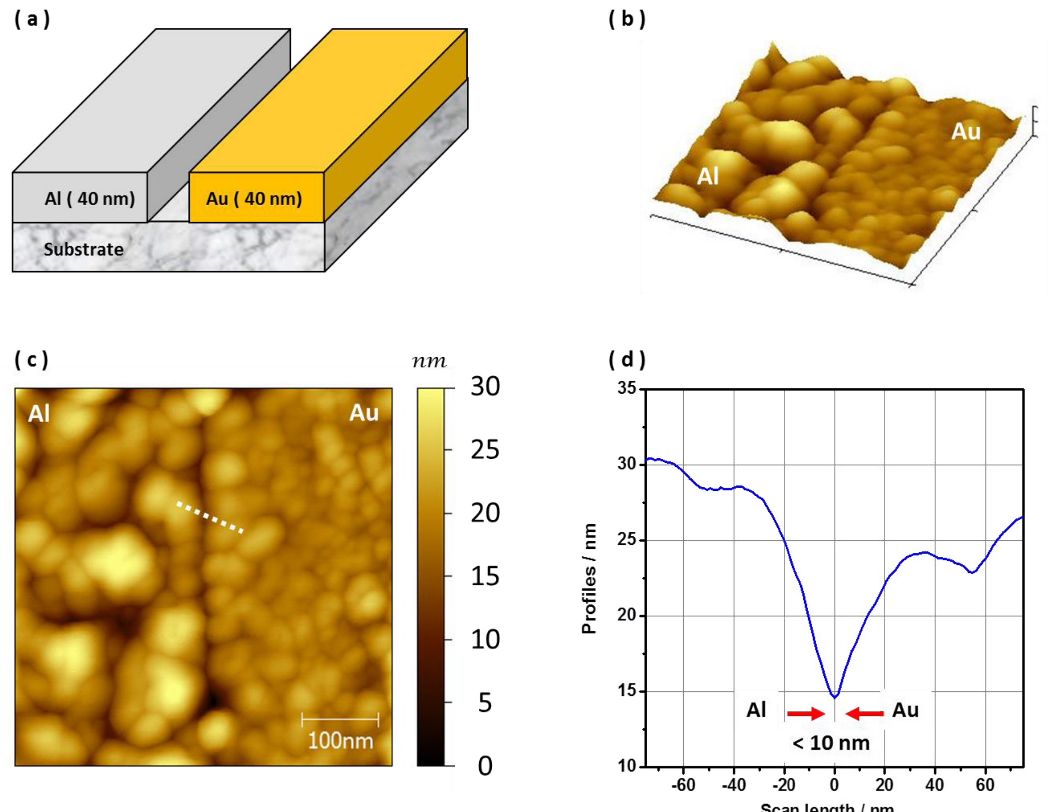


Fig.5.6. (a) Schematic illustration of the in-plane nanogap structure. (b) 3-dimensional atomic force microscopy image of the in-plane nanogap structure. (c) 2-dimensional atomic force microscopy image of the in-plane nanogap structure. (d) The profiles of the gap and the value was sub 20 nm.

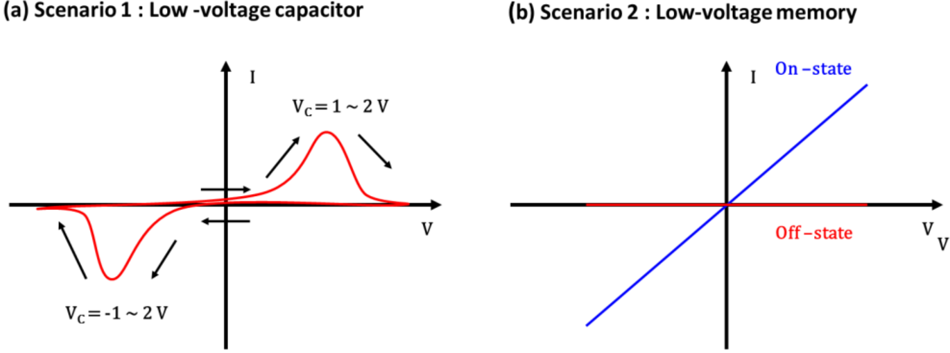


Fig.5.7. Device estimations. (a) In-plane nano capacitors, Due to the sub 20 nm structure, the device could be operated in a low-voltage capacitors. Displacement current would be dominant, hence at the coercive voltage of 1 ~ 2 V, the current density would be maximized. (b) Tunnel-junction memory mode. If the charge carrier can be tunnelled into the nanogap of 20 nm, the device would show the high density of current and duality. There would be significant difference in the density of current between the on and off state.

To test these hypotheses we have performed current-voltage characterisation in as-prepared devices similar to those shown in Figure 5.7. A representative I-V characteristic is shown in Figure 5.8(a). Clearly the device exhibits memory-like characteristics without signs of electrical shorting. In the low bias range the device shows an insulating state with current levels of < 10^{-9} A. However, at approximately 1.2 V the current increases significantly reaching a magnitude of >10^{-6}A. This high conductivity state is maintained until a lower bias is applied where a similar change but from high to low conductivity state is observed in the negative bias regime. In the case of the previous reported organic memory devices, however, the high conductivity state is maintained until the device was biased at the significant level of opposite sign of bias because of the filamentary conduction in the organic layer.[141,142] In other words, the device in this study exhibits two conductivity states at specific biases, which depend on its bias history and hence functions as a memory.

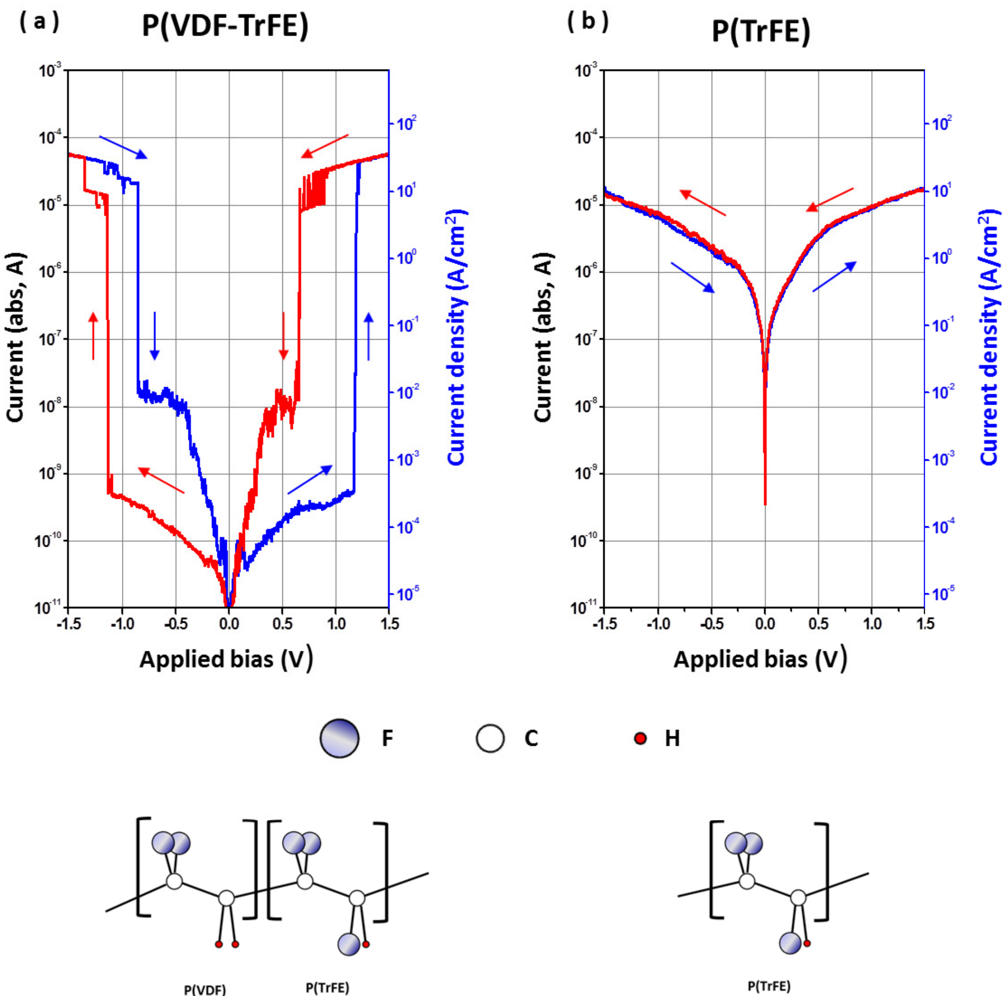


Fig.5.8. Current-voltage characteristics of: (a) the ferroelectric P(VDF-TrFE) junction and (b) the non-ferroelectric (i.e. control) P(TrFE) device.

The on-off ratio between the high and low conductivity state was measured to be typically over 10^3 with operation voltages ranging from 0.7 V to 1.2 V. To verify that the observed switching behaviour is indeed attributed to the ferroelectric nature of the polymer employed, we have performed control experiments where a similar but non-ferroelectric dielectric, namely P(TrFE), was deposited into the nanogap instead of the P(VDF-TrFE). As can clearly be seen in Figure 5.8 (b), in the case of P(TrFE) nanogap devices the measured current density is also high, but no hysteresis loop could be observed. The high current is most likely attributed to charge carrier tunnelling across the nanogap via defect states present within the polymer and/or due to the presence of chemical impurities that act as transport states. To verify the validity of these preliminary results similar measurements were performed on several non-ferroelectric as well as ferroelectric polymer-containing devices (Figure 5.9). These initial experimental results suggested that the memory characteristics observed were indeed related to the organic ferroelectric material [P(VDF-TrFE)] being present in the nano-gap channel.

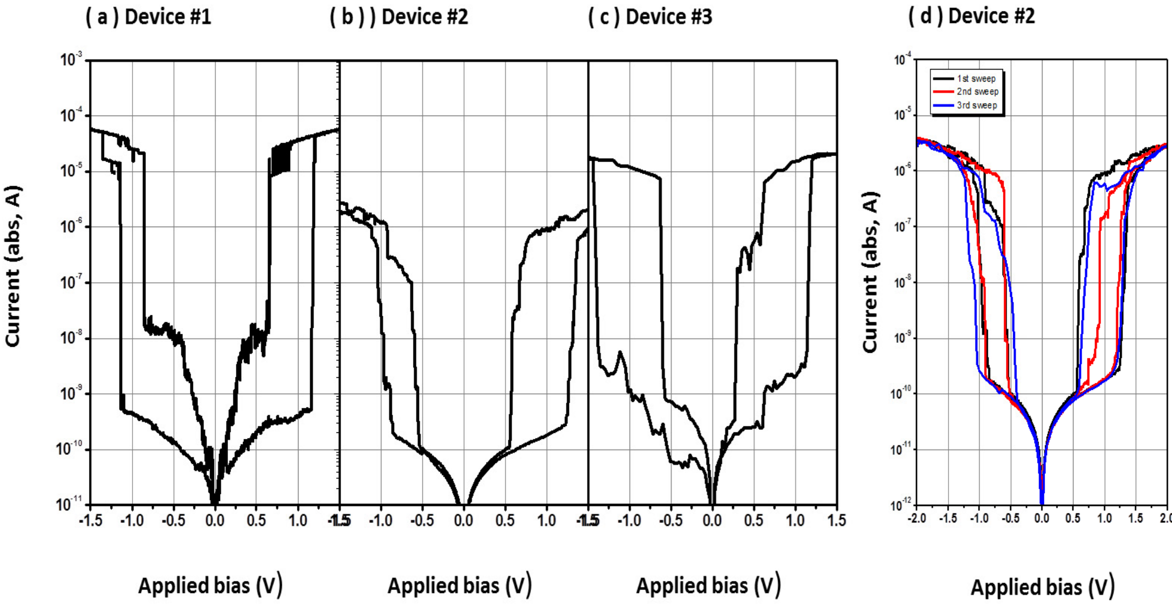


Fig.5.9 (a,b,c) J-V characteristics of several different P(VDF-TrFE) tunnel junctions. (d) Multiple J-V sweeps for device #2 demonstrating good operating stability.

As-fabricated P(VDF-TrFE) nanogap tunnel junctions were further investigated via impedance analyses using a parallel connected capacitance and resistance model. For comparison, conventional sandwich devices based on SiNx were also fabricated. For devices

employing a 200 nm-thick SiNx layer the measured capacitance and resistance were found to be independent of the applied bias [Figure 5.10 (a)] i.e. as expected for a non-ferroelectric material. The behaviour however was rather different for the nanogap-based devices, were both capacitance and resistance depend on the applied bias. In the case of P(TrFE) nanogap junctions, the parallel resistance was found to significantly decrease with increasing applied bias. In particular, the parallel capacitance remained constant in the low bias regime (<0.5 V) followed by a slight decrease and a subsequent increase at higher electrical potentials.

In the case of P(VDF-TrFE)-based nanogap devices, strong hysteric effects are observed. The latter resemble the current voltage characteristics shown in Figure 5.9. For all devices the resistance is found to be high and on the order of 10^9 Ω, but it decreases significantly at around 1.2 V reaching a stable conductive state with a resistance value of ~10^6 Ω. The latter state remained constant at higher bias fields without significant changes. Similarly, the capacitance value of the ferroelectric junction remained relatively constant but changed abruptly at a bias of 1.2 V. These changes were different from conventional butterfly capacitance hysteresis seen in ferroelectric polymer-based devices. This difference is most likely attributed to charge tunnelling in the ferroelectric nanojunction and it will be discussed next.

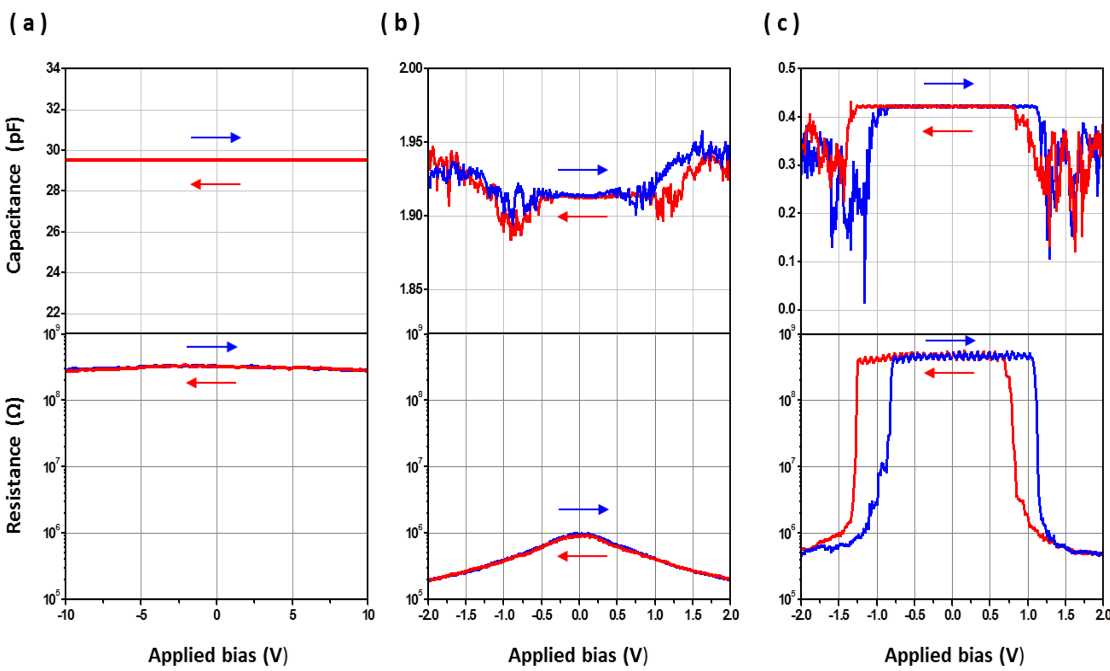


Fig.5.10. Impedance analysis using parallel connected capacitance and resistance model for devices based on (a) SiNx, (b) P(TrFE), and (c) P(VDF-TrFE).

To investigate the nature of current transport mechanism in the nanogap metal-ferroelectric-metal (MFM), the current-voltage characteristics of as-prepared devices were analysed within the framework of the previously discussed charge transport models. In the low bias regime (< 1V) the current-voltage relationship appears to be described by the Schottky or trap-assisted Poole-Frenkel emission models (see Table 5.1) as it exhibits a distinct linear dependence with a positive slope [Figure 5.11 (a-b)]. However, noticeable discontinuities in the I-V characteristics, which cannot be explained by these two models, exist.

In an effort to understand this behaviour we invoked the Fowler–Nordheim tunnelling model discussed earlier. The current-voltage relationship in this model is expressed as:

$$J_{FN} = \frac{q^2 \mathrm{E}^2}{8\pi h \phi_B} exp(-\frac{8\pi\sqrt{2m^*(q\phi_B)^3}}{3qh\mathrm{E}}) \tag{5.6}$$

$$\ln\left(\frac{J_{FN}}{E^2}\right) = \ln\left(\frac{q2}{8\pi h\phi_B}\right) - \frac{4}{3}\frac{\sqrt{2m_T}}{q\hbar}\frac{(q\phi_B)^{3/2}}{E} \tag{5.7}$$

If the current measured in our devices is indeed due to Fowler-Norheim tunnelling, the relationship between $\ln(J_{FN}/E^2)$ and $1/E$ should be linear with a negative slope. As already discussed, however, in the low bias regime (±1.2 V in Figure 5.11(a)), the current dependence on voltage cannot be attributed to Fowler-Norheim tunnelling since the linear dependence has negative slope [see Figure 5.11 (c)]. By assuming the metal nanogap is <20 nm and the coercive field of P(VDF-TrFE) is in the range of 50-75 MV/m, the applied bias of ~ 1.2 V may well be argued that is able to polarize the P(VDF-TrFE) within the nanogap. To investigate this possibility we further analysed the current-voltage characteristics and compared the I-V relationship under different biases.

The I-V characteristics, and hence the derived slope, ultimately depend on the magnitude of the potential barrier present between the injecting metal electrode and the energy levels of the ferroelectric insulator i.e. the P(VDF-TrFE). Since the electron affinity of the P(VDF-TrFE) is ~ 4 eV [140] and the work function of Au and Al are ~ 5.1 eV and ~ 4.2 eV, respectively, the potential barrier for electron injection from Au to the ferroelectric (Fe) layer should be greater than that for the Al electrode. As shown in Figure 5.12(d, f), the characteristic slope measured for Au-based nanogap devices is higher than that seen in Al-based devices. The latter is attributed to the higher potential barrier present in accordance to

the basic energy band picture discussed. On the basis of these results we conclude that the massive and abrupt current density change observed is most likely attributed to Fowler-Norheim tunnelling.

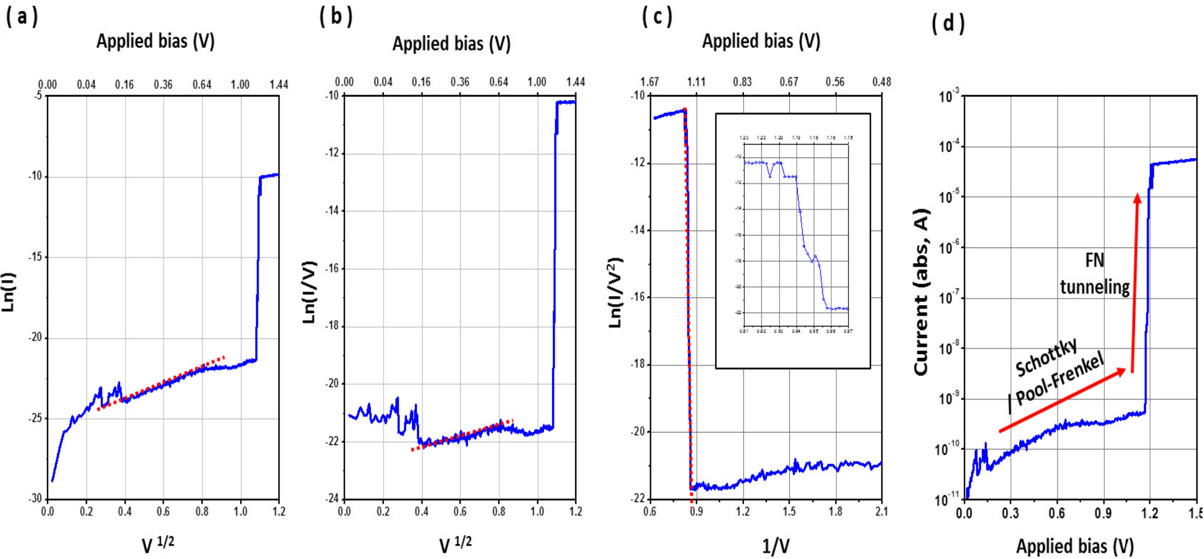


Fig. 5.11. Current-voltage analysis based on: (a) Schottky model, (b) Poole-Frenkel Model, (c) Fowler–Nordheim tunnelling model. Inset: negative slope region above the turning voltage of 1.1 V, well-matched with the Fowler–Nordheim tunnelling model. (d) Charge transport mechanisms of the MFM junctions based on analysis of the I-V characteristic of the device.

Finally, the memory characteristics of the nanogap organic ferroelectric tunnel junctions were analysed in terms of the band diagram shown in Figure 5.12. At the zero bias, the system of MFM junction is assumed to be in equilibrium and no current flows across the junction. When a low bias is applied across the device, current transport is expected to be limited by the potential barrier present between the injecting metal electrode and the Fe layer (b). However, when the bias increases above the coercive voltage, the ferroelectric polymer domains are expected to align to the direction of applied electric field. This alignment induces a local enhanced potential gradient manifested in a Fowler–Nordheim triangular form barrier. This enhanced potential gradient results to significant charge carrier transport via the Fowler–Nordheim tunnelling process (c). In the reverse bias regime, since the polarization vector becomes antiparallel to the applied electric field, the carrier transport is further suppressed (e). When the reverse bias equals or exceeds the coercive field, the direction of polarization in the ferroelectric material changes and aligns with the applied field direction. Hence, the carrier transport starts increasing again due to Fowler–Nordheim tunnelling (g). According to this

band diagram and expected device behaviour, the charge carrier transport across the ferroelectric nanojunction at a fixed voltage could be controlled by programming the direction of polarization as suggested by Esaki *et al.*[132]. This expected behaviour is in excellent qualitative agreement with the experimental measured I-V characteristics shown in Figure 5.13. If correct, these devices represent the first ever example of co-planar ferroelectric tunnel junctions. However, further work is required to prove or refute the operating principles of these devices.

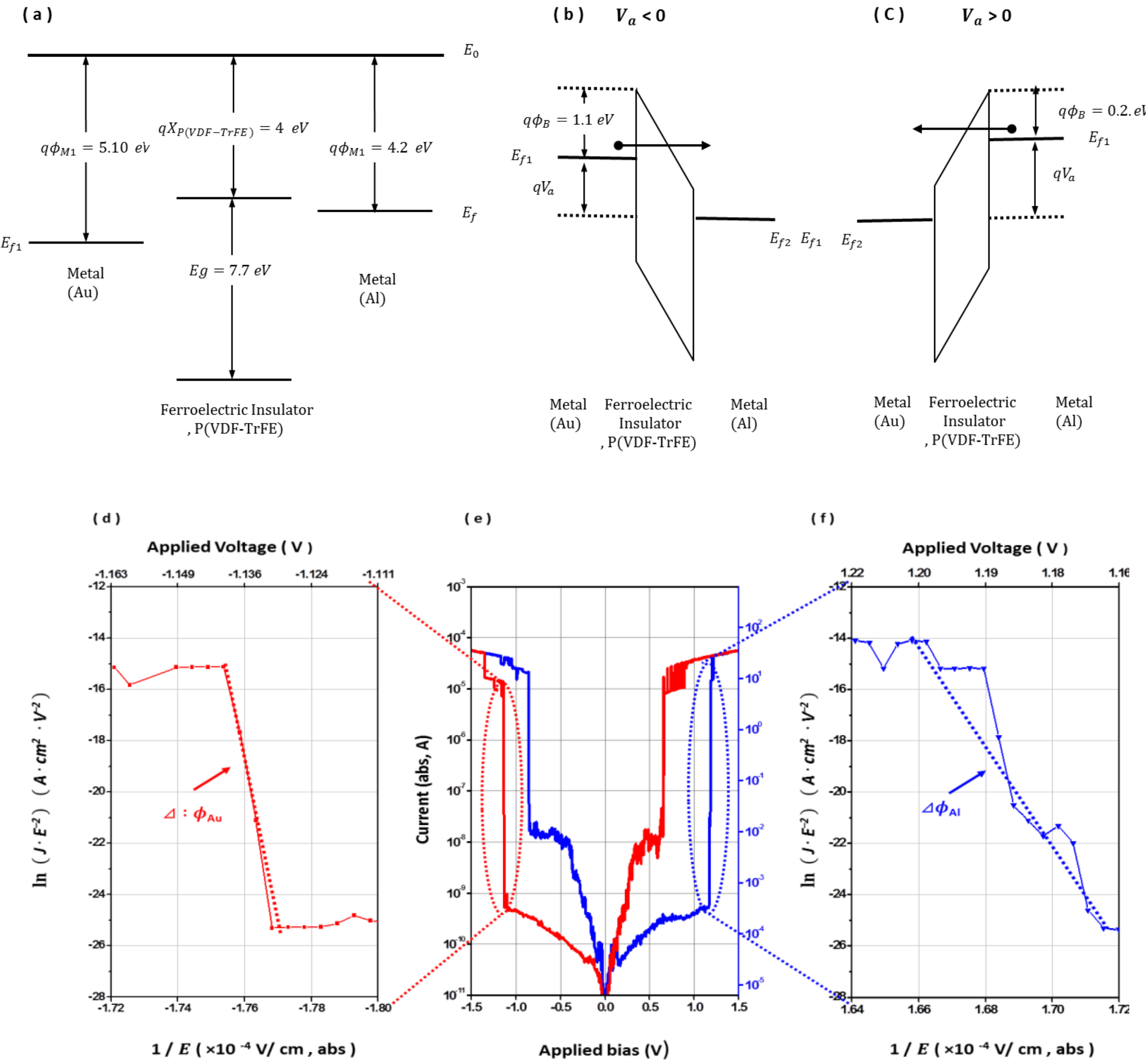


Fig.5.12. (a) Energy band diagrams of the metal-ferroelectric-metal structure/materials before contact. (b, c) Estimated potential barriers for electron injection from Au and from Al to the ferroelectric material of 1.1 eV and 0.2 eV, respectively. (d, f) The characteristic slope measured using Fowler–Nordheim plot analysis of the MFM device under negative and positive bias. The slope of Au/Fe is higher than that of Al/Fe, which indicates that the

analysis is in accordance to the assumed energy band picture. (e) Current-voltage characteristics of the ferroelectric P(VDF-TrFE) and (f) the corresponding Fowler–Nordheim plot.

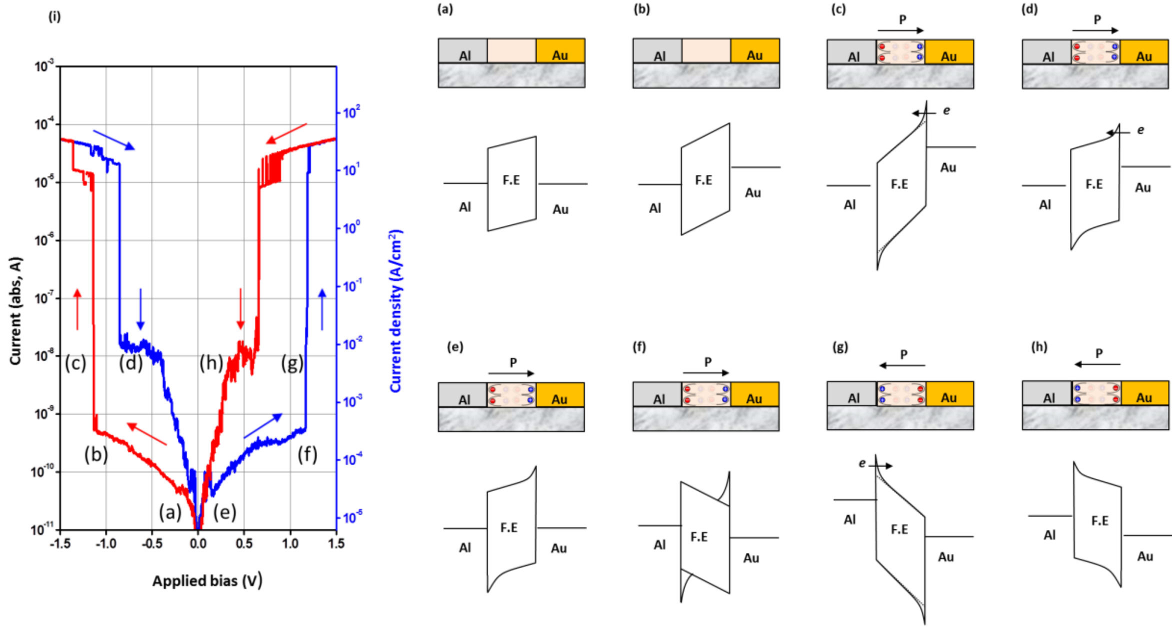


Fig.5.13. Operation mechanism of organic ferroelectric tunnelling memory device at various bias regions. (a) At equilibrium states. (b) Below the coercive voltage, current transport is expected to be limited by the potential barrier between the Au and Fe. (c) Above the coercive voltage, significant charge carrier density is transported via the Fowler–Nordheim tunnelling. (d-e) Insufficient low bias region for Fowler–Nordheim tunnelling. (f) The bias region for the antiparallel polarization vector to the applied electric field. (g) The bias region for realignment of the polarization vector to the applied electric field. Significant charge carrier density is re-transported across the junction. (h) Insufficient low bias region for Fowler–Nordheim tunnelling.

5.4 Summary and conclusions

Large aspect-ratio Au/P(VDF-TrFE)/Al nanogap based devices were successfully fabricated via a-Lith and electrically characterised. The nanogap length of the devices investigated was typically below 20 nm with a constant width of 4 mm. As-prepared P(VDF-TrFE)-based cells exhibited unexpectedly high current transport characteristics with significant hysteresis observed between forward and reverse voltage sweeps. The latter resulted in a memory-like behaviour with a high on-off ratio (>10^3) measured between the programmed on and off

states. Importantly, due to the nanoscale dimensions of the co-planar channel architecture employed, the devices operate at low-voltages that are typically below 2 V. Detailed examination of the current-voltage characteristics of these Au/P(VDF-TrFE)/Al nanogap devices revealed further interesting characteristics. Specifically, in the low bias regime, the devices were highly insulating with very small currents flowing between the two metal electrodes. However, as the applied bias increased, significant current starts to flow reaching a sustainable conducting state. The electric field at which this transition occurred was assumed to be equal to the coercive field of the device. These measurements suggest that the charge carrier transport appears to be controlled by the direction of polarization of the P(VDF-TrFE) material as Esaki *et al* predicted for a ferroelectric tunnel junction[132]. Most importantly, the polarization direction of the Fe material can be programmed at will hence allowing the device to be used as a memory cell. When the polarization direction of P(VDF-TrFE) was aligned to the direction of the electric field, a triangular potential gradient was formed in the injecting junction and the current transport was described by the Fowler–Nordheim tunnelling process. However, when the polarization direction was anti-parallel to the direction of the bias, the pre-induced, programmed potential gradient was found to suppress charge transport. This was confirmed through the use control devices based on the non-ferroelectric polymer P(TrFE), where the hysteresis effects were completely absent.

On the basis of these early results we believe that the nanogap metal-Fe-metal device architecture developed here may provide a unique platform for the realisation of ferroelectric tunnel junctions for numerous applications. If correct, this development alone may impact the emerging field of large area electronics and in general the “Internet of Things”

CHAPTER 6

Summary and Concussions

The Internet of Things (IOT) has emerged as a massive force of change for our society and our daily life by connecting "Things" with self-configurable electronic devices thought the "Internet". A typical self-configurable connected device consists of a sensing node, an embedded processing node and a communicating node. Because the relative complexity and widespread adoption (high volume) of the IoT, a key enabling feature of any candidate device technology has been the energy-efficient and low-cost manufacturing on inexpensive substrate materials such as temperature sensitive plastics. In order to fulfil this goal, device fabrication should be simple, low-cost and compatible with large-area manufacturing. The work described in this thesis has attempted to address some of these challenges through the development of alternative manufacturing processes and device concepts using simple and scalable approaches. Next we summarize some of the most important findings discussed in the thesis.

A new processing technic for the manufacturing of large-area electronics called Interlayer Lithography (IL) was firstly successfully explored as an alternative patterning method. By using a previously deposited electrode as a mask, back-exposure of a suitable photoresist enabled patterning of a second electrode leading to the formation of self-aligned gate (SAG) electrode structures. However, the significant thickness variation between the first and the second metal electrodes proved unavoidable due to the use of a micrometres-thick photoresist layers. Therefore an alternative method called adhesion-lithography (a-Lith) was explored for the development of SAG structures. The a-Lith method relies on the use of carefully engineered self-assembled monolayer (SAM) molecules that can be functionalised onto pre-deposited metal electrodes with suitable surface chemistry. By carefully controlling the surface energy of metal electrodes through the incorporation of SAMs with suitable end-groups (hydrophilic or hydrophobic), we showed that the adhesion forces between the first and a second metal electrodes deposited sequentially can be accurately tuned. For instance, the combination of hydrophobic octadecylphosphonic acid (ODPA) SAM molecules functionalised on the bottom aluminium electrodes enabled lift-off of the second gold electrode from all overlapping regions with the first electrode though a mechanical peel-off

step using an adhesive tape or glue. The latter step enabled the development of co-planar Al/Au and Al/Au/Al structures with high yield. An interesting feature of these structures is the narrow distance separating the two metallic electrodes. The latter was found to be consistently <20 nm, making a-Lith particularly attractive for realising high aspect ratio nanogaps between dissimilar electrodes for a number of opto/electronic applications.

Using the a-Lith process, SAG transistors based on solution-processed indium oxide were fabricated and thoroughly characterised. A stable semiconducting layer of InOx was realised via thermal annealing of the solution-deposited precursor at 300 °C while a high-k hybrid dielectric layer comprised of native Al_2O_3 and ODPA as the SAM, were successfully implemented for the development of low operating voltage devices. The extracted values of the transistor electron motility were in the range of 0.5-1cm^2/V.s and the devices were able to operate at <1.5 V due to the high geometrical capacitance of the hybrid gate dielectric (500-600 nF/cm^2). The SAG transistor structure developed via a-Lith enabled realization of devices without S-D/G overlaps. Analysis of the dynamic response analysis of conventional and SAG transistors revealed that SAG devices exhibited ×10 times higher switching speeds than conventional transistor architectures. This key finding demonstrated the tremendous potential of the a-Lith technology for the manufacturing of SAG metal oxide transistors.

Next, a-Lith was employed for the development of metal nanogap junctions and their use as ferroelectric tunnel junctions in memory devices. Although the nanogap between the two electrodes should ideally be defined by the thickness of the self-assembled monolayer (2-3 nm), resulting gaps were ~20 nm. Using this unique in-plane nanogap structure combined with a polymeric ferroelectric material, namely P(VDF-TrFE), organic ferroelectric tunnel junctions were demonstrated. Best performing devices exhibited low-voltage (< 2 V) memory characteristics with a high current on-off ratio of $>10^3$. Under low bias regime, devices operated showed highly insulating characteristics. However, upon application of higher electric fields, a sustainable conducting state was quickly reached. This asymmetric current injection behavior was attributed to the direction of polarization of the ferroelectric material [i.e. P(VDF-TrFE)] as originally predicted by Esaki *et al*[132]. Specifically, when the polarization direction of the ferroelectric polymer was aligned to the direction of the electric field, the carrier transport was enhanced due to Fowler–Nordheim tunnelling. However, when polarization was anti-paralleled, the pre-induced potential gradient blocked carrier

injection/charge transport across the device. These processes were confirmed by several carefully executed control experiments and appropriate data analysis. This unconventional ferroelectric tunnelling device concept offers many advantages over conventional sandwich-type devices for applications as non-volatile memory devices due to fabrication simplicity and the possibility of integration using simpler cell layout. Most importantly, the co-planar nanogap ferroelectric memory diodes developed here could prove suitable not only for application in large-area electronics but also in high-end memories were similar device concepts have been extremely difficult to implement due to the complexity of standard manufacturing techniques and inorganic materials control.

Although this study focused on the development of a transistor and an organic memory device, the processing methodologies developed could well be adopted for the development of numerous other nano-scale devices such as light-emitting diodes, photo-detectors, biological sensors, to name but a few. Such development could bring the IoT a step closer while enabling a huge range of functionalities that are difficult to explore using conventional device architectures and manufacturing paradigms.

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