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Characterization of the CBC2 readout ASIC for the CMS strip-tracker high-luminosity upgrade

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ABSTRACT: The CMS Binary Chip 2 (CBC2) is a full-scale prototype ASIC developed for the front-end readout of the high-luminosity upgrade of the CMS silicon strip tracker. The 254-channel, 130 nm CMOS ASIC is designed for the binary readout of double-layer modules, and features cluster-width discrimination and coincidence logic for detecting high-P_T track candidates. The chip was delivered in January 2013 and has since been bump-bonded to a dual-chip hybrid and extensively tested. The CBC2 is fully functional and working to specification: we present the result of electrical characterization of the chip, including gain, noise, threshold scan and power consumption, together with the performance of the stub finding logic. Finally we will outline the plan for future developments towards the production version.

KEYWORDS: VLSI circuits; Trigger concepts and systems (hardware and software); Front-end electronics for detector readout

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1 Introduction

The high-luminosity upgrade of the LHC will pose unprecedented challenges which require innovative future detectors. The upgrade of CMS will see, among other major improvements, the complete replacement of the silicon tracker during the so-called phase-II upgrade around 2022.

The current baseline design for the phase-II upgrade of the CMS tracker is the barrel+endcap configuration shown in figure 1. Besides providing improved overall tracking performance with lower mass, one of the main new features of the tracker will be the ability to contribute to the L1 trigger, in order to maintain its rate to about 100 kHz despite the increase in occupancy and pile-up of the high-luminosity scenario. Other measures being considered to improve the performance of the trigger and which have a direct effect on the design of the tracker are a possible increase of the readout latency up to 20 μs and an increased L1 trigger rate up to 1 MHz.

The idea behind the track-trigger concept is to be able to discriminate high transverse-momentum particles from the low-momentum background by looking at the correlation between two closely spaced microstrip sensors [1]. The microstrips are aligned, separated by a few millimeters and read out by the same front-end ASIC. As shown in figure 2, for every cluster in the inner sensor, we look for a correlated cluster in a coincidence window in the outer sensor. A valid correlation is interpreted as a high-P_T track candidate (called *stub*) and is output to contribute to the L1 trigger. The width of the coincidence window is programmable and provides a way to tune

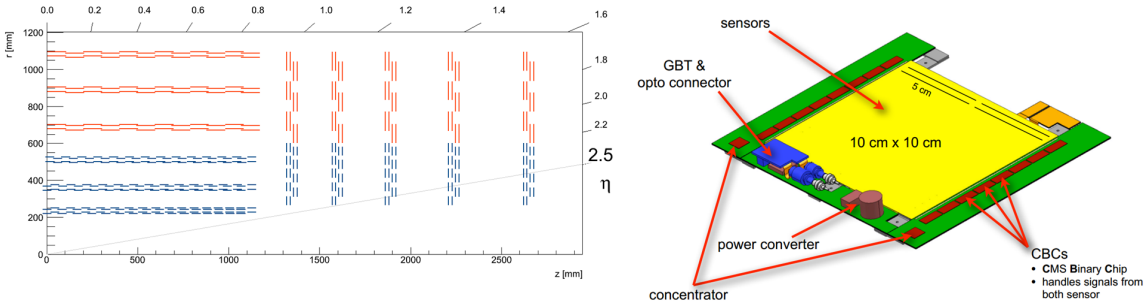

Figure 1. Left: quarter-view of the current baseline for the CMS microstrip tracker (red = 2S-module; blue = PS-modules). Right: Strip-Strip (2S) module for the outer tracker.

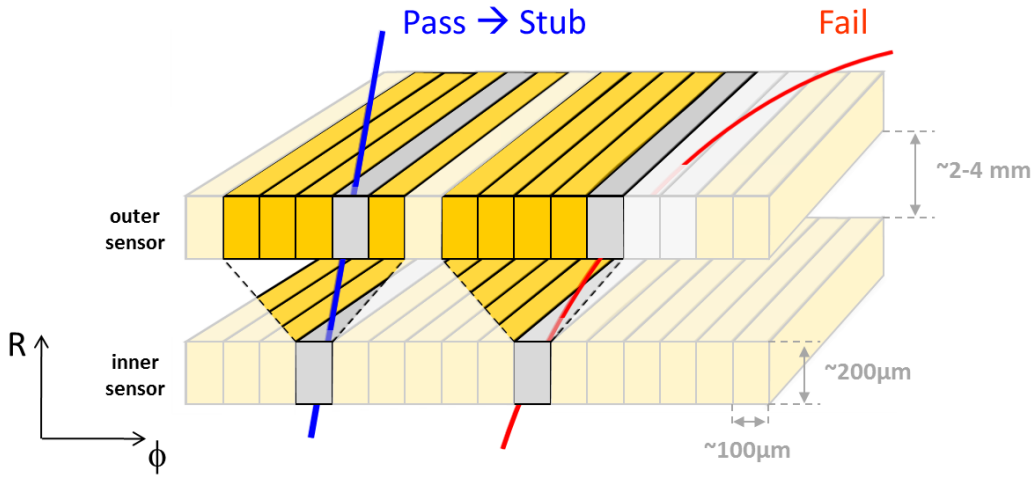

Figure 2. Trigger module concept.

the Pt-cut, together with the spacing between the two sensors (which is tuned at the assembly stage to ensure a uniform Pt-cut across the volume of the tracker).

Figure 1 shows one of the two different modules being designed for the strip tracker: the "2S" module (Strip-Strip) couples two 10×10 cm silicon strip sensors, with a pitch of 90 μm, and will instrument the outer tracker at radii greater than 50 cm.

2 Design and measured performance

The CBC2 is a 254-channel front-end readout ASIC designed in 130 nm CMOS for the readout of silicon microstrip sensors, optimized for the 2S-module of figure 1. The first version of the CMS Binary Chip was a full-scale prototype with 128 channels, binary and un-sparsified readout, which included many of the features present on the CBC2, but did not have the capability to contribute to the L1 trigger [2]. The CBC was delivered in February 2011 and has been extensively tested and employed in a telescope during test beam with good results [3, 4].

The CBC2 doubled the number of channels to 254, adopting a bump-bondable pad layout with 250 μm pitch, and introduced several new features to the CBC1 to improve the design and to address some of the new requirements of the tracker upgrade, such as the stub formation. An

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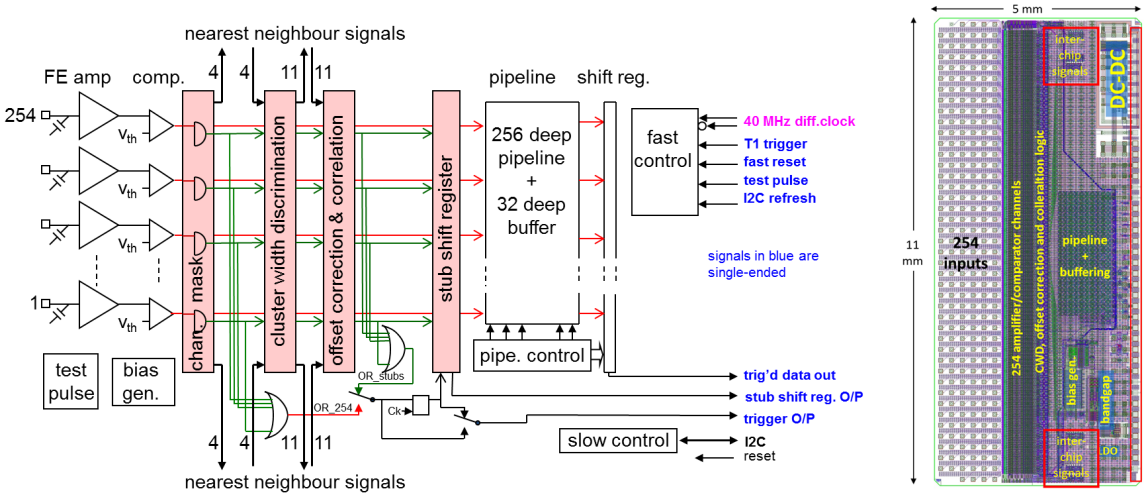

Figure 3. CBC2 block diagram and layout.

on-chip test pulse circuit and minor improvements to the front-end were included, together with an improved version of the on-chip DC-DC converter provided by CERN. The CBC2 was received in January 2013 and is fully functional and working to specifications.

2.1 CBC2 architecture and overview

The chip has 254 front-end channels, with preamplifier, gain amplifier and comparator. The outputs of the comparators follow two separate data paths (figure 3): in one data are stored in a 256-deep RAM memory buffer, together with the bunch crossing ID. When a L1 trigger is received, the data of interest is loaded into a 32-deep readout buffer before being read out serially at 40 Mbps. A second data path is responsible for identifying and reading out stubs through several stages of combinatorial logic (described in 2.3).

2.2 Front-end performance

The front-end for the CBC2 was adopted from the first version of the CBC (described in [2]), with the exception of a few minor improvements to reduce the susceptibility to common mode noise. The charge integrating amplifier can operate in either holes or electrons readout, and a resistive feedback can accommodate input currents of up to 1 μA per channel, so that the chip can be AC or DC-coupled to the sensor strip. To remove any offset due to leakage current in the front-end, the output of the preamplifier is AC-coupled to a gain amplifier which provides the necessary gain for the following discriminator stage. The DC input voltage of this second-stage amplifier is set globally by a programmable 8-bit DAC, while its output voltage can be offset by setting a local 8-bit DAC in order to compensate for the channel-to-channel mismatch due to the gain amplifier and the following comparator stages. The output of the first two stages has a peaking time of about 20 ns.

2.2.1 Noise and power

The front end was originally designed for a capacitance corresponding to a strip length of 2.5 cm, but the detector and module designs have since evolved and a strip length of 5 cm is currently

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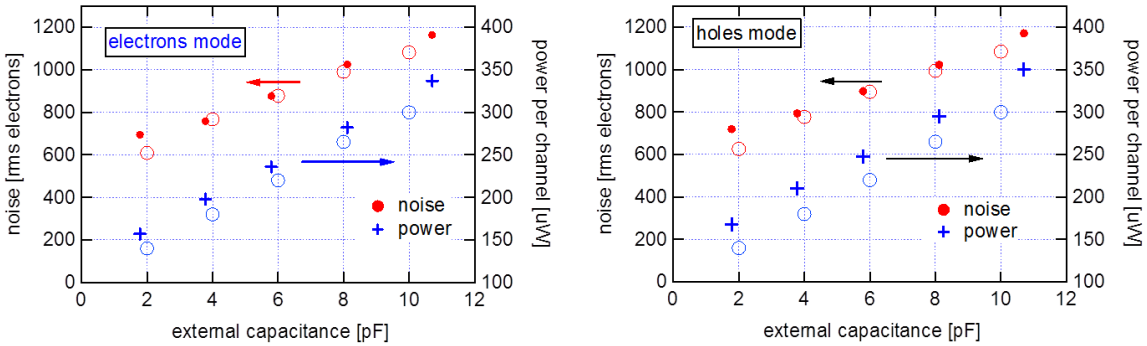

Figure 4. Noise and analogue power consumption as function of the external capacitance for the CBC (solid symbols are measurements, open symbols simulations).

foreseen. Fortunately sufficient headroom was allowed in the design to tolerate larger capacitances by increasing the input device bias current to meet the original noise target of less than 1000 electrons. The noise performance is a function of the input capacitance and the ENC can be expressed as $500 + 64$ Cin/pF electrons rms for both electrons and holes readout; for a typical value of 5 pF the CBC2 achieves a readout noise of 820 electrons for a total power consumption of about 300 μW/channel. The noise and analogue power consumption for the first iteration of the CBC are shown in figure 4 as a function of the external capacitance; the digital power consumption was measured below 50 μW/channel. The measurements performed so far for the CBC2 are compatible with these results, as expected given that the two chips share the same front end with only minor differences.

2.2.2 Comparator

The last stage of the front-end channels is a comparator which provides the binary data to be written into the memory buffer. The hysteresis feedback of the comparator used for the first iteration of the chip has been replaced with a different architecture with internal programmable hysteresis in the CBC2 to avoid common mode susceptibility when many channels are active at the same time. For the same reason, the reference voltage of the gain amplifier is now buffered locally in each channel.

A global 8-bit DAC plus the local 8-bit DAC described in section 2.2 allow a uniform threshold to be set across the chip. Being a binary readout, the analogue performance must be inferred from the S-curves which represent the hit count per channel as a function of the comparator threshold. Figure 5 shows that the threshold dispersion can be limited to 70 electrons rms after calibration.

The comparator is followed by a so-called "hit-detect" logic circuit which, if enabled, limits the duration of the comparator output to one bunch crossing to avoid out-of-time pile-up in the memory buffer. Alternatively, the chip can be operated so that the comparator output follows the output of the gain amplifier when returning to zero.

2.2.3 Gain

The internal test pulse allows to extract the gain of the front-end, which is about 45 mV/fC for both electrons and holes. The slightly undulating characteristic of the gain plots of figure 6 is due to a non-linearity of the DAC used to set the threshold. This problem was not visible in

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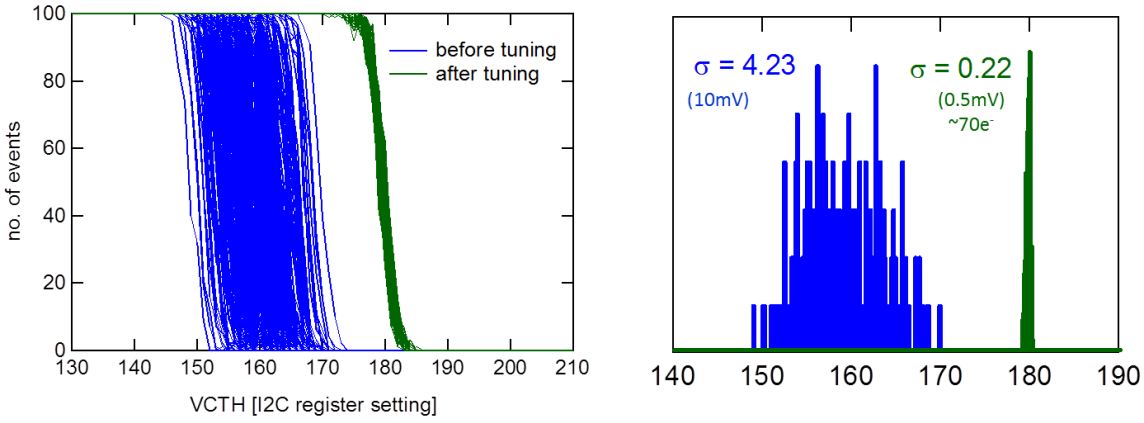

Figure 5. Threshold dispersion for the 254 channels before and after calibration.

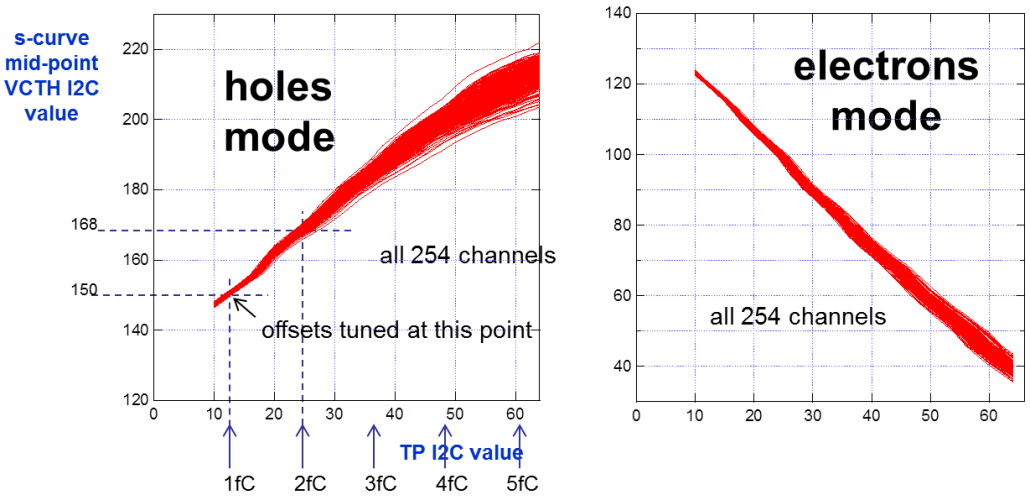

Figure 6. Gain measurements for one CBC2 ASIC.

the first iteration of the chip, where the global threshold was supplied externally to suppress the common mode noise mentioned before, therefore masking the DAC performance. It should be stressed that the gain needs to be linear only in the region where the threshold will be set, between 1 and 2 fC.

2.3 Stub-finding logic

The combinatorial logic responsible for identifying stubs is implemented in successive stages [7]. A programmable mask prevents noisy or faulty channels from saturating the following stages. The Cluster Width Discriminating (CWD) logic that follows removes clusters wider than a selectable width of one, two or three adjacent hits as a first means to reduce the data rate for stubs, since wide clusters are typically associated with low-P_T tracks. The rejection of wide clusters is performed for hits on both sensor layers, and the central hit of clusters which are not rejected is passed on to the following stage of the logic. The CWD can also be programmed to be effectively bypassed so that no cluster is rejected.

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The following stage corrects for geometrical offsets along the module and identifies stubs by performing the correlation between the two sensors. Considering the centers of valid clusters as inputs, for any input belonging to the inner layer, the logic looks for a hit on the outer layer in a "coincidence window" centered on the strips directly above it. If any cluster is found in this window, the inner strip is considered a valid stub. The size of the programmable window determines the P_T cut: the width is programmable up to ± 8 strips in intervals of ± 1 strips, and to compensate for parallax across the width of the module the window can be shifted to the left or to the right of the central strip by a programmable offset in the range ± 3 strips. The window width is set globally for all channels, whereas the offset can be programmed independently in two regions of each chip.

Up to 15 signals must be transmitted by each CBC2 to each neighbouring chip to resolve clusters or stubs crossing two adjacent chip domains in the silicon sensors. Readout modules are designed to be independent units so tracks which extend across module boundaries will be resolved by overlapping the modules along η. The CBC2 does not yet implement a full stub readout; as a test feature, stubs can be written onto a shift register and read-out at 40 MHz. Other interesting test features are a fast-OR of all the stubs and a fast-OR of all the channel outputs. Either can be selected to be output and at the same time used to parallel-load the stubs onto the shift register for serial readout. Once output these ORs can be used to trigger the CBC2, effectively operating the chip in a "self-triggered" mode.

2.4 On-chip power elements

The CBC2 incorporates a DC-DC switched capacitor converter, designed by CERN [8], which can provide the required 1.2 V from a 2.5 V supply. This voltage is filtered off-chip and used to power the digital circuits on the ASIC. An on-chip low-dropout linear regulator is used to provide a clean power supply to the analogue front-end and filter out switching noise from the DC-DC converter. Both these elements were functional in the first iteration of the CBC, but some noise injection from the switched capacitor converter was observed in the front end. The CBC2 incorporates an improved version of the DC-DC converter optimized to reduce switching noise; although the circuit is functional and has been used to power the chip, a measurement of the noise injection on the front end has yet to be performed on the CBC2. The measurements presented in this paper were obtained with an external power supply powering the on-chip linear regulator.

3 Test activities

The CBC2 was part of a multi-project wafer run which underwent a manufacturing split to provide wafers with both wire-bonding and bump-bonding metallization. So far two of the bump-bonded wafers have been screened with yield in excess of 95%. Figure 7 shows how the last row of pads is used to probe the chip on the wafer without damaging the bumps.

The testing of the CBC2 started in February 2013 with the wire-bonded version (figure 8); because of its similarities with the first CBC, this version was useful to quickly develop test procedures for the bump-bonded wafers. It will also be used in the total ionizing dose tests with x-rays since it allows to irradiate the chip face-up.

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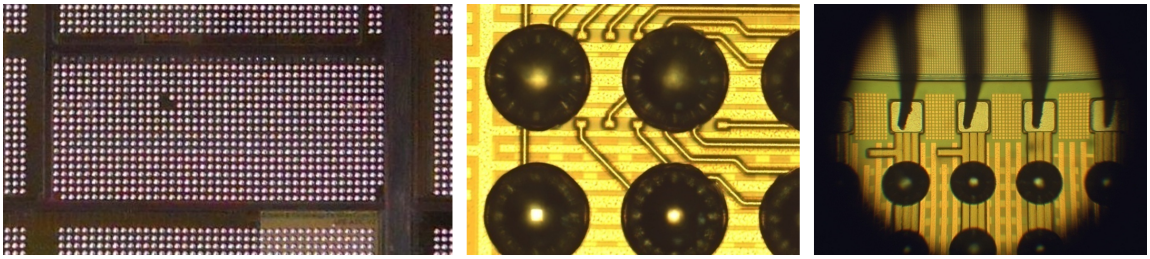

Figure 7. Left: three missing pads in the central region and one in the corner ensure the layout is asymmetric. Center: detail of C4 bumps and top-level tracks. Right: wafer probing of the last row of pads, free of bumps and with wire-bondable metallization.

Figure 8. CBC2 test setups. Left: wire-bonded CBC2 connected to an hybrid interface cards for I2C SLVS level translation. Center: dual-CBC2 hybrid with precision input capacitors, pitch adapter and interface card. Right: dual-CBC2 2S-module with two 5 cm, 80 μm pitch sensors wire-bonded to the hybrid.

3.1 Dual-CBC2 hybrid test

A high-density hybrid for the CBC2, presented in detail in [6], has been designed by CERN as a prototype for the 2S-module hybrids. By accommodating two readout chips side-by-side, it allows to fully exercise the inter-chip links and the coincidence logic, as well as to test the performance of the bump-bonded version of the CBC2, thereby benefiting from the full connectivity of the high number of power and ground connections. The hybrid plus ASICs were initially tested with an electrical setup to inject input signals. Two 5 cm silicon sensors were later mounted and wire bonded to the hybrid to create a dual-CBC2 readout module. The microstrip pitch of 80 μm and the separation of few mm between sensors were kept as close as possible to the design specifications for the 2S-module.

3.2 Results with test pulse

An on-chip test pulse circuit allows the injection of a known charge into the front-end channels, which for this purpose are organized in eight groups of 32 channels each. These test groups are such that channels corresponding to strips aligned above each other on the two sensors layers can be injected at the same time (figure 9): this feature coupled with the possibility to mask individual channels and to offset the coincidence window allows to test all the features of the coincidence logic.

3.3 Results with beta-source

β electrons using a Sr^{90} source positioned on top of the microstrip sensors on the dual-CBC2 module were used to test the functionality of the CBC2 logic. Two distinct profiles are clearly

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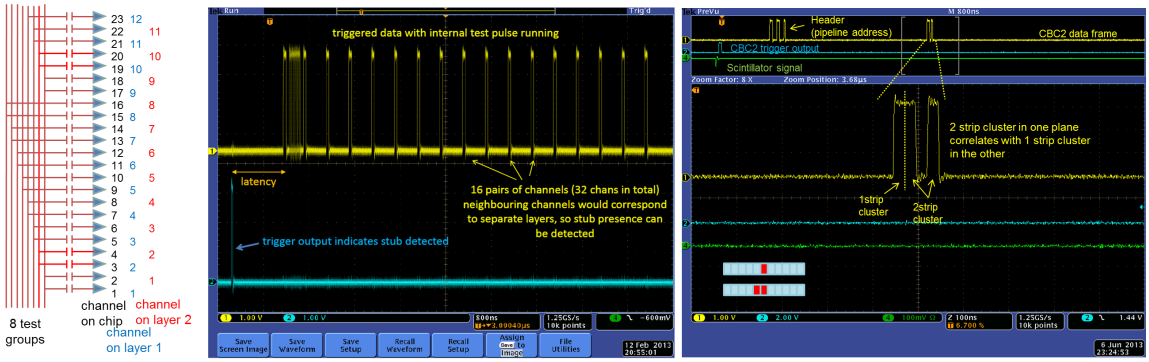

Figure 9. Left: test-pulse connectivity and results. Right: result with cosmic rays; the inset shows the equivalent hit pattern on the strips.

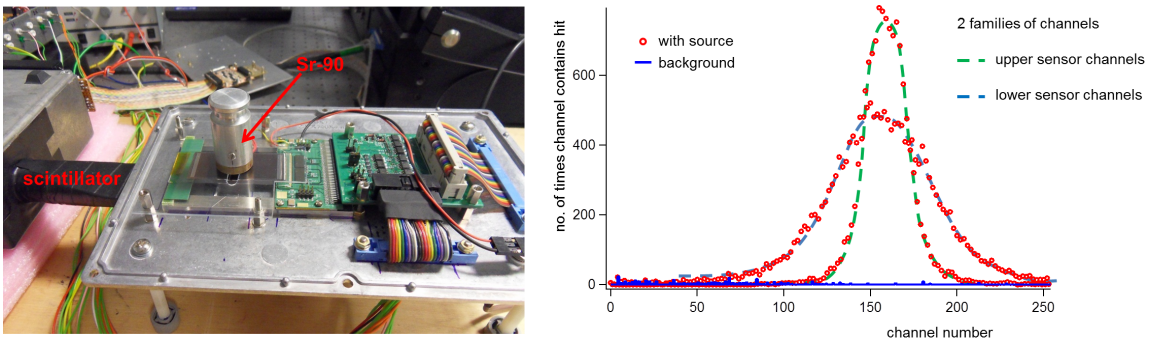

Figure 10. Left: beta source positioned on top of a dual-CBC2 2S-module. Right: hit counts for the channels of one of the two CBC2: upper and lower sensors are clearly mapped in two separate families.

identifiable in the hit counts for channels belonging to the two different sensors but read out by the same chip, as shown in figure 10.

3.4 Results with cosmic rays

The same dual-CBC2 module with its self-triggering capabilities can also be used to effectively trigger on cosmic rays, although the rate is very low ($\ll 1$ Hz) even when the coincidence window is set to its maximum value. An example of a measurement from cosmic ray is given in figure 9: a scintillator is used to trigger the oscilloscope, but the fast OR of the stubs on the chip also provides a low latency signal that can be used for triggering, after which the stubs stored in the shift register can be read out to compare them with the data stored in the memory buffer for L1 readout.

4 Conclusions and future developments

The CBC2 is the latest of two successful full-scale prototype ASICs designed for the phase-II upgrade of the CMS strip tracker. The CBC2 has been tested extensively since February 2013 and all its features are working extremely well. The front-end meets the noise and power specifications and the logic for cluster discrimination and stub identification has been tested successfully. Together with the development of the high-density hybrid developed by CERN, the availability of the

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bump-bondable CBC2 has allowed good progress towards the integration and the prototyping of the 2S module for the outer tracker. Several prototype 2S-modules bonded to microstrip sensors have been assembled and tested with β source and cosmic rays. A first beam test is scheduled at DESY for the end of 2013 and will study the efficiency of stub identification and test the data readout for the module. Total ionizing dose and SEU tests will follow to fully characterize the ASIC.

A road map for the development of the production version of the CMS Binary Chip has been established, and will see an additional prototype followed by a pre-production version. Some of the new features already identified for the CBC3 include half-strip resolution for stubs, front-end optimized for n-on-p, AC-coupled 5 cm strip sensors and a full readout for stubs at 40 MHz.

Acknowledgments

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