Integration of an Active-Filter and a Single-Phase AC/DC Converter with Reduced Capacitance Requirement and Component Count

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***Abstract*— Existing methods of incorporating an active filter into an AC/DC converter for eliminating electrolytic capacitors usually require extra power switches. This inevitably leads to an increased system cost and degraded energy efficiency. In this paper, a concept of active-filter integration for single-phase AC/DC converters is reported. The resultant converters can provide simultaneous functions of power factor correction (PFC), DC voltage regulation and active power decoupling for mitigating the low-frequency DC voltage ripple, without an electrolytic capacitor and extra power switch. To complement the operation, two closed-loop voltage-ripple-based reference generation methods are developed for controlling the energy storage components to achieve active power decoupling. Both simulation and experiment have confirmed the eligibility of the proposed concept and control methods in a 210 W rectification system comprising an H-bridge converter with a half-bridge active filter. Interestingly, the end converters (Type I and Type II) can be readily available using a conventional H-bridge converter with minor hardware modification. A stable DC output with merely 1.1% ripple is realized with two 50 μF film capacitors. For the same ripple performance, a 900 μF capacitor is required in conventional converters without an active filter. Moreover, it is found out that the active-filter integration concept might even improve the efficiency performance of the end converters as compared with the original AC/DC converter without integration.**

***Index Terms*—Single-phase AC/DC converter, capacitance reduction, active filter integration.**

I. INTRODUCTION

The growing use of emerging technologies such as LED lightings, distributed photovoltaic (PV) systems, electric vehicle (EV) charging systems, etc., is placing high reliability, high power density and low-cost single-phase AC/DC power conversion systems in great demand [1]–[4]. A well-known issue in conventional single-phase AC/DC systems is that there is a power difference between the AC and DC side, which varies at twice the line frequency. Without an energy buffer, this varying power could cause significant voltage fluctuation at the DC side, and is detrimental to both ends of the AC/DC system [3], [5]–[16]. Typically, bulky electrolytic capacitors (E-Caps) are mounted across the DC side to buffer the pulsating power. However, E-Caps have short lifetime and low reliability [17], which hampers the actualization of a reliable AC/DC conversion system. Alternatively, long lifetime non-E-Caps (e.g. thin film caps) can be used to directly replace the E-Caps. However, this will result in increased system volume, weight and cost, due to the low capacitance density of non-E-Caps.

Recently, many active-power-filter-based approaches have been proposed to improve the reliability without the use of large non-E-Caps [3], [8]–[10], [13]–[15]. With these methods, the pulsating ripple power can be actively decoupled from the DC side using only a small external energy storage device (e.g. film capacitor(s)), which buffers the ripple power by allowing its voltage and current to vary with large fluctuation without affecting the normal operation of either the AC or the DC side of the system. In this way, high reliability and power density of the overall system are concurrently achieved. Fig. 1 illustrates three previous advancements that are based on the H-bridge converter [3], [8]–[10]. The H-bridge converter with switches Q1–Q4 and filter components L_1 and C_{dc} accomplishes the original functions of active power factor correction (PFC) and DC voltage regulation, while the active filter comprising switches Q5 and Q6 are controlled to divert the ripple power from the DC side into a small external storage L_f or/and C_f to achieve power decoupling. Typically one terminal of the storage component is connected to the mid-point of the active filter switches (connection point of Q5 and Q6), while the other terminal is tied to either the AC side [9], [18], the ground [3], [19], or one leg of the H-bridge converter [10], [14]. The voltage or current waveforms of the storage component can be unipolar or bipolar, depending on circuit configuration.

Despite the improvement in reliability and power density, these solutions typically increase the system cost and complexity, and degrade the overall efficiency, because of the addition of extra active switches and passive

components to the H-bridge converter. It is proposed in [15] that, by controlling the energy storage inductor to have a

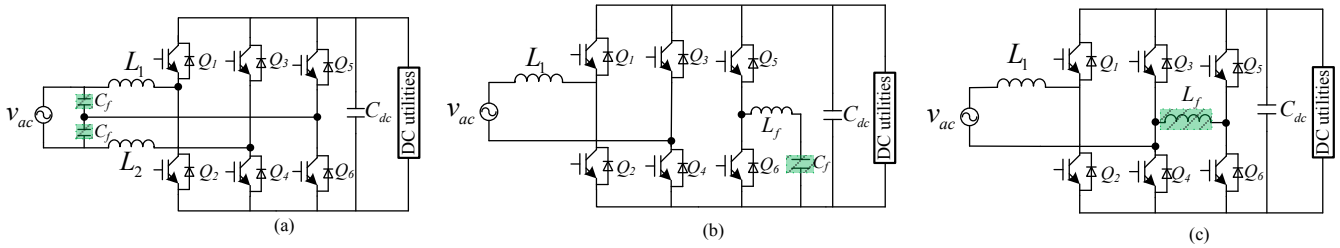


Fig. 1. Examples of existing single-phase H-bridge converter with power decoupling function when storage component connects to (a) AC side [9], [18] (b) ground [3], [19] (c) the phase leg of the H-bridge [10], [14].

unipolar operation, one active switch can be saved in the active filter. Still, one additional active switch and one discrete inductor are required. In [20], power decoupling is accomplished without any additional active switches. However, due to the large DC offset in the energy storage capacitors, there is a large circulating current flowing within the system, which lowers the power efficiency and increases the current stresses of the circuit components.

In this paper, a concept of active-filter integration with a single-phase bidirectional AC/DC converter is reported. The proposal is a natural extension from the previous publications [21], [22], in which a pair of active power switches is shared between an H-bridge converter and a buck-boost type active filter. The resultant converters from the concept can therefore achieve bi-directional AC/DC power conversion that includes power factor (PF) control, voltage regulation, and active power decoupling function without additional power switches or an E-cap. Consequently, high reliability, high power density and low cost are achieved simultaneously. To complement converter operation, two kinds voltage-ripple based closed-loop reference generation methods that require simple controller design and implementation are proposed and compared. As an illustrative example, the feasibility of the active-filter integration concept and the control methods are verified through simulation and experiment on a 210 W hardware prototype of an H-bridge converter with an integrated half-bridge active filter. Compared with a conventional H-bridge converter, the resultant converter can significantly reduce the output voltage ripple to within 1.1%. With active-filter integration, not only the overall cost and system complexity are reduced, the efficiency performance can also be improved.

II. Concept of Active-Filter-Integration With a Single-Phase AC/DC Converter

A. Existing Method

Fig. 2 shows the existing method of deriving a single-phase AC/DC converter with the power decoupling function that is based on the H-bridge topology. It is formed simply by cascading an H-bridge converter with an active filter. Shunt active filtering [3], [8]–[10], [14], [15] and series active filtering [23], [24] are all possible candidates for configuration. The three topologies shown in Fig. 1 are all of such a circuit arrangement. Through proper control, the storage component C_f or L_f will instantaneously absorb the necessary fluctuating power (e.g. the double-line frequency power) from the DC side, so that the power at DC side is effectively constant without low frequency variation. However, the add-on devices required by the solution result in the topology needing additional components as compared to the original H-bridge converter.

B. Concept of Active-Filter-Integration with an Single-Phase AC/DC Converter

The concept of active-filter-integration with a single-phase AC/DC converter is illustrated in Fig. 3. While the converter is also a combination of the H-bridge converter and the active filter, the switches and passive components are shared and multi-used. The resulting converter can thus provide the same functionality as that of existing solutions, but has a reduced component count.

As illustrative examples, two active-filter-integrated AC/DC converter topologies are illustrated in Fig. 4 namely, Type I and Type II. Both topologies are derived from an H-bridge converter and a symmetrical half-bridge type of active filter [25], [26]. Before circuit integration, the

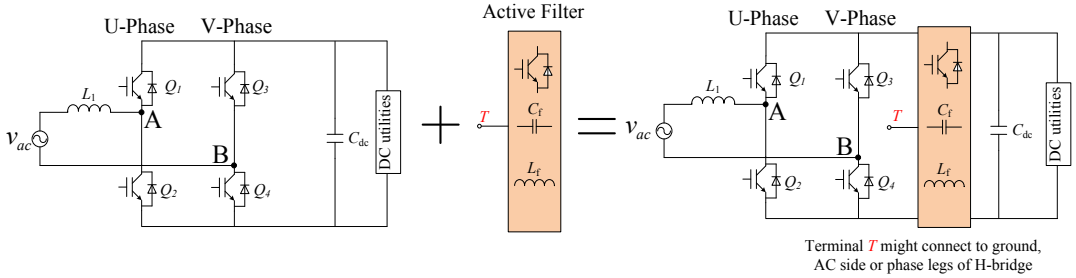


Fig. 2. Circuit configuration of existing single-phase H-bridge rectifier with power decoupling function.

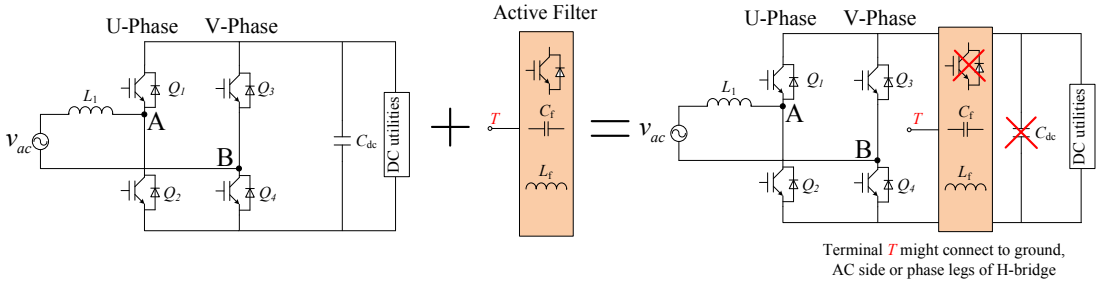


Fig. 3. The concept of a single-phase active-filter-integrated AC/DC converter.

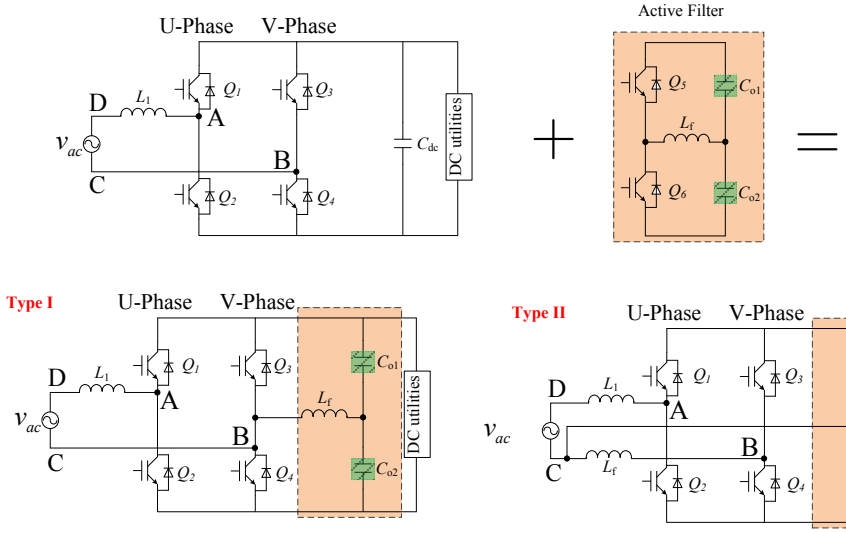


Fig. 4. Two examples of active-filter-integrated AC/DC converter with a symmetrical half-bridge type of active filter

H-bridge converter has two phases (U-phase and two for V-phase), and the active filter has another phase and two storage capacitors C_{o1} and C_{o2}. By sharing the phase leg between the H-bridge converter with that of the active filter, two active switches can be removed. Here, the Type I converter is derived by sharing Q5 and Q6 with Q3 and Q4. Also, due to the configuration of the storage capacitors, which also serve as high frequency filter, the original filter capacitor C_{dc} of the H-bridge can be eliminated. The resultant circuit based on the active-filter-integration concept happens to be the same as that proposed in [27]. Still, such a fundamental equivalence of the Type I converter to an H-bridge converter with a half-bridge active filter was never revealed until now. In Type I configuration, however, an extra inductor L_f used for active filter is still needed. Alternatively, a Type II configuration that is also shown in Fig. 4, takes the active-filter-integration one step further: L_f is used as an active filter inductor and H-bridge inductor at the same time [28]. Therefore, an H-bridge converter with two split input inductors L_1 and L_f can be readily turned into an active-filter-integrated AC/DC converter, without any additional switches or oversize passive components. In this way, the total power density of Type II topology remains low, and is comparable with that of the H-bridge converter. Due to its simplicity, in the following, a Type II converter will be used as a case study example for discussion. Detailed analysis of its operation and control method are also presented. Note that this integration approach can be extended to other types of active filter topologies, such as the bidirectional buck-boost converter [21]. A full comparison of the possible topologies is out of the scope of this paper, but is open for future work.

III. Operation Principles of An Active-Filter-Integrated AC/DC Converter

A. *Circuit Operation of a Single-Phase Active-Filter-Integrated AC/DC Converter*

An averaged equivalent circuit model of the active-filter-integrated AC/DC converter (Type II in Fig. 4) derived through state-space averaging is shown in Fig. 5. Here, i_{ac} is the AC line current, i_{Lf} is the current through inductor L_f, i_C is the total charging current of C_{o1} and C_{o2}, v_{C1} and v_{C2} are respectively the voltages of the energy storage capacitors C_{o1} and C_{o2}. v_{DC} is the DC side voltage. v_A and v_B are the controlled voltage sources in U-phase and V-phase at node A and B, respectively, following

$$\begin{cases} v_A = d_u v_{DC} = \dfrac{1}{2} V_{DC} + V_A \sin(\omega t + \theta_A) \\ v_B = d_v v_{DC} = \dfrac{1}{2} V_{DC} + V_B \sin(\omega t + \theta_B) \end{cases} \quad (0 \le d_u, d_v \le 1), \quad (1)$$

where d_u and d_v are the duty ratios for the high side switches Q_1 and Q_3 in U-phase and V-phase; V_A and V_B are respectively the amplitude of the AC content in v_A and v_B, θ_A and θ_B are their respective phase angles, and V_{DC} is their DC offset.

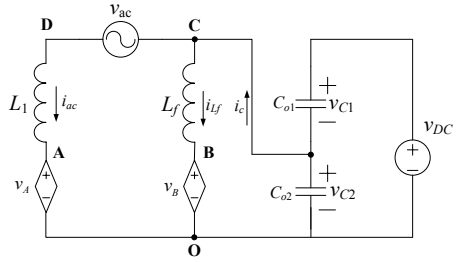


Fig. 5. An averaged equivalent circuit of the Type II active-filter-integrated AC/DC rectifier in Fig. 4.

According to Fig. 5, if the voltages across the inductors L_1 and L_f are neglected, the voltages of v_A and v_B will be approximately equal to that of the respective AC terminals at C and D. Note that the mid-point of C_{o1} and C_{o2} is directly connected to node D, which makes v_B approximately equivalent to v_{C2}. With these assumptions and using (1), the following relationship can be derived.

$$\begin{cases} 0 \le v_A = v_B + v_{ac} = v_{C2} + v_{ac} \le v_{DC} \\ 0 \le v_B = v_{C2} \le v_{DC} \end{cases} \quad (2)$$

In the circuit, if i_{ac} and v_{C2} can be controlled, then both PFC and active power decoupling can be realized. Defining two switching functions of s_U and s_V for U-phase and V-phase respectively, i.e., $s_i \in \{0, 1\}$, $i \in \{U, V\}$, then $s_i = 1$ indicates that the respective top switch (Q_1 or Q_3) is on, and $s_i = 0$ means that it is off.

Intuitively from (2), v_{C2} can be directly controlled by adjusting v_B. According to (1), v_B has a monotonic relationship with s_V, and hence v_{C2} can controlled by s_V in the V-phase switching leg.

Meanwhile, a differential equation with respect to i_{ac} can be obtained from Fig. 5 as

$$L_1 \frac{di_{ac}}{dt} = v_{C2} + v_{ac} - s_U v_{DC} \quad (3)$$

Using (3) and following the principles of (2), the result of different switching mode of s_U can be expressed as follows:

when $s_U = 1$, $di_{ac}/dt = \left(v_{C2} + v_{ac} - v_{DC}\right)/L_1 < 0$, and i_{ac} decreases.

when $s_U = 0$, $di_{ac}/dt = \left(v_{C2} + v_{ac}\right)/L_1 > 0$, and i_{ac} increases.

The above conditions imply that i_{ac} has a monotonic relationship with the switching mode of U-phase. Therefore, i_{ac} can be regulated by simply controlling the U-phase switching leg.

In order to accomplish both PFC and power decoupling, i_{ac} can be controlled to be equal to its command current i_{ac}^* through conventional control techniques (e.g. state feedback control, or hysteresis control) over the U-phase switching leg, and v_{C2} can be controlled to follow a reference voltage v_{C2}^* by modulating it directly with a triangular carrier to drive V-phase. According to (3), the control of v_{C2} and i_{ac} is coupled. At steady state, however, assuming that the switching frequency is much higher than the frequency of v_{C2}, v_{C2} can be treated as a constant voltage source during a switching period. Hence, v_{C2} will not disturb the control of i_{ac}. Similar conclusion can be made for the control of v_{C2} with respect to i_{ac}. Therefore, the control of v_{C2} and i_{ac} can be considered as decoupled at steady state. During transient operations, when v_{C2} undergoes fast changes, the control of v_{C2} will affect the dynamics of i_{ac} as external disturbances. A feedforward term can be adopted to decouple the effect of v_{C2} to the control of i_{ac}, as will be described in Section V.

B. Instantaneous Power Balance Analysis and Modulation Strategy

In this section, the theoretical waveforms of v_{C1} and v_{C2} will be studied based on instantaneous power balance analysis. These waveforms are useful for generating the reference voltage for controlling the energy storage devices. It is assumed in the following analysis that the converter has no power losses, and the instantaneous power in passive components (such as in L_1 and L_f) are neglected. Also, C_{o1} and C_{o2} are assumed identical, i.e., $C_{o1} = C_{o2} = C_f$.

Suppose that the voltage and current at the AC side are sinusoidal with a phase difference of ϕ $\left(0 \le \phi < \pi\right)$, that is

$$v_{ac} = V_{AC} \sin(\omega t) \quad (4)$$

$$i_{ac} = I_{AC} \sin(\omega t + \phi), \quad (5)$$

where ω is the line frequency, and V_{AC} and I_{AC} are respectively the amplitude of the AC voltage and current. For rectifying mode of application, $\phi = 0$, and for inverter mode of operation, $\phi = \pi$.

Using (4) and (5), the instantaneous power at the AC side can be obtained as shown in (6).

$$p_{AC} = v_{ac} \times i_{ac} = \underbrace{\frac{1}{2} V_{AC} I_{AC} \cos\phi}_{P_{DC}} \underbrace{- \frac{1}{2} V_{AC} I_{AC} \cos(2\omega t + \phi)}_{p_r} \quad (6)$$

Note that p_{AC} in (6) contains a DC term P_{DC} and a double-line frequency ripple term p_r. The DC term should equal to the averaged power at the DC side, and the AC term is the oscillating ripple power. In order to absorb p_r using C_{o1} and C_{o2}, the voltage of v_{C1} and v_{C2} can be modulated around $1/2V_{DC}$ with a line frequency AC content, in the form of

$$\begin{cases} v_{C1} = \frac{1}{2}V_{DC} - V_C \sin(\omega t + \theta_C) = \frac{1}{2}V_{DC} - V_C \sin(\frac{\zeta}{2}) \\ v_{C2} = \frac{1}{2}V_{DC} + V_C \sin(\omega t + \theta_C) = \frac{1}{2}V_{DC} + V_C \sin(\frac{\zeta}{2}) \end{cases} (V_C \le \frac{1}{2}V_{DC}), \quad (7)$$

where θ_C is the phase angle relative to v_{ac}; V_C is the amplitude of the AC voltage component in v_{C1} and v_{C2}; and $\zeta/2$ is their instantaneous radiant angle. As v_{C2} is correlated to v_B according to (2), their AC amplitude and phase should satisfy

$$\begin{cases} V_B = V_C \\ \theta_B = \theta_C \end{cases}. \quad (8)$$

From (7), the total instantaneous power absorbed by C_{o1} and C_{o2} can be calculated as

$$p_c = \omega C_f V_C{}^2 \sin(2\omega t + 2\theta_C) = P_C \sin(\zeta), \quad (9)$$

where P_C is the amplitude of p_c.

Let $p_r = p_c$ and using (6) and (9), V_C and θ_C can be determined as

$$\begin{cases} V_C = \sqrt{\frac{V_{AC} I_{AC}}{2C_f \omega}} = \sqrt{\frac{P_C}{C_f \omega}} = \sqrt{\frac{P_{DC}}{\cos\phi C_f \omega}} \\ \theta_C = \frac{\phi}{2} + \frac{3}{4}\pi \ or \ \frac{\phi}{2} - \frac{1}{4}\pi \end{cases}. \quad (10)$$

With (7) and (10) , the reference voltage for C_{o1} and C_{o2} can be generated. It is noted from (10), however, that θ_C could either lead $\frac{\phi}{2}$ by $\frac{3}{4}\pi$ or lag it by $-\frac{1}{4}\pi$. Under both conditions, the half-bridge circuit can absorb exactly the same AC power of p_r (p_c). However, the leading solution is found to be more preferable than the lagging one in practical implementation. This point can be explained with the phasor diagram shown in Fig. 6(a), where the relationships between V_{AC}, V_A and V_C (V_B) are shown. Note that for this phasor diagram, the DC offset in v_A and v_{C2} (v_B) have been removed and only their AC components are considered.

From Fig. 6, it is shown that a lagging θ_C (blue line) leads to a larger V_A, whereas a leading θ_C (red line) results a smaller V_A. In fact, V_A can be calculated as (11) through trigonometric analysis for both cases. It is easy to prove mathematically that V_A in the leading case (first line of (11)) is always smaller than that of the lagging case (second line of (11)), within all possible range of ϕ . Meanwhile, according to (2) and (7), the amplitude of V_A and V_C are constrained by (12), which is represented as a red circle with a radius of $V_{DC}/2$ in Fig. 6.

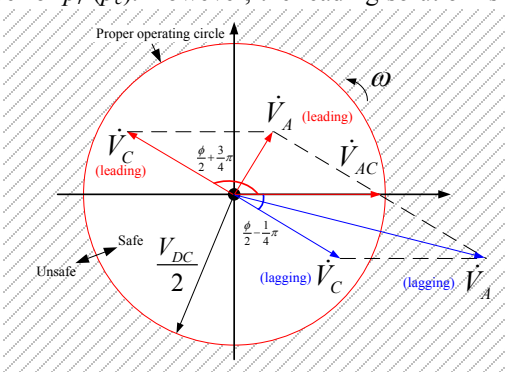
$$\begin{cases} V_A = \sqrt{V_C{}^2 + V_{AC}{}^2 - 2V_C V_{AC} \cos\left(\frac{1}{4}\pi - \frac{\phi}{2}\right)}, & for\ \theta_C = \frac{\phi}{2} + \frac{3}{4}\pi \\ V_A = \sqrt{V_C{}^2 + V_{AC}{}^2 - 2V_C V_{AC} \cos\left(\frac{3}{4}\pi - \frac{\phi}{2}\right)}, & for\ \theta_C = \frac{\phi}{2} - \frac{1}{4}\pi \end{cases} \quad (11)$$

$$0 \le V_{A,}\ V_C \le \frac{1}{2}V_{DC} \quad (12)$$

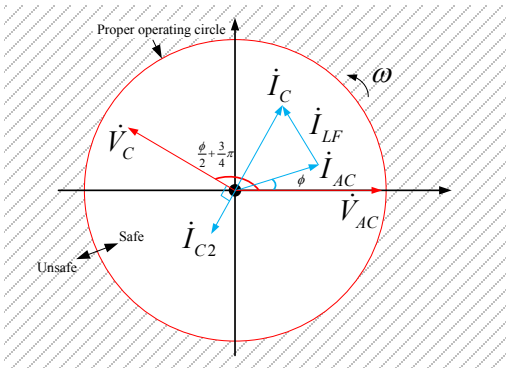
Therefore, if a lagging θ_C is adopted, the constraints posed by (12) can be easily violated (i.e., out of the proper operating circle), and the converter will malfunction. On the other hand, to ensure a proper circuit operation, the lagging solution could limit the maximum amplitude of V_C, and hence reducing the maximum ripple power absorbing capability in accordance to (9), leading to a large C_f value. For these reasons, a leading θ_C is preferred

Substituting $\theta_C = \frac{\phi}{2} + \frac{3}{4}\pi$ into (7) and (9), the radiant angle parameter ζ should satisfy

$$\frac{\zeta}{2} = \omega t + \theta_C = \left(\omega t + \frac{\phi}{2}\right) + \frac{3}{4}\pi. \quad (13)$$



(a)



(b)

Fig. 6. The phasor diagram of (a) V_{AC}, V_A and V_C (V_B) with leading (red) and lagging (blue) θ_C and (b) V_{AC}, V_C, I_{C2}, I_C, and I_{AC}.

IV. Reference Generation for Power Decoupling

A possible method of generating the reference voltage v_{C2}^* is to perform a direct calculation of (7) and (10). Such open-loop instantaneous-power-balance-based methods have been adopted in many literatures for controlling the energy storage devices [8], [15], [25]. Typically, the averaged AC power (i.e., $V_{ac}I_{ac}/2$) and/or the exact value of L_1, L_f and C_f must be explicitly known. These methods provide the insight of the relationship between the ripple power and the operation waveforms of the active filter, and the control implementation can be simple and straightforward. In practice, however, implementation limitations (e.g. inherent sensor offsets) in conjunction with tolerances of the circuit components (e.g. for L_1, L_f and C_f) and so on, will result in deviation from ideal conditions. As a result, the derived v_{C2}^* might be different from the actual value that is required. Also, the results in (10) do not consider the power losses nor the instantaneous power stored in the inductors. Therefore, such an instantaneous-power-balance method will not fully compensate the actual ripple power, and usually some residual voltage ripple still exists at the DC output. In [14], a closed-loop method that is also instantaneous-power-balance-based, is proposed to compensate these deviations.

Alternatively, v_{C2}^* can be predicted based on the instantaneous Δv_{DC} in a closed-loop [21], [26], since the DC voltage ripple Δv_{DC} is a representation of the available ripple power presented at the DC side. The idea is to generate a proper reference v_{C2}^* through feedback control, such that Δv_{DC} =0 at steady state. In this section, two alternative methods for DC ripple based closed-loop reference generation are proposed. Different from the previous methods in [21], [26] which require two current sensors (for i_{ac} and i_{Lf}) and can deal with only the double-line frequency ripple power, the proposed methods can eliminate the need of one current sensor for i_{Lf}, and can be applied for mitigating a multi-frequency ripple power. The proposed control methods can also guarantee a leading θ_C of v_{C2} with respect to v_{ac}.

1) Frame Transformation Method

Fig. 7 illustrates a possible reference generation scheme that is based on frame transformation, of which the DC voltage ripple Δv_{DC} can be tightly controlled. The feedback loop compares v_{DC} with the reference v_{DC}^*, processes the error with a compensator G_c(s), and estimates the ripple power p_r (and hence p_c) as p_c^*, which is transformed into v_{C2}^*. Here, v_c^* is the AC component of v_{C2}^*. Since p_c^* is in the ripple power frame that varies at double-line frequency, whereas the required v_c^* have a line frequency (according to (7)) in the ripple voltage frame, a non-linear frame transformation is required. The transformation from p_c^* to v_c^* should realize the following two functions: (1) a frequency reduction from 2ω to ω; (2) the phase relationship indicated by (13) is met. Such a transformation can be realized by multiplying p_c^* and its reverse orthogonal signal with a matrix as shown in (14). The matrix is

$$T_{trans} = \begin{bmatrix} \cos(\omega t+\varphi) & \sin(\omega t+\varphi) \\ -\sin(\omega t+\varphi) & \cos(\omega t+\varphi) \end{bmatrix}, \quad (14)$$

where φ is a phase angle. It should be emphasized that the use of T_{trans} to perform frequency transformation is a common technique in power electronics and signal processing domain. Suppose $p_c^*=P_c^*\sin(2\omega t+2\theta_c)= P_c^*\sin(\zeta)$, and its reverse orthogonal signal is $-P_c^*\cos(2\omega t+2\theta_c)= -P_c^*\cos(\zeta)$, then

$$T_{trans}\times\begin{bmatrix} P_c^*\sin(2\omega t+2\theta_C) \\ -P_c^*\cos(2\omega t+2\theta_C) \end{bmatrix} = \begin{bmatrix} P_c^*\sin(\omega t+2\theta_C-\varphi) \\ -P_c^*\cos(\omega t+2\theta_C-\varphi) \end{bmatrix}. \quad (15)$$

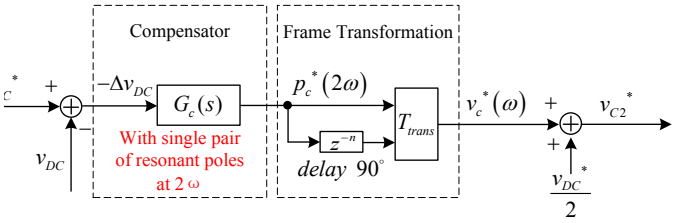


Fig. 7. A closed-loop reference generation scheme based on frame transformation.

Note that the frequency of the output in (15) has been reduced to ω. Meanwhile, in order to satisfy (7), the radiant angle of the output should be $\zeta/2$. Combining (15) with (13), φ can therefore be obtained as

$$\omega t+2\theta_C-\varphi=\frac{\zeta}{2}=\left(\omega t+\frac{\phi}{2}\right)+\frac{3}{4}\pi \Rightarrow \varphi=\theta_C=\frac{\phi}{2}+\frac{3}{4}\pi \quad (16)$$

where φ is a fixed value. Therefore, the transformation matrix in (14) can be easily derived based on the instantaneous radiant angle of line voltage ωt. In this way, a double-line frequency signal p_c^* can be converted into the required line-frequency signal v_c^* and then v_{C2}^* is derived. It should be pointed out, however, that the AC component of the transformed v_{C2}^* using (15) has an amplitude of P_c. This clearly contradicts (10). However, this is not a problem as the control loop can automatically scale the amplitude of p_c^* and hence v_c^* till Δv_{DC} =0. In order for the control loop to respond to the double-line frequency 2ω, which is the dominant frequency for the DC side voltage ripple, a quasi-proportional resonant (Quasi PR) controller that has a pair of resonant poles at 2ω can be used as a compensator G_c(s), as given in (17), to eliminate the double-line frequency content.

$$G_c(s)=k_p+\frac{k_i\omega_c s}{s^2+\omega_c s+(2\omega)^2} \quad (17)$$

where the cutoff frequency ω_c defines the passing band of G_c(s). In practice, in order to minimize the steady-state error of Δv_{DC} , the gain of the Quasi RP controller should be adequate at 2ω. According to (17), the gain of Quasi RP at 2ω is k_p+k_i. On the other hand, ω_c provides an additional degree of design freedom in case that the line frequency varies, which happens in a practical grid. A proper selection of ω_c will ensure a high gain even if the line frequency shifts. It should be noted that, an ideal PR controller [29] can provide infinite gain at 2ω, which is desirable for mitigating the double-line frequency ripple in v_{DC}. However, due to the narrow passing band, the gain of an ideal PR controller will drop drastically when the frequency changes. Therefore, a Quasi RP controller is more preferable from a practical viewpoint.

2) General Transformation Method

The above frame transformation method can effectively mitigate the double-line frequency ripple at the DC side. However, in practical systems, v_{DC} can also contain higher frequency components that are typically introduced by (1) the nonlinearity of the half-bridge active filter, (2) AC voltage and/or current distortion, and (3) the use of nonlinear DC load. In these situations, the ripple power p_r contains both double-line frequency and higher frequency components. The amplitude of these high-frequency components will become considerable as system nonlinearity increases. Unfortunately, the frame transformation method is only applicable for converting signal from double-line frequency into line frequency, and it is inapplicable to signal that contains multi-frequency components. In light of this, a more general approach of transforming p_c^* that contains multi-frequency components into the desired v_{C2}^* is proposed. Fig. 8 shows the proposed reference generation scheme.

As shown in Fig. 8, the state variable v_{DC}^2, instead of v_{DC}, is the control variable regulated to trace the reference $(v_{DC}^*)^2$. The compensator adopted is a multi-PR controller that is the combination of various PR controllers each with predetermined resonant poles (i.e., ω_{c1}, ω_{c2}…), and it can be mathematically described as (18). The poles should be selected at frequencies of which the ripple power is to be eliminated. For example, if p_c^* contains both 2nd and 4th line frequency components, two resonant controllers that have poles at 2ω and 4ω should be adopted to form the compensator.

$$G_c(\mathrm{s}) = k_p + \frac{k_{i1}\omega_{c1}s}{s^2+\omega_{c1}s+(\omega_1)^2} + \frac{k_{i2}\omega_{c2}s}{s^2+\omega_{c2}s+(\omega_2)^2} + \ldots \quad (18)$$

The design principle of a multi-PR controller is similar to that of a single PR controller. The output of the compensator p_c^* is the predicted p_r (p_c), but with high order harmonics. In order to obtain v_{C2}^*, a general form of v_{C1} and v_{C2} are assumed in (19). This is in contrast with (7), in which only the line frequency component is assumed.

$$\begin{cases} v_{C1} = \frac{1}{2}v_{DC} - v_c \\ v_{C2} = \frac{1}{2}v_{DC} + v_c \end{cases} \quad (19)$$

where v_c is the total AC content in v_{C1} and v_{C2}.

Similar to (9), the total instantaneous power absorbed by C_{o1} and C_{o2} can be calculated as

$$p_c = 2C_f v_c \frac{dv_c}{dt} \quad (20)$$

Hence, v_c can be obtained by solving the first-order differential time of (20), and the result is

$$v_c = \pm\frac{1}{\sqrt{C_f}}\sqrt{K_1 + \int p_c dt}, \quad (21)$$

where K_1 is a constant. The transformation of (21) requires only integration and a root operation of p_r (p_c). In the simplest form where K_1 =0, (21) can be simplified to

$$v_c = \pm\frac{1}{\sqrt{C_f}}\sqrt{\int p_c dt}, \quad (22)$$

To visualize the calculated waveforms, Fig. 9 is plotted following three different functions of p_r (p_c) and according to (22):

Case A : p_c=100sin(2ωt);

Case B : p_c=100sin(2ωt)+30sin(4ωt);

Case C : p_c=100sin(2ωt)+30sin(4ωt)+20sin(6ωt),

where ω= 2*π*f =2*π*50= 100 π. C_f= 50 μF.

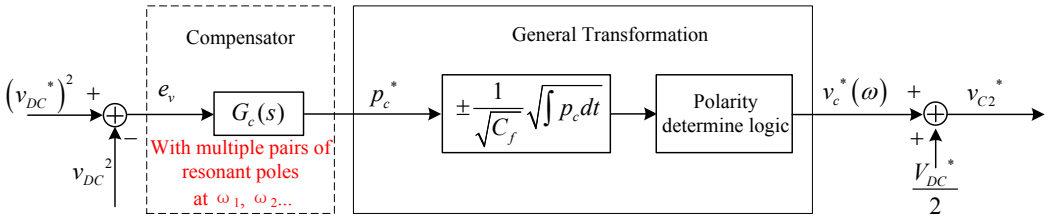


Fig. 8. A closed-loop reference generation scheme based on general transformation.

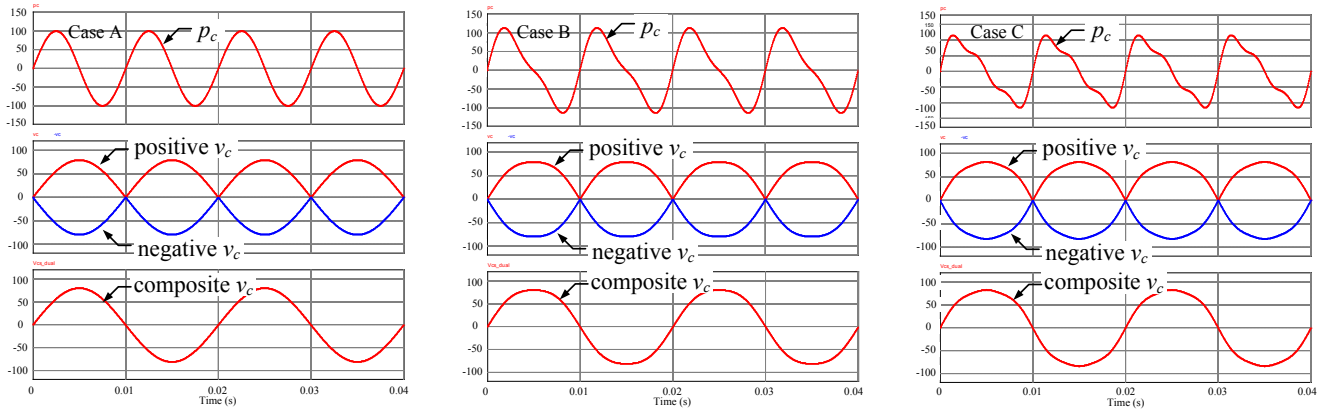


Fig. 9. Some results of general transformation from p_c to v_c based on (22).

Note that the integration in (22) takes place from the initial condition of p_c=0. As seen from Fig. 9, different p_c leads to different solutions of v_c. However, in each case, both the positive and the negative solutions of v_c have a dominant double-line frequency component with some DC offset, rather than being of sinusoidal waveforms varying at line frequency, which would be preferable. Note that the positive and negative v_c come across each other at every half line period. In order to generate a v_c signal that has a dominant line frequency component, the final transformation algorithm that combines the positive and negative v_c can be designed as

$$\begin{cases} v_c = \dfrac{1}{\sqrt{C_f}}\sqrt{\int p_c dt} & \textit{in the } 1^{st} \textit{ half line period} \\ v_c = -\dfrac{1}{\sqrt{C_f}}\sqrt{\int p_c dt} & \textit{in the } 2^{nd} \textit{ half line period} \end{cases} \tag{23}$$

In this way, the composite v_c should have a fundamental frequency ω, as shown in Fig. 9. It may seem from (23) that the exact value of C_f is needed. However, since C_f is only a proportional term in the closed-loop, p_c^* will be automatically adjusted till Δv_{DC}=0, which is similar to the frame transformation method. Therefore, in implementing such a transformation, a precise value of C_f is not required.

On the other hand, since the composite v_c is still assumed to be line-frequency dominated, it is preferred that v_c should lead v_{ac} by a phase angle of approximately $\frac{\phi}{2}+\frac{3}{4}\pi$, which is similar to the case when only the double-line frequency component is considered in p_c^*. Fig. 10 shows the waveforms of v_{ac}, a phase-leaded v_{ac} (lead v_{ac} by $\frac{\phi}{2}$), defined as v_{ac_lead}, and the desired v_c that is leading v_{ac}. Clearly, at the zero crossing instant of v_c, when the radiant of v_{ac_lead} is around $-\frac{3}{4}\pi$ (v_{ac_lead} <0), v_c will be increasing and going into positive range for half-line period; when v_{ac_lead} has a radiant of around $\frac{1}{4}\pi$ (v_{ac_lead} >0), v_c will be decreasing into the negative range. This feature can be used to formulate the polarity determine logic given in Fig. 8, such that a leading v_c can always be guaranteed. For example, as shown in Fig. 10, a positive pulse will be generated at the zero crossing point of v_c if the instantaneous v_{ac_lead} is negative, indicating that v_c is entering a positive half line cycle, and a positive v_c in (23) is adopted. Similarly, if the measured v_{ac_lead} is positive, then a negative pulse will be generated, and hence a negative v_c.

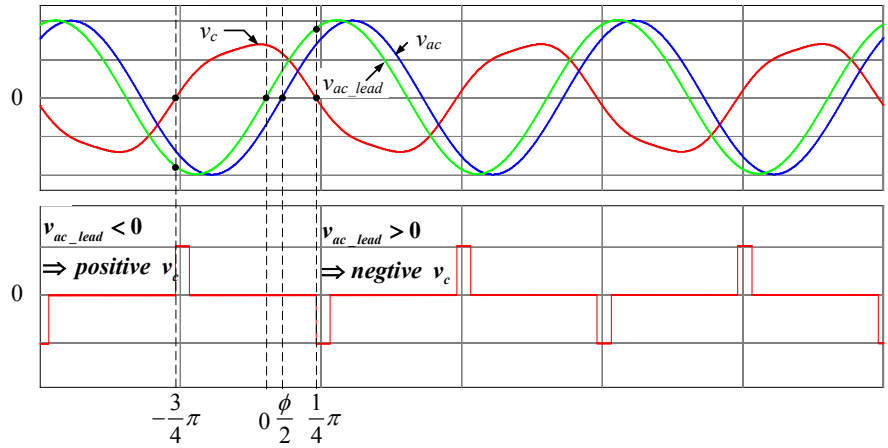


Fig. 10. Diagram of v_{ac}, v_{ac_lead} and the desired v_c (upper scope), and output of polarity determine logic (lower scope).

V. Control Design of An Active-Filter-Integrated AC/DC Converter

The overall control block diagrams for an active-filter-integrated AC/DC converter that works as a rectifier are shown in Fig. 11. The upper part of the control blocks are in charge of AC current shaping and DC output voltage regulation, and the lower part performs the power decoupling function. The design of the PFC controller is similar to that of a typical PFC converter. However, according to the discussions in Section III, there is a coupling effect between the control of i_{ac} and v_{C2}. The small-signal representation of the coupling effect shown in (24) can be obtained from (3). It is clear from (24) that i_{ac} is a non-linear function of its control signal v_A due to the presence of v_{C2}. To decouple the control system, a feedforward term $-v_{C2}^*$ can be added to v_A^*. Therefore, i_{ac} is a linear function of the new control signal $(v_A^* - v_{C2}^*)$ according to (24), and the control of i_{ac} will be independent of that for v_{C2}.

$$L_1 \frac{d\tilde{i}_{ac}}{dt} = \tilde{v}_{C2} - \tilde{v}_A , \tag{24}$$

The other focus of the control loop is the design of the power decoupling control loop. According to the converter configuration, if a resistive load of R is assumed, and the instantaneous power in L_1 and L_f as well as the power losses are neglected, the power balance is

$$p_{AC} = \frac{{v_{DC}}^2}{R} + p_c + C_e v_{DC} \frac{dv_{DC}}{dt} = \frac{{v_{DC}}^2}{R} + p_c + \frac{C_e}{2}\frac{d\left({v_{DC}}^2\right)}{dt} \tag{25}$$

where C_e is the equivalent capacitance of the two series capacitors C_{o1} and C_{o2} in the half-bridge active filter, i.e., C_e=1/2 C_f. It is emphasized that p_c here is the controlled capacitor power assuming a constant v_{DC}, while the 3rd term on the right-hand side of (25) corresponds to the rate of change of energy in C_e, which is effectively in parallel with the DC output when v_{DC} fluctuates.

Linearization of (25) around its steady-state equilibrium gives the small-signal equation

$$\tilde{p}_{ac} = \frac{\widetilde{{v_{DC}}^2}}{R} + \tilde{p}_c + \frac{C_e}{2}\frac{d\widetilde{{v_{DC}}^2}}{dt}, \tag{26}$$

where the symbol ~ denotes small-signal perturbations. Converting (26) into its Laplace domain equivalent results in a transfer function from $\tilde{p}_c$ to $\widetilde{{v_{DC}}^2}$ as

$$G_v(s) = \left.\frac{\widetilde{{v_{DC}}^2}(s)}{\tilde{p}_c(s)}\right|_{\tilde{p}_{ac}=0} = -\left(\frac{2}{C_e}\right)\frac{1}{\tau + s}, \tag{27}$$

where the time constant is

$$\tau = \frac{2}{RC_e}. \tag{28}$$

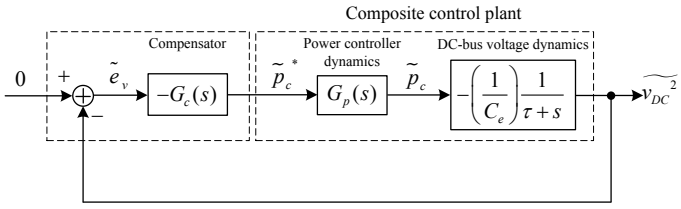


Fig. 12. The control block diagram of the power decoupling loop based on the linearized model.

According to (27) and based on Fig. 11, a control block diagram of the power decoupling loop can be derived as shown in Fig. 12. The assumption here is that the half-bridge active filter can precisely track its command p_c*, such that

$$G_p(s) = \frac{\tilde{p}_c}{\tilde{p}_c^*} = 1. \tag{29}$$

In practice, G_p(s) has a negative phase delay at higher frequencies, which is introduced by the low-pass filter

network of L_f, C_{o1} and C_{o2}. This delay can be significant, especially in high frequency range. Nevertheless, (29) can be ensured if the cut off frequency of $\ell(s)$, i.e., ω_c, be chosen adequately lower than the bandwidth of G_p(s).

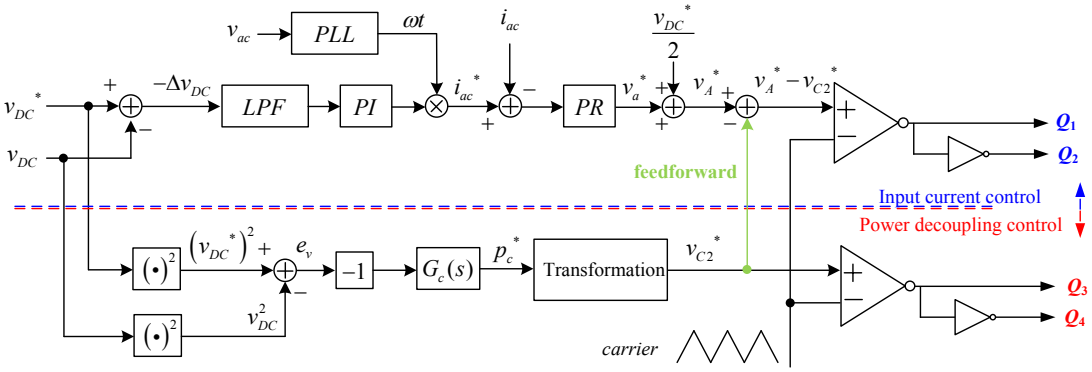


Fig. 11. The control schematic diagram of the active-filter-integrated AC/DC converter when working in rectifying mode.

-1 to compensate the negative sign of G_v(s) in (27). Therefore, the total open-loop gain is

$$\ell(s) = G_c(s)G_p(s)G_v(s). \tag{30}$$

By considering (30), the compensator G_c(s) can be readily designed according to specific transient, steady state and stability requirement. Consider an active-filter-integrated AC/DC converter operating as a rectifier, with circuit parameters listed in Table I, and single PR control with resonant poles at 100 Hz. The Bode plots of the power decoupling loop with and without the consideration of G_c(s) are given in Fig. 13. It can be observed that the incorporation of a PR controller hardly modifies the uncompensated loop gain except at frequencies around the 100 Hz, where there is a gain boost. After compensation, the overall system has a crossover frequency of around 3.18 kHz, which is much faster than that of a DC-bus regulation loop design in a conventional PFC application. The high bandwidth of the power decoupling loop ensures that the low-frequency ripple contents and its including high-order harmonics are effectively mitigated at steady state. The stability of the control loop is also sufficiently guaranteed.

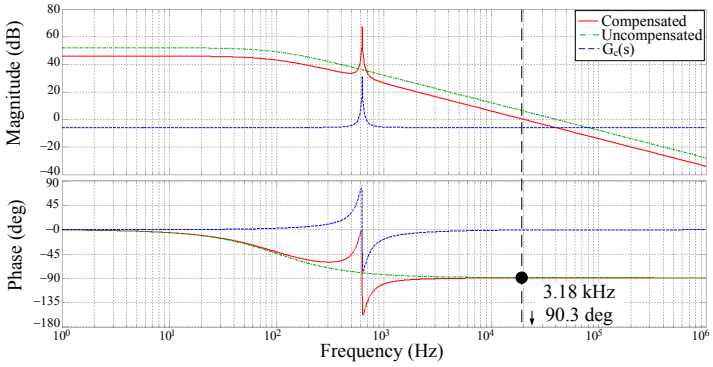


Fig. 13. Bode plots of open loop gain for the power decoupling loop.

According to Fig. 11 and Fig. 12, G_c(s) is multiplied by

VI. Design Criteria of Circuit Components

A. Selection of Energy Storage Capacitors

According to (10), the values of C_{o1} and C_{o2} will determine the amplitude of v_{C1} and v_{C2}. A smaller C_{o1} and C_{o2} will lead to larger swing of v_{C1} and v_{C2}, and vice versa. Given the constrains of v_{C2} in (12), the minimum C_f should satisfy

$$C_{f\_\min} = \frac{4P_{DC\_\max}}{\cos\phi\omega V_{DC}{}^2}, \tag{31}$$

where $P_{DC\_\max}$ is the maximum allowable DC power of the converter. A larger V_{DC} and higher power factor tend to reduce the requirement of the energy storage capacitance. Compared with the DC capacitance requirement C_{dc_H} in a conventional H-bridge converter with a voltage ripple of Δv_{DC} for a DC power of $P_{DC\_\max}$, that is

$$C_{dc\_H} = \frac{P_{DC\_\max}}{\omega V_{DC}\Delta v_{DC}\cos\phi}, \tag{32}$$

the capacitance requirement in an active-filter-integrated converter is reduced by

$$\frac{2C_{f\_\min}}{C_{dc\_H}} = \frac{8\Delta v_{DC}}{V_{DC}}. \tag{33}$$

When the minimum capacitance of (31) is selected for C_f, the peak voltages of v_{C1} and v_{C2} will be V_{DC}, which defines the voltage ratings of C_{o1} and C_{o2}.

On the other hand, by differentiating (7) and using (10), the capacitor current i_{C1} and i_{C2} for C_{o1} and C_{o2} can be derived as

$$\begin{cases} i_{C1} = \sqrt{\dfrac{P_{DC} C_f \omega}{\cos\phi}} \cos\left(\omega t + \theta_C\right) \\ i_{C2} = -\sqrt{\dfrac{P_{DC} C_f \omega}{\cos\phi}} \cos\left(\omega t + \theta_C\right) \end{cases}. \quad (34)$$

Therefore, with the minimum capacitance $C_{f\_\min}$, the current ratings of C_{o1} and C_{o2} can be obtained in (35) when P_{DC} reaches its maximum value of $P_{DC\_\max}$.

$$I_{C1\_\max} = I_{C2\_\max} = \frac{2P_{DC\_\max}}{\cos\phi V_{DC}} \quad (35)$$

B. Selection of the Filter Inductors

The design procedures for L_1 and L_f in an active-filter-integrated converter follow that for an H-bridge converter. The three basic design criteria are the maximum allowable current ripple, continuous conduction mode of operation and the current rating. Since there have been extensive discussions on how to select the optimum inductance based on the first two criteria, the focus of this section is to determine the current ratings of the L_1 and L_f for an active-filter-integrated converter.

With reference to Fig. 5, the current flowing through L_1 is the AC line current i_{ac}. From (6), the amplitude of i_{ac} is related to P_{DC} and $P_{DC\_\max}$ as

$$I_{AC} = \frac{2P_{DC}}{V_{AC}\cos\phi} = \frac{2P_{DC\_\max}\, p\%}{V_{AC}\cos\phi}, \quad (36)$$

where p% is the relative load power, which is defined as the ratio of P_{DC} to $P_{DC\_\max}$. Substitution of p%=100% into (36) will give the current rating of L_1 as

$$I_{AC\_\max} = \frac{2P_{DC\_\max}}{V_{AC}\cos\phi}. \quad (37)$$

On the other hand, from Fig. 5, the current i_{Lf} of L_f can be obtained using i_{ac} and i_c as

$$i_{Lf} = i_c - i_{ac} \text{ or } \overrightarrow{I_{LF}} = \overrightarrow{I_C} - \overrightarrow{I_{AC}}, \quad (38)$$

where i_c=i_{C1}−i_{C2}, $\overrightarrow{I_{LF}}$, $\overrightarrow{I_C}$ and $\overrightarrow{I_{AC}}$ are the phasor representations of i_{Lf}, i_c and i_{ac}.

From (34) and with the minimum capacitance of $C_{f\_\min}$, the amplitude of i_c can be expressed as

$$I_C = 2\sqrt{\frac{P_{DC} C_f \omega}{\cos\phi}} \xrightarrow[P_{DC}=P_{DC\_\max}\cdot p\%]{C_f = C_{f\_\min}} I_C = \frac{4P_{DC\_\max}}{\cos\phi V_{DC}}\sqrt{p\%}. \quad (39)$$

Different from I_{AC} represented in (36), which is determined by V_{AC}, here I_C is a function of V_{DC}. Combining (36), (38) and (39), and referring to the phasor diagram in Fig. 6(b), the amplitude of i_{Lf} can be derived as

$$I_{LF} = \frac{2P_{DC\_\max}}{\cos\phi}\sqrt{\frac{(p\%)^2}{{V_{AC}}^2} + \frac{4(p\%)}{{V_{DC}}^2} - \frac{4(p\%)^{3/2}}{V_{AC}V_{DC}}\cos\left(\frac{\pi}{4} - \frac{\phi}{2}\right)}. \quad (40)$$

Similar to (37), the current rating of L_f is obtained in (41) by substituting p%=100% into (40).

$$I_{LF\_\max} = \frac{2P_{DC\_\max}}{\cos\phi}\sqrt{\frac{1}{{V_{AC}}^2} + \frac{4}{{V_{DC}}^2} - \frac{4}{V_{AC}V_{DC}}\cos\left(\frac{\pi}{4} - \frac{\phi}{2}\right)} \quad (41)$$

According to (36) and (41), the inductor currents i_{ac} and i_{Lf} are different at different loading condition. In contrast, with the conventional H-bridge converter configuration, i_{Lf} will always be the same as i_{ac}. Since a larger inductor current implies more power losses in the inductors and the respective active switches, it is reasonable to compare the Root-Mean-Square (RMS) values of i_{ac} and i_{Lf} such that an efficiency comparison can be made between an H-bridge converter and an active-filter-integrated converter. It can be concluded that when $i_{Lf\_\mathrm{RMS}} > i_{ac\_\mathrm{RMS}}$, an H-bridge converter will be more energy efficient than an active-filter-integrated converter, whereas when $i_{Lf\_\mathrm{RMS}} < i_{ac\_\mathrm{RMS}}$, the active-filter-integrated converter will be more efficient. The normalized I_{AC} and I_{LF} with based of I_{AC} are

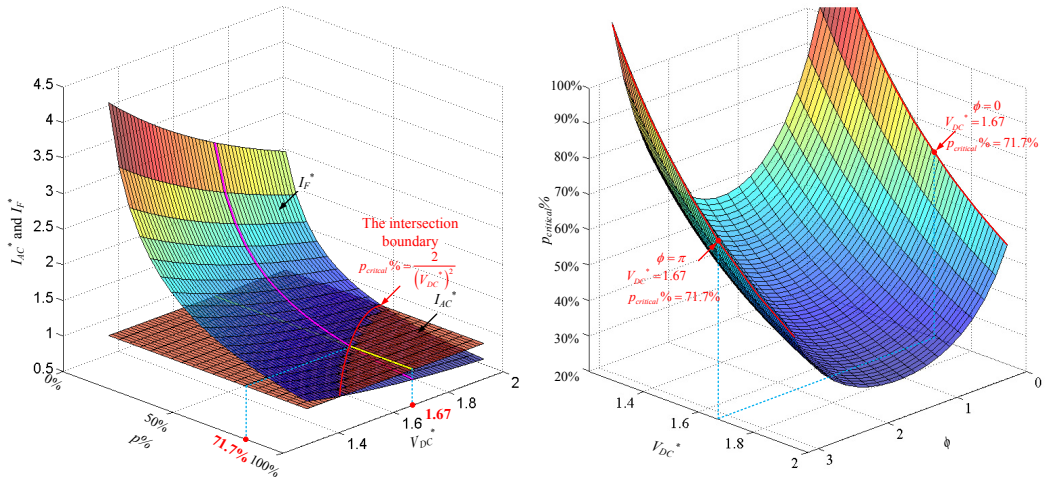
$$\begin{cases} {I_{AC}}^* = 1 \\ {I_{LF}}^* = \sqrt{1 + \dfrac{4}{p\%\left({V_{DC}}^*\right)^2} - \dfrac{4}{\sqrt{p\%}\,{V_{DC}}^*}\cos\left(\dfrac{\pi}{4} - \dfrac{\phi}{2}\right)} \end{cases}, \quad (42)$$

where ${V_{DC}}^*$ is the normalized V_{DC} with base of V_{AC}. Based on (42), the relationship of ${I_{AC}}^*$ and ${I_{LF}}^*$ are shown in Fig. 14(a) for a unity power factor operation, i.e., ϕ=0. It can be observed that there is an intersection boundary between the operating surface of ${I_{AC}}^*$ and ${I_{LF}}^*$. When the relative load power p% is smaller than the power at the intersection boundary, the H-bridge converter is more efficient, whereas at higher load power, the active-filter-integrated converter prevails. The critical load boundary $p_{critcal}$% can be obtained by equating ${I_{AC}}^*$ and ${I_{LF}}^*$ in (42), and is expressed in (43). A full graphical description of the load boundary with respect to ${V_{DC}}^*$ and ϕ is illustrated in Fig. 14(b).

$$p_{critical}\% = \frac{1}{\left[\cos\left(\dfrac{\pi}{4} - \dfrac{\phi}{2}\right){V_{DC}}^*\right]^2} \quad (43)$$

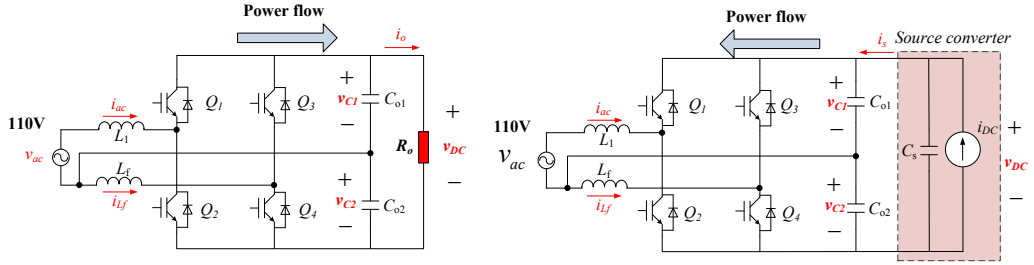
It should be noted from Fig. 14(b) that the derived boundary surface is symmetrical to ϕ. As a result, $p_{critcal}$% will be the same for both rectifying mode and inverting mode of operation. According to the parameters given in Table I, ${V_{DC}}^*$=1.67. The critical loading condition for ϕ=0 and $\phi = \pi$ will be $p_{critcal}$%=71.7%, representing a DC load

of 190 W. Practical verifications of the efficiency performance of an H-bridge converter and an active-filter-integrated converter will be provided in Section VII.



(a) (b)

Fig. 14. (a) Normalized I_{AC}^* and I_{LF}^* with respect to p% and V_{DC}^* and (b).the critical $p_{critical}$% with respect to V_{DC}^* and ϕ .



(a) (b)

Fig. 15. Circuit configuration of (a) an unity power factor rectifier with v_{ac}=110 V and (b) grid-connected inverter with v_{ac}=110 V.

VII. Simulation And Experimental Results

Table I. Key Simulation and Experiment Parameters

Parameters	Rectifying mode	Inverting mode
AC voltage (RMS) v_{ac} (V)	110	110
Averaged DC side voltage v_{DC} (V)	260	260
DC current I_o and I_s (A)	0.81	0.81
Current source internal capacitance C_s (μF)	—	100
Maximum output power $P_{DC\ max}$ (W)	265	265
Rated output power $P_{DC\ rated}$ (W)	210	210
Inductor L_1 (mH)	3.3	3.3
Inductor L_f (mH)	3.3	3.3
Storage capacitor $C_{o1} = C_{o2} = C_f$ (μF)	50	50
Switching frequency (kHz)	25	25
Line frequency (Hz)	50	50

Two sets of simulation are conducted in PSIM environment with the parameters given in Table I. One is for AC/DC rectification application, i.e., ϕ =0, and one is for DC/AC inversion, i.e., $\phi = \pi$. The respective circuit configuration is given in Fig. 15. For rectification, a pure resistive load R_o is used with a load current of i_o. For inversion, the converter is tied to an AC grid, and a current source i_{DC} that is paralleled to C_s is used to emulate a DC energy source converter with an output source current of i_s. The general transformation method is used for generating the voltage reference v_{c2}*for both cases, and G_c(s) has a pair of resonant poles at 100 Hz. It is noted that for inversion, the ac current reference i_{ac}* should have a negative polarity, as opposed to that used for rectification.

Fig. 16 shows the simulation results for both rectification and inversion mode of operation at rated DC power. In both cases, the peak-to-peak DC voltage ripple lies within 5 V, even though the capacitor voltages v_{C1} and v_{C2} are fluctuating significantly. In the inversion mode configuration, the source converter contains a relative large capacitor C_s. However, as can be seen in Fig. 16(b), the stabilized v_{DC} renders a smooth DC source current i_s, and C_s only buffers the high-frequency switching ripples. Obviously, this is beneficial for prolonging the lifetime of the source converters and/or renewable energy sources [2], [9], [30].

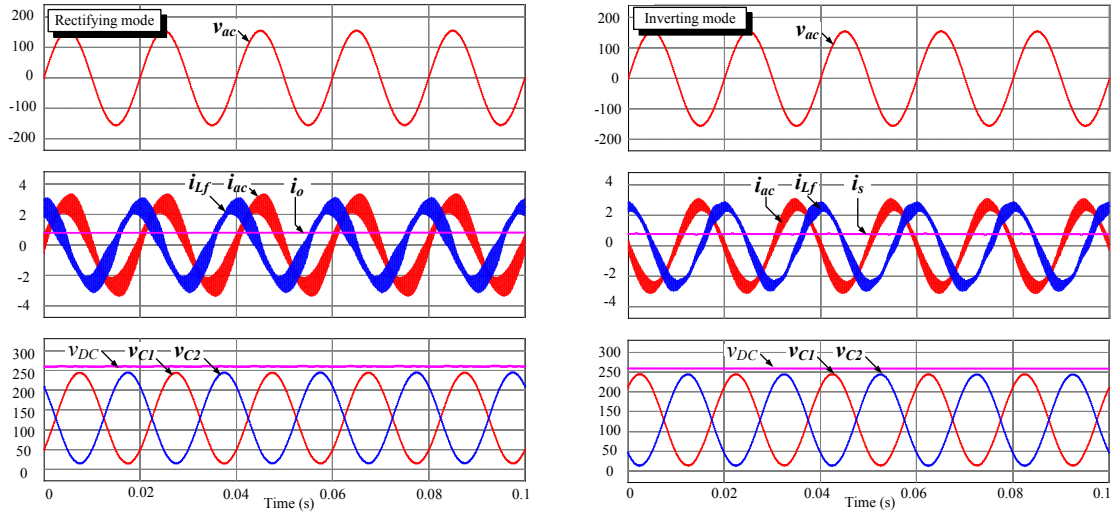
Besides power decoupling, the PFC function is also achieved in both cases, as can be observed from Fig. 16. On the other hand, since the relative load power for P_{DC_rated} is

91.3%, which is higher than the critical load power of 71.7%, from Fig. 14(b), it is predictable that i_{Lf} should have a smaller amplitude than i_{ac}. Clearly, the current waveforms of i_{Lf} and i_{ac} in both Fig. 16(a) and (b) comply with the prediction. Therefore, the current stress in V-Phase is not increased. Moreover, the reduced i_{Lf} will generate less power loss in L_f and V-phase. Therefore, a higher efficiency can be expected with the converter, as compared with an H-bridge converter.

In order to compare the performance of the two reference generation methods, the DC bus of the converter is externally perturbed by 100 Hz and 200 Hz current ripples (both with amplitude of 0.1 A). The simulated waveforms for both the reference generation methods are shown in Fig. 17, which clearly shows that the frame transformation method is incapable of coping with the current disturbances in the presence of the high order harmonics. The DC bus ripple is more than 4.6% (12 V) of the v_{DC}, and the input current is severely distorted. With the general transformation method, the DC bus ripple remains below 1.5%, and the distortion in i_{ac} is acceptable.

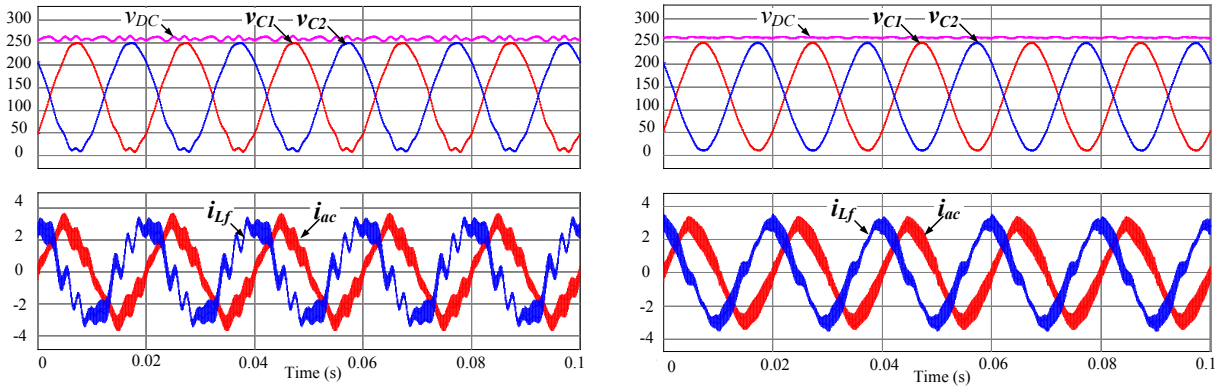
Experimental verification of a 210 W rectification system based on the same system parameters and control method (general transformation method is used here for reference generation) as that given in the simulation is performed. The control is implemented using DSP F28069. Q_1–Q_4 are IGBTs (Model number: IRG4PC30FDPbF). The measured results are given in Fig. 18, which resemble the simulation waveforms given in Fig. 16(a). It can be observed that the input ac current is sinusoidally shaped and in phase with line voltage, and the steady-state peak-to-peak DC voltage ripple stays below 1.9% (5 V) with a large variation of v_{C1} and v_{C2}. Both the PFC and power decoupling functions are practically demonstrated with the active-filter-integrated AC/DC converter.

A comparison of the DC voltage ripple performance between an H-bridge converter rectifier and the active-filter-integrated AC/DC rectifier with different control is provided in Fig. 19. In controlling the active-filter-integrated converter, three reference generation methods are adopted



(a) (b)

Fig. 16. Simulation results for (a) unity power factor rectifier with v_{ac}=110 V (b) grid-connected inverter with v_{ac}=110 V.



(a) (b)

Fig. 17. Simulation waveforms of a non-linear load with (a) frame transformation method and (b) general transformation method for reference generation.

and compared: (a) with frame transformation method (b) with the general transformation method and $G_c(s)$ compensates at 100 Hz (c) with the general transformation method and $G_c(s)$ compensates at 100 Hz and 200 Hz. For comparison fairness, the DC side capacitance C_{dc} in an H-bridge is selected to be equal to the total capacitance used in the active-filter-integrated AC/DC rectifier, that is, $C_{dc} = 2C_f$. Evidently in Fig. 19, all three active-filter-integrated converters perform significant reduction in DC voltage ripple as compared with the H-bridge converter, even though the total capacitance used are the same. From Fig. 19(a) and (b), it is shown that the DC ripple has been mitigated from 10.2% (26.5 V) with the H-bridge to 1.9% (5 V) with the active-filter-integrated converter using frame transformation method. The waveforms are also plotted in the FFT domain, which shows a significant suppression of the 100 Hz ripple content. The waveforms in Fig. 19(b) and (c) indicate that both reference generation methods can compensate the 100 Hz ripple effectively. Nevertheless, the ripple can be further reduced in Fig. 19(d) to merely 1.1% (3.0 V) by using the general transformation method

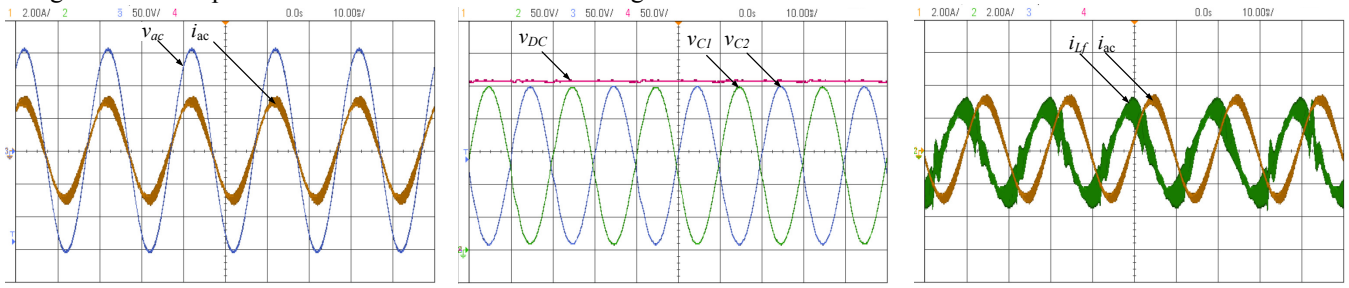
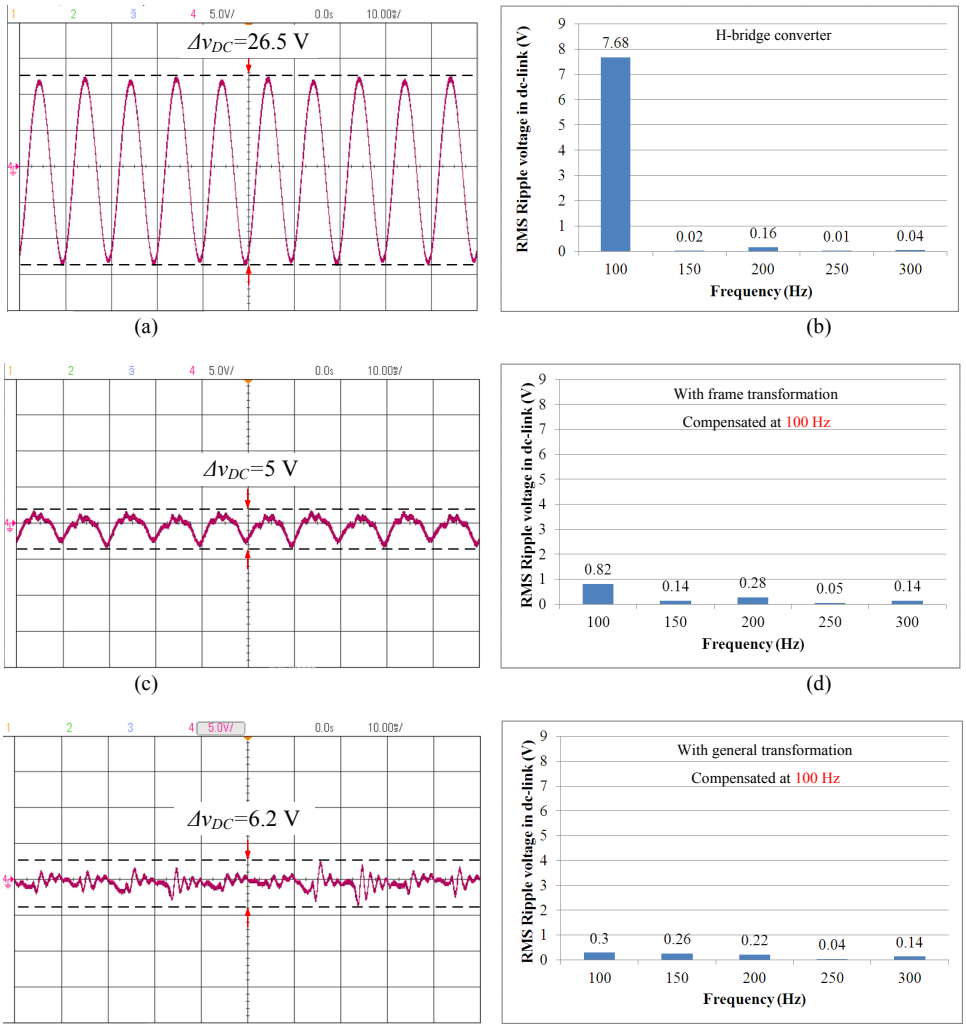


Fig. 18. Experimental results of the steady-state operation waveforms for an active-filter-integrated AC/DC rectifier with v_{ac}=110 V.



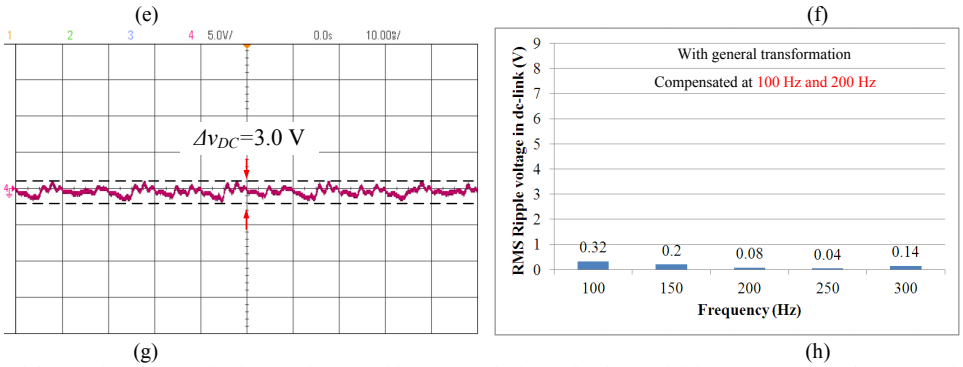


Fig. 19. A comparison of the steady-state DC ripple waveforms and its FFT analysis result of (a) H-bridge converter; (b) the FFT analysis results from (a); (c) the active-filter-integrated converter using frame transformation and G_c(s) compensates at 100 Hz; (d) the FFT analysis results from (c); (e) the active-filter-integrated converter using general transformation and G_c(s) compensates at 100 Hz; (f) the FFT analysis results from (e); (g) the active-filter-integrated converter using general transformation and G_c(s) compensates at 100 Hz and 200 Hz; (h) FFT analysis results from (g).

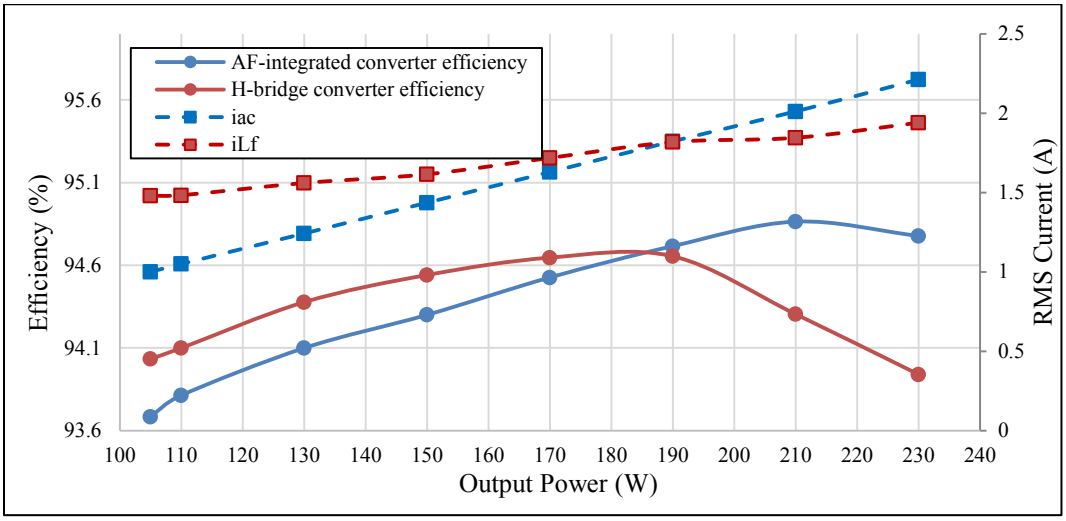


Fig. 20. A comparison of the efficiency performance between an H-bridge and the active-filter integrated converter at different output power.

compensating at 100 Hz and 200 Hz. To achieve the same ripple voltage performance, the H-bridge converter will require approximately 900 μF C_{dc} at DC side [1], whereas with the active-filter-integrated converter, the total capacitance is merely 100 μF. Hence, the required capacitance is reduced 9 times. The result is consistent with (33), which predicts a 10.8 times capacitance reduction given that Δv_{DC} = 3 V and V_{DC}=260 V.

Besides ripple reduction, the active-filter-integrated converter also possesses other merits over an H-bridge converter. Fig. 20 and Fig. 21 give a comparison of the efficiency (the power for gate drive and controllers are not included), THD and power factor performance of the two topologies from 50% load (105 W) to 110% load (230 W). The measured power for gate drive and controllers are around 3.9 W, which accounts for approximately 1.85% loss of rate power. In Fig. 20, the efficiency curves are plotted against the measured RMS inductor currents of i_{Lf} and i_{ac} of the active-filter-integrated converter. Compared with the H-bridge converter, the active-filter-integrated converter has a higher efficiency at a power level higher than 187 W, which is similar to the calculation results of 190 W given in Section VI. At full-load condition, the active-filter-integrated converter can offer a 0.84% efficiency improvement, due to the reduced power losses of L_2 and V-phase. On the other hand, at low power level, the active-filter-integrated converter achieves a maximum of 0.35% lower efficiency at the half load, which is almost negligible. Note that the DC power at the point of intersection in the efficiency curves is consistent with that in the RMS current curves of i_{Lf} and i_{ac}. It must be emphasized that the obtained results are in contrast to all existing methods in which the active filter stage is simply an add-on to the H-bridge converter, thereby leading to an inevitable drop of the efficiency for all load conditions by at least few percentage [31], [32]. For this reason, it can be concluded that the active-filter integration serves not only to reduce overall cost and system complexity, but it can also help to improve the efficiency performance. The efficiency of the converter can be further improved if better switches and inductor design are adopted.

Meanwhile, the THD of the line current as shown in Fig. 21 is reduced in the active-filter-integrated converter. This is because the double-line frequency ripple at the DC output which introduces a 3rd harmonic component into the line current [5] is effectively mitigated by the active-filter-integrated converter.

Finally, Fig. 22 and Fig. 23 show the transient performance of the active-filter-integrated converter under load changes and input voltage variations. In Fig. 22, a comparison is made between the H-bridge converter and the active-filter-integrated converter for a step-load change from full load to 70% load, and back to full load. It can be seen that the active-filter-integrated converter has similar DC output responses as that of an H-bridge converter in terms of overshoot, undershoot and settling time. This implies that the power decoupling control loop has little effect over the PFC control loop, and will not deteriorate the system stability. Fig. 23 shows the transient waveforms of the active-filter-integrated converter with a step change of the input voltage from the rated value to 110%/90% of the rated value and back to the rated value. In both scenarios, the undershoot/ overshoot remains below 3.8% (10 V) of v_{DC}. The undershoot/ overshoot in Fig. 22 and Fig. 23 can be further improved. A undershoot/overshoot is the result of transient power imbalance of input and output power. According to (24), when the input power p_{AC} or the load R changes, the dynamics of v_{DC} is influenced by the decoupled power p_c and the equivalent capacitance C_e. Since the major objective of the active filter in this paper is to decouple the double-line frequency ripple power, the undershoot/ overshoot depends solely on the value of C_e. Assuming that the transient imbalanced energy is ΔE_{tran}, and that all of the

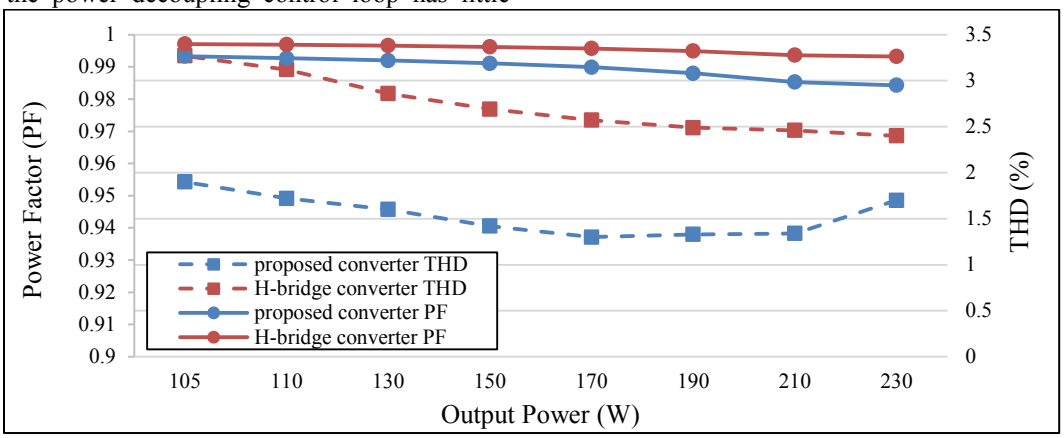


Fig. 21. A comparison of the power factor and THD performance between an H-bridge and the active-filter integrated converter at different output power.

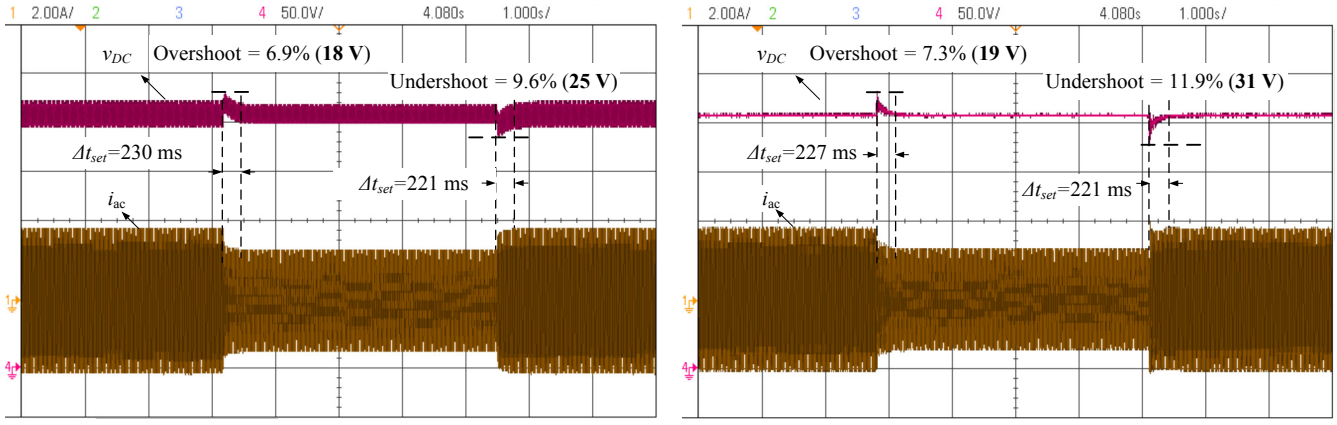


Fig. 22. A comparison of the transient response to step load change between an H-bridge and the active-filter integrated converter.

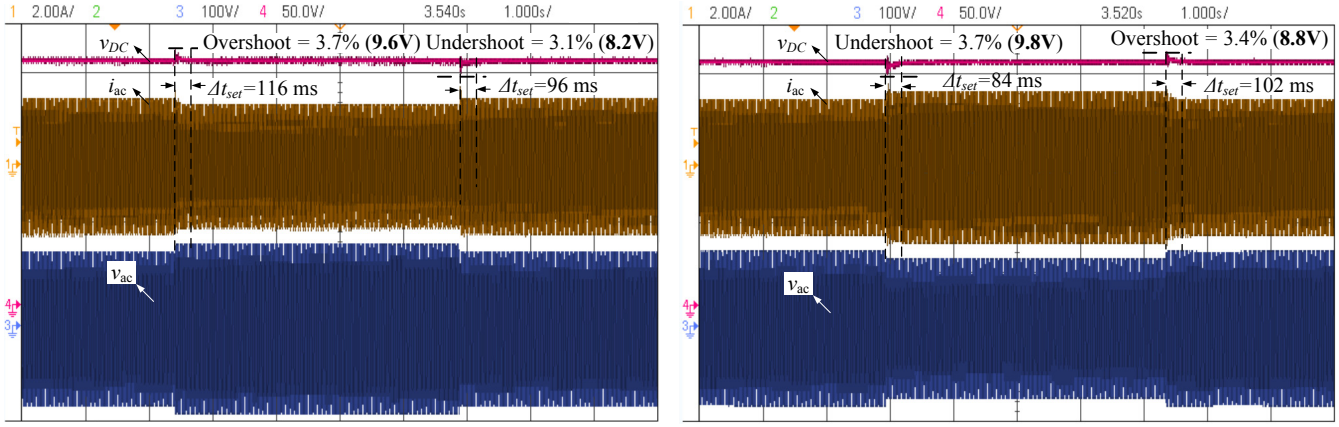


Fig. 23. Transient response of the active-filter integrated converter operating with a step input voltage change.

energy is absorbed by C_e. It is easy to conclude that the voltage ripples are $\Delta v_{DC} = \sqrt{\frac{4\Delta E_{tran}}{C_e} + V_{DC}} - V_{DC}$. Therefore, a larger C_e will lead to a smaller voltage ripples at DC output. However, it should be noted that, by improving the control, the active filter has the potential to decouple the transient imbalanced power, such that C_e can remain relative small. This work is open for future research.

CONCLUSIONS

In this paper, a concept of active-filter integration for a single-phase AC/DC converter is proposed. In the example of an H-bridge converter, the active filter is integrated with the switching actions of the switches in the H-bridge converter to eliminate the need for additional switch. This integration reduces system cost, increases power density and may lead to improved efficiency. Additionally, two methods of reference generation are proposed for the control of this converter. Unlike those used in conventional approaches, these two control methods do not require the knowledge of instantaneous input power, exact system parameters, power losses and the power stored in the passive components. They are closed-loop control methods that require only the voltage-ripple information. Hence, they are simple to implement. Both simulation and experiment results have verified the practicality of the proposed topology and control methods.

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