Development and Evaluation of Silicon Drift Chambers

by

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ABSTRACT

This thesis presents results on silicon drift chambers, which are new detectors based on the idea of electrons drifting along a potential minimum in a fully depleted silicon wafer. Emphasis is placed on the following: (i) fabrication of the devices which was carried out at Micron Semiconductor Ltd., (ii) laboratory tests of the behaviour of the detectors, in particular their DC characteristics and their response to minimum ionising β particles and (iii) computer modelling of the potential distribution and motion of charge carriers within the detector.

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Chapter I

INTRODUCTION

Silicon detectors have found widespread use in several branches of physics in the past and due to the recent advances in fabrication technology they are becoming increasingly more adaptable to many other uses. There are several desirable properties of silicon (and germanium) detectors which make them suitable for radiation detection applications. One obvious property is that silicon detectors are solid-state detectors and in some uses this is a great advantage. This means that for the detection of high energy particles the detector size can be kept small compared to an equivalent gas-filled detector because of the much higher density of silicon. Another great advantage of silicon as a detection medium is the relatively small amount of energy required to produce an electrical signal in the detector. The amount of energy needed to produce one elecron-hole pair in silicon is 3.62 eV. This can be compared to the energy required to produce one photoelectron in a plastic scintillator detector which is of the order of 1000 eV, or the energy needed to produce one electron-ion pair in a gas-filled detector which is approximately 30 eV. The fact that this energy is so low in silicon is a direct consequence of the fact that silicon is a semiconductor and therefore has a very narrow bandgap energy. This means that the number of carriers produced in a typical radiation interaction is much higher in

silicon detectors and so means that the statistical fluctuation in the signal is very low.

Other advantages include the fast charge collection time (typically 20 nsec) and hence good timing characteristics and the compact size of the detector. The disadvantages of silicon detectors include their degradation due to radiation-induced damage and the limitation to small detection areas. All these points will be discussed in subsequent chapters.

In principle, one could construct a silicon detector by simply applying an electric field across a crystal of pure silicon. Then, radiation incident on the crystal would generate electron-hole pairs which would separate and be swept away to opposite contacts by the electric field. This would constitute a signal in the detector. However, in practice, the steady-state leakage currents observed in such a detector would be too high to allow detection of the incident particles or radiation. This leakage current can be reduced to desirable levels by using a crystal of silicon on which a diode is fabricated and, indeed, the diode has formed the basis of semiconductor detectors up to this day.

Because recent semiconductors utilise a pn junction, their fabrication technology has benefitted greatly from the microelectronics industry. One type of detector can be made using the diffusion process. A crystal of, say, n-type silicon is exposed to a gaseous dopant of p-type impurity (e.g. boron) in a diffusion furnace. This produces a thin region of p-type material near the surface and a pn junction is formed, typically 0.1-2.0 μm below the surface. The

opposite surface is treated similarly with an n-type dopant (e.g. phosphorus) to produce an ohmic contact. When a reverse bias voltage is applied (p-type negative with respect to n-type) to the detector a 'depletion region' (containing essentially no free charge carriers) extends from the p-type surface into the bulk of the detector. This depletion region, which increases in thickness as the bias voltage increases, constitutes the active volume of the detector. The limits on thickness are set by the breakdown voltage of the junction and is about 1-2 mm for high resistivity silicon.

A second type of detector is the surface barrier detector which is based on the rectifying junction produced when certian metals are in contact with a semiconductor. The physics of this structure was first described by Schottky's model of the metal-semiconductor contact [1]. Fabrication is achieved by first etching the surface and then evaporating a thin gold film onto this surface. The evaporation is usually carried out under conditions which promote slight oxidation of the surface. It has been shown that this oxide is important in the formation of the surface barrier. Surface barrier detectors have the advantage that they can be made with extremely thin dead windows but they are also particularly sensitive to surface contamination and damage which can dramatically degrade their performance.

Although these types of detectors were used for the detection of radiation it was realised that they suffered from several problems which limited the signal-to-noise ratio. A major problem is that such detectors are susceptible to changes in the surface conditions. The fact that the surface of a semiconductor can drastically affect the

properties of semiconductor devices will be discussed later, but, for example, the introduction of a large number of surface states by contamination or damage can lead to an increase in the leakage current of a silicon detector. Several methods were proposed to reduce this problem including hermetically sealed devices, edge protection using doped epoxies and the use of guard rings. However the most successful method and the one which is used in most modern detectors is oxide passivation in which the silicon surface is passivated by a thermally grown oxide. This is used in conjunction with the so-called planar technology in which the oxide also serves as a mask against impurities thereby defining the pattern of the detector junction diodes. All the detectors fabricated for this work were of this type and the impurity dopants were introduced into the silicon by ion implantation. In this method the oxide-masked silicon is exposed to a beam of monoenergetic ions produced by an accelerator which have a well defined range in the silicon. This method allows the control of both the concentration profile of impurities, by adjustment of the incident beam energy, and the total dose of implanted ions. After implantation the silicon wafers must be annealed at a moderate temperature which serves to electrically activate the dopant ions and to reduce the radiation damage caused by the incident ions. In general, because ion implantation is a moderately low temperature process, high minority carrier lifetimes can be achieved.

Figure 1 shows a schematic cross-section through a typical ion-implanted detector. The particular detector depicted has a single active area (i.e. the implanted area) but detectors are by no means

limited to this design - in reality almost any geometry is possible. The detector can be fabricated on a wafer of silicon of high resistivity (1-20 kΩcm) which in this case is n-type silicon. The main features are the thermally-grown oxide which is usually between 0.5-1.0 μm thick and serves as an implantation mask and to passivate the surface, a thin layer of implanted p-type impurites forming the pn junction and a thin layer of implanted n-type impurites forming an ohmic contact on the back surface. Contacts are made via the thin layer (approximately 1.0 μm) of aluminium which covers some or all of the implanted areas on both surfaces.

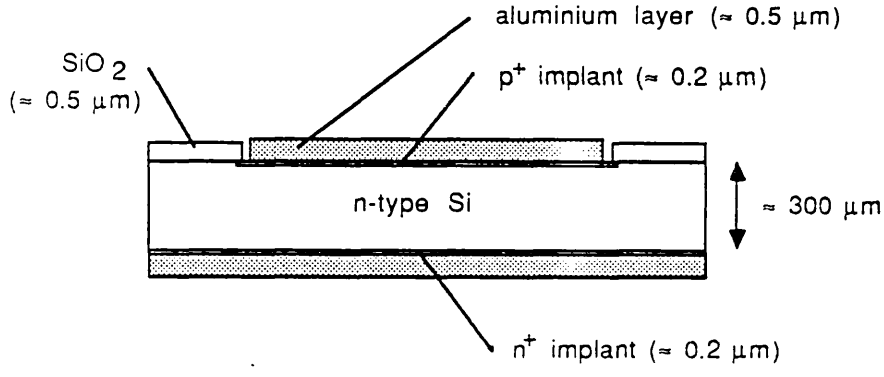


Figure 1: Cross-section through a typical ion implanted detector

Also, associated with the oxide and oxide-silicon interface, are several types of charge centres which may influence the electrical characteristics of the detector if present in high concentrations. In most circumstances it is desirable to have low concentrations of oxide charges to achieve low leakage currents and high breakdown voltages

and this provides another important constraint on the manufacturing process.

1.1 APPLICATIONS OF SEMICONDUCTOR DETECTORS

1.1.1 Nuclear Physics

Silicon detectors are employed in nuclear physics for the spectroscopy of alpha particles, fission fragments and other heavy ions. Silicon surface barrier devices are excellent detectors of alpha particles. Their performance can be gauged by analysing the pulse height spectrum resulting when a source of monoenergetic alpha particles is incident on the detector. The most common source is alpha particles of energy 5.49 MeV emmited from Am^{241} and the pulse height spectrum has a full width at half maximum (FWHM) which is a measure of the energy resolution of the detector. This is true, of course, only if the broadening of the peak due to electronic noise is small compared to the inherent resolution of the detector itself. In practice, for Am^{241} α particles, this is the case and a typical value of the FWHM is about 20 keV although detectors are available with resolutions down to approximately 12 keV FWHM.

Silicon detectors are also suited to fission fragment spectroscopy (and heavy ion spectroscopy) although their response to such particles is more complicated. For heavily ionising fission fragments it is well established that a pulse height defect (PHD), or apparent loss of energy measured in the detector compared to the true energy, is observed. The pulse height for heavy ions is less than that observed for light ions (e.g. αs) of the same energy and this PHD has been

attributed to three different phenomena: (i) the more heavily ionising ions deposit more of their energy in the insensitive entrance windows; (ii) the increased energy loss of the low velocity heavy ions due to nuclear collisions; and (iii) recombination of electron-hole pairs in the dense plasma created along the track of the heavily ionising particles. Measurements of the pulse height defect for surface barriers show that a value of 15 MeV for the defect is possible when fission fragments of average energy of about 80 MeV are used [2]. A further consideration is that radiation damage caused by prolonged exposure to heavy ions or fission fragments can result in rapid deterioration of the performance of the silicon detectors.

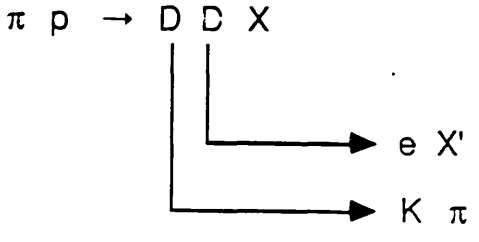
As well as energy measurements, silicon detectors are also widely used for particle identification via measurements of the specific energy loss dE/dx. In such applications the device is often called a 'dE-detector'. For this purpose a detector which is thin compared to the range of the incident particle is required and the thickness has to be made as uniform as possible. The superior energy resolution of silicon detectors is again an advantage in dE-detectors.

1.1.2 High Energy Physics

In high energy physics (HEP), the discovery of charmed particles [3] in 1974 provided the impetus for a great effort towards the development of vertex detectors. Many of these charmed particles were found to have lifetimes in the region 10^{-13} to 10^{-12} sec so that they may travel ~ 1 mm from their production point in a HEP experiment before they decay. Charmed mesons were first observed

as effective mass peaks in e^+e^- annihilation experiments. However, fixed target experiments at Fermilab and at the CERN SPS were unable to detect the presence of the charmed particle resonances in their effective mass plots due to overwhelming combinatorial backgrounds. Meanwhile individual charm decays began to be observed by experiments using vertex detectors - nuclear emulsions or special purpose bubble chambers were used, resulting in events where secondary vertices ~ 100 μm from the interaction vertex were clearly seen.

Despite their high precision nuclear emulsions and bubble chambers have very limiting disadvantages such as their inability to provide an on-line trigger and problems with low data taking rates. This led to a concerted effort to develop silicon vertex detectors with the necessary spatial resolution and an excellent example of the use of such a detector is provided by the NA11 experiment at the CERN SPS. This group, a collaboration from Amsterdam, Bristol, CERN, Cracow, Max Planck Institute, Munich and the Rutherford Laboratory, (ACCMOR), has studied the hadronic production of charmed particles in a beryllium target. The experiment relied on a single-electron trigger to enrich the charm content of the data. This consisted of triggering on the semi-leptonic decay of one of the pair-produced charm particles, and also to see the hadronic decay of the other in their detectors.



However, even with this enriched charm sample, the data from NA11 only showed the $D^{\pm}$ and $\overset{(-)}{D}{}^{0}$ signals as small effects on large backgrounds.

The ACCMOR collaboration then decided to improve the experiment by adding a silicon vertex detector downstream of the beryllium target. Using this detector system, particles consistent with a displaced secondary vertex could be identified. The result was that most events (i.e. events in which all the particles emerged from the primary vertex) could be rejected and many tracks from the remaining events could also be rejected. With this method combinatorial background levels were drastically reduced which enabled the observation of clear charm signals with very little background. It also enabled measurements of the lifetimes of the charmed particles to be made.

The NA11 vertex detector consisted of six planes of silicon microstrip detectors, each detector having an active area of 24×36 mm^2 with 1,200 parallel diode strips. The strip pitch was dictated by the typical average impact parameter which is of the order $c\tau$ (where τ is the particle lifetime), i.e. about 60-300 um. The strip pitch was 20 μm but to overcome fanout problems and to limit the amount of electronics, only 240 strips were read out from each plane. Capacitive charge division was used so that the readout strips could see signals from the passage of a particle between them, determined by the inter-strip and strip-to-substrate capacitances. This resulted in a precision on the impact parameter of typically 15 μm.

The NA11 experiment and other charm investigations such as the NA14 charm photoproduction experiment have shown that semiconductor vertex detectors are very successful tools for the recognition of particles which give rise to a secondary vertex as in charm decay. In the past decade a succession of particles (the τ lepton and hadrons such as $D, F, \Lambda_c, B, \ldots$) have been discovered which have lifetimes in the range 10^{-13}-10^{-12} sec. It is therefore foreseen that silicon vertex detectors will continue to find applications in high energy physics experiments of the future. One such application may be in the case of Z^0-production at SLC or LEP. The Z^0 will decay via all kinematically allowed $q\bar{q}$ final states including the higher flavours. The subsequent heavy quark decays involve a large release of energy with many charged particles usually being produced and decays such as $D \longrightarrow K\pi$ will be hidden in the combinatorial background. Silicon microstrips can be employed here to recognise the K and π tracks not coming from the primary vertex. Another possibility is the production of the Higgs boson which, as yet, has never been detected. A likely production mode is $Z^0 \longrightarrow H^0\, l^+\, l^-$ which would result in two jets due to the decay of the Higgs to $b\bar{b}$ or higher flavours. The large backgrounds caused by leptons from semi-leptonic decays of bottom and charm particles may well swamp the small number (~ 100) of Higgs events expected. Using a vertex detector these leptons could be identified as coming from a secondary vertex and therefore vetoed. In this way the prompt origin of each lepton can be identified providing a powerful method of background rejection.

1.2 OTHER USES OF SILICON DETECTORS IN HIGH ENERGY PHYSICS

1.2.1 Charge Coupled Devices

Charge coupled devices (CCDs) were invented in 1970 at Bell Labs and have recently been adapted to charged particle detection in HEP. In general CCDs consist of a fine matrix of potential wells just below the surface of the silicon, typically 20 μm × 20 μm in area and approximately 10 μm in depth. The potential wells, created by a series of metal-oxide-semiconductor (MOS) structures, are called pixels and the devices are fabricated such that charges from each pixel can be transfered to adjacent pixels and finally to a charge amplifier. The beauty of CCDs is that they measure space points since, unlike microstrip detectors, they provide two-dimensional readout. A group at the Rutherford Laboratory [4] has shown that for the detection of minimum ionising particles these devices can achieve

- detection efficiency of (98 ± 2)%
- two-dimensional spatial accuracy of 4.3 μm × 6.1 μm
- two-particle resolution of 40 μm in space.

Due to the thin depletion layer of these devices, the above performance is not degraded significantly if particles traverse the detector at non perpendicular incidence. However, the small depletion depth of approximately 10 μm, yielding ~ 1000 charge carriers for minimum ionising particles, makes cooling of the devices and the front-end amplifier essential to achieve small leakage currents and low noise. Another disadvantage of CCDs is their relatively slow readout time of typically 50 msec.

1.2.2 Silicon Detectors as Sampling Devices in Calorimeters

The response of silicon detectors to charged particles is very well understood and the idea of using silicon as the active material for energy (and position) measurement in calorimeters has been recently proposed by Barbellini and Rancoita [5]. Silicon detectors could be well suited to this application since (i) they are compact due to high density and efficient conversion of deposited energy into charge carriers, (ii) they have no gain and are therefore very stable and (iii) they are insensitive to magnetic fields.

However, there are several unanswered questions, mainly concerned with the effects of radiation damage and the possible degradation of the energy resolution due to sampling fluctuations. In addition the feasibility of producing the large number of silicon detectors needed for a calorimeter in a typical HEP experiment at reasonable costs has not yet been proven.

1.2.3 Silicon Photodiodes for Scintillator Readout

The basic structure of a silicon photodiode is similar to the structure of a standard silicon particle detector, the differences arising from the fact that photons in the visible and ultraviolet region are absorbed within a very shallow layer near the surface of the silicon. Compared to other light-sensitive detectors such as photomultipliers, they offer several advantages:

- high quantum efficiency over a wide spectral range
- insensitivity to magnetic fields
- compactness
- stability of the device since there is no intrinsic amplification

The recent interest in silicon photodiodes has led to the availability of photodiodes of up to several cm^2 in area and with leakage currents of only a few nA, manufactured using the oxide-passivated ion implantation technology. The important characteristics of a photodiode in most HEP applications are the quantum efficiency, the reverse bias (dark) leakage current and the capacitance. The best devices available at present achieve capacitances of approximately 80-100 pF for 100 μm depletion depth at reverse currents of below 1 nA/cm^2. With amplifier shaping time constants of ~ 2 μsec the equivalent noise charge is around $\sigma \sim 400$ electrons. Since in many situations the light yield from a minimum ionising particle is expected to be of the order of a few thousand photons, the use of silicon photodiodes for scintillator readout is clearly feasible and their performance has been studied experimentally by G.Hall et. al. [6].

1.3 PRESENT STATUS AND RECENT DEVELOPMENTS

Silicon microstrip detectors are the most advanced high spatial resolution detectors which have been used by several groups [7] in HEP experiments. Microstrip detectors with parallel strips of diodes can be fabricated on 3-inch diameter silicon wafers resulting in an active area of up to 50×50 mm^2. For a high spatial resolution it is desirable to make the strip pitch small. The minimum strip pitch which has been used so far is 20 μm and the spatial resolution of such a detector has been measured with minimum ionising particles [8]. The measured position resolution for normal incidence of a

single particle onto the detector was measured to be 3 μm (this is close to the theoretical minimum of ~ 1 μm arising from spatial fluctuation of the ionisation due to delta electrons). To achieve this precision it was necessary to readout every strip of the detector for the measurement. Thus, to achieve a precision of 3 μm over an area of 50×50 mm^2, for example, would require 2,500 channels of electronics. This can be a major disadvantage in many situations for several reasons. Firstly the physical volume of the electronics can become very large compared to the size of the detector. There are also other problems: the high cost of the large amount of electronics; fanout difficulties and the detector-to-preamplifier interconnections; and the problem of heat dissipation in the electronics.

In order to widen the range of applications of microstrip detectors it is therefore desirable to reduce the amount of electronics needed to read out these devices. One method which has been devised is to use capacitive charge division where only every n^{th} strip is connected to readout electronics. Via the array of interstrip capacitances, the charge collection at intermediate strips induces charges on the readout strips which are inversely proportional to the distance between interpolation and readout strips. From this the position where a particle traversed the detector can be calculated. For uniform charge collection, the intermediate strips have to be kept at the same voltage as the readout strips. This can be realised by sputtering a strip of amorphous silicon over the detector. The resistance between adjacent strips is then > 1 MΩ which, combined with a low leakage current of ~ 1 nA, results in a uniform voltage on

each strip. Detectors with a 20 μm pitch and readout pitches of 60, 120 and 240 μm (i.e. n= 3, 6 and 12) using capacitive charge division have achieved resolutions given in table 1.

n	Readout pitch	Measured spatial resolution
3	60μm	4.5μm
6	120μm	7.8μm
12	240μm	20.0μm

TABLE 1

Spatial resolutions of silicon microstrip detectors

with capacitive charge division read out.

Capacitive charge division has two main disadvantages: (a) The summed pulse height measured by the two readout channels nearest to the passage of the particle depends on the position of the particle. This is due to the capacitive coupling of the interpolation strips to ground. The loss of pulse height means that (i) the detectors are not suited to pulse height measurements and (ii) the spatial resolution is worsened; (b) also due to capacitive coupling, charges are induced in the strips beyond the two readout strips nearest to the passage of the particle. This significantly worsens the two-particle resolution of the detector.

Future HEP experiments, for example at SLC, LEP and TEVATRON, will require silicon vertex detectors to have small pitch

and small readout pitch (<20 μm) and at the same time cover larger areas. Thus large numbers of readout electronics must be accomodated in relatively small areas in the vicinity of the detectors. With this in mind, there has been considerable effort in the past few years to achieve a high density of readout electronics for silicon detectors, or to reduce the amount of electronics required. There have been essentially two main developments in this area.

The first approach is the use of large scale integration (LSI) technology. Two projects are under way to develop an LSI readout chip incorporating (i) a low noise charge sensitive preamplifier and (ii) a multiplexer to switch many channels onto a single output line [9]. The first results have been obtained by the CERN-Hawaii University- Stanford University group using an LSI chip to readout a 25 μm pitch microstrip detector fabricated by Micron Semiconductor Ltd. The MICROPLEX chip has been developed for a high resolution microvertex detector for the DELPHI experiment at LEP and for a similar detector for MARK II at SLC. The chip contains 128 readout channels of charge sensitive preamplifiers with serial readout from all 128 channels controlled by a shift register. The chip is ~ 6 mm × 6 mm in size. With this chip, readout speeds of several MHz are possible and the results of experimental tests indicate that the electronic noise was σ ~ 1600 electrons, comparable with the noise obtainable with conventional readout electronics on the same detector.

The second approach is the development of a new type of detector called the silicon drift chamber (SDC). The idea of the SDC was first proposed by E.Gatti and P.Rehak [10] and later demonstrated

by them and J.Walton. The SDC operates by collecting electrons at an anode after they have drifted up to several mm along a fully depleted detector so that a relatively large detection area can be read out by a single channel of electronics connected to the anode. The position of the generation of charge carriers in the detector by an incident ionising particle can then be deduced by the drift time of these charge carriers (electrons). Prototype SDCs have also been built by a Micron-Imperial College collaboration and tested at Imperial College and the results will be presented in subsequent chapters.

Chapter II

THEORY OF SILICON DETECTORS

2.1 BAND THEORY OF SOLIDS

In a solid the atoms are close enough together for the electric fields from one atom to interact with the electrons in another atom. As a consequence the energy levels merge into a series of bands in which the levels are so close together as to be essentially continuous. This concept, which is described by quantum mechanics, is vital in classifying materials into insulators, conductors or semiconductors.

As depicted in figure 2 (a), insulators are characterised by band gaps which are very large compared to kT at room temperature (approximately 0.025eV). For example silicon dioxide, which is a very important insulator in silicon device technology, has a band gap of 9eV. In such materials only the quantum states in the valence band are filled with electrons and therefore if an electric field is applied these electrons cannot increase their kinetic energy sufficiently and so no net current flows. Only if the field was excessively strong (around 10^7-10^8 V/cm), forcing electrons into the conduction band, would a net motion of electrons be allowed. In metals, figure 2 (b), the band gap is small, or the valence and conduction bands actually overlap, so that valence electrons are free to gain energy from very small applied fields because of the empty quantum states above the valence states.

In semiconductors, figure 2 (c), the band gap is sufficiently small that some electrons can have enough thermal energy imparted to them to be promoted to empty states in the conduction band. Semiconductors therefore have conductivities intermediate between metals and insulators.

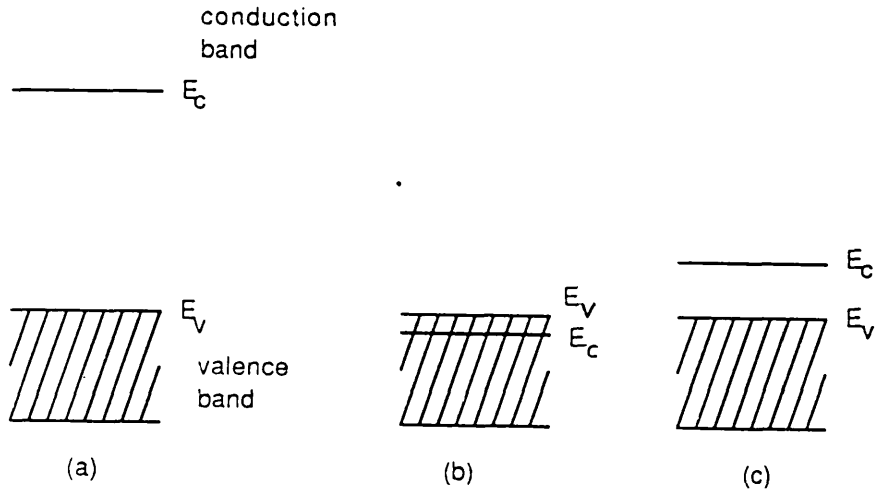


Figure 2: Energy level diagrams for solids
(a) Insulator, (b) metal and (c) semiconductor.

2.2 CONDUCTION IN INTRINSIC AND EXTRINSIC SILICON

In pure or intrinsic silicon the band gap is approximately 1.1 eV at room temperature which results in a very low conductivity. To estimate the concentration of electrons in the conduction band it is necessary to know the form of the Fermi-Dirac function which expresses the probability that a state of energy E is filled by an electron,

$$F(E) = \frac{1}{1 + e^{(E-E_f)/kT}} \qquad (2.1)$$

where E_f is called the Fermi level and is the energy level for which the occupation probability is 0.5. The concentration of electrons in the conduction band is given by F.G where G(E) is the density of states in the silicon. The empty states left in the valence band are called holes and these also act as charge carriers. This can be visualised as the movement of a hole or electron vacancy in response to an applied field due to the repopulation of states in the valence band. The concentration of holes in the valence band is given by (1-F)×G. Figure 3 shows the form of F(E) and G(E) together with the resultant charge carrier distributions. In intrinsic silicon the Fermi level is approximately at the middle of the band gap and the concentrations of electrons and holes are roughly equal. Although the properties of intrinsic silicon can be described theoretically, in practice it is virtually impossible to produce and the electrical properties of real semiconductors are determined by the small levels of residual impurities. In silicon device fabrication it is therefore very important to be able to control the amount and type of impurity atoms in the silicon.

Extrinsic silicon is achieved by doping, that is the addition of controlled amounts of specific impurity atoms with the express purpose of increasing either the electron or hole concentration. For example, phosphorus has five valence electrons compared with four for silicon. When present in small concentrations the phosphorus atom will occupy a substitutional site within the silicon lattice resulting in an extra electron after all four covalent bonds have been formed. At room temperature most of the extra phosphorus electrons

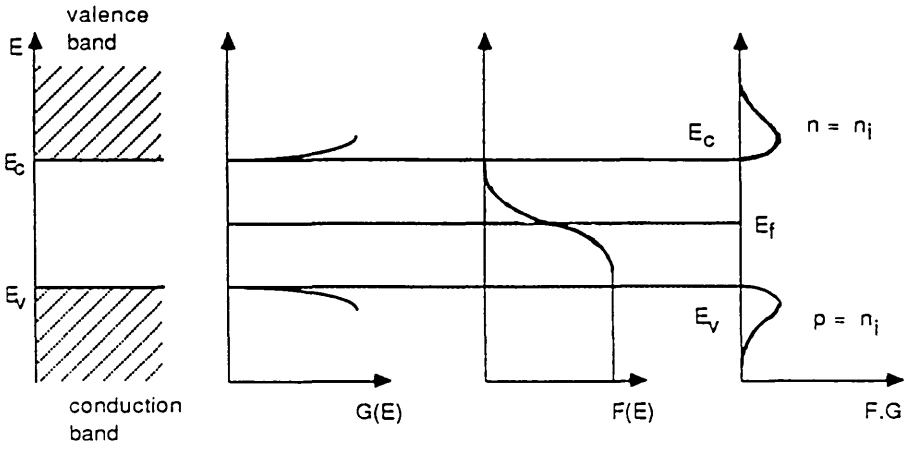


Figure 3: Intrinsic semiconductor at equilibrium
Schematic band diagram, density of states, Fermi-Dirac distribution and carrier concentrations.

are only lightly bound and are therefore available for conduction. This results in n-type extrinsic silicon. Conversely, boron has three valence electrons, leaving one vacant bond, easily filled by the movement of electrons. This is usually visualised as the inverse motion of the vacant bond or hole. This type of material with a high concentration of holes is called p-type.

For doped silicon an important quantity is the resistivity ρ which depends on the concentrations of free electrons and holes and on their mobilities. These are a function of temperature and of impurity concentration. The resistivity is given by

$$\rho = \frac{1}{e\,(\mu_n n + \mu_p p)} \qquad (2.2)$$

where e is the electron charge, n and p are the electron and hole concentrations and μ_n and μ_p are the electron and hole mobilities

respectively. In the fabrication of silicon detectors, for reasons which will become obvious, it is usual practice to use silicon of very high resistivity. Crystals of resistivity of up to approximately 20 kΩcm are commercially available [11], the upper limit being determined by the smallest doping concentrations which can be achieved. 20 kΩcm p-type silicon, for example, requires a doping concentration of 5×10^{11} acceptor atoms cm^{-3}, which is equivalent to one acceptor atom in 10^{11} in the silicon lattice. This presents a major challenge in both the crystal growing process and the subsequent steps in the fabrication of the detector.

The electron and hole concentrations in silicon, given by F.G and (1-F).G, can be calculated, yielding [12]

$$n = N_c\, e^{-(E_c-E_f)/kT}$$
$$p = N_v\, e^{-(E_f-E_v)/kT} \qquad (2.3)$$

for the electron and hole concentrations respectively. Here, N_c and N_v are the effective density of states in the conduction band and valence band respectively, E_c and E_v are the electron (hole) energy at the conduction (valence) band edge respectively and E_f is the Fermi level. Alternatively, these equations can be written in terms of the intrinsic carrier concentration n_i,

$$n = n_i \exp[(E_f-E_i)/kT]$$
$$p = n_i \exp[(E_i-E_f)/kT] \qquad (2.4)$$

where $E_i = \frac{1}{2}(E_c+E_v) + \frac{1}{2}kT\ \ln(N_v/N_c) \sim \frac{1}{2}(E_c+E_v)$ is the intrinsic Fermi level, which is very near to the middle of the band gap. This indicates that the deviation of a doped semiconductor from the

intrinsic material can be represented by the energy difference between the Fermi level and the intrinsic Fermi level. The above formulae become inaccurate when the semiconductor becomes degenerate (i.e. when the Fermi level comes close to the conduction or valence band edge to within ~ kT).

It is evident that for a semiconductor in equilibrium the product of the concentrations of electrons and holes remains constant i.e.

$$np = n_i^2 = N_c N_v e^{-E_G/kT}$$

$$\text{where } E_G = E_c - E_v \qquad (2.5)$$

2.3 THE PN JUNCTION

In an n-type semiconductor the Fermi level is close to E_c and the electron concentration is much greater than the hole concentration. In this case the electrons are called the majority carriers and the holes are called the minority carriers. In p-type semiconductors the Fermi level is close to E_v and the hole concentration is much larger than the electron concentration. The structure formed when n-type material is in contact with p-type material is known as the pn junction and forms the basis of most silicon particle detectors.

Pn junctions can be characterised by the spatial distribution of the dopant concentration across the junction and in this section a simple model - the step junction model - is invoked to predict some of the properties of real pn junctions. The model assumes a step function form of the dopant concentration as shown in figure 4 (a). On contact of the n-type silicon with the p-type, the charge carrier

concentration difference between the two regions causes electrons to diffuse into the electron-free p-region and holes to diffuse into the hole-free n-region and recombine. This produces a region of fixed positively charged donor ions on the right of the junction and a region of fixed negatively charged acceptor ions on the left. The charge imbalance in turn produces an electric field, which eventually counteracts the diffusion so that in equilibrium the net flow of carriers is zero. Once this condition is reached the Fermi levels in the two materials become equal. The charged region near the junction which has been depleted of free charge carriers is called the depletion region or space-charge region.

The characteristics of the space-charge region can be calculated using the depletion approximation in which it is assumed that it consists entirely of the charge of the ionised donors and acceptors. The energy band diagram is shown in figure 4 (b) and it is useful to define the Fermi potential

$$\phi = -(E_f - E_i)/e \qquad (2.6)$$

Thus ϕ is positive for p-type material and negative for n-type material. From (2.4)

$$\phi_n = -(kT/e) \ln (N_D/n_i)$$
$$\phi_p = (kT/e) \ln (N_A/n_i) \qquad (2.7)$$

The total potential variation across the junction is then

$$\phi_B = \phi_p - \phi_n = (kT/e) \ln (N_D N_A/n_i^2) \qquad (2.8)$$

This is called the built-in voltage of a pn junction.

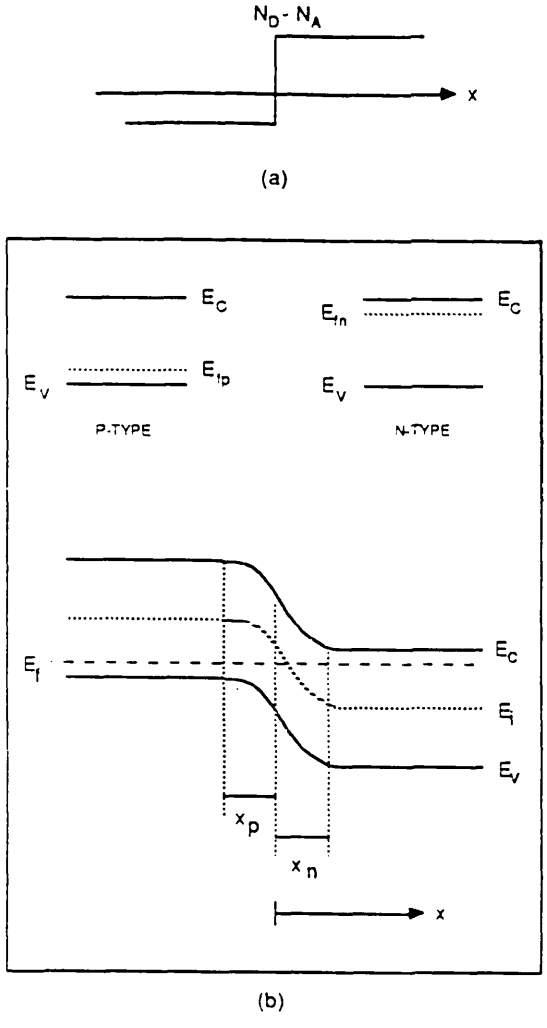


Figure 4: The step junction model
(a) Concentration of dopant atoms in the step junction.
(b) Energy level diagrams for p-type and n-type semiconductors and for a pn step junction.

The electric field E(x) and electric potential $\phi(x)$ can be obtained by solving Poisson's equation

$$\frac{d^2\phi}{dx^2} = -\rho(x)/\varepsilon_s \qquad (2.9)$$

where $\rho(x)$ is the charge density per unit volume, ε_s is the permittivity of silicon = $\varepsilon_o\varepsilon_r$, ε_o is the permittivity of free space and ε_r is the dielectric constant of silicon. With the charge density given by

$$\begin{aligned} \rho(x) &= + eN_D \qquad \text{for } 0 \leqslant x \leqslant x_n \\ &= - eN_A \qquad \text{for } -x_p \leqslant x \leqslant 0 \\ &= 0 \qquad\quad \text{in the bulk, i.e., } x < x_p \text{ and } x > x_n \end{aligned} \tag{2.10}$$

the solution for the field $E(x)$ is

$$\begin{aligned} E(x) &= - (eN_D/\varepsilon_s)\,(x_n - x) \quad \text{for } 0 \leqslant x \leqslant x_n \\ E(x) &= - (eN_A/\varepsilon_s)\,(x + x_p) \quad \text{for } -x_p \leqslant x \leqslant 0 \end{aligned} \tag{2.11}$$

The undepleted silicon on either side of the junction is field-free i.e. $E(x) = 0$. The form of $E(x)$ is shown in figure 5 (d). For continuity of the field at $x = 0$ it is seen that

$$N_A x_p = N_D x_n \tag{2.12}$$

Thus, to obtain deep depletion regions in silicon detectors the dopant concentration of the substrate is made very low, i.e. high resistivity silicon is used. By integration of (2.11) the electric potential is obtained

$$\begin{aligned} \phi(x) &= - \phi_n - (eN_D/2\varepsilon_s)\,(x_n - x)^2 \quad 0 \leqslant x \leqslant x_n \\ \phi(x) &= - \phi_p + (eN_A/2\varepsilon_s)\,(x + x_p)^2 \quad -x_p \leqslant x \leqslant 0 \end{aligned} \tag{2.13}$$

Imposing continuity of $\phi(x)$ at $x = 0$ implies that the total depletion width is given by

$$d = x_n + x_p = \{(2\varepsilon_s/e)\,\phi_B\,[(1/N_A) + (1/N_D)]\}^{1/2} \tag{2.14}$$

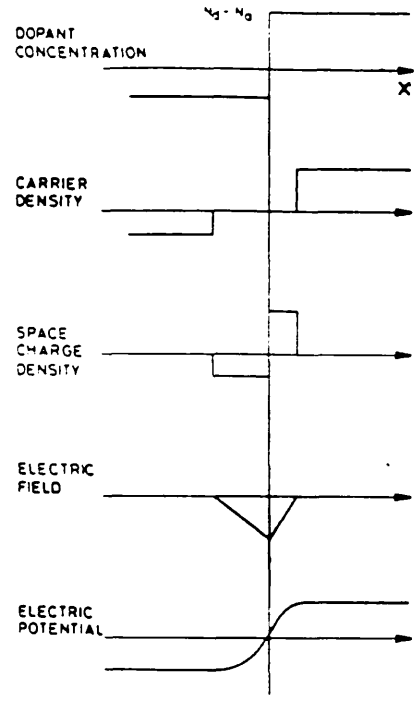


Figure 5: Properties of the step junction model (a) Dopant concentration, (b) carrier density, (c) space charge density, (d) electric field and (e) electric potential.

For a pn junction fabricated on high resistivity n-type material $N_D \ll N_A$ and so $x_p \sim 0$. In this case the depleted region extends into the n-type region of the detector and is given by

$$x_n \approx \{(2\varepsilon_s/e)\,\phi_B\,(1/N_D)\}^{1/2} \qquad (2.15)$$

The above results are summarised in figure 5.

2.4 THE REVERSE BIASED PN JUNCTION

With no external voltage applied, a silicon pn junction diode will function as a detector, but only with very poor performance. The built-in voltage ϕ_B across the junction is small so that the electric field is not large enough to make the charge carriers move very rapidly. In addition, since the depletion region is very narrow, the active detection volume is small. Also the junction capacitance ($\propto d^{-1}$) is high so the noise properties of such a detector when connected to the input stage of a preamplifier may be quite poor. For these reasons most pn junction detectors are used with an external voltage applied so that the junction becomes reversed biased.

The situation is then as shown in figure 6. The Fermi levels are displaced by an amount equal to the bias voltage. The n-bulk region is shifted downward by $-V_B$. The slope of the band edges in the depletion region has increased, reflecting the increase in electric field for reverse bias. Also there is an increase in potential difference across the junction - the applied voltage adds to the built-in voltage. This produces an increase in the barrier height for diffusion of majority carriers across the junction. Consequently the diffusion component of the current is reduced to less than its thermal equilibrium value. However, the drift current component of minority carriers down the potential hill remains approximately at its equilibrium value (small). Evidently there is a net current flowing within the diode, which is typically very small, referred to as the leakage current.

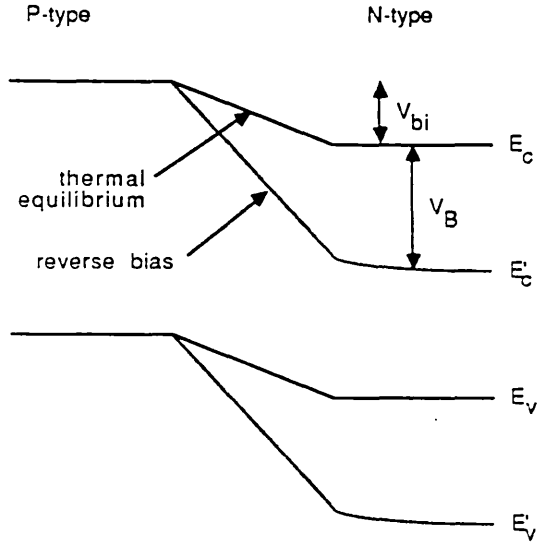


Figure 6: Energy level diagram for reverse bias at thermal equilibrium.

2.5 CONTRIBUTIONS TO THE LEAKAGE CURRENT

The reverse leakage current is the sum of several components which are all due to electron-hole (e-h) pairs generated somewhere in the semiconductor. Under equilibrium conditions electron-hole pairs are continually generated but they recombine giving rise to zero net current. Under reverse bias, e-h pairs, once generated, will be separated by the field and their probability of recombination is diminished. There are three main contributions to the leakage current:

(a) Generation within the depletion region - "generation current"

(b) Generation in the neutral regions - "diffusion current"

(c) Generation at surface states or conduction through surface channels at the edge of the device which I shall call the surface component of the current.

The generation of e-h pairs in the depletion region takes place via intermediate-level centres. These are energy states which have energy levels in the forbidden gap and are associated with impurities such as heavy metal ions and imperfections in the silicon lattice. Because the probability of transitions depends on the size of the step in energy, such states can increase the efficiency of the generation-recombination process, especially if the state is near the centre of the band gap [13].

The intermediate-level centres within the depletion region alternately emit electrons and holes and the rate of generation of e-h pairs is given by

$$U = - \frac{\sigma_p \sigma_n v_{th} N_t n_i}{\sigma_n e^{(E_t - E_i)/kT} + \sigma_p e^{(E_i - E_t)/kT}} \equiv - n_i/(2\tau_0) \qquad (2.16)$$

where N_t is the density of bulk generation-recombination centres with energy E_t, σ_n and σ_p are the electron and hole capture cross-sections respectively and v_{th} is the thermal velocity of carriers. τ_o is defined as the minority carrier lifetime within a reverse biased depletion region and is given by

$$\tau_0 = \frac{\sigma_n e^{(E_t - E_i)/kT} + \sigma_p e^{(E_i - E_t)/kT}}{2 \sigma_p \sigma_n v_{th} N_t} \qquad (2.17)$$

From (2.16) it can be seen that only those centres whose energy level E_t is near the intrinsic Fermi level E_i contribute significantly to the generation rate. The generation current is given by $I_g = q|U|dA$ or

$$I_g = (1/2)\, e\, (n_i/\tau_0)\, d\, A \qquad (2.18)$$

where d is the depletion region width and A is the junction area.

A second contribution to the leakage current is due to the generation of minority carriers in the undepleted region (within a diffusion length of the depletion region boundary) which diffuse into the depletion region and are swept away by the electric field there. The magnitude of the diffusion current can be calculated by solving the diffusion equation [14] and is given by

$$I_d = q\,A\,n_i^2\,\{[D_n/(N_A L_n)] + [D_p/(N_D L_p)]\} \qquad (2.19)$$

where D_n and D_p are the diffusion coefficients for electrons and holes respectively and L_n and L_p are the corresponding diffusion lengths. Since silicon detectors are usually operated in the fully depleted mode the diffusion current is essentially zero and can be neglected. A further contribution to the total leakage current is the surface component. To understand this component of the leakage current it is necessary to understand the effects of charges in the $Si\text{-}SiO_2$ system and a summary is given in section 3.2.5 and reference [15]. The two most important types of charge are the fixed oxide charge Q_f, which is usually positive and located in the oxide within ~ 30 Å of the $Si\text{-}SiO_2$ interface, and the interface trapped charges Q_{it} which have energy states in the forbidden gap and can interact electrically with the underlying silicon. The interface trapped charges act as intermediate centres for the generation process in much the same way as the bulk intermediate centres do. The surface leakage current arising from generation via the interface trapped charge can be calculated in a similar manner to the calculation of I_g and is given by [16]

$$I_s = (1/2)\,q\,A\,\pi\,\sigma\,v_{th}\,D_{it}\,kT\,n_i \qquad (2.20)$$

where it was assumed that $\sigma_n = \sigma_p = \sigma$. Here D_{it} is the surface state density per unit area per electron-Volt near the midpoint of the bandgap. The physical origin of the interface trapped charge is not understood but it is assumed that these states result from either defects in the structure of the interface region, or from impurities in this region, or both. Since I_s can completely dominate the total leakage current if the surface state density is high, suitable steps have to be taken in the processing of the silicon to minimise D_{it}. The techniques used are described in chapters 3 and 4.

Another factor which influences the surface leakage current is the oxide fixed charge Q_f. The effect of oxide fixed charge present in oxidised p-type silicon is depicted in figure 7.

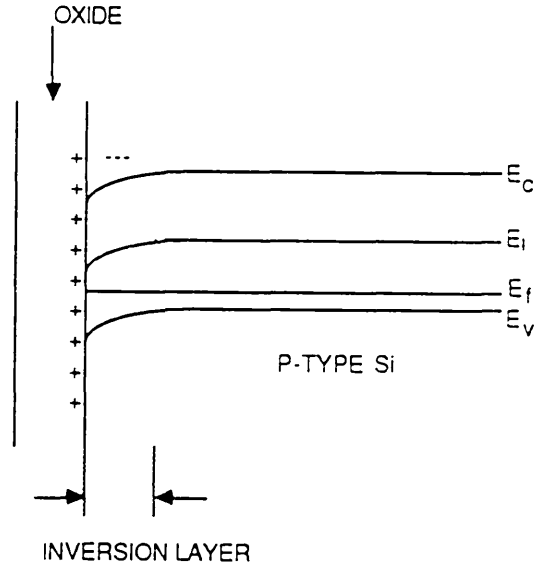


Figure 7: Band-bending due to oxide fixed charge at the surface of a p-type semiconductor.

The positive fixed charge Q_f must be compensated by an equal amount of negative charge within the bulk of the silicon, thus producing an inversion layer of electrons and causing the energy bands to bend downwards as shown. The charge values Q_f and Q_{it} determine how near the Fermi level at the silicon surface is to the midgap, where interface traps generate leakage current most efficiently. Thus for p-type silicon the band-bending resulting from the presence of fixed oxide charge causes the Fermi level to be closer to midgap resulting in an increased leakage current. For n-type silicon the opposite effect occurs.

Figure 8 shows the results of measurements of the leakage current for two ion-implanted n-type detectors of nominal area 1 cm^2. From this plot of leakage current versus reverse bias voltage it is evident that I_{leak} is approximately proportional to V^{α} (α = constant) but it does not follow exactly the $V^{\frac{1}{2}}$ dependence expected if the generation current I_g is the dominant component. This shows that either the surface component I_s or the diffusion component I_d or both have some contribution to the total leakage current.

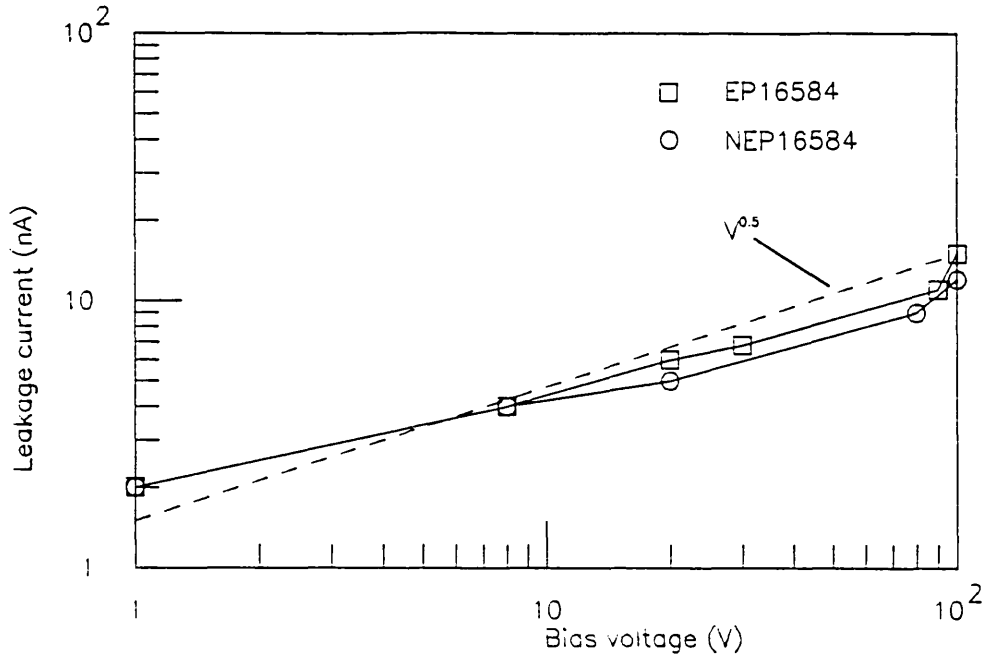


Figure 8: Leakage currents plotted against bias voltage for detectors EP-16584 and NEP-16584.

2.6 DEPLETION LAYER CAPACITANCE

A further important property of the reverse biased pn junction is its capacitance. The capacitance per unit area is defined as $C^{-1} = dV/dQ$, where dV is the incremental increase in voltage when a charge dQ is added. For the pn junction detector in reverse bias the capacitance is due to the depletion region and, for the step junction model, is given by [12]

$$C = \varepsilon_S/d = \sqrt{\{\varepsilon_S/[2\,\mu_n\,\rho\,(\phi_B + V)]\}} \approx \sqrt{\{\varepsilon_S/(2\,\mu_n\,\rho\,V)\}} \qquad (2.21)$$

Figure 9 shows the results of the measurements of the capacitance for two detectors, EP-16584 and NEP-16584. As the depletion region width increases the capacitance falls and reaches a constant value at

~ 80-90V when the detector is fully depleted. The proportionality of the capacitance to $V^{-0.46}$ is close to the theoretical value of $V^{-\frac{1}{2}}$ indicating that the step junction model is valid in this case. If C is plotted against $V^{-\frac{1}{2}}$ the slope of the line can be used to estimate the resistivity of the n-type silicon:

$\rho \sim 3720\ \Omega cm$ (NEP-16584)

$\rho \sim 4100\ \Omega cm$ (EP-16584)

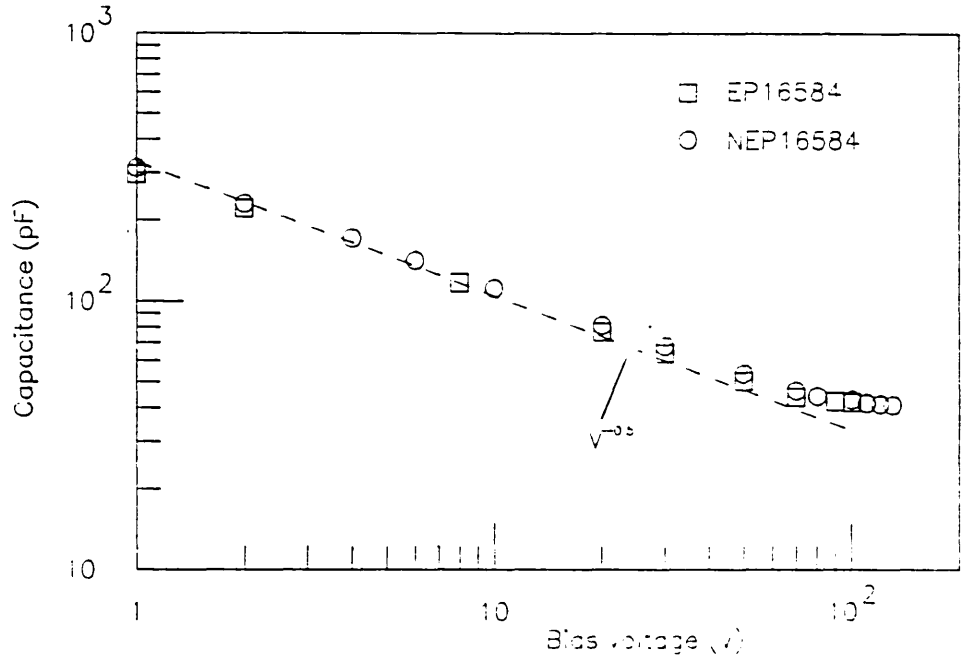


Figure 9: Capacitance characteristics of detectors EP-16584 and NEP-16584.

2.7 SILICON MICROSTRIP DETECTORS

Figure 10 shows the structure of a typical silicon microstrip detector. It consists of a fully depleted crystal of silicon with one surface subdivided into parallel p^+n diode strips with a pitch of typically 20-50 μm. The thickness of the detector depends on the particular application but for the detection of minimum ionising particles a thickness of ~ 300 μm is suitable. Making the detector thinner results in a lower signal-to-noise ratio since the energy loss of the incident particle is less. A suitable reverse bias voltage is applied across the wafer which serves to deplete the detector and to provide a collection field. A fast charged particle passing through the detector produces e-h pairs which drift towards the electrodes under the influence of the electric field. The motion of the charge carriers induces the signal in an external amplifier connected between the n^+ and p^+ contacts.

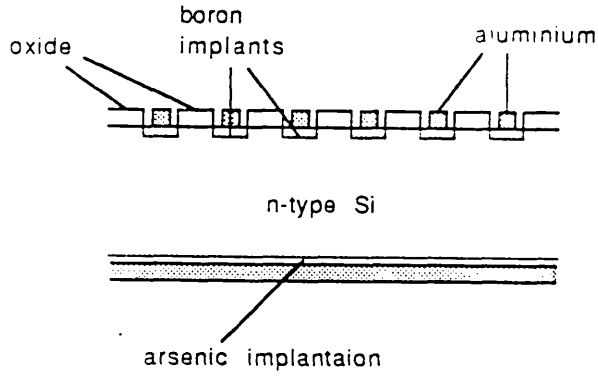


Figure 10: Cross-section through a microstrip detector

The form of the electric potential and electric field inside a silicon microstrip detector is shown in figure 11. These plots are based on the results of a computer simulation using the programs described in chapter 6. The simulation was done for a detector of thickness 300 μm, strip pitch 50 μm and resistivity 10 kΩcm. The electric field varies linearly with the distance and the potential is parabolic as expected on the basis of the step junction model.

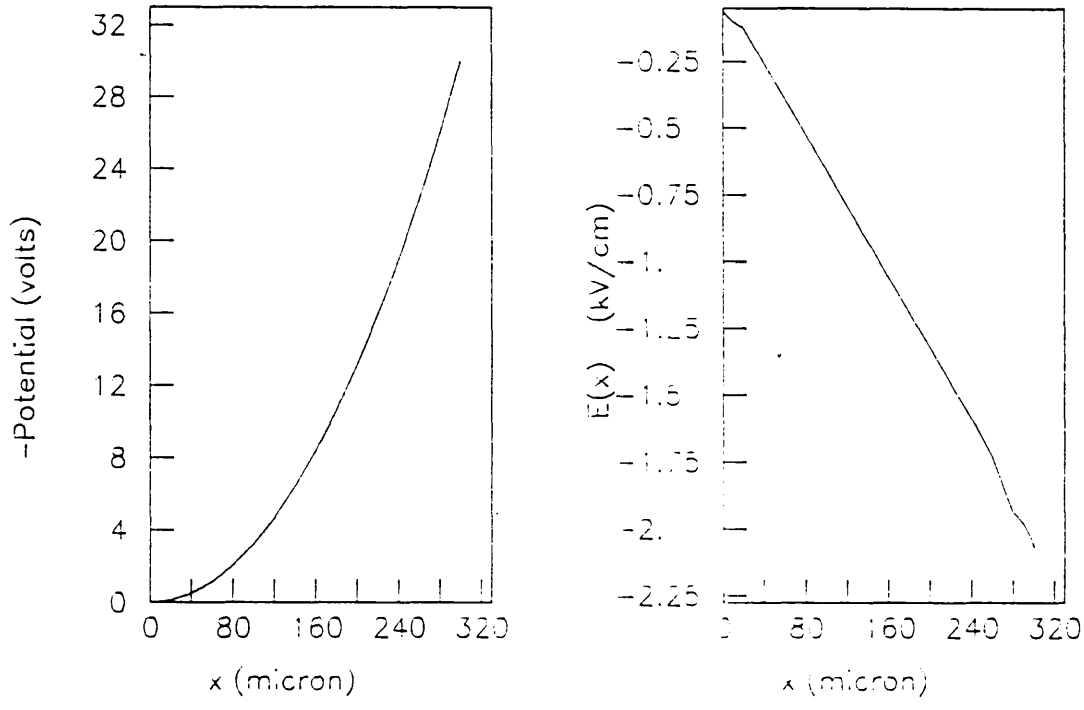


Figure 11: Electric field and potential in a microstrip detector

2.8 SILICON DRIFT CHAMBERS

The principle of the SDC was first described by E. Gatti and P. Rehak [10]. They were able to show that it is possible to fully deplete a thin, large area semiconductor wafer through a small contact somewhere at the edge of the wafer. After full depletion of the silicon wafer a second electric field can be superposed which serves to transport the charge carriers along the plane of the wafer to a collection electrode (the anode).

First consider the depletion of a standard n-type silicon detector. In figure 12 (a) the n^+ contact is shown at zero volts while a negative potential -V is applied to the p^+ contact. As the bias voltage is increased above 0 V the depletion region extends from the p^+ contact into the bulk as shown in figure 12 (b). The form of the potential is given by the solution to Poisson's equation and is parabolic as shown. The remainder of the silicon near the n^+ contact is a field-free undepleted region which acts as a conductor. Electrons and holes generated in the depletion region AB experience forces due to the electric field there, causing holes to be swept to the p^+ contact and electrons to be carried to the undepleted region.

As the bias voltage is increased further the depletion region extends further towards the n^+ contact and eventually the detector becomes fully depleted as shown in figure 12 (c). Neglecting the built-in voltage, the depletion condition is reached when the bias voltage reaches V_D where

$$V_D = \frac{d^2}{2 \varepsilon \mu_n \rho} \qquad (2.22)$$

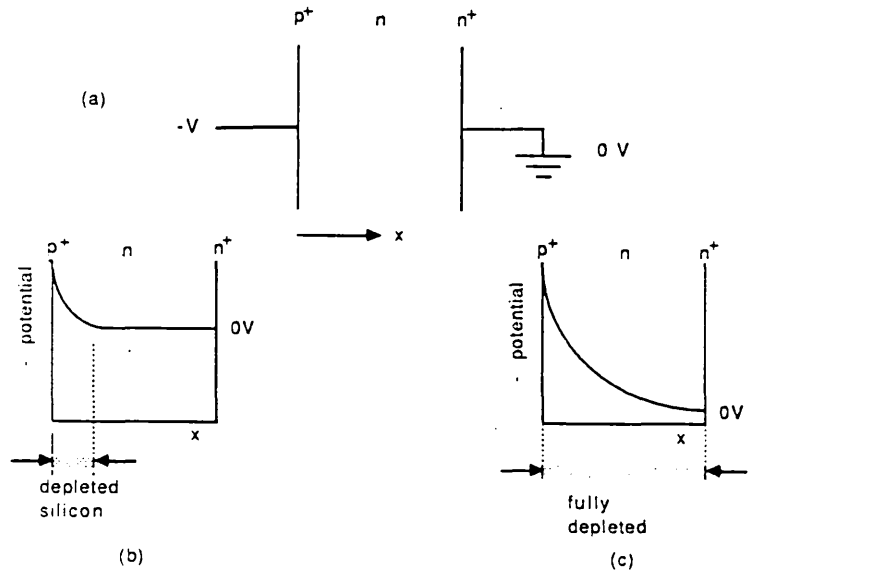


Figure 12: Depletion of a standard p^+n junction detector

Electron-hole pairs thermally generated in the detector are swept out of the depletion region by the action of the electric field - holes to the n^+ contact and electrons to the p^+ contact. Thus the fully depleted condition is stable.

Now consider two n-type silicon detectors placed parallel to each other such that the two n^+ electrodes are in contact as shown in figure 13 (a). If a small reverse bias is applied to both detectors, two depletion regions are formed at each p^+n junction extending into the silicon bulk with equal depths. The depletion regions and potential distribution are shown in figure 13 (b).

The formation of the depletion layers is a consequence of the reverse bias applied to the p^+n junctions. The fixed positive charge of the ionised donors in the depleted region is compensated by an

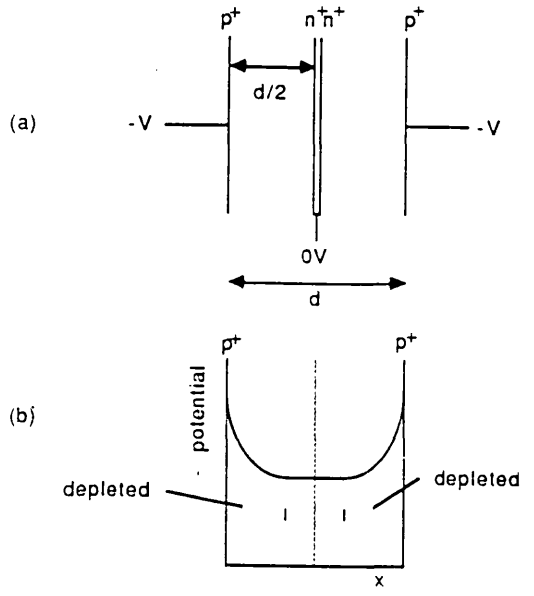


Figure 13: Two standard p^+n detectors in proximity (a) With n^+ electrodes in contact. (b) Potential and depletion regions of the two detectors under reverse bias.

equal amount of negative charge sitting in the p^+n junctions. The n^+n contacts act only to conduct charge and do not play any role in the depletion mechanism. Thus the same situation can be realised using a single semiconductor wafer of twice the thickness with two p^+n junctions at opposite surfaces of the wafer, as shown in figure 14 (a). The depletion mechanism is the same as with the standard p^+n junction - as the bias voltage V is increased, the depletion region increases at the expense of the thickness of the undepleted conductive channel. The contact to the n-type silicon can be made at the edge of the wafer as shown in figure 13 (a), or more realistically via an n^+ implant like that shown in figure 15.

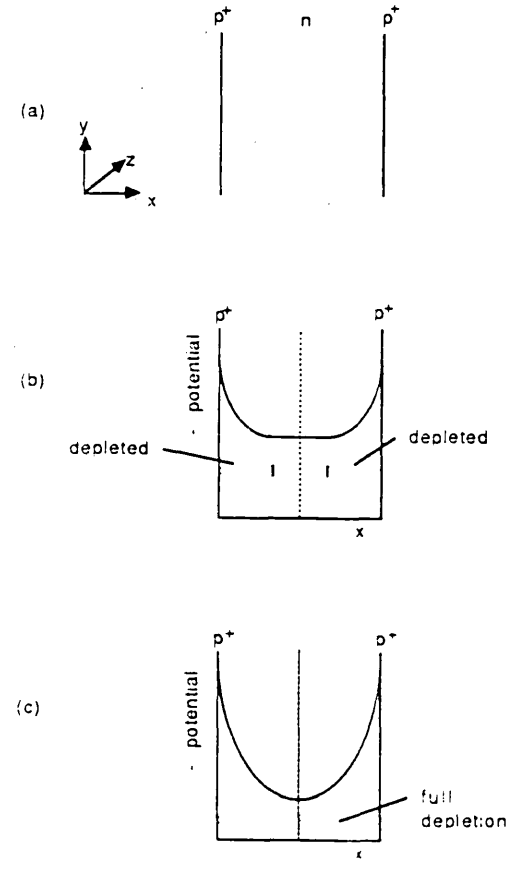


Figure 14: Depletion of a single n-type semiconductor with p^+ junctions on both sides.

As the bias voltage is increased further, the central undepleted conductive channel becomes narrower and eventually, at full depletion, it disappears. In this situation the detector becomes fully depleted and the bias voltage required is given by

$$V_D' = \frac{(d/2)^2}{2\,\varepsilon\,\mu_n\,\rho} = V_D/4 \qquad (2.23)$$

Thus the voltage needed to fully deplete the wafer is equal to a quarter of the voltage required to fully deplete a standard p^+n diode detector of the same thickness and resistivity.

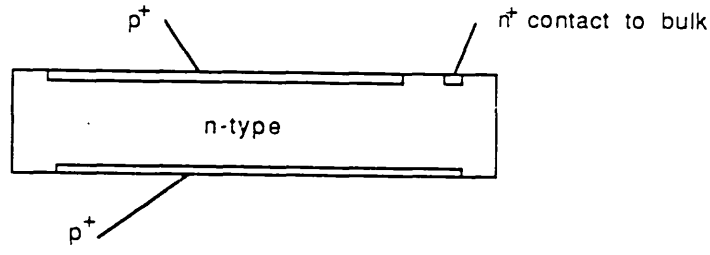


Figure 15: Practical means of contacting the n-type silicon via an n^+ implant at one side of the detector.

The important feature of the fully depleted condition is the existence of the potential minimum for electrons at the centre of the wafer. Since e-h pairs are continuously produced by thermal generation, this depletion state is evidently unstable because electrons would tend to accumulate at this potential minimum. The answer is to incline the potential as shown in figure 16 so that thermally generated electrons are continuously swept towards the n^+ anode. Figure 16 also illustrates the principle of drift in SDCs. Electrons generated by the passage of an ionising particle in the detector are transported along the potential 'gutter' to the anode. The time delay between the passage of the particle and the signal at the anode is due to drift of electrons and can be used to measure the position of the incident particle.

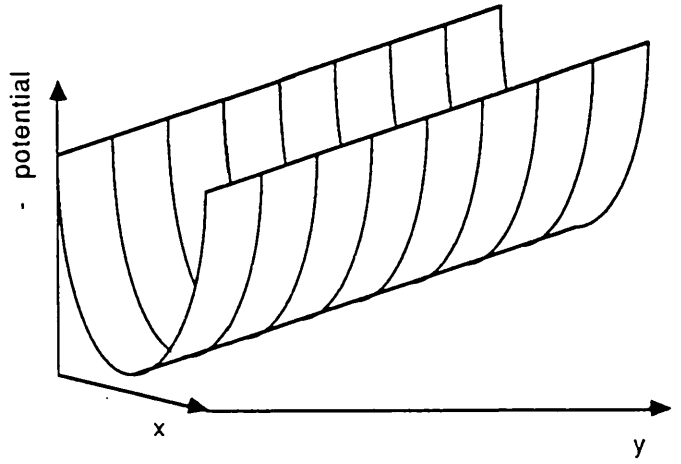


Figure 16: Potential of à fully depleted silicon wafer when an additional constant field along the y-axis is applied.

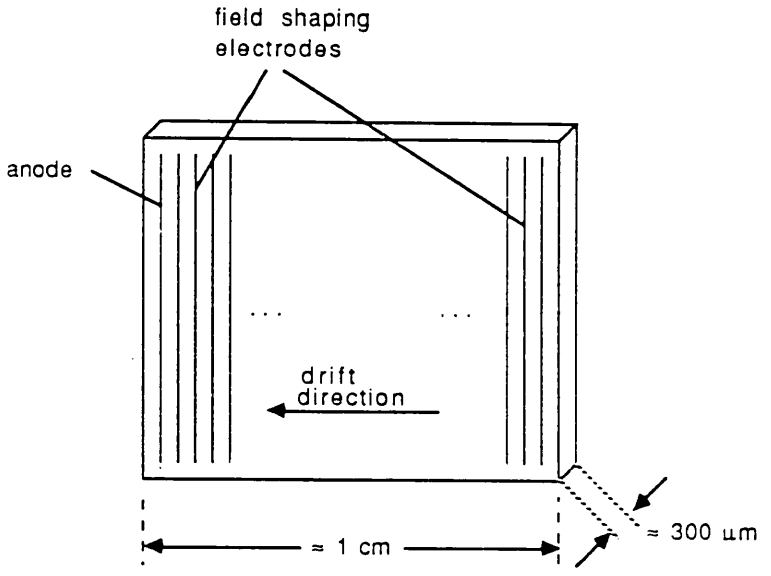


Figure 17: Practical realisation of a silicon drift chamber

The arrangement used in an actual detector is shown in figure 17.

Both surfaces are subdivided into parallel p^+ strips and on one surface the first strip (the anode) is an n^+ implant. A positive potential is applied to the anode to fully deplete the detector as described above and in addition a drift field is provided by superposing a potential of the form

$$\phi = - E \cdot y \qquad (2.24)$$

where E is the electric field. This is achieved in practice by linearly grading the potential on the strips, the potential becoming more positive towards the anode. In the anode region the potential minimum is shifted from the centre of the wafer to the anode surface so that electrons drifting along the detector are finally collected at the anode. The resultant potential distribution in the SDC in a region near the anode is shown in the plots of figure 18.

With an electrode pitch of 250 μm and a voltage per strip of ΔV = 5V, the drift field is 200 V/cm. The drift velocity is then $v_d = -\mu_n E$ = 2.7 μm/nsec. Thus the drift field is small compared to typical internal fields induced by the depletion process allowing drift times which are measurably long. The position information is derived from the measurement of the electron drift time. When a fast charged particle traverses the detector the electrons generated drift along the detector in the potential gutter. During the transit time the signal charge is screened by the p^+ electrodes and the signal appears only when the electrons arrive close to the collecting anode.

The anode can be connected to a charge sensitive amplifier to read out the signal. The capacitance of the anode is very small and independent of the active area of the detector. Also, the single

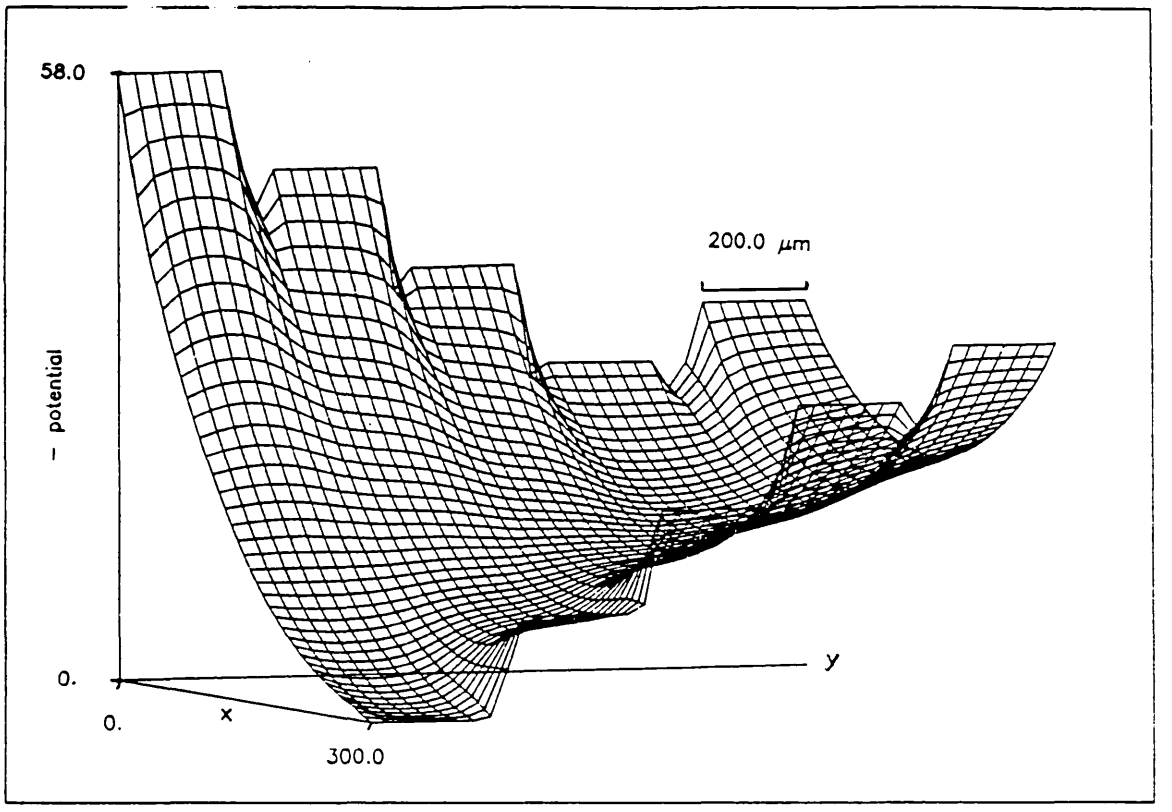


Figure 18: Potential within a silicon drift chamber in a region close to the anode.

channel of electronics connected to the anode is used to read out a relatively large area of the detector thereby reducing the number of readout channels by a factor of ~ 100 compared with a microstrip silicon detector.

Chapter III

FABRICATION TECHNIQUES FOR SILICON DETECTORS

3.1 INTRODUCTION

Silicon detectors fabricated by the planar process, using oxide passivation and ion implantation, were pioneered by J.Kemmer [17, 18]. The planar process is a well known fabrication technique and the technology has been highly developed for the manufacture of silicon devices and integrated circuits (ICs). However, the application of the planar process to silicon detector production is not a trivial step and has caused some difficulties. For IC fabrication, both n-type and p-type silicon are used, but the doping concentration is much higher and the lifetimes of minority carriers are some orders of magnitude lower. Silicon crystals of orientation <100> are generally used since they have the lowest surface state density.

For silicon detectors wafers of high resistivity and of <111> orientation must be used. To obtain low leakage currents special care during the processing must be exercised to ensure low charge densities in the Si-SiO_2 interface system and to avoid killing of the minority carrier lifetime during high temperature treatments. Using a suitable processing plan these aims can be achieved and this chapter describes some of the techniques used in the production of silicon detectors.

The growth of single crystals of silicon from high purity polysilicon represents the first significant step in the manufacture of a highly perfect semiconductor material. For detector grade silicon this is achieved by the floating zone (or float zone crucible-less) technique. In this process a polycrystalline rod of silicon is converted into a single crystal rod by traversing a molten zone of silicon from one end of the polycrystalline rod to the other with the initial zone being created in contact with a single crystal seed. Melting of the silicon to form a zone is achieved by induction heating.

Conversion of silicon ingots into polished wafers requires firstly slicing the crystal followed by etching and polishing. Slicing is performed with a diamond-edged saw blade leaving the surfaces of the resulting wafer damaged and contaminated in a region of typical depth 10 μm. This layer is removed by chemical etching and finally the wafers are polished by a chemi-mechanical process to provide a smooth, specular surface where device features can be photoengraved.

3.2 OXIDATION OF SILICON

In silicon integrated circuit technology oxide layers provide surface passivation for a silicon device, act as a diffusion mask and ion implantation mask and also provide isolation of one device from another. These requirements have led to the development of a number of methods of oxidation. The most widely used ones are plasma anodisation [19, 20], chemical anodisation [21], vapour-phase

reaction [22] and thermal oxidation [23]. For silicon detectors low leakage currents are required and the oxide-silicon interface must have a minimum, stable density of oxide fixed charge and interface trapped charge (see section 3.2.5). The oxide must also be stable under fields normal to the oxide-air interface. The oxide that meets these requirements best is the thermally grown oxide. Thermal oxidation is therefore the predominant oxidation technique used in both silicon detector and IC fabrication.

3.2.1 Silicon Oxidation Model

The growth of oxide layers on silicon by thermal oxidation can be achieved in several ways. For oxidation in pure oxygen, producing 'dry oxides', the chemical reaction is

$$Si(solid) + O_2 \leftrightharpoons SiO_2 \ (solid)$$

For wet oxides, where the oxidation is carried out in a water vapour ambient, the reaction is

$$Si(solid) + 2H_2O \leftrightharpoons SiO_2(solid) + 2H_2$$

The basic process involves shared valence electrons between silicon and oxygen forming covalent bonds. During the oxidation the Si-SiO_2 interface moves into the silicon and the amount of silicon used up can be calculated from the densities and molecular weights of silicon and silicon dioxide. For the growth of an oxide film of thickness d, a layer of silicon 0.45d thick is consumed.

It has been shown experimentally that oxidation of the silicon proceeds at the Si-SiO_2 interface and that the oxidising species diffuses through the oxide layer and reacts at the Si-SiO_2 interface.

Uncertainties exist, however, as evidenced by controversies in the literature as to whether charged or neutral species are transported through the oxide, and on the details of the reaction at the Si-SiO_2 interface. If a silicon sample is exposed to an oxidising ambient, the initial oxidation rate is fast since there are a great number of oxidant molecules available at the silicon suface. As the oxide layer grows the rate becomes limited by the fact that oxidant molecules must diffuse through the silicon dioxide layer. The oxide thickness at which diffusion of the oxidant becomes limiting is about 40 Angstroms for dry oxidation and 1000 angstroms for wet oxidation. The kinetics of the oxidation process are described mathematically by the model of Deal and Grove [24].

For oxides grown in steam the oxide layer is, in fact, SiO_2 containing a given amount of water molecules, the amount being dependent on the oxidation conditions. The amount of hydration of an oxide layer is important since it can determine how well a photoresist layer will adhere to it and can also affect the stability of the device. One advantage of wet oxides is that the time taken to grow an oxide of given thickness at a given temperature is much less than the time required in a pure dry oxygen ambient. However, in general, silicon detectors for HEP have employed dry oxidation because of the improved electrical properties obtained.

3.2.2 Practical Means of Oxidation

The oxidation of all silicon wafers used, for both microstrip detectors and silicon drift chambers, was carried out in a heated furnace system as shown in figure 19. The system consisted of a resistance heated furnace held at a constant temperature by a temperature controller. Typical oxidation temperatures range from 800°C to 1200°C. The furnace tube in which the wafers are placed during oxidation was a cylindrical fused quartz furnace tube about 2 m long. At one end of the furnace tube a gas inlet was provided which was fed by the gases used during the oxidation. All gases used were of high purity and their flow rates in the furnace were controlled by flow regulators in the supply lines.

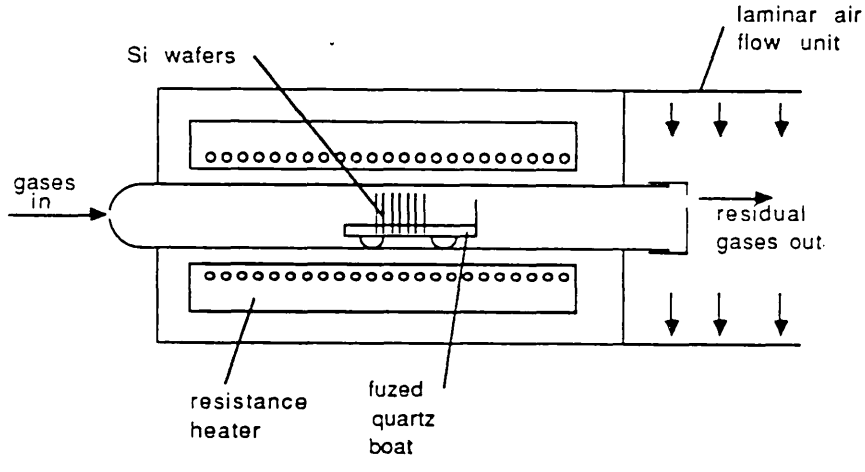


Figure 19: The oxidation furnace

Comtamination from the surrounding air was minimised during the oxidation by positioning the oxidation furnace in a carefully controlled

clean area. Additionally, the loading end of the furnace protruded into a vertical laminar flow unit. This ensured the minimisation of particulate matter in the air surrounding the wafers during loading, which could adhere to the silicon wafers and contaminate the oxide layer grown or the underlying silicon. One of the most common contaminants in the surrounding air is sodium, which can become incorporated into the silicon dioxide layer as positively charged mobile ions. Another source of sodium contamination is the furnace lining. Sodium from the lining can diffuse through the furnace walls and contaminate the wafers inside. For this reason a lining with very low sodium content was used (the sodium content is minimised by the manufacturer).

Loading of the wafers into the furnace proceded by the use of a fused quartz 'white elephant' and a fused quartz pushrod. The wafers were loaded into a slotted quartz boat and placed in the white elephant, which then fitted onto the loading end of the furnace tube. During the loading the furnace was maintained at a temperature of 600°C and a constant flow of inert argon gas was passed through it. The boat was slowly pushed to the centre of the furnace tube over a period of about 5 minutes and then the temperature was ramped up to the oxidation temperature. This minimised the thermomechanical stress exerted on the wafers due to sudden increases in temperature.

3.2.3 Effects of Oxidation

Thermal oxidation has three effects on the electrical properties of silicon. For silicon detectors the most important is the introduction of oxidation-induced stacking faults, which are structural defects at the silicon surface and are important because they can be electrically active, causing increased junction leakage and reduced minority carrier injection efficiency. A second effect is the redistribution of ionised impurities at the silicon surface. A doping impurity initially present in the silicon will redistribute at the interface until equilibrium is established. If diffusion of the impurity through the SiO_2 is relatively slow (as is the case for phosphorus), the impurity piles up near the silicon surface. Thus, for uniformly phosphorus doped n-type silicon, oxidation will result in an enhanced phosphorus concentration near the silicon surface. However, the effect is usually small in this case[1] and does not pose any significant problems in silicon detector manufacture.

Strain is another effect of oxidation on silicon. Growth of an oxide layer on silicon puts the silicon under strain at room temperature because of the mismatch in the coefficient of thermal expansion between silica and silicon. However, for 300 µm thick 3-inch wafers, the wafer warpage that results from these strains is negligible.

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[1] For phosphorus doped silicon oxidised at 1030°C the ratio C_S/C_B (concentration at silicon surface to concentration in silicon bulk) is ~ 1.25 for oxidation in O_2 and ~ 1.65 for oxidation in H_2O [25].

3.2.4 Oxidation-induced Stacking Faults

A stacking fault is a structural defect in the silicon lattice consisting of an extra plane of silicon atoms bounded along the edges by dislocation lines. The generation of stacking faults is a common and undesirable consequence of thermal oxidation of silicon resulting in the introduction of defects into otherwise defect-free crystals. These crystal faults are called oxidation-induced stacking faults and may extend from the silicon surface into the bulk of the silicon. Stacking faults are generated upon oxidation when the surface of the wafer is damaged by some sort of abrasion or if mechanical damage generated by the crystal cutting operation is not entirely removed by chemical polishing. The regions of mechanical damage function as nucleating regions for stacking faults.

The electrical activity of a stacking fault is greatly increased when it is decorated with impurities, typically heavy metals. As discrete defects possessing localized strain fields, stacking faults act as sinks for impurities. The impurities diffuse towards the dislocation lines bounding the stacking faults where they can easily fit, minimising lattice energy. A cluster of impurity atoms builds up with time at elevated temperatures at the sites of the stacking faults. Some of these impurity atoms have energy levels near the centre of the silicon bandgap and therefore act as efficient generation-recombination centres. If such stacking faults pass through the depletion region of a pn junction, they will increase the leakage current by generation and reduce the minority carrier lifetime by recombination. If the concentration of impurities at the stacking fault is sufficiently high,

leakage currents can be so large that the junction is effectively a short circuit. This increase in leakage current due to electrically active oxidation-induced stacking faults has been observed experimentally [26].

The effects of stacking faults on the characteristics of silicon detectors can be minimised by either gettering impurities or reducing the size and number of the stacking faults. In order to minimise the presence of stacking faults it is necessary to have some understanding of the mechanism of creation of stacking faults. Although the process is not fully understood, it has been established that (a) formation of oxidation-induced stacking faults is related to the presence of excess silicon atoms at the Si-SiO_2 interface (due to the oxidation process) and that (b) stacking faults are created by the coalescence of excess silicon atoms at nucleation centres.

It has been observed that the stacking fault length increases with increasing temperature and this is a major factor in determining the oxidation temperature. In this respect a low oxidation temperature is desirable, but since this results in increased oxidation time, a compromise was made. There are also other effects of the oxidation temperature which must be taken into account and these are described later. For silicon detectors an oxidation temperature of 1030°C is found to be suitable. Detectors produced using this oxidation temperature were found to have low leakage currents (~ 10 nA cm^{-2}) showing that the suppression of harmful effects due to stacking faults was achieved.

3.2.5 Charges in the Si-SiO_2 System

The Si-SiO_2 system has several types of charge states associated with it. A charge near the Si-SiO_2 interface can induce a charge of the opposite polarity in the underlying silicon, thereby affecting the ideal characteristics of silicon detectors. This results in both yield and and quality problems in the device fabrication. The various types of charges are briefly described here.

(a) Oxide Fixed Charge Q_f

The oxide fixed charge is a stable, positive charge located in the oxide within approximately 34 Å [27] of the Si-SiO_2 interface. It cannot be charged or discharged by the exchange of mobile carriers with the silicon. Its density ranges from 10^{10} to 10^{12} cm^{-2}, depending on oxidation and annealing conditions and it is related to the oxide structure in the interface region between the SiO_2 and the silicon.

(b) Interface Trapped Charge Q_{it}

Q_{it} is located at the Si-SiO_2 interface and can change its charge state by exchange of carriers with the silicon. The interface trapped charge includes several types of fast states, appearing both at discrete energy levels and as a continuous distribution throughout the silicon bandgap. Although the origin of Q_{it} is not known it is assumed at present that these states result from either structural defects related to the oxidation process and/or metallic impurities. The density of these charges is expressed in terms of unit area and energy in the silicon bandgap and values of 10^{10} cm^{-2} eV^{-1} and lower have been observed.

(c) Mobile Ionic Charge Q_m

Q_m is normally attributed to positive alkali ions (Na^+, K^+, Li^+) in the oxide. Due to the abundance of sodium in the environment and because of its rapid transport in SiO_2, Na^+ is the most important mobile ionic charge present. The human body is one of the major sources of sodium contamination in the processing laboratory. The rearrangement of the ionic charge distribution within the oxide due to applied fields can cause device instability and this effect is known as ionic drift.

(d) Radiation-induced Charge Q_{ot}

Q_{ot} is a positive charge located in the oxide, generally near the $Si-SiO_2$ interface, caused by ionising radiation. Fast states are also produced at the $Si-SiO_2$ interface by ionising radiation. The origin of Q_{ot} has been attributed to (i) trapping of holes (produced in e-h pair creation by the radiation) in the oxide and (ii) the activation of impurities such as Na^+, although the correct mechanism is unknown. The effects of radiation damage on silicon detectors have been investigated by several authors [28] and will not be discussed further here.

3.2.6 Control of Oxide Charges

(a) Sodium Ionic charge Q_m

The main sources of mobile ionic charge (sodium) are oxidation, high temperature annealing and other high temperature processes such as the photoresist bake. Other sources include chemical reagents used in cleaning and general handling of the wafers. The oxidation process is the most critical and several precautions were taken to

avoid sodium contamination. A method which is widely used to reduce the sodium concentration to negligible levels in the oxidation furnace (sodium free fused quartz) is to clean the furnace with an $HCl-O_2$ mixture at elevated temperatures and this was performed before each oxidation. The furnace was cleaned by passing a few percent $HCl-O_2$ mixture through it at oxidation temperature. In addition, the furnace tube was periodically removed from the furnace and cleaned. This procedure consisted of an HF rinse followed by a rinse in deionised water. The furnace tube was then replaced in the furnace and purged in an $HCl-O_2$ mixture for ~ 24 hours.

The mechanism of HCl cleaning is thought to be the oxidation of HCl in the $HCl-O_2$ mixture to form water vapour and chlorine gas, followed by the reaction between chlorine and sodium in the furnace tube to form NaCl. The NaCl is volatile at these high temperatures and is carried away with the outgoing gases.

Since almost all chemicals contain some sodium except deionised water, the last step in any process involving chemical reagents should always be a rinse in deionised water. Also, electronic grade reagents should be used for processing since they contain low levels of sodium and other contaminants.

Another well established method used to eliminate sodium contamination during processing and device life is that of gettering using a mixture of $HCl-O_2$ and this was implemented during the processing of the silicon detectors fabricated for this study. Gettering using a few percent $HCl-O_2$ mixture is effective since the HCl getters sodium in the ambient of the furnace tube in a similar

way to the furnace-cleaning action described above. Secondly and more important, is the fact that chlorine is incorporated into the oxide around the $Si-SiO_2$ interface, neutralising sodium ions when they arrive there. It has been shown that the chlorine not only neutralises the sodium ions at the $Si-SiO_2$ interface but that it also imobilises them - they lose their charge by becoming chemically bound to chlorine located near the $Si-SiO_2$ interface.

The gettering effect of an $HCl-O_2$ mixture continues even after the oxidation and is effective in gettering sodium during subsequent high temperature steps in the processing (e.g. photoresist bake) and also during the device lifetime. The effect of gettering by chlorine requires that the HCl be mixed with dry oxygen. $HCl-H_2O$ mixtures have been shown to be ineffective in gettering. The dry oxygen provides chlorine by the reaction

$$4HCl + O_2 \leftrightharpoons 2H_2O + 2Cl_2$$

and it is this chlorine which is the active getterer.

(b) Oxide Fixed Charge Q_f and Interface Trapped Charge Q_{it}

Assuming the mobile ionic charge can be controlled the remaining charges left in the $Si-SiO_2$ system which can significantly affect the electrical properties of silicon detectors are Q_f and Q_{it}. These charges affect the reverse bias leakage current of junction detectors as described in section 2.5. Also, positive oxide fixed charge can cause reduction of the breakdown voltage in a p^+n junction detector as illustrated in figure 20. Q_f causes an accumulation of electrons at the surface of the n-type substrate, forming a p^+n^+ junction there

that has a lower avalanche breakdown voltage than the p^+n junction in the bulk. In silicon drift chambers the presence of oxide fixed charge causes distortions of the electric field distribution in the detector. This can lead to undesirable charge transport properties (as discussed in chapters 5 and 6) and also affects the voltage at which the hole current will flow (see section 6.3.4). Thus it is desirable to control the densities of Q_f and Q_{it} present in the detectors.

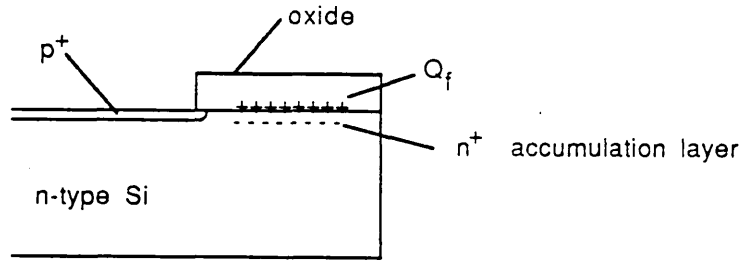


Figure 20: Effect of oxide fixed charge on a planar p^+n detector

It has been found that oxide fixed charge density depends mainly on oxidation temperature and annealing conditions. In general, for high oxidation temperatures, dry oxidation results in a lower density of Q_f. Figure 21 summarises the relation of Q_f to oxidation conditions and annealing in dry nitrogen or argon. This shows that the higher the oxidation temperature the lower the density of Q_f obtained. In addition, slow cooling from the oxidation temperature permits oxidation

to continue at low temperatures, resulting in a higher Q_f. This is avoided by converting from oxygen to an inert gas (e.g. nitrogen or argon) at oxidation temperature and then cooling down slowly as shown in figure 21.

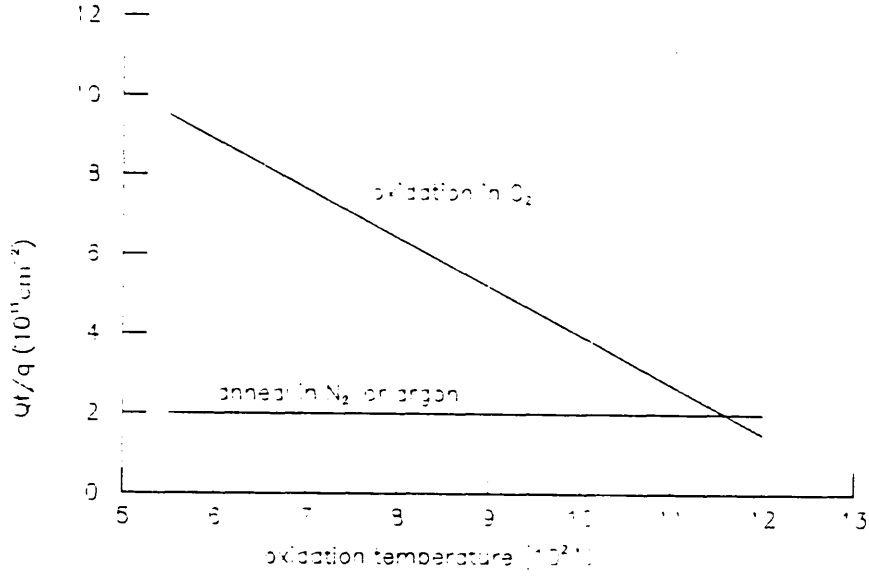


Figure 21: Oxide fixed charge density
as a function of oxidation temperature and annealing temperature.

The value of the interface trapped charge density D_{it} can be minimised by using a high oxidation temperature but it must be reduced further by an anneal. Two methods are available: (i) the low temperature postmetallisation anneal and (ii) the high temperature postoxidation anneal.

(i) The Low Temperature Postmetallisation Anneal

This involves the low temperature annealing of the wafers after aluminium metallisation. The annealing is done in a separate furnace at ~ 300-400°C in a hydrogen ambient for up to 30 min.

Deal et. al. [29] proposed a mechanism to explain low temperature postmetallisation annealing. Water, present even in dry oxides, chemically reacts with aluminium to form aluminium oxide and atomic hydrogen. Some of the atomic hydrogen then diffuses to the Si-SiO_2 interface and chemically reacts with the interface traps, making them electrically inactive. The postmetallisation anneal also serves to anneal the X-ray damage caused by the electron beam evaporation of aluminium (see section 3.5).

(ii) The High Temperature Postoxidation Anneal

This involves a high temperature (~ 1150°C) anneal in hydrogen or an inert gas after oxidation.

3.3 PHOTOLITHOGRAPHY

Photolithography is the process of transferring geometric patterns on a mask to the surface of a silicon wafer. Once a silicon wafer has been oxidised, certain areas of the oxide may need to be etched away forming a pattern of 'windows' in the oxide. This pattern of windows determines the areas which become doped with impurities - on ion implantation, only those areas with no oxide become doped since ions implanted into the SiO_2 layer do not become electrically active. The required pattern is usually computer generated, the data being used to produce a physical mask which usually consists of a chromium pattern on a glass plate.

Photolithography relies on the use of a photosensitive polymer film called photoresist. Positive photoresists are typically three-component materials consisting of a base resin, which gives the resist its

film-making properties, a photoactive compound, and volatile solvents to make the material liquid for application. In a dried photoresist film (typically 0.5-2.0 μm thick), the photoactive compound (inhibitor) serves to inhibit dissolution of the resist in an alkaline aqueous solution (developer). Exposure to blue or ultraviolet (UV) light causes destruction of the inhibitor creating byproduct molecules that allow dissolution of the resist. Thus when a positive photoresist film is exposed to an optical pattern, using UV light, the areas which are exposed become soluble in developer solution. Unlike negative photoresist where the developer permeates the whole resist film causing swelling of the film, development of positive photoresist is a surface reaction and so results in higher resolution. After developing , the wafer is put into an ambient that etches the exposed SiO_2 but does not attack the resist. Buffered hydrofluoric acid is a typical SiO_2 etchant. Finally the resist is stripped, leaving behind the required SiO_2 image.

Two methods of optical exposure were used in the fabrication of the SDCs. In one case the mask alignment system was a contact printer, figure 22 (a). The resist-coated silicon wafer was brought into physical contact with the glass photomask. The wafer was held on a vacuum chuck and to align the mask pattern to a previously etched SiO_2 pattern, the mask and wafer were separated by about 25 μm. Viewing of the patterns was achieved using two objectives connected to a split field microscope. When the exposure button on the aligner was pushed the microscope was retracted and a collimated beam of UV light illuminated the whole wafer. The second mask

aligner used proximity printing (figure 22 (b)) which is very similar to contact printing except that a small gap (~ 7 μm) was maintained between the wafer and mask during exposure. This gap minimised mask defects accumulated during successive mask uses, which is the main disadvantage of contact printing.

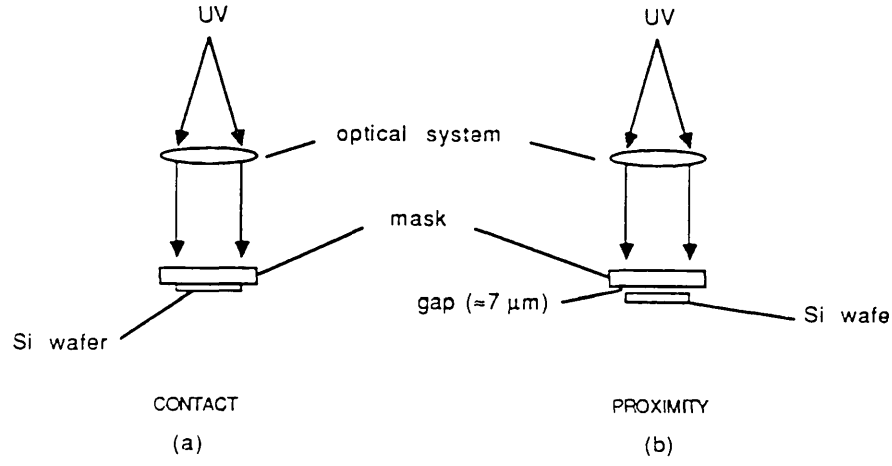


Figure 22: Optical lithographic exposure techniques
(a) Contact printing. (b) Proximity printing.

3.4 ION IMPLANTATION

Due to the absence of ion implantation facilities at Micron Semiconductor Ltd. this was the only step in the fabrication of the detectors which was done elsewhere. In this process the dopant atoms are implanted into the surface of the wafer by ionising the impurity atoms, accelerating them to the required energy, and allowing them to impinge upon the wafer.

Ion implantation has several advantages over conventional diffusion for the formation of pn junctions. Since implantation is usually done at room temperature, it is possible to use a variety of materials to mask the implantation from regions of the wafer which are not required to be doped. As well as SiO_2, other materials can be used as a mask including photoresist which cannot be used for a mask in conventional diffusion. Also, by controlling the impurity dose and the ion beam energy, precise tailoring of the profile of the implanted ion distribution can be achieved.

Due to the applications of ion implantation in silicon device fabrication much research has been carried out in the calculation and measurement of implanted ion distributions [30]. The depth distribution or profile of stopped ions can be approximated by a symmetric Gaussian distribution function:

$$n(x) = \frac{\phi}{\sqrt{(2\pi)}\ \Delta R_p} \exp\{-(x-R_p)^2/2\,\Delta R_p^2\}$$

where R_p is the projected range,

ΔR_p is the projected straggle

and ϕ is the total dose implanted .

Although the fit to experimental data is almost always good near the peak, there is pronounced skewness in the actual distributions. To account for the skewness and also any tailing character more sophisticated models are needed [31].

3.5 METALLISATION

Metallisation serves to make electrical contacts to silicon detectors. For an n-type detector, this requires low resistance contacts to be made to the p^+ and n regions with good metal adherence and a straightforward method of patterning the metal.

For a metal-semiconductor contact in forward bias there are two main components of the current. For low semiconductor doping densities the diffusion current (or thermionic emission current) dominates, leading to relatively high contact resistances. For high doping densities the tunnelling current dominates leading to lower contact resistances. In the latter case the contact resistance R_c is [32]

$$R_c \propto \exp \{\phi_B/\sqrt{N_D}\}$$

where ϕ_B is the metal-semiconductor barrier height and N_D is the doping density concentration. Thus high doping concentration, low barrier height or both must be used to obtain low resistance (ohmic) contacts.

Aluminium satisfies all of the above requirements and was used to make ohmic contacts to the detectors produced. However, before contacting the n-type region of the detectors an n^+ layer was formed at the surface using ion implantation. This served to increase N_D thereby lowering R_c to make a low resistance contact.

The aluminium metallisation was achieved using electron beam evaporation. This was carried out in a high vacuum chamber shown schematically in figure 23. This consists of a large stainless steel

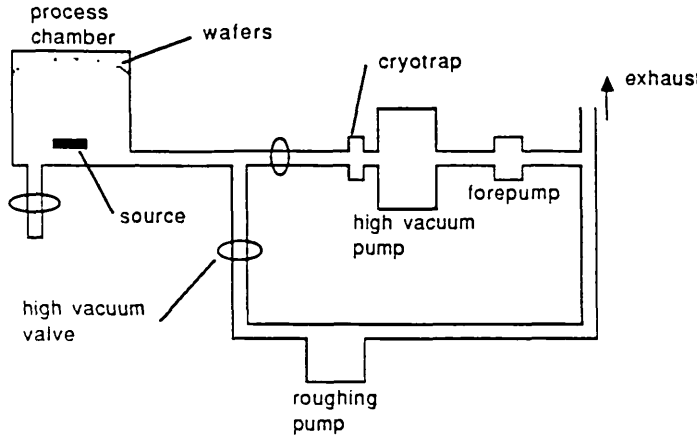


Figure 23: Schematic representation of the high vacuum chamber used for the metallisation process.

cylindrical vessel ('bell jar') sealed at its base by a gasket, in which the evaporation was carried out. The remainder of the apparatus constitutes the pumping system which brings the pressure in the bell jar down to a working value of $< 10^{-6}$ torr.

Figure 24 shows a simplified diagram of the electron beam evaporation system. A tungsten filament acts as a cathode and the electrons are accelerated through ~ 10-15 kV and strike the aluminium source. A magnetic field bends the electrons in a curve which permits screening of the hot filament so that impurities from the filament cannot reach the evaporant. The aluminium source sits in a water cooled copper hearth to eliminate evaporation of the holder material. During the evaporation the film thickness was monitored by a quartz crystal monitoring system and the final film thicknesses were approximately 1 μm.

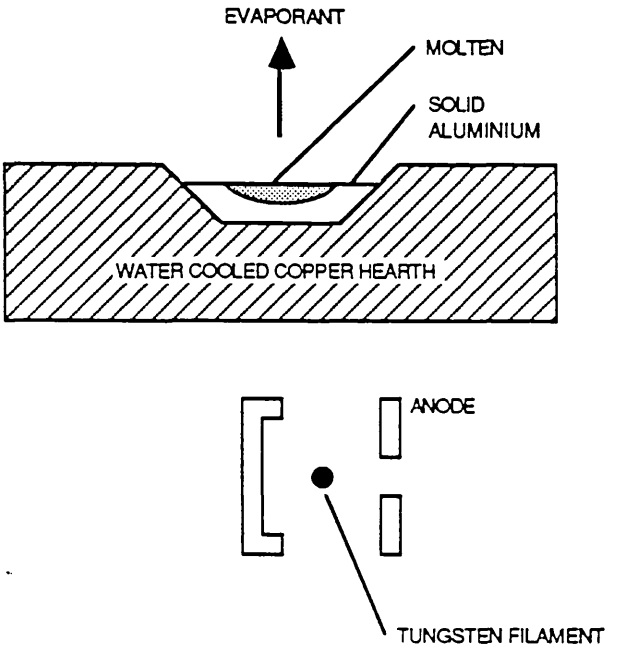


Figure 24: The electron beam evaporation system

At voltages of the order 10 kV the characteristic aluminium K-shell X-rays, along with a continuum, are emitted. This causes radiation damage in the silicon wafers and so subsequent annealing is necessary. This is achieved by the postmetallisation anneal described in section 3.2.6.

Patterning of the aluminium was achieved by photolithography using a suitable solution to etch the metal.

Chapter IV

FABRICATION OF SILICON DRIFT CHAMBERS

4.1 PRODUCTION OF THE PHOTOLITHOGRAPHIC MASKS

The first step in the fabrication of the silicon drift chambers was the production of the masks used for the photolithographic processes. The prototype detectors were designed with simplicity in mind and a structure consisting of 40 parallel strips, each 1 cm long, was decided upon. The strip width and pitch were chosen to be 200 μm and 250 μm respectively, although these values were not optimal (see chapter 6). On one side of the detector strip 10 was an n-type implant to act as the anode while the remainder of the strips were p-type implanted to act as field shaping electrodes. On the opposite surface two alternative designs were made. The structure consisted of either 40 parallel p-type field shaping strips or a uniform single-area p-type implant, 1 cm^2 in area.

Three-inch diameter n-type silicon wafers were used for the processing so that a 4×4 matrix of sixteen 1 cm^2 detectors could be fabricated on each wafer. The detectors were grouped into pairs with one detector incorporating a guard ring structure as shown in figure 25. In addition, groups of fiducial marks were included which consisted of four 100 μm crosses. These were used to aid mask alignment.

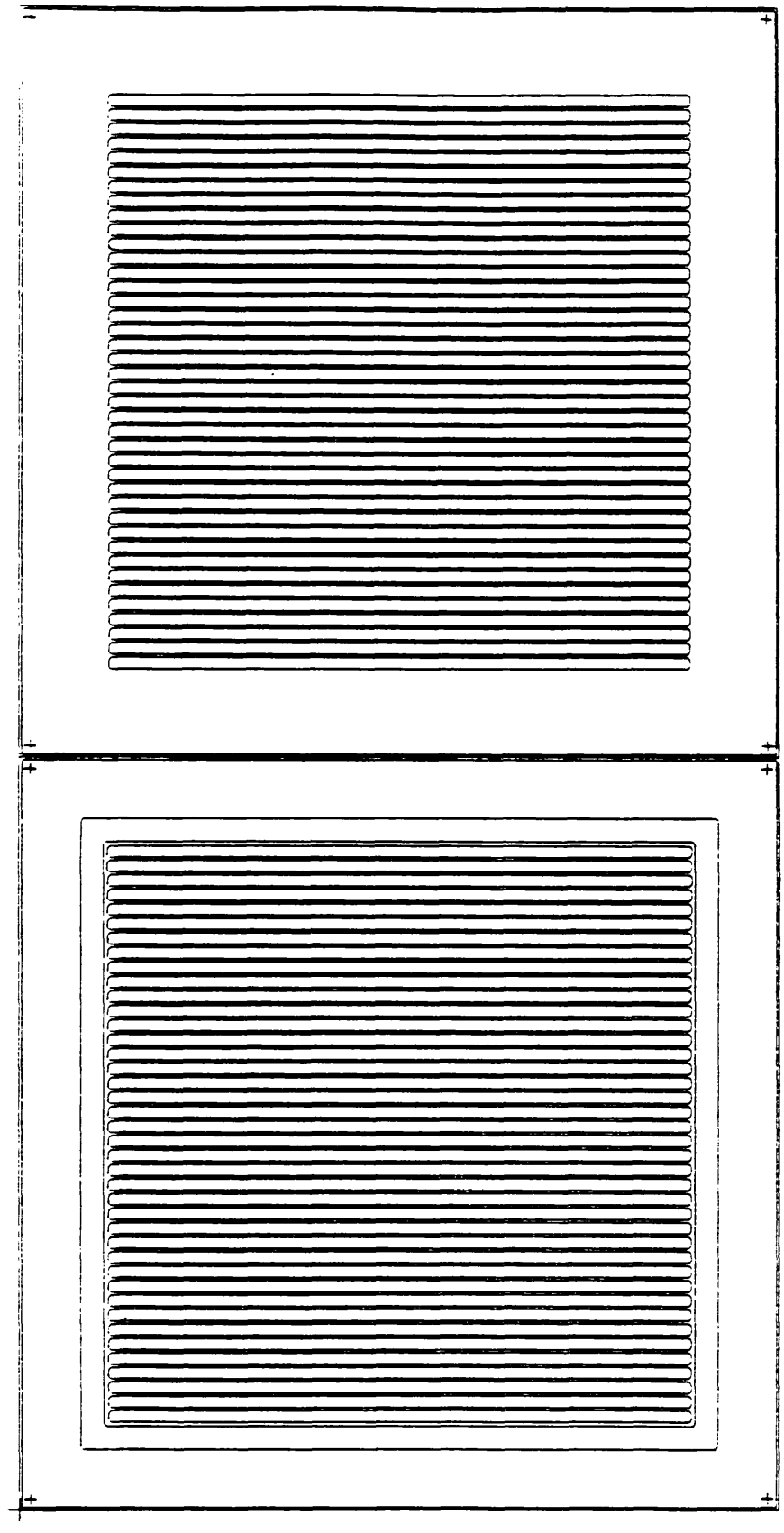


Figure 25: Magnified diagram of a pair of SDCs
The bottom SDC has a guard ring incorporated in the design.

The designs were defined using computer aided design incorporating GAELIC coding [33]. Once the GAELIC source program was compiled, checking of the layout for errors was done using on-line computer editing facilities and by producing magnified pen plots of the mask designs. The design data file was transferred to the Rutherford Appleton Laboratory (RAL) where, after suitable post-processing, it was used to control a machine at the Electron Beam Lithography Facility (EBLF). In this method of mask making a 4-inch × 4-inch glass plate covered with a thin film of chromium is used. The chromium is covered with a layer of electron resist which is then exposed by a focused electron beam. The exposed areas are determined by computer control of the electron beam and the masks are completed by developing the resist and etching the chromium.

All the masks used were produced using this technique at the RAL EBLF. After completion, the masks were inspected under a microscope. No visible errors in the layout of the masks could be seen. However, the masks were not free from defects. Several chrome spots and pinholes with radii of the order of 20 μm were seen on the masks which have been attributed to the electron beam lithography process. On average there were a total of about three such defects on each mask and the masks were considered adequate for the purposes of fabrication of prototype detectors.

4.2 DETECTOR FABRICATION

Fabrication of the silicon drift chambers was carried out by the author at Micron Semiconductor Ltd. The basic sequence of processing steps used in the production of the detectors is shown in figure 26 and is described in this section, although certain details are considered commercially sensitive and are therefore omitted.

The main difficulties encountered in the fabrication of the SDCs arose from the requirement for processing double-sided polished silicon wafers, using photolithography and ion implantation on both surfaces. The starting material was 3-inch n-type silicon wafers with low impurity doping concentrations to achieve high resistivities of $\rho >$ 3.5 kΩcm. The wafers were supplied with both surfaces etched and polished.

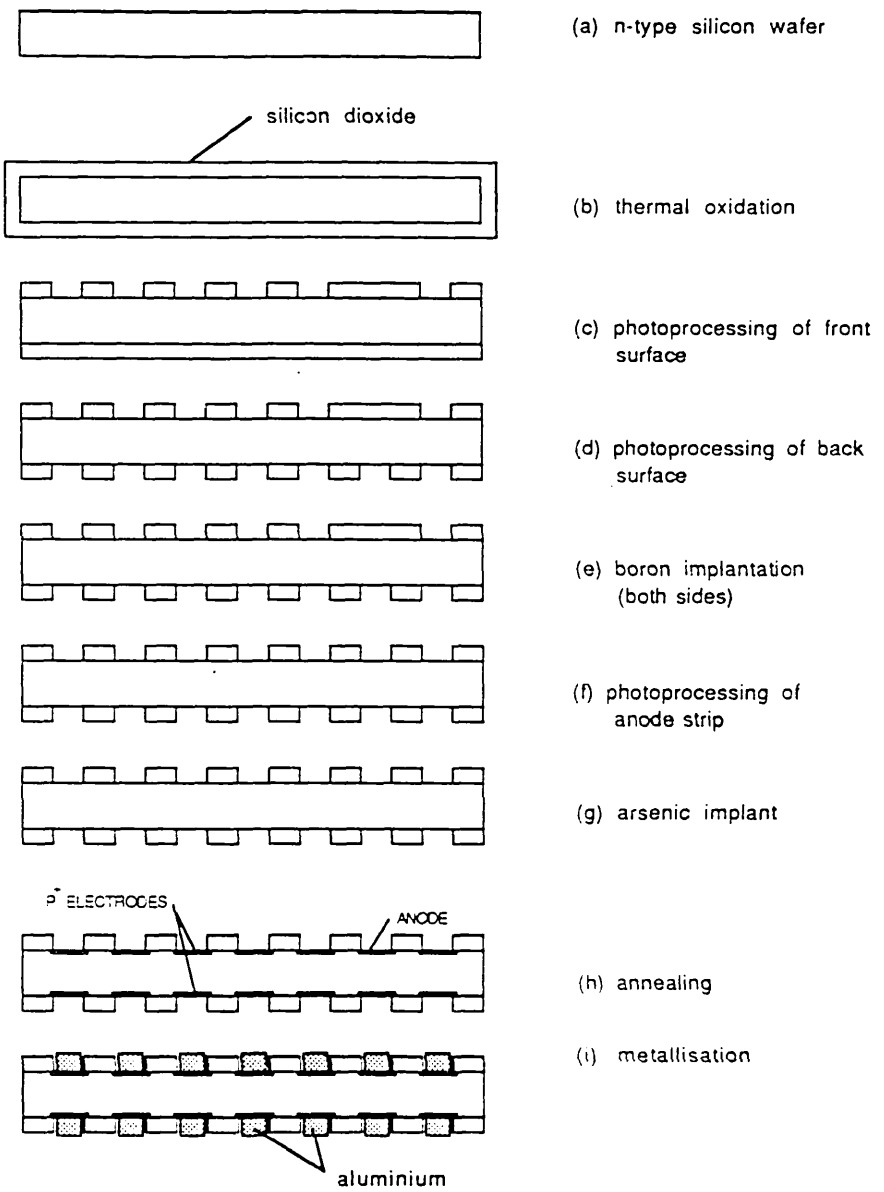


Figure 26: Processing steps in the fabrication of the SDCs

4.2.1 Oxidation

Before loading into the furnace the wafers were treated with cleaning solutions to remove surface contaminants [34]. A solution of hydrogen peroxide/ammonium hydroxide was used which removes organic contaminants by the solvating action of ammonium hydroxide and the powerful oxidising action of hydrogen peroxide. Also some group I and II metal ions are complexed by the small quantities of NH_3^+ found in equilibrium with NH_4^+. In addition, the wafers were treated with a solution of hydrogen peroxide/hydrochloric acid. During this process metal impurities are oxidised by the action of both hydrogen peroxide and chlorine in the solution to form stable chloride complexes.

After cleaning, the wafers were thermally oxidised at 1030°C using a standard oxidation procedure. HCl gettering was used to reduce oxidation-induced stacking faults and the wafers were cooled in an inert ambient to minimise the oxide fixed charge (see section 3.2.6).

4.2.2 Photoprocessing of the p^+ Electrodes

The next step was to etch the oxide to determine the pattern of p^+ electrodes on both sides of the wafer. This was done using the photolithographic process illustrated in figure 27. The wafer was coated with positive photoresist on both surfaces using a spinning machine. Typical resist thickness is 1-2 μm. After softbaking of the resist, the wafer was loaded into a mask aligner where the front (anode) surface of the wafer was exposed to a collimated UV light source through the relevant mask. The wafer was then developed

and after a hardbake of the resist the oxide was etched using buffered hydrofluoric acid (HF) solution. The resist was then chemically removed leaving the correct SiO_2 pattern on the front surface of the wafer (figure 26 (c)).

The oxide pattern on the opposite (back) surface was defined in a similar manner. However, since alignment of the back surface exposure mask with the front surface oxide pattern was necessary, a special purpose mask aligner was used. This consisted of a standard mask alignment machine modified so that an infra-red light source was placed beneath the wafer as shown in figure 28. The transmitted infra-red light was detected by means of a phosphor screen imaging system so that the front surface oxide pattern and the back surface mask pattern could be viewed simultaneously with a split-field microscope. After alignment, the photoresist was exposed and developed and the SiO_2 etched thereby forming the correct back surface pattern as shown in figure 26 (d).

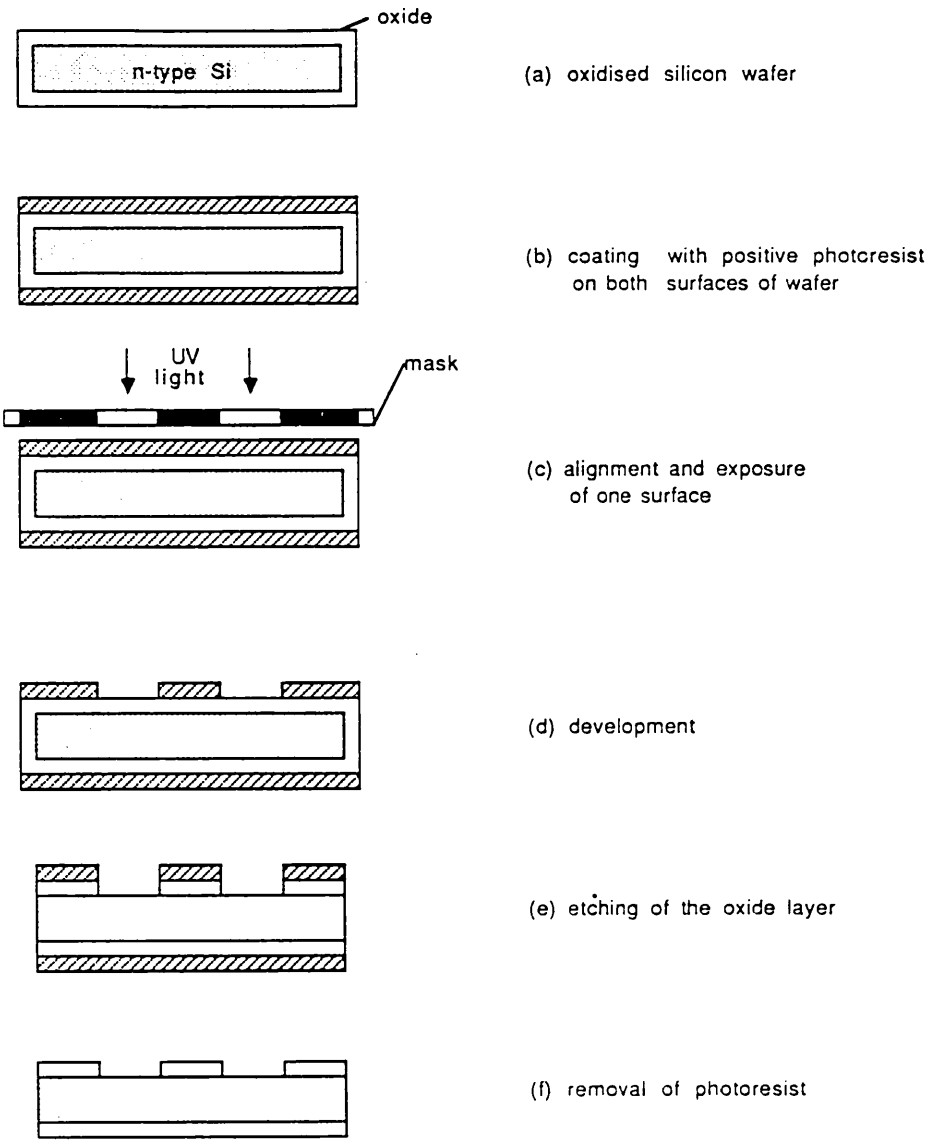


Figure 27: Basic steps in the photolitography for double-sided polished silicon.

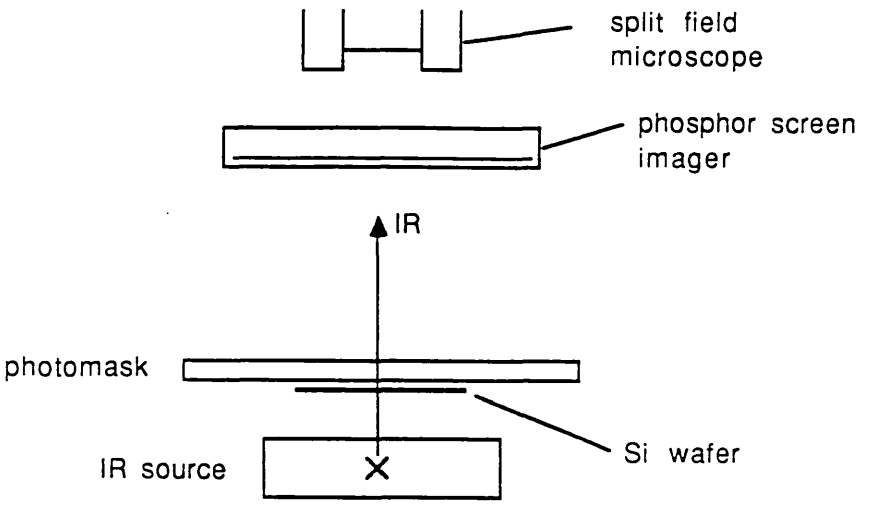


Figure 28: The infra-red alignment system

4.2.3 Boron Implantation

Figure 26 (e) represents a boron implantation on both sides of the wafer to produce the p^+ strips which acted as the field shaping electrodes. The implantation was performed one surface at a time and the non-implanted side was coated with a layer of photoresist for protection.

4.2.4 Fabrication of the n^+ Anode Strip

The n^+ anode strip was formed by an ion implantation through a photoresist mask. After the boron implantation, both sides of the wafer were coated with photoresist. The front surface resist layer was exposed through the 'anode' mask which was aligned with the existing oxide pattern on the front side of the wafer. After exposure and development, the SiO_2 was etched to form a window for the anode

implant (figure 26 (f)). The hardbaked photoresist layer served to mask the rest of the wafer from the implanted ions. From reference 35 it is found, for example, that the minimum thickness of photoresist required to stop 0.9999 of incident As^+ ions of energy 100 keV is approximately 0.2 μm. Thus a layer of photoresist of thickness ~ 1-2 μm serves as a suitable mask.

The ion implantation was performed using arsenic as the n-type dopant. It has been reported (e.g. [35]) that photoresist films used as masks for ion implantation can expand or even crack at high doses (> 10^{16} As^+/cm^2). In addition, ion bombarded photoresist layers become heavily cross-linked and are often difficult to remove. Thus the As^+ ion implantation dose was kept low enough to avoid these problems but sufficiently high to produce a good ohmic contact.

4.2.5 Annealing

During ion implantation target atoms (i.e. silicon atoms) will be displaced by each implanted ion resulting in damage of the crystal structure. To anneal out the damage and restore the crystallinity of the wafer, and to electrically activate the impurity atoms which do not occupy substitutional sites in the crystal, annealing at elevated temperatures was performed. The wafers were annealed in a fused quartz tube (similar to the oxidation furnace) with a nitrogen ambient for at least 30 min.

4.2.6 Metallisation

To achieve ohmic contacts to the p^+ and n^+ electrodes the next stage of the processing was the metallisation. The thin oxide which forms naturally when the wafers are exposed to oxygen in the air was first removed using a dilute buffered HF solution. This process was not successful for one surface of the wafers for the first set of prototypes and led to problems in the ultrasonic wire bonding of these detectors as described in section 5.1.1.

After removal of the thin oxide the wafers were transferred to the evaporation plant and a thin layer of aluminium was evaporated onto both surfaces. Electron beam evaporation was used and the thickness of the resulting aluminium film was ~ 0.8-1.0 μm. Patterning of the aluminium was achieved using photolithography leaving aluminium covering the p^+ and n^+ electrode areas only. Etching of the aluminium was performed using a phosphoric acid/nitric acid solution. Figure 26 (i) shows the device structure after this stage.

The next step was to separate the wafer into the sixteen individual detectors. This was done using a diamond saw. The wafer was covered with photoresist on both surfaces for protection and during sawing a lint-free tissue was placed between the wafer and the metal vacuum chuck for further protection.

4.2.7 Postmetallisation Annealing

To anneal radiation damage caused during the electron beam evaporation of aluminium and to reduce the interface trapped charge density, postmetallisation annealing was carried out. This consisted of a low temperature hydrogen anneal (see section 3.2.6).

4.2.8 Mounting and Wire Bonding

The detectors were mounted in fanout printed circuit boards (PCBs) as shown in figure 29. The PCBs, which were produced at Imperial College, were of area 18 cm × 18 cm and gold-plated copper tracks on the surface fanned out from 250 μm pitch at the centre to standard 40-way connectors at the edge of the boards. Gold-plated copper tracks were present on both sides of the boards to enable wire bonding of both surfaces of the SDCs.

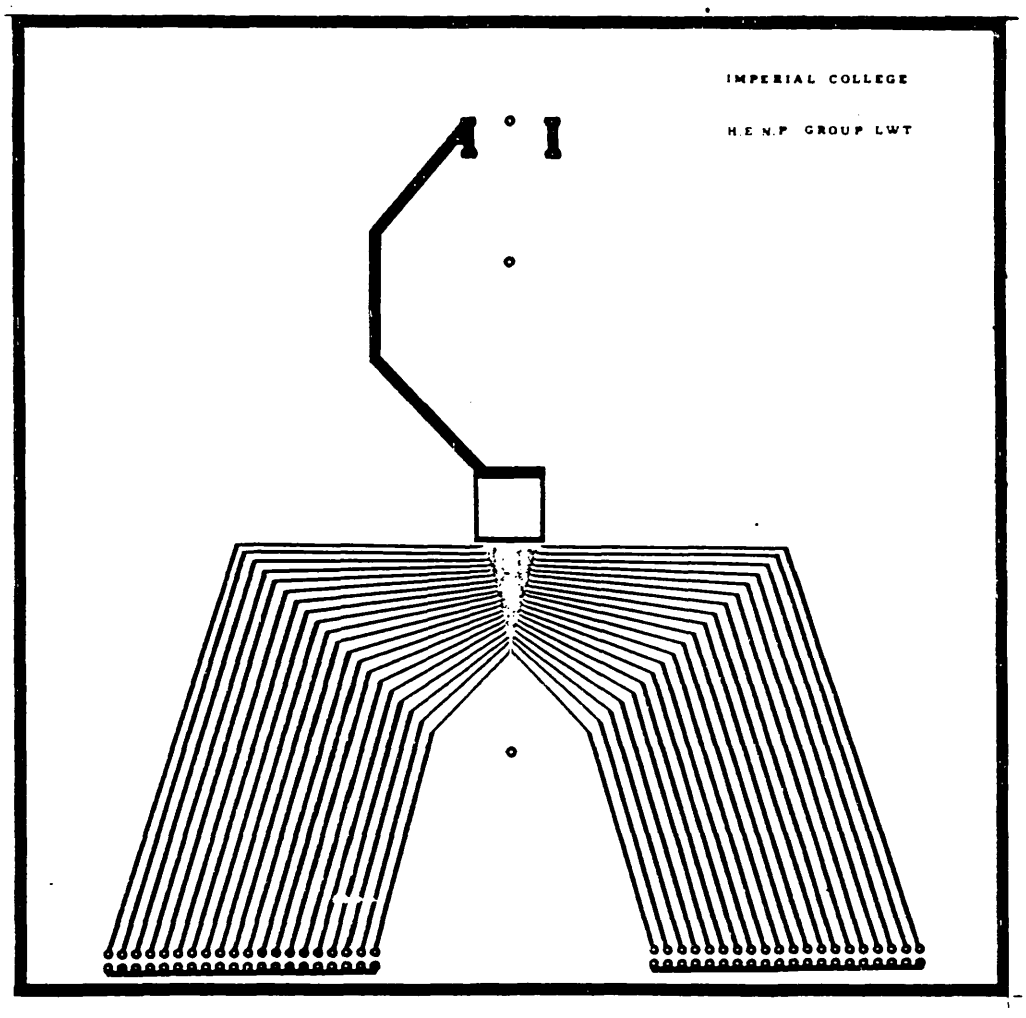


Figure 29: The fan out printed circuit board

Silver loaded epoxy resin was used to mount the SDCs onto the boards since it was readily available in the processing laboratory and was found to be of sufficient bonding strength to withstand the force exerted by the wire bonding tool. The epoxy was cured at 90°C for 3 hours and the PCBs were allowed to cool before wire bonding.

Connection of the SDC electrodes to the gold-plated tracks on the PCB was made with 25 μm aluminium wire using ultrasonic wire bonding.

4.3 DETECTOR EVALUATION AND SELECTION

During the processing, the only method of monitoring and evaluating the electrical properties of the SDCs was by the measurement of leakage currents using a wafer probe. This consisted of a vacuum chuck to hold the wafer and several probe needles which could be gently lowered onto the surface of the wafer by means of a fine adjustment screw thereby avoiding damage to the surface. By this method the leakage current flowing between the n^+ anode and any p^+ electrode on the same surface could be measured. However, since probing of both surfaces at once was not possible, the leakage current between the anode and p^+ electrodes on the opposite surface could not be measured until after wire bonding.

Front surface leakage currents were measured after several steps in the processing of the SDCs. Since the wafer probe was manually operated and each wafer contained 16 × 39 p^+ strips on the front surface, only a small percentage of the strips were tested. The first measurement was performed after the N_2 annealing step. Typical

leakage currents flowing between the anode and a single p^+ electrode on the same surface were approximately 100-300 nA. However, a small proportion of the strips tested had relatively high leakage currents > 1 μA. After metallisation the leakage currents were found to be roughly the same i.e. 100-300 nA per strip. The leakage currents obtained after the postmetallisation anneal were typically 50-200 nA although the high leakage current strips remained > 1 μA.

Selection of the detectors to be mounted onto the PCBs was made on the basis of these leakage current measurements. The most suitable detectors had one or two high leakage current strips out of the total of 39 with the remainder of the electrodes having leakage currents in the lower portion of the 50-200 nA range.

After mounting and wire bonding, the leakage currents were approximately 10 nA per strip. At this stage the leakage currents between the anode and the p^+ electrodes on the opposite surface could be measured. The values obtained were ~ 10 nA per strip.

Chapter V

EXPERIMENTAL TESTS OF SILICON DRIFT CHAMBERS

5.1 THE PROTOTYPE DETECTORS

The two types of design of SDCs produced are depicted in figure 30. The designs of these prototype detectors were made very simple with the initial objective of showing the feasibility of producing drift detectors and demonstrating the drift principle. The design consisted of a series of 40 parallel strips of width 200 μm and length 1 cm, each strip separated from its neighbour by a 50 μm gap. On one side of the high resistivity n-type wafer strips 1 to 9 and strips 11 to 40 were p-type implants to provide the field shaping electrodes and strip 10 was an n^+ implant to act as an anode. On the opposite surface of the wafer two alternative designs were made. In the case of the standard SDC, a similar pattern of p-type implants was made on the back with the only difference being that there was no anode. This design is shown in figure 30 (a). In the second case (figure 30 (b)) the opposite surface consisted of a uniform single-area p-type implant, 1 cm^2 in area. In both designs the total active area was 1 cm^2 and the maximum drift distance was 7.5 mm. The thickness of the detectors was approximately 300 μm.

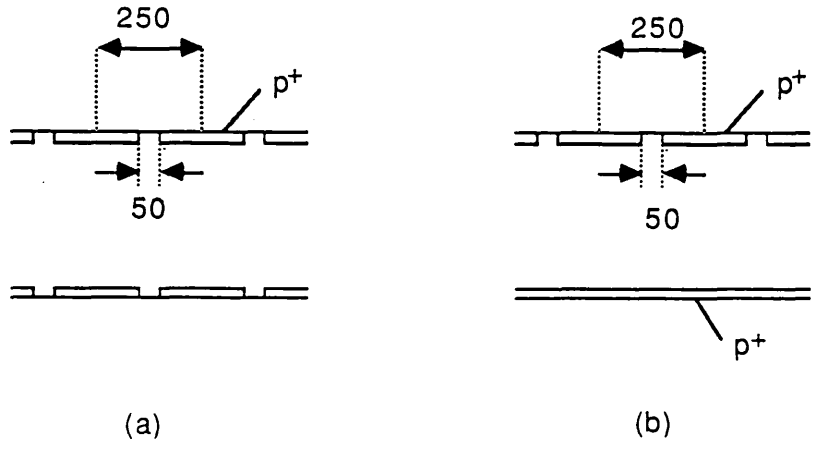


Figure 30: Cross-sections of the SDC designs
(a) Standard design. (b) Single-area p^+ electrode on one side.

5.1.1 Results From the First Prototype SDCs

The first set of prototype SDCs were produced by myself at Micron Semiconductor Limited using the processing steps outlined in chapter 4. Detectors of both the designs described in the previous section were produced. However, due to an error in the metallisation stage of the processing it was discovered that wire bonding of the detectors to the printed circuit boards (PCBs) was only possible for one surface of the detector. This almost certainly arose from the fact that a thin natural oxide existed directly beneath the aluminium on one surface of the detector as a direct consequence of the processing error. This problem could only be overcome in the case of those detectors which had a uniform p-type implant on one surface. The electrodes on the anode side of these detectors were connected to the PCB by ultrasonic wire bonding while a contact was made to the other surface by bonding a wire onto it using silver-loaded epoxy. This could not be achieved with the detectors of the other design

since the electrodes were only 200 μm wide and handling of the epoxy could not be controlled on this scale. Thus, only those SDCs with a uniform p-type implant on one surface were bonded to the PCBs and available for experimental tests in the laboratory.

5.1.2 Leakage Currents

The detector leakage current is one of the limiting factors of the energy and position resolution since it contributes to the total electronic noise.

Several measurements of the leakage currents flowing in the detectors have been made using two SDCs with uniform implants on the surface opposite the anode. The first measurements made were those of the current flowing between the anode and a single p-type electrode with the whole detector biased. With a reverse bias of 50 V (detector over-depleted - see next section) the leakage currents of the electrodes were found to be the same for 38 out of 39 strips on each detector and equal to approximately 1-2 nA. The remaining strip had a significantly larger leakage current of > 1 μA. These results were expected on the basis of experience with microstrip detectors. For example, the value observed for the NA14 microstrip detectors (which have a similar strip area and detector thickness) was ~ 3 nA per strip.

Measurements were also made of the reverse bias current flowing between the anode and the single area p-contact on the reverse side of the detectors. The variation of this leakage current with the reverse bias voltage for the two detectors is shown in figure 31.

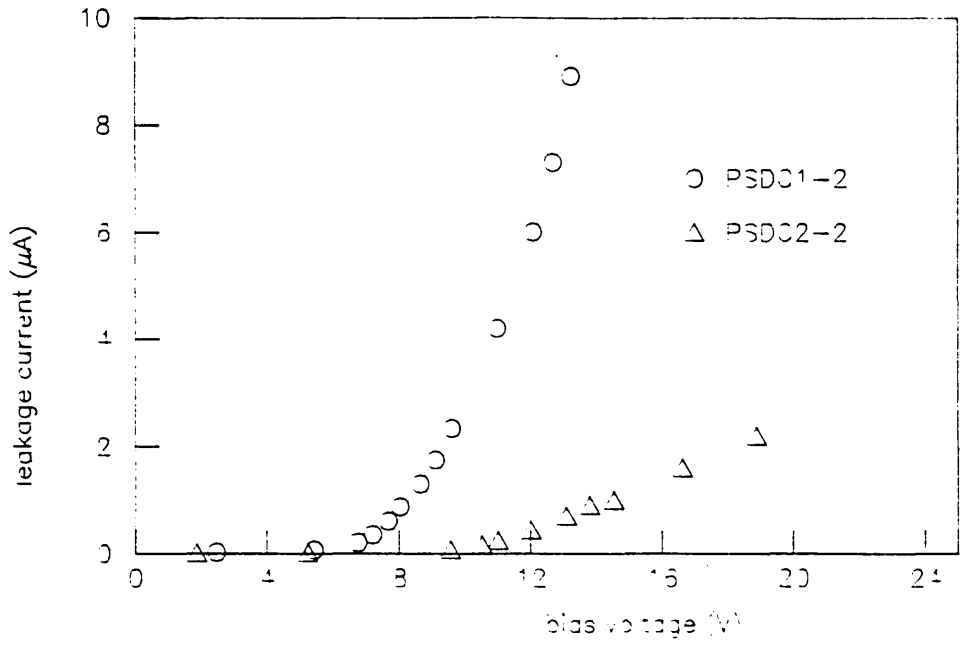


Figure 31: Leakage current of the single-area p^+ electrode versus bias voltage for two SDCs.

The current starts to rise rapidly at a reverse bias of only 7-10 volts and because of this the total leakage current of these detectors under operating conditions was rather high. The total anode current was about 3 μA.

5.1.3 Capacitance Characteristics

To provide evidence for full depletion of SDCs the capacitance characteristics must be studied. The expected behaviour of the capacitance between all the p^+ electrodes connected together and the anode as the bias voltage is increased is illustrated in figure 32.

For voltages below depletion, the capacitance is essentially that of two standard detectors in parallel. As the bias voltage approaches the

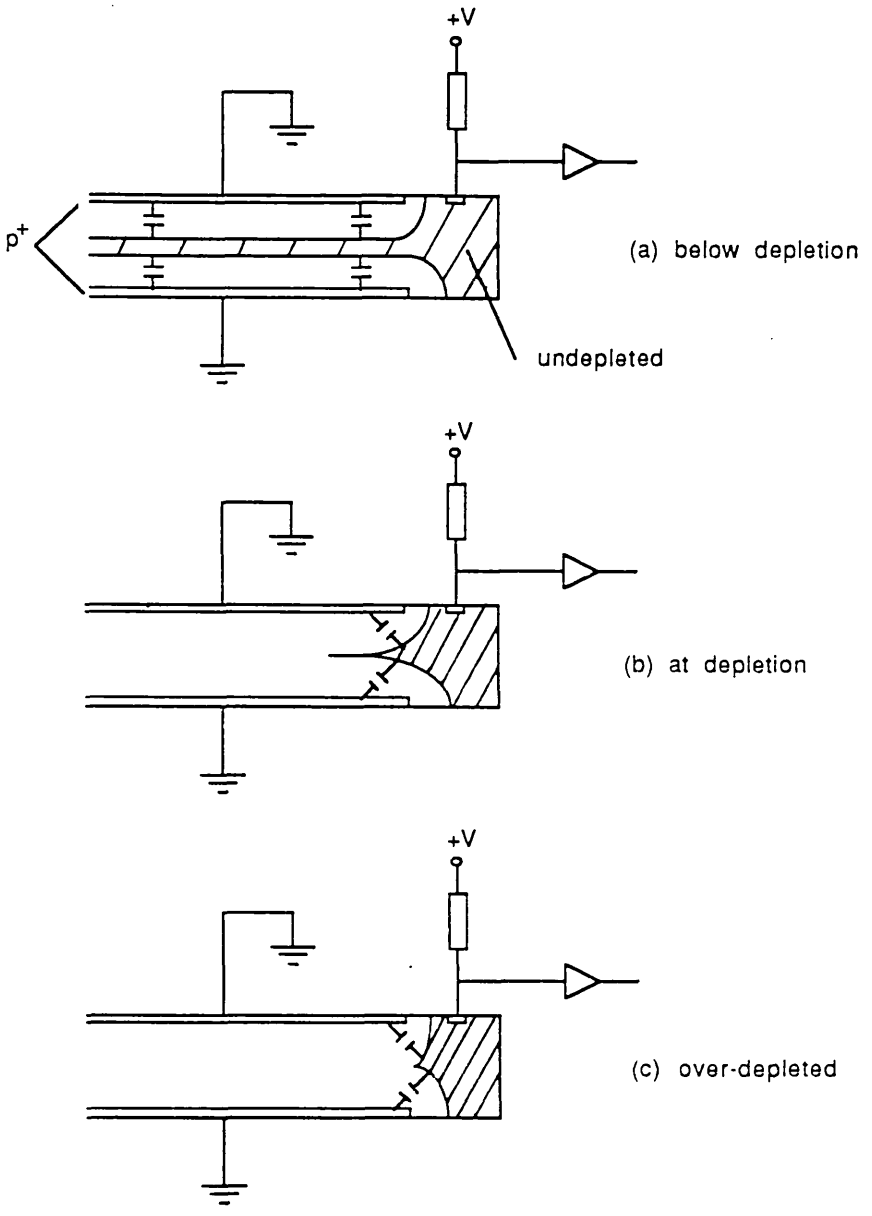


Figure 32: Capacitance between all p^+ electrodes and the anode

total depletion voltage, the conductive channel retracts and the capacitance drops abruptly. The remaining value is constant and equal to the much smaller geometrical capacitance between the anode and the surrounding electrodes.

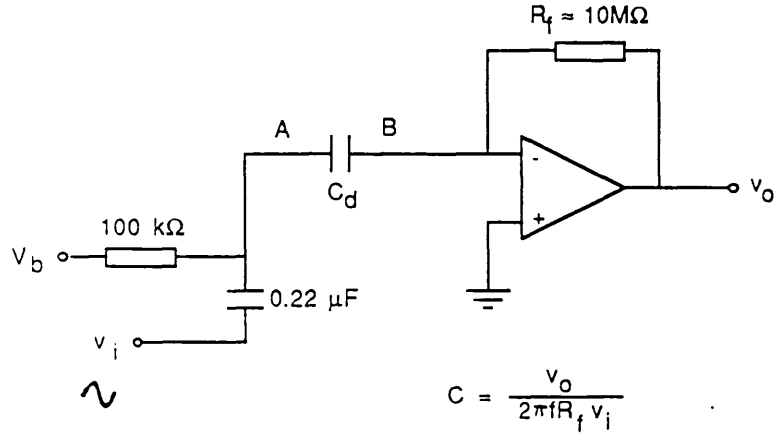


Figure 33: Circuit used for capacitance measurements

The capacitance-voltage characteristics of the SDCs were measured using the operational amplifier circuit of figure 33. The detector is represented by the capacitance C_d connected between points A and B in the circuit. At various values of the bias voltage, the capacitance was measured by using a digital multimeter to determine the ratio of the rms output voltage v_o to the rms input voltage v_i :

$$C_d = \frac{v_o}{2\pi f R_f v_i}$$

The detector was biased such that the anode was kept at ground (point B) while all the p^+ electrodes on both surfaces were connected together and held at a negative potential $-V_d$. The set-up is shown in figure 34.

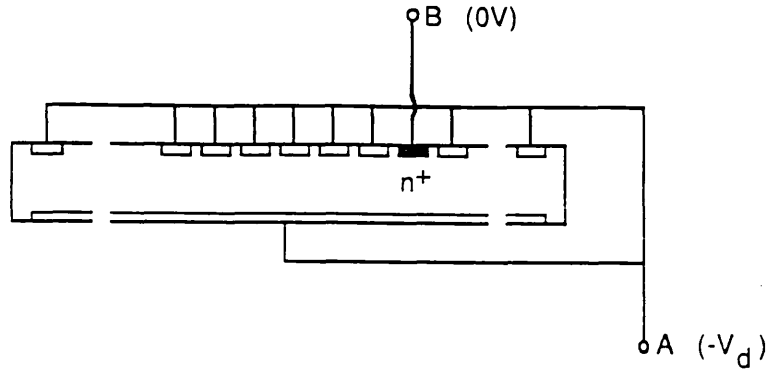


Figure 34: Biasing arrangement for the CV measurements

Figure 35 (a) shows the CV curve obtained for a prototype silicon drift chamber. At bias voltages below depletion, the capacitance decreases with increasing potential due to the enlarging depletion layers. The expected sharp drop in capacitance is observed at about 10 V and this value is in agreement with the value calculated on the basis of the detector resistivity and thickness. However, the capacitance drops to ~ 175 pF which is much higher than the value expected. At depletion the geometric anode capacitance is expected to be about 1 pF.

These results were interpreted in the following way. The sudden drop in the capacitance at ~ 10 V was due to a pinch-off of the conducting channel in the anode region only. Further from this region there is no field to allow thermally generated electrons to flow out of the potential gutter. Thus electrons will tend to accumulate in the potential gutter forming a thin band of undepleted silicon at the

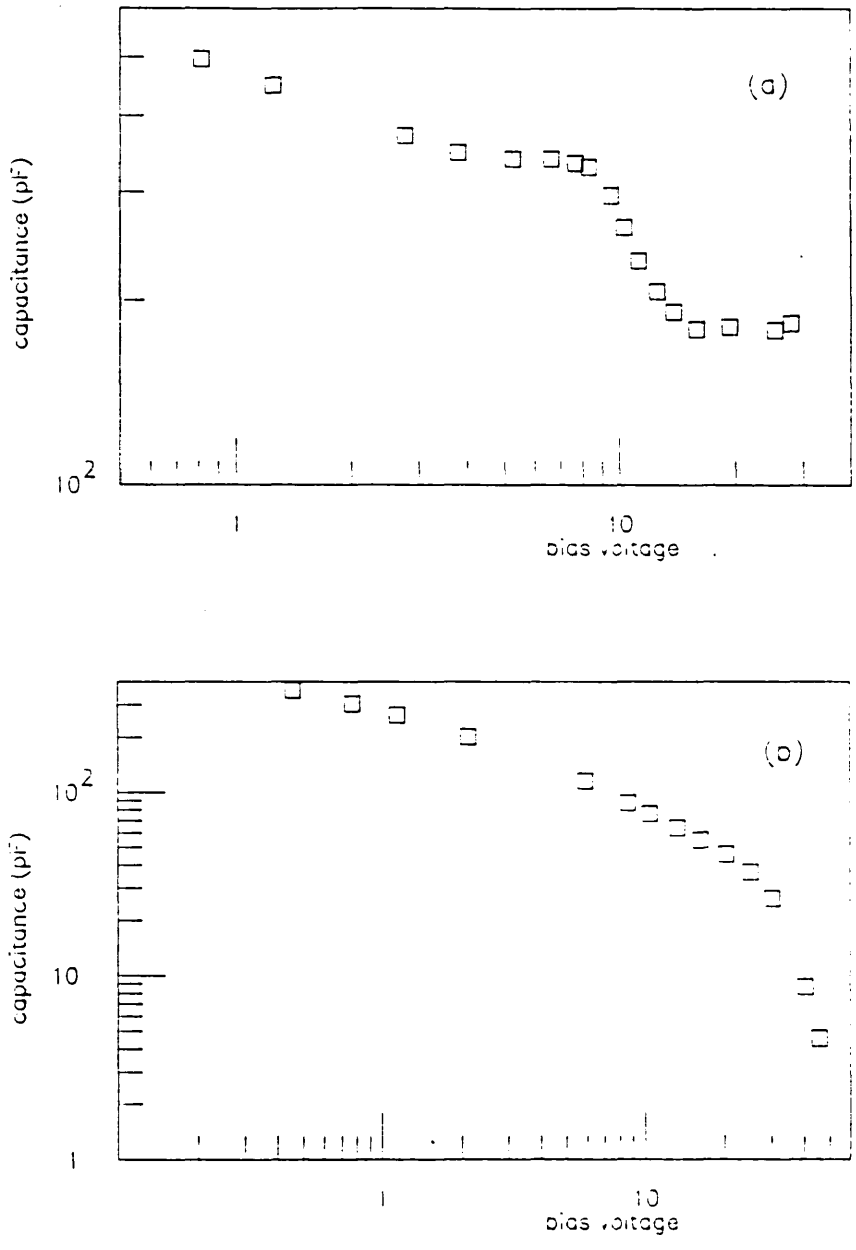


Figure 35: Measurements of two capacitance characteristics of the SDC. (a) Capacitance between all p^+ electrodes connected together and the anode vs. bias voltage. (b) Capacitance between the single-area p^+ electrode and the anode vs. bias voltage.

centre of the detector extending away from the anode in both directions as shown in figure 36 (a). The diagram shows the situation for an SDC with strips on both sides. The argument holds just as well for the SDC with a uniform p^+ implant on one surface, although the potential minimum (and hence the band of undepleted silicon) is no longer in the centre of the detector but moves linearly from the anode to the opposite surface as shown in figure 36 (b). Because of capacitive coupling, the effect of this band of undepleted silicon is to make an additional contribution to the overall measured capacitance, as was observed.

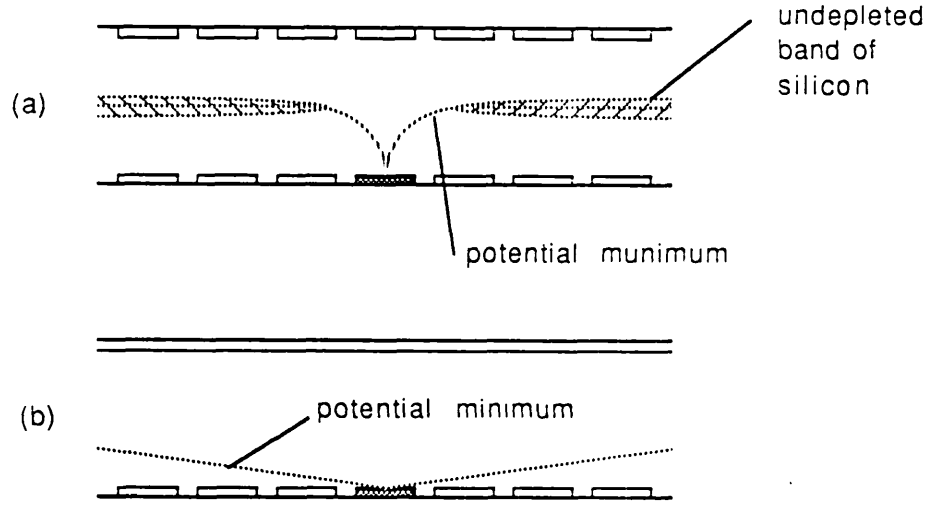


Figure 36: Interpretation of the capacitance measurements (a) Cross-section through a silicon drift chamber showing the thin band of undepleted silicon at the centre. (b) Potential minimum in an SDC with a single-area p^+ electrode on one side.

A second measurement made was that of the capacitance between the anode and the uniform single-area p^+ contact on the opposite surface. The p^+ strips on the same side as the anode were all kept at ground. The biasing arrangement was as shown in figure 37. In this case no potential gutter exists within the detector since the depletion mechanism is analogous to that in a standard p^+n junction detector. Hence bands of undepleted silicon are not expected to exist inside the detector under sufficiently high bias voltages, resulting in a fully depleted detector with no 'residual' capacitance.

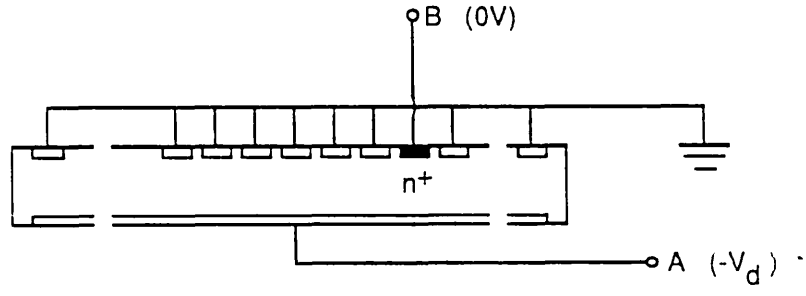


Figure 37: Biasing arrangement for CV measurement of figure 35(b)

Figure 35 (b) shows the CV curve obtained for this measurement. As can be seen the anode capacitance drops to a very small value when the detector becomes fully depleted at around 40 V. This indicates the absence of any bands of undepleted silicon within the detector, as expected.

5.1.4 Observation of Signals From β Particles

The drift behaviour has been observed using β particles. Electrons from a Ru^{106} β source were incident on the SDC and a prompt trigger on minimum ionising βs was provided by a scintillator beneath the detector. The detector was connected to an ORTEC 142A charge sensitive preamplifier. The preamplifier output was shaped and amplified by an ORTEC 474 amplifier with adjustable shaping time constants and variable gain. This amplifier acts as a CR-RC filter and differentiation and integration time constants of 0.2 μsec were used which resulted in an equivalent noise charge of $\sigma \sim 2200$ electrons. Timing of the output signal was achieved by a constant fraction discriminator which provided a STOP pulse for the time-to-amplitude converter (TAC). The START pulse was provided by the discriminated photomultiplier tube output signal. The output of the TAC was split in two with one output being discriminated and delayed to provide a 0.2 μsec gate to a LeCroy 2259 peak voltage sensing ADC. A diagram of the electronics chain is given in figure 38.

Signals in the detector due to the electrons from the (uncollimated) β source which passed through the SDC, producing a prompt signal in the scintillator, were observed. The signals were delayed with respect to the trigger pulse and this could be attributed to the delays caused by electrons drifting along the SDC to the anode.

Figure 39 shows the time spectrum obtained. The detector was biased such that the anode was kept at ground and the single area p^+ electrode was at -17.2 V. The drift field was provided via a

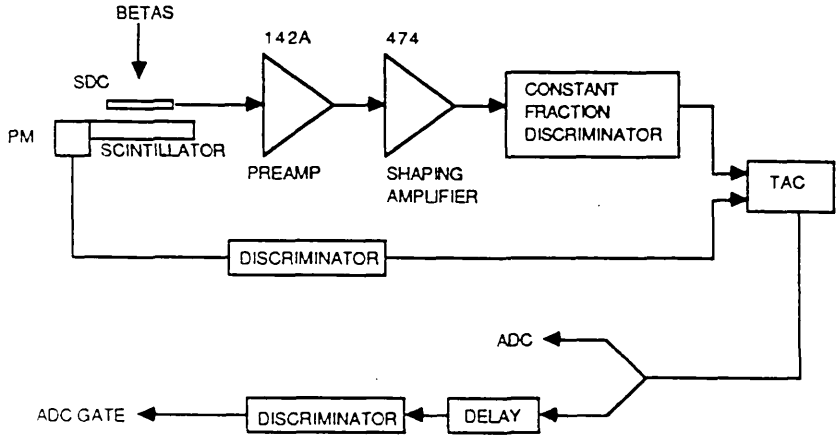


Figure 38: Electronics chain used for timing measurements

potential divider circuit such that the strips next to the anode were at -16.2 V and each successive strip towards the edge of the detector was decremented by -3.2 V. Since the strip pitch was 250 μm the drift field was therefore 128 V/cm. The maximum drift field applied was limited by the high leakage currents of these detectors.

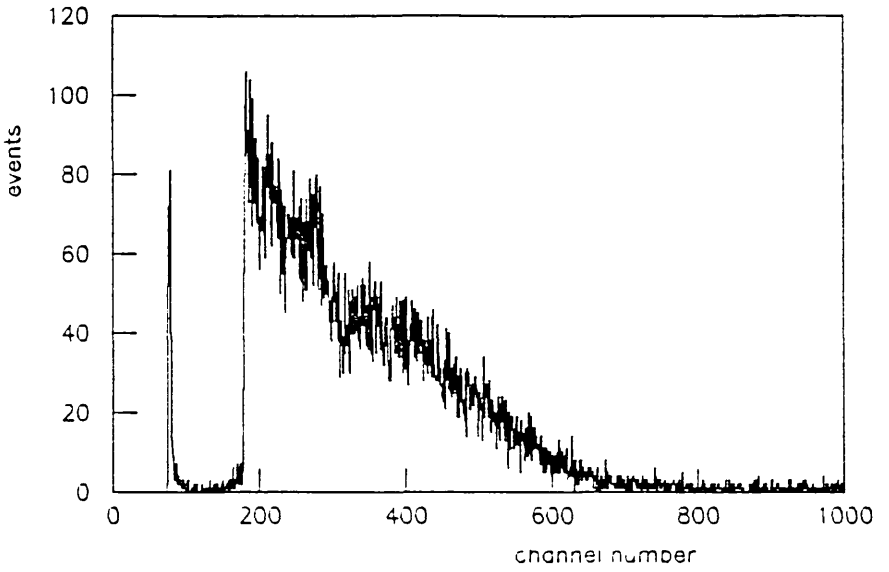


Figure 39: Time spectrum of signals in the SDC

5.1.5 Pulse Heights and Noise

The variation in the pulse height has been studied using the set-up shown in figure 40.

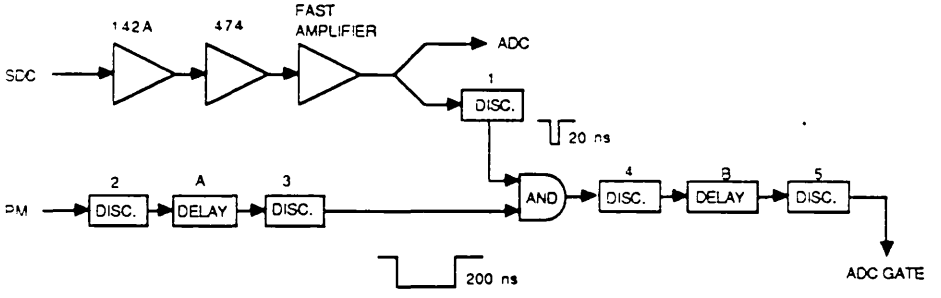


Figure 40: Electronics chain used for pulse height measurements

The silicon drift chamber was irradiated with β particles from the Ru^{106} source and a fast trigger was provided by the scintillator placed below the SDC. The trigger pulse from the photomultiplier tube was discriminated and delayed by an amount τ_A to provide a gate of width 200 nsec which was used to sample the output pulses from the SDC at varying delays τ_A. A fast amplifier was used to provide extra gain for the SDC signal. The output was split in two with one output being discriminated to provide a NIM pulse of duration ~ 20 nsec. This was done by ANDing the 200 nsec gate with the short 20 nsec pulse from discriminator 1. The output from the AND gate was discriminated and delayed to provide a gate to a LeCroy 2259 peak voltage sensing ADC.

Figure 41 shows the pulse height spectra obtained with six different values of the delay τ_A. A clear Landau type peak is visible in all the spectra and the peak ADC channel is seen to decrease as the delay time increases. The peak channel for τ_A = 100 nsec corresponds to an equivalent of 23550 electrons deposited in the silicon drift chamber .

The corresponding variation in the pulse height with delay time is plotted in figure 42. This shows a clear trend in decreasing pulse height as the delay time becomes longer - for a delay time of 2.5 μsec the pulse height was one half its maximum value of approximately 24000 electrons at τ_A = 0.

The results of figure 42 have been attributed to small regions of undepleted silicon inside the detector. Consider a standard SDC with p^+-implanted strips on both surfaces (the argument also holds for the

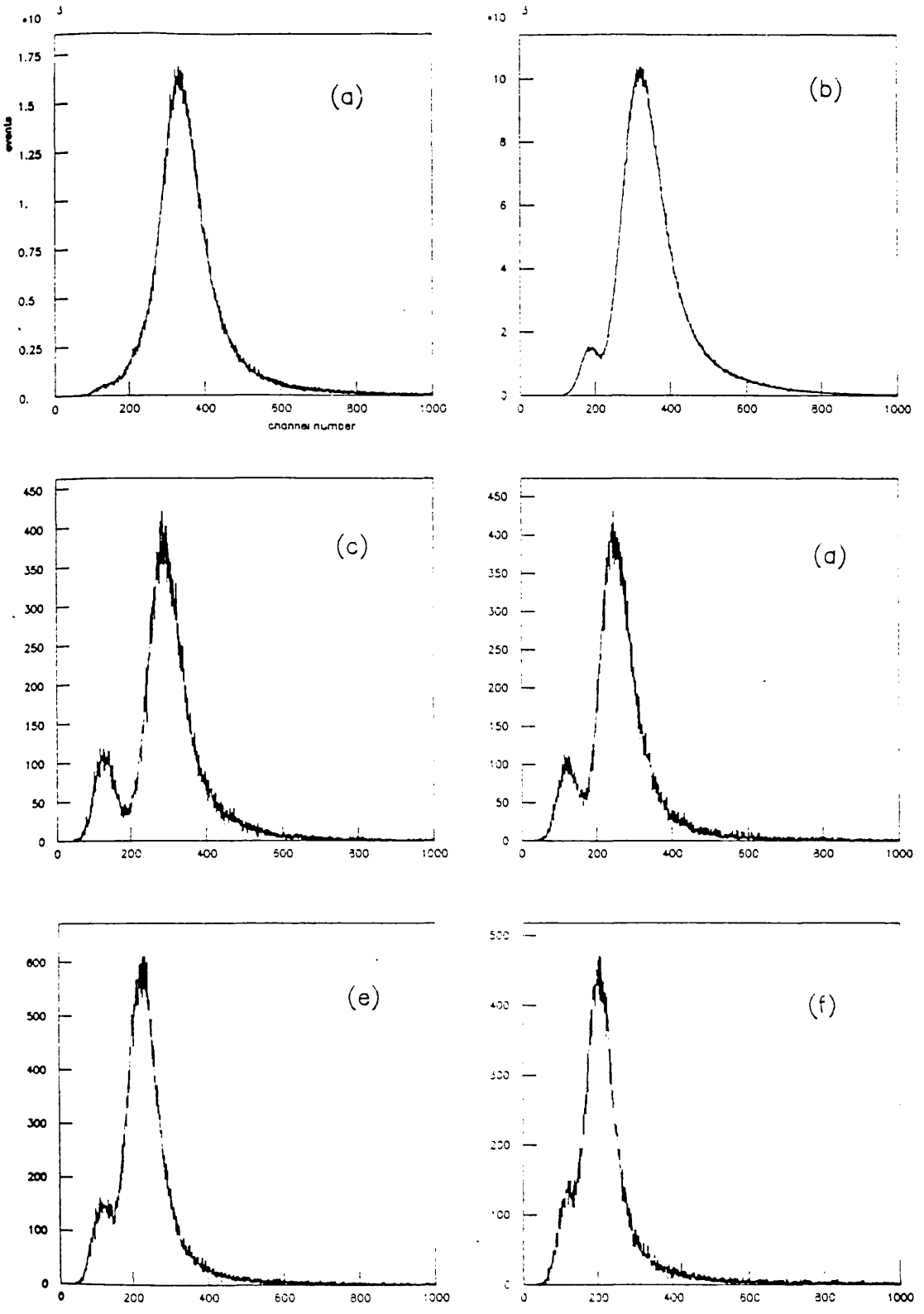


Figure 41: Pulse height spectra for various time delays (a) 100 ns, (b) 500 ns, (c) 1.0 µs, (d) 1.5 µs, (e) 2.0 µs, and (f) 2.5 µs.

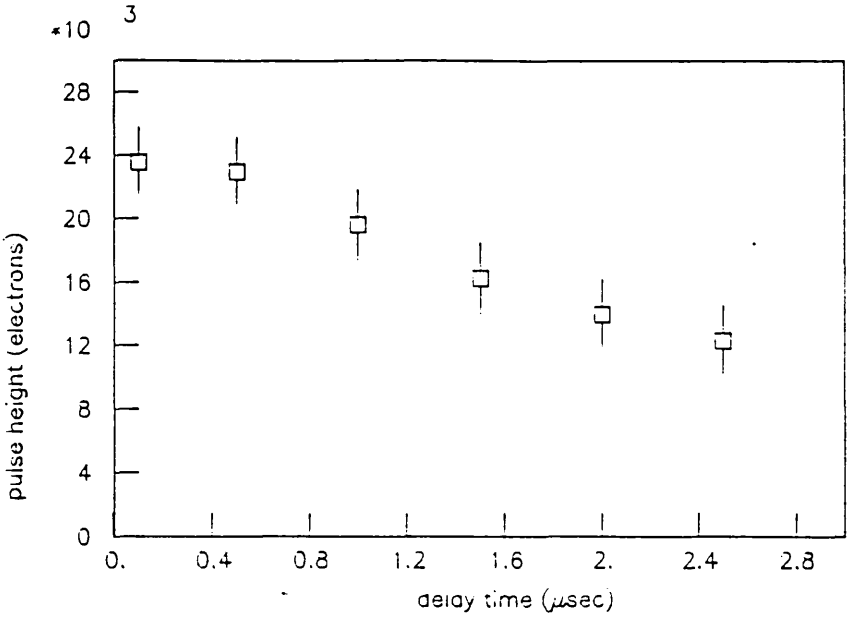


Figure 42: Pulse height as a function of time delay

SDC with a single-area p^+ implant on one surface). Computer simulations (see chapter 6) and subsequent experimental measurements (this chapter) have provided evidence for the existence of a periodic variation in the potential minimum. The effect of these 'undulations' in the potential is to produce small areas along the centre of the silicon wafer which act as potential wells for electrons (see, for example, figure 43).

These potential wells along the detector are approximately adjacent to the oxide regions as shown in figure 44 and the presence of positive oxide charge enhances the effect. Since these 'pockets' act as potential wells for electrons they may be expected to be undepleted and results of the capacitance measurements of section 5.2.1 indicate that this is so.

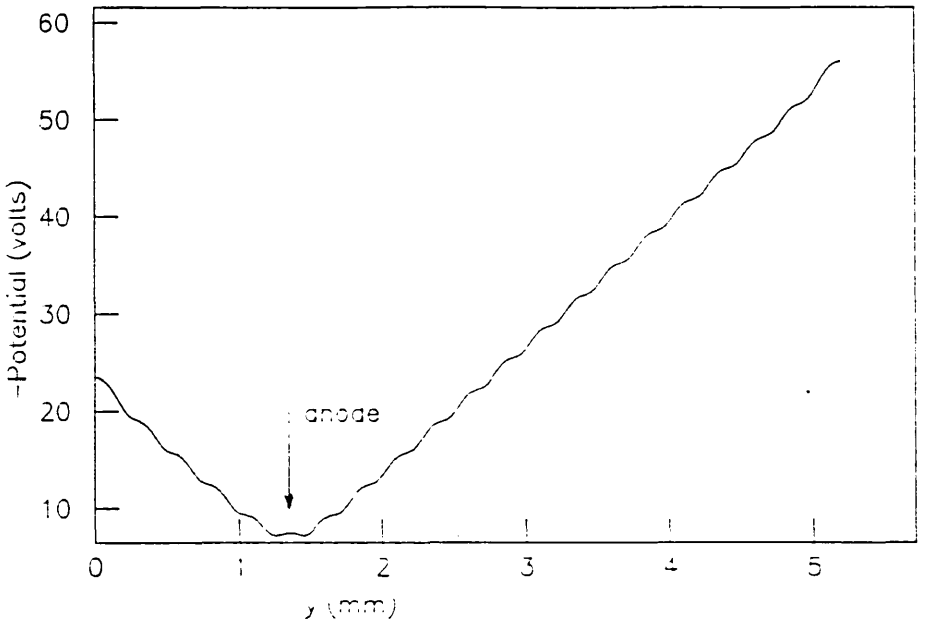


Figure 43: Undulations in the potential minimum at the centre of a silicon drift chamber.

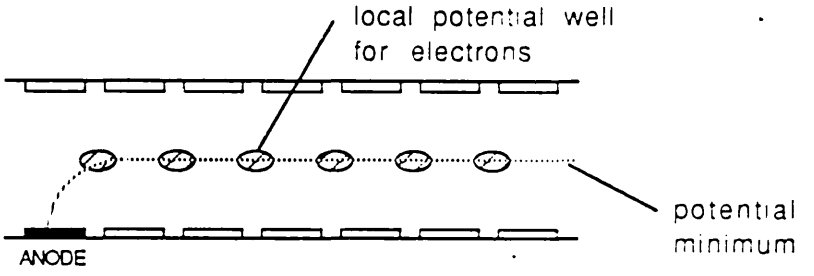


Figure 44: Pockets of undepleted silicon within the detector

Electrons generated by the passage of a charged particle drift along the detector towards the anode following a drift path determined by the position of the potential minimum which is depicted by the

dashed line in figure 44. During drift along this path, the electrons will inevitably encounter the undepleted pockets and since these act as potential wells some of the electrons may get trapped. This leads to a loss of signal charge as observed in the pulse height measurements. For longer drift distances (and hence longer drift times) more electron wells are encountered by the charge cloud during its drift to the anode and therefore a greater loss of charge is expected. This is seen as a reduction in the measured pulse height and this picture is consistent with the observations made.

The energy resolution of the system was estimated by obtaining a pulse height spectrum when the SDC was exposed to gammas from a sealed 14 mCi americium-241 source whose principal emission is at 59.5 keV.

Figure 45 shows the spectrum obtained. The lower peak is the remnant of the pedestal while the upper peak is the 59.5 keV γ-line. The asymmetry in this peak is due to the significant proportion of events with reduced pulse height resulting in more events contained in the low energy side of the peak. To estimate the energy resolution the high energy part of the γ peak was fitted to a Gaussian distribution. The fitted Gaussian was centred on 59.0 keV. The energy resolution obtained from the fit was σ = 8.0 keV (= 2220 electrons).

The major contribution to the noise was the high anode leakage current of the SDC.

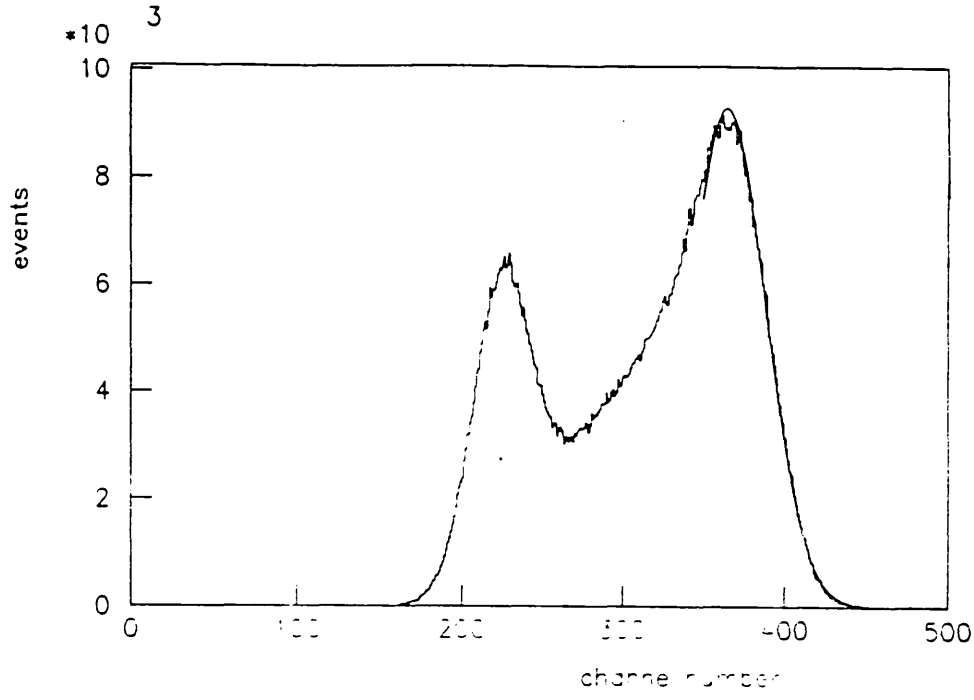


Figure 45: Am^{241} γ spectrum obtained with an SDC showing the 59.5 keV γ line. Also plotted is the result of a Gaussian fit to the high energy part of the peak.

5.2 THE SECOND SET OF PROTOTYPE DETECTORS

Since the total anode current under moderately low applied drift fields was rather high for the prototype detectors, it was decided to go ahead with the fabrication of a second set of prototypes with the same design. The hope was that the experience gained during the processing of the first SDC prototypes would provide the basis for an improvement in the overall fabrication techniques of the second set. The new detectors were produced by Micron Semiconductor Ltd. using the same set of photolithographic masks and the same processing plan used previously. Both designs of SDC, as described in section 5.1, were produced and wire bonding of the detectors was

successfully carried out at Micron. The following sections describe the improved performance of this set of detectors as indicated by the experimental tests carried out at Imperial College.

5.2.1 Capacitance Measurements

The first measurement carried out was that of the capacitance between all the p^+ electrodes connected together and the anode. A variation of the capacitance measuring circuit of figure 33 was used. All the p^+ electrodes were connected together and a reverse bias V_b was applied as shown in figure 46 (a). The CV characteristics obtained are shown in figure 46 (b). The sharp drop in capacitance as expected for these devices occurs at around V_b = -20 V. This indicates a depletion voltage for the full 300 μm thickness of $4V_b$, i.e. 70-90 V giving a resistivity of 3.3-4.2 kΩcm. This agrees with the expected value - the n-type silicon used was supplied by Topsil Semiconductor Materials [36] with specifications for the resistivity ρ = 3629-4456 Ωcm. At V_b = 70 V, well over the expected depletion voltage, the capacitance was measured to be 40 pF. This is still much larger than the expected geometrical anode capacitance of ~ 1 pF and only 6 pF of this could be accounted for by the stray capacitance (not subtracted from the plotted results). C_{stray} was measured with an approximate accuracy of 3 pF.

Further insight into these capacitance measurements was obtained by computer simulations of the SDCs. Computer modelling of the devices was done using the programs described in chapter 6. Poisson's equation was solved for a 2-dimensional SDC by a relaxation

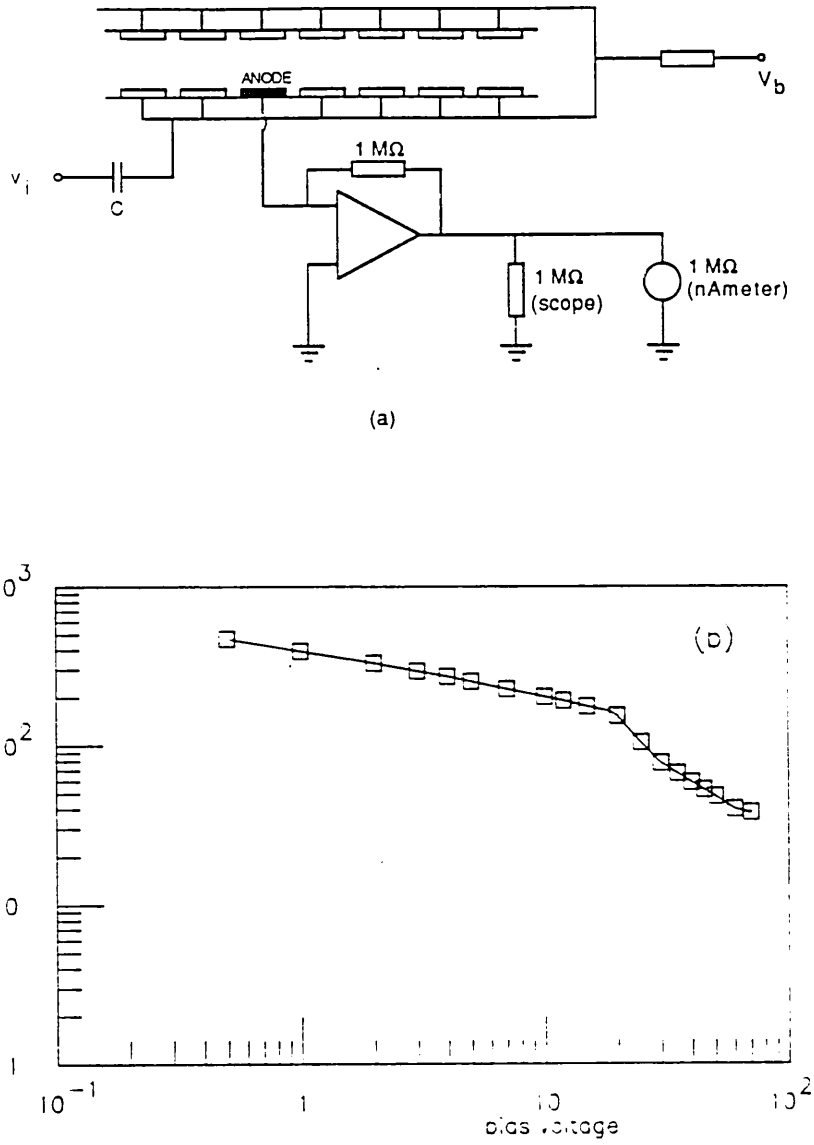


Figure 46: Measurement of the capacitance characteristics (a) Biasing arrangement. (b) Capacitance between all p^+ electrodes and the anode vs. bias voltage.

method so that the potential distributions within the detector could be calculated. The results showed (see figure 43) that for a detector of

strip pitch 250 μm and strip width 200 μm there existed a periodic variation of the potential minimum in the centre of the detector. These 'undulations' in the potential minimum were further enhanced by the presence of oxide charge. It was also found that the size of these undulations varied with the applied drift field and for sufficiently high fields they become insignificant.

The computer modelling thus suggested that under certain conditions significant undulations of the potential minimum occurred giving rise to a series of local potential minima for electrons along the centre of the detector. Therefore small areas of undepleted silicon were expected to exist along the centre and these undepleted 'pockets' could, via capacitive coupling, make an additional contribution to the overall measured capacitance.

Figure 47 (a) shows the arrangement used for the measurement of the CV characteristics of the SDC with an applied drift field. The detector was biased using an external resistor chain with the bias voltage V_b applied to strip 1. On both surfaces strips 11-19 were maintained at identical potentials to those of strips 1-9 while strips 20-40 were held at a potential equal to V_b. The strip opposite the anode was biased independently - initially it was allowed to float and finally its potential was raised to -80 V. The arrangement was such that when V_b was -100 V the potential of strip 9 (next to the anode) was -20 V at which point full depletion was expected. The results are plotted in figure 47 (b).

The behaviour of the anode capacitance is in agreement with the model described above. The gradual decline of the capacitance with

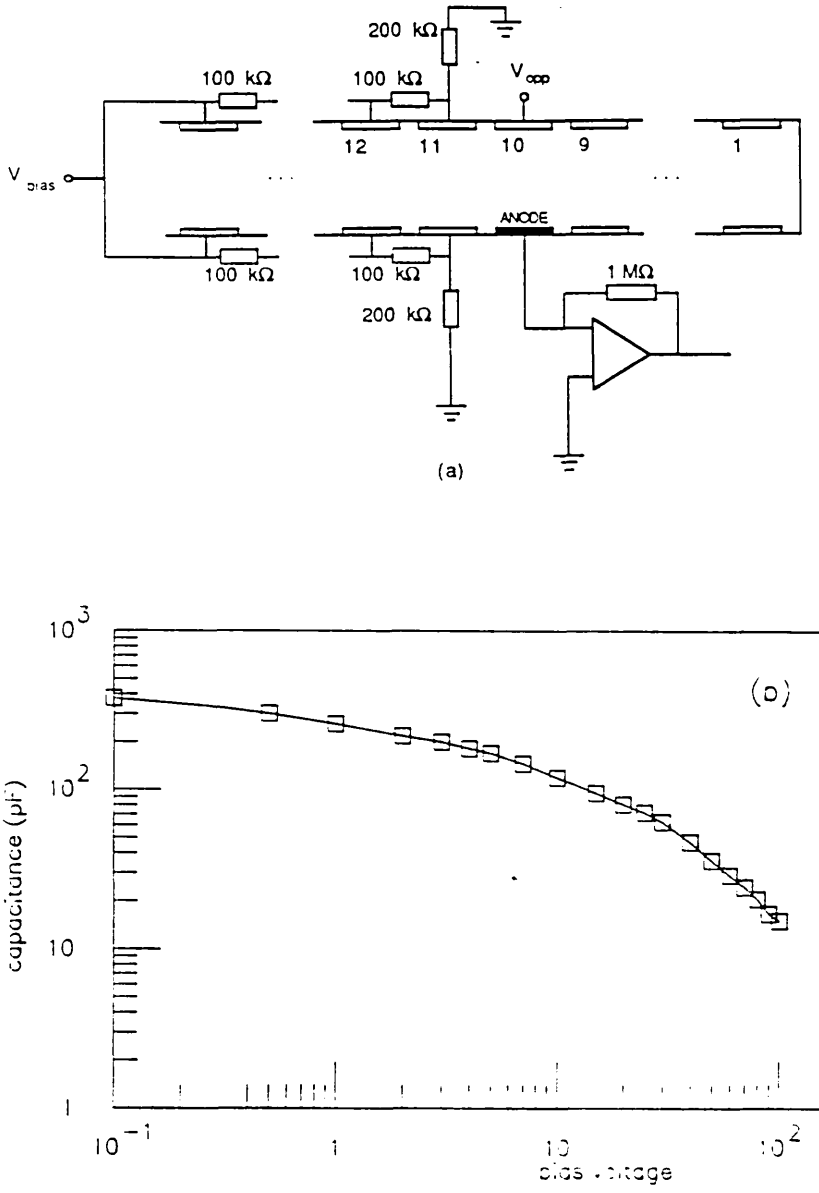


Figure 47: CV characteristics of an SDC with applied drift field (a) Biasing arrangement. (b) Capacitance between all p^+ electrodes and anode with an applied drift field.

increasing V_b is due to a gradual reduction, in the y-direction, of the central undepleted region in the SDC. At V_b = -100 V the drift field was approximately 390 V/cm which is sufficient to almost

completely eliminate the undulations in the potential minimum and hence the undepleted pockets along the centre of the SDC. Accordingly the capacitance at this point was very small.

5.2.2 Leakage Current and Noise

To determine the constraints due to the reverse bias current of the SDC the total anode leakage current was measured. Figure 48 shows a plot of the anode current versus bias voltage where the same voltage V_b was applied to all the p^+ electrodes. The leakage current follows the expected behaviour - at low bias voltages it varies roughly as $V_b^{\frac{1}{2}}$ showing that the generation current is the dominant component. The overall magnitude of the leakage current was significantly less than the currents observed in the first prototype SDCs, and this was probably due to the improvement in processing. Under operating conditions the total anode current was approximately 600 nA.

The SDCs were read out in the same way as in section 5.1.4, using an ORTEC 142A preamplifier followed by an ORTEC 474 shaping amplifier. The rms noise at the output of the 474 was measured using a RACAL-DANA rms voltmeter. Calibration was achieved by injecting a known test pulse into the ORTEC preamplifier. The equivalent noise charge at the input was found to vary between σ = 1350-1600 electrons under varying operating conditions. The contribution expected from the 600 nA leakage current with 200 nsec shaping time constant is σ = 1180 electrons. Thus the anode leakage current was still the major contributor to the noise.

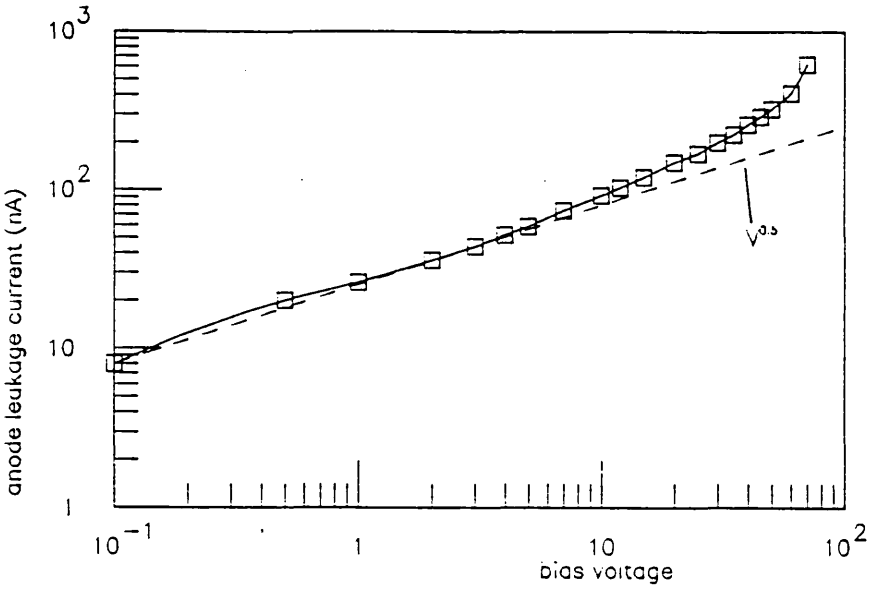


Figure 48: Anode leakage current vs. bias voltage

5.2.3 Observation of Drift Using a Collimated β Source

Drift action of the SDCs was initially investigated using a collimated Sr^{90} β source. This consisted of a thick aluminium holder containing the Sr^{90} source and a 5 mm thick brass collimator in which a 200 μm diameter hole was drilled.

The detector was biased using an external resistor chain as shown in figure 49. The bias voltages were applied such that the average increment in potential per strip was 5.5 V corresponding to a drift field of 220 V/cm.

The experimental arrangement is shown in figure 50. By fixing the Sr^{90} source and brass collimator to an XY-table the β source could be scanned along the surface of the detector so that the β electrons crossed the SDC at different distances from the anode.

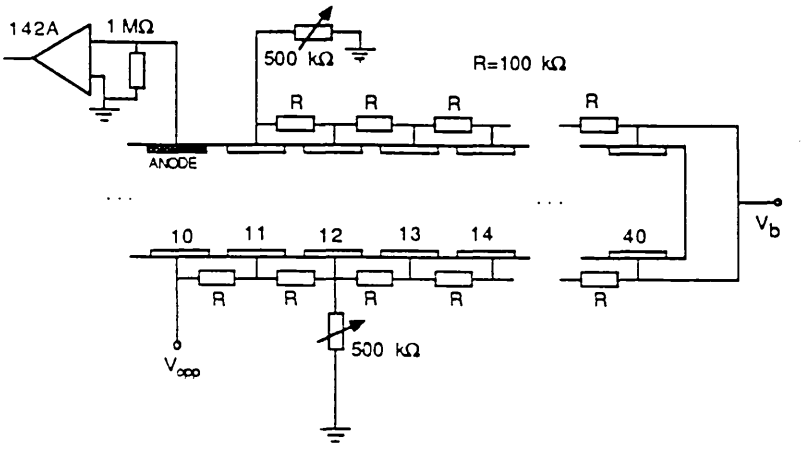


Figure 49: Biasing arrangement for observation of drift action

After crossing the SDC the electrons entered a fast scintillator which was used to produce a prompt trigger pulse. The electronics chain used was identical to that shown in figure 38.

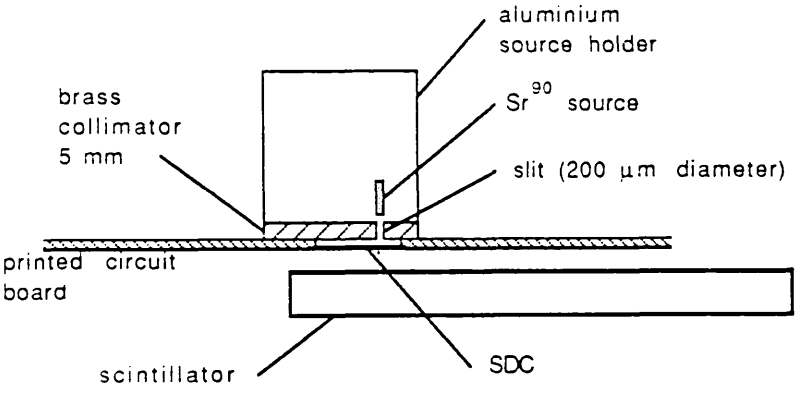


Figure 50: Experimental set up for observation of signals

As the β source was moved along the detector a clear correlation was observed between the source position and the average time of the pulses from the SDC. Figure 51 shows the waveforms from the output of the 474 shaping amplifier on the scope. The scope was triggered by the lower trace which shows the output signal of the scintillator after it had been discriminated. Waveforms are shown for three different positions of the collimator. In figure 51 (a) the collimator was 4.5 mm from the anode. In figure 51 (b) the collimator was moved 1.0 mm towards the anode and the peak of the waveform has clearly moved by approximately 300-400 nsec. Figure 51 (c) shows the waveform for a position of 0.5 mm from the anode.

Figure 52 shows the corresponding time spectra obtained. The distributions appear to be approximately Gaussian in shape with $\sigma \sim$ 100 nsec. This is equivalent to ~ 300 μm of drift distance and is a consequence of multiple Coulomb scattering of the βs in the detector. Results were obtained for positions of the collimator ranging over the whole active length of the detector and the observations were in agreement with the expected drift behaviour.

Figure 53 shows the results in the form of a distance-time plot and the approximate linearity of the detector over a wide range of drift distances is evident. Also shown is the result of a computer simulation of the SDC with the same drift field of 220 V/cm. The comparison between the experimental data and the predictions of the computer simulation shows good agreement between the two. The drift velocity found by a least-squares fit to the linear portion of the curve was found to be 3.0 μm/nsec compared to the expected value of

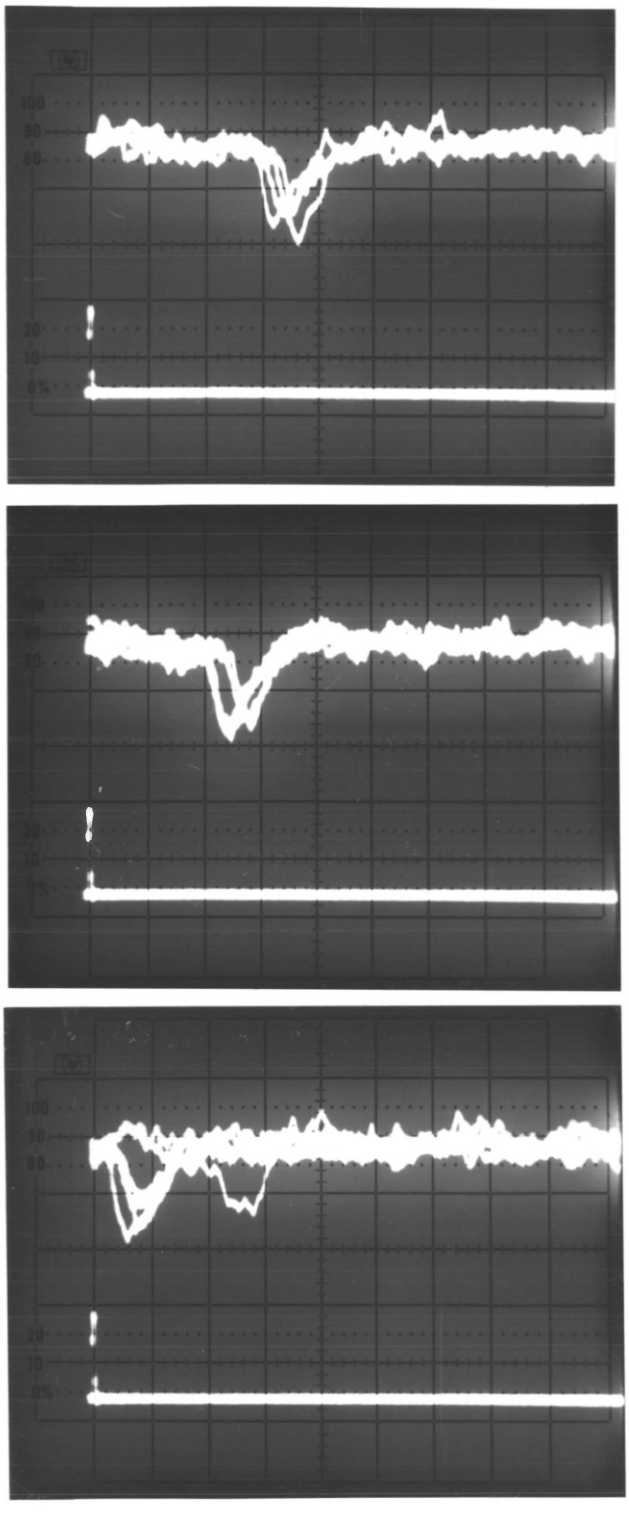


Figure 51: Waveforms at the output of the shaping amplifier for drift distances of (a) 4.5 mm, (b) 3.5 mm and (c) 0.5 mm. The scope was triggered on the scintillator pulse (lower trace). The timebase was 0.5 μsec/div and the voltage scale was 0.5 V/div on all traces.

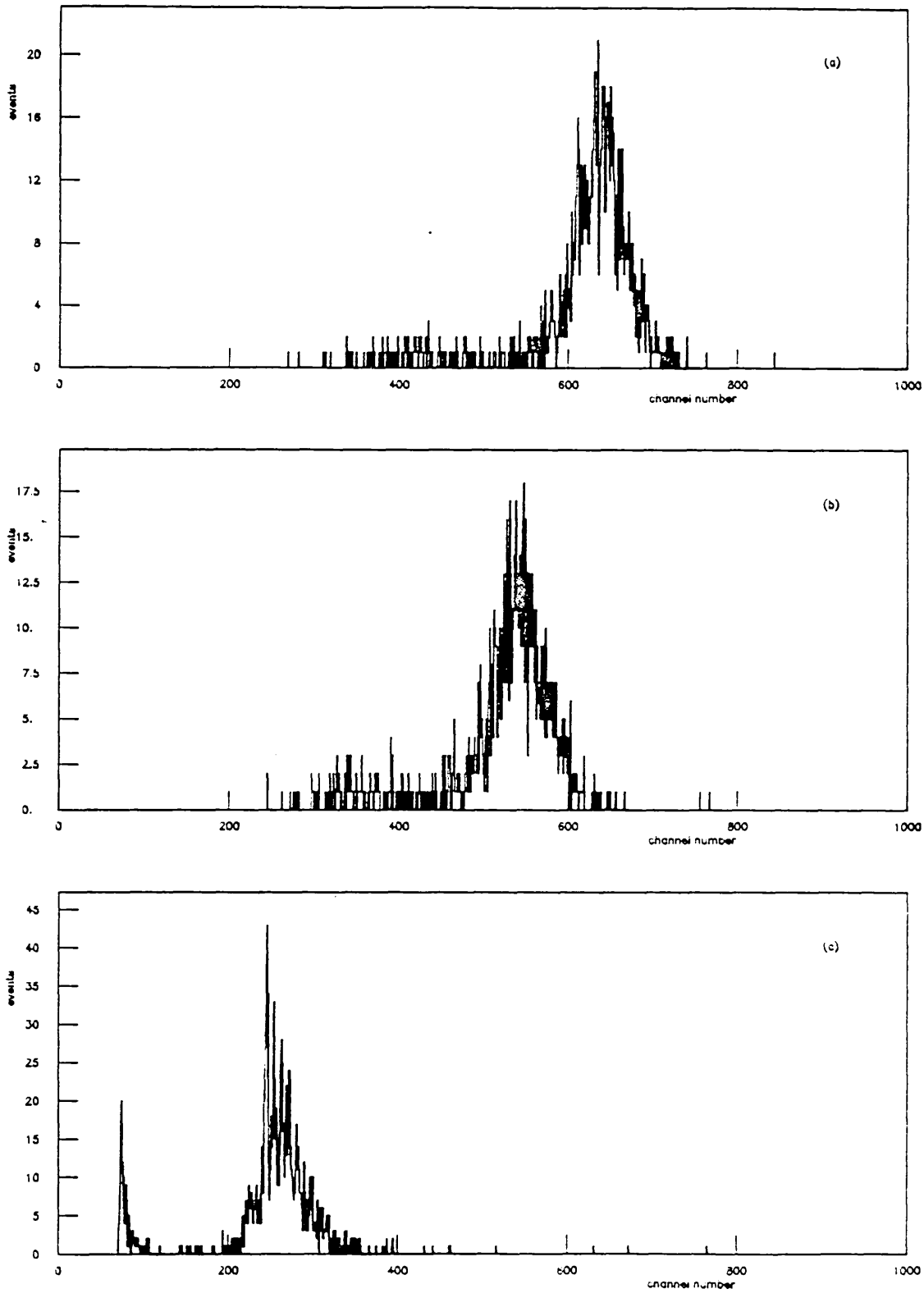


Figure 52: Time spectra of pulses in the SDC
for drift distances of (a) 4.5 mm, (b) 3.5 mm and (c) 0.5 mm.

3.2 μm/nsec calculated from $v_d = \mu_n E_{drift}$ where the electron mobility was assumed to be 1450 $cm^2V^{-1}s^{-1}$.

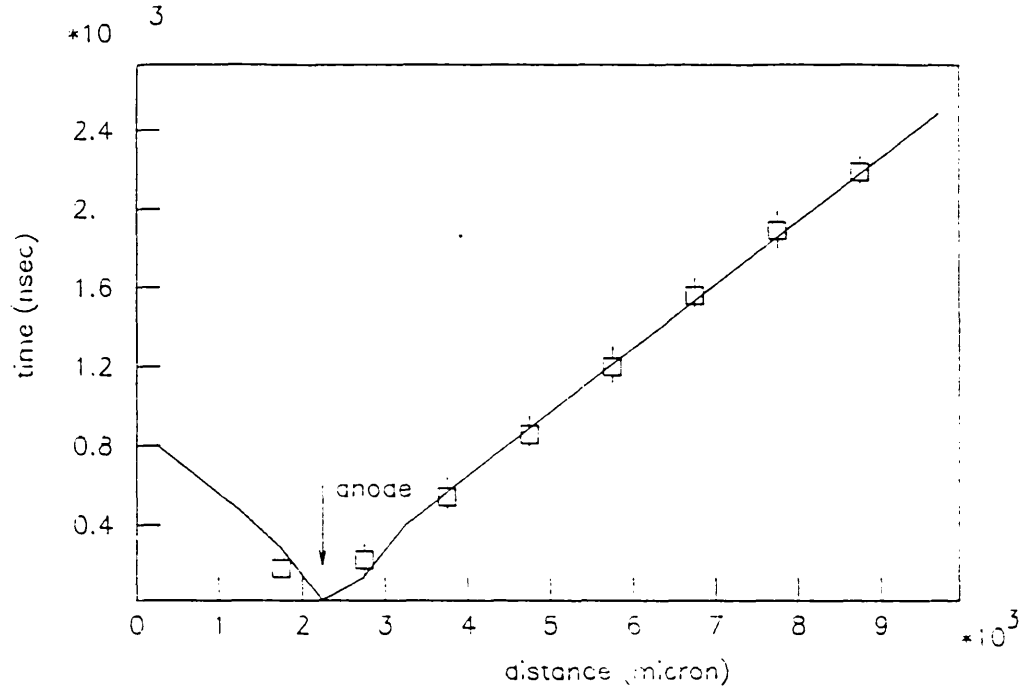


Figure 53: Drift time as a function of drift distance
The squares represent the experimental data and the solid line is the result of a computer simulation.

Chapter VI

ANALYSIS AND SIMULATION OF SILICON DRIFT CHAMBERS

6.1 INTRODUCTION

This chapter presents an outline of the methods used to model the electrical behaviour of SDCs. The aim was to predict some of the important properties of the detectors so that experimental results could be compared with a theoretical model. Modelling and simulations also provided valuable pointers towards the improved SDC designs described in section 6.4.

The basic physical description of the electrical behaviour of semiconductor devices consists of a set of coupled non-linear differential equations [12]. Poisson's equation

$$\nabla^2\phi = -\rho/\varepsilon \;\; ; \;\; \rho = q\,(p - n + N_D^{+} - N_A^{-}) \qquad (6.1)$$

describes the situation under equilibrium conditions.

Here

ϕ = electrostatic potential

ρ = charge density

ε = permittivity of silicon

q = elementary charge

p = concentration of holes

n = concentration of mobile electrons

N_D^{+} = concentration of ionised donors

and N_A^+ = concentration of ionised acceptors. When bias voltages are applied currents will flow in the device and these can be described by the current-density equations

$$J_n = q\, n\, \mu_n\, E + q\, D_n\, \nabla n$$
$$J_p = q\, p\, \mu_p\, E + q\, D_p\, \nabla p \qquad (6.2)$$

and the continuity equations,

$$\nabla \cdot J_n - q\,(\partial n/\partial t) = q \cdot R$$
$$\nabla \cdot J_p - q\,(\partial p/\partial t) = -q \cdot R \qquad (6.3)$$

where J_n, J_p are the electron and hole current densities respectively, μ_n, μ_p are the carrier mobilities, E is the electric field, D_n, D_p are the carrier diffusion constants and R describes the net generation ($R < 0$) or recombination ($R > 0$) of electrons and holes.

Although the above equations can be used to describe semiconductor devices, simplification of the problem is often necessary since the physics involved is rather complex. For the modelling of the SDCs the problem was simplified by assuming that the concentrations of electrons and holes (due to e-h creation by thermal generation and ionising particles) in the detector were small enough to be ignored. This can be justified since the charge densities which arise from these two contributions are less than, or at least comparable with, the density of ionised donors in a fully depleted detector. Thus the mobile electrons and holes are not expected to greatly affect the electric field distribution in the detector, although a small local perturbation may be expected. Thus $J = \nabla \cdot J = 0$ and the problem is reduced to solving Poisson's equation with the correct

boundary conditions. A further assumption was that the detector was fully depleted so that the charge density in the bulk consisted of the density of ionised donors only (n-type detector). Thus

$$\rho = q \cdot N_D \qquad (6.4)$$

Since there is no electric field in the z-direction (figure 54) the problem is essentially 2-dimensional. Although Poisson's equation can be solved analytically in one dimension it is far more difficult in 2-dimensions and so a numerical method was used.

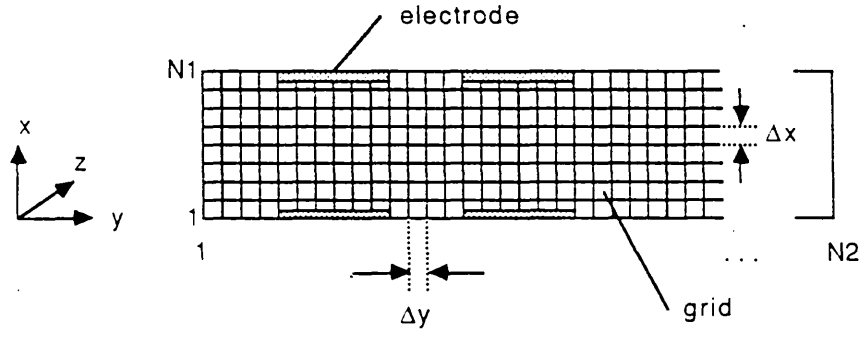


Figure 54: Schematic representation of a silicon drift chamber showing the grid lines used for the numerical solution to Poisson's equation.

6.2 DESCRIPTION OF THE SIMULATION PROGRAMS

6.2.1 Solution for Electrostatic Field and Potential

The numerical method used consisted of first expressing Poisson's equation as a set of simultaneous linear equations on a finite grid in coordinates x and y [31]. Discretisation yields

$$\nabla^2\phi_{i,j} = \frac{\phi_{i+1,j} - 2\phi_{i,j} + \phi_{i-1,j}}{(\Delta x)^2}$$

$$+ \frac{\phi_{i,j+1} - 2\phi_{i,j} + \phi_{i,j-1}}{(\Delta y)^2} = -\rho_{i,j}/\varepsilon$$

or $a_{i,j}\phi_{i,j-1} + b_{i,j}\phi_{i-1,j} + c_{i,j}\phi_{i,j}$

$$+ d_{i,j}\phi_{i+1,j} + e_{i,j}\phi_{i,j+1} = -\rho_{i,j}/\varepsilon \qquad (6.5)$$

where $a_{i,j} = e_{i,j} = 1/(\Delta y)^2$

$$i = 1,2,3,\ldots,N1$$

$b_{i,j} = d_{i,j} = 1/(\Delta x)^2$

$$j = 1,2,3,\ldots,N2$$

and $c_{i,j} = -2/[(\Delta x)^2+(\Delta y)^2]$

The set of equations (6.5) can then be expressed as a matrix equation

$$M\Phi = Q$$

where M is the (N1 × N2) matrix of coefficients (a,b,c, etc.), Φ is the unknown electrostatic potential column vector and Q is the known charge density (× ε^{-1}) column vector. The latter was equal to $\rho_{ij}/\varepsilon = qN_D/\varepsilon$ where the concentration of ionised donors was obtained from

$$qN_D = 1/(\mu_n\rho)$$

The carrier mobilities were taken from published values [37]. The system is solved iteratively, from a starting approximation $\Phi^{(1)}$, by the formulae [38]

$$R^{\langle n\rangle} = Q - M\Phi^{\langle n\rangle}$$

$$MS^{\langle n\rangle} = R^{\langle n\rangle}$$

$$\Phi^{\langle n+1\rangle} = \Phi^{\langle n\rangle} + S^{\langle n\rangle}$$

$R^{(n)}$ is the residual of the n^{th} approximate solution $\Phi^{(n)}$ and $S^{(n)}$ is the up-date change vector. For the starting approximation $\Phi^{(1)}$ the potentials at each grid point were set to the values of the 1-dimensional solution for each j. Convergence was based on both the maximum residuals and on the maximum change made to the values of Φ [38]. Convergence parameters of R < 0.005 V and S < 0.01 V were found to be suitable [39].

At the detector edges j = 1 and j = N2 the boundary conditions applied were

$$d\phi/dy = 0$$

At the detector surfaces the boundary conditions were of the form

$$\text{at } x = 0, \quad \phi(x) = V_1$$

$$\text{at } x = d, \quad \phi(x) = V_2$$

where V_1 and V_2 are the bias voltages for the relevant strip. For points at the Si-SiO_2 interface the boundary conditions applied were

$$E_x = d\phi/dx = -Q_f/\varepsilon \quad \text{at } x = 0$$

$$= +Q_f/\varepsilon \quad \text{at } x = d$$

where Q_f is the oxide fixed charge density.

6.2.2 Electron Drift Paths

The motion of charges generated by ionising radiation in the detector was modelled assuming that the presence of these charges does not perturb the electric field. This assumption can be supported by considering an ionising particle which gives rise to 10^4 electrons and holes deposited in a cylinder of radius r ~ 5 μm and length l = 300 μm. The resulting electron charge density is $\rho = 10^4/(\pi r^2) \sim 0.4$

10^{12} cm^{-3} compared to N_D ~ 1.0 10^{12} ionised donors / cm^{-3} in a typical detector.

The components of velocity of an individual electron for given electric field components were obtained by interpolation from the data of Canali et al. [37]. These data were based on experimental measurements of the drift velocity as a function of the electric field. For low fields (E_x, E_y < 1.5 kV/cm) the dependence is approximately linear so that $v_x = \mu_n E_x$ and $v_y = \mu_n E_y$ where the mobility is constant μ_n = 1450 $cm^2 V^{-1} s^{-1}$. The drift time was defined as the time difference between the generation of a charge and its arrival at the anode. This is a reasonable assumption provided the drift distance is large since nearly all of the signal is induced when the charge is under the anode.

By generating charges at various points in the detector the electron drift paths and an estimation of the drift distance-time relationship were obtained.

6.2.3 The Shape of the Output Signal

Initial experiments with the prototype SDCs using minimum ionising β particles indicated that the pulse height decreased as the drift time increased (see section 5.1.5). To discover if diffusion of the drifting electron cloud could produce this effect modelling of the output signal from SDCs was performed. Thus the final part of the detector simulation was the calculation of the signal at the anode and the pulse shape at the output of the shaping amplifier. Charges generated in the SDC by an ionising particle were assumed to be uniformly

distributed along the linear track of the particle. Each charge, treated separately, was tracked as it drifted along the detector. The contribution to the output signal was calculated on the basis of the charge induced on the anode by the moving charge. The total signal was the sum of these contributions.

The effect of diffusion is to spread the charge cloud radially in space. The charge distribution is Gaussian with the rms radius of the charge cloud given by

$$\sigma = \sqrt{(2Dt)}$$

where t is the time and D is the diffusion constant for electrons $D = (kT/q)\mu_n$. Diffusion was simulated by adding random increments dx and dy to the electron position after every 5 μm of drift. Thus dx = RND * $\sqrt{(2Ddt)}$ where RND is a normally distributed random number with mean zero and $\sigma = 1$ and dt is the drift time corresponding to 5 μm of drift. Effects of the mutual repulsion of electrons were not considered.

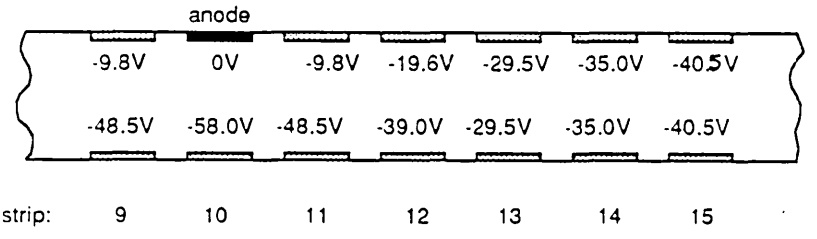
To obtain the pulse shape at the output of the the shaping amplifier the signal current distribution i(t) was convolved with the impulse response of the amplifier. Since the ORTEC 474 acts as a CR-RC filter the impulse response used was [40]

$$f(t) = (t/\tau) \exp(-t/\tau)$$

where both time constants were assumed to be equal to τ.

6.3 RESULTS OF THE SIMULATIONS OF SDCS

Simulations were performed for various detector geometries under several operating conditions. Figure 55 shows a silicon drift chamber with electrode pitch and width 250 μm and 200 μm respectively. In the drift regions, away from the anode, a voltage increment of 5.5 V per strip was used so that the drift field was 220 V/cm. The other detector parameters are defined in the figure.



strip pitch = 250 μm
strip width = 200 μm
thickness = 300 μm
resistivity = 5.2 kΩ cm
oxide fixed charge = 1.0 10^{10} cm^{-2}
40 strips on each surface

drift field = 220 V/cm
voltage increment per strip = 5.5V

Figure 55: Parameters used for the simulation of the SDC

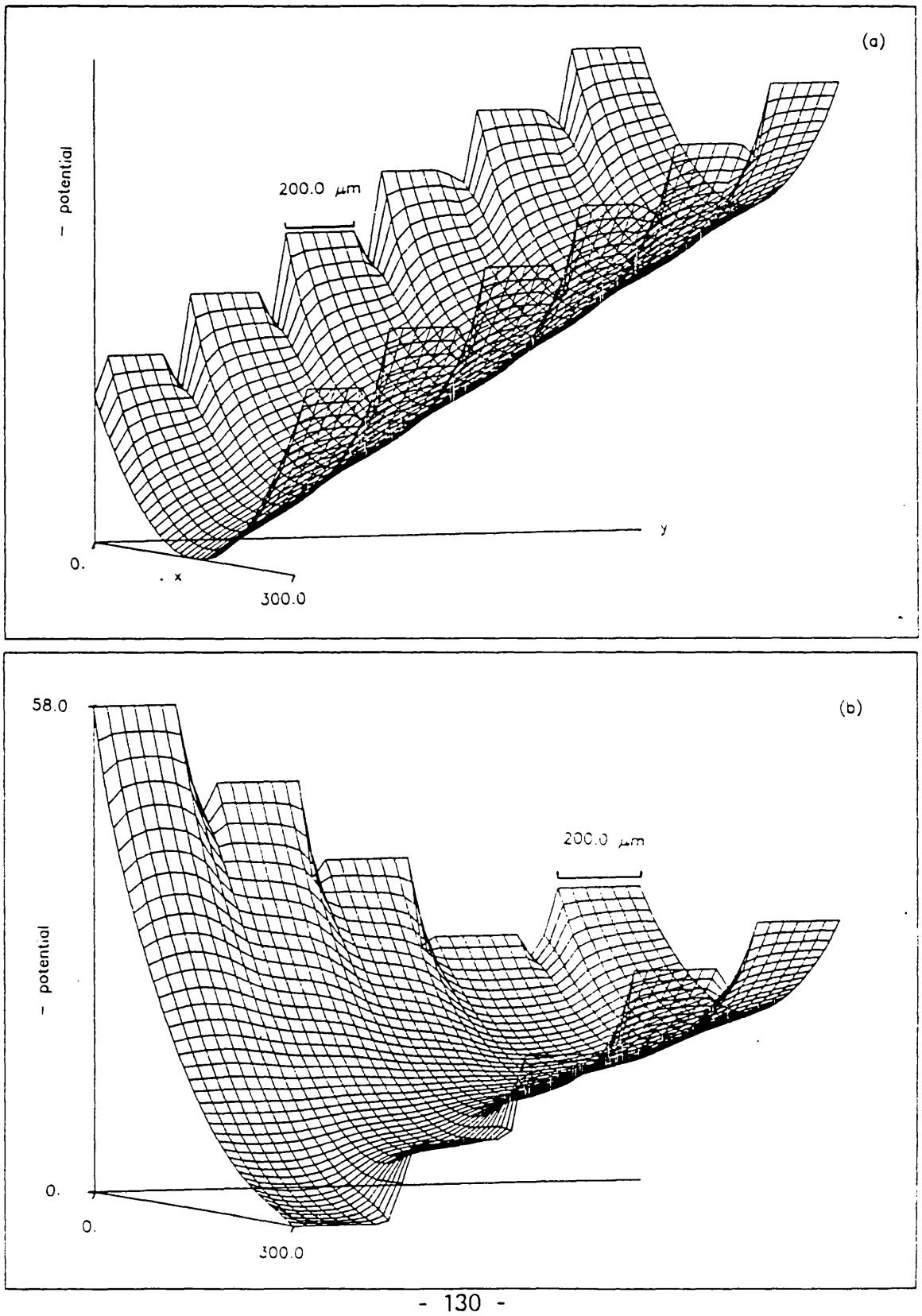
Figure 56 represents contour plots of the electrostatic potential for electrons (i.e. $-\phi(x,y)$) in two regions of the detector. Figure 56 (a) shows the potential for a section of the detector in the drift region. The existence of the potential minimum or 'gutter' is evident.

The gutter is inclined in the y-direction so that electrons drift along the detector towards the anode. Due to the biasing arrangement on strips 10 - 13 (anode region) the potential minimum is shifted from the centre of the wafer (x = d/2) at strip 13 to the anode surface (x = d) at the anode, strip 10 (figure 56). At strips 11 and 12 the potential minima are approximately at x = 5d/6 and x = 2d/3 respectively.

Figure 57 shows the calculated drift paths in the SDC for charges generated at both surfaces of the detector. It is evident from the figure that electrons first drift in the x-direction to the potential minimum at the centre of the detector and then drift in the y-direction along the line x = d/2 until they approach the anode region. Here the potential is shifted towards the surface (x = d) so that electrons are finally collected at the anode.

Figure 58 shows a plot of the drift time versus distance. In the drift regions the drift time varies linearly with distance as expected since the constant drift field gives rise to a uniform drift velocity. In the anode region the electric field is no longer constant and so linearity does not hold. The conditions for this simulation were chosen to resemble closely the experimental conditions described in section 5.2.3 where the delay time was measured as a function of drift distance. The experimental data (plotted as squares in figure 58) show good agreement with the simulated time-distance relation as shown in the plot.

Figure 56: Calculated potential distribution in the SDC
(a) in the drift region and (b) in a region close to the anode.



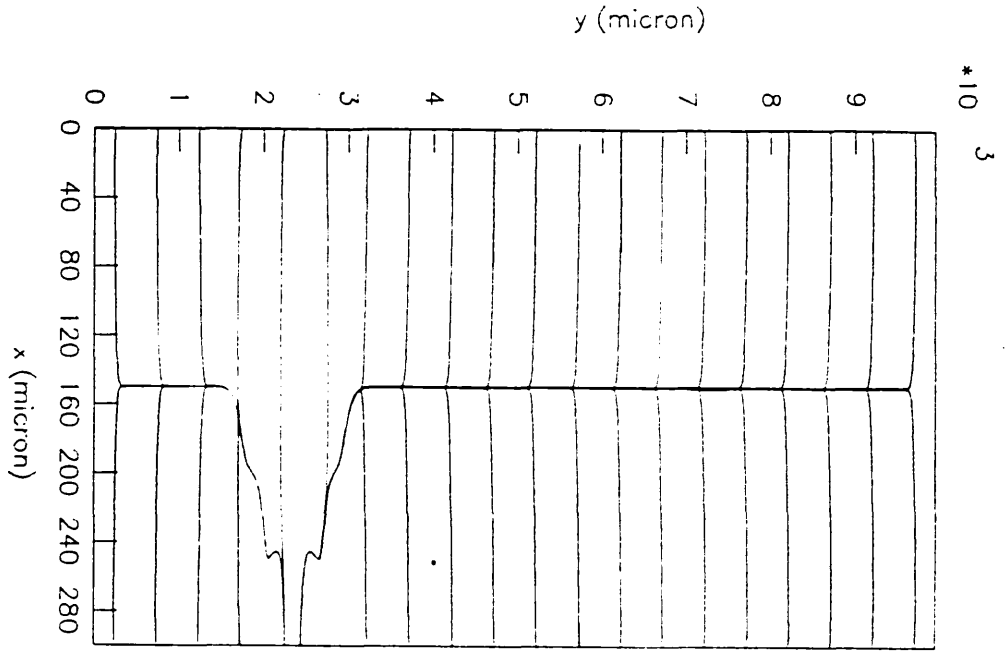


Figure 57: Drift paths of electrons in the SDC

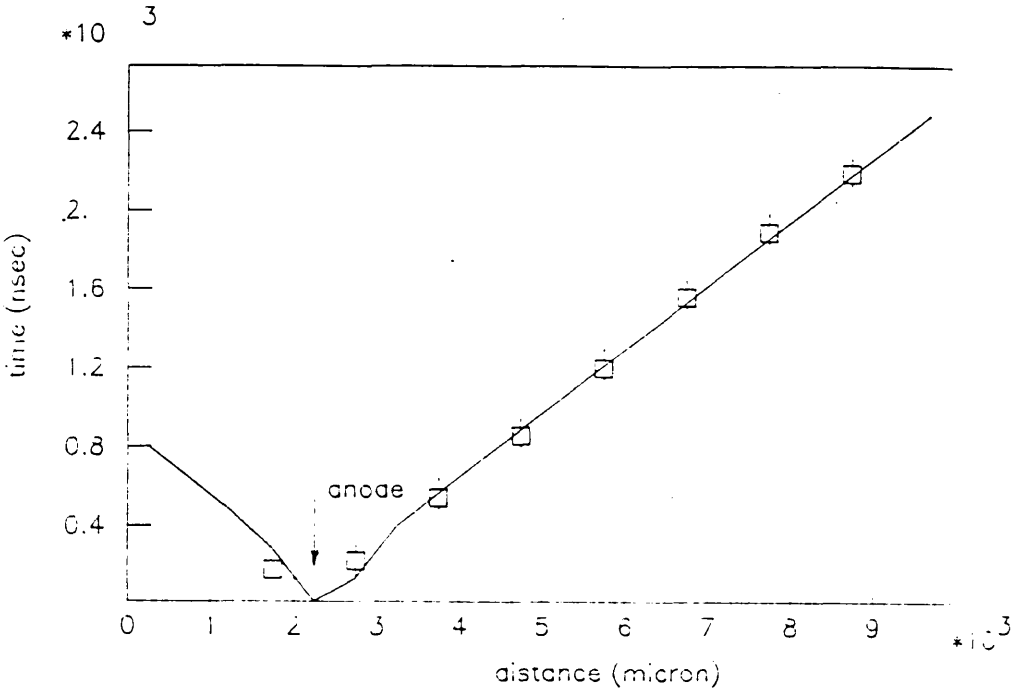


Figure 58: Simulated distance-time relationship for SDC (solid line). Also plotted are the experimental data points (squares).

6.3.1 Modelling of the Output Signal

The development of signals in the SDC can be demonstrated by considering an electron-hole pair created in the detector, some distance from the anode, as shown in figure 59. The potential minimum (PM) is at the centre of the detector and the e-h pair is assumed to be created in the upper half of the detector , nearest surface A. As the electron (-q) and the hole (+q) separate and move in opposite directions along x, currents are induced at the p^+ contacts on both surfaces,[2] A and B. This is analogous to the

---

[2] For practical purposes all the p^+ strips on side A can be capacitively coupled and signals induced at at the p^+ strips on surface A can be detected by an amplifier connected to all the strips. A similar arrangement can be used to detect signals at B.

charge collection in a conventional p^+n detector. However, since the charges travel only half the detector thickness, a total charge of q/2 is induced at each surface. The polarity of the signal is opposite for the two surfaces and it depends on which side of the PM the e-h pair is created. As the electron drifts in the y-direction along the PM, virtually no signal is induced at the anode until the electron comes very close to the anode. This is because, during drift, all the charge is induced at the p^+ contacts - $+q/2$ at A and $+q/2$ at B - so that the p^+ electrodes effectively shield the charge of the moving electron. As the electron is collected at the anode, a signal of $+q/2$ is induced at each surface A and B and a charge of -q is induced at the anode.

The development of the signals can be further illustrated by the results of computer simulations. The signals were modelled for a silicon drift chamber with the parameters defined in figure 55. Figure 60 shows the situation. 20 charges were generated at some distance from the anode in a region close to surface A. A given y-coordinate was specified and the charges were uniformly distributed along x = 250-260 µm.

The results are shown in figure 61 where the drift distance Δy was 7.0 mm. In (a) the signal induced at surface B is shown while (b) shows the anode signal. All signals are normalised to the generated charge which is defined as $+q$. As can be seen, both a prompt signal of $+q/2$ and a delayed signal of $-q/2$ are observed at B while at the anode only the delayed signal $+q$ is observed. The shaped pulses were calculated for CR-RC shaping with a time constant of 0.2 µsec.

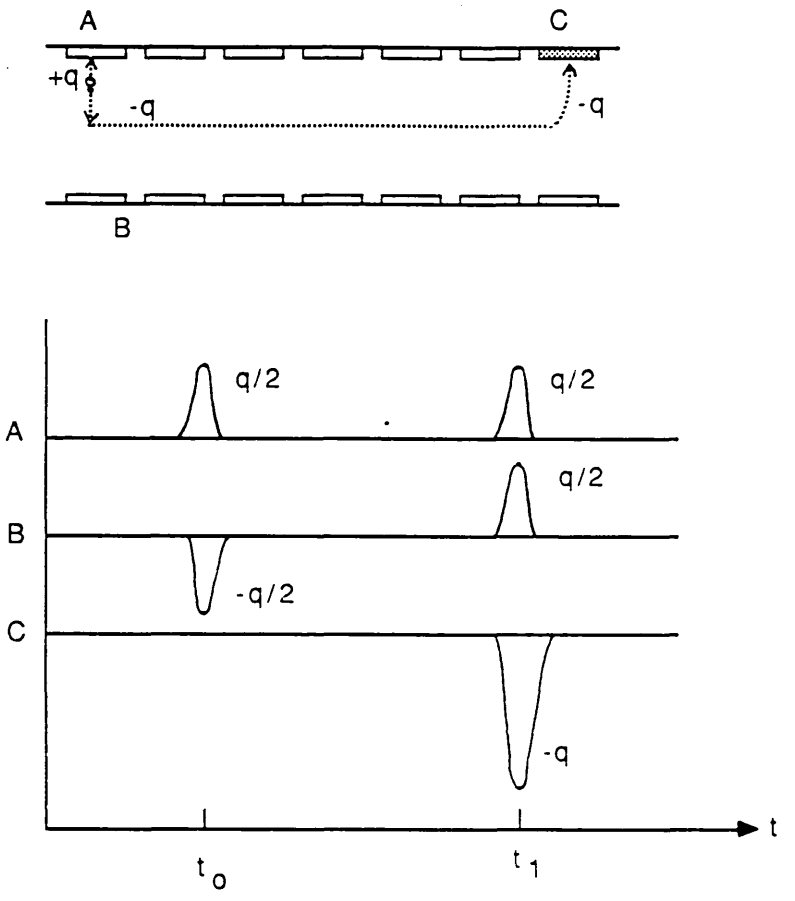


Figure 59: Development of signals due to charge deposited in the SDC

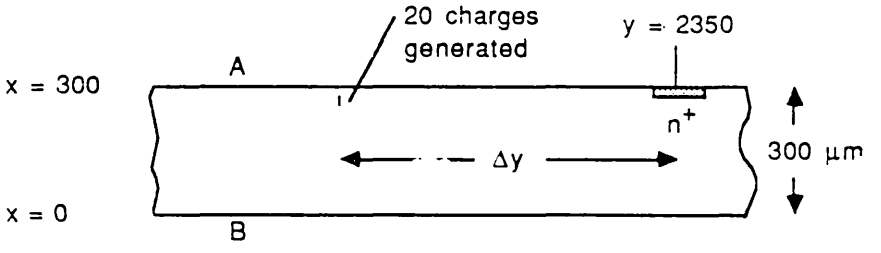
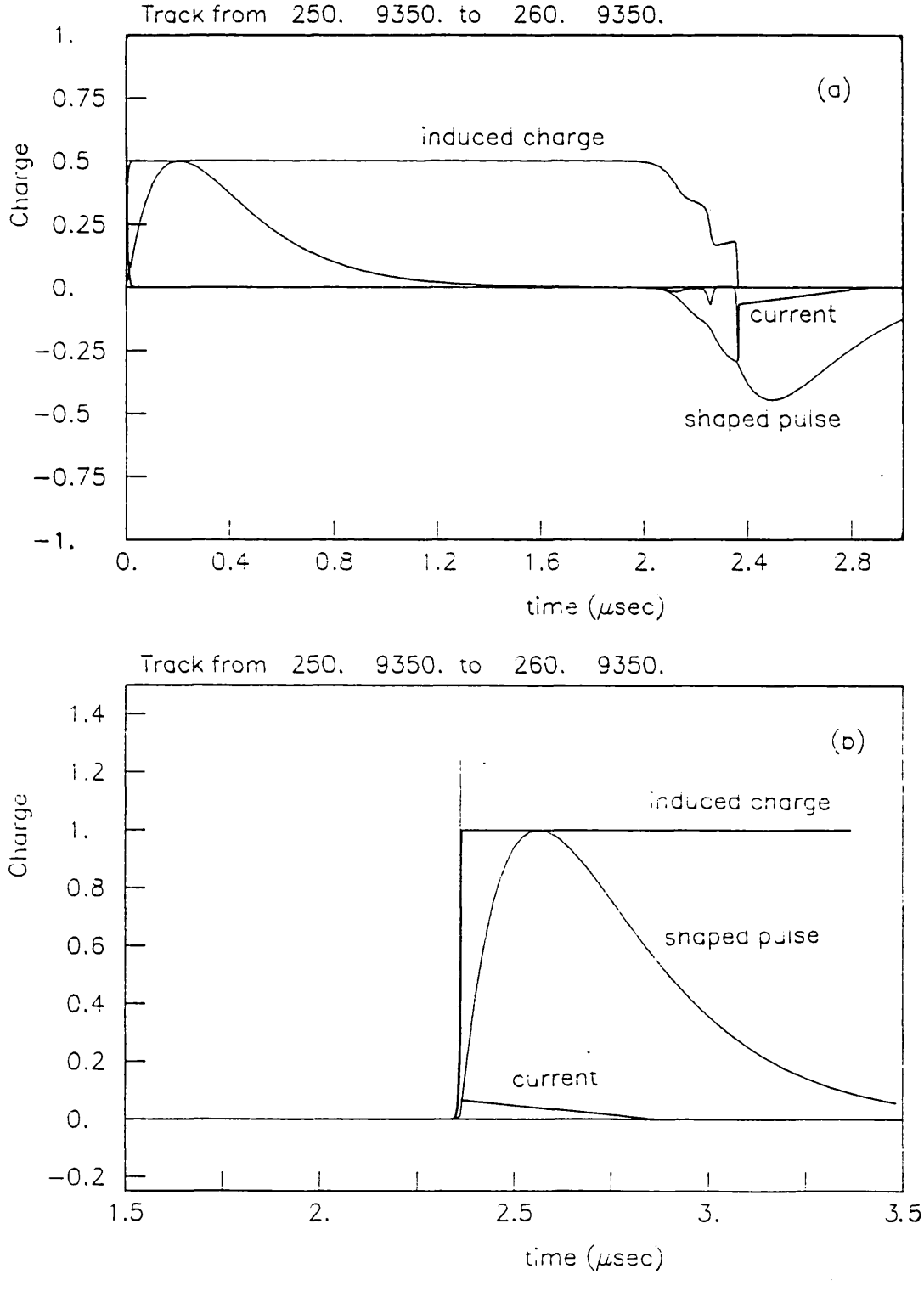


Figure 60: Generation of charge in the SDC for modelling the output signals.

Figure 61: Signals induced by charges for 7.0 mm drift distance
Induced charge, current and shaped output pulse
(a) at surface B and (b) at the anode.
The shaping time constant was 0.2 μsec.



It is evident that by measuring the time difference between the prompt signal at t_o induced in the p^+ contacts and the anode signal at t_1 it is possible to evaluate the drift time (t_1-t_o) without the use of an external timing trigger. This is potentially a very useful feature of SDCs, although in this self-triggering mode the SDC is expected to have a degraded position resolution due to the additional timing error in the prompt signal measurement.

6.3.2 Effects of Diffusion of the Charge Cloud

The effects of diffusion were simulated by modelling the anode signal for several drift distances with a constant drift field. A charged particle traversing the SDC was simulated by generating 20 charges uniformly distributed along a track parallel to the y-axis. These charges have to be viewed as groups of e-h charges utilised for practical purposes, since to run the simulation for ~ $2.5\ 10^4$ charges, which is the approximate number of e-h pairs created by a minimum ionising particle traversing the SDC, would require very large amounts of computing time. Four situations were simulated corresponding to drift distances of 1.0 mm, 3.0 mm, 5.0 mm, and 7.0 mm. The anode signals are shown in figure 62. The development of the signals is as expected from the model of induced signals described above. The effects of diffusion were included in each simulation. However, comparing the output pulses, it is seen that there is no significant loss of pulse height or broadening of the pulse even up to drift distances of 7.0 mm (corresponding to a drift time of approximately 2.4 μsec).

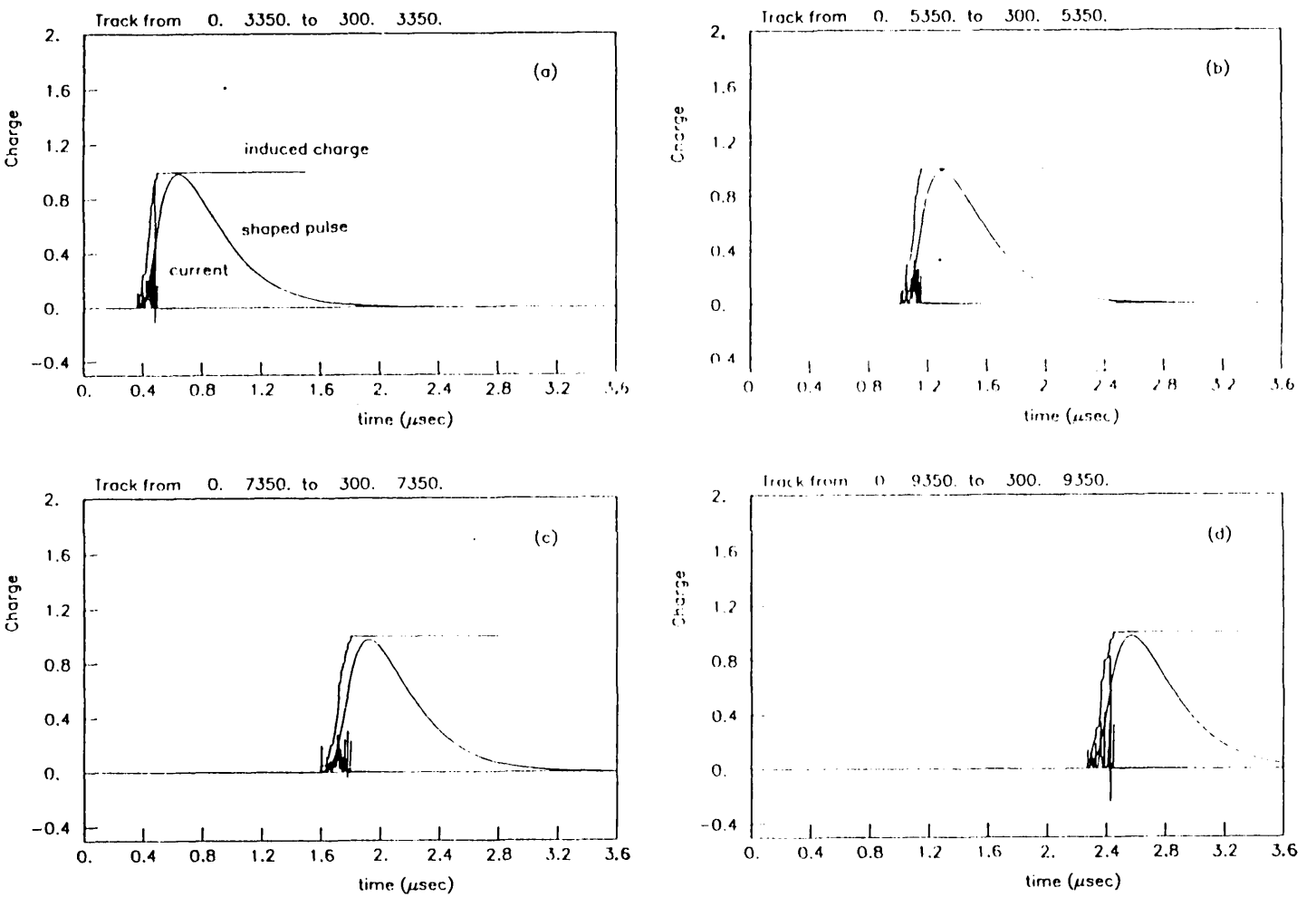


Figure 62: Simulated anode signals for drift distances of (a) 1.0 mm, (b) 3.0 mm, (c) 5.0 mm and (d) 7.0 mm.

6.3.3 Undulations in the Potential Minimum

Computer modelling has revealed that certain operating conditions of the SDCs may give rise to unwanted variations in the potential minimum at the centre of the detector. These variations take the form of undulations of the potential minimum (PM) with a periodicity equal to the pitch of the field shaping electrodes. To establish the magnitude of this effect, simulations were performed for a silicon drift chamber with several applied drift fields. The detector parameters were chosen to be

strip pitch = 250 μm

strip width = 200 μm

detector thickness = 300 μm

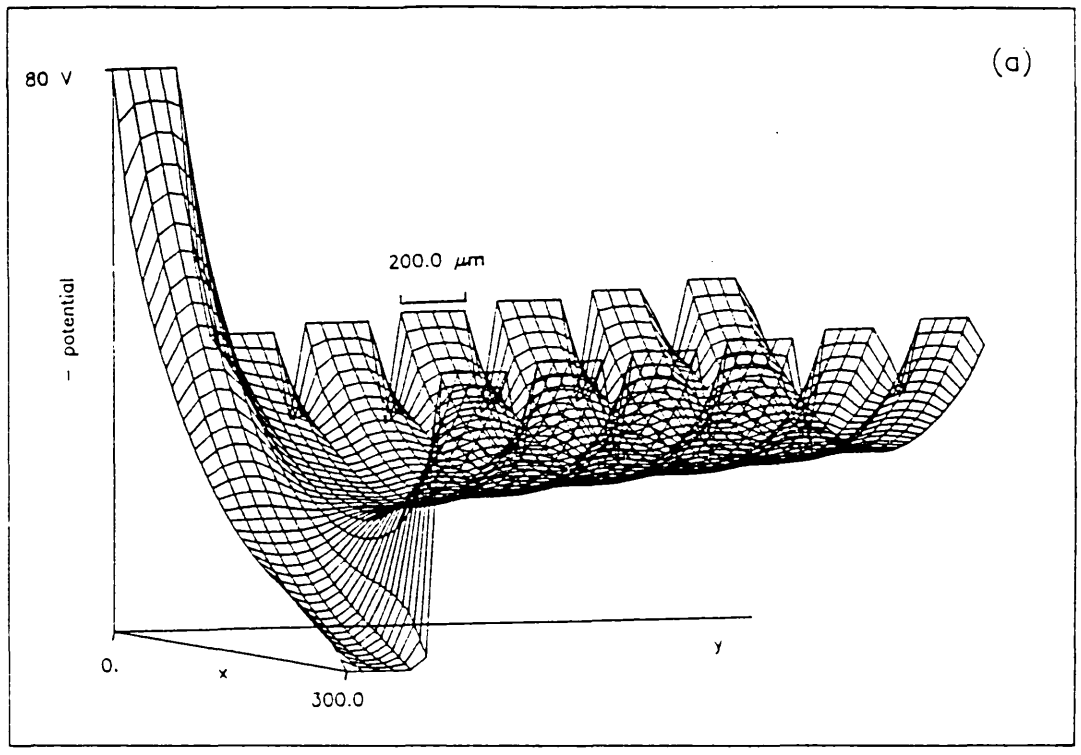
resistivity = 3.7 kΩcm

40 strips on both sides; anode at strip 10

which are representative of the real SDCs used in the experiments.

Figure 63 (a) shows a contour plot of the potential distribution for electrons in the anode region of the detector for an applied drift field of 50 V/cm. Undulations of the PM at the centre of the detector can be seen and these are made more evident by figure 63 (b) which shows the potential at x = 150 μm (= d/2) plotted against y.

The effect of these undulations is to produce a series of local potential minima for electrons along the centre of the detector which may give rise to pockets of undepleted silicon. Experimental observations fit this picture as described in chapter 5. Figure 64 shows the variation of the PM at x = 150 μm for drift fields of (a) 130



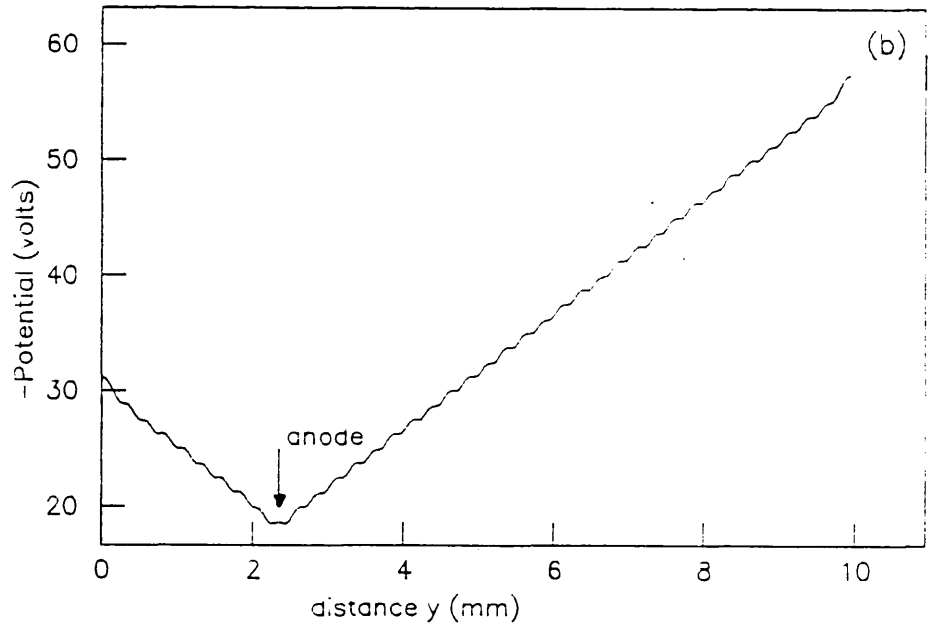


Figure 63: Variation of the potential minimum (a) Potential distribution in the SDC in a region close to the anode. (b) Variation of the potential along the centre of the detector (x = d/2). The drift field was 50 V/cm.

V/cm and (b) 390 V/cm. Comparing with figure 63 (b) it can be seen that the undulations are reduced for higher drift fields and at E = 390 V/cm the undulations become very small. This is also in agreement with the experimental evidence presented in chapter 5.

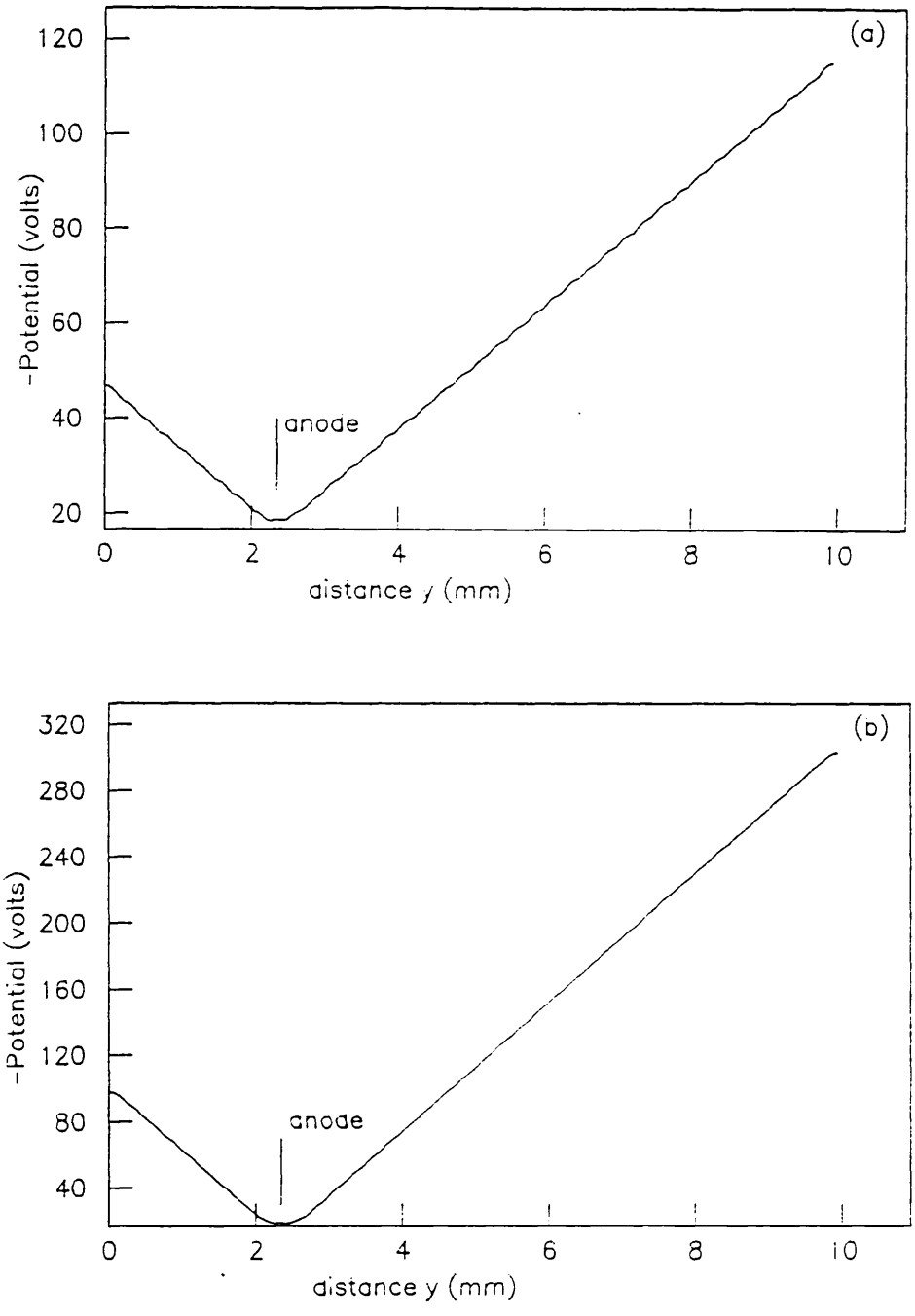


Figure 64: Variation of the potential along the centre of the SDC for drift fields of (a) 130 V/cm and (b) 390 V/cm.

6.3.4 Self-biasing of SDCs - Hole Currents

It has been discovered that, under certain conditions, a hole current can be made to flow at the surface of a silicon drift chamber between the p^+ electrodes [41]. This hole current can be used to bias the SDC so that it is not necessary to connect all p^+n junctions to an external voltage divider. It is found that when the potential difference between adjacent p^+ electrodes is low, a potential barrier exists between the two electrodes and therefore the hole current cannot flow. However, if the voltage difference is high enough the potential barrier can be removed so that the hole current will start to flow. The voltage required to remove the potential barrier will be referred to as the threshold voltage V_T. Figure 65 shows the potential distribution along the surface of the SDC under two bias conditions. In figure 65 (a) the voltage difference between adjacent strips is less than V_T. As can be seen, the potential energy for holes in any p^+ electrode increases in all directions away from the electrode. In this situation mobile holes cannot flow out of the p^+ electrodes. Figure 65 (b) shows the potential when the voltage difference between strips is just less than V_T. Here the potential barrier for holes has almost disappeared in the direction toward the adjacent p^+ strip at the lower potential. Thus, if the potential difference between strips was increased a large hole current would flow, thereby restoring the voltage difference to V_T. If a sufficiently large voltage difference is applied between a p^+ electrode near the anode and a p^+ electrode at the edge of the SDC, a hole current flows from the first to the last electrode and the intermediate

strips float at potentials such that the voltage difference between neighbouring strips is V_T. By this means the SDC can be self-biased.

Experimental observations of the hole currents in the SDCs and in silicon microstrip detectors[3] have shown that the value of V_T depends on the gap between adjacent p^+ strips. For the microstrips, with a gap of 25 μm between strips, the value of V_T was found to lie between 8 V and 15 V. This range of values resulted because V_T was found to vary with the depletion depth of the p^+n junctions, to be reduced by exposure to light and to change with time during bias. These effects are not completely understood and need to be investigated further. Similarly, for SDCs, which had a 50 μm gap between strips, the value of V_T was approximately 60 V.

Simulations were performed to predict the variation of V_T with the gap. It was found that to fit the experimental data the value of Q_f used had to be chosen carefully. Values of $Q_f = 1.0\ 10^{10}\ cm^{-2}$ up to $Q_f = 5.75\ 10^{10}\ cm^{-2}$ were found to encompass the data reasonably well as shown in figure 66 (b). The upper curve is for $Q_f = 5.75\ 10^{10}\ cm^{-2}$ and the lower curve is for $Q_f = 1.0\ 10^{10}\ cm^{-2}$. The curves show that the dependence of V_T on the gap is approximately quadratic. This is expected since when the hole current flows the potential between the strips is of the same form as that for a fully depleted p^+n detector. The depletion voltage for a given thickness d of silicon is proportional to d^2.

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[3] These detectors were built for the NA14 experiment at CERN by Micron Semiconductor Ltd.

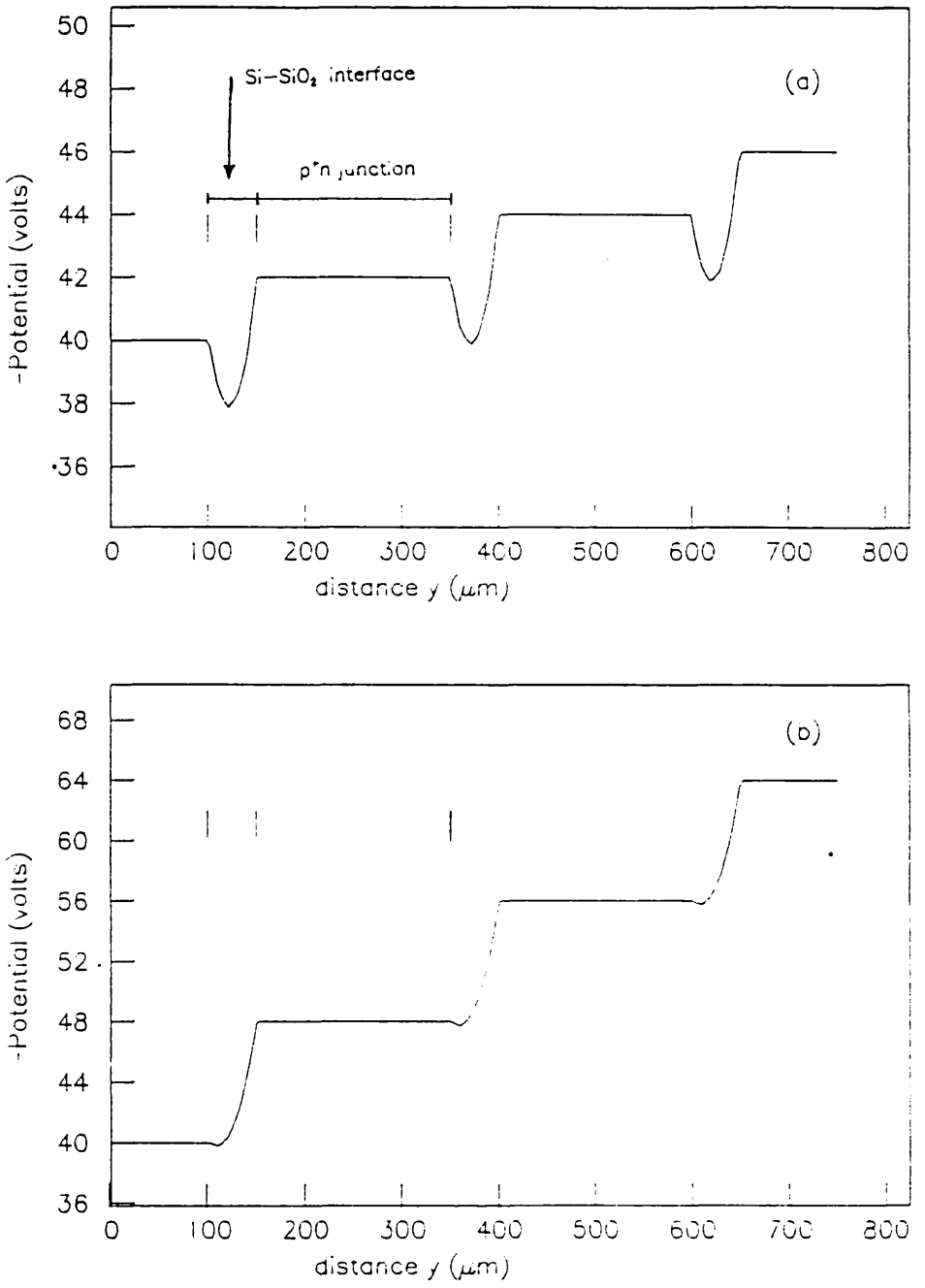


Figure 65: Potential distribution along the surface of the SDC with an applied voltage increment between adjacent strips of (a) ΔV less than V_T and (b) ΔV just less than V_T.

The results of figure 66 (b) are directly relevant to the design of

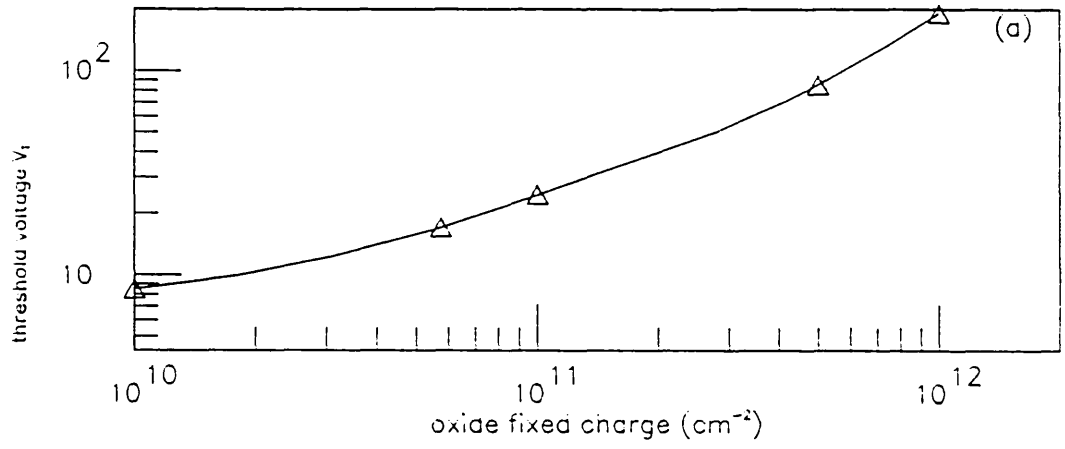
self-biased SDCs since it is immediately obvious that the drift field is determined by V_T and the strip pitch p, i.e.

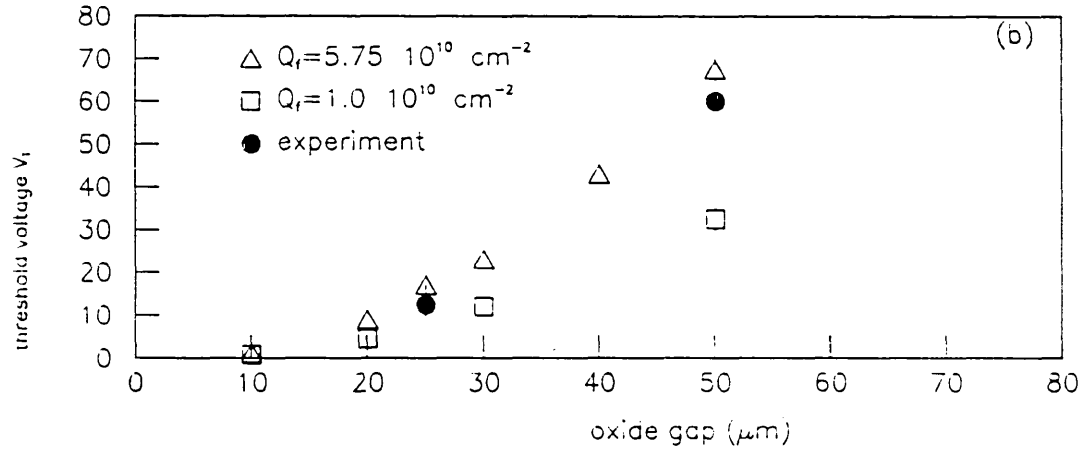
$$E = V_T/p$$

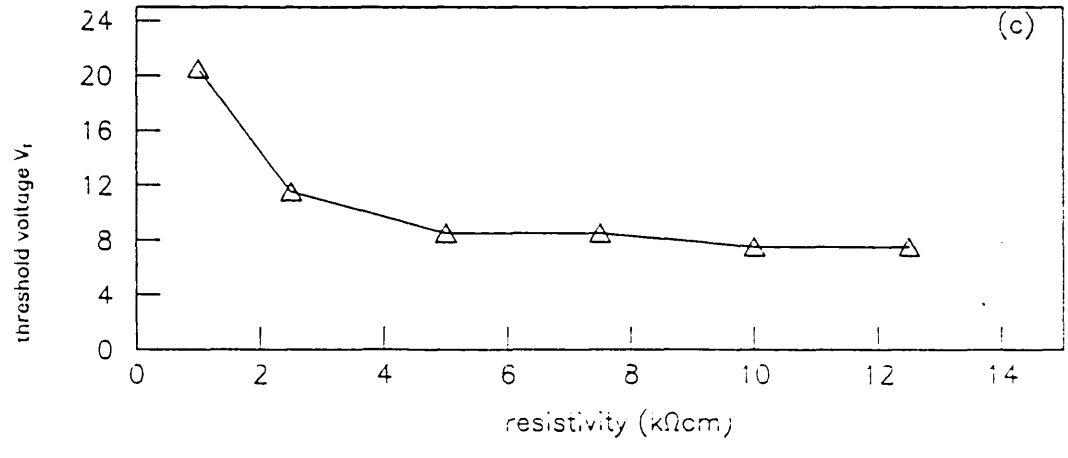
Thus V_T and p must be chosen to obtain the required drift fields. Simulations to predict the variation of V_T with the resistivity of the detector were also performed. For high resistivities, $\rho > 3.0$ kΩcm, the threshold voltage was found to be essentially independent of ρ as shown in figure 66 (c). For silicon detectors the resistivity is often larger than 3 kΩcm and therefore variations in V_T are not likely to be due to variations in the resistivity.

Although the simulation programs were found to describe the main properties of the SDCs rather well, it is known that the modelling of the effects of the oxide fixed charge is not correct. For n-type silicon the presence of Q_f causes the energy bands to bend downwards as shown in figure 67 and therefore an accumulation layer of electrons forms at the surface. The same phenomenon is expected to occur in the silicon drift chambers even though the bulk of the detector is fully depleted. The depth of the accumulation layer is of the order of a Debye length ($L_D \sim 4$ μm at 300 K for a doping density of 10^{12} cm^{-3}) and the electrons in this layer 'cancel' out some of the oxide fixed charge. Thus when applying the boundary condition at the $Si\text{-}SiO_2$ interface Q_f must be replaced with an effective oxide charge density $Q_{eff} < Q_f$. The values used to agree reasonably with the experimental data were $Q_{eff} \sim (1.0 - 5.75)\ 10^{10}$ cm^{-2} compared to values of $Q_f \sim 10^{11} - 10^{12}$ cm^{-2} for the actual oxide charge density in a typical oxide passivated silicon detector.

Figure 66: Variation of the threshold voltage V_T. V_T plotted against (a) oxide fixed charge density, (b) oxide gap and (c) resistivity. Also plotted in (b) are some experimental data.







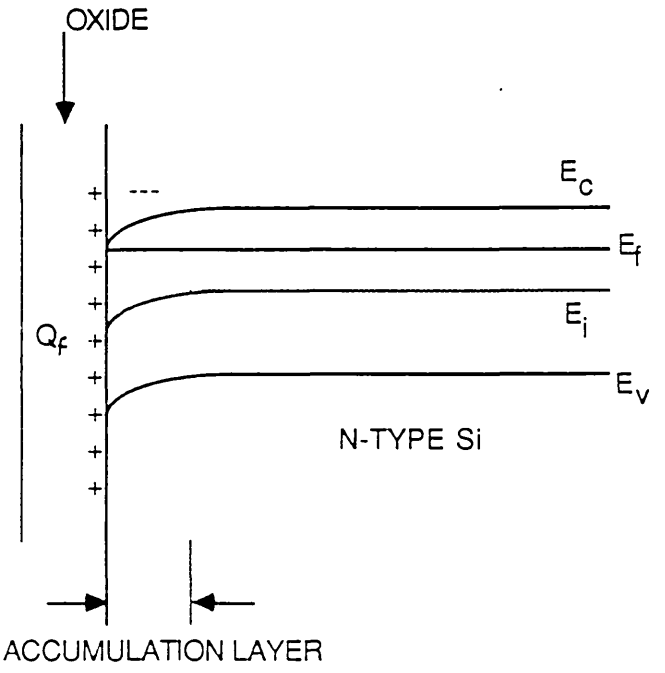


Figure 67: Band-bending at the surface of an n-type semiconductor due to the presence of oxide fixed charge .

6.4 DESIGN OF SILICON DRIFT CHAMBERS

Experimental observations and computer simulations of the prototype SDCs have shown that although the simple design of these detectors was useful for demonstrating the principle of SDCs and evaluating some of their important properties, several improvements in the design can be made. Therefore, new SDC designs were made and the photolithographic masks have been produced by the method described in chapter 4.

Figure 68 shows the front side of one of the designs. Two regions of the detector can be defined; (a) the drift region and (b) the anode region. Figure 69 (a) shows a cross-section of the

pitch (μm)	oxide gap (μm)	V_T (V)	E_{drift} (V/cm)
120	20	4.5-9.0	375-750
100	15	2.0-5.0	200-500

TABLE 2

Electrode dimensions and expected drift fields for the new SDC designs

detector in the drift region where the strip pitch was either 120 μm or 100 μm (two different designs). Simulations have shown that, for a given detector thickness, the magnitude of the potential undulations increases with the strip pitch and calculations [42] have suggested that to sufficiently supress the undulations

$$p/d \leq 0.5$$

where p is the strip pitch and d is the detector thickness. The strip pitch for both designs were chosen to satisfy this criterion, assuming a wafer thickness of 300 μm.

In the drift region the separation between strips (i.e. the oxide gap) was chosen to be small enough to enable the devices to be self-biased by the hole current whilst obtaining suitable drift fields. The drift fields were chosen using figure 66 (b) as a guideline to estimate the required gap between strips. Table 2 shows the drift fields expected - gaps of 15 μm and 20 μm were chosen for the designs.

The voltage difference between the undepleted region and the field shaping electrodes can be very high, especially for the strips which are farthest from the anode. To avoid breakdown at the edges of these strips, a set of electrodes perpendicular to the field strips were incorporated in the design as shown in figure 68

In the anode region of the SDC (figure 69 (b)) the front surface consists of two parallel n^+ anodes (A_L and A_R) separated by a p^+ electrode (F_o) to resolve the left-right ambiguity which would exist in the position measurement if there was only one anode. Thus signals originating fom the left-hand side of the detector would be detected

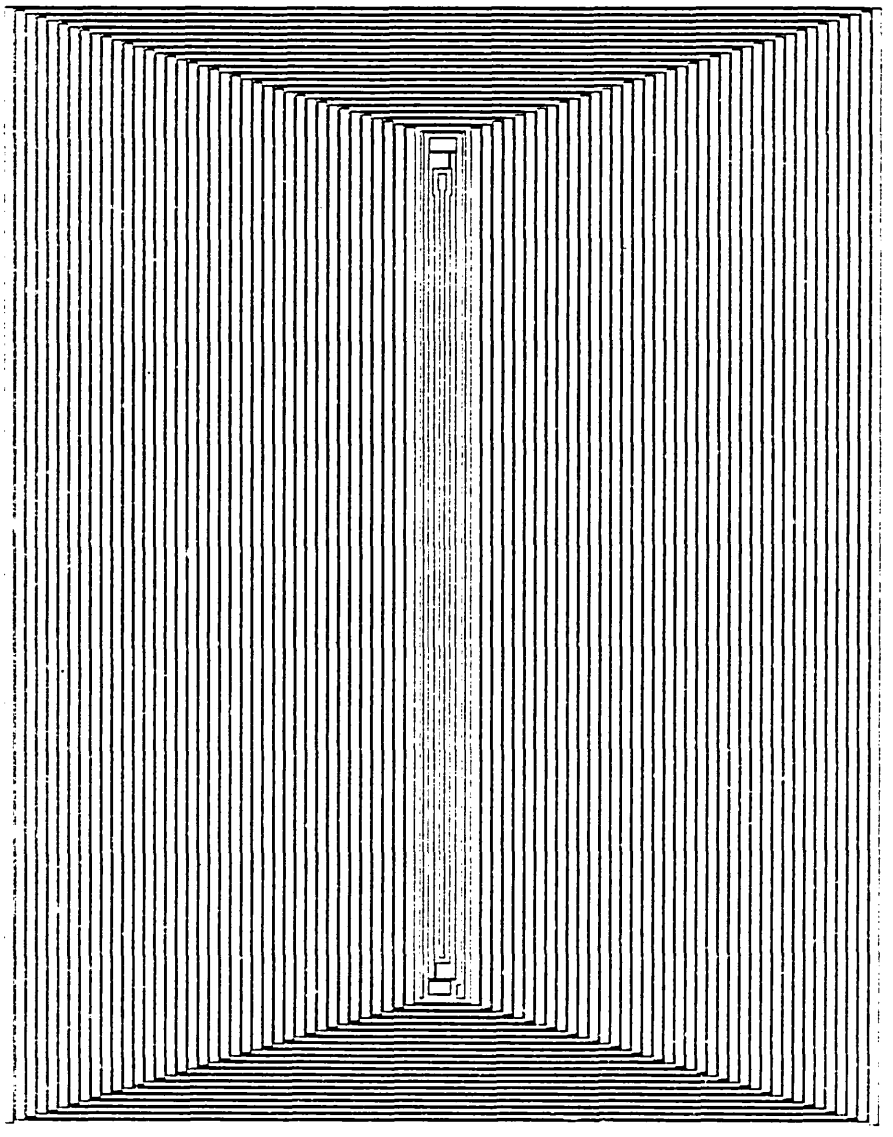


Figure 68: Design of the front surface of the SDC (metallisation mask).

in anode A_L and vice versa. The back surface of the detector in the anode region consists of a wide p^+ electrode (B1) which, together with electrodes F1 on the front, can be suitably biased in order to

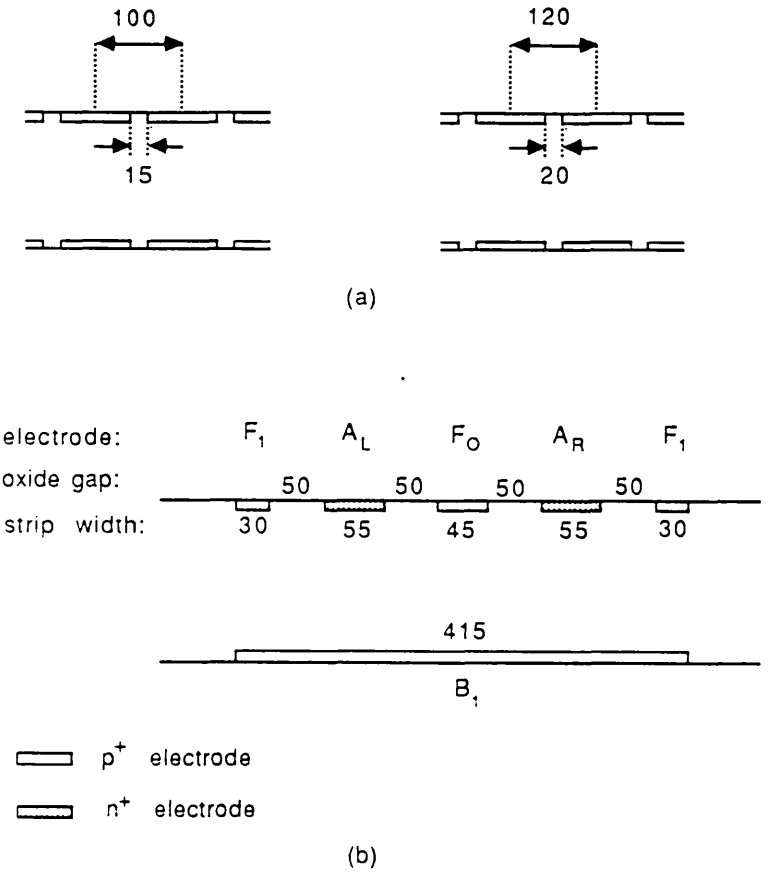


Figure 69: Cross-sectional view of the new SDC designs (a) in the drift region and (b) in the anode region.

shift the potential minimum from the centre of the detector to the surface at the anodes.

The active chamber region was designed to coincide with the p^+ field shaping electrodes. Thus, to prevent charges generated in the region containing the perpendicular electrodes from reaching the anodes, two guard anodes GA1 and GA2 were provided.

These designs will be fabricated and tested in 1987.

Chapter VII

SUMMARY AND CONCLUSIONS

Silicon drift chambers were successfuly fabricated on double-side polished silicon using the oxide passivated planar technology. Diode strips fabricated on both surfaces of the wafer using ion implantation were found to have leakage currents of ~ 1-2 nA. These leakage currents are roughly the same as those obtained with conventional microstrip detectors which employ diode strips on one surface of the wafer only, making their fabrication simpler. However, due to the presence of one or two high leakage current strips on the detectors, the minimum leakage current achieved for the whole SDC was found to be ~ 600 nA. The electronic noise was dominated by this rather high leakage current and was approximately 1400 electrons (ENC) for CR-RC shaping with 200 nsec shaping time constants.

The expected CV characteristics were observed in the SDCs - a gradual fall of the capacitance followed by a sharp drop in the capacitance at depletion. With a suitable drift field applied the detector capacitance, including printed circuit board, was found to be < 5 pF at depletion.

For low drift fields non-ideal behaviour of the devices was observed. This was attributed to the presence of local potential minima in the detector giving rise to pockets of undepleted silicon, originating from the nature of the applied potentials and the

non-optimum strip pitch. However, by applying a sufficiently high drift field, these potential minima could be eliminated.

The drift action was observed using a collimated β source. Delayed pulses due to the drift of electrons along the potential minimum were seen as the source was scanned across the whole active area of the detector. The drift distance - time relationship was approximately linear and was well reproduced by computer simulations of the SDCs. The maximum distance over which drift of electrons was achieved was ~ 7.5 mm, limited only by the detector geometry.

Several improvements have been made to the SDC designs, including a reduced strip pitch, and a new set of photolithographic masks have been produced. Improvements in the leakage currents of these new devices are expected.

REFERENCES

1. See, for example, S.M. Sze, "Physics of Semiconductor Devices", Wiley-Interscience, New York (1981), or, H.K. Henisch, "Rectifying Semiconductor Contacts", Clarendon, Oxford (1957).

2. E.C. Finch et al., Nucl. Instr. and Meth. 142 (1977) 539.

3. J.J. Aubert et al., Phys. Rev. Lett. 33 (1974) 1404; J.E. Augustin et al., Phys. Rev. Lett. 33 (1974) 1406.

4. R. Bailey et al., Nucl. Instr. and Meth. 213·(1983) 201.

5. G. Barbiellini and P.G. Rancoita, CERN-EP/83-01 (1983).

6. G. Hall, D. Robinson and I. Siotis, Nucl. Instr. and Meth. A245 (1986) 344; G. Hall, D. Robinson, C. Seez and I. Siotis, Nucl. Instr. and Meth. A253 (1987) 491.

7. G. Bellini, L. Foa and M.A. Giorgi, Phys. Lett. 83, No. 1 (1982) 9; B.D. Hyams et al., Nucl. Instr. and Meth. 205 (1983) 99; G. Barber et al., Nucl. Instr. and Meth. A253 (1987) 530.

8. P. Weilhammer, CERN-EP/86-54 (1986).

9. J.T. Walker et al., Nucl. Instr. and Meth. 226 (1984) 200; R. Hofmann et al., Nucl. Instr. and Meth. 226 (1984) 175.

10. E. Gatti and P. Rehak, Nucl. Instr. and Meth. 225 (1984) 608.

11. Wacker-Chemitronic GmbH, 8263-Burghausen, Fed. Rep. Germany.

12. S.M. Sze, "Physics of Semiconductor Devices", Wiley-Interscience, New York (1981).

13. R.N. Hall, Phys. Rev. 87 (1952) 387; W. Shockley and W.T. Read, Phys. Rev. 87 (1952) 835.

14. W. Shockley "Electrons and Holes in Semiconductors", D. Van Nostrand, Princeton, NJ (1950)

15. B.E. Deal, J. Electrochem. Soc. 121 (1974) 198C.

16. C.K Kim, "The Physics of Charge-coupled Devices", in M.J. Howes and D.V. Morgan (Eds.) "Charge-coupled Devices and Systems", Wiley, New York (1979).

17. J. Kemmer, Nucl. Instr. and Meth. 169 (1980) 499.

18. J. Kemmer, Nucl. Instr. and Meth. 226 (1984) 89.

19. J.R. Ligenza, J. Appl. Phys. 36 (1965) 2703.

20. J.R. Ligenza and M. Kuhn, Solid-State Technol. 13 (1970) 33.

21. P.F. Schmidt and W. Michel, J. Electrochem Soc. 104 (1957) 230.

22. E.L. Jordan, J. Electrochem. Soc. 108 (1961) 478.

23. M.M. Atalla, in H. Gatos Ed., "Properties of Elemental and Compound Semiconductors" Vol. 5, Wiley-Interscience, New York (1960) pp 163-181.

24. B.E. Deal and A.S. Grove, J. Appl. Phys. 36 (1065) 3770.

25. A.S. Grove, O. Leistiko and C.T. Sah, J. Appl. Phys. 35 (1964) 2695.

26. C.J. Varker and K.V. Ravi, J. Appl. Phys. 45 (1974) 272.

27. E.H. Nicollian and J.R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology", Wiley-Interscience, New York (1982).

28. P. Borgeaud, J.G. McEwan, P.G. Rancoita and A. Seidman, Nucl. Instr. and Meth. 211 (1983) 363; E. Heijne, CERN Report 83-06 (1983).

29. B.E. Deal, E.L. Mackenna and P.L. Castro, J. Electrochem. Soc. 116 (1969) 997.

30. J.F. Gibbons, "Ion Implantation", in T.S. Moss (series Ed.), "Handbook on Semiconductors", Vol. 3, (S.P Keller Ed.), North-Holland, Amsterdam (1980).

31. S. Selberherr, "Analysis and Simulation of Semiconductor Devices", Springer-Verlag (1984).

32. F.A. Padovanni and R.Stratton, Solid State Electron. 9 (1966) 695.

33. "GAELIC For Beginners: An Introductory Guide to GAELIC Language", Rutherford Appleton Laboratory Electron Beam Lithography Facility (1980).

34. W. Kern and D.A. Poutien, RCA Review 31 (1970) 187.

35. K.A. Pickar, "Ion Implantation in Silicon - Physics, Processing and Microelectronic Devices", in R. Wolfe Ed., Appl. Sol. State Sci., Vol.5, Academic Press, New York (1975).

36. TOPSIL Semiconductor Materials A/S, DK-3600 Frederikssund, Denmark.

37. C. Canali, G. Ottaviani and A. Alberigi Quaranta, J. Phys. Chem. Solids 32 (1971) 1707.

38. Numerical Algorithms Library (NAGLIB) Routine Document

39. Suitable convergence parameters were determined by G. Hall, Blackett Laboratory, Imperial college, London SW7.

40. P.W. Nicholson, "Nuclear Electronics", Wiley-Interscience, New York (1974).

41. P. Rehak, E. Gatti, A. Longoni, J. Kemmer, P. Holl, R. Klanner, G. Lutz and A. Wylie, Nucl. Instr. and Meth. A235 (1985) 224.

42. Analytic calculations by G. Hall, Blackett Laboratory, Imperial College, London SW7.