SWITCHED-CAPACITOR SYSTEMS FOR NARROW BANDPASS FILTERING

by

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ABSTRACT

Integrated circuit Switched-Capacitor (SC) filters, and, in particular, SC bandpass filters, are important in modern analogue signal processing systems, especially for telecommunication applications.

Conventional design techniques for SC bandpass filters lead to unacceptably large capacitance ratios when the relative bandwidth, B, is less than 10%. For B<1%, they have an additional problem of very high sensitivity of the response to capacitance ratio errors. This has been overcome by using SC N-path filters, but N-path filters suffer from poor dynamic range.

This thesis presents alternative SC design techniques for B<10% and B<1% bandpass filters which overcome the problems of large capacitance ratios and high sensitivity of the response to capacitance ratio errors, thus making the circuits attractive for integrated circuit fabrication, yet providing good dynamic range. Key elements of the approaches are (i) an analysis of capacitance ratios in SC biquads leading to the concept of an optimum low value of switching frequency which minimises such ratios, (ii) the development of novel attractive decimator and interpolator circuits, based on polyphase networks and specifically designed to reject the resulting unwanted alias and image signals in the bandpass filter systems, (iii) the proposal of Single-Path Frequency-Translated (SPFT) systems which allow a B>1% SC filter to realise an effective B<1%

response, thus obtaining acceptable capacitance ratios and sensitivity without sacrificing dynamic range. Demonstration systems with relative bandwidths of 2.4% and 0.48%, and rejection of all alias and image signal components up to 300KHz and 364KHz, respectively, are used as examples. Measurements made on discrete component models confirmed the approaches, integration facilities not being available.

Finally, this thesis presents some speculative work on another type of system combining the basic ideas of N-path and SPFT systems, which is aimed, primarily, at the realisation of ultra narrow bandpass responses ($B<0.1\%$).

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INTRODUCTION

1.1 INTRODUCTION AND GENERAL AIM

Modern signal processing systems for analogue filtering applications in the audio-frequency range (DC to 20KHz) can be realised using one of the three major architectures shown in Fig.1.1. A fully analogue filter

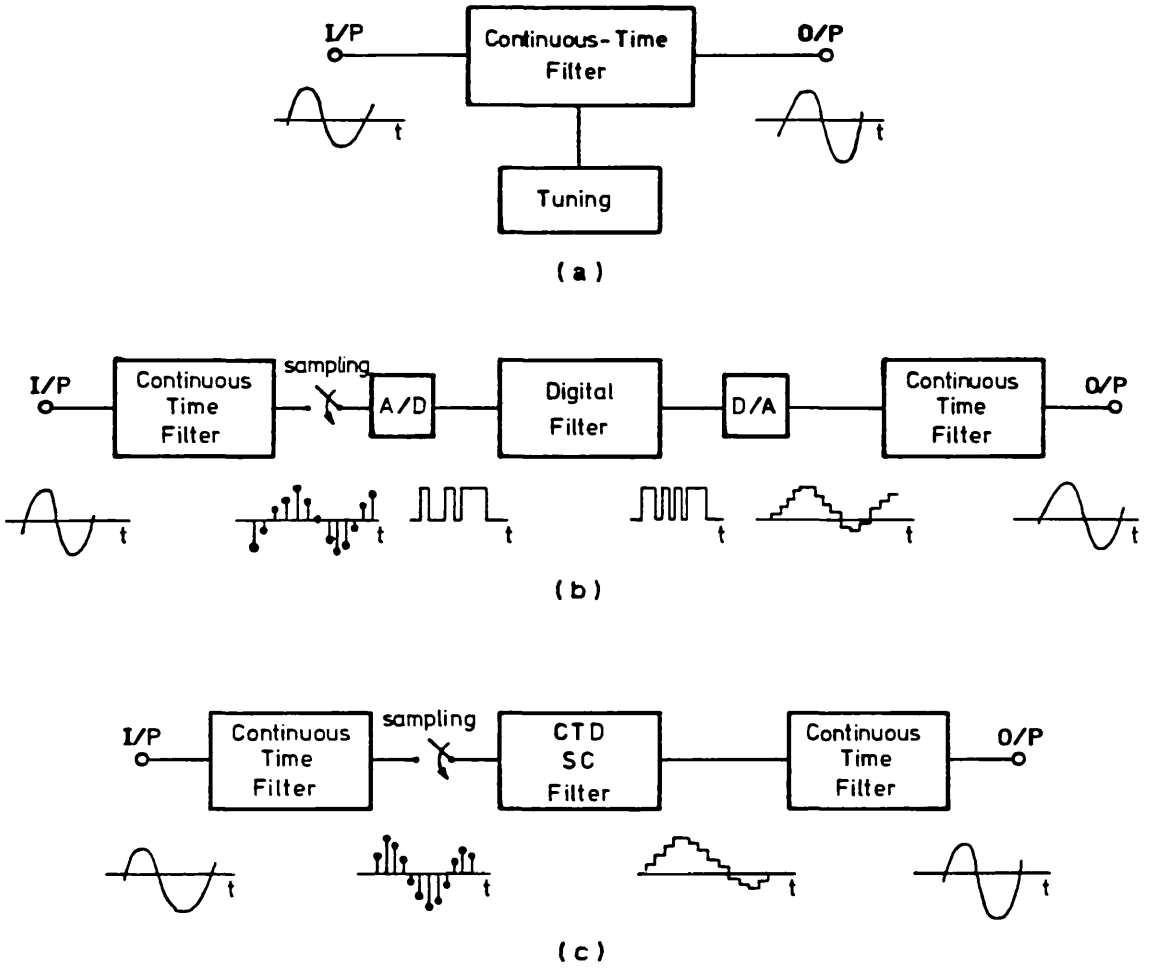


Fig.1.1: Signal processing system architectures for analogue filtering
(a) Analogue; (b) Digital; (c) Sampled-data

system employs a continuous-amplitude/continuous-time filter (or simply, continuous-time filter) realised in Metal Oxide Semiconductor (MOS) technology and which is continuously tuned by means of an auxiliary control

circuit, as shown in Fig.1.1-a [1.1]. This is required due to poor accuracy of time constants obtained using integrated MOS capacitors and MOS transistor-simulated resistors. Fig.1.1-b shows a typical digital filter system which employs a discrete-amplitude/discrete-time filter, frequently implemented using a digital signal processor together with analogue/digital and digital/analogue converters [1.2], and which also comprises two simpler continuous-time filters at the input and at the output of the system. The typical architecture of an analogue sampled-data filter system, illustrated in Fig.1.1-c, comprises a continuous-amplitude/discrete-time filter, implemented using either Charge-Transfer Devices (CTD's) [1.3] or Switched-Capacitor (SC) circuits [1.4], and also two additional input and output continuous-time filters. Whereas CTD transversal structures have the advantage of much higher operating speed, SC circuits realise recursive structures more efficiently and with better performance than CTD's, and are usually preferred for audio-frequency filtering applications [1.5].

Over the past five years, analogue sampled-data SC filter systems (or simply, SC filter systems) have generally yielded the best solution among such system architectures for realising high-quality low-cost Integrated Circuit (IC) audio-frequency filters, for the following main reasons [1.6]-[1.11],[1.3]: In comparison with fully analogue filter systems, they have greater precision of the frequency response, with better linearity

and also better temperature stability. SC filter systems also have higher operating speed, lower power consumption, smaller size, simpler hardware and usually much lower cost than digital filter systems and, in addition, are free from amplitude quantisation errors. The fact that SC filter systems can be implemented in MOS technology, allows full integration on a single silicon chip in conjunction with digital circuitry to form complex VLSI systems (Very Large Scale Integration).

Early research on SC filter design techniques has been primarily concerned with SC lowpass filter systems, particularly for application in PCM (Pulse Code Modulation) telephony systems (e.g. [1.12]-[1.18]). Some of the SC PCM filters which have since then been comercially produced have excellent performance [1.19], which demonstrates that the techniques available for the design of audio-frequency SC lowpass filter systems have already achieved a high degree of maturity. SC bandpass filter systems, on the other hand, have a potential for applications in many other Telecommunication systems [1.20]-[1.26] as well as in Speech Processing systems [1.27],[1.28] but, for reasons we shall come to in this Chapter, the design techniques currently available show a varying degree of success depending on the difficulty of the filter. The aim of this thesis, which we shall discuss more fully later on, is to study new design techniques for audio-frequency SC bandpass filter systems with narrow and very narrow relative bandwidths, which are suitable for integrated circuit

fabrication in view of the state-of-the-art of MOS technology.

The background material to support the treatment of SC bandpass filter systems in this thesis will be given in the remainder of this Chapter, and in Chapter 2. Here, we shall introduce the basic circuit aspects and principles of analysis and design of SC filters whereas in Chapter 2 we shall be concerned with the principles of operation of SC filter systems, mainly from the standpoint of the system design techniques to be proposed in this thesis.

1.2 SWITCHED-CAPACITOR FILTERING

1.2.1 SC resistor

The approach of SC filtering implemented in MOS technology is attributed to Fried [1.29] who, in 1972, showed that an analogue sampled-data resistor could be realised using the circuit of Fig.1.2-a. This simple circuit consists of one capacitor C and two switches S1 and

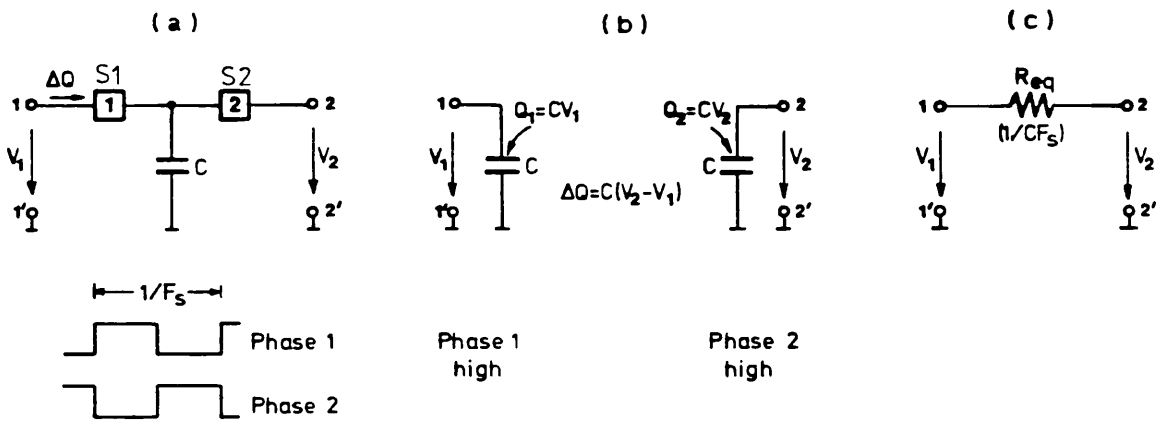


Fig.1.2: (a) Switched-capacitor resistor and (b) operation; (c) Equivalent analogue resistor

S2 controlled by two periodic non-overlapping switching waveforms, respectively with phases 1 and 2. As shown in Fig.1.2-b, in each period $T_s=1/F_s$ the capacitor C is alternately charged to V_1, when 1 is high, and to V_2, when 2 is high, yielding a packet of charge $\Delta Q=C(V_1-V_2)$ which flows with the polarity indicated in Fig.1.2-a. Since this operation is repeated every $1/F_s$ seconds, the average current flowing from terminal 1 to terminal 2 will be

$$(1.1) \ldots \qquad I_{av} = \frac{C(V_1-V_2)}{(1/F_s)}$$

Therefore, under the assumption that the switching frequency is much higher than the frequency of the input and output signals, the above sampled-data circuit simulates an analogue resistor connected between terminals 1 and 2, Fig.1.2-c, whose equivalent resistance value is

$$(1.2) \ldots \qquad R_{eq} = \frac{1}{CF_s}$$

1.2.2 MOS operational amplifiers

SC circuits did not receive much recognition until late 1976, when the first monolithic MOS Operational Amplifier (OA) with internal compensation became available. In this manner, amplifiers could be integrated on the same silicon chip with the switches and capacitors [1.30]. The DC gain of such OA, about 50dB, was rather modest in comparison with traditional bipolar OA's, but the low power consumption ($\simeq$150mW) on the one hand, and the small die

area ($\simeq 0.787mm^2$) on the other hand, showed great potential for integrating on a single silicon chip high order filters requiring many OA's [1.30]. Thereafter, MOS OA design techniques using both n-channel-MOS (NMOS) and complementary-MOS (CMOS) technologies improved very rapidly, which contributed to a great extent to the success of SC technology. For example, the first IC SC filters demonstrated in practice (in the late-1977) employed one [1.31] or two [1.32] NMOS OA's with 75dB DC gain, power consumption of the order of 13mW and occupying about $0.398mm^2$ die area [1.32]. In the late-1979, CMOS OA's for the first generation of SC lowpass PCM filters achieved without too much difficulty a DC gain of 85dB, with about 5mW power consumption and $0.106mm^2$ die area (5μm line width) [1.12]. Modern CMOS OA's consume as little as 0.5mW and occupy a meagre $0.047mm^2$ die area (4μm line width), which makes it possible to integrate as many as 40-50 OA's on a single silicon chip [1.24],[1.25]. The dynamic performance of such CMOS OA's is typically 70-80dB DC gain, about 4MHz unity gain bandwidth and 500ns settling time, which is adequate for most applications of SC filters in the audio-frequency range [1.33],[1.11].

1.2.3 SC integrator and time constant

The original approaches for the design of SC filters consisted of replacing the resistors in active-RC filters by their SC equivalents, while keeping the capacitors and the OA's of the original circuits [1.31], [1.32]. The basic building block of the active-RC filters was the Miller

integrator (e.g. [1.34]) shown in Fig.1.3-a whose time constant τ_{RC} is defined as

(1.3) ... $$\tau_{RC} = RC_f$$

This circuit is unsuitable for direct integration in MOS technology because the accuracy of the time constant is rather low and, besides, its implementation consumes a large area of silicon [1.7],[1.11]. Instead, an equivalent SC integrator may be obtained by replacing in Fig.1.3-a the input resistor by its SC equivalent in Fig.1.2, leading to the circuit of Fig.1.3-b. The SC integrator time constant τ_{SC} obtained from (1.2) and (1.3) is

(1.4) ... $$\tau_{SC} = \left(\frac{1}{F_S}\right).\left(\frac{C_f}{C}\right)$$

The accuracy of the SC integrator time constant, typically between 0.1% and 1% [1.7], depends on the accuracy of the capacitance ratio C_f/C which, as we shall discuss in the next Section, is determined essentially by geometric aspects of the capacitor areas. As a result, the values of the SC integrator time constants are also very stable with

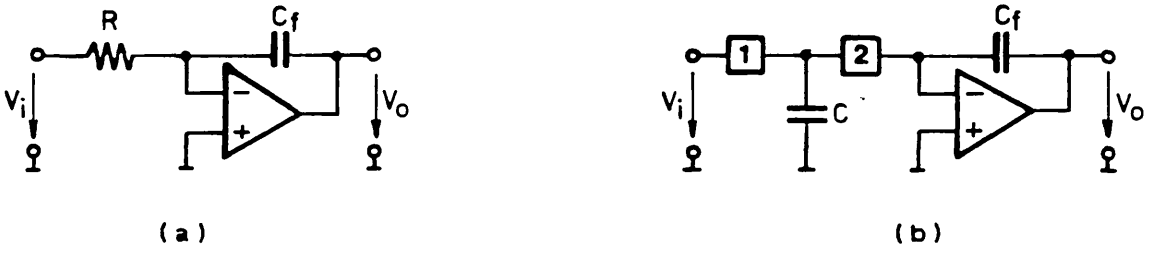


Fig.1.3: (a) Active-RC Miller integrator
(b) SC integrator

respect to temperature variations and ageing [1.7],[1.11]. The switching frequency F_s can be derived from a quartz-stabilised oscillator, and it has such a high precision that it is usually considered invariant.

The switching frequency plays an important role in the operation of SC filters in general, since it provides a simple means of changing the values of the time constants, with constant capacitance ratios, thus moving the frequency response along the frequency axis, i.e. band-edge frequency programmability. Conversely, the value of switching frequency is important because it affects the values of capacitance ratios for given time constants of the SC filters. Usually, it is desirable to adopt low values of switching frequency for reducing the values of capacitance ratios, in order to improve their accuracies and to minimise the total silicon area required for implementation. This is particularly relevant in critical applications of SC filters with high selectivity, such as those considered in this thesis, where there is an inherent problem of large capacitance ratios and high sensitivity of the frequency response to capacitance ratio errors. Other important implications of the choice of switching frequency are related to the design of the complete SC filter system, including the continuous-time filters. These implications will be discussed in Chapter 2.

1.3 IMPERFECTIONS OF SC CIRCUITS

1.3.1 Grounded parasitic capacitances

The operation of SC circuits is affected to a greater or to a lesser extent by parasitic capacitances which are associated with the MOS switches, capacitors and OA's [1.7],[1.9],[1.11], as shown in Fig.1.4. The effect of the

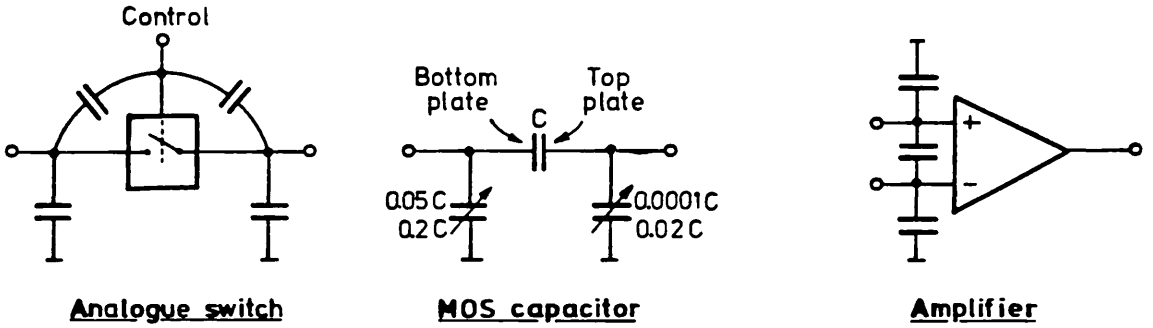


Fig.1.4: Parasitic capacitances of SC circuit elements

parasitic capacitances which are connected to ground is, in general, to modify the capacitance ratios in SC circuits and thus to affect their accuracy. Some grounded parasitic capacitances are nonlinear, and therefore may also produce signal distortion. This is the case for the parasitic capacitances of the MOS capacitor, which are particularly important because their values may be rather high and also very dependent on the fabrication process. Typically, the value of the bottom-plate parasitic capacitance is in the range 5% to 20% of the nominal capacitance value, while the range for the top-plate parasitic capacitance value is of the order of 0.1%-2% [1.7],[1.11].

In order to minimise the effect of the grounded parasitic capacitances in SC circuits the top and bottom plates of the capacitors may be arranged as shown in Fig.1.5, for the case of the SC integrator considered

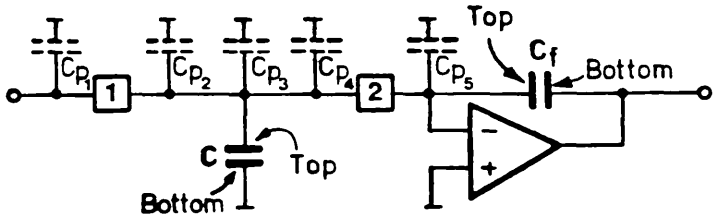


Fig.1.5: SC integrator with TSC branch

before. In this way, the operation of this SC circuit will be affected only by the switch parasitic capacitances C_{p2} and C_{p3} and by the top-plate parasitic capacitance C_{p4} which, essentially, modify the effective capacitance value C of the SC branch. The effect of the large bottom-plate parasitic capacitances has been eliminated by connecting these plates to ground (capacitor C) and to the low impedance output terminal of the OA (capacitor C_f). The parasitic capacitance C_{p1} is charged permanently by the input voltage source, and, therefore, it does not affect the performance of the circuit. The parasitic capacitance C_{p5} is also harmless because it is connected between ground and the virtual ground of the OA (infinite gain) and thus is never charged. In order to take into account the effect of the parasitic capacitances C_{p2}, C_{p3} and C_{p4}, we can use a new capacitance value C' of the SC branch such that $C'=C-C_{p2}-C_{p3}-C_{p4}$. However, since the values of the

parasitic capacitances can not be predicted exactly, they may impair the accuracy of this SC integrator and, in general, of SC circuits using this type of SC branch, which is known as the Toggle-Switched Capacitor (TSC) [1.35]. Nevertheless, TSC branches may still be employed whenever their effect on the operation of SC circuits can be neglected.

A solution to eliminate the effect of the above parasitic capacitances is to consider the Parasitic-Compensated Toggle-Switched Capacitor (PCTSC) branch shown in the SC integrator of Fig.1.6 [1.36]. As we saw before,

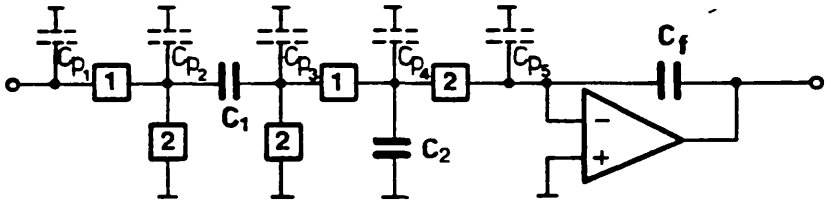


Fig.1.6: SC integrator with PCTSC branch

the parasitic capacitances C_{p1} and C_{p5} do not affect the operation of the circuit. The parasitic capacitance C_{p2} is also unimportant because in phase 1 it is charged to the input voltage, and, in phase 2, it is discharged to zero voltage. For the parasitic capacitances C_{p3} and C_{p4}, it can be shown that their effect is eliminated by a mechanism of compensation requiring [1.36]

$$\frac{C_1}{C_2} = \frac{C_{p3}}{C_{p4}} \qquad (1.5)\ \ldots$$

In this case it suffices to ensure that the parasitic capacitances are matched, rather than having to know their absolute values as before. In practice, however, this renders the layout of such SC circuits rather critical and thus PCTSC branches are employed only when the accuracy of TSC branches is inadequate (e.g. [1.37]).

The SC integrators shown in Fig.1.7-a and in Fig.1.7-b [1.38] contain SC branches, respectively known as Toggle-Switched Inverter (TSI) and Open Floating Resistor (OFR) [1.35], whose effective capacitance values are not affected by grounded parasitic capacitances.

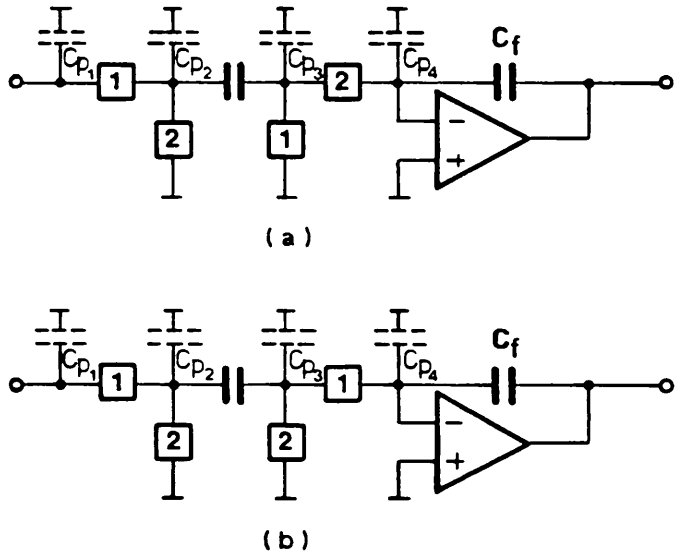


Fig.1.7: SC integrators insensitive to grounded parasitic capacitances. (a) TSI branch (positive integrator); (b) OFR branch (negative integrator)

In general, in order to design SC filter circuits which are insensitive to grounded parasitic capacitances it is

required to satisfy the following constraints [1.39]:
1. In each switch phase of an SC circuit, the nodes of the circuit must be connected to ground, to the virtual ground and output terminal of the OA's, or to the input terminals.
2. A plate of a capacitor must never be switched between virtual ground and either an input terminal or the output terminal of an OA.

The SC integrators in Fig.1.7 are commonly designated parasitic-insensitive SC integrators. In strict sense such designation is accurate only when referring to the grounded parasitic capacitances considered in the above discussion. Other parasitic capacitances, such as those associated with the control terminals of the analogue switches, also affect the operation of the SC integrators, mainly with respect to the DC offset voltage and harmonic distortion [1.40]. It has been found that such effects are critically dependent on the characteristics of the switching waveforms of the SC integrators, and can be substantially reduced by adopting appropriate switching schemes [1.40].

1.3.2 Accuracy of capacitance ratios

In the so called parasitic-insensitive SC integrators, in Fig.1.7, the accuracy of the time constants is essentially determined by the ratio between two capacitance values. The capacitance values in an MOS IC depend on the areas of the corresponding capacitors and also on the oxide capacitance per unit area, C_{ox}, as illustrated in Fig.1.8 [1.7],[1.11],[1.41]. For small capacitor areas (e.g. A_1,A_2 $<2500\mu m^2$) we can assume that C_{ox} is uniform and hence the

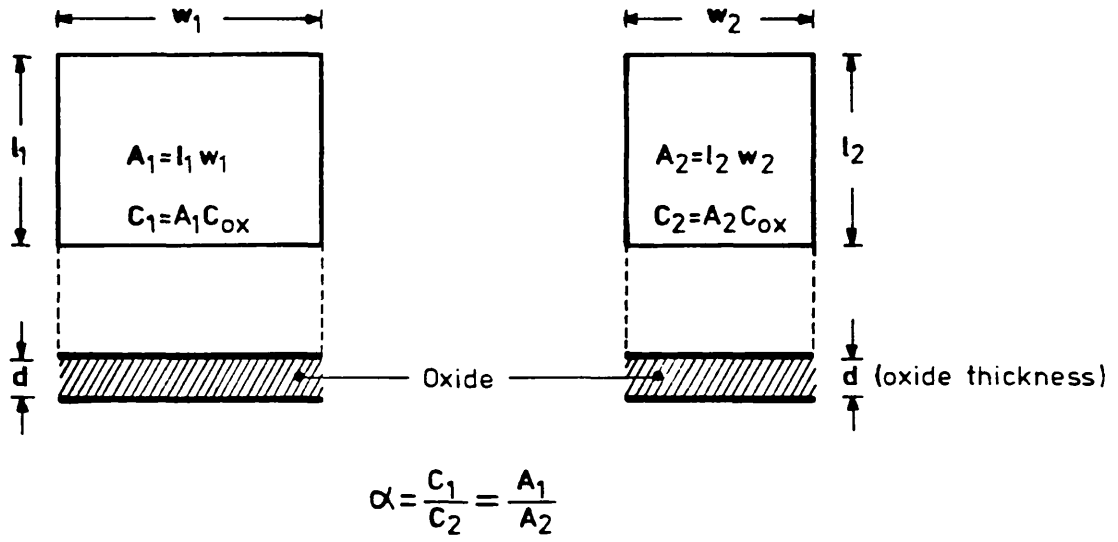


Fig.1.8: Geometric aspects of MOS capacitors and capacitance ratio

capacitance ratio $\alpha=C_1/C_2$ is determined by the ratio between the areas of two capacitors, i.e. $\alpha=A_1/A_2$. The accuracy of small capacitor areas, and therefore their ratio, is affected by edge errors due mainly to uniform undercut (over-etching) and, to a less extent, to random edge variation (mask defects, photolithographic innaccuracies), as illustrated in Fig. 1.9-a [1.41],[1.42]. In practice, such errors imply a minimum capacitor area in an IC SC filter of typically about $400\mu m^2$ [1.7], because below this limit the accuracy degrades considerably. One remedy for minimising the effect of edge errors in MOS capacitors is to increase their areas, in which case the errors due to capacitance oxide variations, Fig.1.9-b, become larger [1.41],[1.43]. Large capacitor areas also increase the total silicon area required for implementation which, in turn, reduces the yield and increases the cost of

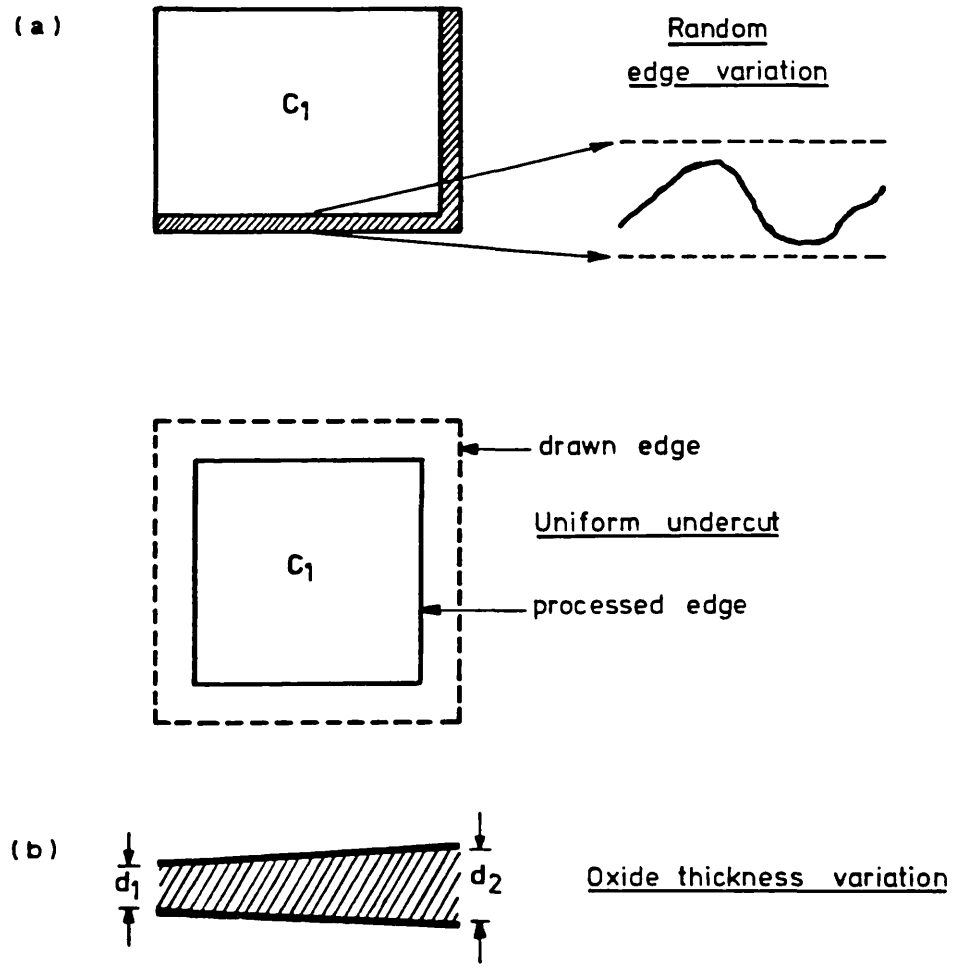


Fig.1.9: (a) Edge errors in MOS capacitors
(b) Oxide thickness variation

manufacturing. Hence, the maximum acceptable capacitor area in an IC SC filter is limited typically to about 40000μm^2 [1.7]. For the range of capacitor areas between 400μm^2 and 40000μm^2, the accuracy of capacitance ratios varies between 0.5%-1%, for large ratios (e.g. $50<\alpha<100$), and can be as low as 0.1%, for ratios close to unity [1.41],[1.7].

1.4 TIME-DOMAIN ANALYSIS OF SC CIRCUITS

The SC circuits that we shall consider in this thesis consist, in general, of the interconnection of simpler SC subcircuits with the single amplifier structure shown in Fig.1.10, comprising a number of feedforward and feedback branches with switched and unswitched capacitors.

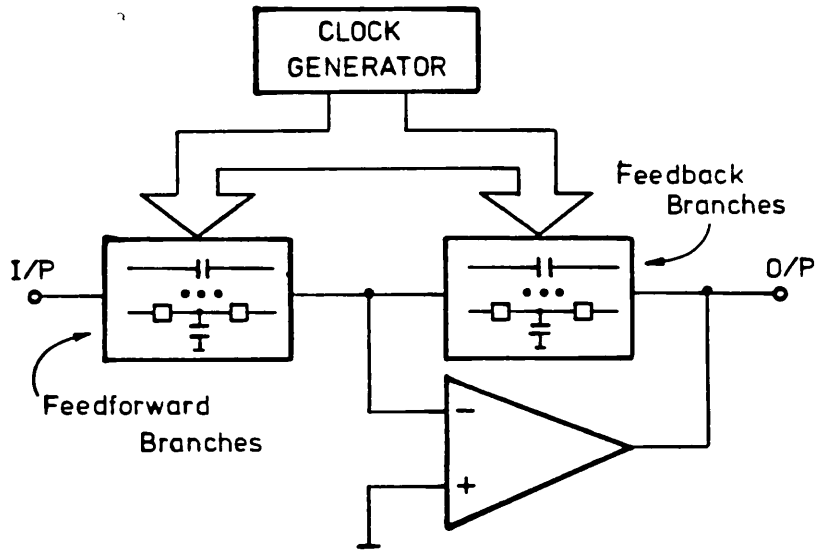


Fig.1.10: General single amplifier SC structure

The switched-capacitor branches may operate with uniform two-phase switching schemes, i.e. two switching waveforms with the same duty-cycle[1] and with the same switching period, as in the previous SC integrators, or they may require arbitrary multiphase switching schemes with different duty-cycles and even different switching periods. In either case, it is desirable to obtain the transfer function of such single amplifier SC circuits in a

[1] The duty-cycle of the switching waveform is the time when it is high relative to the switching period.

straightforward manner, e.g. simply by inspection of the feedforward and feedback branches, and of the switching scheme. This will be illustrated by means of an example.

The SC circuit given in the example of Fig.1.11-a contains one unswitched capacitor branch in the feedback loop of the OA, and three feedforward SC branches, which we considered in previous circuits, operating with arbitrary switching waveforms. It is convenient to interpret the operation of each SC branch in two phases: in the sampling phase, the switched-capacitor is connected to the input voltage source; in the charge transfer phase, the switched-capacitor is connected to the virtual ground of the OA. Such mechanisms of operation of the SC circuit, as well as the other mechanisms of charge storage and voltage holding, are illustrated by means of the waveforms of the input voltage, the capacitor voltages and the output voltage shown in Fig.1.11-b. Starting with the TSI branch with capacitor C_1, we have the following sequence of sampling and charge transfer:

At the beginning of the sampling phase (slot 1),[2] i.e. at $t=t_1^+$, capacitor C_1 charges instantaneously to the input voltage; during the sampling phase, the voltage across C_1 follows the input voltage; at the end of the sampling phase, i.e. at $t=t_2^-$, the capacitor samples the value of the input voltage at that instant, thus the sampling instant occurs at the end of the sampling phase. The

[2] Time slots, or simply slots, designate the time intervals when the switching waveforms are high.

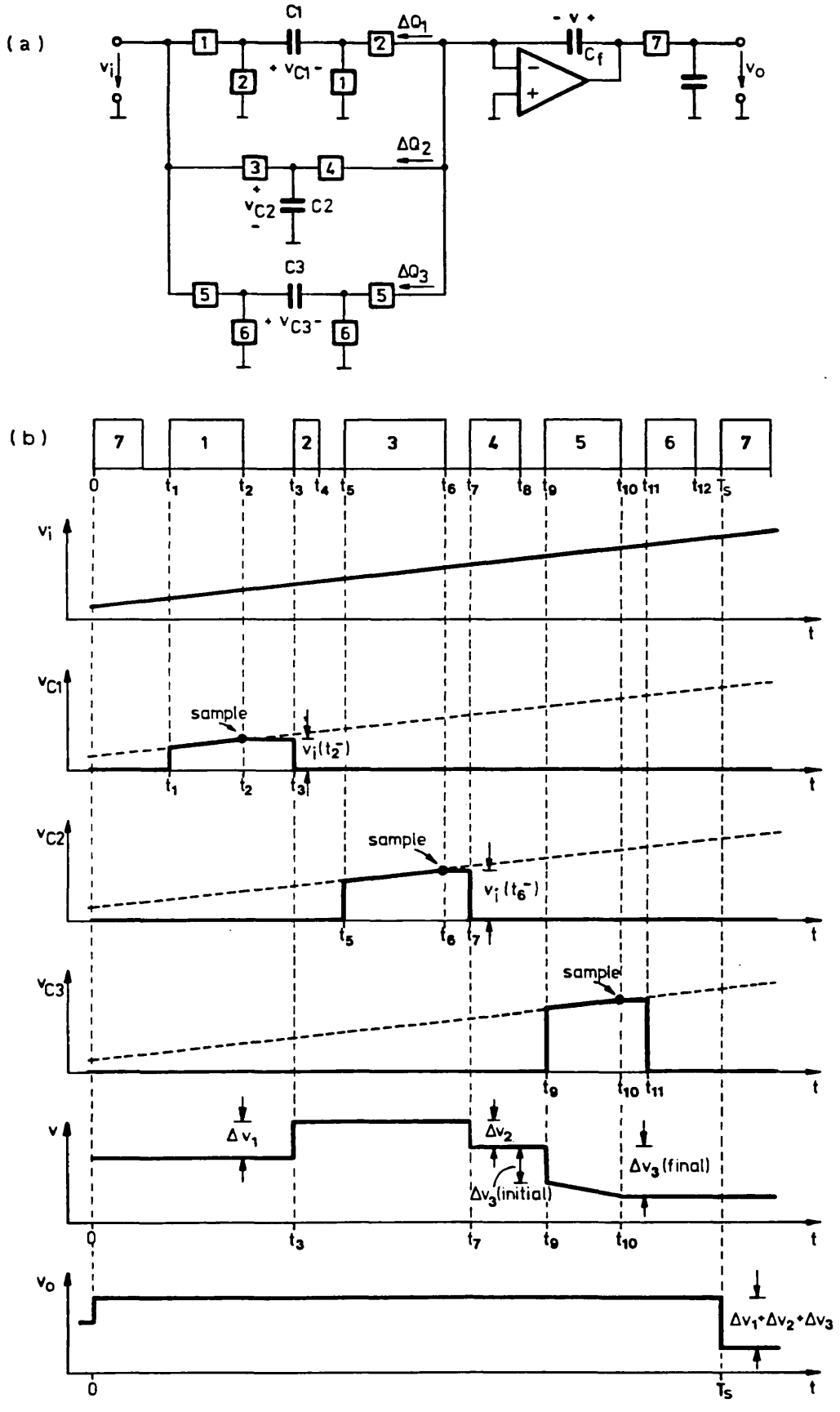


Fig.1.11: Illustration of time-domain operation of SC circuits

interval of charge storage occurs from $t=t_2^+$ to $t=t_3^-$; at $t=t_3^+$ (slot 2) C_1 discharges to zero voltage yielding a packet of charge $\Delta Q_1=C_1.v_i(t_2^-)$ transferred into the feedback capacitor C_f with the polarity indicated, thus the instant of charge transfer occurs at the beginning of the phase of charge transfer. The incremental voltage produced at the output of the amplifier by this SC branch is given by

$$(1.6\text{-a}) \ldots \qquad \Delta v_1 = \left(\frac{C_1}{C_f}\right).v_i(t_2^-)$$

Similar operations occur for the TSC branch with capacitor C_2 during slots 3 and 4; at $t=t_7^+$, the incremental output voltage produced at the output of the amplifier is given by

$$(1.6\text{-b}) \ldots \qquad \Delta v_2 = -\left(\frac{C_2}{C_f}\right).v_i(t_6^-)$$

With respect to the OFR branch with capacitor C_3, the switching phase is such that the operation of charge transfer in slot 5 occurs at the same instant $t=t_9^+$ as the charge of C_3, thus yielding an initial increment $\Delta v_3=-(C_3/C_f).v_i(t_9^+)$ of the amplifier output voltage; the final increment of the amplifier output voltage is obtained at the end of slot 5 yielding

$$(1.6\text{-c}) \qquad \Delta v_3 = -\left(\frac{C_3}{C_f}\right).v_i(t_{10}^-)$$

At the beginning of slot 6 the capacitor C_3 discharges to zero voltage. In slot 7, the output capacitor stores the

voltage at the output of the amplifier and holds that value until a new slot 7 begins. Hence, during two consecutive instants $t=0^+$ and $t=T_s^-$ the operation of the SC circuit is described by the input-output equation

$$(1.7)\ \ldots \qquad v_o(T_s)-v_o(0) = \left(\frac{C_1}{C_f}\right).v_i(t_2) - \left(\frac{C_2}{C_f}\right).v_i(t_6) - \left(\frac{C_3}{C_f}\right).v_i(t_{10})$$

which can be expressed directly in terms of fractional powers of the discrete-time complex variable Z as [1.44],[1.45]

$$(1.8)\ \ldots \qquad (Z-1).V_o(Z) = \left[\frac{C_1}{C_f}.Z^{t_2/T_s} - \frac{C_2}{C_f}.Z^{t_6/T_s} - \frac{C_3}{C_f}.Z^{t_{10}/T_s}\right].V_i(Z)$$

The term in the left-hand side of the above equation represents the periodic incremental variation of the output voltage of the SC circuit; the terms in the right-hand side represent periodic impulse sampled signals corresponding to the sampling operation of the SC circuit, and which can be determined simply by inspection of the SC branches and of the corresponding time slots. Finally, the discrete-time transfer function H(Z) of the SC circuit in Fig.1.11-a is expressed as

$$(1.9)\ \ldots \qquad H(Z) = \frac{V_o(Z)}{V_i(Z)} = \frac{1}{C_f} \cdot \frac{C_1 Z^{t_2/T_s} - C_2 Z^{t_6/T_s} - C_3 Z^{t_{10}/T_s}}{Z-1}$$

It would have been equally correct to express the equation (1.7) and the subsequent discrete-time equation (1.8) in terms of sequences of samples at the input and at

the output of the SC circuit [1.46],[1.47]. This suggests that we can consider the operation of SC circuits, with the ideal assumptions considered before, partly as the operation of an input sample circuit followed by an ideal discrete-time processor with discrete-time transfer function H(Z) [1.46],[1.47]. The sample and hold effect of the output signal which, we should note, does not appear in (1.7) or in (1.8) and therefore it does not appear in (1.9) either, corresponds to a continuous-time filtering operation at the output of the SC circuit. The interpretation of such an effect, as well as of the implications for the discrete-time operation of SC circuits have both to be examined in the frequency-domain, which we shall do in the next Chapter.

1.5 DESIGN METHODS FOR SC FILTERS

Because of the abundance of design methods for SC filters that are available in the literature, many of them having similar features, it is sometimes difficult to decide which method should be chosen for a particular application. One possible way of looking at this problem is to adopt a "top-down" strategy in which we consider fundamental options with respect to (i) structure of the filter (ii) derivation of transfer function and (iii) basic SC building block for implementation.

1.5.1 Filter structures

Starting with the structure of the SC filter, we can consider three major categories, namely recursive digital

direct-form, cascade, and ladder structures. Digital direct-form SC structures comprise SC multiply, delay and adder circuits which are interconnected in a recursive structure typical of digital filters [1.48]. Such structures are very sensitive to capacitance ratio errors and also to switch timing errors, both of which affect mainly the performance of the SC multiply and delay circuits. Furthermore, recursive digital direct-form SC structures require a large number of OA's for implementation, and therefore are not appropriate for realising high-order SC filters with high-precision frequency responses.

Cascade structures using SC biquadratic sections (biquads) yield a simple method of designing SC filters (e.g. [1.35],[1.49]-[1.52]), and are particularly attractive because of their suitability for custom and semi-custom SC filter design (e.g. [1.53]). Although the sensitivity of cascade SC biquad structures is too high for realising high-quality SC filters [1.35], it is still acceptable for many practical filtering applications which do not require high accuracy of the frequency response. This is the case for some of the SC bandpass filter systems described in Chapter 5, which employ such non-critical cascade SC biquad filters in conjunction with high-quality high-selectivity SC filters.

By adding feedforward and feedback branches to an SC cascade structure, it is possible to reduce the sensitivity of the SC filter response [1.35],[1.54] at the expense of

much more elaborate design techniques. Even so, for critical filtering applications, the sensitivity of this type of SC multifeedback structures is not as low as it is possible to achieve with the type of structures considered next.

The most widely used low-sensitivity filter design techniques are based on Orchard's observation that doubly terminated LC filters, usually with a ladder structure, designed to have maximum power transfer at the passband loss minima frequencies, have very low sensitivity of the frequency response with respect to variations of their nominal component values [1.55]. This led Orchard to suggest that a close simulation of the transfer functions of such an LCR prototype filter, at that time by means of active-RC circuits, would also preserve this desirable property. The same principle has been generally applied to the design of low-sensitivity SC filters which, from a conceptual point of view, have largely benefited from the vast amount of knowledge available in the context of active-RC filters (e.g. [1.34],[1.56],[1.57]). SC filter structures based on the simulation of LCR ladder prototype filters, which became known as SC ladder filters, are indispensable for the realisation of high-quality SC filters (e.g. [1.4],[1.7]-[1.10],[1.58]). There are also some types of SC ladder filters which are derived by means of direct synthesis techniques [1.59]-[1.61].

1.5.2 Discrete-time transfer functions

For a given SC filter structure, it is required to obtain the discrete-time transfer function H(Z) in order to represent as closely as possible a desired continuous-time transfer function $H_a(\tilde{s})$. Such a process involves a transformation $\tilde{s}=F(Z)$ between the continuous-time complex variable $\tilde{s}=j\tilde{\omega}$ and the discrete-time complex variable $Z=e^{j\omega T_s}$, such that

$$H(Z) = H_a(\tilde{s})\Big|_{\tilde{s} = F(Z)} \qquad (1.10)$$

F(Z) must be rational in Z in order to ensure realisability of H(Z) (assuming $H_a(\tilde{s})$ is realisable) and, ideally, it should possess the following two additional properties [1.35],[1.46]:

1. Mapping of the continuous-time $j\tilde{\omega}$ axis onto the discrete-time unit circle $e^{j\omega T_s}$, in order to preserve the continuous-time amplitude/frequency response.
2. Mapping of the continuous-time left-half plane inside the unit circle, in order to preserve stability.

The best known $\tilde{s}$-to-Z transformations are Backward Difference (BD) (or backward Euler), Forward Difference (FD) (or forward Euler), Lossless Discrete Integrator (LDI) and Bilinear (BL) whose definitions, and mapping characteristics, are summarised in Table1.1. The BD and the FD require that $\omega T_s << 1$, because they do not map the $j\tilde{\omega}$ axis onto the unit circle. Additionally, the FD transformation may not even preserve stability since part

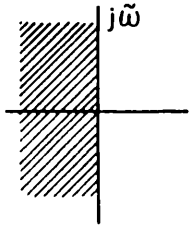
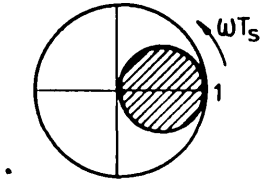
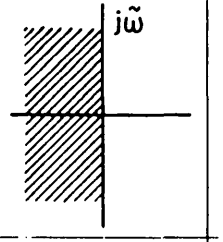
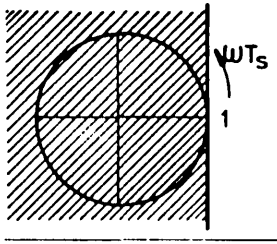
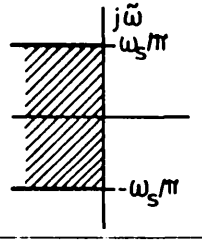
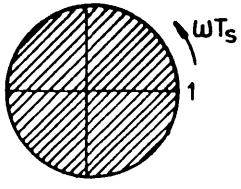
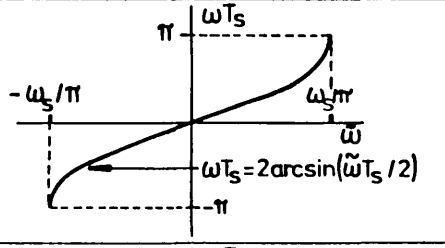
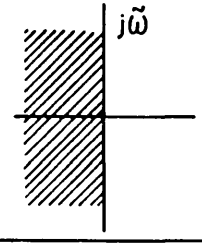
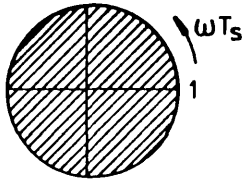
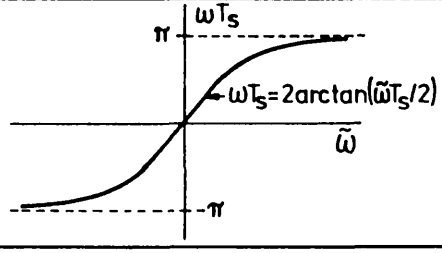
TRANSFORMATION	F(Z)	MAPPING		WARPPING EFFECT
		Continuous-time	Discrete-time	
Backward Difference(BD)	$\frac{1}{T_s}.(1-Z^{-1})$			
Forward Difference(FD)	$\frac{1}{T_s}.\left(\frac{1-Z^{-1}}{Z^{-1}}\right)$			
Lossless Discrete Integrator (LDI)	$\frac{1}{T_s}.\left(\frac{1-Z^{-1}}{Z^{-1/2}}\right)$			
BiLinear (BL)	$\frac{2}{T_s}.\left(\frac{1-Z^{-1}}{1+Z^{-1}}\right)$			

Table 1.1: Definitions, and illustration of mapping characteristics of $\tilde{s}$-to-Z transformations

of the continuous-time left-half plane maps outside the unit circle. The LDI transformation [1.62] maps only a portion of the $j\tilde{\omega}$ axis onto the unit circle, hence it does not preserve the overall continuous-time frequency response. The LDI transformation may be utilised when $\omega T_s << 1$ (e.g. [1.9]), otherwise it leads to errors of the frequency response which are not tolerable for high-quality SC filters. The BL transformation, on the contrary, maps the entire $j\tilde{\omega}$ axis onto the unit circle and therefore it does preserve the shape of the continuous-time frequency response, both in the passband, and in the stopband. This property is indispensable when the ratio of the switching frequency to the band-edge frequency of the SC filter is low, which is usually the case in highly selective SC filters such as those considered in this thesis. In Chapter 3, and in Chapter 5, we shall consider in detail the use of the BL transformation to derive the desired discrete-time transfer function of SC filters, paying special attention to the frequency warping effect that is also indicated in Table 1.1.

1.5.3 Basic building blocks

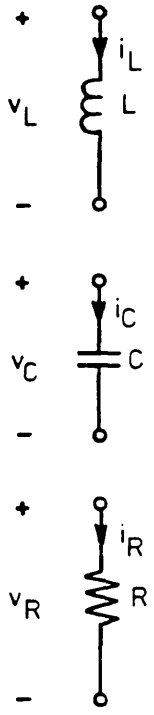
The basic building blocks considered here are employed to implement SC filters with the following characteristics: (i) they utilise a ladder structure with low sensitivity with respect to variations of the component values and (ii) they employ the BL transformation for derivation of the discrete-time transfer function, yielding accurate mapping of the desired continuous-time frequency response. SC

filters with such characteristics are usually called bilinear SC ladder filters [1.63]-[1.69].

One method for realisisng bilinear SC ladder filters is by component simulation of an LCR ladder prototype filter [1.64]. This consists of replacing each component L, C and R of the continuous-time prototype by their corresponding bilinear discrete-time one-port SC circuits. In this method, the OA's are needed only to implement the bilinear SC inductor and thus the resulting SC filters employ a reduced number of OA's (equal to the number of L's in the original LCR prototype). However, such SC filters are affected by parasitic capacitances and therefore this method is not practically useful for realising high-quality SC filters suitable for MOS IC fabrication [1.64].

There are several methods available in the literature for the design of parasitic-insensitive bilinear SC ladder filters [1.63],[1.65]-[1.69]. These methods are called operational simulation methods because the SC building blocks simulate equations of the corresponding LCR prototype filter. Such simulation, and the corresponding SC building blocks, may have different forms depending on a particular choice of variables.

(a) Lee/Temes/Chang/Ghaderi (LTCG) method [1.65]-[1.68]: The LTCG method is based on the simulation of the bilinear discrete-time equations relating the voltage and the incremental charge of inductors, capacitors and resistors of an LCR prototype filter, as illustrated in Fig.1.12-a. The incremental charge $\Delta Q(Z)$ represents the charge $Q(Z)$

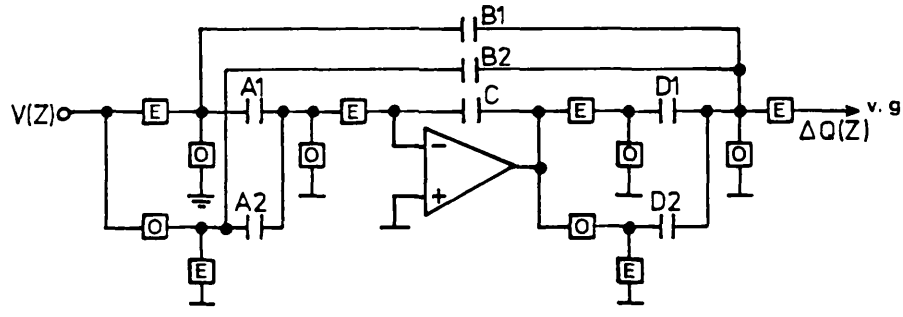


$$Q_L(\tilde{s}) = \frac{1}{\tilde{s}^2 L} V_L(\tilde{s}) \qquad \Delta Q_L(Z) = \frac{T_s^2}{4L} \cdot \frac{(1+Z^{-1})^2}{(1-Z^{-1})} \cdot V_L(Z)$$

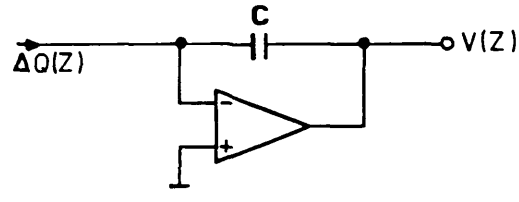
$$V_C(\tilde{s}) = \frac{1}{C} \cdot Q_C(\tilde{s}) \qquad V_C(Z) = \frac{1}{C} \cdot \frac{1}{(1-Z^{-1})} \cdot \Delta Q_C(Z)$$

$$Q_R(\tilde{s}) = \frac{1}{\tilde{s}R} \cdot V_R(\tilde{s}) \qquad \Delta Q_R(Z) = \frac{T_s}{2R} \cdot (1+Z^{-1}) \cdot V_R(Z)$$

(a)



Voltage-to-Dynamic Charge Converter



Dynamic Charge-to-Voltage Converter

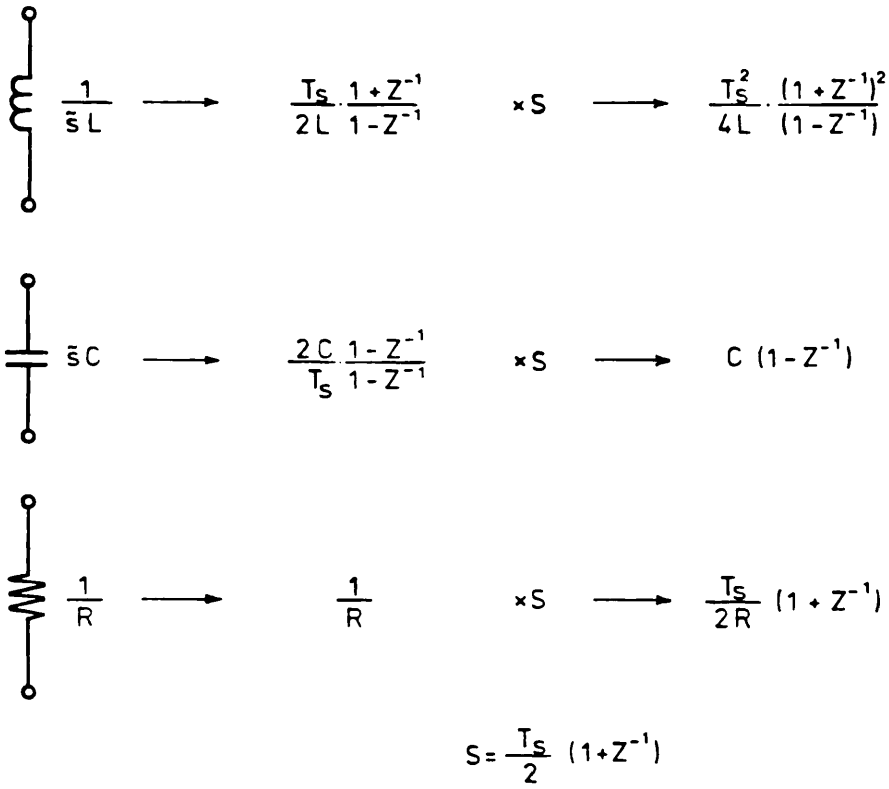
(b)

Fig.1.12: (a) Discrete-time equations and, (b) building blocks in the LTCG operational simulation method

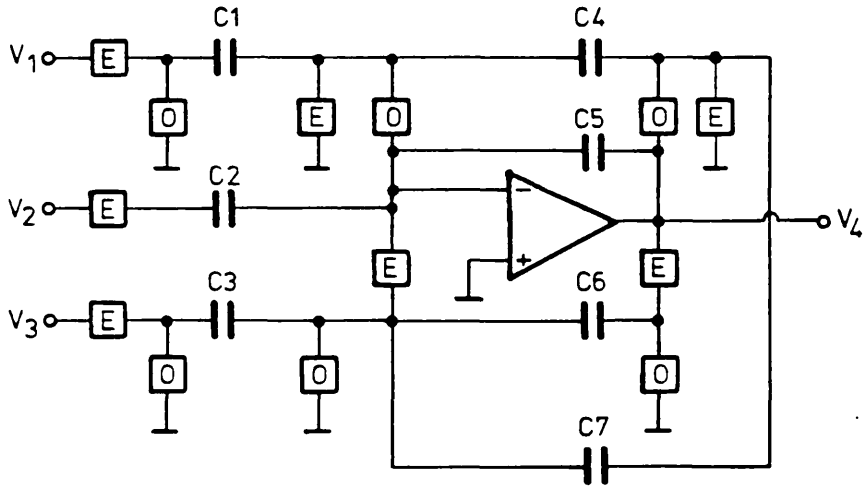
flowing during one switching period, i.e. $\Delta Q(Z)=Q(Z).(1-Z^{-1})$. Such equations can be implemented using the building blocks shown in Fig.1.12-b, where the SC voltage-to-dynamic charge converter building block constitutes a generalisation of the SC building blocks given in [1.65]-[1.68]. By considering this general SC voltage-to-dynamic charge converter building block, it is possible to derive bilinear SC ladder filters based on the LTCG method using a more systematic procedure than that described in [1.65]-[1.68]. This, however, will not be explored in this thesis, since we have come to adopt an alternative design method for the design of SC filters, as we shall explain later on.

(b) Bilinear-Transformed Admittance-Scaled (BITAS) method [1.69]: The bilinear discrete-time equations are obtained as illustrated in Fig.1.13-a: (i) the bilinear s̃-to-Z transformation is first applied to the immittances of the LCR prototype filter and (ii) the resulting discrete-time admittances are then scaled using a discrete-time scaling factor [1.70]. The general SC building block for implementation of the resulting bilinear discrete-time ladder is shown in Fig.1.13-b.

(c) Martin/Sedra (MS) method [1.63]: One form of the MS method is based on the simulation of bilinear-transformed discrete-time biquadratic equations relating the voltage and the current of generalised impedances in an LCR prototype filter [1.71],[1.72], as illustrated in Fig.1.14-a. An alternative form of the MS method consists of simulating the bilinear discrete-time biquadratic equations representing the interaction of the nodal

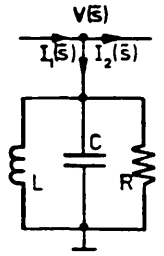


(a)



(b)

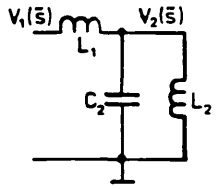
Fig.1.13: (a) Discrete-time equations in the BITAS operational simulation method; (b) General SC building block for implementation



$$V(\bar{s}) = \frac{\bar{s}L}{\bar{s}^2 LC + \bar{s}\frac{L}{R} + 1}\left[I_1(\bar{s}) - I_2(\bar{s})\right]$$

$$V(Z) = \frac{L\left(T_S/2\right)\left(1-Z^{-2}\right)}{\left[LC + \frac{T_S}{2}\cdot\frac{L}{R} + \left(\frac{T_S}{2}\right)^2\right] - 2\left[LC - \left(\frac{T_S}{2}\right)^2\right]Z^{-1} + \left[LC - \frac{T_S}{2}\cdot\frac{L}{R} + \left(\frac{T_S}{2}\right)^2\right]Z^{-2}}\left[I_1(Z) - I_2(Z)\right]$$

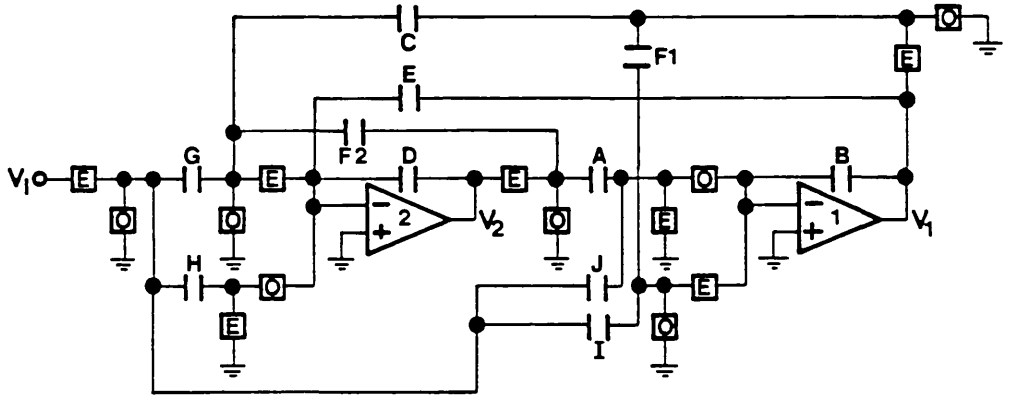
(a)



$$V_2(\bar{s}) = \frac{L_2}{L_1 + L_2}\cdot\frac{1}{\bar{s}^2\left(L_1 // L_2\right)C_2 + 1}\,V_1(\bar{s})$$

$$V_2(Z) = \frac{L_2}{L_1 + L_2}\cdot\frac{\left(T_S/2\right)\left(1 + Z^{-1} + Z^{-2}\right)V_1(Z)}{\left[\left(L_1 // L_2\right)C_2 + \left(\frac{T_S}{2}\right)^2\right] - 2\left[\left(L_1 // L_2\right)C_2 - \left(\frac{T_S}{2}\right)^2\right]Z^{-1} + \left[\left(L_1 // L_2\right)C_2 + \left(\frac{T_S}{2}\right)^2\right]Z^{-2}}$$

(b)



(c)

Fig.1.14: Discrete-time equations in the MS method corresponding to (a) generalised impedances and (b) interaction of the nodal voltages of an LCR prototytpe filter; (c) General SC biquad building block for implementation

voltages of an LCR prototype filter [1.73], as shown in Fig.1.14-b. In either form, the bilinear discrete-time biquadratic equations are simulated using SC biquads which can be obtained, for example, from the general SC biquad building block shown in Fig.1.14-c, which will be derived in Chapter 3. The resulting SC filter structures are usually known as coupled-biquad structures.

Despite their conceptual differences, the various operational simulation methods lead to SC circuits with similar sensitivity of the frequency response to capacitance ratio errors [1.74]. There are even situations where different operational simulation methods may lead to equivalent SC filter structures, as it has been shown for the case of the LTCG and MS methods [1.75]. It is therefore justified to employ one specific operational simulation method for realising high-quality SC filters as part of a general strategy for SC filter design, which we adopted in our research work. Such strategy is based on the use of SC biquadratic sections, not only for high-quality SC filters employing coupled-biquad structures -the MS method- but also for less critical SC filters using cascade structures. The MS method adopted in this thesis will described in detail in Chapter 5.

1.6 STATE-OF-THE-ART SC NARROW BANDPASS FILTERING

The degree of difficulty of realising an SC bandpass filter, as any bandpass filter, is usually measured in terms of its relative bandwidth

$$(1.10) \ldots \qquad B(\%) = 100.\left(\frac{BW}{f_o}\right)$$

where BW and f_o are the -3dB passband bandwidth and the midband frequency of the filter, respectively. Often, the equivalent Q-factor of the bandpass filter, i.e. Q=100/B, is also used to indicate the difficulty of the filter. According to the value of the relative bandwidth, we can consider the following three levels of difficulty of SC bandpass filters:

Wide-Band (WB) bandpass filters, when B$\geq$10%

Narrow-Band (NB) bandpass filters, when 1%$\leq$B$<$10%

Very Narrow-Band (VNB) bandpass filters, when B$<$1%

1.6.1 Conventional SC bandpass filters

The design of WB SC bandpass filters is well established in the literature. Such filters are obtained, for example, utilising any one of the operational simulation methods described above yielding SC circuits with acceptably low capacitance ratios, with low sensitivity of the frequency response to capacitance ratio errors, and with good dynamic range [1.63],[1.67]-[1.69].

The design of NB SC bandpass filters based on equivalent LCR ladder prototype filters becomes substantially more complicated because of the problem of large capacitance ratios which arise in the circuit. Capacitance ratio requirements greater than 100 are typical, which renders the frequency response rather affected by capacitance ratio errors. Besides, such large capacitance ratios are not practical for integrated circuit

fabrication on account of increased area, reduced yield, and thus increased cost of manufacturing. One possible solution to this problem consists of employing SC transformations, an example of which is shown in Fig.1.15 [1.35], in order to obtain an effective low capacitance value by subtraction of two higher capacitance values. For

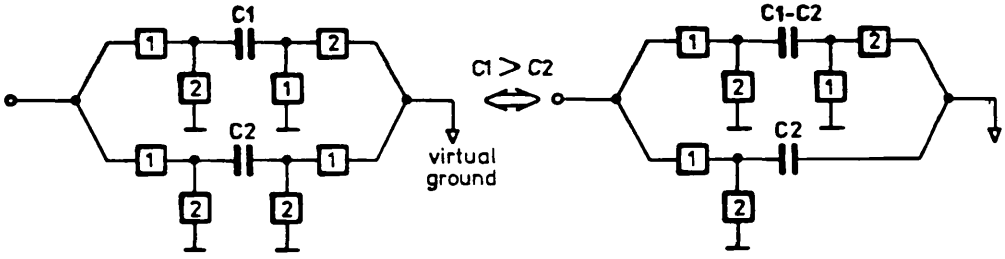


Fig.1.15: Example of a switched-capacitor transformation for capacitance ratio reduction

example, this technique has been used by Fischer and Moschytz [1.76] for the design of an SC biquad with low capacitance ratios. However, as Fischer and Moschytz observed, the sensitivity of the circuit with respect to capacitance ratio errors increases considerably due to the cancellation, which is not acceptable for high-selectivity filtering applications. An alternative solution available for the reduction of capacitance ratios consists of replacing the switched-capacitors by the capacitive-T network illustrated in Fig.1.16 [1.77]. The disadvantage of this approach is that it destroys the parasitic insensitive property of the circuit, which may lead to capacitance ratio errors of the order of 2% [1.77]. Appropriate IC layouts may reduce the effect of parasitic capacitances in

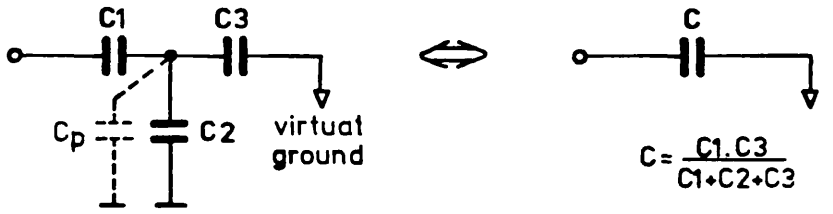


Fig.1.16: Example of a capacitive-T network transformation for capacitance ratio reduction

capacitive-T networks which may then be employed for implementing those capacitors whose capacitance value variations do not affect significantly the overall frequency response of the filter [1.78]. However, from a practical point of view, such an approach may not be very attractive, because the critical circuit layout renders the implementation of the SC filter more dependent on the fabrication process.

For VNB SC bandpass filters, it is no longer feasible to simulate an equivalent LCR ladder prototype filter, on account of the insurmountable problems of extremely large capacitance ratios arising in the SC filter, and high sensitivity of the frequency response to capacitance ratio errors which, together, lead to a large variability of the filter response. Typically, we find variations of the passband ripple of ideal VNB LCR prototype filters of the order of 10dB for 1% variation of their nominal component values, and the equivalent SC filter has capacitance ratios greater than 1000. For this range of VNB bandpass responses, and, in many cases, also for NB bandpass

responses, the solution has been to employ the N-Path (NP) SC filters that we review next.

1.6.2 SC N-path filters

The principle of NP filtering was introduced originally in the context of continuous-time active-RC filters [1.79]. It is based on a double frequency-translation operation in order to allow low selectivity filters at low frequency -the path filters- to realise the desired bandpass response with much higher selectivity, and, at higher frequency. In active-RC NP filters, such frequency translations are produced by means of conventional modulator circuits which precede and follow the path filters. In SC NP filters, on the other hand, the required frequency-translations simply result from the discrete-time nature of the SC path filters to be examined in the next Chapter.

One type of SC NP filter proposed in the literature employs a minimum of N=3 SC path filters with lowpass frequency response [1.80]-[1.83], as shown in Fig.1.17-a. It can be shown from the NP filtering theory [1.79],[1.84] that this type of 3-path filter produces a bandpass response at midband frequency $f_o=F_s$, Fig.1.17-b, which is formed by the joining of two frequency-translated bands of the lowpass path filters. It is also known that the unwanted frequency-translated components, generated along with the bandpass response, cancel out under the ideal conditions of perfect matching of the filter paths. In practice, however, since matching of the filter paths is

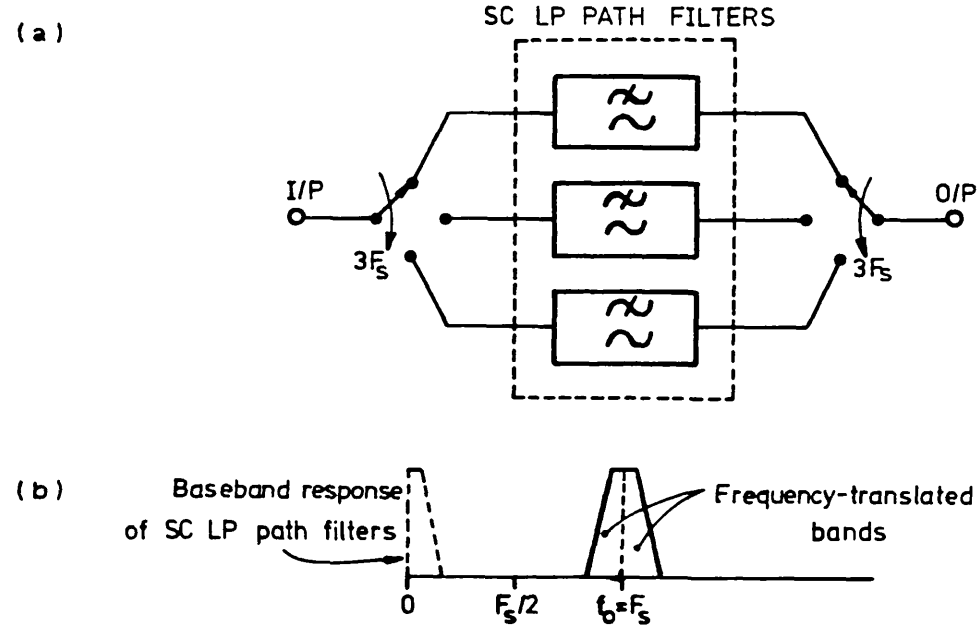


Fig.1.17: (a) SC NP filter model (N=3) using lowpass path filters; (b) Illustration of the formation of the bandpass response, with two adjacent frequency-translated bands

not perfect, such cancellation is incomplete giving rise to residual unwanted frequency-translated components in the passband, usually known as mirror frequency components, which degrade the dynamic range of the filter. The generation of mirror frequency components in this type of SC NP filter with lowpass path filters is illustrated in Fig.1.18. In Fig.1.18-a, an input frequency component at $F_s-\Delta f$ produces the wanted output frequency component at $F_s-\Delta f$ together with the unwanted mirror frequency component at $F_s+\Delta f$. Conversely, an input frequency component at $F_s+\Delta f$ produces the wanted frequency component at $F_s+\Delta f$ together with the unwanted mirror frequency component at $F_s-\Delta f$, as shown in Fig.1.18-b. Besides the problem of incomplete cancellation of such unwanted frequency-

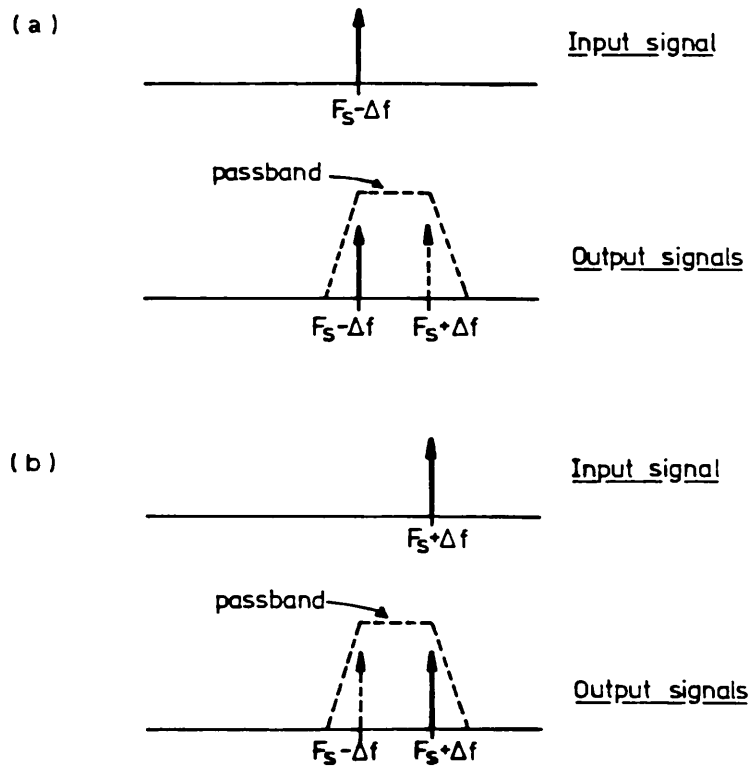


Fig.1.18: Mirror frequency components in SC NP filters with lowpass path filters. (a) Passband signal at $F_s-\Delta f$ generates an unwanted frequency-translated component at mirror frequency $F_s+\Delta f$; (b) Passband signal at $F_s+\Delta f$ generates an unwanted frequency-translated component at mirror frequency $F_s-\Delta f$

translated components, this type of SC NP filter also suffers from the problem of clock feedthrough occuring at midband frequency $f_o=F_s$. This degrades even further the overall noise performance of the filter.

The alternative type of SC NP filter proposed in the literature employs SC path filters with highpass, rather than lowpass, frequency response [1.85],[1.68]. SC NP filters with highpass path filters need only two paths

(N=2), Fig.1.19-a, in order to obtain a bandpass response centred at $f_o=F_s/2$. In this case, the bandpass response is formed by the joining of the baseband and the adjacent frequency-translated band of the path filters, as shown in Fig.1.19-b. Due to path mismatch, the mirror frequency

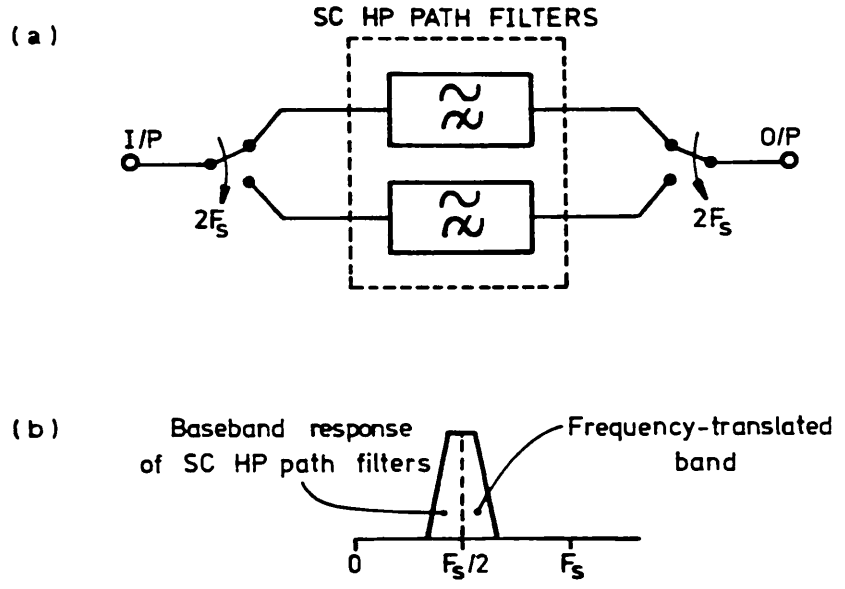


Fig.1.19: (a) SC NP filter model (N=2) using highpass path filters; (b) Illustration of the formation of the bandpass response, by the joining of the baseband and the adjacent frequency-translated band

components which occur at $F_s/2\pm\Delta f$, also lead to the generation of unwanted frequency-translated components in the passband (when Δf is small), as illustrated in the examples of Fig.1.20-a and Fig.1.20-b. This type of SC NP filter is, however, immune to the effect of clock feedthrough, which occurs outside the passband.

In order to eliminate the undesirable effect of mirror frequency components in NP filters, Fettweis and Wupper introduced the concept of pseudo NP filters [1.86], which

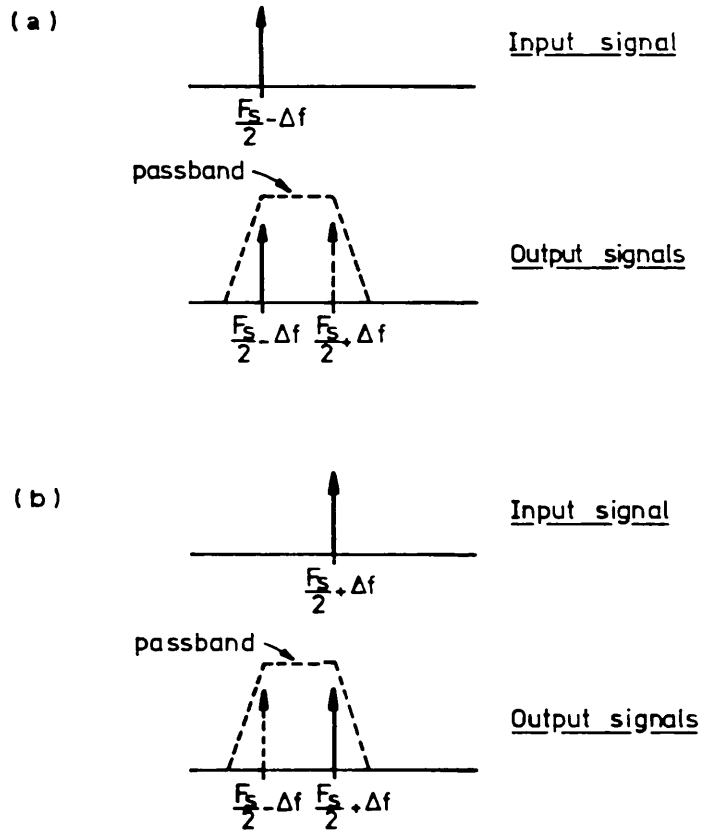


Fig.1.20: Illustration of the generation of mirror frequency components, at $F_s/2\pm\Delta f$, in an SC NP filter with highpass path filters

was subsequently applied to the realisation of SC pseudo NP filters [1.87],[1.88],[1.68]. In SC pseudo NP filters there is only one physical path which is multiplexed between the input and the output terminals, as represented schematically in Fig.1.21, thus the problem of path mismatch is ideally overcome. However, there are imperfections of SC circuits affecting the operation of multiplexing, as a result of which SC pseudo NP filters are not totally immune to the effect of mirror frequency components. As a matter of fact, although the solution of SC pseudo NP filters improves the mechanism for

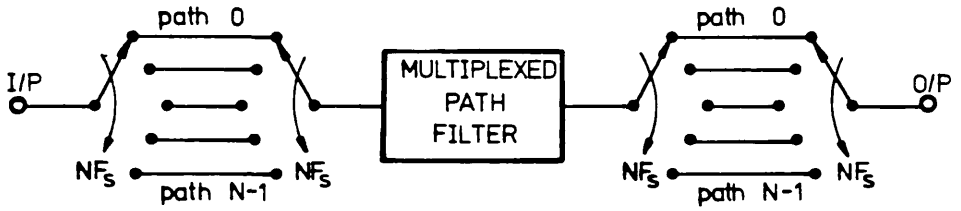


Fig.1.21: Schematic representation of a pseudo NP filter with multiplexing of a single path filter

cancellation of unwanted mirror frequency components, their level may still be too high for applications with high dynamic range [1.88],[1.68]. In addition to this problem, the dynamic range of SC pseudo NP filters is further aggravated because the SC circuits have been found to have poor noise performance, compared with true SC NP filters and conventional SC filters [1.89].

1.6.3 A summary of some practical realisations of SC bandpass filters

Table 1.2 summarises some aspects of the most relevant practical realisations of SC bandpass filters we are aware of. According to the degrees of difficulty defined earlier, all these SC bandpass filters have NB bandpass responses. Conventional SC bandpass filters have been preferably employed for the realisation of NB bandpass responses down to about 3%. For NB bandpass responses around 1%, SC NP filters have been employed instead. The SC bandpass filters indicated in 2, 6, 7, 8 and 10, are considered in the context of a complete SC bandpass filter system, which can be implemented in integrated circuit form using simple

SC BANDPASS FILTER	MIDBAND FREQUENCY	RELATIVE BANDWIDTH	SELECTIVITY	IMPLEMENTATION	REFERENCE
1 CONVENTIONAL LADDER SIMULATION	950 Hz	10.54% @ -0.25 dB	8th order General Parameter	Discrete Component	MARTIN et al [1.63]
2 CONVENTIONAL LADDER SIMULATION	10 KHz	10% @ -0.5 dB	6th order Chebyshev	Discrete Component	HAIGH et al [1.90]
3 PSEUDO NP FILTER N=3 LOWPASS FILTERS	2 KHz	10% @ -0.178dB	6th order Elliptic	Discrete Component	GHADERI et al [1.88]
4 NP FILTER N=4 LOWPASS FILTERS	1 KHz	5% @ -0.269dB	6th order Elliptic	Discrete Component	LEE et al [1.81]
5 PSEUDO NP FILTER N=2 HIGHPASS FILTERS	1 KHz	4% @ -0.178dB	6th order Elliptic	Discrete Component	GHADERI [1.68]
6 CONVENTIONAL LADDER SIMULATION	2.6 KHz	3.85% @ -3 dB	6th order Butterworth	Integrated Circuit	GREGORIAN [1.91]
7 CONVENTIONAL LADDER SIMULATION	3.825 KHz	3.66% @ -3 dB	10th order Chebyshev	Integrated Circuit	FUKAHORI [1.92]
8 CONVENTIONAL LADDER SIMULATION	260 KHz*	2.77% @ -3 dB	6th order Elliptic	Integrated Circuit	CHOI et al [1.78]
9 NP FILTER N=2 HIGHPASS FILTERS	1 KHz	1.27% @ -3 dB	2nd order	Integrated Circuit	DESSOULAVYet al [1.85]
10 NP FILTER N=4 LOWPASS FILTERS	1 KHz	1.15% @ -3 dB	4th order all pole	Integrated Circuit	GRUNIGEN et al [1.82]
11 NP FILTER N=4 LOWPASS FILTERS	10 KHz	0.95% @ -0.1 dB	6th order Chebyshev	Discrete Component	ALLSTOT et al [1.80]

* Application for intermediate frequency filter in radio receivers

Table 1.2: Aspects of some practical realisations of SC bandpass filters with narrow relative bandwidths

input and output continuous-time filters, as indicated in Fig.1.1c. For the remaining SC bandpass filters, it would have been necessary to design more complex continuous-time filters which, as we shall see in Chapter 2, are unsuitable for integrated circuit fabrication.

1.7 PURPOSE OF RESEARCH

The purpose of the work presented in this thesis is to study design techniques for audio-frequency SC bandpass filter systems, whith NB and with VNB bandpass responses, in order to overcome the problems of the methods currently available. These problems are large capacitance ratios and high sensitivity in conventional SC bandpass filters, and, in SC NP filters, poor dynamic range performance. Moreover, it is required that the systems should be suitable for integrated circuit fabrication. The key aspects of this work are described below.

The organisation of this thesis reflects aspects of SC circuit design, on the one hand, and development of SC system architectures, on the other hand. In this present Chapter (Chapter 1), we are primarily concerned with introductory aspects for analysis and design of SC circuits, besides the identification of the basic limitations of the state-of-the-art of SC narrowband bandpass filtering. Chapter 2 will deal with the principles of operation of an SC filter system, which, basically, are determined by the characteristics of an Anti-Aliasing Filter (AAF) and of an Anti-Imaging Filter

(AIF), respectively before and after the SC filter in the system. Hitherto, SC filter systems have operated in a baseband filtering mode, in which lowpass AAF and AIF select the baseband below $F_s/2$, and reject the unwanted frequency-translated bands above $F_s/2$. An important idea introduced in Chapter 2 concerns novel operating modes for SC filter systems, which consist of employing bandpass AAF and AIF to select input and output frequency-translated bands above $F_s/2$, and to reject the unwanted frequency-translated bands above $F_s/2$, as well as the baseband below $F_s/2$. Such systems, which we designate as Single-Path Frequency-Translated (SPFT) SC filter systems, are vital for the realisation of high-quality SC bandpass filter systems with VNB bandpass responses. In addition to the traditional input and output continuous-time filters, the AAF and AIF to be considered in this thesis also comprise sophisticated SC decimators and interpolators, respectively. SC decimators and interpolators are utilised to allow alteration of the sampling rate in SC systems, which requires appropriate frequency responses in order to eliminate the unwanted frequency-translated signal components arising in the processes of sampling rate alteration. In this context, we pay special attention to the derivation of optimum Finite Impulse Response (FIR) transfer functions which are suitable for decimation and interpolation applications for NB and VNB SC bandpass systems.

In the second part of this thesis, comprising Chapters 3 and 4, we shall describe design techniques for SC circuits required in SC filter systems. Chapter 3 concerns the development of general SC biquadratic sections (biquads) to be employed for high-quality coupled-SC biquad structures, as well as for cascade SC biquad structures with moderate sensitivity. A detailed capacitance ratio analysis allows us to design high quality-factor SC biquads with an optimum low value of the switching frequency yielding absolute minimum capacitance spread, which is crucial for the design of the NB SC bandpass filters in this thesis. This low value of the switching frequency implies a system requirement for attenuation of unwanted frequency-translated signals at low frequency, which can be efficiently done using the SC decimator and interpolator circuits to be developed in Chapter 4. In particular, the FIR SC decimator and interpolator circuits employing non-recursive polyphase structures are shown to be very attractive from the points of view of low capacitance ratios and high operating speed.

Chapter 5 will cover the aspects of the design and implementation of SC bandpass filter systems suitable for NB and VNB filtering applications. For the example of an NB bandpass response with -3dB relative bandwidth of 2.4%, we shall consider the design of a baseband SC bandpass filter system, with optimised capacitance spread, and efficient FIR SC lowpass decimators and interpolators to provide the required rejection of unwanted frequency-translated

signals. A VNB bandpass response with -3dB relative bandwidth of 0.48% will be realised using an SPFT SC filter system. In order to obtain the desired bandpass response for the decimator and interpolator, we shall discuss alternative architectures employing FIR and IIR (Infinite Impulse Response) SC circuits, whose performances are compared mainly from the points of view of capacitance ratios, operating speed, and, also, circuit complexity. One important requirement to be met by the SC interpolator in the AIF concerns the compensation for the attenuation of the selected frequency-translated band, which is due to the effect of the sample and hold signal at the output of the SC bandpass filter in the system. Both the NB and VNB SC filter systems are implemented using discrete component models. The experimental results confirm the operating principles, and demonstrate the good performance of the proposed systems with respect to the accuracy of the frequency response, dynamic range, and specified attenuation of the unwanted frequency-translated signals. In Chapter 5, we shall also demonstrate the operation of SPFT systems as single sideband generators and detectors, i.e. corresponding to the selection of input and output frequency bands at different frequencies.

The material that we shall present in Chapter 6 constitutes an exploratory investigation of a type of SC NP filter systems, using bandpass path filters, which are intended to overcome the attenuation problem of SPFT systems, and, also, the limitations concerning the poor

dynamic range performance of conventional SC NP filter systems using lowpass and highpass path filters.

The main results obtained in this thesis will be summarised in Chapter 7. There, we shall also present some suggestions for possible further research in this area of SC circuits and systems for narrow bandpass filtering, as well as further potential applications for frequency-translated SC filter systems, both with conventional SC bandpass filters and with SC NP filters using bandpass path filters.

1.8 STATEMENT OF ORIGINALITY

The following most significant results of the research work presented in this thesis are, to the best of our knowledge, original, and, as we indicate below, some of these results have been published (or accepted for publication):

- In Chapter 2, the introduction of operating modes for SC systems corresponding to the selection of frequency-translated bands above the Nyquist frequency, which represents a radically different approach to the way in which SC filter systems have been traditionally regarded. We quote from, for example, Reference [1.83]:
"... Because of the Nyquist theorem, sampled-data filters can only process input signals up to half of the clock frequency ..."

- In Chapter 3, the systematic procedure for the generation of SC biquads using signal flow graph techniques and the concept of optimum switching frequency leading to the design of SC biquads with absolute minimum capacitance spread. The design of an SC bandpass filter with optimum value of the switching frequency, and the resulting system implications of this, have been discussed in

[J.E.FRANCA, "Decimators and Interpolators for Narrowband Switched-Capacitor Bandpass Filter Systems", in Proc. IEEE ISCAS'84, pp.789-793, Montreal, Canada, May 1984]

- In Chapter 4, the work concerned with the design of SC decimator and interpolator circuits with optimum multinotch approximations for application of NB and VNB SC bandpass filter systems. In particular, we emphasise the comprehensive procedures introduced for the design of non-recursive polyphase SC structures for decimation and interpolation, which is the subject of the paper

[J.E.FRANCA, "Non-recursive Polyphase Switched-Capacitor Decimators and Interpolators", to be published in the IEEE Trans. on Circuits and Systems]

- In Chapter 5, the design of NB and VNB SC bandpass filter systems, respectively with baseband and frequency-translated operating modes, employing efficient architectures of SC circuits for decimation and interpolation. The proposal of SPFT SC bandpass filter systems constitute, in our opinion, the best solution available for the realisation of bandpass responses with very narrow relative bandwidths. The practical demonstration of an SPFT SC filter system for VNB bandpass

filtering applications is presented in

[J.E.FRANCA, "A Single-Path Frequency-Translated Switched-Capacitor Bandpass Filter System", to be published in the IEEE Trans. on Circuits and Systems].

An SPFT SC system with a new architecture for operation at higher frequency and improved rejection of unwanted alias and image signals, and, also, for demonstration of the operation as single sideband generator and detector, is described in

[J.E.FRANCA, "A Single-Path Frequency-Translated Switched-Capacitor System for Filtering and Single Sideband Generation and Detection", to be presented at the IEEE ISCAS'85, Kyoto, Japan, June 1985]

These systems have been the subject of one patent application which has been filed by the Ministry of Defence, [J.E.FRANCA, "Switched-Capacitor Circuits", British Patent Application No.8411547, 4th.May 1984], which describes the original idea of SPFT systems and gives preliminary experimental results obtained on a demonstration system. This patent application has been augmented to include further developments and new improved results on SPFT systems, which produced a new British Patent Application No.8511218, filed 2nd. May 1985, claiming priority from the British Patent Application No.8411547.

- In Chapter 6, the idea of SC NP filter systems combining the basic operating principles of NP filters employing bandpass path filters, and of SPFT systems. This is discussed in

[J.E.FRANCA, "On Switched-Capacitor Bandpass Filter Systems With Very Narrow Relative Bandwidths", to be presented at the ECCTD'85, Prague, Czechoslovakia, September 1985]

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CHAPTER 2

PRINCIPLES OF OPERATION OF SC FILTER SYSTEMS

2.1 INTRODUCTION

In the previous Chapter we examined the principles of operation of SC circuits and reviewed the basic aspects of the analysis and design of SC filters. This Chapter is concerned with the analysis of the spectral characteristics of SC filters and with their implications in the context of a complete SC filter system.

The analysis of the spectral characteristics of SC filters, in Section 2.2, shows two forms of ambiguity, known as aliasing and imaging. Aliasing refers to the multiplicity of components of the input continuous-time spectrum that relate to one component of the output discrete-time spectrum. Imaging, on the other hand, corresponds to the multiplicity of components of the discrete-time spectrum that are produced by one component of the continuous-time spectrum. In Section 2.3, we consider an SC filter system in which such ambiguities are eliminated by means of an Anti-Aliasing Filter (AAF) and an Anti-Imaging Filter (AIF), respectively before and after the SC filter, and whose shapes determine the operation mode of the system. In general, such filters employ a combination of low selectivity continuous-time active-RC filters together with specialised SC filters, called decimators and interpolators, which are introduced in Section 2.4. In Section 2.5 we describe a simple procedure for optimising the transfer functions of a class of SC decimators and SC interpolators which are ideally suitable for application in narrow and very narrow SC bandpass

filter systems. Finally, Section 2.6 summarises the Chapter.

2.2 SPECTRAL CHARACTERISTICS OF SC FILTERS

2.2.1 SC filter model

According to the time-domain operation described in the previous Chapter, we can represent an SC filter by means of the model shown in Fig.2.1. The sampling circuit

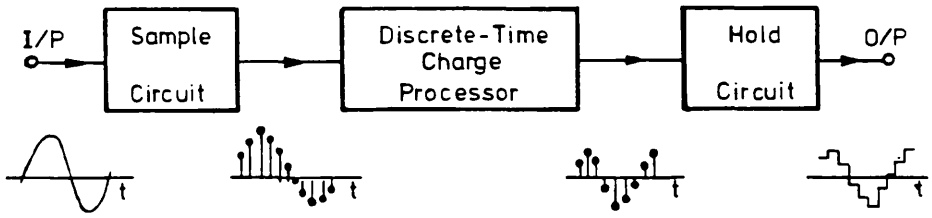


Fig.2.1: SC filter model

describes the operation of input voltage sampling, the discrete-time charge processor implements the discrete-time transfer function H(Z) of the SC filter and the hold circuit represents the effect of output voltage holding. After examining the spectral characteristics of each one of these circuits, we shall then discuss the overall spectral characteristics of SC filters.

2.2.2 Sampling operation: aliasing and imaging

The process of sampling illustrated in Fig.2.2 is viewed as an impulse train s(t), with sampling period $T_s=1/F_s$, modulating a continuous-time signal $x_a(t)$ yielding

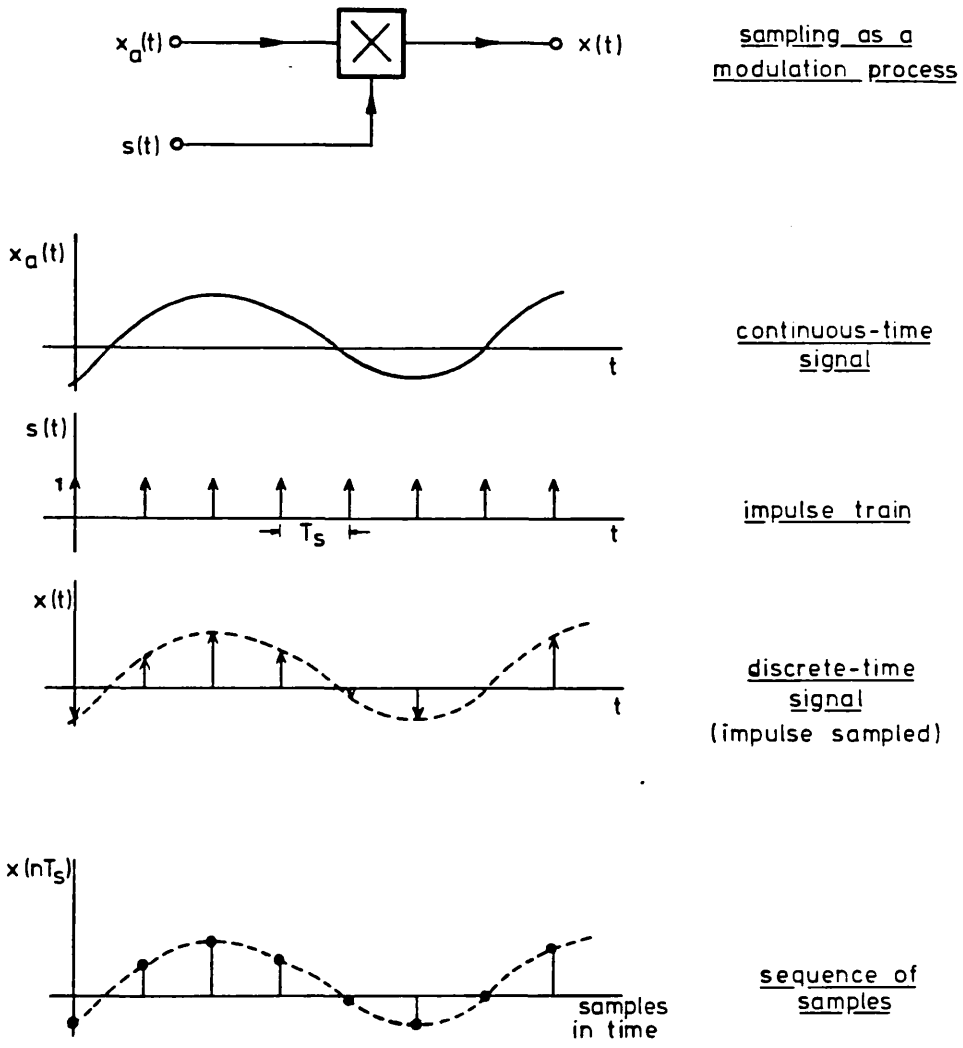


Fig.2.2: Illustration of impulse sampling operation

the discrete-time signal x(t). Mathematically, this signal can be expressed as [2.1]

$$(2.1) \quad \ldots \qquad x(t) = \sum_{n=0}^{\infty} x\,(nT_s).\delta(t-nT_s)$$

where $\delta(t)$ is the impulse (Dirac) function and $x(nT_s)$ represents the sequence of samples of the discrete-time (impulse sampled) signal. The Laplace transform of the

discrete-time signal (2.1) is given by [2.1]

$$(2.2)\ \ldots \qquad \mathcal{L}[x(t)] = X(s) = \sum_{n=0}^{\infty} x(nT_s).e^{-snT_s}$$

which yields the Fourier transform ($s=j\omega$)

$$(2.3)\ \ldots \qquad \mathcal{F}[x(t)] = X(j\omega) = \sum_{n=0}^{\infty} x(nT_s).e^{-j\omega nT_s}$$

If we express the Fourier transform of the impulse sampled signal (2.3) using the discrete-time variable $Z=e^{j\omega T_s}$, then we obtain

$$(2.4)\ \ldots \qquad \mathcal{Z}[x(nT_s)] = X(Z) = \sum_{n=0}^{\infty} x(nT_s).Z^{-n}$$

which corresponds to the definition of the Z-transform of the sequence of samples $x(nT_s)$ [2.2]. The link between the Z-transform (2.4) of the sequence of samples of a signal on the one hand, and both the Laplace (2.2) and the Fourier (2.3) transforms of the impulse sampled version of the signal on the other hand, is important for interpreting the transfer function of the discrete-time processor, which we shall examine later on.

In the frequency domain, the above operation of modulation corresponds to the convolution of the Fourier transforms of the impulse train and of the continuous-time signal. Mathematically, this can be expressed by [2.1]

$$(2.5)\ \ldots \qquad X(j\omega)=X[j(\tilde{\omega}-n\omega_s)] = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X_a[j(\tilde{\omega}-n\omega_s)] \qquad , \omega_s = 2\pi F_s$$
$$\omega = \tilde{\omega}-n\omega_s$$

where $X_a(j\tilde{\omega})$ represents the spectrum (Fourier transform) of a continuous-time signal before sampling, while $X(j\omega)$ represents the spectrum of the resulting discrete-time signal after sampling. This equation provides the fundamental link between the components of the continuous-time spectrum with frequency $\tilde{\omega}$, and the components of the discrete-time spectrum with frequency $\omega=\tilde{\omega}\pm n\omega_s$. The discrete-time frequency components such that $\omega=\tilde{\omega}$, i.e. for $n=0$, will be called baseband components, while the remaining components at $\omega=\tilde{\omega}-n\omega_s$ $(n\neq 0)$ will be called frequency-translated components. In the above equation (2.5), both ω and $\tilde{\omega}$ can be either negative or positive since they represent the argument of sine and cosine functions. However, we shall regard the frequencies always as positive measurable quantities with physical significance, i.e. representing the number of cycles per time-unit. Therefore, for $\tilde{\omega}>0$, we would write the difference frequency of the frequency-translated components as $\omega=\tilde{\omega}-n\omega_s$ if $\tilde{\omega}>n\omega_s$, and as $\omega=n\omega_s-\tilde{\omega}$ if $\tilde{\omega}<n\omega_s$.[1]

Let us now consider the discrete-time spectra produced by impulse sampling of two continuous-time frequency components $\tilde{\omega}_1$ and $\tilde{\omega}_2$ such that $\tilde{\omega}_2=\omega_s+\tilde{\omega}_1$, for example. For the case of the continuous-time frequency component $\tilde{\omega}_1$, in Fig.2.3-a, equation (2.5) leads to the discrete-time spectrum shown in Fig.2.3-b. However, the frequency-translated components with negative difference frequency,

[1] The corresponding phase inversion is not important in the present discussion.

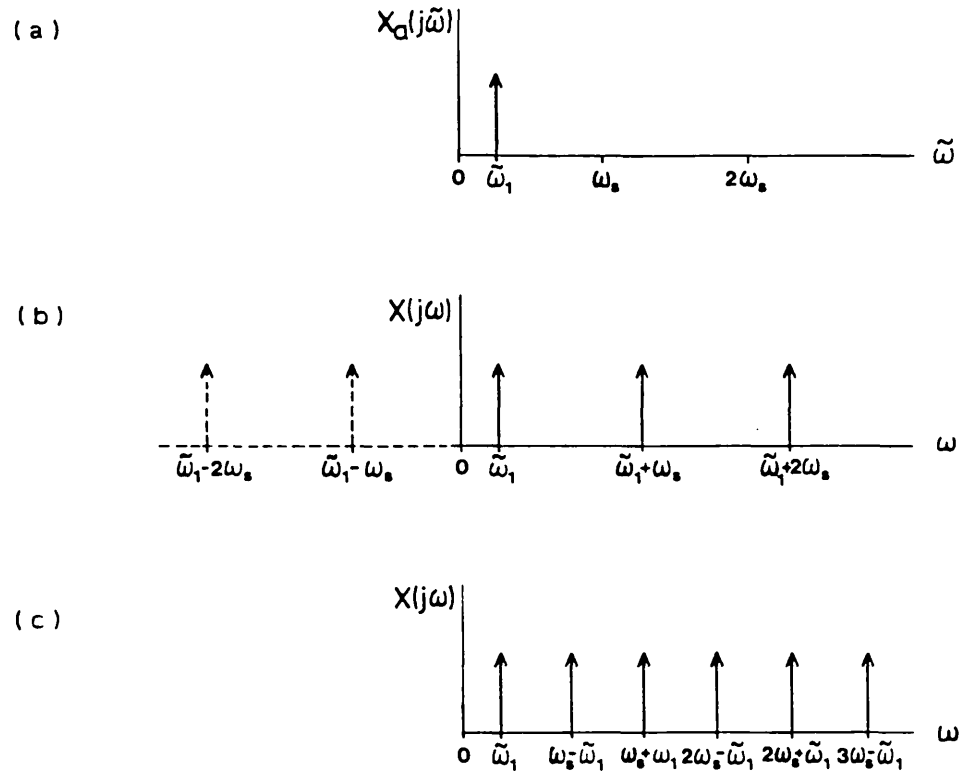


Fig.2.3: (a) continuous-time spectrum with component at frequency $\tilde{\omega}_1$; (b) resulting image spectrum with discrete-time components at positive and negative frequencies; (c) image spectrum with discrete-time components at positive frequencies

i.e. $\tilde{\omega}_1-n\omega_s$ $(n\geq 1)$, are represented as $n\omega_s-\tilde{\omega}_1$ $(n\geq 1)$ thus yielding the (measurable) discrete-time spectrum of Fig.2.3-c. This is called the <u>image</u> spectrum of the impulse sampled continuous-time signal with frequency $\tilde{\omega}_1$, and which consists of one baseband component at $\omega=\tilde{\omega}_1$ plus an infinite number of frequency-translated images at $\omega=n\omega_s\pm\tilde{\omega}_1$ $(n\geq 1)$. Fig.2.4 illustrates the formation of the image spectrum of the impulse sampled continuous-time signal with frequency $\tilde{\omega}_2$, which is obtained in a similar way as above. The continuous-time frequency components $\tilde{\omega}_2$ and $\tilde{\omega}_1$ yielding the same image spectrum, respectively in Fig.2.4-c and in

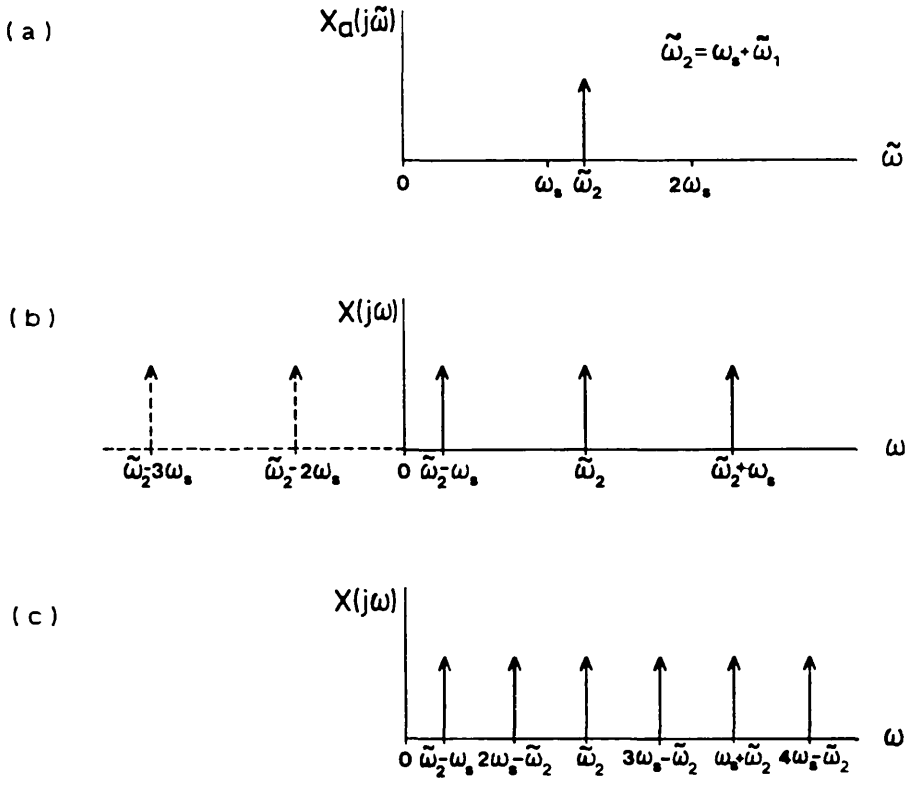


Fig.2.4: Formation of the image spectrum of the impulse sampled continuous-time component at frequency $\tilde{\omega}_2=\omega_s+\tilde{\omega}_1$

Fig.2.3-c, are called alias components. Aliasing distortion arises when the continuous-time spectrum contains at the same time both of the alias components at frequencies $\tilde{\omega}_1$ and $\tilde{\omega}_2$, Fig.2.5-a, in which case the resulting image spectrum Fig.2.5-b does not distinguish the frequency component $\tilde{\omega}_1$ from the frequency component $\tilde{\omega}_2$, and vice-versa. Therefore, in order to prevent aliasing distortion it is essential that the frequency components of the continuous-time spectrum are contained in only one of the frequency bands illustrated in Fig.2.6. If the continuous-time spectrum includes a DC component, then it must be bandlimited within the Nyquist band from DC to

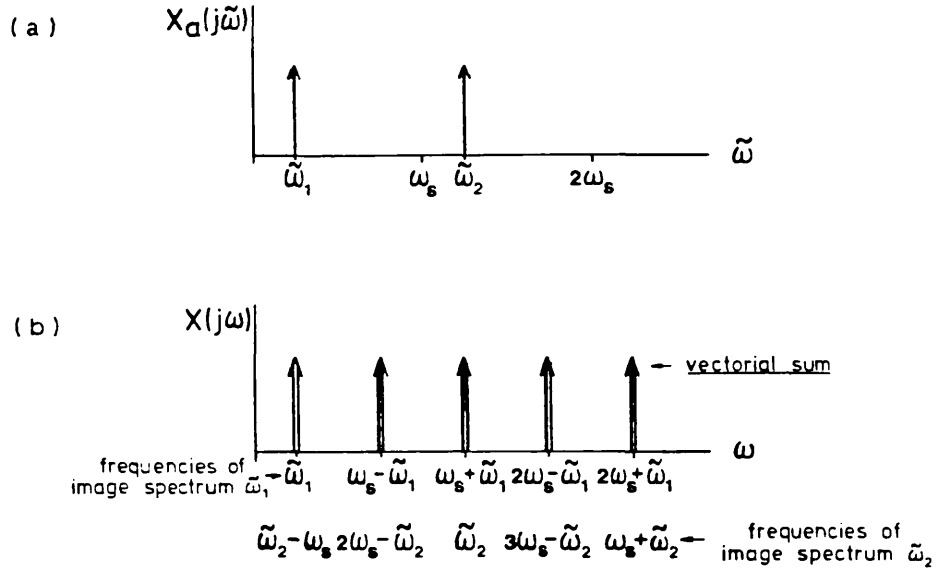


Fig.2.5: Impulse sampling of (a) two continuous-time alias components at frequencies $\tilde{\omega}_1$ and $\tilde{\omega}_2=\omega_s+\tilde{\omega}_1$ produces (b) aliasing distortion corresponding to the superimposition of the resulting discrete-time image spectra

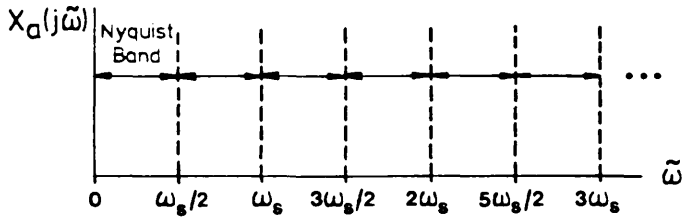


Fig.2.6: Continuous-time spectrum split-up into frequency bands that do not contain alias components

$\omega_s/2$, which is the result of the sampling theorem applied to lowpass responses [2.1],[2.2]. If the continuous-time spectrum does not include a DC component, then it can be bandlimited either within the Nyquist band below $\omega_s/2$ or within any other frequency band above $\omega_s/2$, which is a result of the sampling theorem applied to bandpass responses [2.3],[2.4]. The results illustrated in Fig.2.3,

in Fig.2.4 and in Fig.2.5 constitute the fundamental aspects of the sampling operation of SC filters, viewed in the frequency-domain, and which can be summarised as follows:

1. Each component of the continuous-time spectrum with frequency $\tilde{\omega}$ is characterised by one image spectrum with frequency components at $\omega=\tilde{\omega}\pm n\omega_s$.
2. The alias frequency components $\tilde{\omega}$ and $n\omega_s\pm\tilde{\omega}$ of the continuous-time spectrum produce the same image spectrum.
3. In order to prevent aliasing distortion, the continuous-time spectrum must not contain alias frequency components, i.e. two or more signals yielding the same image spectrum.

2.2.3 Discrete-time charge processor

The SC filter interpreted as a discrete-time charge processor with transfer function H(Z), is a linear time-invariant network which relates the sequence of samples $x(nT_s)$ at the input to the sequence of samples $y(nT_s)$ at the output, as indicated in Fig.2.7-a [2.1],[2.2]. We saw before that the sequence of samples at the input is characterised by the discrete-time spectrum $X(j\omega)$; then, the discrete-time output spectrum $Y(j\omega)$ is obtained using

$$Y(j\omega) = X(j\omega).H(j\omega) \qquad (2.6)\ \ldots$$

$H(j\omega)$ is the discrete-time frequency response of the discrete-time processor, which is determined by evaluating the discrete-time transfer function H(Z) on the unit circle

$Z=e^{j\omega T_s}$. The modulus of the frequency response yields the amplitude response $H(\omega)$, i.e.

$$(2.7)\ \ldots \qquad H(\omega) = \left| H\left(e^{j\omega T_s}\right) \right|$$

which is a periodic function of ω, as illustrated in the example of Fig.2.7-b. Hence, knowledge of the amplitude

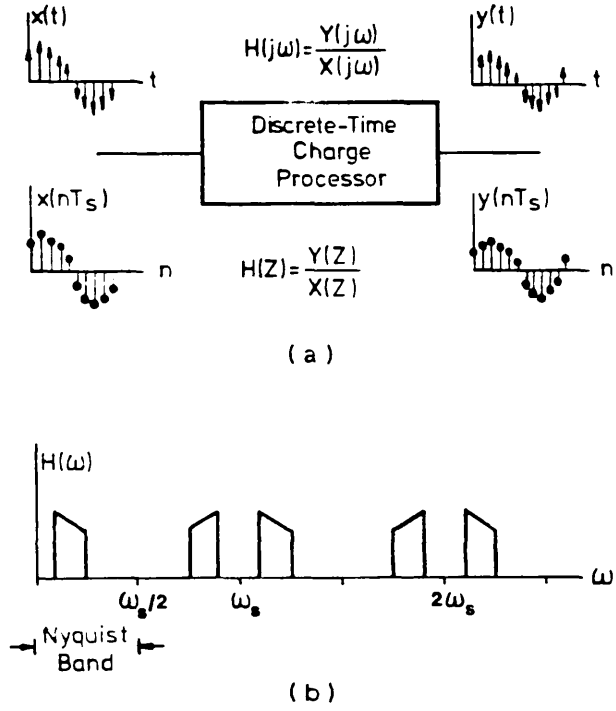


Fig.2.7: (a) SC filter viewed as a discrete-time charge processor; (b) Periodic amplitude response

response of the discrete-time charge processor in the Nyquist band $0<\omega<\omega_s/2$ is sufficient to obtain the amplitude response for all ω. Note that $H(\omega)$ defined in (2.6) and calculated in (2.7) represents a linear time-invariant amplitude response, and thus frequency components above $\omega_s/2$ are as valid as the frequency components below $\omega_s/2$. As we saw before, this requires a set of constraints on the

continuous-time spectrum $X_a(j\tilde{\omega})$ producing $X(j\omega)$ which is different from that required for the frequency components below $\omega_s/2$.

2.2.4 Hold effect

The hold circuit is a linear time-invariant network whose operation is illustrated in Fig.2.8-a. The impulse sampled signal at the output of the discrete-time charge

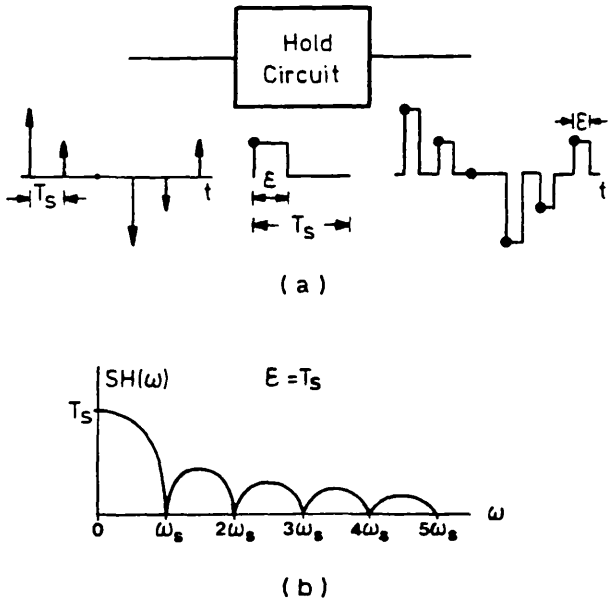


Fig.2.8: (a) Operation of the hold circuit and (b) corresponding amplitude response with full period held signal

processor is held constant during an interval of time $\varepsilon \leqslant T_s$, after which there is a return to zero in the remaining of the switching period T_s. This leads to the frequency response [2.1]

(2.8) ... $$SH(j\omega) = \frac{1 - e^{-j\omega\varepsilon}}{j\omega\varepsilon}$$

yielding the amplitude response

$$(2.9)\ \ldots \qquad SH(\omega) = \left|SH(j\omega)\right| = \varepsilon \frac{\sin(\omega\varepsilon/2)}{(\omega\varepsilon/2)}$$

Usually, the output signal of SC filters is held during the full switching period, i.e. $\varepsilon=T_s$, which implies the familiar sample and hold function plotted in Fig.2.8-b.

2.2.5 Interpretation of the discrete-time output spectrum of an SC filter

From equations (2.5), (2.6) and (2.9), the discrete-time output spectrum $Y(j\omega)$ of an SC filter is given by

$$(2.10)\ \ldots \qquad Y(j\omega) = \frac{1}{T_s} \sum_{n=0}^{\infty} \left[X(j\omega).H(j\omega).SH(j\omega)\right] \quad , \omega = \tilde{\omega} \pm n\omega_s$$

Assuming that the input continuous-time spectrum consists of only one frequency component at each time, i.e. we eliminate the vectorial summation of terms in (2.10), we can write the amplitude spectral characteristic of an SC filter, with full period sample and hold, as

$$(2.11)\ \ldots \qquad Y(\omega) = \left|Y(j\omega)\right| = X(\omega).H(\omega).\frac{\sin(\omega/2F_s)}{(\omega/2F_s)} \quad , \omega = n\omega_s \pm \tilde{\omega} \quad (n=0,1,2,\ldots)$$

In the laboratory, such an amplitude spectral characteristic is measured using the experimental set-up illustrated in Fig.2.9. This consists of a synthesised signal generator which provides the continuous-time signals with frequency $\tilde{\omega}$, and of a synthesised spectrum analyser which is able to tune to each one of the components of the

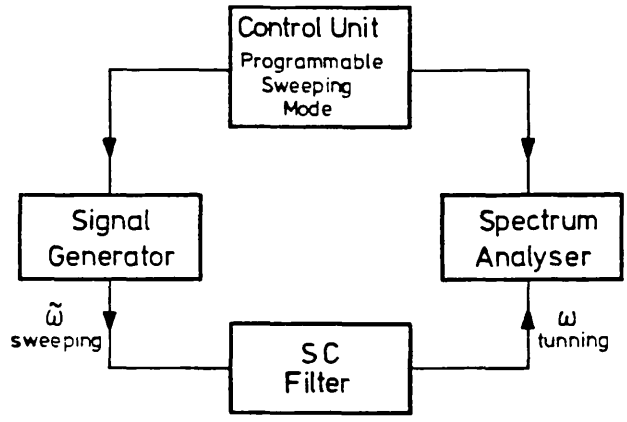


Fig.2.9: Experimental set-up for spectral measurements in SC filters

discrete-time spectrum, at frequency $\omega=\tilde{\omega}\pm n\omega_s$. The synthesised frequencies of both the signal generator and spectrum analyser are synchronised by means of a control unit in which we can program, for example, either one of the sweeping modes illustrated in Fig.2.10. In the light of the previous discussion of the sampling operation, such sweeping modes are interpreted as follows:

Alias sweeping mode (Fig.2.10-a): the discrete-time frequency components in the band $0<\omega<\omega_s/2$ are baseband components of $0<\tilde{\omega}<\omega_s/2$, but they are frequency-translated components of $\tilde{\omega}>\omega_s/2$.

Image sweeping mode (Fig.2.10-b): the continuous-time spectrum in the band $0<\tilde{\omega}<\omega_s/2$ produces baseband discrete-time frequency components in the band $0<\omega<\omega_s/2$ and frequency-translated components for $\omega>\omega_s/2$.

Baseband sweeping mode (Fig.2.10-c): the frequency components in both the continuous-time and the discrete-

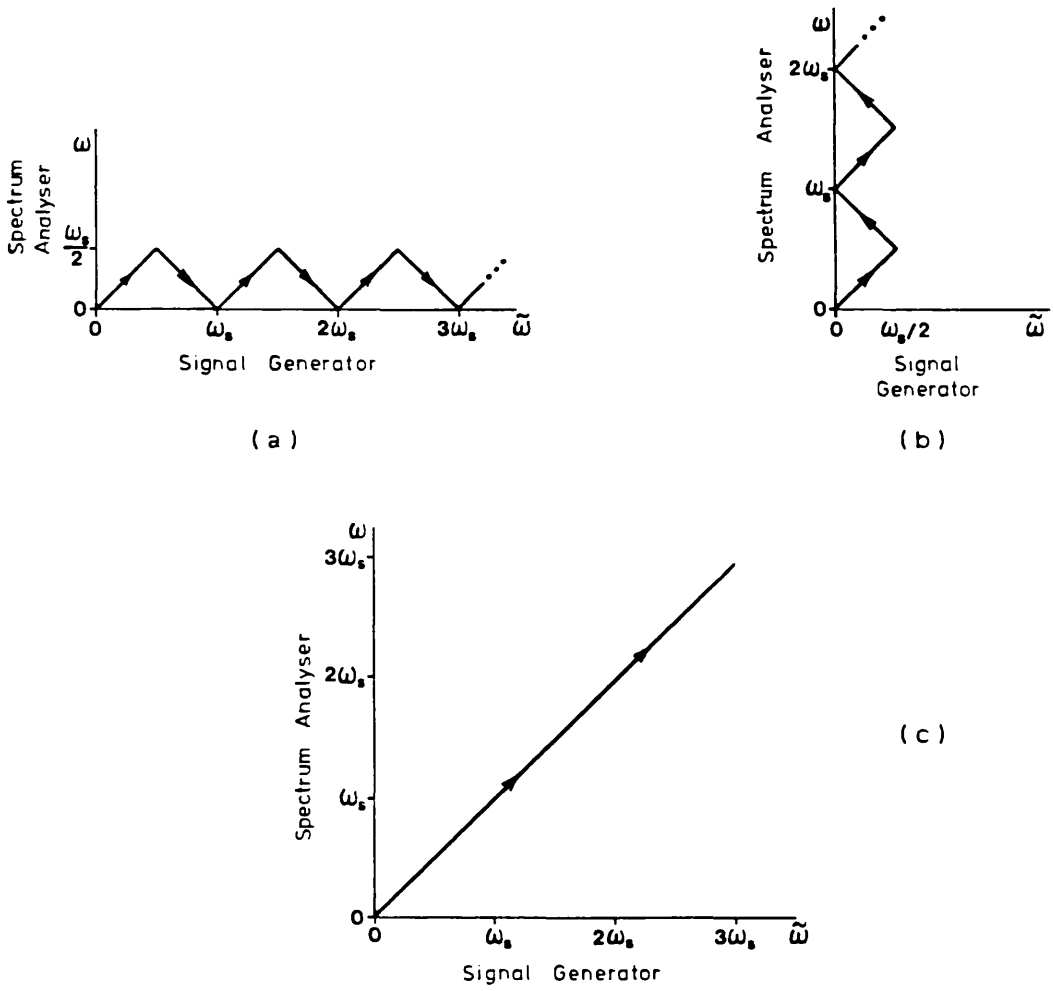
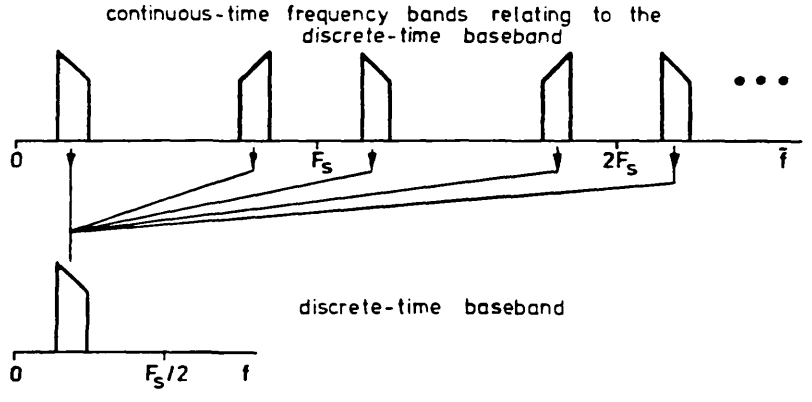


Fig.2.10: Programmable sweeping modes for spectral measurements in SC filters. (a) Aliasing measurement; (b) Imaging measurement; (c) Baseband measurement

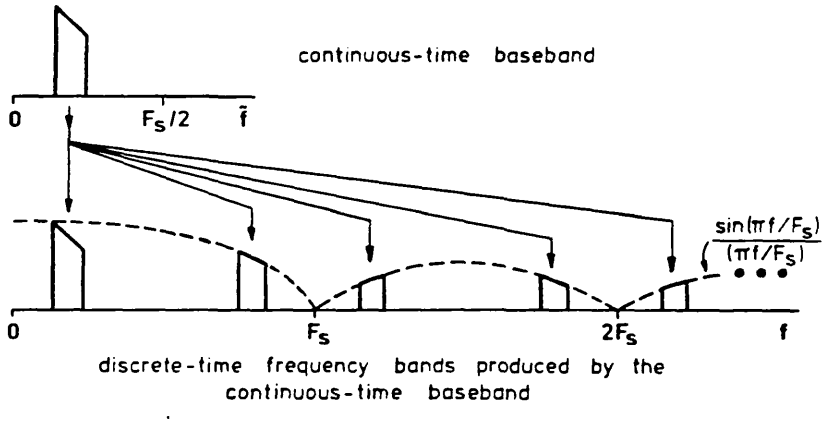
time spectra correspond to baseband components (in equation (2.5) we have always n=0).

For the sake of uniformity, we shall designate the frequency bands of the input and of the output spectra of an SC filter as follows: the frequency band below the Nyquist frequency $F_S/2$, either continuous-time or discrete-time, corresponds to the baseband of the SC filter, whereas the frequency bands above the Nyquist

frequency $F_S/2$ correspond to frequency-translated bands of the SC filter. Such designation leads to the representation of the alias and image responses of an SC bandpass filter, for example, as shown in Fig.2.11-a and in Fig.2.11-b, respectively. The alias sweeping mode of Fig.2.10-a yields the alias response illustrated in Fig.2.11-a, showing the continuous-time frequency-translated bands above $F_S/2$ that relate to the discrete-time baseband of the filter. The image sweeping mode of Fig.2.10-b yields the image response illustrated in Fig.2.11-b, showing the discrete-time



(a)



(b)

Fig.2.11: Illustration of the (a) alias and (b) image responses of an SC bandpass filter

frequency-translated bands above $F_s/2$ produced by the continuous-time baseband of the filter. The image response is multiplied by the sample and hold function $\sin(\pi f/F_s)/(\pi f/F_s)$. By combining the alias and the image responses in Fig.2.11 we obtain Fig.2.12, which represents symbolically the multiple input and output frequency bands that relate to the response of an SC bandpass filter in the baseband from DC to $F_s/2$.

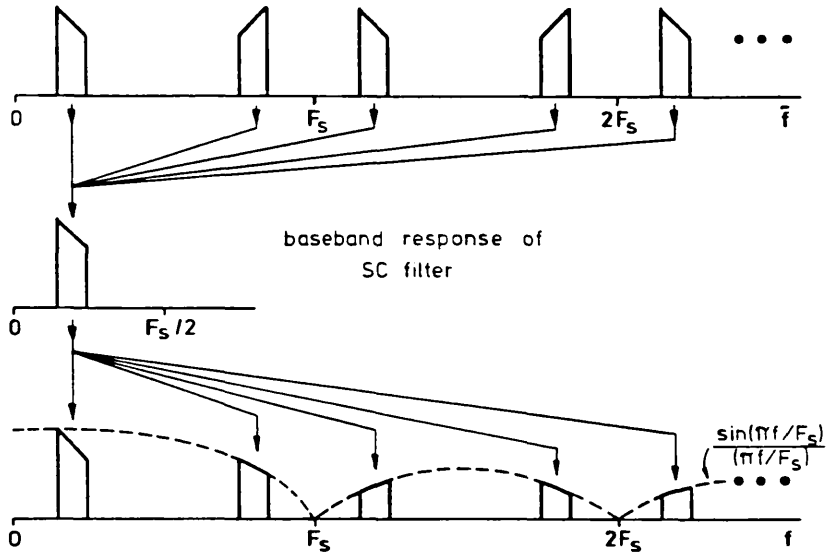


Fig.2.12: Symbolical representation of the multiple input and output frequency bands relating to the baseband response of an SC bandpass filter

2.3 FUNDAMENTAL ASPECTS OF SC FILTER SYSTEMS

2.3.1 Modes of operation

The purpose of embedding an SC filter in an SC filter system, as shown in Fig.2.13, is to achieve a single-path operation relating only one continuous-time frequency band with components at frequency $\tilde{f}$ to only one output discrete-time frequency band with components at frequency f. The Anti-Aliasing Filter (AAF) before the SC filter selects the desired continuous-time frequency band, while the Anti-Imaging Filter (AIF) after the SC filter selects the desired discrete-time frequency band. Depending on the

Fig.2.13: General architecture of an SC filter system

selected values of $\tilde{f}$ and f, such a correspondence may have any one of the forms illustrated in Fig.2.14, which define the system operating modes [2.5]. The <u>baseband filtering</u> mode illustrated in Fig.2.14-a, which corresponds to the selection of frequency components in the Nyquist band, i.e. $f=\tilde{f}<F_s/2$, has been the traditional mode of operation of SC filter systems. In this thesis we propose SC filter systems which operate in the following frequency-translated modes, corresponding to the selection of frequency-translated bands above the Nyquist frequency $F_s/2$:

<u>Upwards frequency translation</u> corresponds to $f>\tilde{f}$, and it

may take two forms: in direct frequency-translation (Fig.2.14-b) we have $f=\tilde{f}+nF_s$, whereas in frequency-translation with spectral inversion (Fig.2.14-c) we have $f=nF_s-\tilde{f}$.

Downwards frequency translation corresponds to $f<\tilde{f}$ and, as above, we may have either a direct frequency-translation (Fig.2.14-d) or a frequency-translation with spectral inversion (Fig.2.14-e).

Frequency-translated filtering corresponds to $f=\tilde{f}>F_s/2$, which can imply either a direct frequency-translation (Fig.2.14-f) or a frequency-translation with double spectral inversion (Fig.2.14-g).

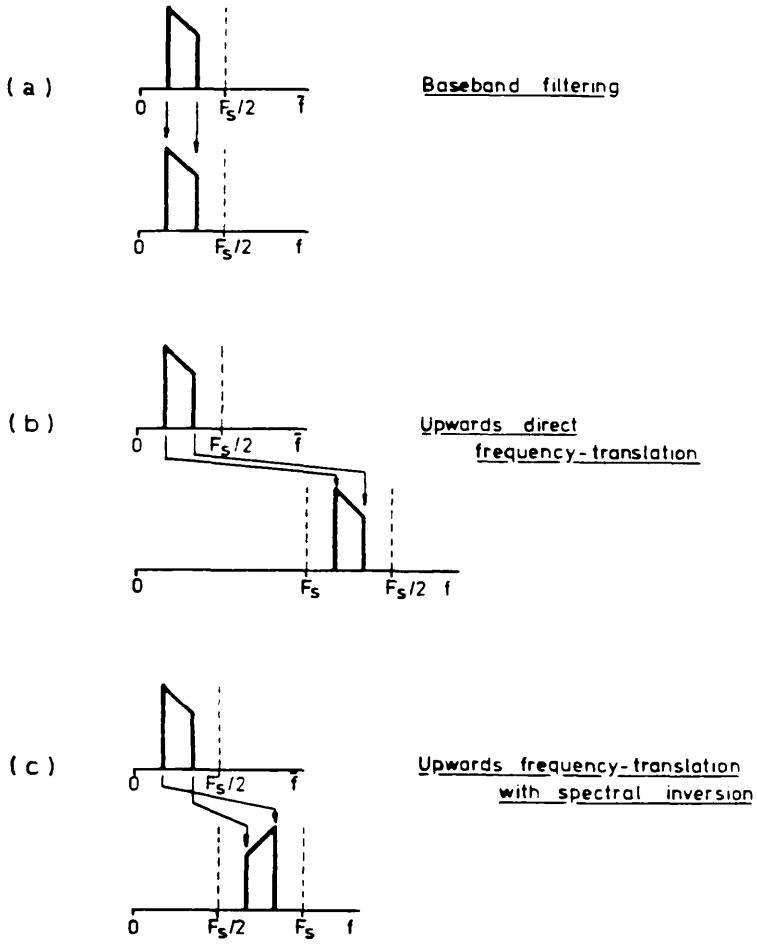
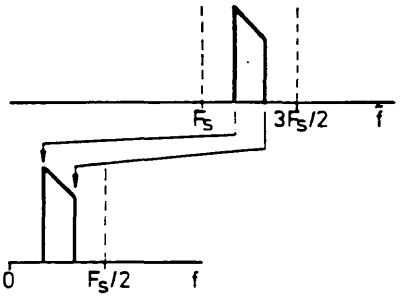


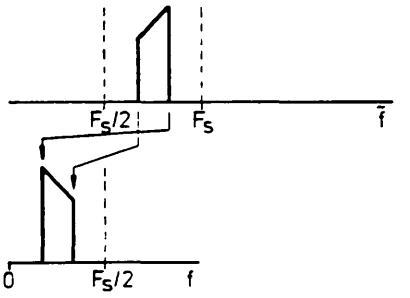
Fig.2.14: Illustration of the operating modes of an SC filter system with an SC bandpass filter

(d)



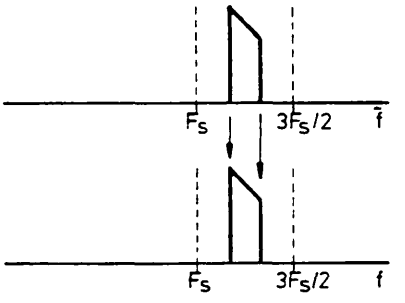
Downwards direct frequency-translation

(e)



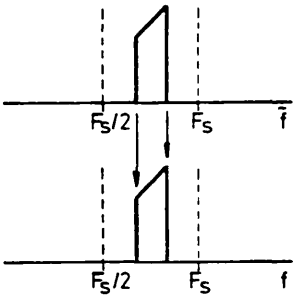
Downwards frequency-translation with spectral inversion

(f)



Direct frequency-translated filtering

(g)



Frequency-translated filtering with double spectral inversion

Fig.2.14: Operating modes of an SC filter system (continued)

SC filter systems based on frequency-translated modes, which we designate Single-Path Frequency-Translated (SPFT) systems, are particularly attractive for the realisation of bandpass responses with very narrow relative bandwidths. The design, implementation and evaluation of such SPFT SC filter systems, as well as of SC filter systems with baseband operating mode, will be considered in detail in Chapter 5. Here, we shall continue to look at some introductory aspects of SC filter systems, in particular the design of the AAF and of the AIF taking into account the technological constraints to bear in mind for the implemention of such filters.

2.3.2 Anti-Aliasing Filter

The characteristic of the AAF depends, first of all, on the operation mode of the system. A lowpass AAF is employed for applications which require the selection of the continuous-time baseband $f<F_s/2$, as in the baseband filtering mode. A bandpass AAF, on the other hand, is utilised for frequency-translated filtering applications requiring the selection of one continuous-time frequency-translated band above $F_s/2$. The second major factor which determines the characteristic of the AAF is the sampling ratio of the SC filter, $m=F_s/f_c$, where f_c is the upper band-edge frequency of the passband. In SC bandpass filters with narrow relative bandwidths, we usually define the sampling ratio in relation to the midband frequency f_o, i.e. $m=F_s/f_o$. The example given in Fig.2.15 shows how the selectivity of the AAF, in this case with lowpass response,

depends on the sampling ratio m of an SC bandpass filter.

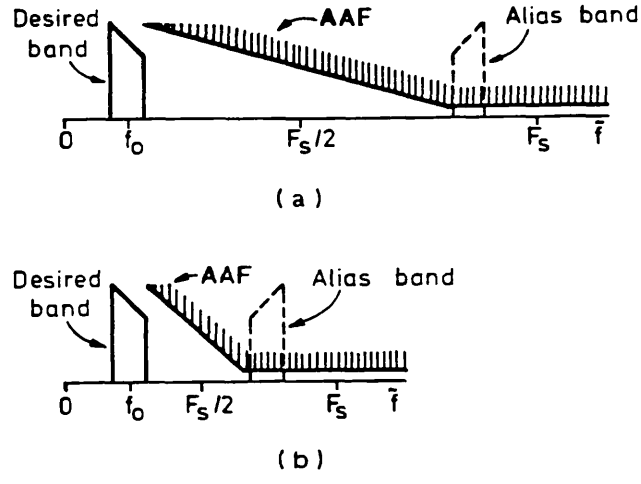


Fig.2.15: Selectivity of lowpass AAF as a function of the sampling ratio F_s/f_o. (a) High sampling ratio; (b) Low sampling ratio

When the sampling ratio is high, the AAF may have a wide transition band, as shown in Fig.2.15-a. Lower sampling ratios imply narrower transition bands, as illustrated in Fig.2.15-b.

2.3.3 Anti-Imaging Filter

The amplitude characteristic of the AIF depends on the selection of the desired image of the discrete-time output spectrum as well as on the sampling ratio of the SC filter, in a similar way as for the AAF. In addition, the design of the AIF is affected by the shaping of the image response by the function sinx/x. A lowpass AIF, for example, may be less selective than its AAF counterpart, because the function sinx/x increases the attenuation of the unwanted frequency-translated images above $F_s/2$ while introducing little attenuation on the desired baseband image below $F_s/2$

which, if necessary, can be easily compensated [2.6],[2.7]. On the other hand, the design of a bandpass AIF for selecting one frequency-translated image above $F_s/2$ is usually more complicated than the design of an equivalent AAF, because the required compensation for the function sinx/x increases for higher frequency selected images.

2.3.4 Technological constraints of continuous-time AAF and AIF

The AAF and the AIF realised as continuous-time filters in the conventional active-RC form utilise polysilicon resistors, and MOS capacitors [2.8],[2.9]. Typically, the nominal resistance value of a polysilicon resistor has a tolerance between ±25% and ±50%, depending on the process of fabrication. The accuracy of the absolute capacitance value of an MOS capacitor is between ±10% and ±20% [2.9]. Assuming that such variations are uncorrelated, the nominal value of an RC time constant can vary as much ±70%, and, consequently, the accuracy of the amplitude response of an active-RC will be rather poor. Moreover, time constants in the audio frequency range (e.g. $RC\simeq 10^{-5}$ seconds) require very large resistance values of the order of $10^5\Omega$ and also large capacitance values of the order of 10^{-10}F. The implementation of such time constants requires a large area of silicon, which can be as much as 10-20 times the area which is required to implement the largest capacitance ratio typically allowed in an SC filter [2.10], [2.9]. Besides, monolithic resistors and capacitors are voltage and temperature dependent thereby introducing

sources of signal distortion in SC filter systems [2.9].

In view of the above technological constraints, on-chip continuous-time active-RC filters of the AAF and of the AIF are required to have (i) lowpass response with maximum 3rd. order to reduce circuit complexity and (ii) high nominal passband cut-off frequency, not only to reduce the time constants, but also to allow high variability of the nominal amplitude response. Therefore, such continuous-time filters can be employed for attenuating only those frequency-translated components whose frequencies are much higher than the maximum frequency of interest of the SC filter system, typically a ratio of 15 or even more. In the case of an SC bandpass filter system, for example, this implies an SC bandpass filter with high sampling ratio $F_s/f_o \geq 16$. An SC bandpass filter operating with a lower sampling ratio $F_s/f_o < 16$, which may be required for capacitance ratio reduction, for example, generates unwanted frequency-translated components at lower frequencies which the AAF and AIF with continuous-time filters can not attenuate adequately. This gives rise to undesirable effects of aliasing and imaging in the system. In order to overcome such problem, we have to increase the selectivity of the AAF and AIF by means of specialised SC circuits, respectively called SC decimators and SC interpolators, whose fundamental filtering aspects will be examined in the next Section.

2.4 AAF AND AIF WITH INCREASED SELECTIVITY

2.4.1 AAF with SC decimator

The general architecture of an AAF is shown in Fig.2.16. After the input continuous-time filter, we have an SC decimator with input sampling rate MF_s (M is an integer >1) and whose output signal is sampled at lower rate F_s by the following SC filter. Reduction of the

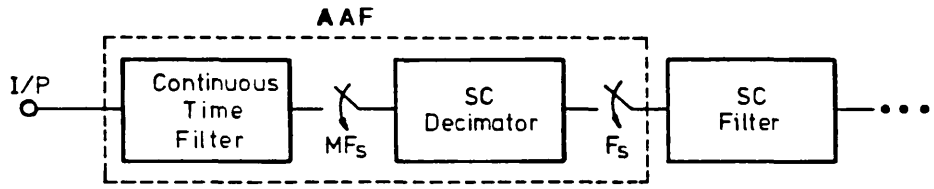


Fig.2.16: AAF with SC decimator

sampling rate from a high value MF_s to a lower value F_s is called decimation by a factor M [2.11]. In the frequency domain, the characteristic of the SC decimator is important because it should attenuate those unwanted alias frequency-translated components associated with the signal at lower sampling rate F_s which have not been sufficiently attenuated by the input continuous-time filter. This is illustrated by means of the simple example in Fig.2.17, for an SC decimator with M=2. Fig.2.17-a shows the alias response of an SC lowpass filter with upper band-edge frequency f_c, and switching frequency F_s, in which we want to select the baseband below the Nyquist frequency $F_s/2$. A low selectivity continuous-time filter attenuates the

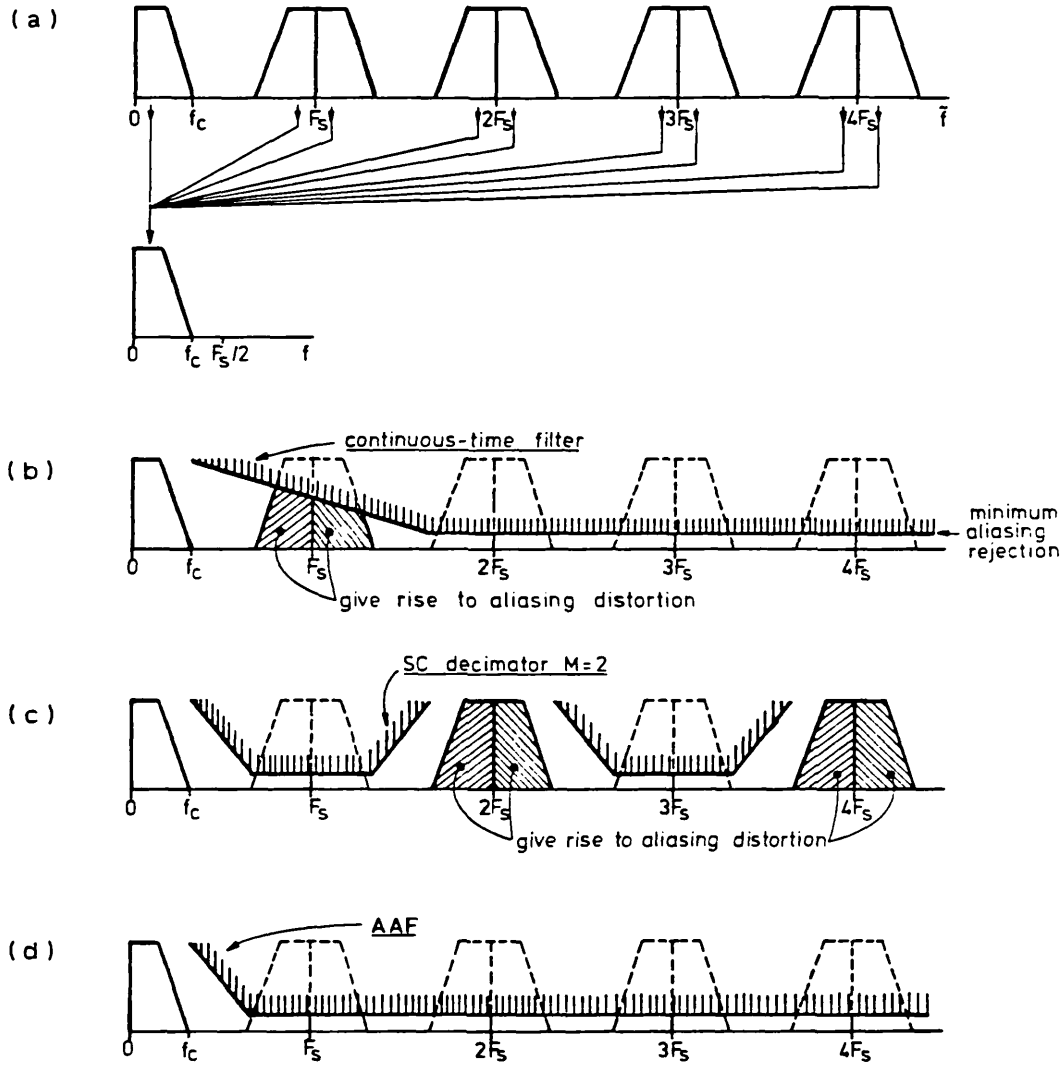


Fig.2.17: Illustration of the anti-aliasing characteristic of an AAF with combined low-selectivity continuous-time filter and SC decimator

unwanted alias frequency-translated components above $2F_s-f_c$, as shown in Fig.2.17-b. In order to attenuate the unwanted alias frequency-translated components around F_s, which would give rise to aliasing distortion, we introduce an SC decimator M=2 with the periodic characteristic shown in Fig.2.17-c. The combination of the continuous-time

filter, on the one hand, together with the SC decimator, on the other hand, provides the required anti-aliasing characteristic of the AAF illustrated in Fig.2.17-d.

2.4.2 AIF with SC interpolator

The general architecture of an AIF is represented in Fig.2.18. After the SC filter operating at low sampling rate Fs, we have an SC interpolator with output sampling rate LF_s (L is an integer >1), which is followed by the output continuous-time filter. Increase of the sampling

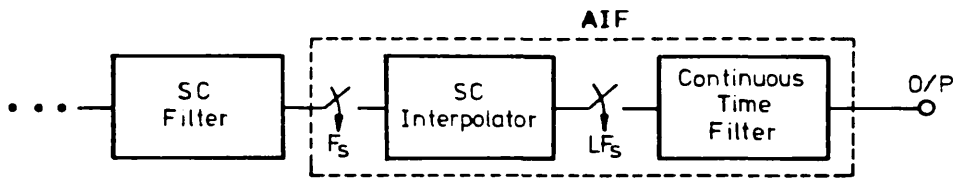


Fig.2.18: AIF with SC interpolator

rate from a low value F_s to a higher value LF_s is called interpolation by a factor L [2.11]. The characteristic of the SC interpolator in the frequency-domain is also important because it should attenuate those unwanted frequency-translated components produced by the SC filter at low sampling rate F_s which will not be sufficiently attenuated by the output continuous-time filter. This is illustrated in the simple example given in Fig.2.19 for an SC interpolator with L=2. In Fig.2.19-a we have the image response of the SC filter which is partly tailored by the sample and hold function corresponding to the low sampling

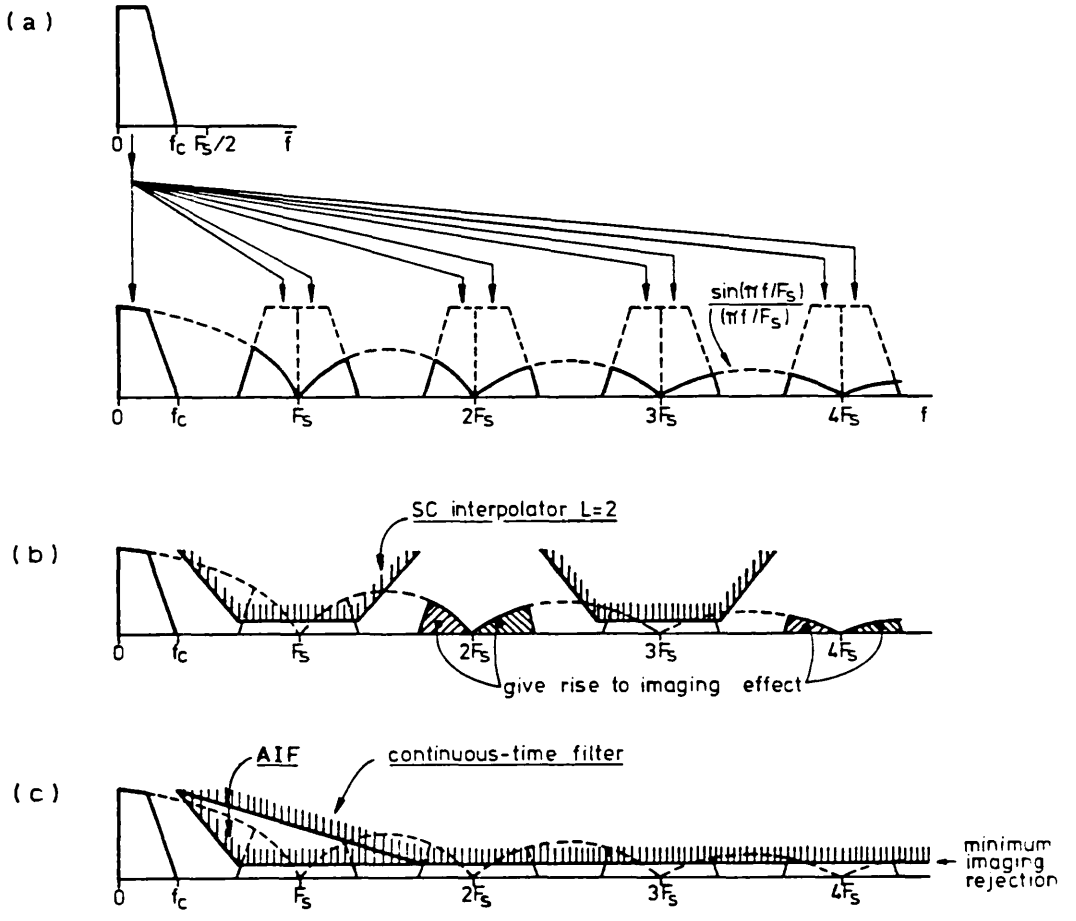


Fig.2.19: Illustration of the anti-imaging characteristic of an AIF with combined low-selectivity continuous-time filter and SC interpolator

rate F_s. The SC interpolator L=2 is designed to attenuate the unwanted image frequency-translated components around F_s, as shown in Fig.2.19-b. The remaining unwanted image frequency-translated components around $2F_s$, and above, will then be attenuated by the output continuous-time filter with low selectivity yielding the overall anti-imaging characteristic of the AIF illustrated in fig.2.19-c.

2.4.3 Filtering characteristics of SC decimators and interpolators

Decimation and interpolation are regarded as linear filtering processes in which appropriate frequency responses of the decimators and interpolators, either with FIR or IIR transfer functions, reject unwanted alias and image frequency-translated components [2.4],[2.12],[2.13]. In SC bandpass filter systems, the derivation of such frequency responses for SC decimators and interpolators must take into account the following system aspects [2.5],[2.14]:

1. System operating mode (e.g. baseband, frequency-translated).
2. Sampling ratio of the SC bandpass filter.
3. Required factors M and L of sampling rate alteration to allow low selectivity continuous-time filters in the system.
4. Required level of attenuation of unwanted frequency-translated components in the system.

Some of these aspects are illustrated in Fig.2.20, referring to the process of decimation. The examples given in Fig.2.20-a, Fig.2.20-b and Fig.2.20-c correspond to SC bandpass filter systems operating in a baseband filtering mode, in which the SC bandpass filter has different sampling ratios. A high sampling ratio, say m>10, permits an SC decimator with low factor of sampling rate reduction, e.g. M=2, and it suffices to have an FIR single notch approximation with notch frequency at F_s, as shown in Fig.2.20-a [2.15]-[2.18]. A lower sampling ratio of the SC

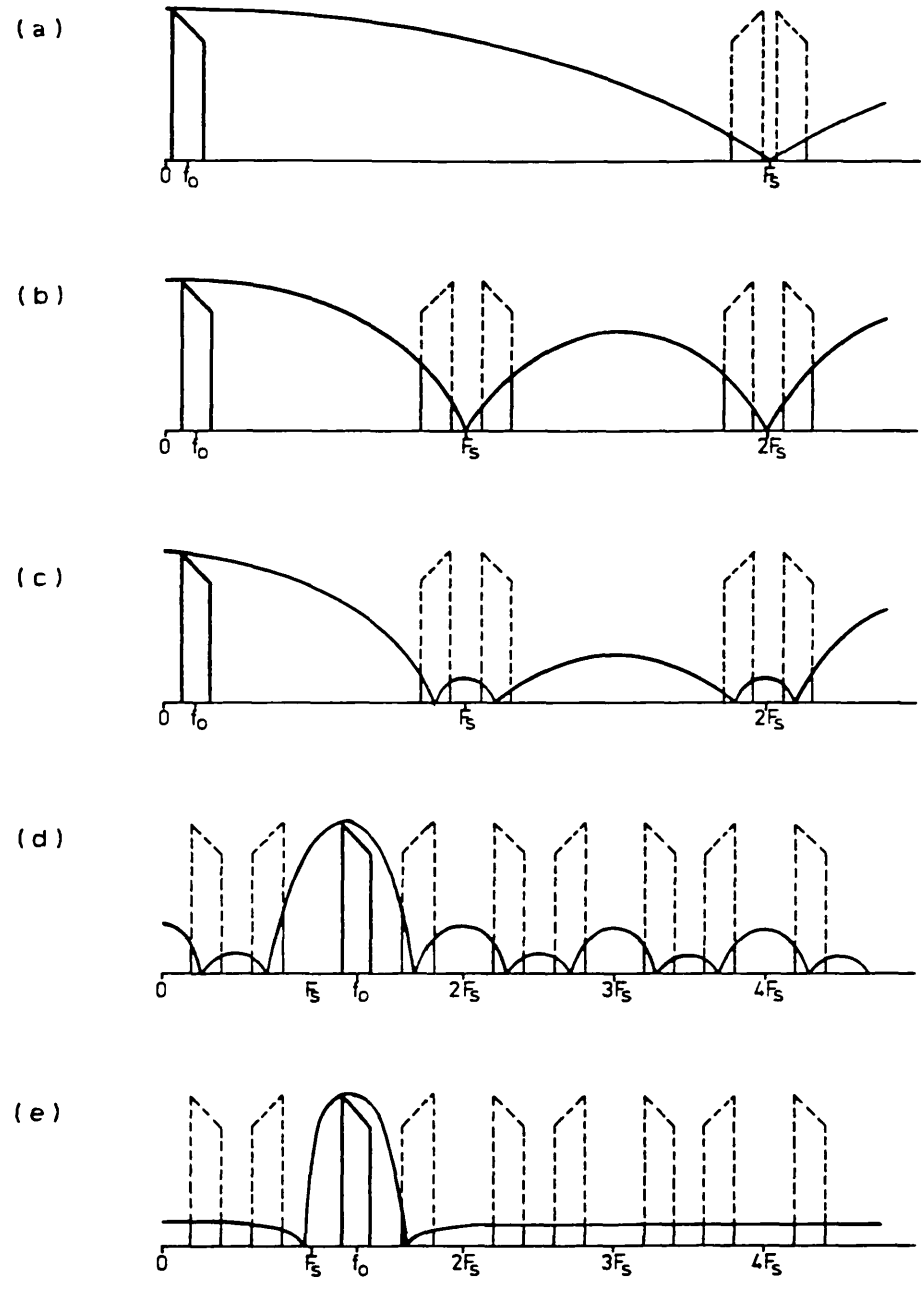


Fig.2.20: Filtering characteristics of SC decimators as a function of the sampling ratio F_s/f_o and system operating mode. (a) FIR lowpass decimator with M=2 and single notch at F_s; (b) FIR lowpass decimator with M=4 and single notches at F_s and and $2F_s$; (c) FIR lowpass decimator with M=4 and optimum notch placement around F_s and $2F_s$; (d) FIR bandpass decimator with M=8 and optimum multinotch placement; (e) IIR bandpass decimator with M=8 and wideband stopband approximation

bandpass filter requires a higher factor, M>2, of sampling rate reduction of the SC decimator in order to allow a continuous-time filter in the system with similar characteristics. However, even an SC decimator with M=4, but with single notches at F_s and $2F_s$, does not provide the required rejection of the unwanted alias frequency-translated components, as indicated in Fig.2.20-b. Instead, we employ the optimised FIR multinotch stopband approximation shown in Fig.2.20-c whereby the notch frequencies are shifted exactly to the centre of the alias frequency-translated bands to be attenuated. By reducing even further the sampling ratio of the SC bandpass filter, such that m<1, we have a frequency-translated operating mode illustrated in the examples of Fig.2.20-d and Fig.2.20-e, in which the SC decimator is required to have even higher factors M of sampling rate reduction. Although an optimised FIR multinotch stopband approximation may still be employed, as shown in fig.2.20-d, it may be more efficient to employ the IIR wideband stopband approximation illustrated in Fig.2.20-e. The adoption of either one of such amplitude/frequency approximations, e.g. FIR multinotch stopband or IIR wideband stopband, implies further considerations concerning the SC decimator (and interpolator) circuits available for implementation. We shall describe these aspects in Chapter 3 and in Chapter 4.

2.5 OPTIMUM FIR TRANSFER FUNCTIONS FOR DECIMATION AND INTERPOLATION

IIR wideband stopband approximations can be obtained without too much difficulty, for example employing any one of the many procedures available for the design of SC filters in general [2.19],[2.20]. On the other hand, the derivation of FIR multinotch stopband approximations using known techniques is more time consuming, and usually requires the use of numerical tools for optimisation (e.g. [2.21],[2.22]). In this Section we consider a very simple technique for optimisation of FIR transfer functions for decimation and for interpolation, which produce notch frequencies exactly at the centre of the alias and image frequency-translated bands to be attenuated.

The problem of exact placement of the notch frequencies of the frequency responses for decimation and for interpolation is solved directly in the discrete-time frequency domain in order to avoid warping effects inherent to the transformations from the continuous-time domain. For this purpose, let us consider a narrowband SC bandpass filter with midband frequency f_o and switching frequency F_s which is symbolically represented on the unit circle by a complex conjugate pole-pair with $r_p=1$ and argument $\theta_p=2\pi f_o/F_s$ and $\theta_p^*=2\pi(F_s-f_o)/F_s$, respectively on the upper half-circle corresponding to the baseband from DC to $F_s/2$ and on the lower half-circle corresponding to the frequency-translated band from $F_s/2$ to F_s, as shown in Fig.2.21-a. The periodic characteristic of such an SC

bandpass filter in the frequency band from DC to $2F_s$, for example, is shown in Fig.2.21-b. A sampling rate alteration

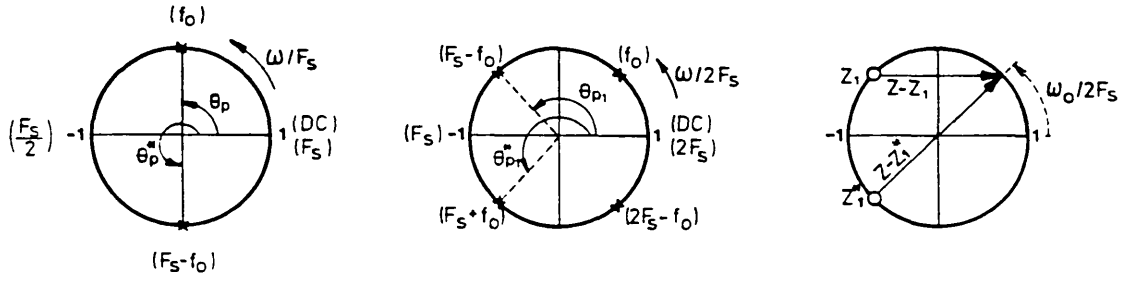


Fig.2.21: Representation of a complex conjugate pole-pair (a) on the unit circle from DC to F_s, and, (b) on the unit circle from DC to $2F_s$; (c) Complex conjugate zero-pair giving an optimum placement of notch frequencies around F_s, for factors M=2 and L=2 of sampling rate alteration

factor M=2 or L=2 implies elimination of the unwanted frequency-translated components, respectively alias and image, which correspond to the pole arguments $\theta_{p1}=2\pi(F_s-f_o)/2F_s$ and $\theta^*_{p1}=2\pi(F_s+f_o)/2F_s$. This can be achieved by means of an FIR transfer function which corresponds to the complex conjugate zero-pair illustrated in Fig.2.21-c and which is expressed as

$$(2.12)\ \ldots \qquad H(Z) = \sum_{i=o}^{2} h_i Z^{-i}$$

where the unit delay period is $1/2F_s$. In order to obtain the design equations for optimisation of the coefficients h_0, h_1 and h_2, we consider first the product

$$(2.13\text{-a})\ \ldots \quad (Z-Z_1).(Z-Z_1^*) = K\left[\left(Z-e^{j\pi(F_s-f_o)/F_s}\right).\left(Z-e^{-j\pi(F_s-f_o)/F_s}\right)\right]$$

yielding

$$(2.13\text{-b}) \quad \ldots \qquad (Z-Z_1).(Z-Z_1^*) = Z^2.K.\left\{1-2\cos\left[\pi(F_S-f_o)/F_S\right].Z^{-1}+Z^{-2}\right\}$$

where K is an arbitrary gain constant. By simple geometric considerations illustrated in Fig.2.21-c, the modulus of (2.13-b) at midband frequency f_o is given by

$$(2.13\text{-c}) \quad \ldots \qquad \left[\,|Z-Z_1|.|Z-Z_1^*|\,\right]_{Z=e^{j2\pi f_o/2F_s}} = K.4.\cos(\pi f_o/F_s)$$

Hence, from (2.13-a) and (2.13-b), and for K=1 at midband frequency f_o, we obtain the design equations given in Table 2.1 for the optimum coefficients h_0, h_1, and h_2.

$H(Z) = \sum_{i=o}^{2} h_i Z^{-i}$
$h_o=h_3= \left[4\cos(\pi f_o/F_s)\right]^{-1}$ $h_2= -\dfrac{\cos\left[\pi(F_S-f_o)/F_S\right]}{2\cos(\pi f_o/F_s)}$
Unity gain @ f_o

Table 2.1: Design equations for optimum FIR transfer functions for factors M=2 and L=2 of sampling rate alteration

Another often used factor of sampling rate alteration is M=L=3, which implies elimination of the unwanted frequency-translated components up to $3F_s-f_o$, as illustrated in Fig.2.22-a. The zero-pattern shown in

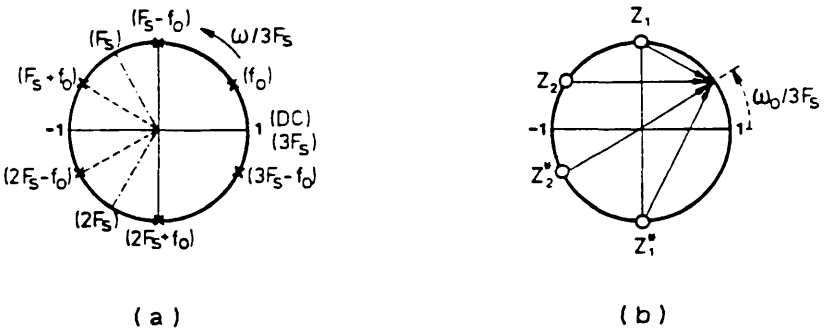


Fig.2.22: (a) Representation of the complex conjugate pole-pair in Fig.2.21-a on the unit circle from DC to $3F_s$; (b) Complex conjugate zero-pairs giving an optimum placement of notch frequencies around F_s and $2F_s$, for factors M=3 and L=3 of sampling rate alteration

Fig.2.22-b leads to an FIR transfer function of the form

$$(2.14)\ \ldots \qquad H(Z) = \sum_{i=o}^{4} h_i Z^{-i}$$

where the unit delay period is $1/3F_s$. The design equations for the optimised FIR coefficients are summarised in Table 2.2.

Optimum FIR transfer functions for higher factors of sampling rate alteration can also be derived using the above procedure, for subsequent implementation using a single stage SC decimator or interpolator circuit. Alternatively, we can employ the elementary transfer functions for M=L=2 or M=L=3 in order to implement SC

$H(Z) = \sum_{i=o}^{4} h_i Z^{-i}$
$h_o = h_4 = \gamma/16$ $h_1 = h_3 = (1-\alpha^2-\beta^2)\cdot\gamma/4$ $h_2 = (3-4\alpha^2-4\beta^2-8\alpha^2\beta^2)\cdot\gamma/8$
$\alpha = \cos[\pi(F_s-f_o)/3F_s]$ $\beta = \cos[\pi(2F_s-f_o)/3F_s]$ $\gamma = \left\{\left[\cos^2\left(\frac{\pi f_o}{3F_s}\right)-\alpha^2\right]\cdot\left[\cos^2\left(\frac{\pi f_o}{3F_s}\right)-\beta^2\right]\right\}^{-1}$
Unity gain @ f_o

Table 2.2: Design equations for optimum FIR transfer functions for factors M=3 and L=3 of sampling rate alteration

decimators and interpolators with cascade structures. Examples of both of these approaches will be given in Chapter 4 and in Chapter 5.

2.6 SUMMARY

We started this Chapter by examining the aspects of aliasing and imaging in SC filters, consisting of a multiplicity of input and output frequency-translated bands above the Nyquist frequency of the SC filter, which relate to the baseband response below the Nyquist frequency.

Based on the manipulation of those spectral characteristics, we discussed various operating modes for SC filter systems which depend on the selection of appropriate input and output frequency bands, either baseband or frequency-translated. Hitherto, SC filter systems have operated in the conventional baseband filtering mode, corresponding to the selection of the frequency band below the Nyquist frequency. In this Chapter, we introduced novel SC system operating modes, corresponding to the selection of specified input and output frequency-translated bands above the Nyquist frequency, which are particularly important for bandpass filtering applications with very narrow relative bandwidths. We then described the general architecture for implementation of SC filter systems, with baseband and frequency-translated operating modes, which are required to have appropriate AAF and AIF with lowpass and bandpass responses, respectively. In general, the AAF and AIF consist of a combination of low-selectivity low-precision continuous-time filters for attenuating unwanted signal components at high frequency, together with efficient SC decimator and interpolator circuits for attenuating unwanted signal components with frequency close to the passband of the system. SC decimators and interpolators can have IIR or FIR transfer functions, or even a combination of both, which have to be derived bearing in mind the operating mode of the system, the sampling ratio of the SC filter and the anti-aliasing and anti-imaging specifications. For FIR transfer functions we introduced a

simple optimisation technique, which allows us to place the notch frequencies in such a way that the attenuation of the unwanted alias or image components is maximised.

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CHAPTER 3

SIGNAL FLOW GRAPH GENERATION OF SC BIQUADS AND DESIGN OPTIMISATION FOR MINIMUM CAPACITANCE SPREAD

3.1 INTRODUCTION

SC biquadratic sections (biquads) are utilised in various parts of the SC bandpass filter systems that we shall describe in Chapter 5. Cascade SC biquad structures with moderate sensitivity are employed for SC decimators and interpolators, whereas for high-quality SC bandpass filters we employ instead SC coupled-biquad structures based on the simulation of low sensitivity LCR ladder prototype filters. The purpose of this Chapter is to develop SC biquad building blocks which are suitable for such applications, and to study their properties, particularly with respect to the problem of large capacitance ratios which arise in filters with high selectivity.

In order to deal with the synthesis and analysis of SC biquads we need versatile tools that are simple to use and give a good interpretation of the operation of the circuits. The SC equivalent circuits established by Laker [3.1] are not entirely satisfactory, mainly because they lead to complicated networks that are difficult to manipulate and to analyse. Signal Flow Graph (SFG) techniques provide a much simpler means of representing SC circuits, both for synthesis and for analysis [3.2]-[3.5]. The approach by Moschytz and Brugger [3.4],[3.5], although being generally applicable to the analysis of any type of SC circuit, does not provide the desirable physical interpretation of SC circuits that is achieved using the SFG's proposed by Haigh and Singh [3.2] and which we

generalise in Section 3.2. Such SFG's are then employed, in Section 3.3, to develop parasitic-insensitive SC biquad building blocks based on a Two Integrator Loop (TIL) structure. In Section 3.4, we present a full set of design equations for SC biquads whose discrete-time transfer functions are derived from continuous-time transfer functions using the bilinear transformation. It is shown that the resulting SC biquads have low sensitivity of the frequency and quality-factor (Q-factor) of the complex conjugate pole-pair with respect to changes of the nominal capacitance values.

As we saw in Chapter 1, the capacitance ratio requirements for the design of highly selective SC filters become unacceptably large, both from the point of view of their accuracies, and from the point of view of the silicon area required for implementation. The techniques currently available for reduction of capacitance ratios are not fully satisfactory, either because they render the frequency response of the SC filters rather sensitive to capacitance ratio errors [3.6], or because they destroy the parasitic insensitive property of the circuits thus increasing the effective capacitance ratio errors [3.7],[3.8]. In the second part of this Chapter, which comprises Sections 3.5, 3.6, and 3.7, we present a novel analysis of capacitance ratios in SC biquads, which leads to the proposal of an optimum value of the switching frequency yielding absolute minimum capacitance spread. Section 3.5 introduces the basic definitions and scaling operations that can be

applied to the capacitors of the SC biquad building blocks, and compares, from the viewpoint of capacitance spread, SC biquads using different types of damping. The strategy for capacitance spread analysis is described in Section 3.6 with respect to an SC bandpass biquad. We introduce the concept of optimum switching frequency yielding absolute minimum capacitance spread which, as we show, trades-off with respect to the maximum signal handling capability of the SC biquad. Further aspects of the design of SC biquads, concerning not only capacitance spread but also total capacitor area, and also the choice of the switching frequency, are illustrated by means of the examples given in Section 3.7. In Section 3.8 we present a summary of this Chapter.

3.2 DERIVATION OF GENERAL SFG'S FOR SC INTEGRATORS

3.2.1 Single-phase SC integrators

The parasitic-insensitive SC integrator shown in Fig.3.1-a, with switch timing, is represented by the SFG given in Fig.3.1-b [3.2]. By recalling the aspects of time-domain analysis of SC circuits given in Chapter 1, the above SFG is interpreted as follows. The branch with transmission factor $1/(1-Z^{-1})$ represents the periodic discrete-time integration of the SC integrator. The branches with transmission factors $-K_1$ and $K_1.Z^{-1/2}$ convey information of two kinds. The powers of Z, 0 and -1/2, describe instants of input voltage sampling at the end of the sampling phases, i.e. 0 and $T_s/2$; the coefficients $-K_1$

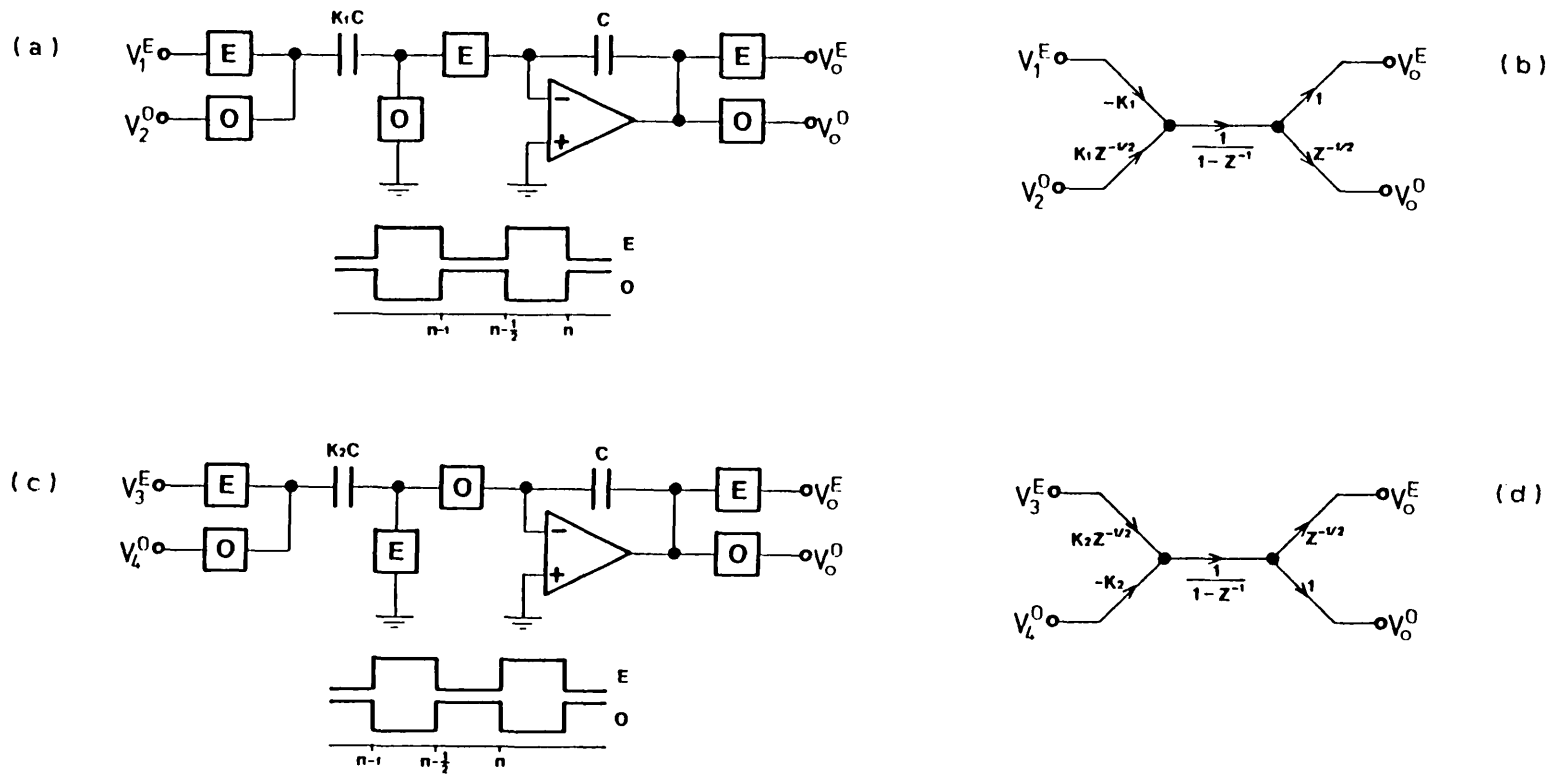
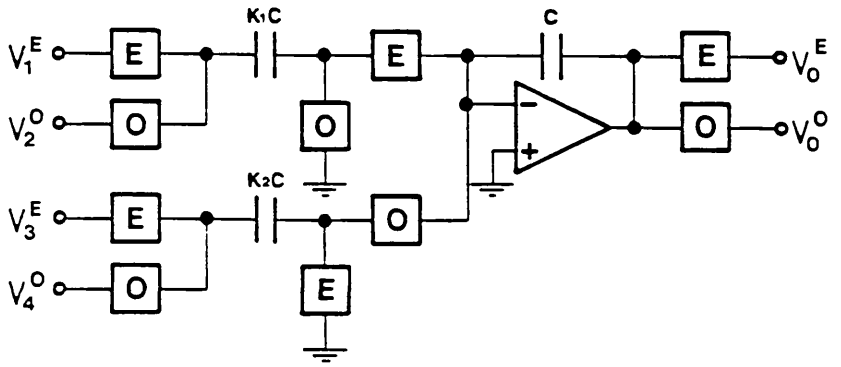


Fig.3.1: Illustration of single-phase SC integrators.
(a) E-integrator, and (b) corresponding SFG
(c) O-integrator, and (d) corresponding SFG

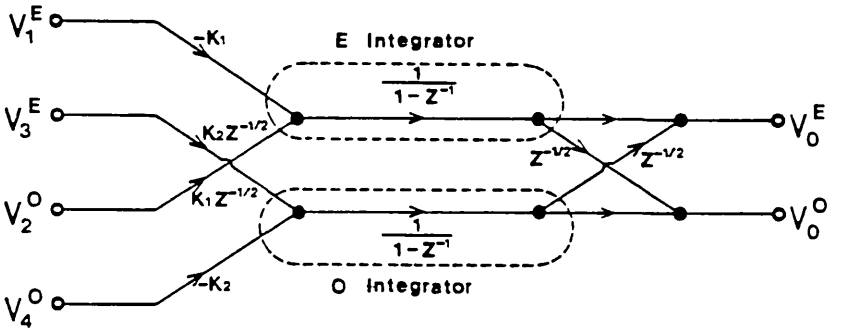
and $+K_1$ indicate the increment of the amplifier output voltage, relative to the input voltage, produced by each one of the input SC branches every switching period. The branches with transmission factors 1 ($=z^0$) and $z^{-1/2}$ give information of the output sampling instants. The output voltage of this SC integrator changes in the E phase because the switch connected to the input of the OA is controlled by the E phase switching waveform. Therefore, this integrator will be referred to as an E-integrator. Interchange of switch phasing leads to the O-integrator shown in Fig.3.1-c, where the output voltage changes in the O phase. The switch timing for this SC integrator is also shown in Fig.3.1-c, and the corresponding SFG is given in Fig.3.1-d. The SC integrators of Fig.3.1-a and Fig.3.1-c change the output voltage only once in each switching period and therefore they will be referred to as single-phase integrators. In these integrators, the output voltages sampled in the E phase and in the O phase have the same magnitude but are delayed by half a switching period.

3.2.2 Double-phase SC integrators

In the development of the SC biquad building blocks we require also the more general SC integrator shown in Fig.3.2-a. The output voltage of this integrator changes twice in each switching period, i.e. in the E phase and in the O phase, because of the two switches that are connected to the virtual ground of the OA. This SC integrator will be referred to as a double-phase integrator. The output voltage of the double-phase integrator sampled in each



(a)



(b)

Fig.3.2: (a) Double phase integrator, and (b) SFG

phase, i.e. V_o^E or V_o^O, is the sum of the output voltages of an E-integrator and of an O-integrator sampled in the same phase. This is represented by the SFG of Fig.3.2-b. The two extra branches at the output represent the delay of half a switching period that exists between the reference switch timings of the E-integrator and of the O-integrator (see Fig.3.1-a and Fig.3.1-c). The voltages V_o^E and V_o^O in the SFG of Fig.3.2-b have different magnitudes and therefore they are not related simply by a delay factor, as in the case of the SFG's of single-phase integrators. In order to obtain an SFG in which we represent the relationship between these two voltages, directly, we adopt a procedure which is described using the example of

Fig.3.3. Firstly, in the original SFG of Fig.3.3-a we choose the output voltage of an E-integrator sampled in the E phase, i.e. V_o^E, as the output voltage reference. Secondly, we modify the transmission factors of the input branches according to the phase of the output voltage reference. In Fig.3.3-b, this corresponds to the additional delay $z^{-1/2}$ for both the transmission factors $-K_2$ and $K_2.z^{-1/2}$, where both z^0 and $z^{-1/2}$ refer to the O phase. Finally, we express the output voltage sampled in the complementary phase, i.e. V_o^O in this example with V_o^E reference, as a linear combination of the output voltage reference and also of the input voltages, as shown in Fig.3.3-c. The extra branches with transmission factors $-K_2.z^{-3/2}$ and $K_2.z^{-1}$ cancel the terms $K_2.z^{-3/2}.V_3^E$ and $-K_2.z^{-1}.V_4^O$ fed to the output V_o^O via the output reference V_o^E. The SFG in Fig.3.3-c reduces to the simpler form given in Fig.3.3-d. By adopting a similar procedure we can also derive the SFG's corresponding to the remaining three possible output voltage references, namely V_o^O of the E-integrator, and both V_o^E and V_o^O of an O-integrator. The simplest forms of such SFG's are shown in Fig.3.4, together with the SFG derived in Fig.3.3-d.

The interconnection of SC integrators in order to realise SC biquads will be carried-out according to the following rules:

Rule 1: The output of a single-phase SC integrator can be sampled in both the E phase and the O phase.

Rule 2: The output of a double-phase SC integrator is

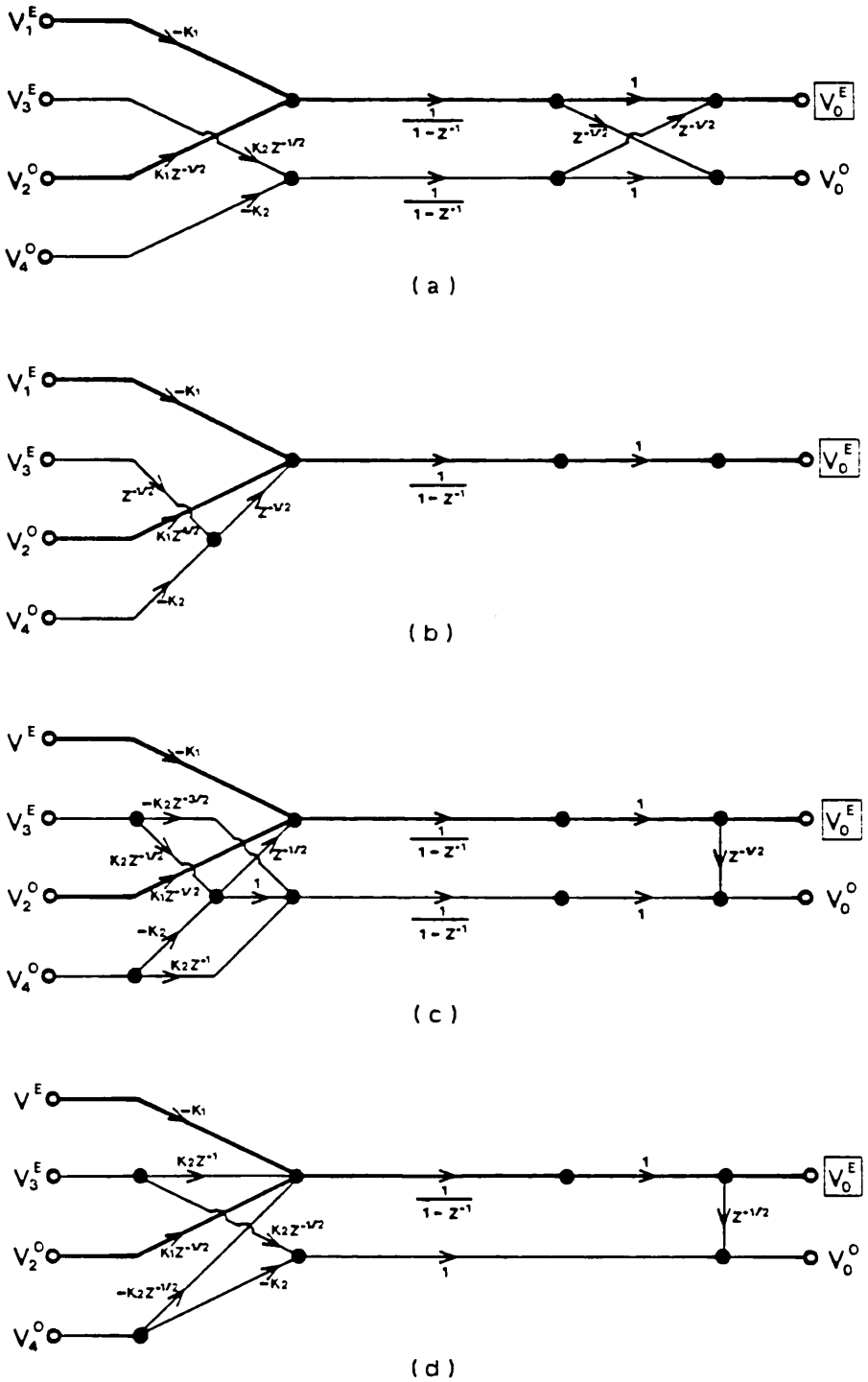


Fig.3.3: Illustrating the SFG derivation of a double-phase integrator. (a) Original SFG; (b) Referring the input branches to the output voltage reference V_o^E; (c) Obtaining the complementary output voltage V_o^O; (d) SFG in simple form

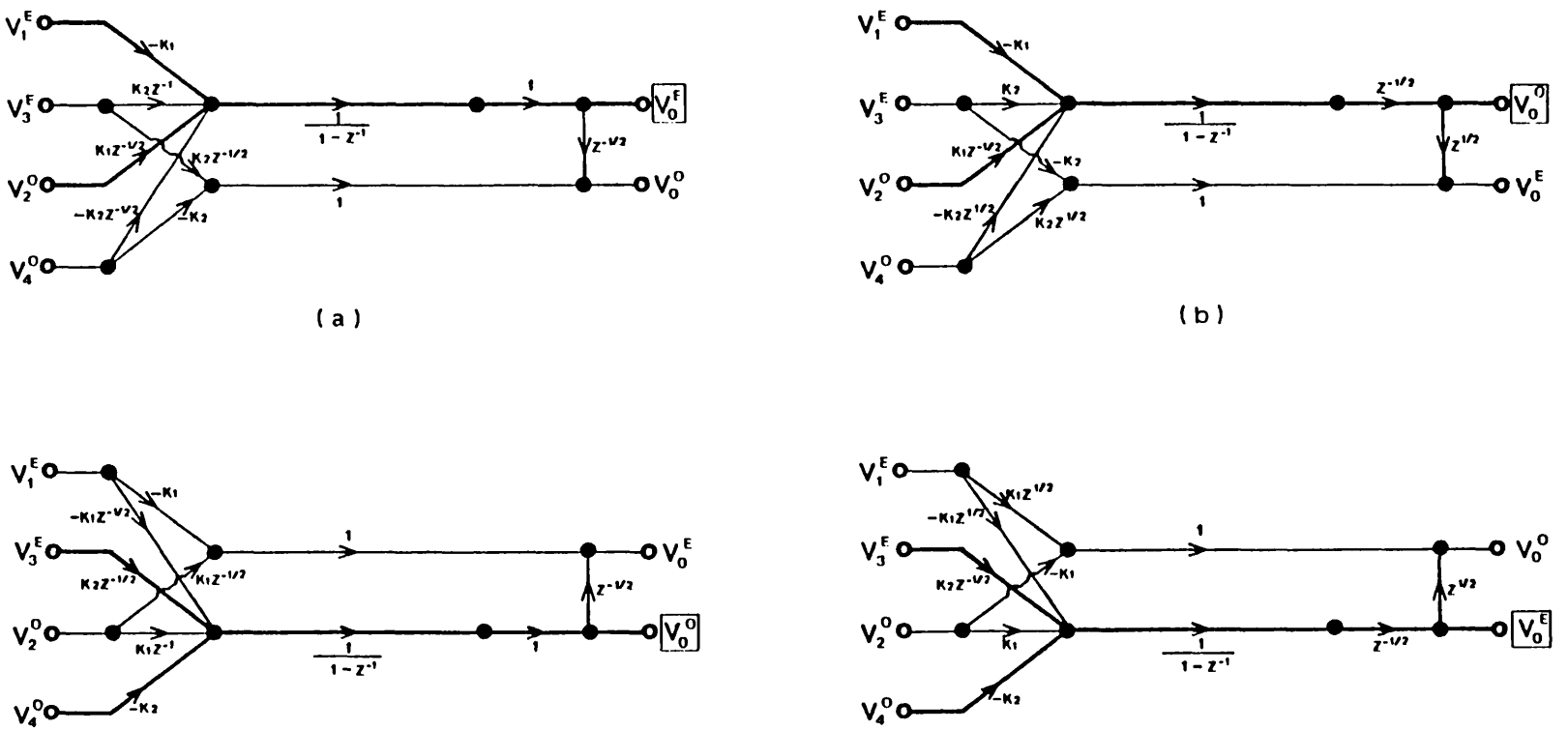


Fig.3.4: General SFG's for double-phase SC integrator, referring to:
(a) E-integrator with E phase output sampling;
(b) E-integrator with O phase output sampling;
(c) O-integrator with O phase output sampling;
(d) O-integrator with E phase output sampling

sampled in only one phase, which can be either the E phase or the O phase.

Rule 2 does not restrict the generality of subsequent developments in this Chapter. It simply means that in each switching period the sampled voltage of a double-phase integrator assumes only one possible magnitude value. This, of course, is implicit in single-phase integrators, which justifies Rule 1.

3.3 DEVELOPMENT OF SC BIQUAD BUILDING BLOCKS

The discrete-time biquadratic transfer function is expressed by

$$(3.1) \quad \ldots \qquad H(Z) = K \frac{1-2r_o\cos\theta_o z^{-1}+r_o^2 z^{-2}}{1-2r_p\cos\theta_p z^{-1}+r_p^2 z^{-2}}$$

where r_p, θ_p and r_o, θ_o are the polar coordinates of the poles and zeroes on the unit circle, respectively, and K is a gain factor. In the first part of the development of the SC biquad building blocks, we consider a basic loop of two SC integrators (TIL) in order to realise the quadratic denominator function. Then, in the second part, we augment the structure using feedforward switched-capacitor branches from the input terminal in order to realise also the quadratic numerator function.

3.3.1 Quadratic denominator function

By analogy with the active-RC case, one positive integrator and one negative integrator connected together

form the basic loop of a TIL biquadratic section (e.g. [3.9]). For the negative SC integrator we arbitrarily choose the E-integrator in Fig.3.1-a, with $V_2^o=0$. This is connected to a positive integrator, i.e. we make $V_4^o=0$ in the circuit of Fig.3.1-c, to form the basic loop shown in Fig.3.5-a. The corresponding SFG is given in Fig.3.5-b.[1] The discrete-time loop gain $L_g(Z)$ is

$$(3.2\text{-a}) \quad \ldots \qquad L_g(Z) = -\frac{C}{A} \cdot \frac{A}{B} \cdot \frac{z^{-1}}{\left(1 - z^{-1}\right)^2}$$

and the corresponding determinant $\Delta(Z)=1-L_g(Z)$ is

$$(3.2\text{-b}) \quad \ldots \qquad \Delta(Z) = \frac{1 + \left(\frac{A}{B} \cdot \frac{C}{D} - 2\right)z^{-1} + z^{-2}}{\left(1 - z^{-1}\right)^2}$$

The natural modes of the loop, i.e. the roots of the determinant, are on the unit circle ($r_p=1$), which means that the loop forms a resonator with infinite quality-factor Q.

For finite Q, damping for the loop can be provided in three ways, all of which are shown in Fig.3.5-c: (i) with capacitor E (capacitive or E-damping), (ii) with switched-capacitor F_1 (resistive-1 or F_1-damping) and (iii) with switched-capacitor F_2 (resistive-2 or F_2-damping). Switched-capacitors F_1 and F_2 implement negative feedback

[1] Later, we shall discuss an alternative arrangement of the switch phasing leading to a negative E-integrator and a positive E-integrator.

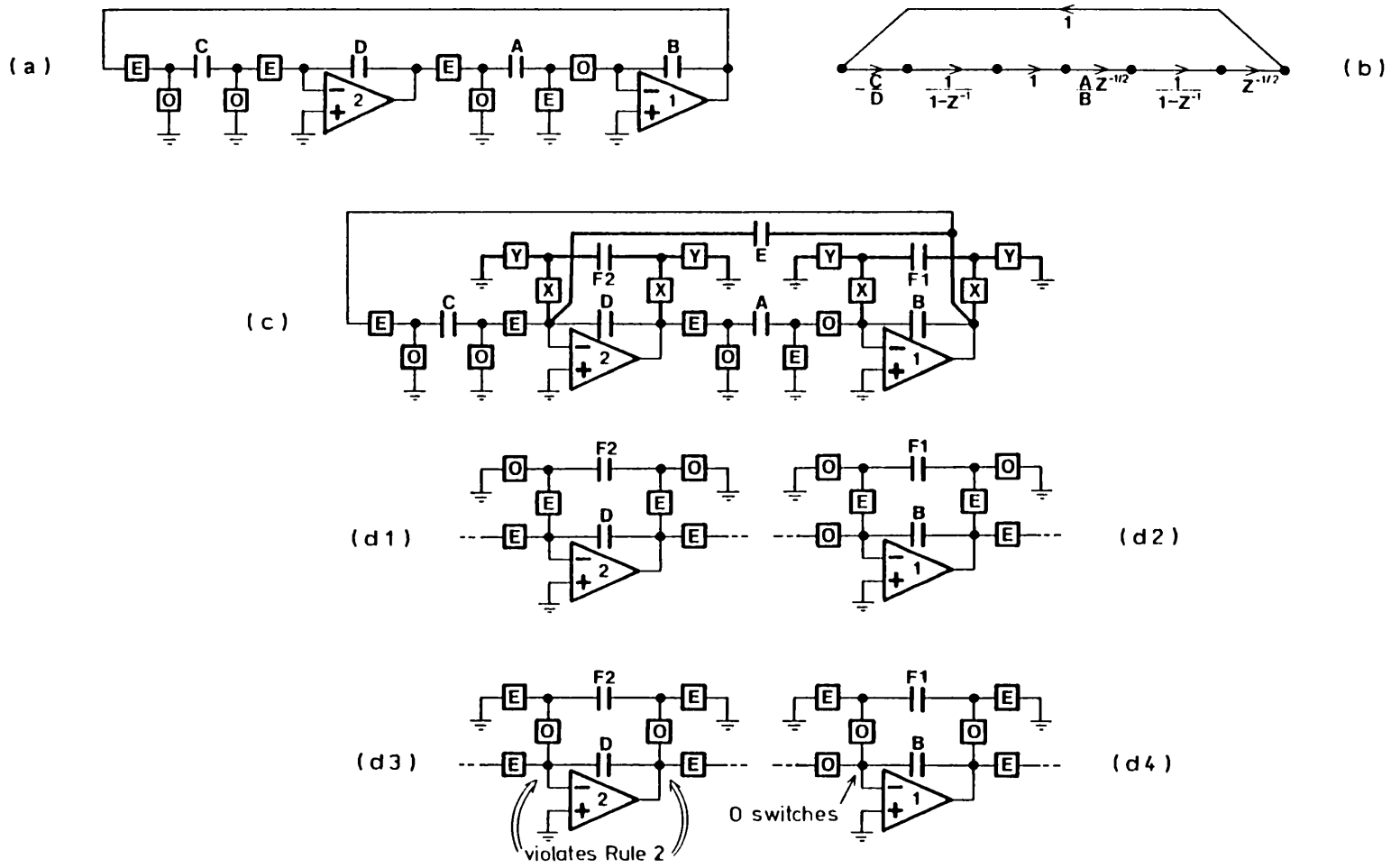


Fig.3.5: Illustrating the formation of the quadratic denominator function.
(a) E-integrator - O-integrator loop, and (b) corresponding SFG;
(c) General E-damping, F1-damping, and F2-damping for the loop;
(d) Alternative switch phasing for F1-damping, and F2-damping

paths using one of the four arrangements of the switch phasing indicated in Fig.3.5-d. The arrangement of Fig.3.5-d3 leads to a double-phase integrator that is sampled in both of the phases, and thus violates Rule 2. The output voltage of the amplifier in Fig.3.5-d4 is also sampled in both of the phases, and, therefore, because of Rules 1 and 2, it can only be an O-integrator. The remaining switch phasing arrangements in Fig.3.5-d1 and in Fig.3.5-d2, neither of which violate the interconnecting Rules, nor impose restrictions for further connections to the input of the amplifiers, lead to the SC biquadratic loop in Fig.3.6-a. The corresponding SFG of this loop is

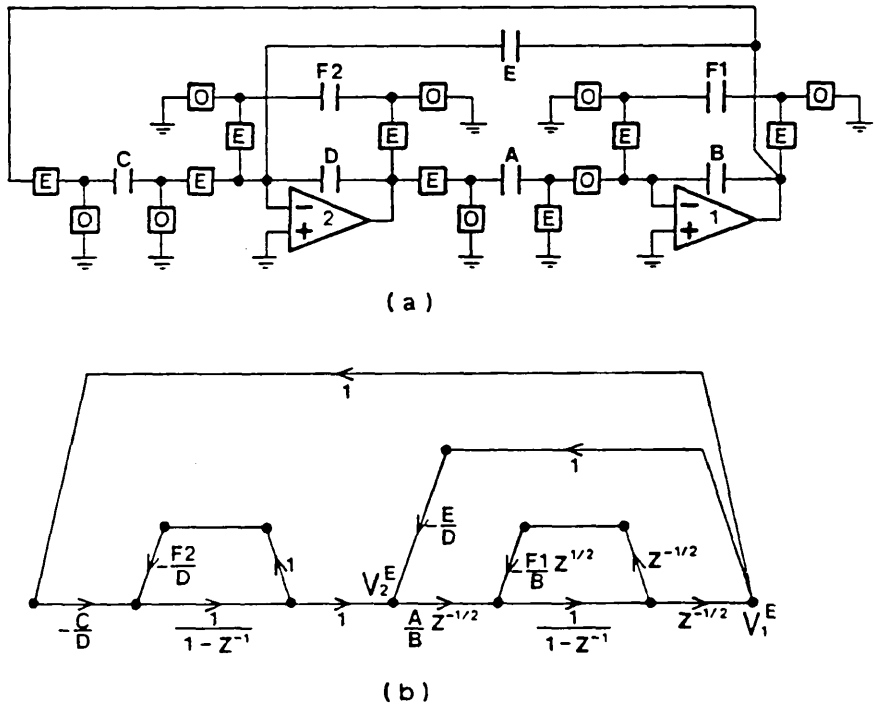


Fig.3.6: (a) Basic damped loop, and (b) SFG

given in Fig.3.6-b, yielding

$$(3.3\text{-a}) \ldots \quad L_g(Z) = \left[-\frac{C}{D}\cdot\frac{1}{\left(1+\frac{F2}{D}\right)-Z^{-1}}-\frac{E}{D}\right]\left[\frac{A}{B}\cdot\frac{Z^{-1}}{\left(1+\frac{F1}{B}\right)-Z^{-1}}\right]$$

for the discrete-time loop gain, and

$$(3.3\text{-b}) \quad \ldots \qquad \Delta(Z) = \frac{D(Z)}{\left[\left(1 + \frac{F2}{D}\right) - Z^{-1}\right]\cdot\left[\left(1 + \frac{F1}{B}\right) - Z^{-1}\right]}$$

for the corresponding determinant, where the quadratic denominator function D(Z) is given by

$$(3.4) \quad \ldots \qquad D(Z) = \left(1 + \frac{F1}{B}\right)\cdot\left(1 + \frac{F2}{D}\right) +$$

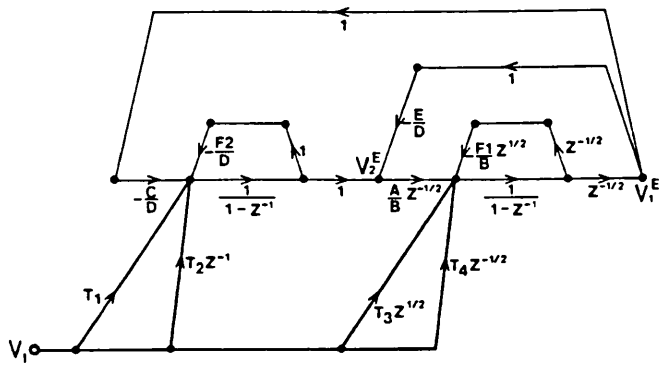
$$+ \left[\frac{C}{D}\frac{A}{B} + \left(\frac{E}{D}\frac{A}{B} - 1\right)\cdot\left(1 + \frac{F2}{D}\right) - \left(1 + \frac{F1}{B}\right)\right]Z^{-1} + \left(1 - \frac{E}{D}\frac{A}{B}\right)Z^{-2}$$

3.3.2 Quadratic numerator function

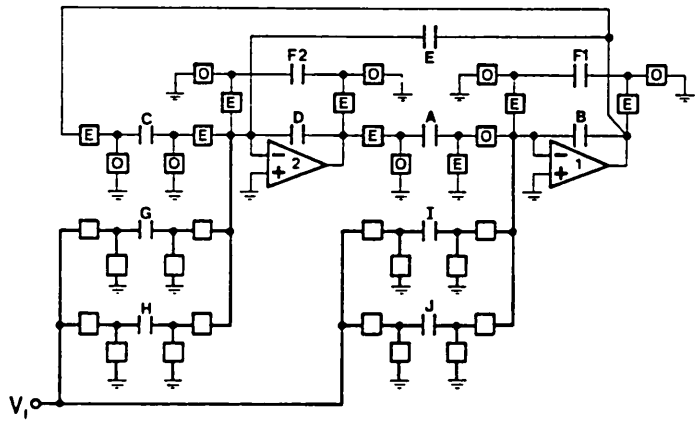
In order to realise the quadratic numerator function we utilise the technique of multiple feedforward paths from the input terminal [3.10], leading to the SFG of Fig.3.7-a which possesses four such feedforward branches. The transmission factors of these branches may have either a positive or a negative coefficient, and their delays are such that the feedforward transmission factors to the output terminals of OA1 and of OA2 have integer powers of Z, i.e. Z^0, Z^{-1} and Z^{-2}. By considering the voltage at the output of the OA's sampled in the E phase, i.e. V_1^E and V_2^E, we obtain from the SFG in Fig.3.7-a the feedforward transmission factor for OA1

(3.5) ...

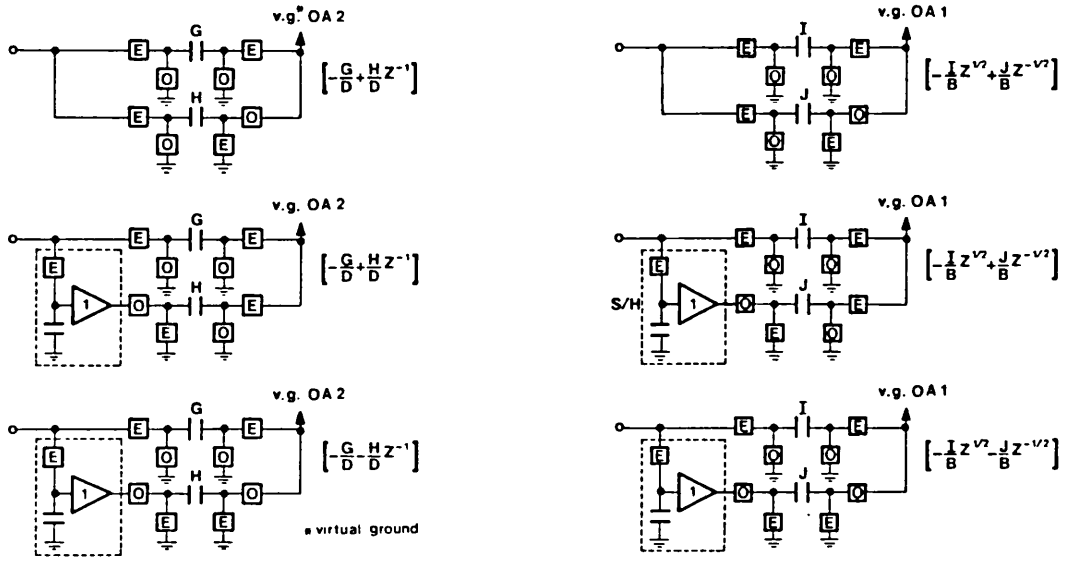
$$FF_1(Z) = \frac{T_3\left(1 + \frac{F2}{D}\right) + \left[T_1\frac{A}{B} - T_3 + T_4\left(1 + \frac{F2}{D}\right)\right]Z^{-1} + \left(T_2\frac{A}{B} - T_4\right)Z^{-2}}{\left[\left(1 + \frac{F1}{B}\right) - Z^{-1}\right]\cdot\left[\left(1 + \frac{F2}{D}\right) - Z^{-1}\right]}$$



(a)



(b)



(c)

Fig.3.7: Realisation of the quadratic numerator function. (a) Multiple feedforward paths from the input terminal; (b) Switched-capacitor implementation; (c) Discussion of switch phasing

The feedforward transmission factor for OA2 is given by

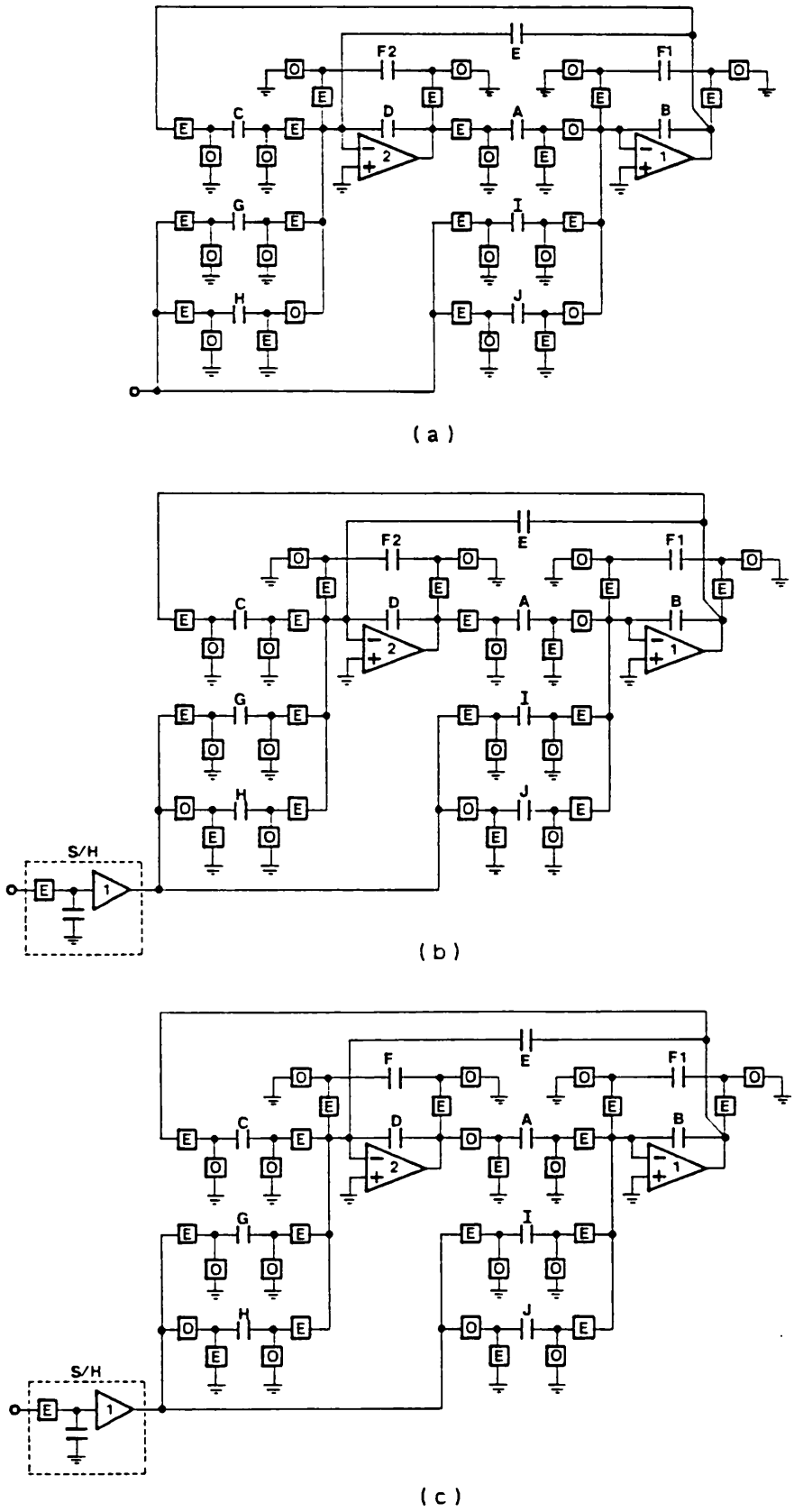
$$(3.6)\ \ldots\quad FF_2(Z) = \frac{\left[T_1\left(1+\frac{F1}{B}\right) - T_3\,\frac{E}{D}\left(1+\frac{F2}{D}\right) - T_3\,\frac{C}{D}\right]}{\left[\left(1+\frac{F1}{B}\right) - Z^{-1}\right]\cdot\left[\left(1+\frac{F2}{D}\right) - Z^{-1}\right]} +$$

$$+\frac{\left[T_2\left(1+\frac{F1}{B}\right) - T_4\,\frac{E}{D}\left(1+\frac{F2}{D}\right) - T_1 + T_3\,\frac{E}{D} - T_4\,\frac{C}{D}\right]Z^{-1} + \left(-2 + T_4\,\frac{E}{D}\right)Z^{-2}}{\left[\left(1+\frac{F1}{B}\right) - Z^{-1}\right]\cdot\left[\left(1+\frac{F2}{D}\right) - Z^{-1}\right]}$$

These expressions define two alternative forms for the quadratic numerator function. The multiple input feedforward paths are implemented using the parasitic-insensitive SC branches shown in Fig.3.7-b. The modulus of the coefficients T_1, T_2, T_3 and T_4 correspond to the capacitance ratios G/D, H/D, I/B and J/B, respectively, while the sign (positive or negative) of the coefficients as well as the delays of the transmission factors are determined by the switch phasing. In order to obtain the switch phasing of the input SC branches, we have to consider the general SFG's derived in the previous Section. For simplicity, we consider that the output voltage references for the SFG's of the double-phase SC integrators in the loop coincide with the sampled output voltages. This means that we utilise the SFG of Fig.3.4-a in connection with OA2, and the SFG of Fig.3.4-d in connection with OA1. Then, from both of these SFG's we obtain the switch phasing arrangements indicated in Fig.3.7-c, which provide the required transmission factors. In the situations where the input switches operate in different phases we utilise a sample and hold circuit to guarantee that the input signal is constant during the full switching period, i.e. $V_i^O = Z^{-1/2}.V_i^E$.

There are nine different circuits that we can obtain using the switch phasing arrangements shown in Fig.3.7-c. The most useful of these circuits are presented in Fig.3.8-a and in Fig.3.8-b, which produce two alternative types of switching with practical interest for interconnecting SC biquads in order to realise high order filters. The circuit in Fig.3.8-a samples the input signal only in the E phase, and hence does not need a sample and hold circuit at the input. However, since it comprises two double-phase SC integrators, it is always necessary to have a sampling switch at the output of the amplifiers. This type of switch phasing arrangement will be referred to as Type-A switching. In the circuit of Fig.3.8-b, the output voltage of OA2 does not change from the E phase to the O phase, and therefore we can alter the switch phasing of switched-capacitor A in order to obtain the circuit in Fig.3.8-c. In this circuit formed by two E-integrators, one negative and one positive, we may omit the sampling switches at the output of either OA1 or OA2 but, on the other hand, the input signal must be sampled and held. This type of switch phasing arrangement will be referred to as Type-B switching. For both SC biquads in Fig.3.8-a, with Type-A switching, and in Fig.3.8-c, with Type-B switching, the resulting coefficients for the feedforward SC branches are given by

$$(3.7)\ \ldots \qquad T_1 = -\frac{G}{D}\ ;\ T_2 = \frac{H}{D}\ ;\ T_3 = -\frac{I}{B}\ ;\ T_4 = \frac{J}{B}$$



(a)

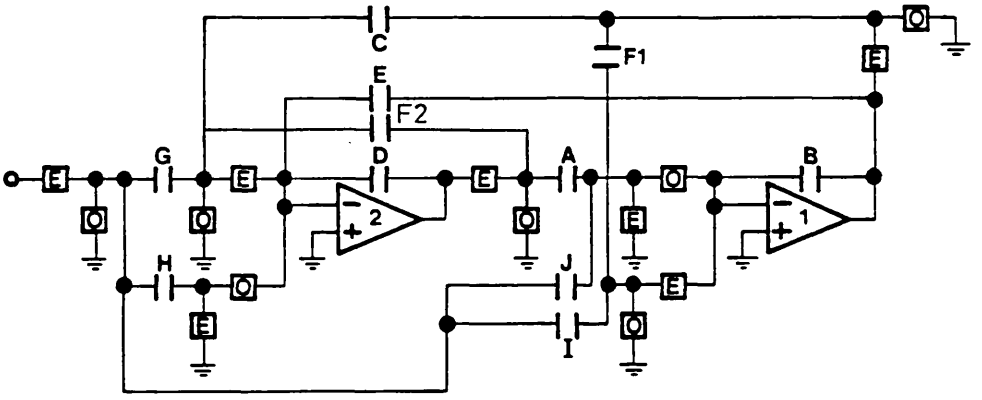
(b)

(c)

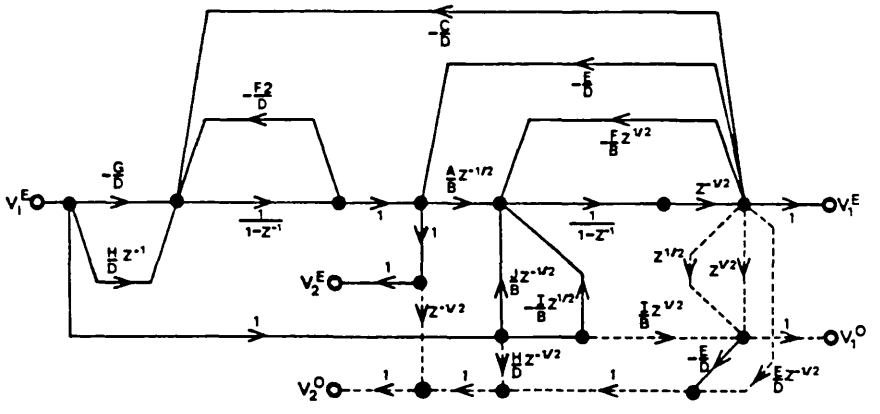
Fig.3.8: General SC biquads with alternative switch phasing

3.3.3 Biquadratic transfer functions

By allowing similarly switched-capacitors to share common switches, the SC biquad building blocks in Fig.3.8-a and in Fig.3.8-c, can have the more efficient implementations given in Fig.3.9-a and in Fig.3.10-a, respectively. The corresponding respective SFG's given in Fig.3.9-b, and in Fig.3.10-b, also show (in broken line) the complementary output voltage (sampled in the O phase), which we did not consider in the above derivation. The transfer functions corresponding to such complementary outputs, especially for the SC biquad with Type-A switching



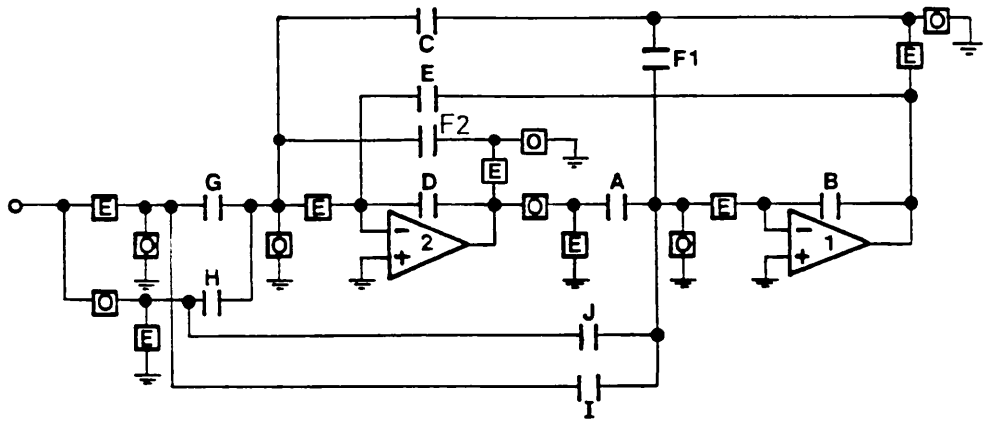
(a)



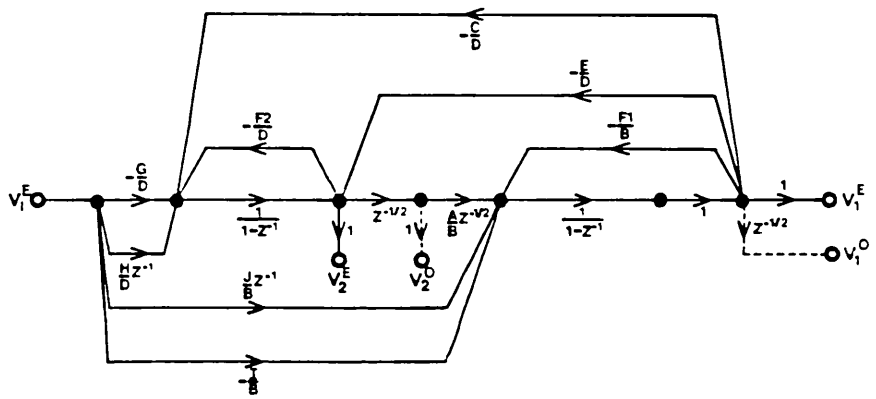
(b)

Fig.3.9: (a) General SC biquad with Type-A switching;
(b) Signal Flow Graph

(Fig.3.9-a and Fig.3.10-a), have little practical interest [3.11]. The transfer functions corresponding to the output voltage reference (sampled in the E phase), which are derived below, are the same for the SC biquads with both types of switching.



(a)



(b)

Fig.3.10: (a) General SC biquad with Type-B switching;
(b) Signal Flow Grapph

By applying Mason's formula [3.12], the transfer functions of the SC biquads sampled in the E phase are given by

(3.8) ... $$H_1(Z) = \frac{FF_1(Z)}{\Delta(Z)}$$

with respect to the output terminal of OA1 (terminal 1), and by

$$(3.9)\ \ldots \qquad H_2(Z) = \frac{FF_2(Z)}{\Delta(Z)}$$

referring to the output terminal of OA2 (terminal 2). By substituting (3.7) into (3.5) and (3.6) in order to express the numerator quadratic functions in terms of the capacitance ratios, and by using (3.3-b) and (3.4), we arrive at the expressions of the biquadratic transfer functions

$$(3.10)\ \ldots \qquad H^E_{1A}(Z) = \frac{V^E_1(Z)}{V_i(Z)} = -\frac{\hat{I}(1+\hat{F}2)}{(1+\hat{F}1)\cdot(1+\hat{F}2)} \cdot \frac{1 - \dfrac{\hat{I}+\hat{J}(1+\hat{F}2)-\hat{A}\hat{G}}{\hat{I}(1+\hat{F}2)}\cdot Z^{-1} + \dfrac{\hat{J}-\hat{H}\hat{A}}{\hat{I}(1+\hat{F}2)}\cdot Z^{-2}}{1 - \dfrac{1+\hat{F}1-\hat{C}\hat{A}-(1+\hat{F}2)(\hat{E}\hat{A}-1)}{(1+\hat{F}1)\cdot(1+\hat{F}2)}\cdot Z^{-1} \dfrac{1-\hat{E}\hat{A}}{(1+\hat{F}1)\cdot(1+\hat{F}2)}\cdot Z^{-2}}$$

for output terminal 1, and

$$(3.11)\ \ldots \qquad H^E_{2A}(Z) = \frac{V^E_2(Z)}{V_i(Z)} = \frac{\hat{I}\hat{E}(1+\hat{F}2)+\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}{(1+\hat{F}1)(1+\hat{F}2)} \cdot \frac{1 - \dfrac{\hat{I}\hat{E}+\hat{J}\hat{E}(1+\hat{F}2)+\hat{J}\hat{C}-\hat{G}-\hat{H}(1+\hat{F}1)}{\hat{I}\hat{E}(1+\hat{F}2)+\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}\cdot Z^{-1} + \dfrac{\hat{J}\hat{E}-\hat{H}}{\hat{I}\hat{E}(1+\hat{F}2)+\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}\cdot Z^{-2}}{1 - \dfrac{1+\hat{F}1-\hat{C}\hat{A}-(1+\hat{F}2)(\hat{E}\hat{A}-1)}{(1+\hat{F}1)(1+\hat{F}2)}\cdot Z^{-1} + \dfrac{1-\hat{E}\hat{A}}{(1+\hat{F}1)(1+\hat{F}2)}\cdot Z^{-2}}$$

for output terminal 2. The capacitance ratios $\hat{X}$ correspond to the simplified representation given in Table 3.1.

For each type of damping, i.e. E-damping (F_1=F_2=0), F_1-damping (E=F_2=0), and F_2-damping (E=F_1=0), Table 3.2 and Table 3.3 summarise the expressions for the coefficients of the biquadratic discrete-time transfer function (3.1) in

A/B	$\hat{A}$
F1/B	$\hat{F}1$
I/B	$\hat{I}$
J/B	$\hat{J}$
C/D	$\hat{C}$
E/D	$\hat{E}$
F2/D	$\hat{F}2$
G/D	$\hat{G}$
H/D	$\hat{H}$

Table 3.1: Simplified representation of capacitance ratios

terms of the capacitance ratios. Since the denominator coefficients are a function only of the basic loop, their expressions do not depend on which of the output terminals, from OA1 or from OA2, is considered. On the contrary, we find different expressions for the numerator coefficients because the feedforward paths to the output terminal 1 and to the output terminal 2 are different. The quadratic numerator function corresponding to output terminal 1 is

TYPE OF DAMPING	$2r_p \cos \theta_p$	r_p^2
E	$-\hat{C}\hat{A} - \hat{E}\hat{A} + 2$	$1 - \hat{E}\hat{A}$
F1	$\dfrac{-\hat{C}\hat{A} + \hat{F}1 + 2}{1 + \hat{F}1}$	$\dfrac{1}{1 + \hat{F}1}$
F2	$\dfrac{-\hat{C}\hat{A} + \hat{F}2 + 2}{1 + \hat{F}2}$	$\dfrac{1}{1 + \hat{F}2}$

Table 3.2: Coefficients of the quadratic denominator function

TYPE OF DAMPING	OUTPUT TERMINAL	K	$2r_o \cos\theta_o$	r_o^2
E	1	$-\hat{I}$	$\frac{-\hat{A}\hat{G}+\hat{I}+\hat{J}}{\hat{I}}$	$\frac{\hat{J}-\hat{A}\hat{H}}{\hat{I}}$
	2	$\hat{I}(\hat{E}+\hat{C})-\hat{G}$	$\frac{-\hat{G}-\hat{H}+\hat{I}\hat{E}+\hat{J}(\hat{E}+\hat{C})}{\hat{I}(\hat{E}+\hat{C})-\hat{G}}$	$\frac{\hat{J}\hat{E}-\hat{H}}{\hat{I}(\hat{E}+\hat{C})-\hat{G}}$
F1	1	$-\frac{\hat{I}}{1+\hat{F}1}$	$\frac{-\hat{A}\hat{G}+\hat{I}+\hat{J}}{\hat{I}}$	$\frac{\hat{J}-\hat{A}\hat{H}}{\hat{I}}$
	2	$\frac{\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}{(1+\hat{F}1)}$	$\frac{-\hat{G}-\hat{H}(1+\hat{F}1)+\hat{J}\hat{C}}{\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}$	$-\frac{\hat{H}}{\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}$
F2	1	$-\hat{I}$	$\frac{-\hat{A}\hat{G}+\hat{I}+\hat{J}(1+\hat{F}2)}{\hat{I}(1+\hat{F}2)}$	$\frac{\hat{J}-\hat{A}\hat{H}}{\hat{I}(1+\hat{F}2)}$
	2	$\frac{\hat{I}\hat{C}-\hat{G}}{1+\hat{F}2}$	$\frac{-\hat{G}-\hat{H}+\hat{J}\hat{C}}{\hat{I}\hat{C}-\hat{G}}$	$-\frac{\hat{H}}{\hat{I}\hat{C}-\hat{G}}$

Table 3.3: Coefficients of the quadratic numerator function

usually preferred for the design of cascade SC biquads because it yields simpler solutions for the capacitance ratios than the alternative numerator function corresponding to output terminal 2. But, on the other hand, for the design of SC coupled-biquad structures it is necessary to have SC biquads both with negative and with positive gain constants [3.13], which the numerator function associated with output terminal 1 does not realise. Therefore, for such situations, we shall utilise SC biquads with output terminal 1 for the realisation of transfer functions with a negative gain constant, whereas SC biquads with output terminal 2 are employed for the realisation of transfer functions with a positive gain constant.

3.4 SC BIQUADS WITH BILINEAR TRANSFORMED TRANSFER FUNCTIONS

3.4.1 Design equations

In order to derive the discrete-time biquadratic transfer function from the continuous-time domain, we employ the bilinear $\tilde{s}$-to-Z transformation

$$\tilde{s} = 2F_S \cdot \frac{1 - Z^{-1}}{1 + Z^{-1}} \qquad (3.12)$$

which, as we stated in Chapter 1, maps the entire continuous-time plan into the discrete-time plan, and, by this means, preserves the magnitude characteristic of the frequency response. Such mapping, however, does not preserve a linear relationship between the frequencies $\tilde{\omega}$ of the continuous-time domain, and the frequencies ω of the discrete-time domain. Instead, there is a tangent relationship

$$\tilde{\omega} = 2F_S \cdot \tan \frac{\omega}{2F_S} \qquad (3.13)$$

the effect of which has to be taken into account by prewarping of the original continuous-time transfer function [3.14]. This will be explained below.

In the continuous-time biquadratic transfer function

$$H_a(\tilde{s}) = \frac{\tilde{a}_2\tilde{s}^2 + \tilde{a}_1\tilde{s} + \tilde{a}_o}{\tilde{s}^2 + \frac{\tilde{\omega}_p}{Q_p}\tilde{s} + \tilde{\omega}_p^2} \qquad (3.14)$$

the coefficients $\tilde{a}_2$, $\tilde{a}_1$ and $\tilde{a}_0$ of the quadratic numerator function, and the coefficients $\tilde{\omega}_p$ and $\tilde{Q}_p$ of the quadratic denominator function correspond to the prewarped values of the desired coefficients a_2, a_1, a_0, ω_p and Q_p of the frequency response of the SC biquad. For the complex conjugate pole-pair for example, the prewarped pole frequency $\tilde{\omega}_p$ is readily calculated from (3.13) yielding

$$\tilde{\omega}_p = 2F_s \cdot \tan \frac{\omega_p}{2F_s} \qquad (3.15)$$

For prewarping of the Q-factor we determine, in the first place, the frequencies

$$\omega_1 = \omega_p \left(1 - \frac{1}{2Q_p}\right) \qquad (3.16\text{-a})$$

and

$$\omega_2 = \omega_p \left(1 + \frac{1}{2Q_p}\right) \qquad (3.16\text{-b})$$

which represent the -3dB frequencies of the peaking response (for, say Q_p>5). After applying the prewarping formula (3.13) to both of the frequencies in (3.16), and by using (3.15), we obtain the prewarped pole Q-factor

$$\tilde{Q}_p = \frac{\tan \frac{\omega_p}{2F_s}}{\tan \frac{\omega_p(1+1/2Q_p)}{2F_s} - \tan \frac{\omega_p(1-1/2Q_p)}{2F_s}} \qquad (3.17)$$

The subsequent steps to obtain the design equations for the

capacitance ratios of the SC biquad are the following: (i) to apply (3.12) to (3.14) in order to express the discrete-time transfer function (3.1) in terms of the prewarped continuous-time coefficients, and (ii) to equate the resulting discrete-time coefficients to the corresponding expressions in terms of the capacitance ratios given in Table 3.2 and in Table 3.3. The resulting design equations are summarised in Table 3.4, for the quadratic denominator function, and in Table 3.5 for the

TYPE OF DAMPING	DESIGN EQUATIONS
E	$1 - \hat{E}\hat{A} = \dfrac{1 - \frac{1}{\tilde{Q}p}\left(\frac{\tilde{\omega}p}{2Fs}\right) + \left(\frac{\tilde{\omega}p}{2Fs}\right)^2}{m}$ $2 - \hat{C}\hat{A} - \hat{E}\hat{A} = 2\,\dfrac{1 - \left(\frac{\tilde{\omega}p}{2Fs}\right)^2}{m}$
F1	$\dfrac{1}{1 + \hat{F}1} = \dfrac{1 - \frac{1}{\tilde{Q}p}\left(\frac{\tilde{\omega}p}{2Fs}\right) + \left(\frac{\tilde{\omega}p}{2Fs}\right)^2}{m}$ $\dfrac{1}{1 + \hat{F}1}\left(2 + \hat{F}1 - \hat{C}\hat{A}\right) = 2\,\dfrac{1 - \left(\frac{\tilde{\omega}p}{2Fs}\right)^2}{m}$
F2	$\dfrac{1}{1 + \hat{F}2} = \dfrac{1 - \frac{1}{\tilde{Q}p}\left(\frac{\tilde{\omega}p}{2Fs}\right) + \left(\frac{\tilde{\omega}p}{2Fs}\right)^2}{m}$ $\dfrac{1}{1 + \hat{F}2}\left(2 + \hat{F}2 - \hat{C}\hat{A}\right) = 2\,\dfrac{1 - \left(\frac{\tilde{\omega}p}{2Fs}\right)^2}{m}$

$$m = 1 + \frac{1}{\tilde{Q}p}\left(\frac{\tilde{\omega}p}{2Fs}\right) + \left(\frac{\tilde{\omega}p}{2Fs}\right)^2$$

Table 3.4: Design equations for the quadratic denominator function

	TYPE OF DAMPING	OUTPUT TERMINAL	SC BIQUAD COEFFICIENTS	LOWPASS	HIGHPASS	BANDPASS	GENERAL NOTCH	ALLPASS
K	E	1	$\hat{I}$	$H_o \dfrac{\left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}{1 + \frac{1}{Q_p}\left(\frac{\tilde{\omega}_p}{2Fs}\right) + \left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}$	$H_o \dfrac{1}{1 + \frac{1}{Q_p}\left(\frac{\tilde{\omega}_p}{2Fs}\right) + \left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}$	$H_o \dfrac{\frac{1}{Q_p}\left(\frac{\tilde{\omega}_p}{2Fs}\right)}{1 + \frac{1}{Q_p}\left(\frac{\tilde{\omega}_p}{2Fs}\right) + \left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}$	$H_o \dfrac{1 + \left(\frac{\tilde{\omega}_o}{2Fs}\right)^2}{1 + \frac{1}{Q_p}\left(\frac{\tilde{\omega}_p}{2Fs}\right) + \left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}$	1
		2	$\hat{I}(\hat{E}+\hat{C})-\hat{G}$					
	F1	1	$\dfrac{\hat{I}}{1+\hat{F}1}$					
		2	$\dfrac{\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}{1+\hat{F}1}$					
	F2	1	$\hat{I}$					
		2	$\dfrac{\hat{I}\hat{C}-\hat{G}}{1+\hat{F}2}$					
$2r_o\cos\theta_o$	E	1	$\dfrac{\hat{I}+\hat{J}-\hat{A}\hat{G}}{\hat{I}}$	-2	2	0	$2\dfrac{1 - \left(\frac{\tilde{\omega}_o}{2Fs}\right)^2}{1 + \left(\frac{\tilde{\omega}_o}{2Fs}\right)^2}$	$2\dfrac{1 - \left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}{1 + \frac{1}{Q_p}\left(\frac{\tilde{\omega}_p}{2Fs}\right) + \left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}$
		2	$\dfrac{\hat{I}\hat{E}+\hat{J}(\hat{E}+\hat{C})-\hat{G}-\hat{H}}{\hat{I}(\hat{E}+\hat{C})-\hat{G}}$					
	F1	1	$\dfrac{\hat{I}+\hat{J}-\hat{A}\hat{G}}{\hat{I}}$					
		2	$\dfrac{\hat{J}\hat{C}-\hat{G}-\hat{H}(1+\hat{F}1)}{\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}$					
	F2	1	$\dfrac{\hat{I}+\hat{J}(1+\hat{F}2)-\hat{A}\hat{G}}{\hat{I}(1+\hat{F}2)}$					
		2	$\dfrac{\hat{J}\hat{C}-\hat{G}-\hat{H}}{\hat{I}\hat{C}-\hat{G}}$					
r_o^2	E	1	$\dfrac{\hat{J}-\hat{A}\hat{H}}{\hat{I}}$	1	1	-1	1	$\dfrac{1 + \frac{1}{Q_p}\left(\frac{\tilde{\omega}_p}{2Fs}\right) - \left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}{1 + \frac{1}{Q_p}\left(\frac{\tilde{\omega}_p}{2Fs}\right) + \left(\frac{\tilde{\omega}_p}{2Fs}\right)^2}$
		2	$\dfrac{\hat{J}\hat{E}-\hat{H}}{\hat{I}(\hat{E}+\hat{C})-\hat{G}}$					
	F1	1	$\dfrac{\hat{J}-\hat{A}\hat{H}}{\hat{I}(1+\hat{F}2)}$					
		2	$\dfrac{-\hat{H}}{\hat{I}\hat{C}-\hat{G}(1+\hat{F}1)}$					
	F2	1	$\dfrac{\hat{J}-\hat{A}\hat{H}}{\hat{I}}$					
		2	$\dfrac{-\hat{H}}{\hat{I}\hat{C}-\hat{G}}$					

Table 3.5: Design equations for the quadratic numerator function

various solutions of the quadratic numerator function (e.g. lowpass, bandpass) [3.11].

3.4.2 Estimation of sensitivities

In SC biquads it is usual to estimate the sensitivities of the quadratic numerator function with respect to changes of the nominal capacitance values on a case-by-case basis, in view of the many possible forms the numerator may assume (see Table 3.5) [3.15]-[3.17].

In order to estimate the sensitivities of the quadratic denominator function it is convenient to express the complex conjugate pole-pair of the SC biquad in terms of the polar coordinates [3.18], which leads to

$$\omega_p = 2F_s\left[\frac{1 - 2r_p\cos\theta_p + r_p^2}{1 + 2r_p\cos\theta_p + r_p^2}\right]^{1/2} \quad \text{(3.18-a)} \ldots$$

for the frequency, and

$$Q_p = 2F_s \frac{\left[\left(1 - 2r_p\cos\theta_p + r_p^2\right).\left(1 + 2r_p\cos\theta_p + r_p^2\right)\right]^{1/2}}{1 - r_p^2} \quad \text{(3.18-b)} \ldots$$

for the Q-factor of the complex conjugate pole-pair. By entering the expressions of Table 3.2 into (3.18), we obtain the expressions in terms of the capacitance values given in Table 3.6. Then, by applying the classical definition of differential sensitivity [3.19]

$$S_x^{\omega_p} = \frac{\delta\omega_p}{\delta x} \cdot \frac{x}{\omega_p} \quad ; \quad S_x^{Q_p} = \frac{\delta Q_p}{\delta x} \cdot \frac{x}{Q_p} \quad \text{(3.19)} \ldots$$

we obtain, after some simple algebraic manipulations, the general sensitivity expressions for ω_p and for Q_p summarised in Table 3.7, and which we discuss below.

TYPE OF DAMPING	$(\omega p/2Fs)^2$	$2Qp$
E	$\frac{AC}{4BD - 2EA - AC}$	$\frac{[AC(4BD - 2EA - AC)]^{1/2}}{EA}$
F1	$\frac{AC}{4BD + 2F_1D - AC}$	$\frac{[AC(4BD + 2F_1D - AC)]^{1/2}}{F_1D}$
F2	$\frac{AC}{4BD + 2F_2B - AC}$	$\frac{[AC(4BD + 2F_2B - AC)]^{1/2}}{F_2B}$

Table 3.6: Expressions for the analysis of the sensitivities of the quadratic denominator function

The values of the capacitance ratios of the quadratic denominator function depend on the Q-factor Q_p, on the one hand, and on the sampling ratio F_s/f_p, on the other hand. For SC biquads with moderate to high Q-factors (e.g. $Q_p>5$) the damping terms are small, i.e. $\hat{E}\hat{A}<<1$, $\hat{F}_1<<1$ or $\hat{F}_2<<1$, and, when the sampling ratio is high, i.e. $F_s/f_p>>1$, we have also $\hat{C}\hat{A}<<1$. In both these situations, the sensitivities of the pole frequency with respect to the capacitance values A, B, C and D are approximately

$$\left|S_A^{\omega_p}\right| = \left|S_B^{\omega_p}\right| = \left|S_D^{\omega_p}\right| \simeq \left|S_C^{\omega_p}\right| \simeq \frac{1}{2}$$

The sensitivities of ω_p with respect to the damping

TYPE OF DAMPING	CAPACITOR X	$S_x^{\omega p}$	S_x^{Qp}
E	A	$\frac{2}{E(X)}$	$-\frac{1}{E(X)}$
	B	$-\frac{2}{E(X)}$	$\frac{2}{E(X)}$
	C	$\frac{2-\hat{E}\hat{A}}{E(X)}$	$\frac{2-\hat{E}\hat{A}}{E(X)}$
	D	$-\frac{2}{E(X)}$	$\frac{2}{E(X)}$
	E	$\frac{\hat{E}\hat{A}}{E(X)}$	$-\frac{4-\hat{E}\hat{A}-\hat{A}\hat{C}}{E(X)}$
F1	A	$\frac{2}{F_1(X)}$	$\frac{2+\hat{F}_1-\hat{A}\hat{C}}{F_1(X)}$
	B	$-\frac{2}{F_1(X)}$	$\frac{2}{F_1(X)}$
	C	$\frac{2+\hat{F}1}{F_1(X)}$	$\frac{2+\hat{F}_1-\hat{A}\hat{C}}{F_1(X)}$
	D	$-\frac{2+\hat{F}1}{F_1(X)}$	$-\frac{2+\hat{F}_1-\hat{A}\hat{C}}{F_1(X)}$
	F1	$-\frac{\hat{F}_1}{F_1(X)}$	$-\frac{4+\hat{F}_1-\hat{A}\hat{C}}{F_1(X)}$
F2	A	$\frac{2}{F_2(X)}$	$\frac{2+\hat{F}_2-\hat{A}\hat{C}}{F_2(X)}$
	B	$-\frac{2+\hat{F}2}{F_2(X)}$	$-\frac{2+\hat{F}_2-\hat{A}\hat{C}}{F_2(X)}$
	C	$\frac{2+\hat{F}2}{F_2(X)}$	$\frac{2+\hat{F}_2+\hat{A}\hat{C}}{F_2(X)}$
	D	$-\frac{2}{F_2(X)}$	$\frac{2}{F_2(X)}$
	F2	$-\frac{\hat{F}2}{F_2(X)}$	$-\frac{4+\hat{F}_2-\hat{A}\hat{C}}{F_2(X)}$
$E(X) = 4-2\hat{E}\hat{A}-\hat{A}\hat{C}$ $F1(X) = 4+2\hat{F}_1-\hat{A}\hat{C}$ $F2(X) = 4+2\hat{F}_2-\hat{A}\hat{C}$			

Table 3.7: Sensitivity expressions of the pole frequency, and pole Q-factor

capacitors E, F_1 and F_2 are much smaller, especially when the ratio F_s/f_p becomes very large. On the other hand, the larger sensitivities of the Q-factor occur with respect to the damping capacitors giving approximately

$$\left|S_E^{Q_p}\right| \simeq \left|S_{F_1}^{Q_p}\right| = \left|S_{F_2}^{Q_p}\right| \simeq \frac{1}{2}$$

Another situation of practical interest in some SC biquads is when we adopt a low sampling ratio F_s/f_p for the purpose of capacitance spread minimisation, as we shall discuss in Section 3.6. For $F_s/f_p=4$, for example, we have $\hat{C}\hat{A}=2$ yielding

$$\left|S_A^{\omega_p}\right| = \left|S_B^{\omega_p}\right| = \left|S_D^{\omega_p}\right| \simeq \left|S_C^{\omega_p}\right| \simeq 1$$

which indicates some increase of the sensitivities of the pole frequency compared to the previous situations with higher sampling ratio F_s/f_p. This situation trades-off with improved accuracy of the capacitance ratios, which we obtain by means of reducing F_s/f_p. When the SC biquads have very high Q-factors, say above 50, it is crucial to adopt a low sampling ratio. Otherwise, as we mentioned in Section 3.1, the capacitance ratios become unacceptably large, both from the point of view of their accuracies and from the point of view of the silicon area required for implementation.

Overall, the sensitivities of the quadratic denominator function of SC biquads are comparable to the case of active-RC biquads, and, therefore, have similar

properties with respect to the sensitivity of the amplitude response [3.9],[3.19],[3.20].

3.5 PRINCIPLES FOR THE ANALYSIS OF CAPACITANCE SPREAD

3.5.1 Definitions and operations

In the SC biquads derived in Section 3.3 we shall consider the following three groups, or sets, of capacitors:

The Loop Capacitor Set (LCS) comprises the capacitors A, B, C and D that form the resonator loop of the SC biquad and the capacitors E, F_1 and F_2 that define the type of damping. This capacitor set determines the quadratic denominator function and is symbolically represented by the SFG shown in Fig.3.11.

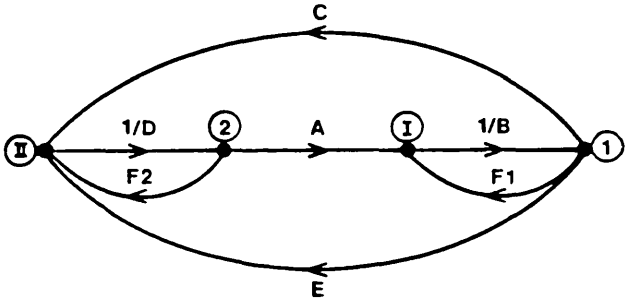
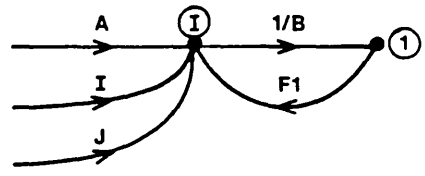


Fig.3.11: Loop Capacitor Set

The Integrator Capacitor Set-1 (ICS-1) comprises the capacitors of the SC integrator associated with OA1, i.e. the input capacitors I and J, the loop capacitors A and B and the damping capacitor F_1. This capacitor set is represented by the SFG of Fig.3.12, where all the

capacitors have one terminal connected to the virtual ground of the amplifier.

Fig.3.12:
Integrator Capacitor Set-1



The Integrator Capacitor Set-2 (ICS-2) comprises the input capacitors G and H, the loop capacitors C and D and the damping capacitors E and F_2, all of which have one terminal connected to the virtual ground of OA2, which forms the other SC integrator in the loop. This capacitor set is represented by the SFG of Fig.3.13.

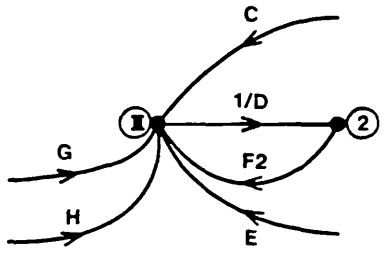


Fig.3.13:
Integrator Capacitor Set-2

In each capacitor set there will be a maximum and a minimum capacitance value, the ratio of which defines the capacitance spread of the capacitor set. Usually, the maximum capacitance values are associated with the capacitors A, B, C and D of the resonator loop, whereas the minimum capacitance values are associated either with the damping capacitors E, F_1 and F_2 or with the input capacitors G, H, I and J that define the type of response

of the SC biquad. Hence, we have:

$$\underline{\text{Capacitance Loop Spread}}: \ (CLS)=\frac{\text{Max}\{A,B,C,D\}}{\text{Min}\{E,F_1,F_2\}}$$

$$\underline{\text{Capacitance Set Spread-1}}: \ (CSS\text{-}1)=\frac{\text{Max}\{A,B\}}{\text{Min}\{F_1,I,J\}}$$

$$\underline{\text{Capacitance Set Spread-2}}: \ (CSS\text{-}2)=\frac{\text{Max}\{C,D\}}{\text{Min}\{E,F_2,G,H\}}$$

There are two scaling operations, namely capacitance scaling and voltage scaling, that affect the capacitance values in the SC biquad, which are viewed as operations of contour scaling [3.10] in the SFG's shown above. Capacitance scaling is applied to a contour around either node I or node II (virtual grounds of the OA's), respectively in the graphs of ICS-1 and ICS-2, as illustrated in the example of Fig.3.14. In Fig.3.14-a, let I be the minimum capacitance value ICS-1. For capacitance normalisation, with I=1, we apply a scaling factor 1/I to the closed contour around node I such that the incoming branches (A, F_1, I and J) are multiplied by 1/I, while the outgoing branch (1/B) is divided by the scaling factor, i.e. multiplied by I. This produces the normalised capacitance values in Fig.3.14-b. Such capacitance scaling operations can be carried-out independently to either CCS-1 or CCS-2 (the capacitor sets define two separate contours)

(a) Original capacitance values (I=minimum)

(b) Normalised capacitance values (minimum=1 unit)

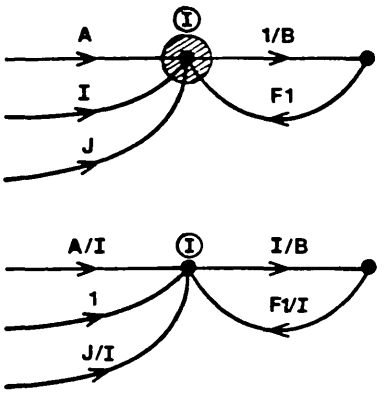


Fig.3.14: Capacitance scaling

such that, for example, they have equal minimum capacitance values. Then, the capacitor set with larger capacitance spread will determine the overall capacitance spread of the SC biquad.

The operation of voltage scaling is employed in order to modify the signal amplitude at the output of the OA's such that, for example, they have equal maximum value in order to obtain maximum signal handling capability [3.21]. Voltage scaling consists of applying an operation of contour scaling around the output terminals of the OA's, which are represented by node 1, and by node 2, in the SFG of Fig.3.11. In the example shown in Fig.3.15, the scaling

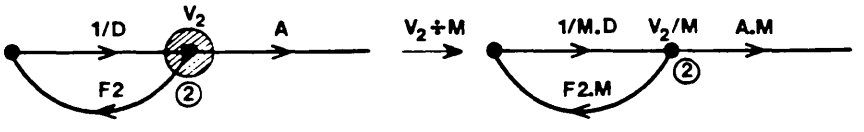


Fig.3.15: Voltage scaling

operation multiplies the output voltage of OA2 by a factor

1/M, i.e. the incoming branches (1/D) are multiplied by 1/M, while the outgoing branches (F_2, A) are multiplied by M. Since such scaling operation affects only capacitor A of ICS-1, and capacitors F_2 and D of ICS-2, the corresponding capacitor set spreads will be affected. A similar situation occurs when we scale the output voltage of OA1.

3.5.2 Loop voltage magnification and loop gain

The loop voltage magnification and the loop gain are defined with respect to the SFG of Fig.3.11 where, for simplicity, we neglect the damping capacitors E, F_1 and F_2. This approximation is valid for moderate to high Q-factors. The loop voltage magnification L_m corresponds to the ratio between the output voltages of the amplifiers, i.e.

$$(3.20) \ldots \qquad L_m = \frac{V_2}{V_1} = \left[\frac{C/D}{A/B}\right]^{1/2}$$

For maximum signal handling capabilitiy, i.e. $L_m=1$, we have C/D=A/B. Otherwise, the ratio (C/D)/(A/B) determines the magnification of one output voltage with respect to the other.

The product $(C/D).(A/B)=L_g$ defines the loop gain L_g of the SC biquad, which is essentially a function of the sampling ratio F_s/f_p. This is obtained from the expressions in Table 3.4 yielding

$$(3.21) \ldots \qquad L_g = \frac{C}{D} \cdot \frac{A}{B} \simeq \frac{4}{1 + \left(2F_s/\tilde{\omega}_p\right)^2}$$

where the term $(1/\tilde{Q}_p).(\tilde{\omega}_p/2F_s)<<1$ has been approximated to zero. Unity loop gain is obtained when the sampling ratio is

$$(3.22) \ldots \qquad F_{su} = \pi\sqrt{3\ \tilde{f}_p}$$

in terms of the prewarped pole frequency $\tilde{f}_p$. In terms of the pole frequency f_p this gives

$$(3.23) \ldots \qquad F_{su} = 6.2\ f_p$$

For lower sampling ratios with $F_s<F_{su}$ the loop gain of the SC biquad is $L_g>1$, whereas for higher sampling ratios with $F_s>F_{su}$ the loop gain is $L_g<1$.

3.5.3 Capacitance loop spread

In this analysis of the capacitance loop spread we shall consider the condition for maximum signal handling capability, i.e. C/D=A/B yielding $L_m=1$. Later on, we shall also examine situations of non-maximum signal handling capability, i.e. C/D≠A/B, which is required for capacitance spread optimisation. For $L_m=1$, we have

$$(3.24) \ldots \qquad \frac{C}{D} = \frac{A}{B} = \sqrt{L_g} = 2\left[1 + \left(2F_s/\tilde{\omega}_p\right)^2\right]^{-1/2}$$

which will determine the maximum capacitance value among A, B, C and D. When $F_s=F_{su}$ the loop gain is unity, and we

make all capacitance values equal, i.e.

(3.25-a) ... $A = B = C = D \quad , \quad F_s = F_{su}$

$F_s < F_{su}$ yields $L_g > 1$, thus C=A will be the largest capacitance values, i.e.

(3.25-b) ... $A = C = B\sqrt{L_g} = D\sqrt{L_g} \quad , F_s < F_{su}$

For $F_s > F_{su}$, we have $L_g < 1$, and then B=D become the largest capacitance values, i.e.

(3.25-c) ... $\frac{A}{\sqrt{L_g}} = \frac{C}{\sqrt{L_g}} = B = D \quad , \quad F_s > F_{su}$

With respect to the damping capacitors E, F_1, and F_2, we obtain from the expressions in Table 3.4 the capacitance ratio

(3.26) ... $$\frac{C}{E} = \tilde{Q}_p \frac{\tilde{\omega}_p}{F_s}$$

for the SC biquad with E-damping, and the capacitance ratios

(3.27) ... $$\frac{B}{F1} = \frac{D}{F2} = \tilde{Q}_p \frac{\tilde{\omega}_p}{4F_s}\left[1 + \left(\frac{2F_s}{\omega_p}\right)^2\right]$$

for the SC biquad either with F_1-damping or with F_2-damping. The capacitance loop spread for the SC biquad with E-damping is obtained by entering the conditions

(3.25) into (3.26), which gives

$$(3.28\text{-a}) \quad \ldots \qquad CLS_E = \frac{C}{E} = \tilde{Q}_p \frac{\tilde{\omega}_p}{F_s} \quad , F_s < F_{su}$$

and

$$(3.28\text{-b}) \quad \ldots \qquad CLS_E = \frac{D}{E} = \tilde{Q}_p \frac{\tilde{\omega}_p}{2F_s} \left[1 + \left(\frac{2F_s}{\tilde{\omega}_p}\right)^2\right]^{1/2} \quad , F_s > F_{su}$$

Similarly, the capacitance loop spread for the SC biquad with F-damping, i.e. with respect either to F_1 or to F_2, is obtained from (3.25), and from (3.27). This leads to

$$(3.29\text{-a}) \quad \ldots \qquad CLS_F = \frac{A}{F1} = \frac{C}{F2} = \tilde{Q}_p \frac{\tilde{\omega}_p}{2F_s} \left[1 + \left(\frac{2F_s}{\tilde{\omega}_p}\right)^2\right]^{1/2} \quad , F_s < F_{su}$$

and to

$$(3.29\text{-b}) \quad \ldots \qquad CLS_F = \frac{B}{F_1} = \frac{D}{F_2} = \tilde{Q}_p \cdot \frac{\tilde{\omega}_p}{4F_s} \left[1 + \left(\frac{2F_s}{\tilde{\omega}_p}\right)^2\right] \quad , F_s > F_{su}$$

The above equations (3.28) and (3.29) can be expressed in terms of the pole frequency, f_p, and Q-factor, Q_p, of the SC biquad by using the warping equations (3.15) and (3.17), respectively.

A comparison between the capacitance loop spreads of an SC biquad with E-damping, and of an SC biquad with F-damping, both with maximum signal handling capability, is presented in Fig.3.16. Both types of damping produce approximately the same CLS when $F_s=F_{su}$. When $F_s>F_{su}$, the

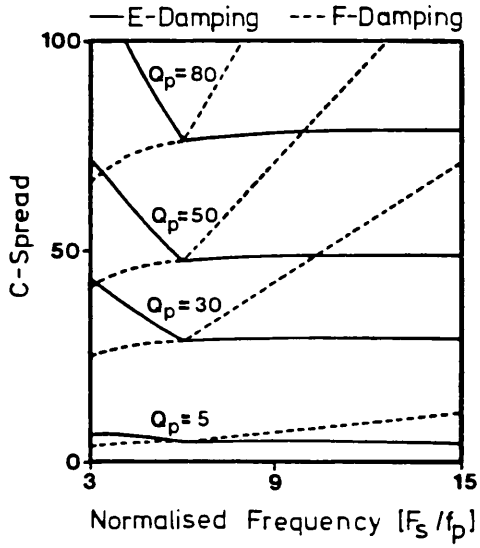


Fig.3.16: Evaluation of CLS of SC biquads with E-damping, and with F_1, F_2-damping, for $L_m=1$ (maximum signal handling capability)

CLS for an SC biquad with E-damping remains constantly equal to Q_p. This is much better than the CLS for an SC biquad with F-damping, which increases with the sampling ratio F_s/f_p. On the other hand, for $F_s<F_{su}$, the CLS for an SC biquad with F-damping is better than with E-damping. It is interesting to note that similar conclusions are obtained in [3.22], for the evaluation of the capacitance spread in the SC biquads given in [3.6], [3.15] and [3.23]. All these SC biquads can be derived from the general SC biquad building blocks presented in this Chapter [3.11].

In order to obtain the overall capacitance spread in the SC biquad we have to consider also the input capacitors G, H, I, and J. These capacitors enter the quadratic numerator function, and thus determine the type of response of the SC biquad. This will be explained in the next Section considering the example of an SC bandpass biquad.

3.6 DESIGN OF SC BANDPASS BIQUADS FOR MINIMUM CAPACITANCE SPREAD

3.6.1 Capacitance set spreads

In the general SC biquad with Type-B switching (Fig.3.10-a), we consider I=J, and G=H, such that the input switched-capacitors are replaced by two unswitched capacitors, respectively I and G, as illustrated in Fig.3.17-a [3.15]. This leads to the SC biquad shown in Fig.3.17-b, with E-damping (F_1=F_2=0), and output terminal

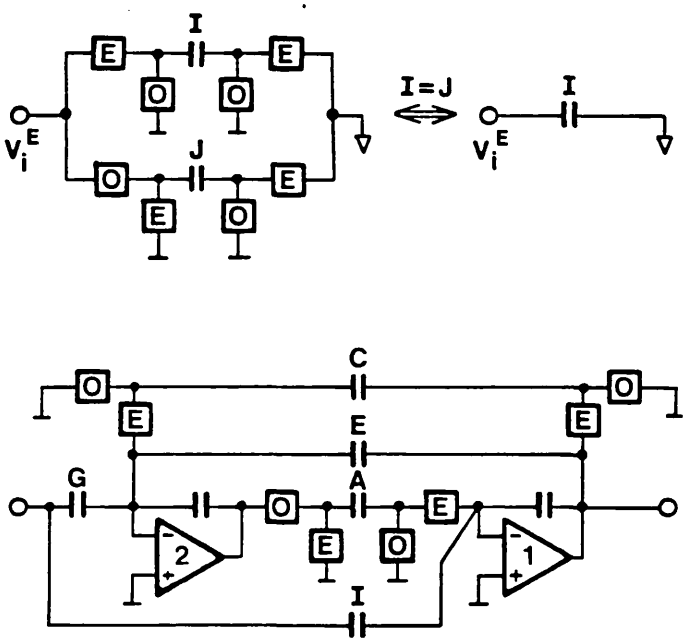


Fig.3.17: (a) SC transformation of two SC branches with equal capacitance values; (b) SC bandpass biquad with Type-B switching, and with E-damping

from OA1, which we shall consider in order to realise the quadratic numerator function of a bilinear SC bandpass biquad, i.e.

(3.30) ... $$N(Z) = K\left(1 - Z^{-2}\right)$$

From Table 3.5, we obtain the following conditions for the capacitance ratios

(3.31) ... $$\frac{D}{G} = \frac{1}{2}\frac{A}{B} \cdot \frac{B}{I} \quad ; G = H, \quad I = J$$

and the following design equation

(3.32-a) ... $$\frac{B}{I} = \frac{1}{H_o}\left[1 + \tilde{Q}_p\left(\frac{2F_s}{\tilde{\omega}_p}\right) + \tilde{Q}_p\left(\frac{\tilde{\omega}_p}{2F_s}\right)\right]$$

which we approximate to

(3.32-b) ... $$\frac{B}{I} = \frac{1}{H_o}\,\tilde{Q}_p\,\frac{\tilde{\omega}_p}{2F_s}\left[1 + \left(\frac{2F_s}{\tilde{\omega}_p}\right)^2\right]$$

where H_o is the desired midband gain of the SC biquad. In the following analysis we shall make H_o=1; later on, the desired midband gain H_o will be restored by a simple operation of contour scaling around the input node.

In the SC biquad of Fig.3.17, ICS-1 contains the capacitors A, B and I. The minimum capacitance value is I whereas the maximum capacitance value is either A or B, depending on the sampling ratio F_s/f_p. From (3.32-b) and from the conditions in (3.25), the capacitance spread of ICS-1 is determined by

$$(3.33\text{-a}) \ldots \qquad \text{CSS-1} = \frac{A}{I} \simeq \tilde{Q}_p \frac{\tilde{\omega}_p}{F_s} \left[1 + \left(\frac{2F_s}{\tilde{\omega}_p}\right)^2\right]^{1/2} \quad , F_s < F_{su}$$

and by

$$(3.33\text{-b}) \ldots \qquad \text{CSS-1} = \frac{B}{I} = \tilde{Q}_p \frac{\tilde{\omega}_p}{2F_s} \left[1 + \left(\frac{2F_s}{\tilde{\omega}_p}\right)^2\right] \quad , F_s > F_{su}$$

For high sampling ratios with $F_s > F_{su}$, CSS-1=B/I depends only on the Q-factor Q_p of the SC biquad. But, for low sampling ratios with $F_s < F_{su}$, CSS-1=A/I depends additionally on the loop gain L_g of the SC biquad.

Depending also on the sampling ratio F_s/f_p, the maximum capacitance value in ICS-2, for the SC biquad in Fig.3.17, can be either C or D, and the minimum capacitance value can be either E or G. By using a similar procedure as above, we obtain the following expressions for the capacitance spread of ICS-2

$$(3.34\text{-a}) \ldots \qquad \text{CSS-2} = \frac{C}{G} = \frac{C}{E} = \tilde{Q}_p \frac{\tilde{\omega}_p}{2F_s} \quad , F_s < F_{su}$$

and

$$(3.34\text{-b}) \ldots \qquad \text{CSS-2} = \frac{D}{G} = \frac{D}{E} = \tilde{Q}_p \frac{\tilde{\omega}_p}{2F_s} \left[1 + \left(\frac{2F_s}{\tilde{\omega}_p}\right)^2\right]^{1/2} \quad , F_s > F_{su}$$

Unlike CSS-1, we can see in the above expressions that CSS-2 does not depend on the loop gain of the SC biquad. For low sampling ratios with $F_s < F_{su}$, C is the largest capacitance value in ICS-2, and, hence, C/E and C/G depend

only on the Q-factor Q_p. In the same way, for high sampling ratios with $F_s > F_{su}$ D becomes the largest capacitance value in ICS-2, which also means that D/G and D/E depend only on the Q-factor Q_p of the SC biquad.

3.6.2 Optimum switching frequency

For an example with $Q_p=30$, Fig.3.18 shows the variation of CSS-1, obtained from (3.33), and of CSS-2, obtained from (3.34), as a function of the sampling ratio F_s/f_p. As we saw above, CSS-2, as well as the portion of

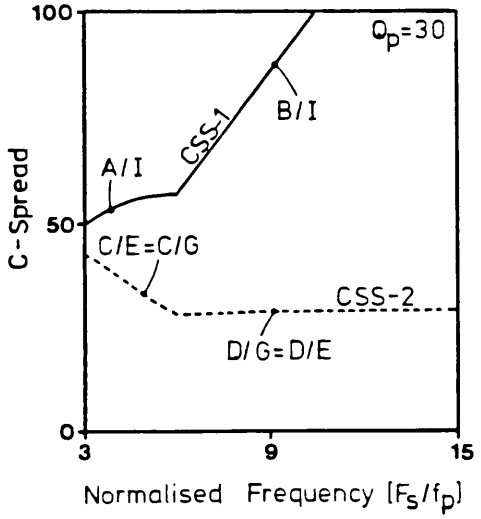


Fig.3.18: Overall capacitance spread in the SC bandpass biquad with $L_m=1$

CSS-1 for $F_s > F_{su}$ (B/I), are characteristic of the biquadratic transfer function. But, for $F_s < F_{su}$, the capacitance ratio B/I has been multiplied by the loop gain factor $\sqrt{L_g}$, in order to satisfy the condition C/D=A/B for maximum signal handling capability. This produced a larger value, A/I, for the capacitance spread. In order to obtain the original ratio B/I also when $F_s < F_{su}$, we have to scale the output voltage of OA2 by a factor $1/\sqrt{L_g}$, making A=B,

the result of which is illustrated in Fig.3.19. Therefore, the absolute minimum capacitance spread of the SC biquad is obtained when CSS-1=CSS-2 which, from (3.33-b), and from (3.34-a), leads to the optimum switching frequency

$$(3.35) \ldots \qquad F_{s_{opt}} = \frac{\tilde{\omega}_p}{2}$$

In terms of the pole frequency of the SC biquad this gives

$$(3.36) \ldots \qquad F_{s_{opt}} = 4f_p$$

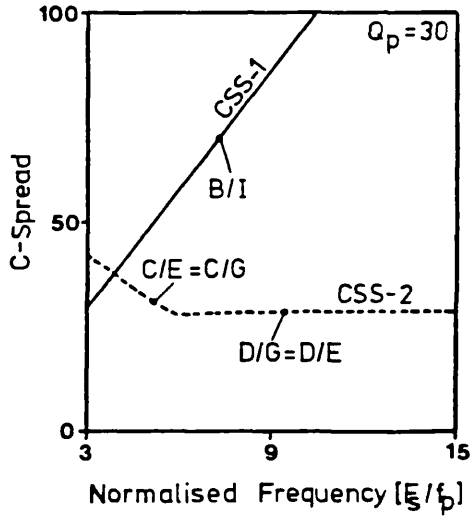
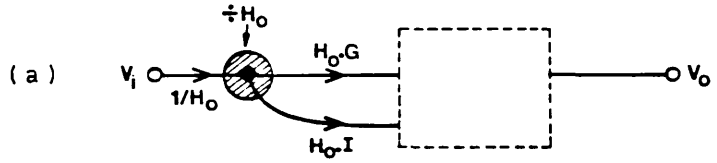


Fig.3.19: SC bandpass biquad with absolute minimum capacitance spread, for CSS-1=CSS-2

The optimum switching frequency given in (3.35) implies, from (3.21), the loop gain $L_g=(C/D).(A/B)=2$; since A=B, the resulting voltage magnification in the SC biquad, equation (3.20), becomes $L_m=\sqrt{2}$. As a result, the signal handling capability of the SC biquad will be reduced by 3dB, in order to satisfy the condition for absolute minimum capacitance spread.

3.6.2 Optimum switching frequency versus gain

In order to restore the midband gain H_o we apply a contour scaling around the input node of the SC biquad yielding the capacitance values $G.H_o$ and $I.H_o$, as illustrated in Fig.3.20-a. This operation will affect the capacitance spread in the SC biquad as follows. For $H_o<1$, we can see in Fig.3.19 that both CSS-2 and CSS-1 increase, and thus keeping the optimum switching frequency $F_{s_{opt}}=4f_p$ approximately constant, as shown in Fig.3.20-b. Increasing of the midband gain H_o, i.e. $H_o>1$, does not modify CSS-2 because the capacitance ratios C/E and D/E are not affected



Before scaling : $V_o=1.V_i$
After scaling : $V_o=H_o.V_i$

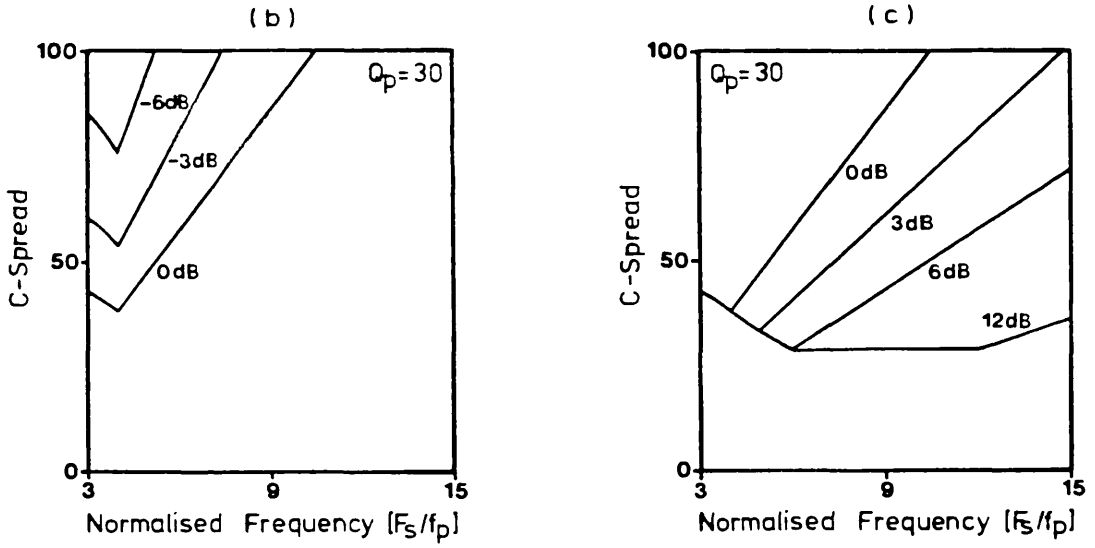


Fig.3.20: Optimum switching frequency versus gain. (a) Input scaling for gain H_o; (b) $H_o<1$; (c) $H_o>1$

by the scaling operation. On the contrary, CSS-1 decreases when H_o increases. Overall, for $H_o>1$, there will be a reduction of the absolute minimum capacitance spread, as well as an increase of the optimum switching frequency, as shown in Fig.3.20-c.

In general, the operation of gain scaling can be employed in order to reduce the capacitance spread in an SC biquad, either with or without the optimum switching frequency, whenever the capacitance values of the input capacitors G, H, I, and J, are smaller than the capacitance values of the damping capacitors E, F_1, and F_2. Such mechanism of capacitance spread reduction is explained with reference to the example in Fig.3.21. In the design of an

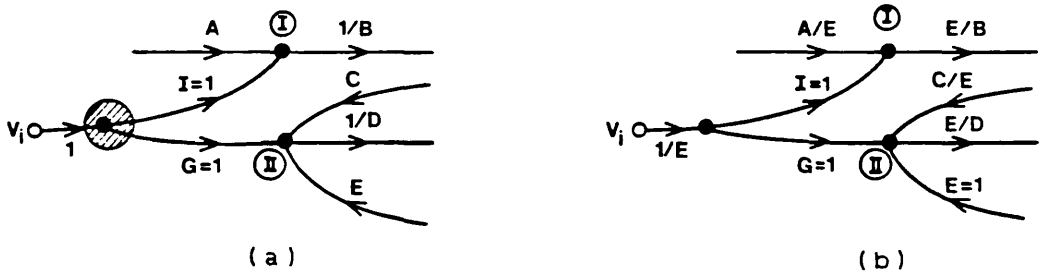


Fig.3.21: Gain scaling for capacitance spread reduction

SC biquad for a given sampling ratio, we scale the capacitance values of ICS-1, and ICS-2, in order to obtain capacitance values G=1 and I=1, respectively, as shown in Fig.3.21-a. The minimum capacitance spread which depends only on the characteristics of the quadratic denominator function will be obtained when the minimum capacitance value of the SC biquad corresponds to the damping capacitor

E. In order to achieve this, we apply a gain scaling factor E such that the input capacitors and the damping capacitor have the same capacitance value. This produces a reduction by a factor E of the capacitance spreads of ICS-1 and ICS-2, as shown in Fig.3.21-b, and thus a reduction of the overall capacitance spread of the SC biquad.

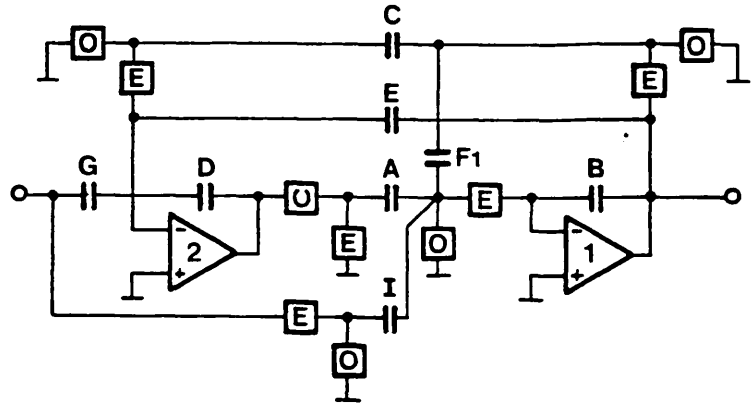
Designing for minimum capacitance spread, as we did before, reduces the total capacitor area of the SC biquad although it does not necessarily yield an absolute minimum capacitor area. This aspect must be considered separately when we compare various possible design solutions of an SC biquad, as we illustrate in the examples given in the next Section.

3.7 DESIGN EXAMPLES

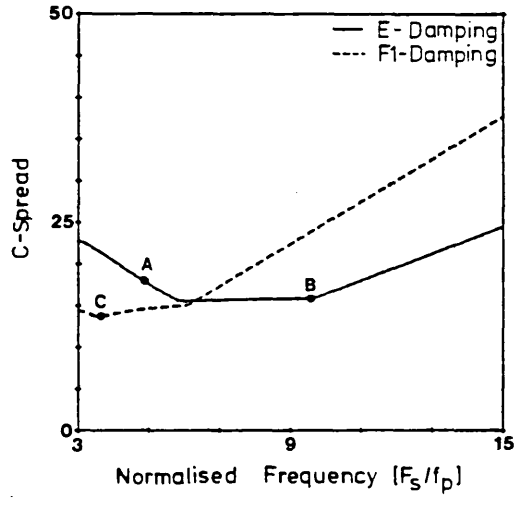
The design example illustrated in Fig.3.22 refers to an SC bandpass biquad with the specifications given in Table 3.8 [3.15]. The SC biquad in Fig.3.22-a results from the general SC biquad building block in Fig.3.10-a, with F2=0, J=0, and G=H. Following the procedure described above for analysis of the overall capacitance spread, we arrive at the curves plotted in Fig.3.22-b, both for the SC biquad

Q-factor	16
Centre frequency	1633Hz
Mid-band gain	10dB
Voltage magnification	0dB

Table 3.8: Design specifications for a bilinear SC bandpass biquad

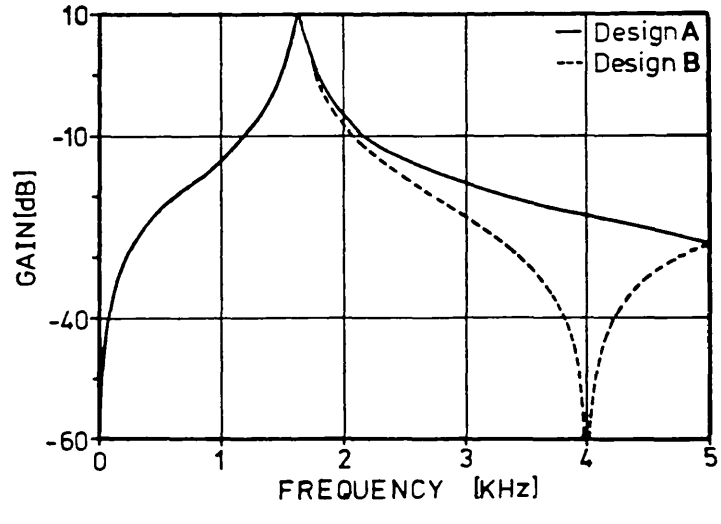


(a)



		Design A	Design B
ICS-1	A	9.62922	10.05080
	B	8.20335	16.09541
	F1	———	———
	I	1	1
ICS-2	C	17.85130	9.91316
	D	15.22514	15.83180
	E	1	1
	G	1.58114	1.58114
Total Capacitance		54.490	55.532

(b)



(c)

Fig.3.22: (a) SC bandpass biquad; (b) Overall capacitance spread, and normalised capacitance values for design solutions A, and B; (c) Computer simulated amplitude response

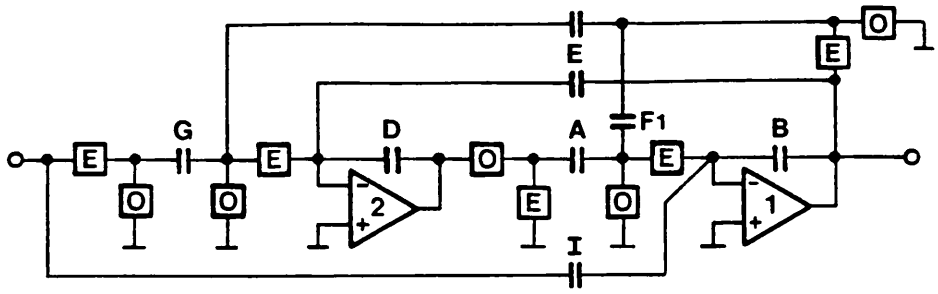
with E-damping (full line), and for the SC biquad with F_1-damping (broken line). Solution C, with F_1-damping, and sampling ratio $F_s/f_p \tilde{=} 3.5$, yields the minimum capacitance spread ($\tilde{=}14$). The capacitance spread is also low in both of the solutions with E-damping, i.e. $\tilde{=}18$ in solution A, and $\tilde{=}16$ in solution B. By adopting solution B with a higher sampling ratio $F_s/f_p \tilde{=} 10$, which only slightly increases the capacitor area in the SC biquad, we have the advantage of reducing the requirements of the AAF and AIF in a complete SC filter system. On the other hand, adoption of a higher sampling ratio reduces the selectivity of the upper stopband due to a smaller effect of the bilinear transformation. This can be seen in Fig.3.22-c, showing the amplitude responses corresponding to solutions A and B.

The example illustrated in Fig.3.23 refers to an SC lowpass notch biquad with the design specifications given in Table 3.9.

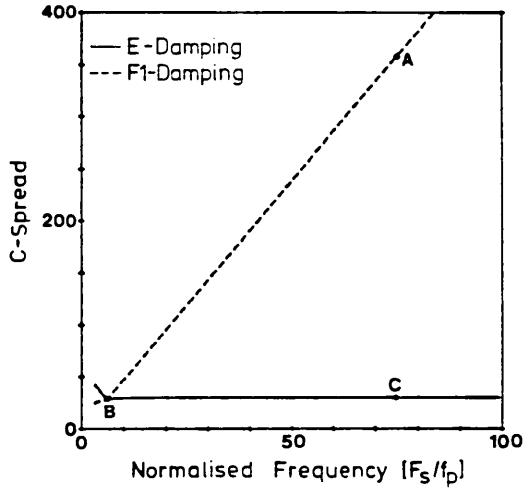
Qp-factor	30
Pole-frequency	1700Hz
Notch-frequency	1800Hz
Gain @ DC	0dB
Voltage magnification	0dB

Table 3.9: Design specifications for a bilinear SC lowpass notch biquad

The SC biquad in Fig.3.23-a results from the general SC biquad building block in Fig.3.10-a, with F2=0, H=0 and I=J. Three design solutions are compared on the basis of the curves shown in Fig.3.23-b, which represent the overall

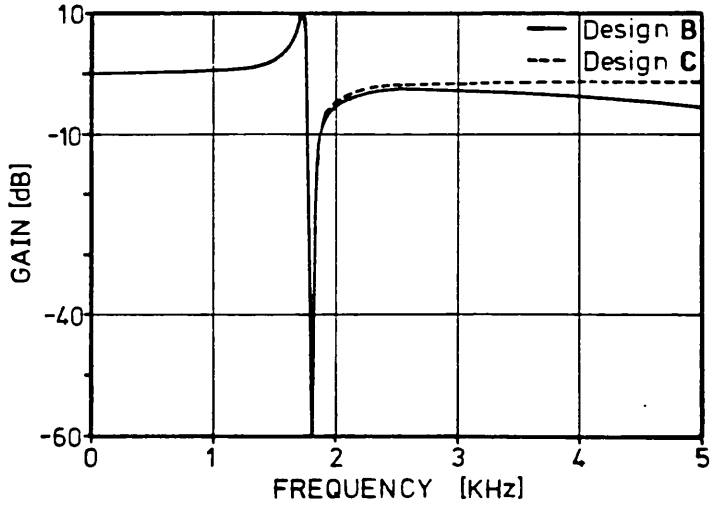


(a)



		Design B	Design C
ICS-1	A	26.39533	1
	B	28.14644	11.99524
	F1	1	———
	I	25.84198	10.68535
ICS-2	C	1.00884	2.50200
	D	1	30.01214
	E	———	1
	G	1.00884	2.50200
Total Capacitance		86.401	59.697

(b)



(c)

Fig.3.23: (a) SC lowpass notch biquad; (b) Overall capacitance spread, and normalised capacitance values for design solutions B, and C; (c) Computer simulated amplitude response

capacitance spread of the SC biquad. Solution A, with F_1-damping, and sampling ratio $F_s/f_p \simeq 75$, is rejected because of the enormous capacitance spread $\simeq 350$. Designing the SC biquad also with F_1-damping, but with the optimum sampling ratio $F_s/f_p \simeq 6$, solution B, gives the minimum capacitance spread $\simeq 28$. For a smaller capacitor area, we could adopt instead solution C, with E-damping. This solution has the additional advantage of much higher sampling ratio, and thus simpler requirements for the AAF and AIF. As we can see in Fig.3.23-c, the adoption of a higher sampling ratio also reduces the effect of the sample and hold attenuation, compared with solution B with lower sampling ratio.

3.8 SUMMARY

In the first part of this Chapter, we developed general SC biquad building blocks based on the Two Integrator Loop structure, which are fully insensitive to grounded parasitic capacitances, and have low sensitivity of the pole frequency and pole Q-factor with respect to capacitance ratio errors. Design formulae were presented for discrete-time transfer functions derived from continuous-time transfer functions using the bilinear transformation.

The second part of this Chapter was concerned with the analysis of capacitance ratios in SC biquads derived from the general structures. By considering the example of an SC bandpass biquad, we showed that the overall capacitance spread is determined by two types of capacitance ratios,

namely those which depend solely on the biquadratic transfer function, and those which, in addition, relate to the signal handling capability of the SC biquad. For applications with low Q-factors, it is appropriate to design the SC biquad with maximum signal handling capability, at the expense of increasing the overall capacitance spread. On the other hand, for highly selective filtering applications, it is vital to minimise the capacitance spread of the SC biquad, even implying some reduction of the signal handling capability. This is achieved by designing the SC biquad using an optimum value of the switching frequency, which leads to an absolute minimum capacitance spread, and, as a result, maximises the accuracy of the capacitance ratios, and reduces the total capacitor area.

Further aspects of the design of SC biquads, which we illustrated by means of numerical examples, are concerned with the total capacitor area required for implementation as well as the range of optimum, or nearly optimum, switching frequency which allows for the best compromise between the complexity of the AAF and AIF in an SC filter system and, for example, the selectivity of the amplitude response of the SC biquad.

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CHAPTER 4

SC DECIMATOR AND INTERPOLATOR CIRCUITS FOR APPROXIMATIONS BASED ON OPTIMUM FIR TRANSFER FUNCTIONS

4.1 INTRODUCTION

As we mentioned in Chapter 2, SC decimators and interpolators can have IIR or FIR transfer functions, or even consist of a combination of circuits having IIR and FIR transfer functions, depending on the anti-aliasing and anti-imaging system specifications. IIR SC decimators and interpolators are more suitable for wideband stopband approximations, and are implemented using the general SC biquad building blocks derived in the previous Chapter. This Chapter deals with SC decimator and interpolator circuits which are suitable for multinotch stopband approximations based on the optimum FIR transfer functions introduced in Section 2.5.

FIR transfer functions can be realised using recursive and non-recursive structures. The use of SC biquads for realising FIR transfer functions is considered in the first part of this Chapter, in Section 4.2. Based on our experimental work, we show that the recursive nature of the circuits produces errors of the impulse response coefficients, which are rather dependent on the non-ideal characteristics of the OA's, and which affect the exact placement of the notch frequencies. Such errors become more important when the switching frequency is high which, as a result, limits the operating speed of this type of SC circuits.

The main purpose of this Chapter is to develop non-recursive polyphase structures for SC decimators and interpolators, which are typically used in multirate

digital signal processing. The resulting SC decimator and interpolator circuits, whose development is described in the second part of this Chapter, from Section 4.3 to Section 4.5, are found to be very attractive from the points of view of low capacitance spread, high operating speed, and, also, low power consumption since they employ few OA's. In Section 4.3, we briefly describe the general principles of the polyphase structures and show how such structures are derived from a given impulse response of the decimator and interpolator. In Section 4.4, we consider the basic SC building blocks for implementation and also discuss various arrangements of the switch phasing which allow multiplexing of the input SC branches. Examples of the realisation of both single-stage and cascade polyphase SC decimators and interpolators are presented in Section 4.5.

In the third part of this Chapter, corresponding to Section 4.6, we describe an alternative type of SC decimator and interpolator circuit in which we combine IIR SC biquads together with FIR SC polyphase structures, as a means of obtaining an optimum multinotch amplitude response with increased selectivity. A summary of the Chapter is presented in Section 4.7.

4.2 SC RECURSIVE QUADRATIC STRUCTURES

4.2.1 Design example

An SC biquad can be employed for realising a quadratic FIR transfer function, provided the quadratic denominator of the transfer function reduces to unity. A simple solution consists of making all the capacitors of the capacitor loop set equal to unity, i.e. A=B=C=D=E=1, as shown in the general SC biquad in Fig.4.1 with Type-A switching. From the general expressions given in the

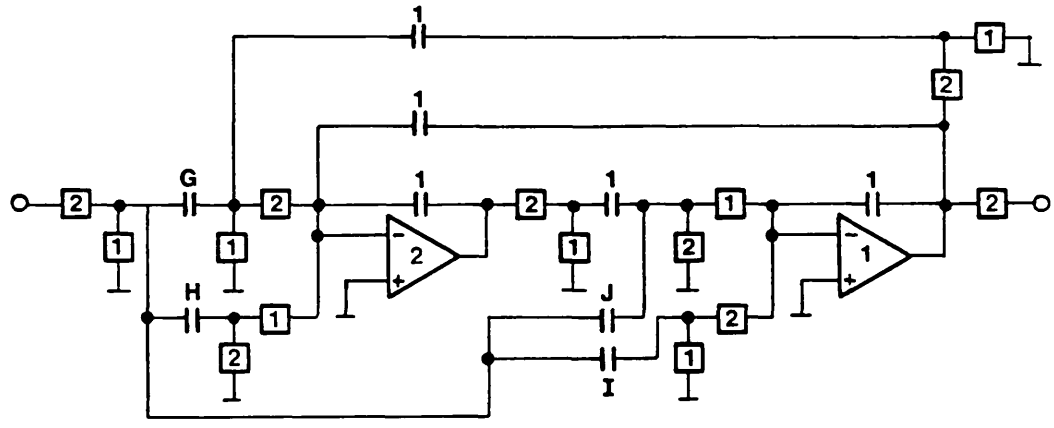


Fig.4.1: FIR SC biquad with Type-A switching

previous Chapter (Table 3.2 and Table 3.3 in Section 3.3), the discrete-time transfer function of the FIR SC biquad is given by

$$H(Z) = I + (G - I - J)Z^{-1} + (J - H)Z^{-2} \quad \text{(4.1) ...}$$

yielding the design equations

(4.2) ... $I = h_o$; $J - H = h_2$; $G + H = h_o + h_1 + h_2$

for the input capacitors G, H, I and J.

We consider the example of an SC bandpass filter at midband frequency f_o=20KHz and switching frequency F_s=80KHz, where it is required to increase the sampling rate to $4F_s$=320KHz. Therefore, for this application, we have to design an SC interpolator with a factor L=4 for sampling rate increase, which produces notch frequencies at $F_s \pm f_o$, $2F_s \pm f_o$, and $3F_s \pm f_o$. We consider the cascade of two FIR SC biquads shown in Fig.4.2. The first SC biquad with switching frequency $2F_s$=160KHz produces the notch frequencies at $F_s \pm f_o$, and their repetitions at $3F_s \pm f_o$, while the second SC biquad with switching frequency

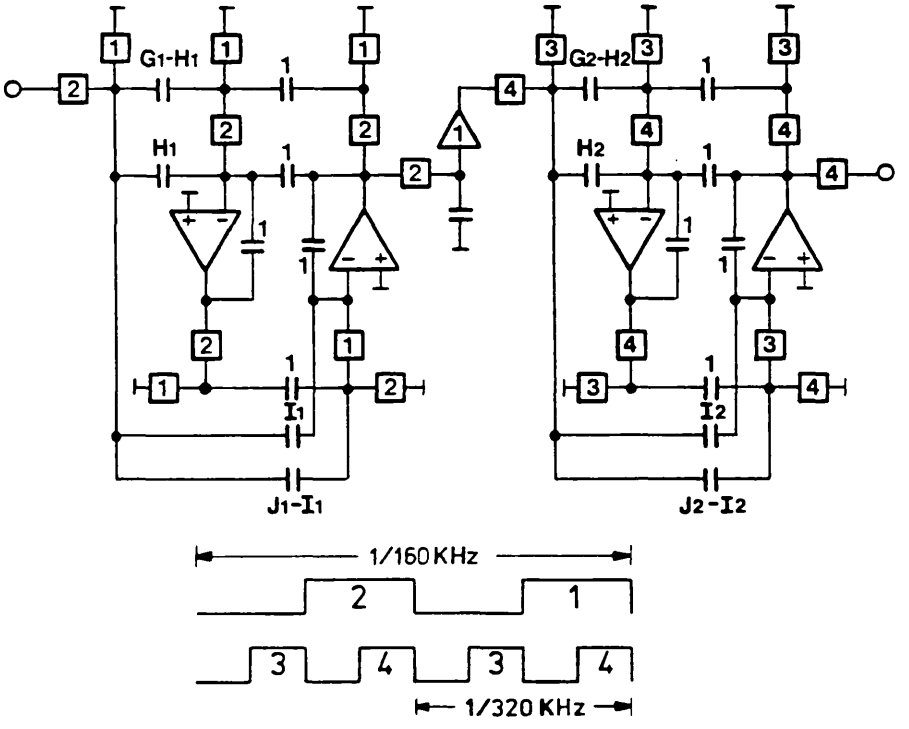


Fig.4.2: Cascade SC interpolator L=4 with FIR SC biquads

$4F_s$=320KHz yields the notch frequencies at $2F_s \pm f_o$. The optimised FIR coefficients, which are derived using the technique described in Section 2.5, and the resulting capacitance values obtained from (4.2) are given in Table 4.1. The circuit in Fig.4.2 was constructed as a discrete

1st STAGE: $F_s \rightarrow 2F_s$		2nd STAGE: $2F_s \rightarrow 4F_s$	
COEFFICIENTS	CAPACITANCES	COEFFICIENTS	CAPACITANCES
h_o=0.3536	G_1-H_1=1.2071	h_o=0.2706	G_2-H_2=1.0412
	H_1=1		H_2=1
h_1=0.5		h_1=0.5	
	I_1=0.3536		I_2=0.2706
h_2=0.3536	J_1-I_1=1	h_2=0.2706	J_2-I_2=1

Table 4.1: Optimised coefficients and capacitance values for an SC biquad realisation of an interpolator with L=4

component model, using CMOS 4016 analogue switches and BiMOS 3140 OA's. The measured amplitude response of this SC interpolator is presented in Fig.4.3. At lower frequencies (<50KHz), and in the vicinity of the notch frequencies at $F_s \pm f_o$ (60KHz and 100KHz), and at $3F_s \pm f_o$ (220KHz and 260KHz), the measured amplitude response is fairly close to the computed (ideal) response. On the contrary, there is a visible deterioration of the amplitude response at the notch frequencies $2F_s \pm f_o$ (140KHz and 180KHz), which are produced by the SC biquad with higher switching frequency ($4F_s$=320KHz). This is due to different errors affecting the

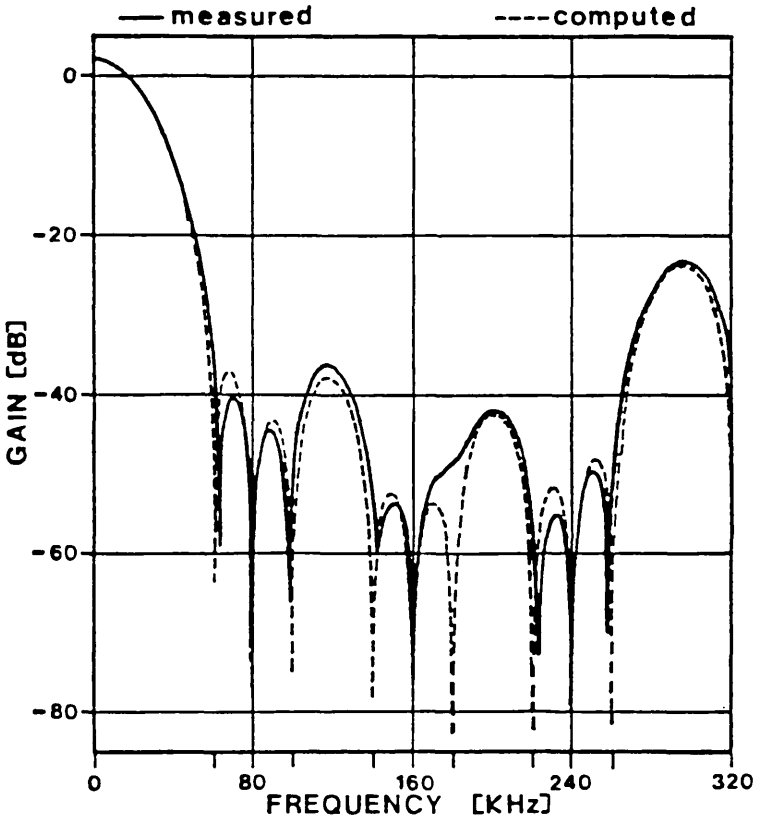


Fig.4.3: Measured baseband response of the SC interpolator with L=4

terms of the FIR transfer function, which, in turn, we shall explain below as resulting from the recursive nature of the circuits.

4.2.2 Speed limitation

The above FIR SC biquads have very low capacitance ratios, and thus high capacitance ratio accuracy. The errors which affect the terms of the FIR transfer function result primarily from the finite gain bandwidth product of the OA's, the effect of which increases as the switching frequency increases [4.4]-[4.6]. Looking at the circuit in

Fig.4.1, and the corresponding discrete-time transfer function (4.1), we can see that the term $I.Z^0$ is the least affected by such amplifier imperfections because the SC branch containing capacitor I links the input terminal directly to the virtual ground of the OA (OA1) whose output terminal is the output terminal of the circuit; the term $(G-I-J).Z^{-1}$ is more affected because it has an additional path via OA2, i.e. $(G.Z^{-1})$; the term $(J-H).Z^{-2}$ is the most affected because it has a further path via the entire loop of the SC biquad, i.e. $(J.Z^{-2})$. This recursive nature of the SC biquad yields different errors for the different terms of the FIR transfer function which, as we shall see in the Appendix, implies poorer accuracy of the multinotch amplitude response. This becomes more critical at high switching frequencies because the OA's are more affected. In order to overcome this problem, we develop an alternative non-recursive type of structures for FIR SC decimators and interpolators, which employ parallel processing and only one OA per transfer function. As we shall show, these structures are much more tolerant to the non-ideal characteristics of the OA's.

4.3. NON-RECURSIVE POLYPHASE STRUCTURES FOR DECIMATION AND INTERPOLATION

4.3.1 Polyphase structure for decimation

As we saw in Chapter 2, the operation of decimation consists of reducing the sampling rate from a high value MF_s (M is an integer >1) to a lower value F_s, and is

implemented by a decimator circuit symbolically represented as in Fig.4.4-a. The conceptual operation of the decimator in the time-domain is illustrated in Fig.4.4-b. The prototype filter at the heart of the decimator receives

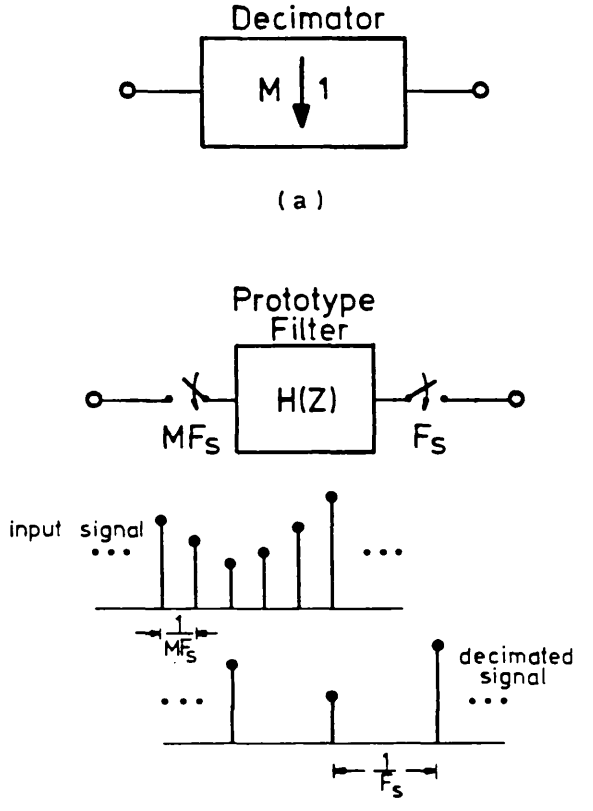


Fig.4.4: Sampling rate reduction by a factor M. (a) Symbolical representation of the decimator; (b) Illustration of decimation in time

input samples at the higher rate MF_s, weights and combines those samples, and then produces output samples at lower rate F_s. The prototype filter is a linear time-invariant filter with discrete-time transfer function H(Z) which, for FIR decimators, has the general form

$$H(Z) = \sum_{n=0}^{N-1} h_n Z^{-n} \qquad (4.3) \ldots$$

where the unit delay period is $1/MF_s$. The length N, and the coefficients h_n of the prototype filter can be optimised using the procedure described in Section 2.5, whereby the notches of the frequency response are placed exactly at the centre of the unwanted alias components associated with the output signal at lower rate F_s.

An analogue sampled-data decimator can be implemented using the polyphase structure shown in Fig.4.5 [4.1]-[4.3], in which the prototype filter is decomposed into a set of M

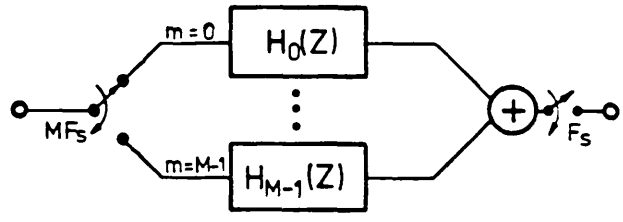


Fig.4.5: Polyphase structure for decimation

sub-filters that operate at lower rate F_s. The discrete-time transfer function $H_m(Z)$ of each polyphase filter (m=0,1,...,M-1) is given by

$$H_m(Z) = \sum_{i=0}^{I_m} h_{m+iM} Z^{-iM} \qquad (4.4)$$

where the coefficients h_{m+iM} of the polyphase filters are equal to the coefficients h_n in (4.3) with n=m+iM; the length I_m of each polyphase filter m is such that (I_m-1) is the integer part of (N-1-m)/M. This process of polyphase decomposition of the prototype filter is illustrated with the simple example given in Fig.4.6, for a factor M=2 of

sampling rate reduction. The original impulse response of Fig.4.6-a is decomposed into two simpler impulse responses shown in Fig.4.6-b, yielding the polyphase structure of Fig.4.6-c. The delay between equivalent samples of each sub-filter corresponds, in the frequency domain, to a phase shift and hence the sub-filters are designated polyphase filters.

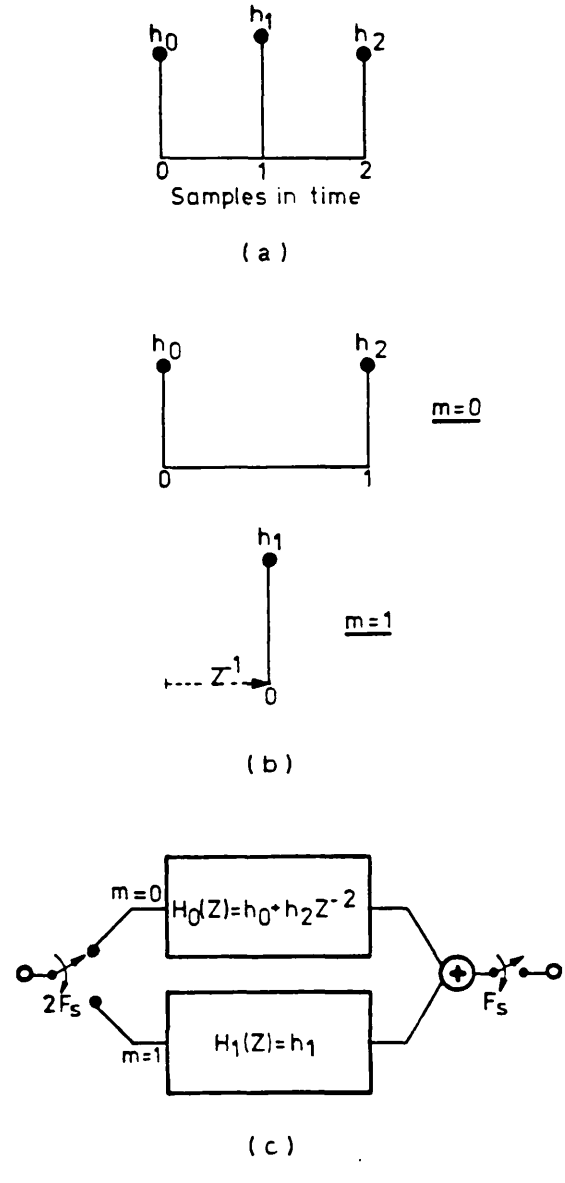


Fig.4.6: Example of an FIR polyphase decimator M=2. (a) Prototype filter; (b) Decomposed polyphase filters; (c) Polyphase structure

4.3.2 Polyphase structure for interpolation

The operation of increasing the sampling rate from a low value F_s to a higher value LF_s (L is an integer >1) is known as interpolation and complements the operation of decimation described above. An interpolator circuit is symbolically represented as in Fig.4.7-a. The interpolation of sampled and held signals, which occur in SC circuits, is illustrated in Fig.4.7-b. Every period $1/F_s$ of the input signal, the prototype filter produces a sequence of L samples, each of which are determined by its discrete-time transfer function H(Z), and which are also held for a period $1/LF_s$. The frequency response of the prototype filter is also important because it should eliminate the image components associated with the input signal at lower

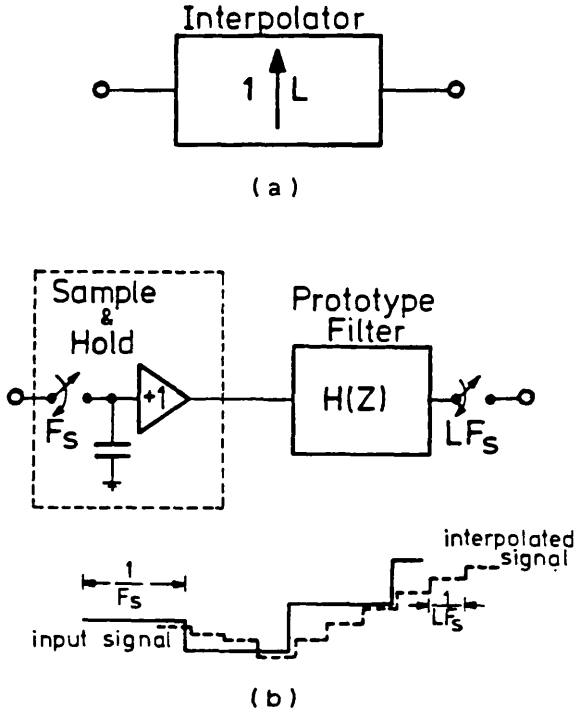


Fig.4.7: Sampling rate increase by a factor L. (a) Symbolical representation of the interpolator; (b) Interpolation of a sampled and held signal

rate. In SC bandpass filter systems, the decimators and interpolators may have the same factor of sampling rate alteration, i.e. M=L, and their original prototype filters may also have the same discrete-time transfer function H(Z). But because the operation of interpolation refers to sampled and held signals, the original prototype filter for interpolation can be modified according to

$$(4.5) \quad \ldots \qquad H'(Z) = H(Z) \cdot \sum_{l=0}^{L-1} Z^{-1} \qquad (4.5)$$

where the unit delay period is $1/LF_s$.

An analogue sampled-data interpolator with modified prototype filter can be implemented using the polyphase structure of Fig.4.8. Each one of the L polyphase filters at lower rate F_s produce one output sample determined by their transfer functions $H_l(Z)$. The output signal of the interpolator is obtained by resampling the outputs of the polyphase filters at higher rate LF_s. The impulse responses of the polyphase filters are derived from the impulse response of the modified prototype filter using a decomposition process similar to that for the decimator. A simple example of this process for L=2 is given in Fig.4.9.

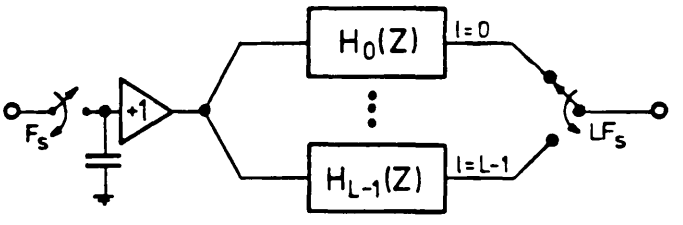
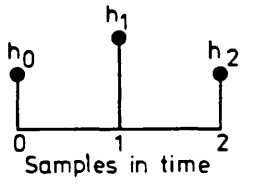
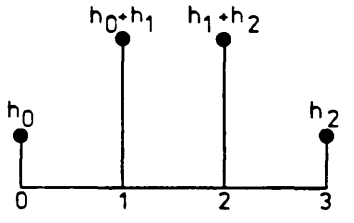


Fig.4.8: Polyphase structure for interpolation

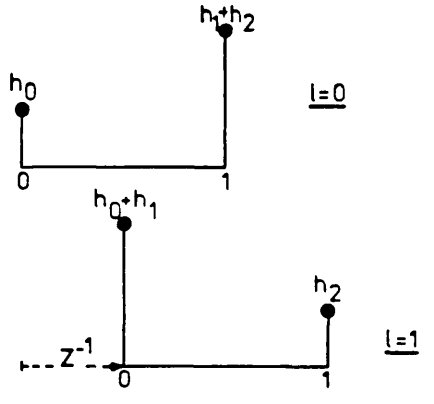
The prototype filter with the original impulse response of Fig.4.9-a is modified according to (4.5) yielding the impulse response shown in Fig.4.9-b. Then, this is decomposed into L=2 simpler impulse responses represented in Fig.4.9-c which yields the polyphase structure of Fig.4.9-d.



(a)

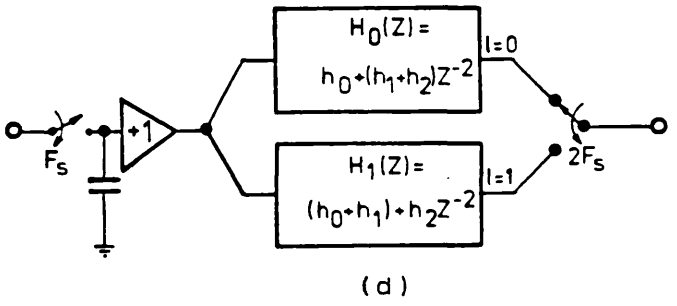


(b)



(c)

Fig.4.9: Example of an FIR interpolator L=2. (a) Original and (b) modified prototype filters; (c) Decomposed polyphase filters;



(d)

Fig.4.9 (continued): (d) Polyphase structure for FIR polyphase interpolator L=2

4.4. SC BUILDING BLOCKS FOR POLYPHASE STRUCTURES

4.4.1 General Structures

The conventional form of realising an FIR transfer function is by means of the transversal tapped delay line shown in Fig.4.10, in which the delays giving the required powers of Z are obtained by means of a form of serial processing. This structure can be implemented in SC form either using OA's [4.7] or using unity gain buffers [4.8], but none of these types of circuits are suitable for high-quality SC decimators and interpolators, on account of their sensitivity to parasitic capacitances and to the non-ideal characteristics of the active elements.

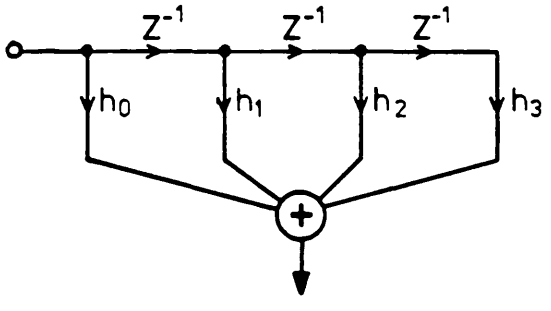


Fig.4.10: Non-recursive transversal structure

Additionally, there is the problem of serial processing which renders such nonideal characteristics even more severe because of the propagation of errors throughout the delay line.

The practical limitations mentioned above for the conventional SC tapped delay line, are overcome by the adoption of the alternative direct-form structure of Fig.4.11 [4.9], using parallel processing. An additional

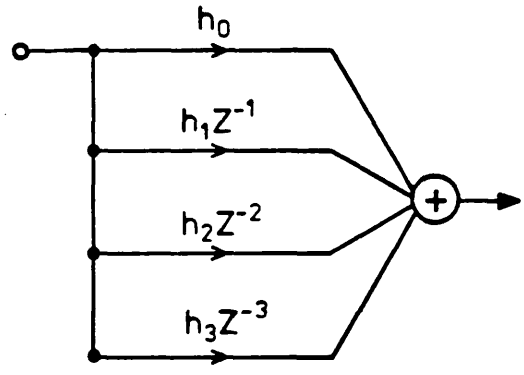
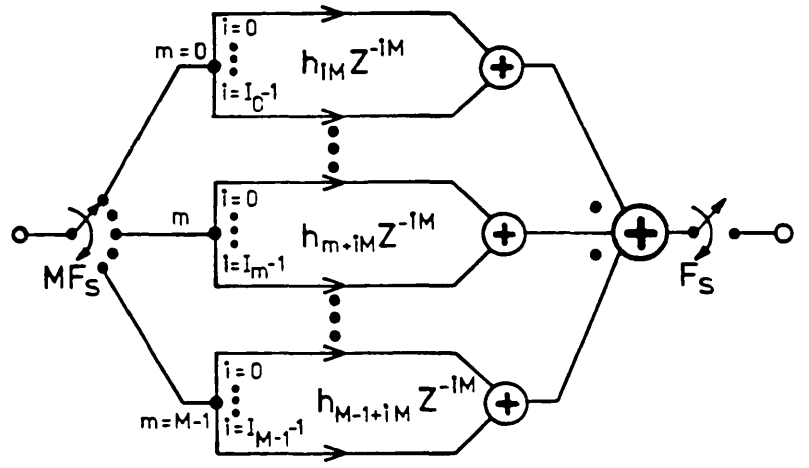
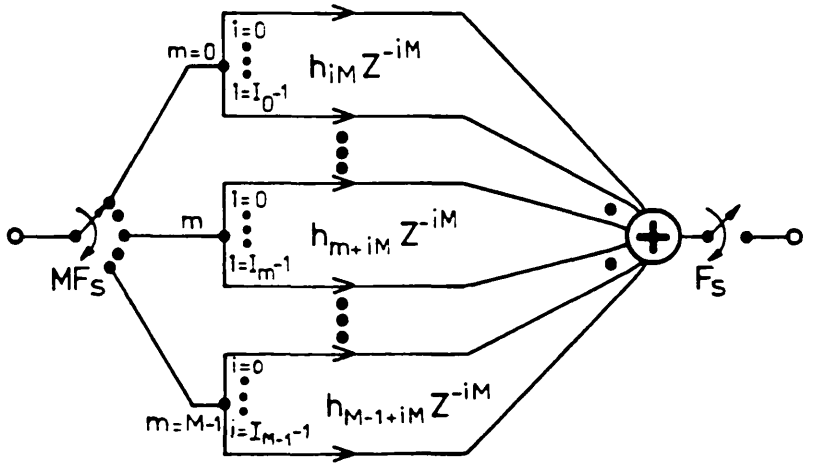


Fig.4.11: Modified direct-form non-recursive structure

advantage of this structure is that each term of the FIR transfer function can be implemented separately with passive SC elements employing only analogue switches and capacitors. Not only this improves their accuracy, thus leading to higher precision of the multinotch amplitude response, but also increases the speed of operation. For the SC decimator, this direct-form structure for the individual polyphase filters produces to the general polyphase structure shown in Fig.4.12-a, using M+1 accumulators. However, since the outputs of the polyphase filters and the output of the decimator are at the same



(a)



(b)

Fig.4.12: Polyphase decimator structures with direct-form polyphase filters

lower rate F_s, only one accumulator is needed, as shown in Fig.4.12-b. For the SC interpolator, the resulting general polyphase structure with direct-form polyphase filters is shown in Fig.4.13-a. This structure needs L accumulators at lower rate F_s, the outputs of which are resampled at higher rate LF_s. However, since the outputs of the polyphase filters only matter during the periods of time when they are connected to the output of the interpolator,

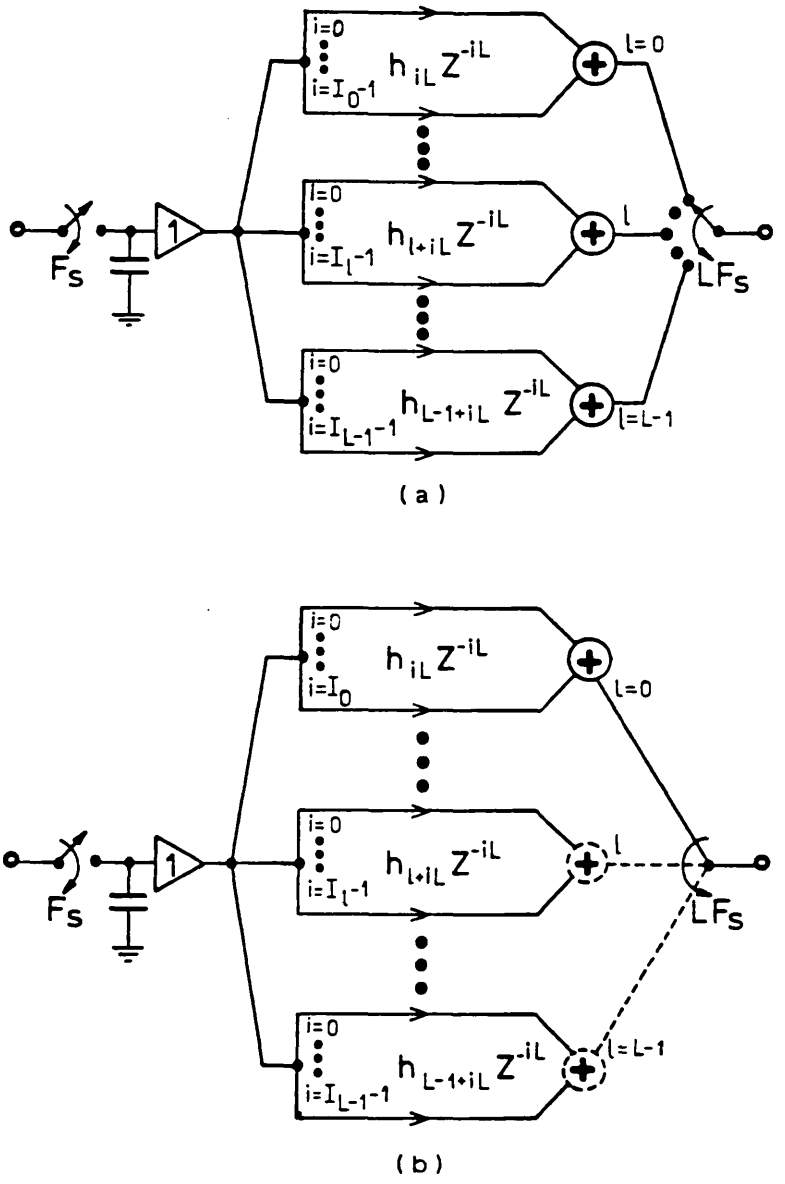


Fig.4.13: Polyphase interpolator structures with direct-form polyphase filters. (a) L accumulators at lower rate F_s; (b) 1 time-shared accumulator at higher rate LF_s

it is possible to utilise only one time-shared accumulator, as shown in Fig.4.13-b.

The implementation in SC form of the polyphase structures in Fig.4.12-b and Fig.4.13-b can be divided into two parts. The first part corresponds to the implementation of the transmission factors using SC elements with only

switches and capacitors. These SC elements realise the operations of sampling, delay and weighting, and their discrete-time input-output relation is of the form

$$\Delta Q_n = C_n z^{-n} V_i(z) \qquad (4.6) \ldots$$

The capacitance values correspond to the coefficients of the transmission factors, i.e. the impulse response coefficients, while the delays are obtained by an appropriate switch phasing for each SC element. The second part of the polyphase structures consists of an SC accumulator that realises the addition of the charge packets $\Delta Q_n(Z)$ produced by the SC elements. Its ideal discrete-time input-output relation is of the form

$$V_o(z) = \frac{1}{C} \Sigma \Delta Q_n(z) \qquad (4.7) \ldots$$

Next, we shall consider the SC implementations of these blocks, starting with the accumulator.

4.4.2 SC accumulator

For the SC decimator, implemented using the polyphase structure in Fig.4.12-b, the accumulator may be realised as shown in Fig.4.14. During the reference period of the decimator, i.e. <u>one period of the output signal</u>, the incoming charge packets $\Delta Q_n(Z)$ corresponding to all terms of the FIR prototype filter are transferred into the memoried feedback capacitor C. At the end of the reference period, in slot 1, the new output voltage is sampled by the

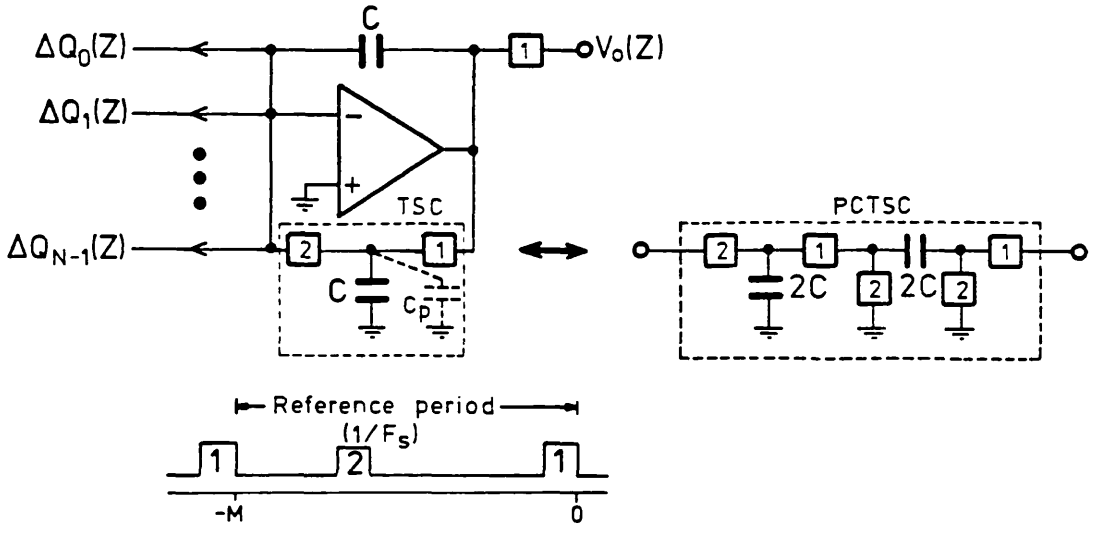


Fig.4.14: SC accumulator for decimation

following SC circuit and also by the feedback TSC branch; then, in slot 2 of the next reference period, the TSC branch transfers its charge to the feedback capacitor and thus resets the previous output voltage. At the same time, a new cycle of charge accumulation is executed. By taking into account the parasitic capacitance C_p we obtain the following discrete-time input-output relation

$$V_o(Z) = \frac{1}{C} \frac{\sum_{n=0}^{N-1} \Delta Q_n(Z)}{1 + \frac{Cp}{C} Z^{-M}} \qquad (4.8) \ldots$$

As we saw in Fig.4.13-b, the preferred structure for interpolation employs only one time-shared SC accumulator. This is shown in Fig.4.15 for the simple case of L=2. During one reference period of the interpolator, i.e. one period of the input signal, there are L=2 cycles of the operation of the SC accumulator, each of which produces one

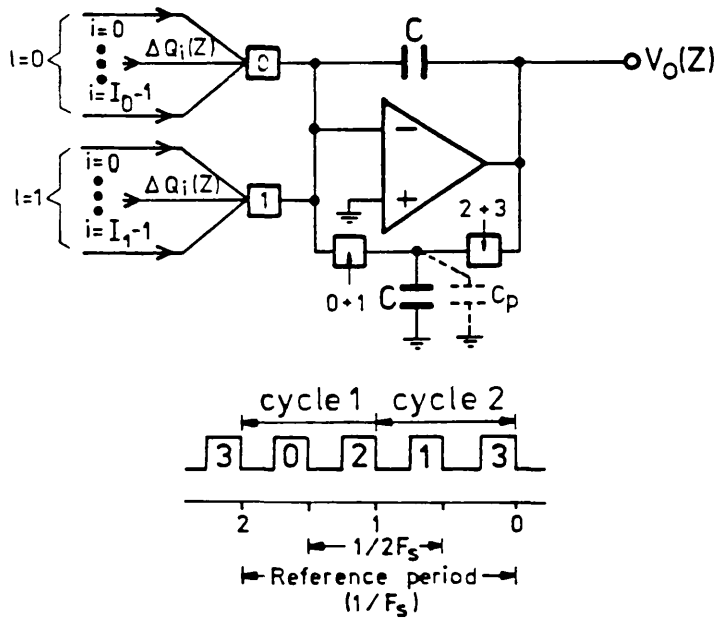


Fig.4.15: A simple time-shared SC accumulator for interpolation (L=2)

sample of the output interpolated signal. Firstly, in slot 0, the charge packets of the polyphase filter l=0 are transferred to the output of the accumulator, while the previous output voltage is reset by the charge transfer from the feedback TSC branch. In slot 2, the new output voltage is sampled by the feedback TSC branch. In the second cycle, the charge packets of the polyphase filter l=1 are transferred to the output of the accumulator in slot 1, while the previous output voltage is reset by the charge transfer from the feedback TSC branch. This second cycle ends with slot 3, when the new output voltage is sampled by the feedback TSC branch. With such an arrangement of the switch phasing the output of the interpolator is implicitly sampled and held, because the output voltage changes only during slots 0 and 1. The

discrete-time input-output relation of the SC accumulator for the first interpolated sample, in slot 0, is given by

$$(4.9\text{-a}) \quad \ldots \qquad V_{o1} = \frac{1}{C} z^{3/2} \frac{\sum_{i=0}^{I_o-1} \Delta Q_i(z)}{1 + \frac{Cp}{C} z^{-1}}$$

and for the second interpolated sample, in slot 1, by

$$(4.9\text{-b}) \quad \ldots \qquad V_{o2} = \frac{1}{C} z^{1/2} \frac{\sum_{i=0}^{I_1-1} \Delta Q_i(z)}{1 + \frac{Cp}{C} z^{-1}}$$

We can observe in (4.8), and in (4.9), that the discrete-time expressions in the numerators are not affected by the parasitic capacitance C_p of the MOS capacitor (top-plate) and switches. Since these numerators define the FIR transfer functions of the SC decimators and interpolators, the location of the notches of the amplitude response will not be affected either. The parasitic capacitance C_p does introduce a parasitic pole at $Z=-C_p/C$, and a DC gain variation of $-20\log(1+C_p/C)$, but both of these effects are usually negligible. In order to improve the accuracy of the amplitude response, the effects of the parasitic capacitance can be eliminated by employing the PCTSC reset branch shown in Fig.4.14 [4.10].

4.4.3 Direct-form SC elements

Now, we shall look at the implementation of the transmission factors of the polyphase structures in Fig.4.12-b and Fig.4.13-b using SC elements. It is

convenient to refer the operation and the switch phasing of such SC elements to the reference periods defined for the SC accumulators. Various situations have to be considered depending on the number of terms, i.e. the length, of the polyphase filters.

Simple SC elements implement the first term of the polyphase filters, i.e. the terms with transmission factors hm or hl, and correspond to a situation where the input signal is sampled during the reference period. Such SC elements can be realised using conventional SC branches switched in the normal manner, which means that during the reference period the time slot for sampling precedes the time slot for charge transfer. The TSI branch in Fig.4.16-a realises positive coefficients, whereas the OFR branch in Fig.4.16-b realises negative coefficients. An alternative realisation of the terms with negative coefficients uses the PCTSC branch in Fig.4.16-c. For the SC decimator, the delays of these SC branches refer to the reference period in Fig.4.16-d, and are determined with respect to the sampling slots, e.g. slot 1. On the contrary, for the SC interpolator the delays should be referred to the charge transfer slots, e.g. slot 2. The SC elements in Fig.4.16 are canonic in the sense that they utilise only one SC branch with one capacitor in order to realise one term of the FIR impulse responses.[1]

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[1] We assume that the PCTSC branch with two capacitors 2C is equivalent to an SC branch with one capacitor C [4.10].

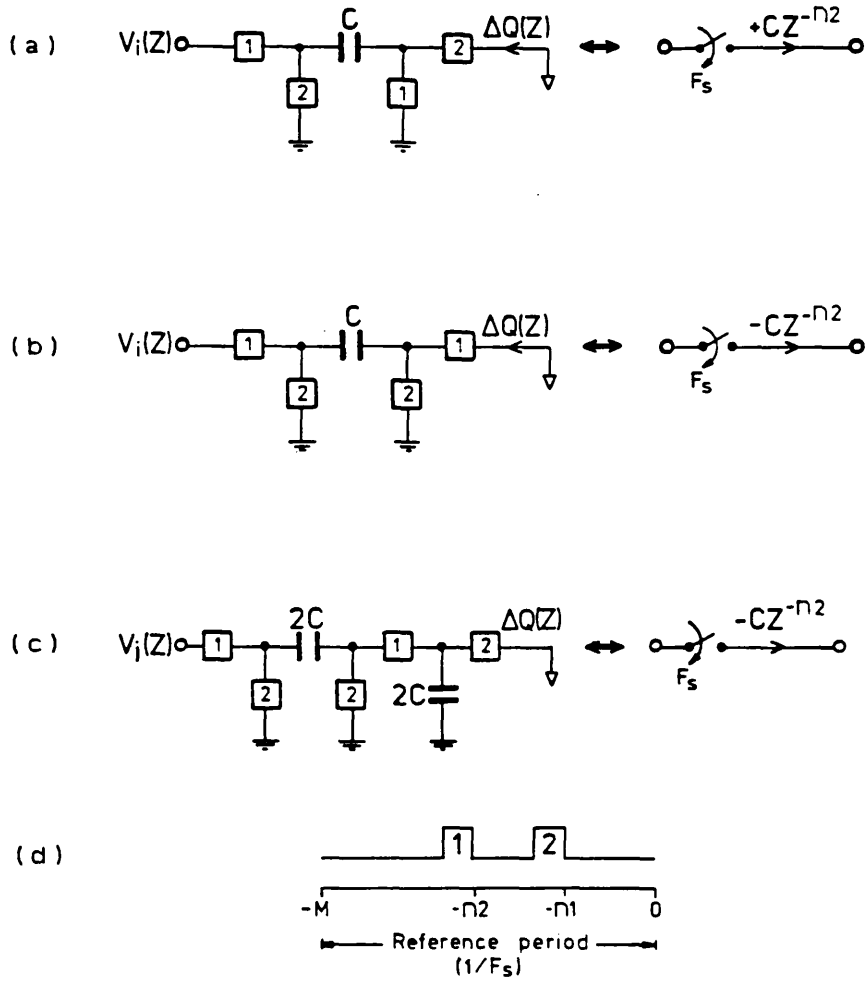


Fig.4.16: SC elements for the first term of the polyphase filters, using a normal sequence of sampling followed by charge transfer

The SC elements that implement the terms with transmission factors $h_{m+M}.Z^{-M}$ or $h_{l+L}.Z^{-L}$ correspond to a situation where the input signal is sampled in the period preceeding the reference period. Such SC elements can be realised by inverting the sequence of sampling and charge transfer, during the reference period. This operation can only be achieved using TSI and PCTSC branches because, in these branches, sampling and charge transfer take place in different slots. The TSI branch in Fig.4.17-a realises

positive coefficients, while the PCTSC branch in Fig.17-b realises negative coefficients. It is easy to see that these SC elements are also canonic, as before.

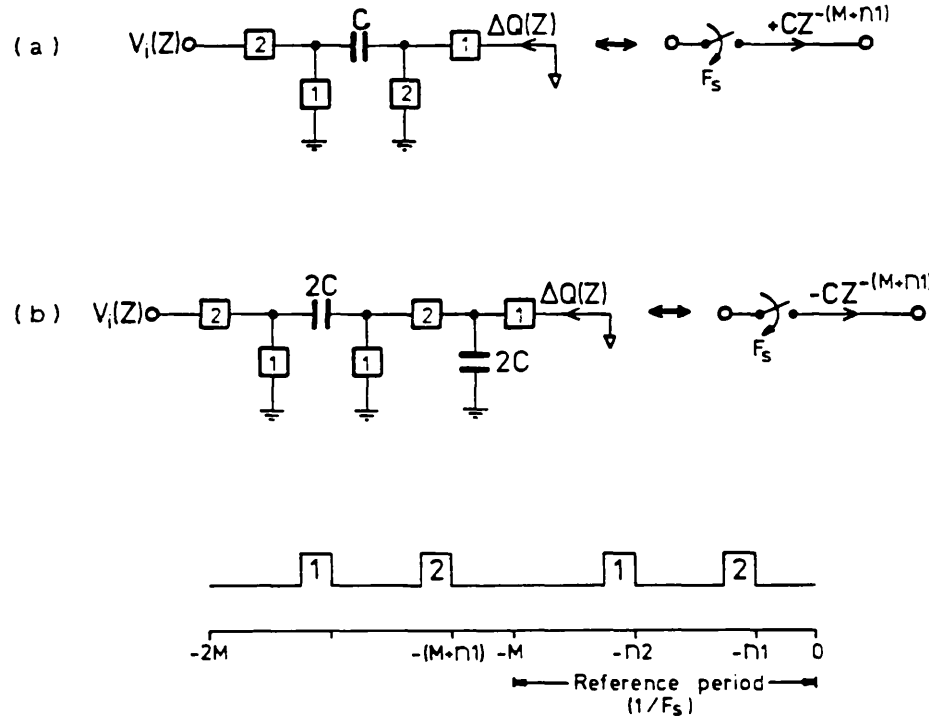


Fig.4.17: SC elements for the second term of the polyphase filters, using an inverted sequence of charge transfer followed by sampling

In order to implement terms with transmission factors $h_{m+2M}.Z^{-2M}$ or $h_{1+2L}.Z^{-2L}$, $h_{m+3M}.Z^{-3M}$ or $h_{1+3L}.Z^{-3L}$, and so forth, it is necessary to introduce SC branches with reduced sampling rate that can sample the input signal at two, three or more periods before the reference period. But, because of the reduced sampling rate, it is also necessary to have multiple SC branches to ensure that such terms are realised every reference period. Such a scheme is illustrated in Fig.4.18, for a transmission factor $h_{m+2M}.Z^{-2M}$. The SC element consists of two paralleled SC

branches, with reduced sampling rate $F_s/2$, and with an inverted sequence of charge transfer followed by sampling.

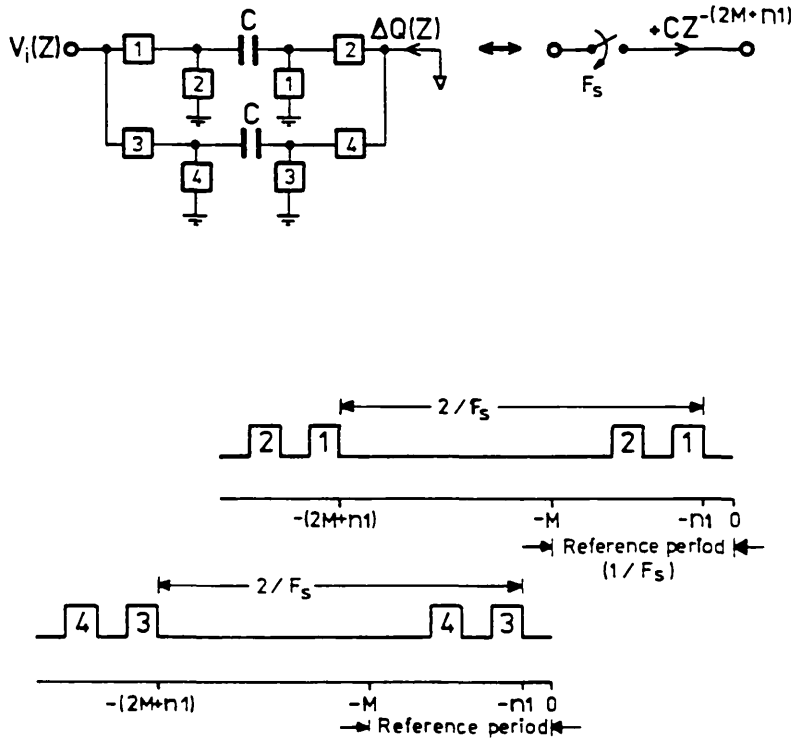


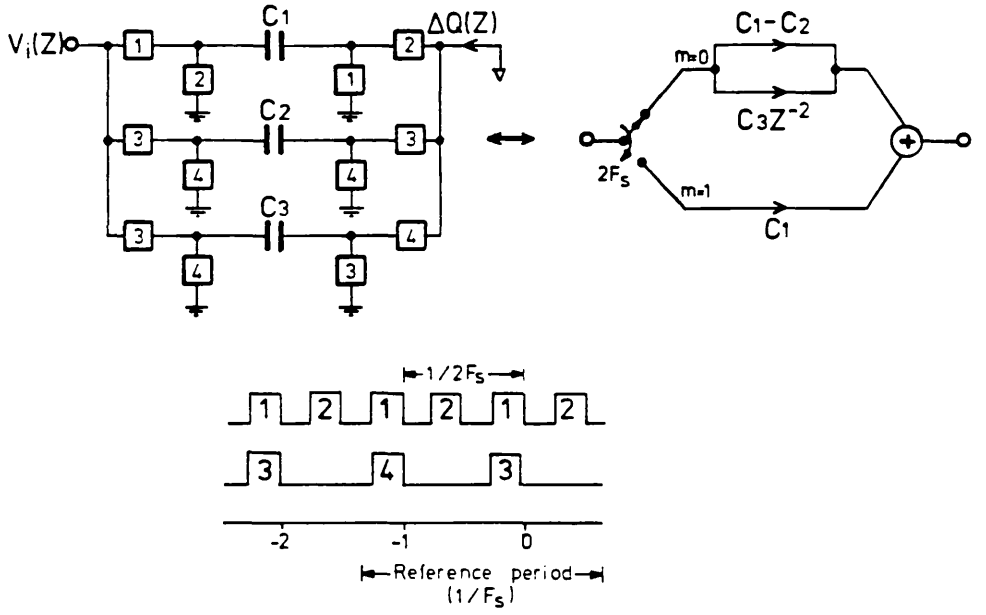
Fig.4.18: Example of a non-canonical SC element for the third term of the polyphase filters, using SC branches with reduced sampling rate

We should note that although this SC element is non-canonic with respect to the number of SC branches and capacitors, it is still a direct-form implementation since it realises only one term of the FIR impulse response.

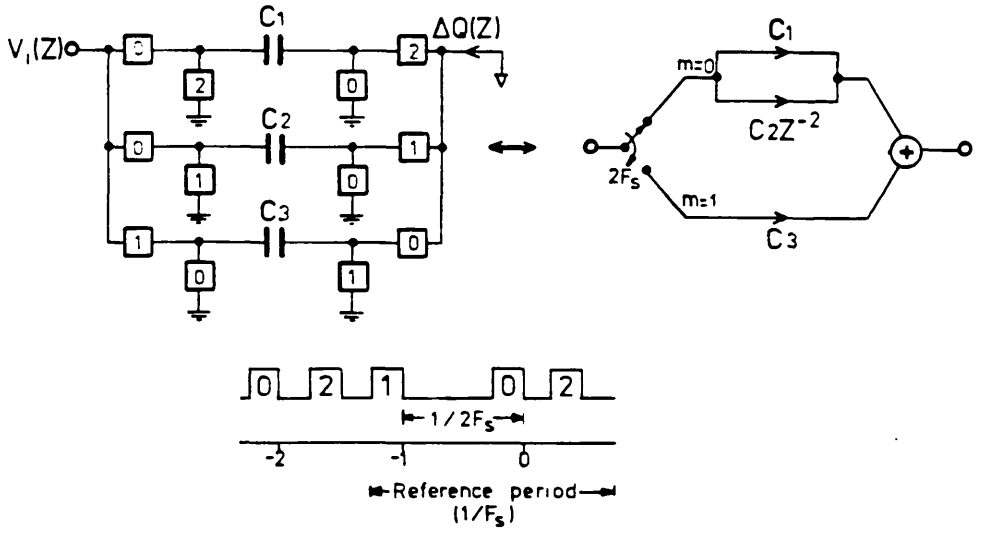
4.4.4 Multiplexed SC elements

There are other forms of non-canonical implementations of the SC elements which may lead, in some cases, to a reduction of the total number of SC branches and capacitors. These are the multiplexed implementations of SC

elements which lead to non-direct-form SC structures. An example of a polyphase structure with a multiplexed implementation of SC elements is shown in Fig.4.19-a. Here, the SC branch with capacitor C_1 is switched at higher rate $2F_s$, and realises terms that correspond to different



(a)

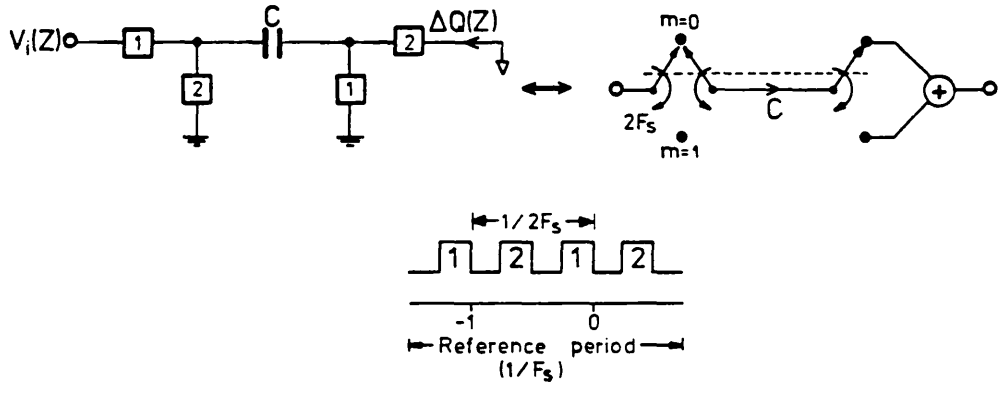


(b)

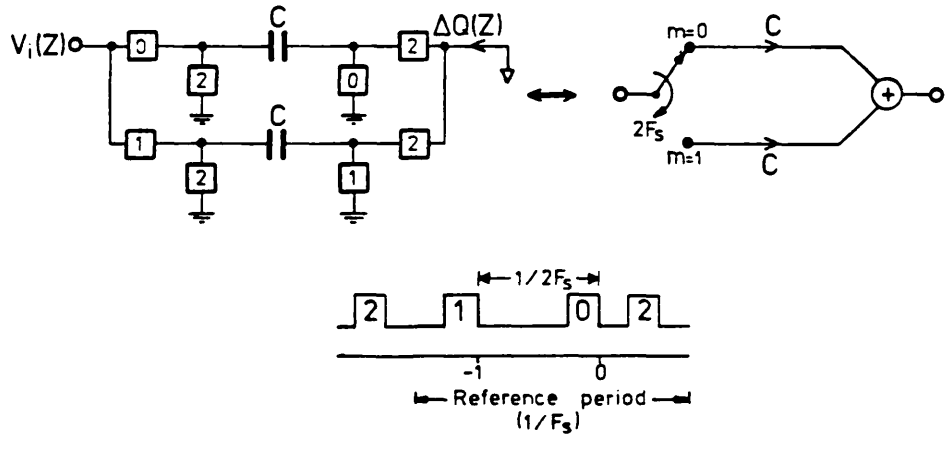
Fig.4.19: Alternative implementations of polyphase filters. (a) Multiplexed SC elements, and (b) direct-form SC elements

polyphase filters. The alternative direct-form implementation is shown in Fig.4.19-b.

Multiplexed schemes are especially attractive for applications of SC decimators in which the prototype filter has equal coefficients and the length is N=M [4.11]-[4.13]. It is easy to see that in such cases the polyphase filters have only one term, and thus only one SC branch is needed to implement the polyphase structure. This form of multiplexing is illustrated in Fig.4.20-a (M=2), and we can compare it with the equivalent direct-form realisation in



(a)



(b)

Fig.4.20: Simple prototype filters with equal coefficients. (a) Multiplexed, and (b) direct-form SC implementation

Fig.4.20-b. This multiplexing scheme is particularly advantageous when M is large [4.12],[4.13].

4.4.5 Memoried SC elements

One characteristic common to all previous SC elements is that they are memorieless, in the sense that before each new sampling phase they have been discharged to zero voltage. The Single-Phase Floating Capacitor (SPFC) [4.14] branch shown in Fig.4.21, on the contrary, is a memory

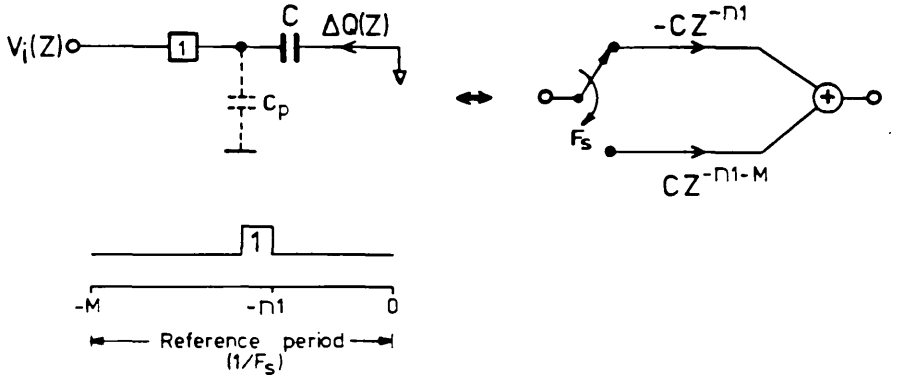


Fig.4.21: Memoried SC element (SPFC)

possessing element, which holds information between two consecutive sampling instants. Therefore, an SPFC branch contributes to the realisation of terms with transmission factors $h_{m+iM} \cdot Z^{-iM}$ and $h_{m+(i+1)M} \cdot Z^{-(i+1)M}$, in the polyphase filters for decimation, or with transmission factors $h_{l+iL} \cdot Z^{-iL}$ and $h_{l+(i+1)L} \cdot Z^{-(i+1)L}$, in the polyphase filters for interpolation. This is illustrated in the polyphase structure for decimation M=2 shown in Fig.4.22 [4.15].

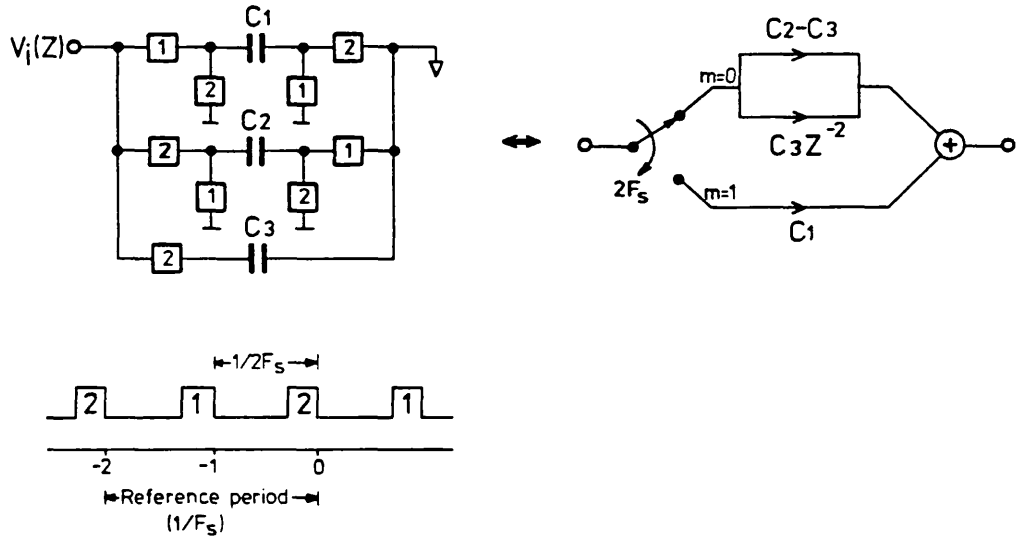


Fig.4.22: Implementation of polyphase filters using a memoried SC element

As we can see in Fig.4.21, the SPFC branch is not strictly insensitive to grounded parasitic capacitances, since the switched terminal of the capacitor remains floating after the sampling phase. It was found in practice that this characteristic affects considerably the performance of SC circuits [4.15],[4.16], and, therefore, despite its simplicity, this type of memoried SC element is not very attractive for high-quality SC decimators and interpolators.

4.5 DESIGN EXAMPLES OF NON-RECURSIVE POLYPHASE SC DECIMATORS AND INTERPOLATORS

This Section illustrates the systematic procedure for the design of polyphase SC decimators and interpolators, considering examples which are suitable for the

applications of SC bandpass filter systems that we shall describe in the next Chapter.

4.5.1 Single-stage SC decimator M=4

For a narrow SC bandpass filter centered at f_o=20KHz it is required to reduce the sampling rate from $4F_s$=192KHz to F_s=48KHz. The amplitude response of the prototype filter must have the notches at frequencies $3F_s \pm f_o$, $2F_s \pm f_o$ and $F_s \pm f_o$, and by using the simple technique described in Section 2.5 we arrive at the optimum impulse response given in Fig.4.23-a. The prototype filter is decomposed into M=4 polyphase filters leading to the polyphase structure given

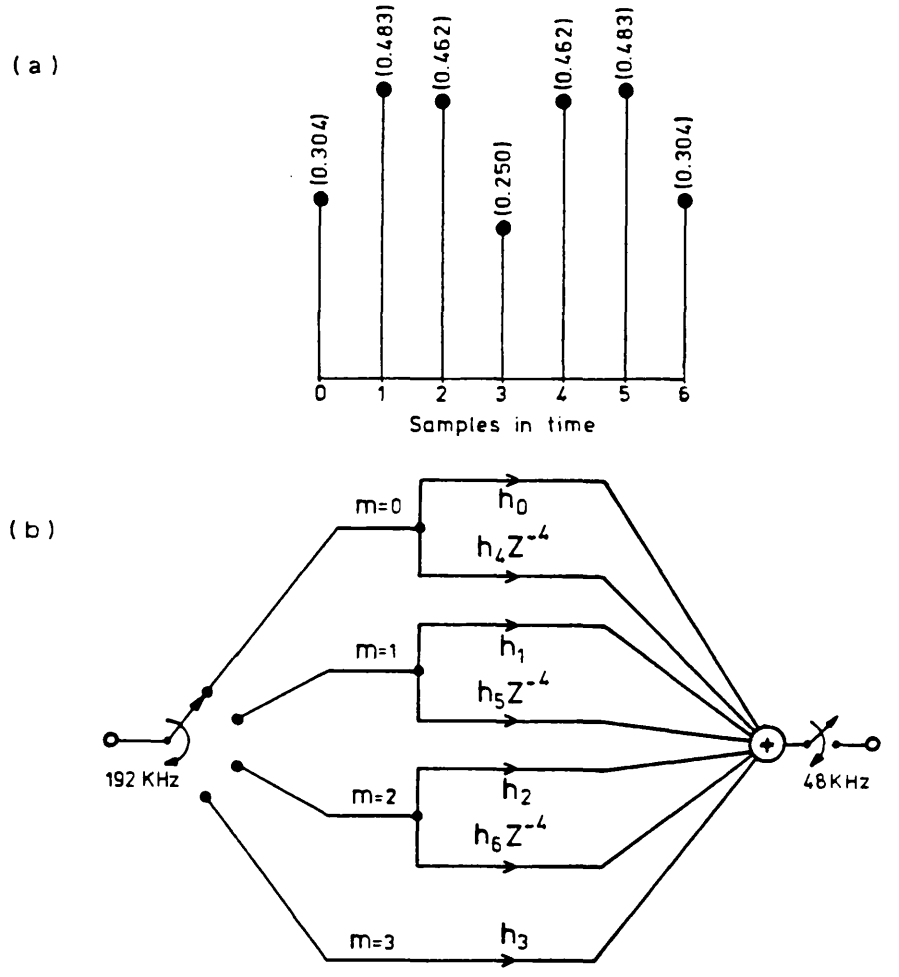


Fig.4.23: FIR prototype filter for a decimator M=4. (a) Optimised impulse response; (b) Corresponding polyphase structure

in Fig.4.23-b. The SC implementation in direct-form leads to the polyphase SC decimator shown in Fig.4.24-a, which operates with the time frame of Fig.4.24-b. It is easy to observe the correspondence between the SC decimator and the polyphase structure. For example, the input signal is sampled in slot 0 by the polyphase filter m=0, in slot 1 by the polyphase filter m=1, and so forth. The terms with transmission factors h_m are realised by SC branches switched in the normal manner, and thus the charge transfer

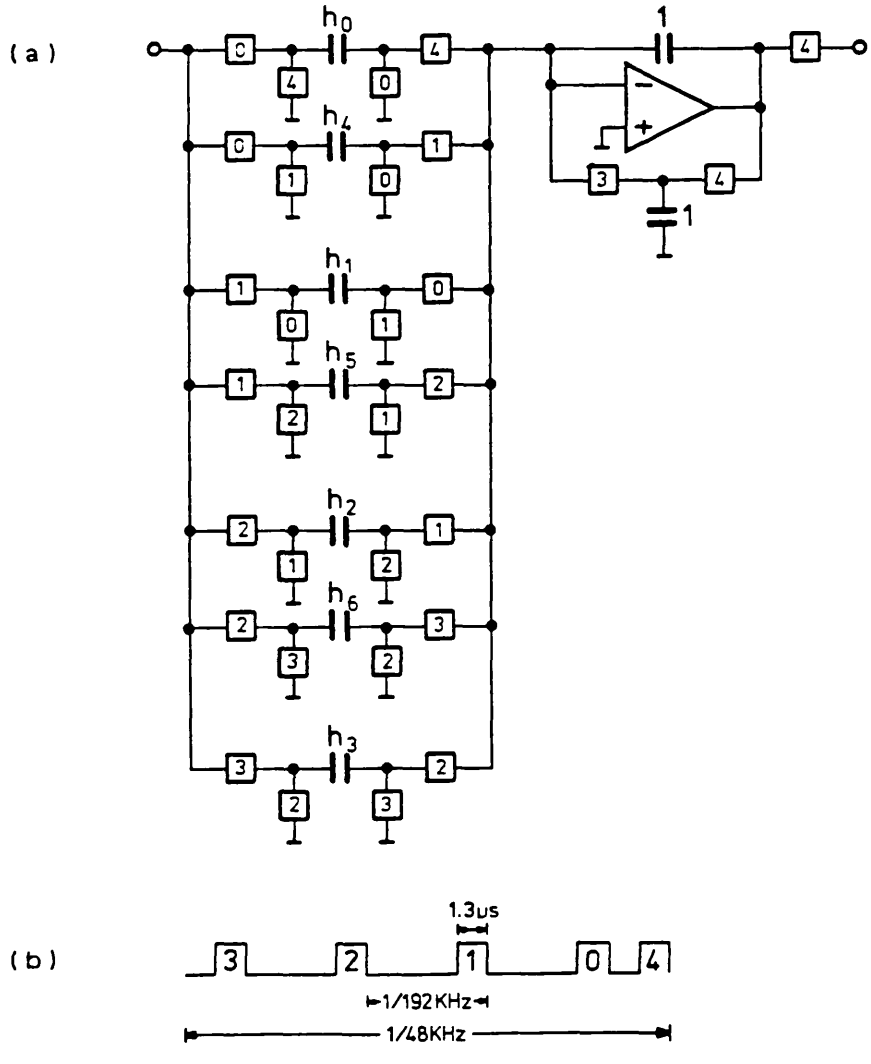


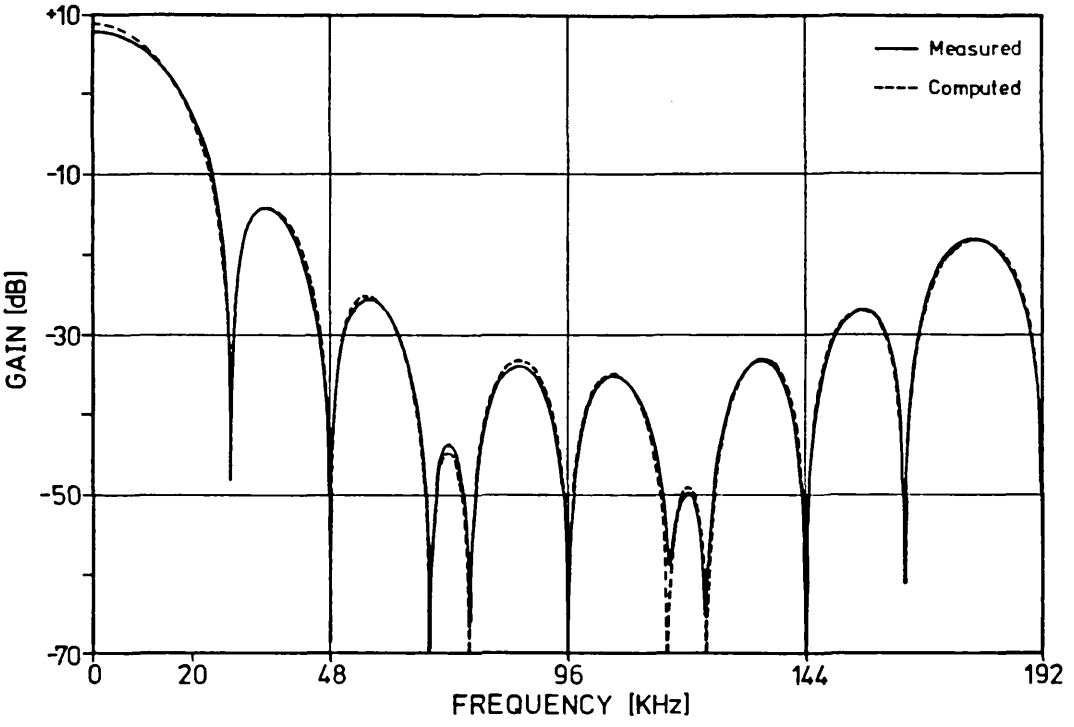
Fig.4.24: (a) Single-stage polyphase SC decimator M=4;
(b) Time frame

slots appear after the sampling slots. But the terms with transmission factors $h_{m+4}.z^{-4}$ are realised by SC branches with an inverted sequence of charge transfer followed by sampling, and thus the charge transfer slots appear before the sampling slots within the reference period.

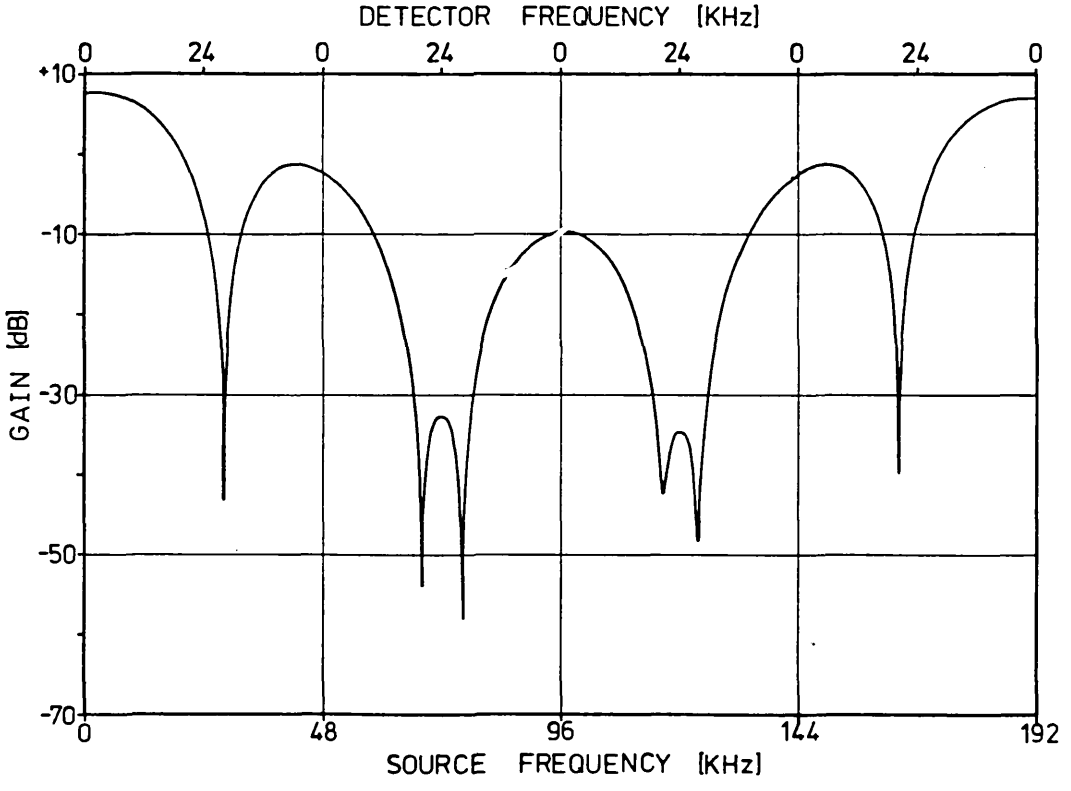
This SC decimator circuit was built using discrete components: CMOS 4016 analogue switches, BiMOS 3140 OA's and capacitance values ranging from 18.17pF to 59.68pF. By using a baseband sweeping mode, as defined in Section 2.2, we obtain the measured amplitude response in Fig.4.25-a, which includes additional notch frequencies at multiples of F_s=48KHz due to the sample and hold effect. This effect was also simulated in the computed response using the computer program SWITCAP [4.17]. In the experimental curve, the slight attenuation at DC is due to the parasitic capacitance in the feedback TSC branch of the SC accumulator, as we saw in (4.8). This effect is negligible in the passband centred at f_o=20KHz. We can obtain the effective anti-aliasing performance of this SC decimator by using an alias sweeping mode, also defined in Section 2.2, giving the measured amplitude response shown in Fig.4.25-b.

4.5.2 Cascade SC interpolator L=4

In this example we design an SC interpolator which is complementary to the previous decimator. We adopt a cascade approach where the first section increases the sampling rate from F_s=48KHz to $2F_s$=96KHz, and then the second section further increases the sampling rate from $2F_s$=96KHz to $4F_s$=192KHz. The notch frequencies in the first section



(a)



(b)

Fig.4.25: Evaluation of the SC decimator M=4.
(a) Baseband response
(b) Aliasing response

are placed at $F_s \pm f_o$, but they are also repeated at $3F_s \pm f_o$; the notch frequencies at $2F_s \pm f_o$ are introduced in the second section. For the requirements of the first section, for example, we obtain the FIR prototype filter with the original impulse response given in Fig.4.26-a. This impulse response is modified according to (4.5), on account of the sampled and held signals at the input. Then, the modified impulse response in Fig.4.26-b is decomposed into L=2

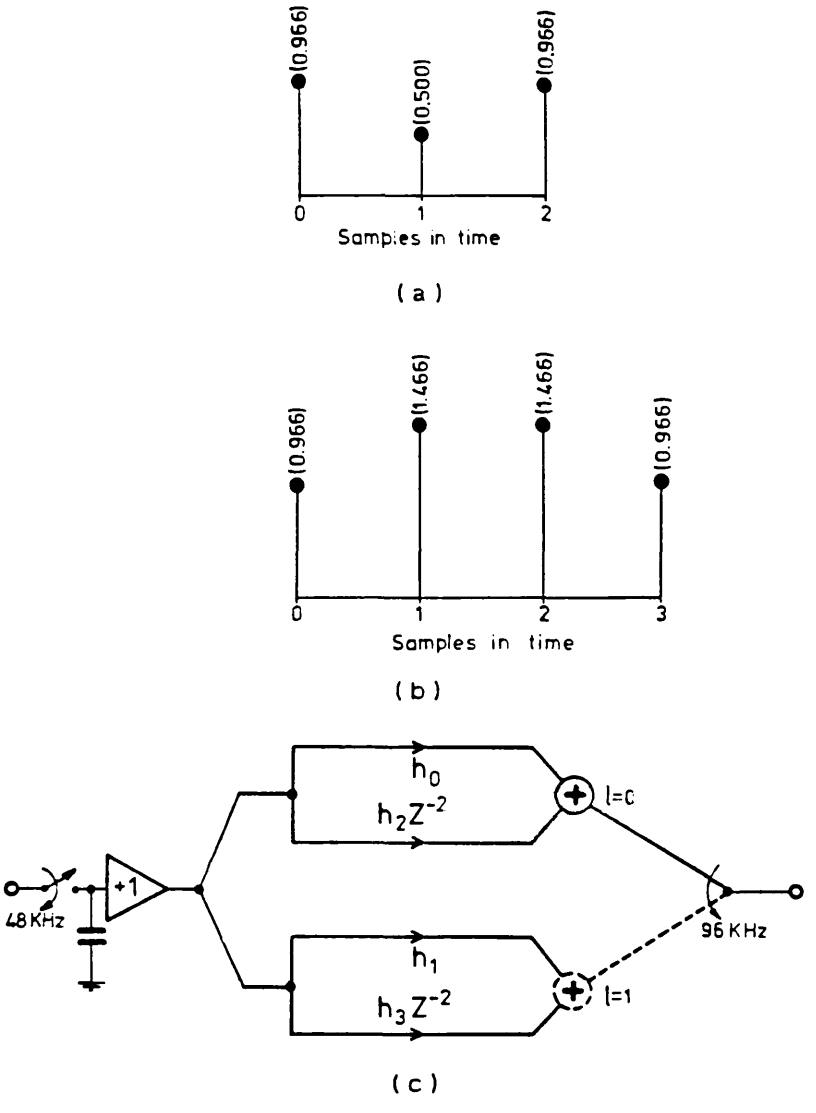


Fig.4.26: FIR prototype for an interpolator L=2. (a) Original, and (b) modified impulse responses; (c) Polyphase structure

polyphase filters indicated in Fig.4.26-c. This polyphase structure leads to the polyphase SC interpolator shown in Fig.4.27-a, with the time frame given in Fig.4.27-b.

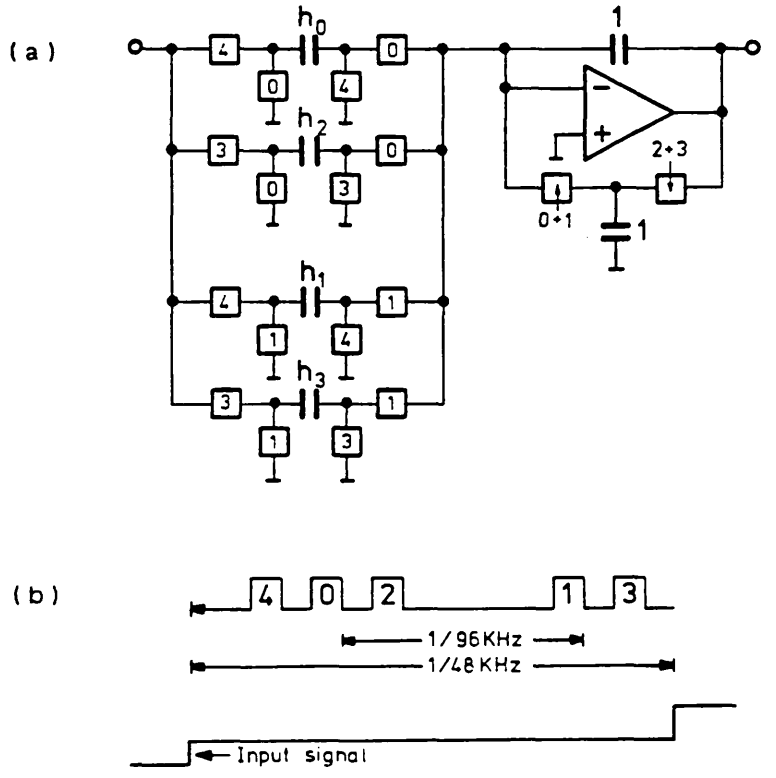


Fig.4.27: (a) Polyphase SC interpolator L=2;
(b) Time frame

In order to observe the correspondence between the SC interpolator and the polyphase structure we should look at the charge transfer slots. The first output sample is produced by the polyphase filter l=0 in slot 0, and the second output sample is produced by the polyphase filter l=1 in slot 1. The SC branches that realise the terms with transmission factors h_1 have the sampling slots before the charge transfer slots; but since the input signal is sampled and held, only one sampling slot is needed, slot 4.

For the terms with transmission factors $h_{1+2}.z^{-2}$ the SC branches have an inverted sequence, of charge transfer followed by sampling; as before, only one sampling slot is needed, slot 3.

By using a similar procedure we obtain the structure for the second SC interpolator section, and then the cascade realisation of Fig.4.28 results. No sample and

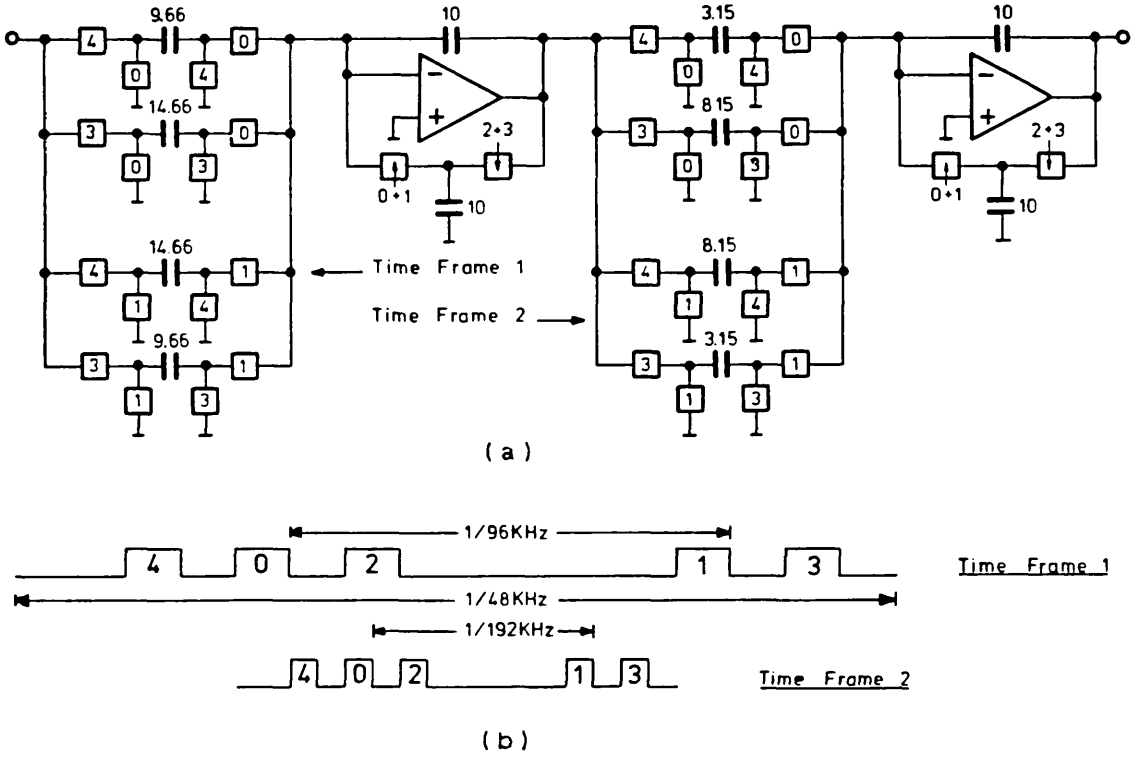


Fig.4.28: (a) Cascade polyphase SC interpolator L=4;
(b) Time frame

hold circuit is needed to interface the two sections because the output of the first SC interpolator section is implicitly sampled and held in the slots 0 and 1 of time frame 1. We built a discrete component model of this SC interpolator circuit using the same type of components indicated before; the nominal capacitance values range from

32.28pF to 102.44pF. The measured baseband baseband response of the SC interpolator is given in Fig.4.29 and compared to the computed response.

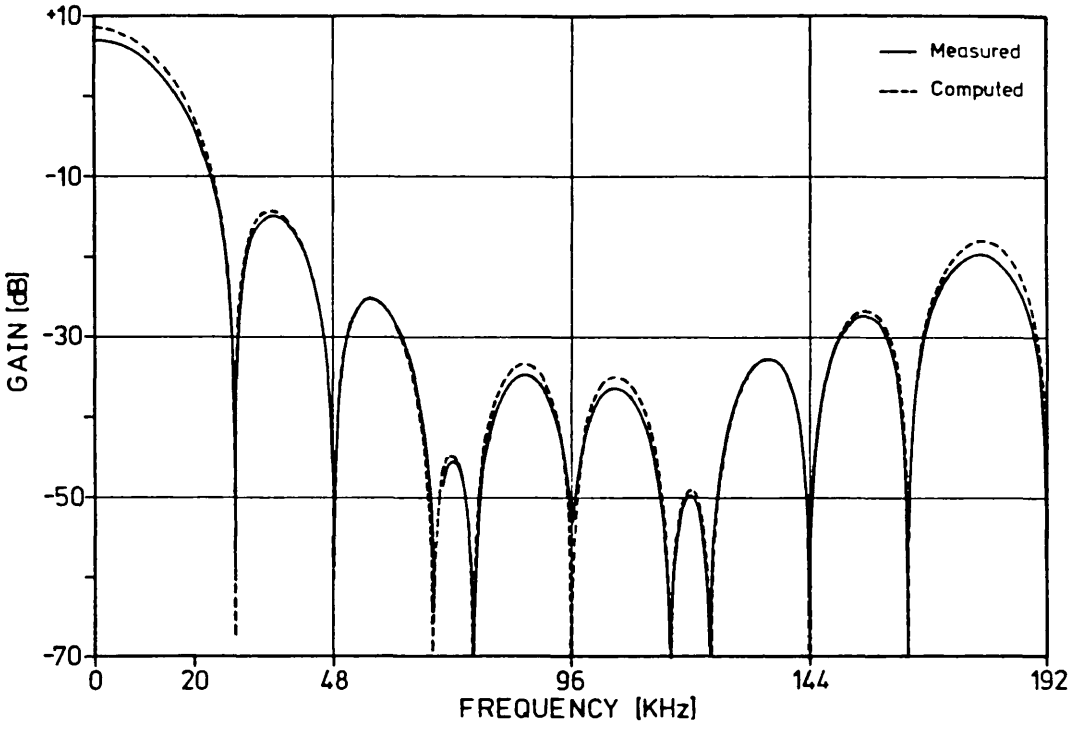


Fig.4.29: Baseband response of the cascade SC interpolator L=4

4.5.3 Single-stage SC interpolator L=4

Here, we design a polyphase SC interpolator L=4 using only one OA. We consider the same requirement which was used for the cascade biquad realisation of the FIR SC interpolator L=4 considered in Section 4.2, and shown in Fig.4.2. For this single-stage SC interpolator, the optimised impulse response of the prototype filter is given in Fig.4.30-a, and the corresponding modified impulse response is shown in Fig.4.30-b. In the polyphase

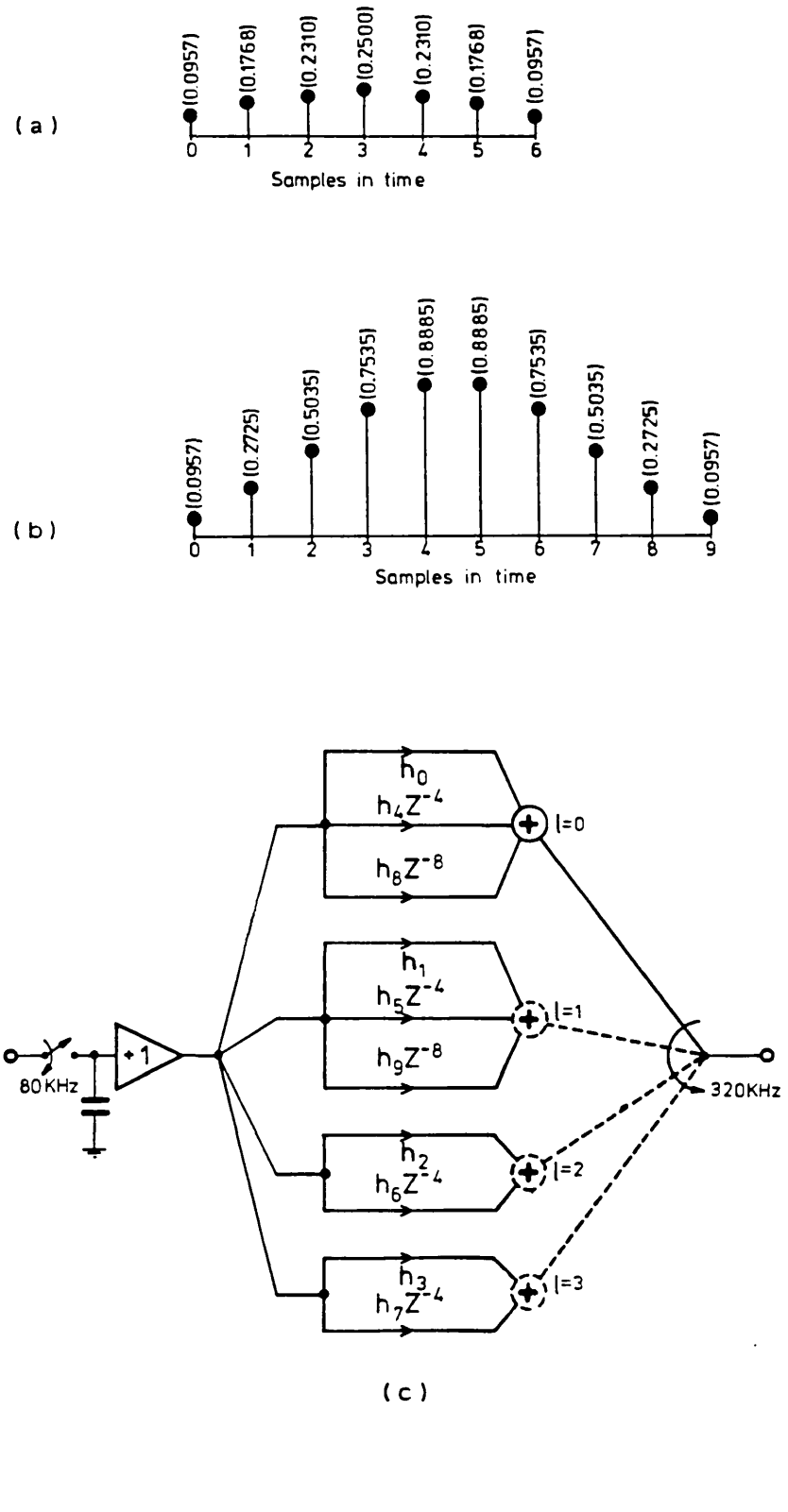


Fig.4.30: FIR prototype filter for an interpolator L=4.
(a) Original, and (b) modified impulse responses;
(c) Polyphase structure

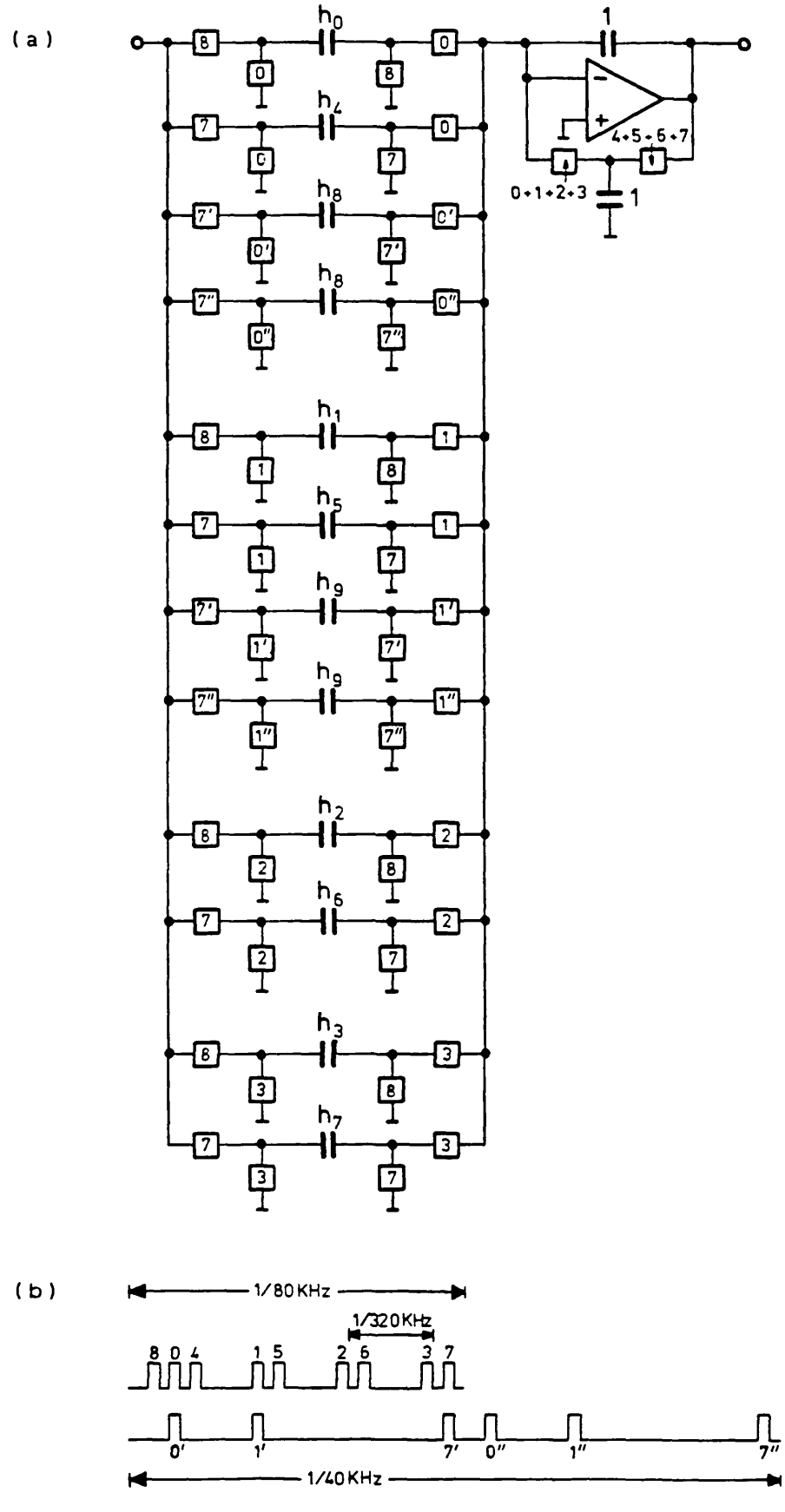


Fig.4.31: (a) Single-stage polyphase SC interpolator L=4; (b) Time frame

structure of Fig.4.30-c, the implementation of the terms with transmission factors $h_{l+8}.z^{-8}$, in the polyphase filters l=0 and l=1, requires non-canonic SC elements with multiple SC branches. The scheme given in Fig.4.18 is appropriate for this purpose. The resulting polyphase SC interpolator is shown in Fig.4.31-a which operates with the time frame of Fig.4.31-b. This SC interpolator circuit was also built with standard discrete components and we obtained the measured amplitude response shown in Fig.4.32.

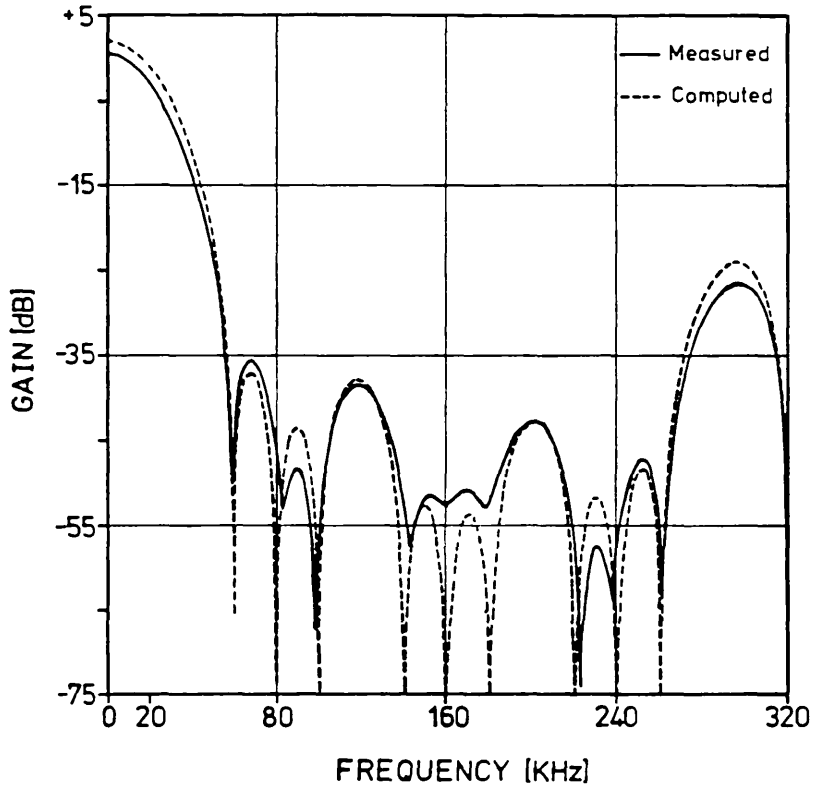


Fig.4.32: Baseband response of the single-stage SC interpolator L=4

In the light of the analysis of the non-ideal effects that we shall present in the Appendix, the increased complexity of this single amplifier SC interpolator with respect to

the number of input SC branches, and time slots, may explain the poorer accuracy of the amplitude response compared to the cascade polyphase non-recursive structure. A brief summary of the results derived in the Appendix, particularly with respect to capacitance ratio and timing errors, will be presented next.

4.5.4 Practical considerations

The errors produced in the impulse response coefficients of the FIR transfer functions of the SC polyphase structures are primarily due to capacitance ratio errors associated with the input SC branches. Considering the example of the SC decimator M=4 in Fig.4.24-a, we can minimise the effect of such errors by implementing the capacitance ratios as illustrated in Fig.4.33. The most

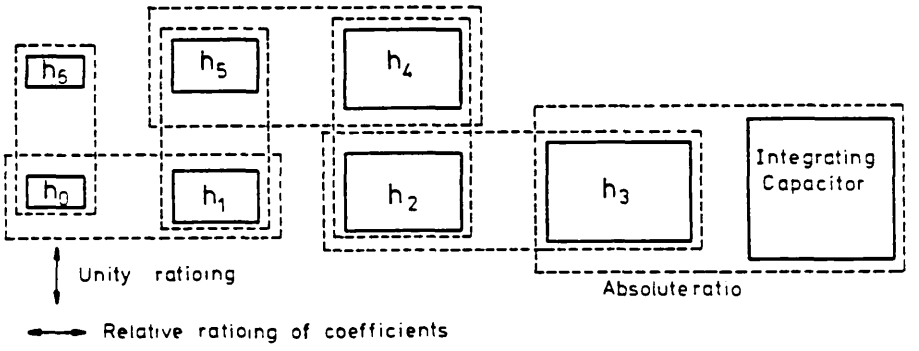


Fig.4.33: Ratioing strategy for the polyphase SC decimator M=4, which reduces impulse coefficient errors

critical capacitance ratios are in relation to the capacitors of the input SC branches, whereas the capacitance ratios relative to the feedback capacitor of

the OA, which are most critical in conventional SC filter circuits, are here less important. Capacitors corresponding to symmetric impulse response coefficients, for instance h_0 and h_6, have equal areas, and thus the capacitance ratio accuracy is maximum. The ratios between horizontally adjacent capacitors, h_0 and h_1, for example, are also maximised, because such ratios correspond to a difference between adjacent impulse response coefficients, which is smaller than their absolute values. In the case of implementation in integrated circuit form, it is also important that equal valued capacitors on-chip are physically close to each other, in order to minimise effects of oxide thickness variations, for example, thus maximising tracking of capacitance values [4.18].

The timing of the non-recursive polyphase SC decimator and interpolator circuits is affected by differential time errors between each critical slot in the time frame, i.e. the time slots that determine the powers of Z in the corresponding FIR transfer function. These errors are essentially due to the digital time slot generators. In order to minimise such errors, which produce large variations of the multinotch amplitude response, we designed time slot generators with identical digital paths for the time slots. This ensures that the timing errors result only from differential propagation delays of similar gates, and thus can be acceptably small.

4.6 DESIGN OF DECIMATORS AND INTERPOLATORS WITH COMBINED SC BIQUAD-SC POLYPHASE STRUCTURES

In frequency-translated SC systems we have to reject unwanted alias and image frequency-translated components below as well as above the desired passband, for which it is necessary to utilise SC decimators and interpolators with highpass or with bandpass amplitude responses. Such SC decimators and interpolators are usually required to have higher selectivity than the SC lowpass decimators and interpolators of the previous examples.

Highpass and bandpass FIR polyphase SC decimators and interpolators can be derived by employing the procedure described above for lowpass FIR polyphase SC decimators and interpolators. In order to increase the selectivity of the multinotch amplitude response, for given L and M, we have to increase the number of notch frequencies which, in turn, implies increasing the length of the optimum FIR prototype filter for decimation and the modified prototype filter for interpolation. This may lead to SC circuits which may not be practical for implementation, mainly due to the many time slots, thus switching waveforms, required to operate the SC branches. We consider here an alternative type of SC decimator and interpolator circuits, in which we combine an FIR polyphase SC structure together with an IIR SC biquad as a means of achieving the required increased selectivity of the multinotch amplitude response. We shall consider an example of the design of such SC decimators and interpolators with factors of sampling rate alteration M=3

and L=3, respectively, and with highpass multinotch amplitude responses.

4.6.1 SC decimator M=3

For an SC bandpass filter with centre frequency f_1=4KHz and switching frequency F_s=16KHz, the alias frequency components in the frequency range up to $3F_s$=48KHz are symbolically represented on the discrete-time unit circle as shown in Fig.4.34-a. In the frequency band from

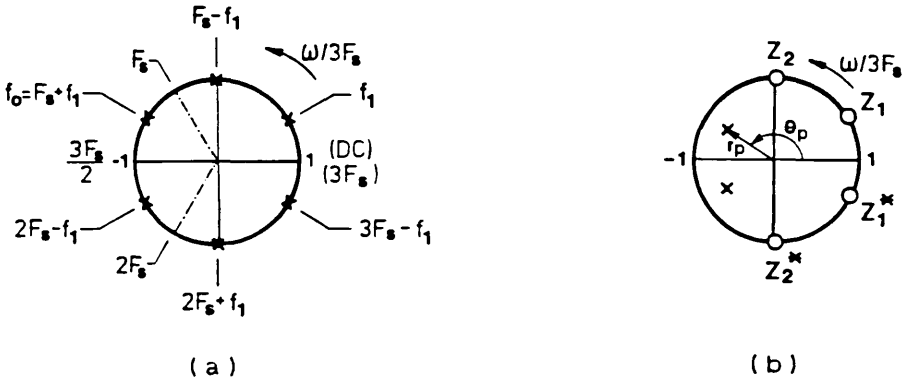


Fig.4.34: (a) Symbolical representation of an SC bandpass filter with switching frequency F_s, on the unit circle from DC to $3F_s$; (b) Pole-zero pattern of SC decimator for selection of the frequency-translated band centred at $f_o=F_s+f_1$

DC to $3F_s/2$=24KHz, an SC decimator M=3 is required to select the alias frequency-translated component at f_o=20KHz and to reject the unwanted baseband component at 4KHz as well as the unwanted alias frequency-translated component at 12KHz. For increased selectivity of such SC decimator we consider the pole-zero pattern illustrated in Fig.4.34-b (the pole-zero pattern in the upper half-circle is repeated in the lower half-circle), which leads to the following

discrete-time transfer function

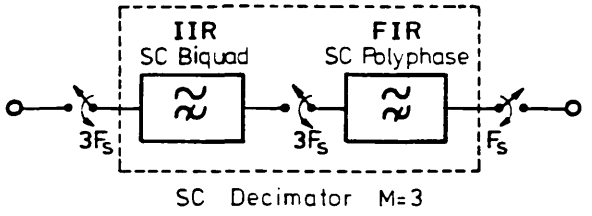
$$(4.10)\ \ldots \quad H(Z) = \left(\frac{h_{01}+h_{11}Z^{-1}+h_{21}Z^{-2}}{1-2r_p\cos\theta_p Z^{-1}+r_p{}^2Z^{-2}} \right).\left(h_{02}+h_{12}Z^{-1}+h_{22}Z^{-2} \right)$$

where the unit delay period is $1/3F_s$. The numerator of the biquadratic function corresponds to the complex conjugate zero-pair $Z_1.Z_1^*$ yielding the notch frequency at 4KHz and the first repetition at 44KHz. The denominator of the biquadratic function, which is also designed directly on the discrete-time domain corresponds to the required complex conjugate pole-pair (equivalent Q-factor is approximately $Q_p=2$, and the pole frequency is approximately $f_p=20KHz$). The FIR quadratic function corresponds to the complex conjugate zero-pair $Z_2.Z_2^*$ yielding the notch frequency at 12KHz and the first repetition at 36KHz. The optimised coefficients for the transfer function (4.10) are given in Table 4.2.

Biquadratic Function	FIR Quadratic Function
$h_{01}=h_{21}=0.14434$	$h_{02}=h_{22}=0.5$
$h_{11}=-0.25$	$h_{12}=0$
$r_p{}^2=0.25$	
$-2r_p\cos\theta_p=0.86603$	

Table 4.2: Optimised coefficients for decimator M=3, with IIR SC biquad-FIR SC polyphase structure

The architecture of the SC decimator M=3 which implements the above transfer function is illustrated in Fig.4.35-a. First, we have the IIR SC biquad with switching



(a)

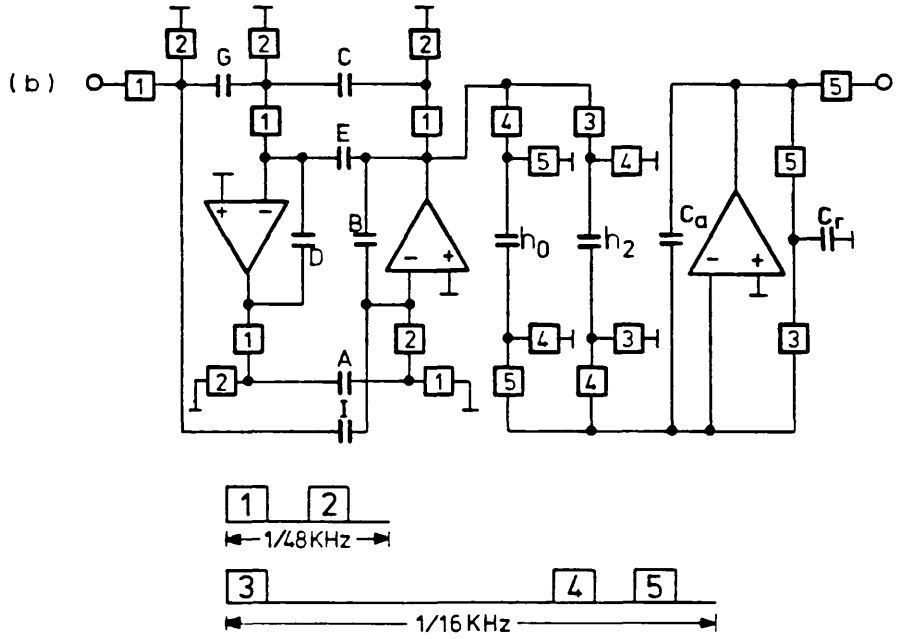


Fig.4.35: (a) Architecture, and (b) circuit, of decimator M=3 with combined SC biquad-SC polyphase structure

frequency $3F_s$=48KHz, which realises the biquadratic function; then we have the FIR polyphase SC structure, which realises the FIR quadratic function, and reduces the sampling rate to F_s=16KHz. The resulting SC decimator with time frame is shown in Fig.4.35-b, and the normalised capacitance values are given in Table 4.3. The SC circuit in Fig.4.35-b was constructed as a discrete component

IIR SC Biquad		FIR SC Polyphase
ICS-1	A - 10.0781 B - 6.9282 I - 1	h_o=1 h_2=1 C_a=2
ICS-2	C - 54.7110 D - 37.6109 E - 19.3917 G - 1	C_r=2

Table 4.3: Normalised capacitance values for SC decimator M=3

model, using CMOS 4016 analogue switches and CMOS 7611 OA's. The measured and computed baseband amplitude responses of the circuit are shown in Fig.4.36. The notches at 16KHz, 32KHz, and 48KHz, result from the sample

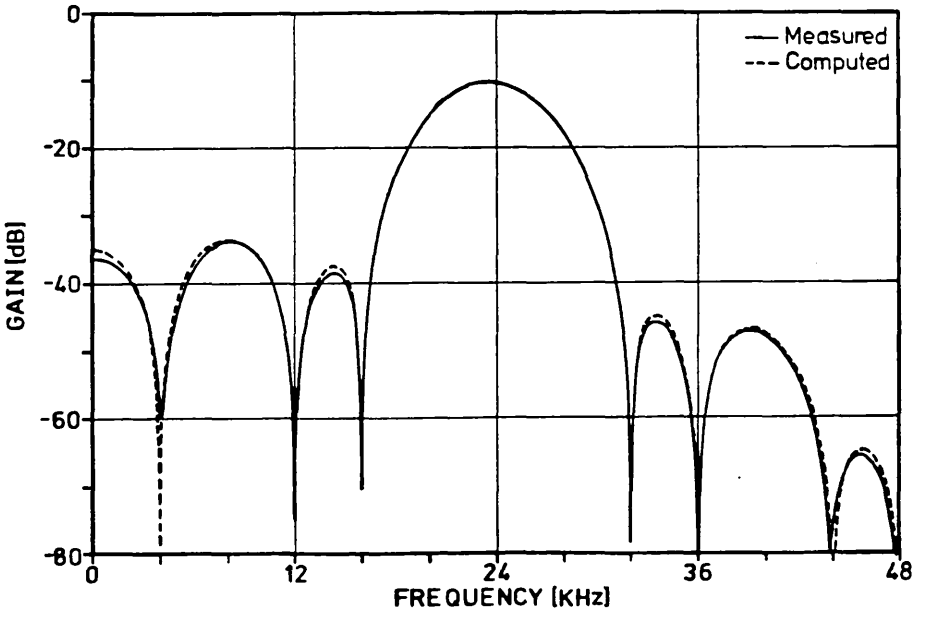


Fig.4.36: Measured baseband amplitude response of SC decimator M=3

and hold effect, which also produces the attenuation at midband frequency f_o=20KHz.

4.6.2 SC interpolator L=3

For an SC interpolator L=3 which is complementary to the previous SC decimator, the original transfer function of the prototype filter has the same form as in (4.10). For the modified prototype filter we have to increase the selectivity of the biquadratic function (equivalent Q-factor is approximately Q_p=5) in order to compensate for the sample and hold effect at the lower sampling rate F_s=16KHz, which attenuates the desired output image at f_o=20KHz. The sample and hold effect also implies a modification of the original FIR function, which will be implemented by a polyphase SC structure for interpolation. The resulting discrete-time transfer function is

(4.11) ...

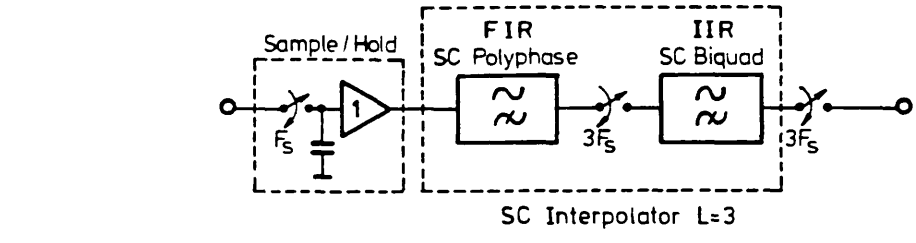
$$H'(Z) = \left(h_{01}+h_{11}z^{-1}+h_{21}z^{-2}+h_{31}z^{-3}+h_{41}z^{-4}\right)\cdot\left(\frac{h_{02}+h_{12}z^{-1}+h_{22}z^{-2}}{1-2r_p\cos\theta_p z^{-1}+r_p{}^2z^{-2}}\right)$$

where the unit delay period is $1/3F_s$. The optimised coefficients are given in Table 4.4.

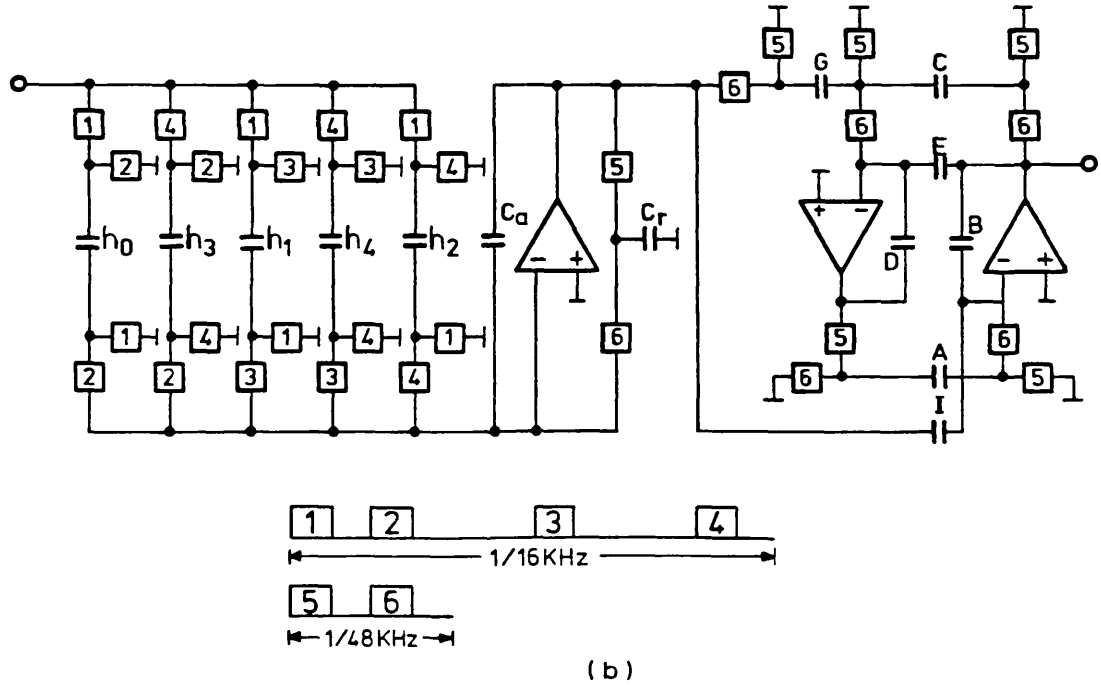
The general form of the SC interpolator L=3, which implements the modified transfer function (4.11) is illustrated in Fig.4.37-a. Now, the polyphase SC structure comes first, in order to increase the sampling rate from F_s=16KHz to $3F_s$=48KHz yielding the notch frequency at 12KHz, and the repetition at 36KHz. Then, we have the SC biquad with switching frequency $3F_s$=48KHz, which realises

Biquadratic Function	Modified FIR Function
$h_{02}=h_{22}=0.32390$	$h_{01}=h_{11}=h_{31}=h_{41}=0.5$
$h_{12}=-0.56101$	$h_{21}=1$
$r_p^2=0.70215$	
$-2r_p\cos\theta_p=1.39346$	

Table 4.4: Optimised coefficients for interpolator L=3, with FIR SC polyphase-IIR SC biquad structure



(a)



(b)

Fig.4.37: (a) Architecture, and (b) circuit, of interpolator L=3 with combined SC polyphase-SC biquad structure

the biquadratic function yielding the notch frequency at 4KHz and the repetition at 44KHz. The resulting SC interpolator with time frame is shown in Fig.4.37-b, with the normalised capacitance values given in Table 4.5. This was constructed as a discrete component model, using CMOS 4016 analogue switches and CMOS 7611 OA's. The measured and computed baseband amplitude responses of the SC circuit in Fig.4.37-b are shown in Fig.4.38.

IIR SC Biquad		FIR SC Polyphase
ICS-1	A - 5.43205	h_0=1
	B - 3.08738	h_1=1
	I - 1	h_2=2
ICS-2	C - 35.6688	h_3=1
	D - 20.27287	h_4=1
	E - 3.43187	Ca=2
	G - 1	Cr=2

Table 4.5: Normalised capacitance values for SC interpolator L=3

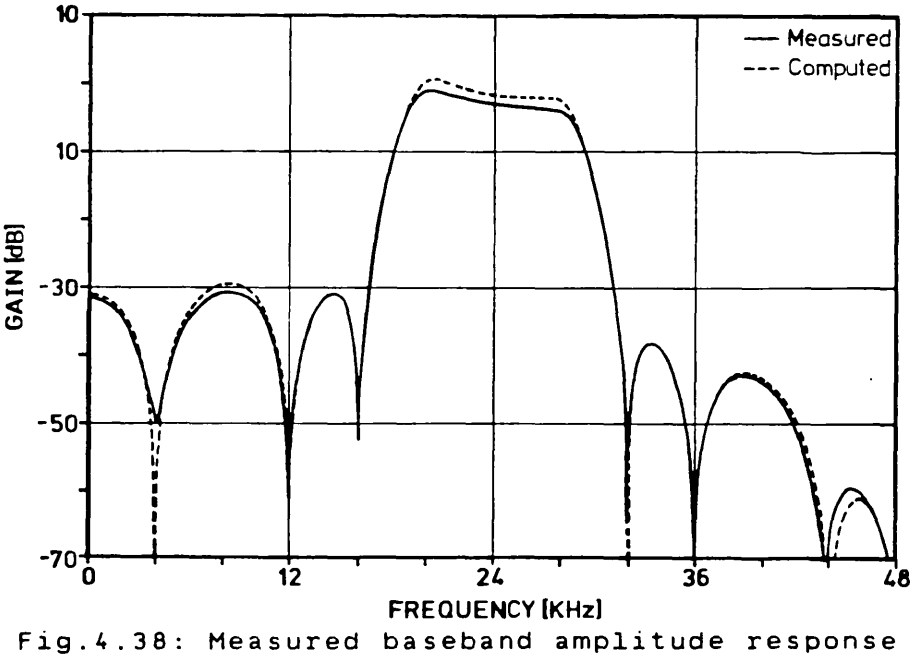


Fig.4.38: Measured baseband amplitude response of SC interpolator L=3

4.7 SUMMARY

In this Chapter we presented SC decimator and interpolator circuits which are ideally suitable for multinotch stopband approximations.

The solution of FIR SC biquads for sampling rate alteration has the advantage of simple switching schemes at the expense of a larger number of OA's. FIR SC biquads have good accuracy of the amplitude response at low frequencies, whereas at high frequencies their recursive nature renders the circuits more affected by the imperfections of the amplifiers thus reducing the speed of operation.

For increased speed of operation as well as improved accuracy of the multinotch amplitude response we adopted instead non-recursive polyphase SC structures employing only one OA per transfer function. In these structures, the desired FIR transfer function of the prototype filter for decimation or modified prototype filter for interpolation depends on the input SC branches with appropriate switch phasings. Direct-form SC polyphase structures yield a one-to-one correspondance between the input SC branches and each term of the FIR transfer function, which allows maximisation of the accuracy of the multinotch amplitude response against capacitance ratio errors and timing errors. The good performance of such direct-form SC polyphase structures was demonstrated using practical discrete component models of a single-stage SC decimator M=4 and of a cascade SC interpolator L=4. A single-stage SC interpolator L=4 showed some degradation of the accuracy of

the multinotch amplitude response, which can be explained in view of the increased complexity of the input SC branches, and the inherent higher sensitivity to capacitance ratio errors and timing errors. For applications requiring increased selectivity of the multinotch amplitude response, FIR SC polyphase structures may not be very attractive, on account of a greater sophistication of the switching schemes. Therefore, we considered alternative SC decimator and interpolator circuits which employ a combination of FIR SC polyphase structures, with reduced complexity, together with an IIR SC biquad with optimised discrete-time biquadratic transfer function.

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APPENDIX: Non-ideal effects in non-recursive SC polyphase structures

A4.1 Variability of the frequency response

The evaluation of the FIR transfer function (4.3) on the unit circle, $Z=e^{(-j\Omega)}$, gives

$$(A4.1) \ldots \quad H(j\Omega) = \sum_{n=0}^{N-1} h_n e^{-jn\Omega}$$

where $\Omega=\omega/MF_s$, for an SC decimator, and $\Omega=\omega/LF_s$ for an SC interpolator. For positive symmetry FIR transfer functions, i.e. $h_n=h_{N-1-n}$, we can write (A4.1) as [4.19]

$$(A4.2) \ldots \quad H(j\Omega) = e^{-j\frac{N-1}{2}\Omega}.H(\Omega)$$

where $H(\Omega)$ is the amplitude response. The corresponding attenuation, in decibels, is

$$(A4.3) \ldots \quad A(\Omega) = -20 \log H(\Omega) \quad dB$$

Let us consider complex variations of the nominal terms $h_n.e^{(-jn\Omega)}$ such that

$$(A4.4) \ldots \quad h_{n_a}(j\Omega) = \left(1 + \Delta h_n\right).e^{-j\Delta s_n\Omega}.h_n e^{-jn\Omega}$$

where Δh_n and Δs_n correspond to a capacitance ratio error and to a timing error, respectively. In SC polyphase structures in direct-form, Δh_n is associated with the

capacitor h_n of the input SC branches while Δs_n is associated with the time slot that produces the delay z^{-n}. A timing error may occur either due to a delay or due to an advance of the actual time slot relative to the nominal time slot, as illustrated in Fig.A4.1. Usually, such timing

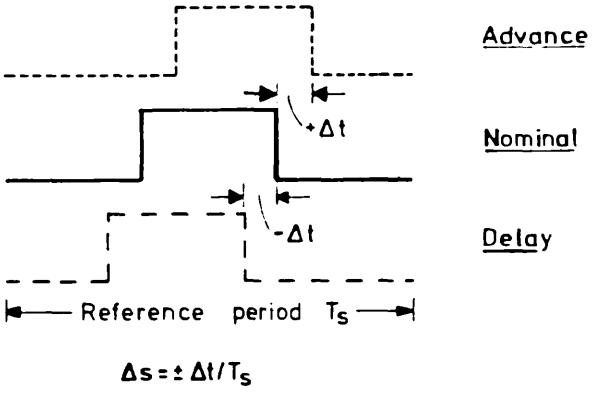


Fig.A4.1: Illustration of timing errors

error is small, i.e. $\Delta s_n << 1$, and thus we can write (A4.4) as

$$(A4.5) \ldots \qquad h_{n_a}(j\Omega) = \left(1 + \Delta h_n + j\Delta s_n \Omega\right) h_n e^{-jn\Omega}$$

where we have neglected the term $\Delta h_n . \Delta s_n << \Delta h_n, \Delta s_n$. By entering (A4.5) into (A4.1), and by using (A4.2), we obtain

$$(A4.6) \ldots \qquad H_a(j\Omega) = e^{-j\frac{N-1}{2}\Omega} . H(\Omega) + \left(\Delta h_n + j\Delta s_n \Omega\right) h_n e^{-jn\Omega}$$

The errors in the passband of the SC decimator and interpolator circuits, where $H(\Omega) \simeq 1$, are small, since $\Delta h_n << 1$, and, also $\Delta s_n << 1$. On the contrary, the errors which arise in the multinotch stopband, even if they are small, become much more important since $H(\Omega) \simeq 0$.

A4.2 Evaluation of single-stage SC decimator M=4

(a) Capacitance ratio errors

For conciseness, we shall consider now the evaluation of the single-stage SC decimator M=4 represented in Fig.4.24-a with respect to the capacitance ratio errors ($\Delta s_n=0$). An error Δh which affects all capacitance ratios at the same time, produces a frequency response in the form

$$(A4.7)\ \ldots \qquad H_a(j\Omega) = e^{-j\frac{N-1}{2}\Omega}.H(\Omega).\left(1 + \Delta h\right)$$

which indicates a mere variation of the gain of the amplitude response, while nominal notch frequencies are preserved. This is a feature of the implementation in direct-form.

Another feature of the SC polyphase structure in direct-form is that the capacitance ratios associated with the input SC branches replicate the symmetry of the FIR impulse response, i.e. capacitance ratio errors corresponding to symmetric FIR coefficients are equal. For an error Δh of two such symmetric capacitance ratios, i.e. $h_n=h_{N-1-n}$, the actual frequency response (A4.6) can be written as

(A4.8) ...

$$H_a(j\Omega) = e^{-j\frac{N-1}{2}\Omega}.H(\Omega) + \Delta h.h_n.e^{-jn\Omega} + \Delta h.h_{N-1-n}.e^{-j(N-1-n)\Omega}$$

yielding

$$(A4.9)\ \ldots \quad H_a(j\Omega) = e^{-j\frac{N-1}{2}\Omega}.\left\{H(\Omega) + 2\Delta h.h_n\cos\left[\left(n - \frac{N-1}{2}\right)\Omega\right]\right\}$$

At the nominal notch frequencies, $H(\Omega)=0$, the finite attenuation provided by the SC decimator will be

$$(A4.10)\ \ldots\quad A(\Omega)\Big|_{\text{Notches}} = -20\log\left\{2\Delta h.h_n\cos\left[\left(n-\frac{N-1}{2}\right)\Omega\right]\right\}$$

The periodic error $h_n.\cos[(n-(N-1)/2).\Omega]$ is plotted in Fig.A4.2, for the pairs of capacitors in the SC decimator

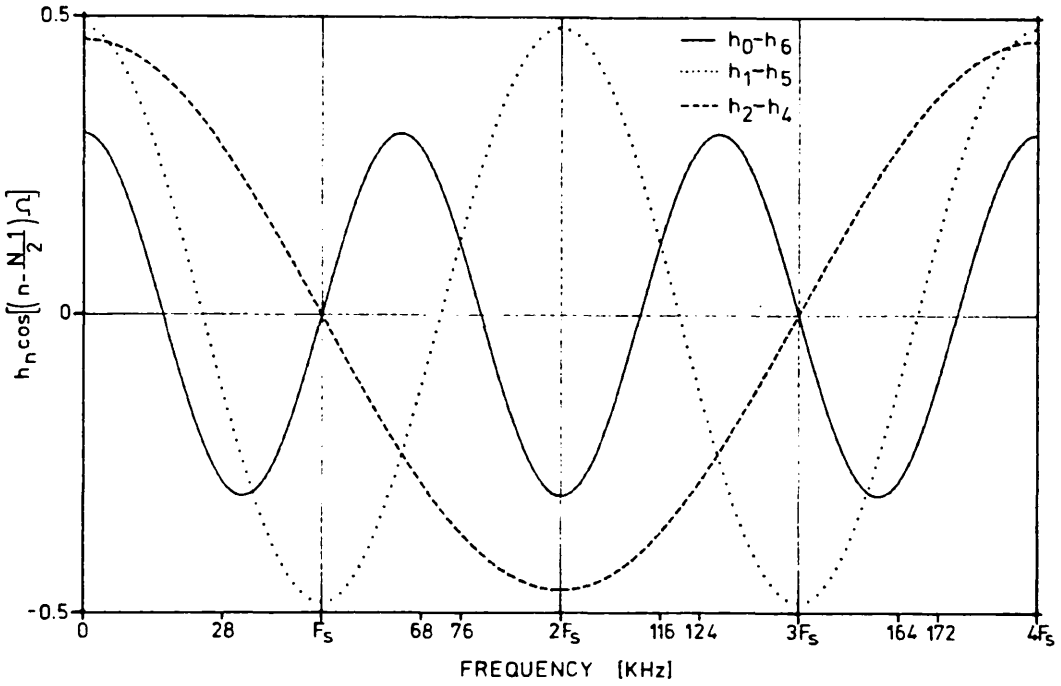
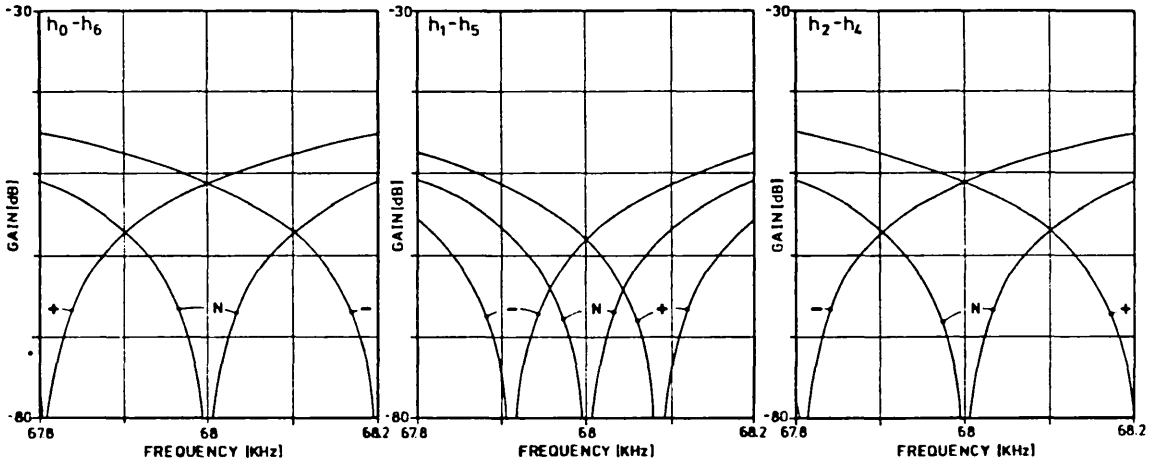


Fig.A4.2: Periodic errors associated with the pairs of capacitors h_0-h_6, h_1-h_5, and h_2-h_4, in the single-stage SC decimator M=4

of Fig4.24-a with equal capacitance values, i.e. h_0-h_6, h_1-h_5, and h_2-h_4. Since these periodic errors are real quantities, they produce deviations of the nominal notch frequencies, as shown in Fig.A4.3. These curves were obtained by simulation of the SC decimator using the SWITCAP program, considering variations of ±0.5% for the

capacitor-pairs with equal capacitance values.



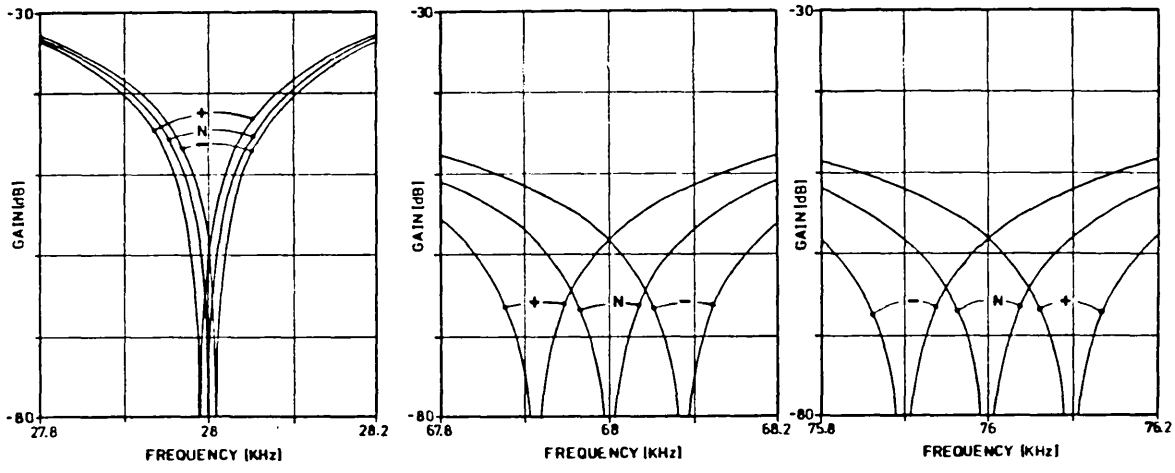
N - nominal amplitude response

Fig.A4.3: Computer simulated amplitude responses of the SC decimator M=4, around notch frequency at 68KHz, for ±0.5% variations of equal capacitors corresponding to symmetric impulse response coefficients

The capacitance ratio associated with the capacitor h_3 in the SC decimator M=4 is a special case of the above situation, since it corresponds to the coefficient at the centre of symmetry of the FIR impulse response. The actual frequency response for an error Δh in h_3 becomes

$$H_a(j\Omega) = e^{-j3\Omega}.\left[H(\Omega) + \Delta h.h_3\right] \qquad \text{(A4.11)} \ \ldots$$

Since the error term $\Delta h.h_3$ is a real constant quantity, the variation of the notch frequencies will be symmetrical around their nominal values, as we can see in Fig.A4.4.



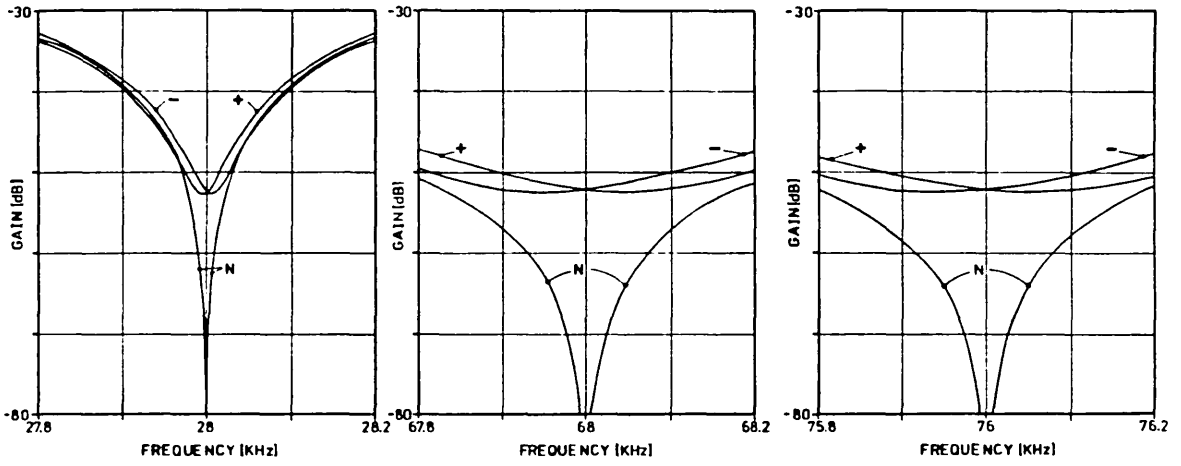
N - nominal amplitude response

Fig.A4.4: Computer simulated amplitude response of the SC decimator M=4, around notch frequencies at 28KHz, 68KHz, and 76KHz, for ±0.5% variation of capacitor h_3

Capacitance ratio errors Δh associated with each capacitor h_n ($n \neq 3$) imply complex error functions which lead to amplitude responses with finite, rather than infinite, attenuation in the vicinity of the nominal notch frequencies. The attenuation at the nominal notch frequencies is given by

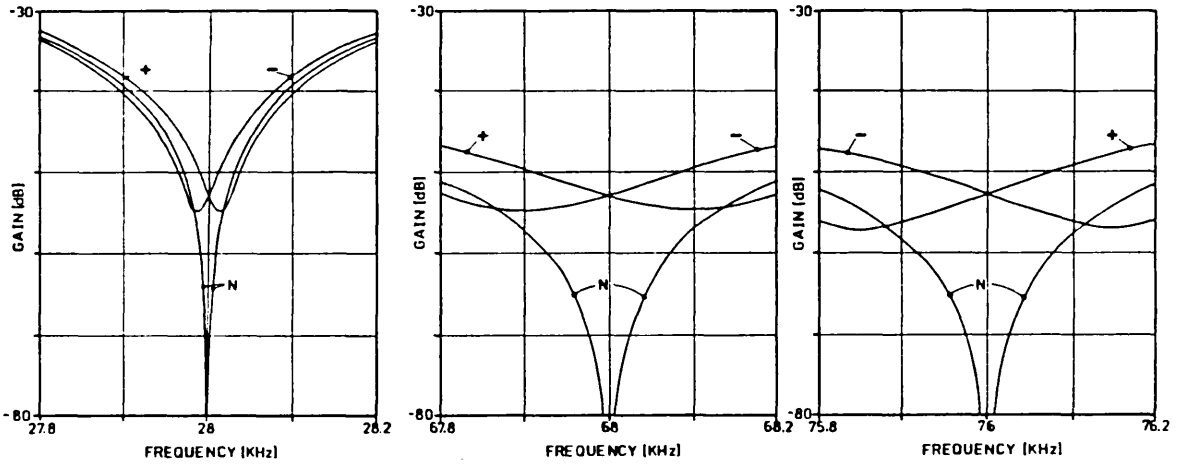
$$A(\Omega)\Big|_{\text{Notches}} = -20 \log\left(\Delta h . h_n\right) \qquad \text{(A4.12) ...}$$

The variation of the amplitude response of the SC decimator around some of the notch frequencies is shown in Fig.A4.5, which were obtained considering variations of ±0.5% of the nominal capacitance values of the input capacitors.



N - nominal amplitude response

capacitor h_1, and capacitor h_5



N - nominal amplitude response

capacitor h_2, and capacitor h_4

Fig.A4.5: Computer simulated amplitude responses of the SC decimator M=4, around notch frequencies at 28KHz, 68KHz, and 76KHz, for ±0.5% variation of single capacitors ($\neq h_3$)

(b) Timing errors

Each polyphase filter of an SC polyphase structure in direct-form is assigned only one sampling slot for decimation, and only one charge transfer slot for

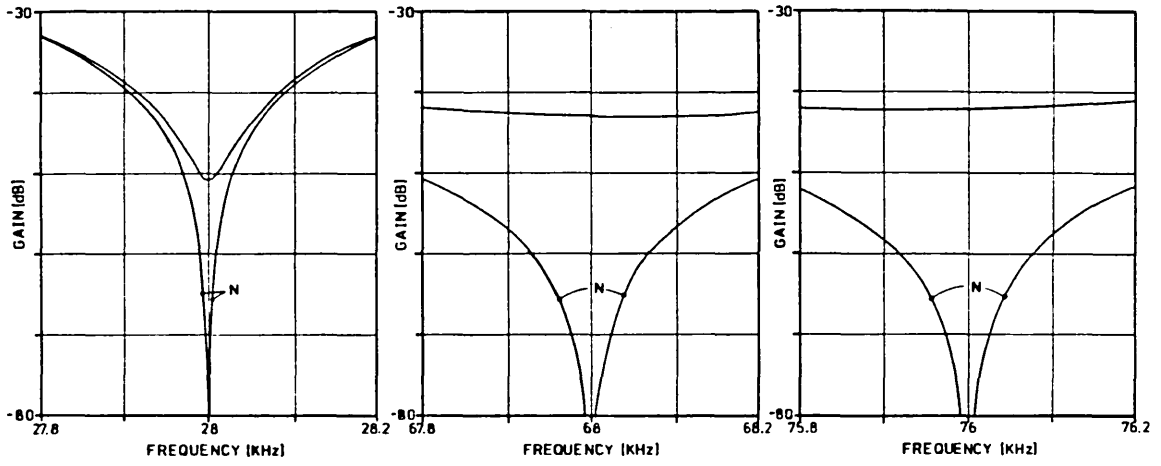
interpolation. Therefore, one such slot affects the timing of all the terms of the corresponding polyphase filter. In the SC decimator M=4 in Fig.4.24-a, with the time frame in Fig.4.24-b, the simplest situation for analysis of timing errors is for slot 3, since it corresponds to a polyphase filter with only one term. For a relative timing error Δs_3, the actual frequency response in (A4.6) becomes

$$(A4.13) \quad \ldots \qquad H_a(j\Omega) = e^{-j3\Omega}.\left[H(\Omega) + j\Delta s_3.h_3.\Omega\right]$$

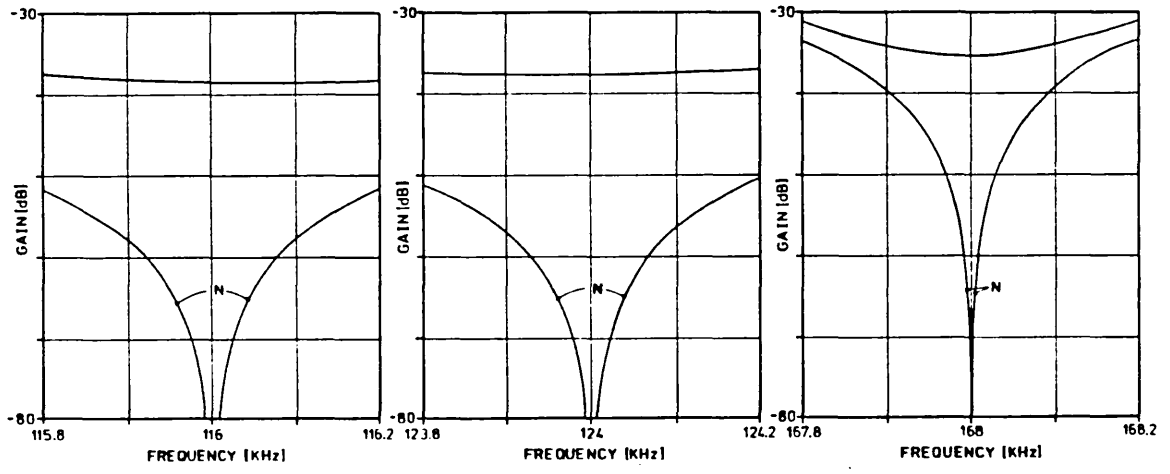
At the nominal notch frequencies, $H(\Omega)=0$, the attenuation is given by

$$(A4.14) \quad \ldots \qquad A(\Omega)\Big|_{\text{Notches}} = -20 \log\left(\Delta s_3.h_3.\Omega\right)$$

which indicates an error variation which increases with frequency. Therefore, the attenuation around the notches at higher frequencies becomes much more critical. This effect can be observed in the curves of Fig.A4.6, which were obtained considering an advance of 65.1ns of slot 3, i.e. 1/80 of the unit delay period 1/192KHz.



N - nominal amplitude response



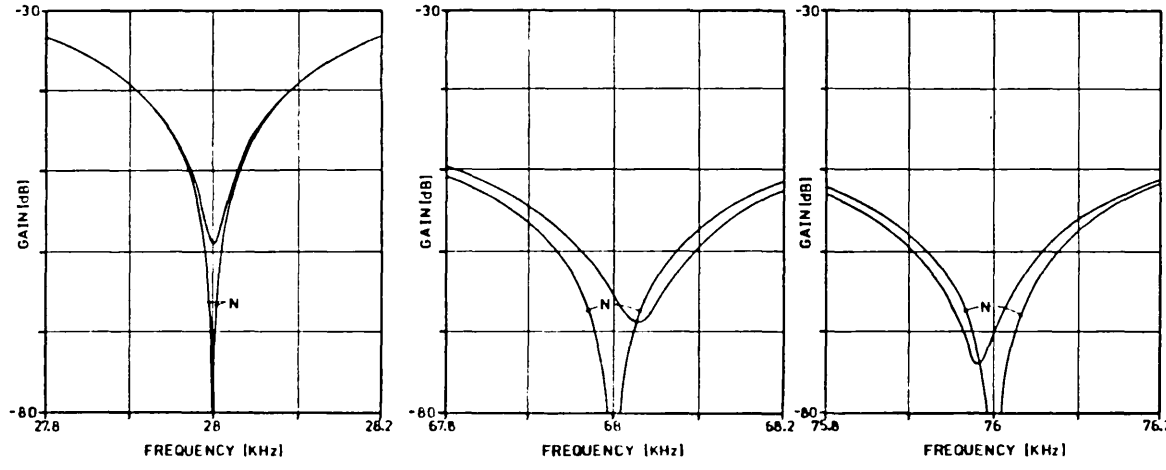
N - nominal amplitude response

Fig.A4.6: Computer simulated amplitude responses of the SC decimator M=4, around notch frequencies at 28KHz, 68KHz, 76KHz, 116KHz, 124KHz, and 168KHz, for 65.1ns advance of time slot 3

(c) Amplifier DC gain

The nonideal characteristics of the OA affect the performance of the SC polyphase structures by preventing complete transfer of charge from both the input and the feedback SC branches to the feedback capacitor of the OA. The effect of finite DC gain, for example, can be viewed as

yielding errors of the capacitance ratios associated with the input SC branches. Ideally, the feature of parallel processing of the polyphase structures would make the performance of the circuit immune to such errors whose effect would then correspond merely to a variation of the gain of the amplitude response. The deviations that can be observed also with respect to the variability of the multinotch characteristic, result from the fact that the voltage at the negative input terminal of the amplifier depends, at each time, on the output voltage of the amplifier. Therefore, the conditions of charge transfer are not the same for all the input SC branches. Nevertheless, the overall effect is low, as we can see from the results given in Fig.A4.7, corresponding to the simulation, using the SWITCAP program, of the SC decimator M=4 with a DC gain of 500 for the OA.



N - nominal amplitude response

Fig.A4.7: Computer simulated amplitude responses of the SC decimator M=4, around notch frequencies at 28KHz, 68KHz, and 76KHz, considering a finite DC gain of 500 for the amplifier

A4.3 Clock Feedthrough

The problem of clock feedthrough in the polyphase SC decimator M=4 results from the parasitic capacitances which are connected between the control terminals of the switches and the negative terminal of the OA, as shown in Fig.A4.8-a. Such parasitic capacitances produce an injection of charge into the feedback capacitor whose main effect is to

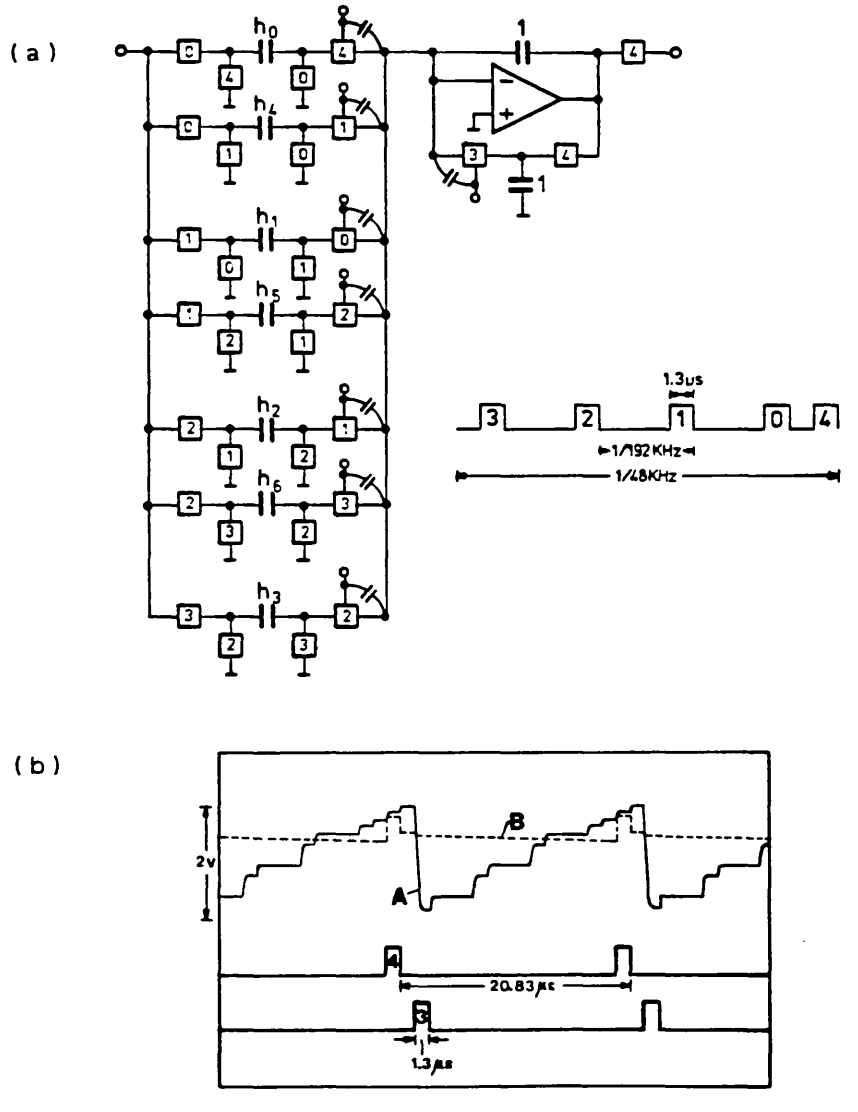


Fig.A4.8: (a) Parasitic capacitances associated with the control terminals which contribute to clockfeedthrough; (b) Waveforms in the SC decimator M=4, with zero input voltage

produce an offset voltage at the output of the amplifier, as shown in the waveforms of Fig.A4.8-b, obtained with zero input voltage. Waveform A shows the charge accumulation during one reference period of the SC decimator, and waveform B shows the sampled DC output voltage. The DC output voltage reduces the signal handling capability of the circuit and it may also prevent the realisation of cascade structures with many sections. However, in such cases, we can employ schemes that are available for reduction of the clock feedthrough in SC networks (e.g. [4.20]).

A4.4 Fast Reset Schemes for SC Decimators

In the waveform A shown in Fig.A4.8-b, we can see that the amplifier output voltage is reset to zero voltage, in slot 3. This reset operation produces a large output voltage swing, which is affected, primarily, by the finite slew rate of the amplifier. In the case of the SC decimator circuits, where the SC accumulator operates at lower rate F_s, it is possible to implement reset schemes which make an efficient use of the many time slots of the time frame, in order to reduce the voltage swing at the output of the OA [4.21]. An example of such a reset scheme is illustrated in Fig.A4.9-a. The chain of TSC branches in the feedback network provide the reset of the output voltage in various phases, each of which produces much smaller output voltage swings, as shown in Fig.A4.9-b.

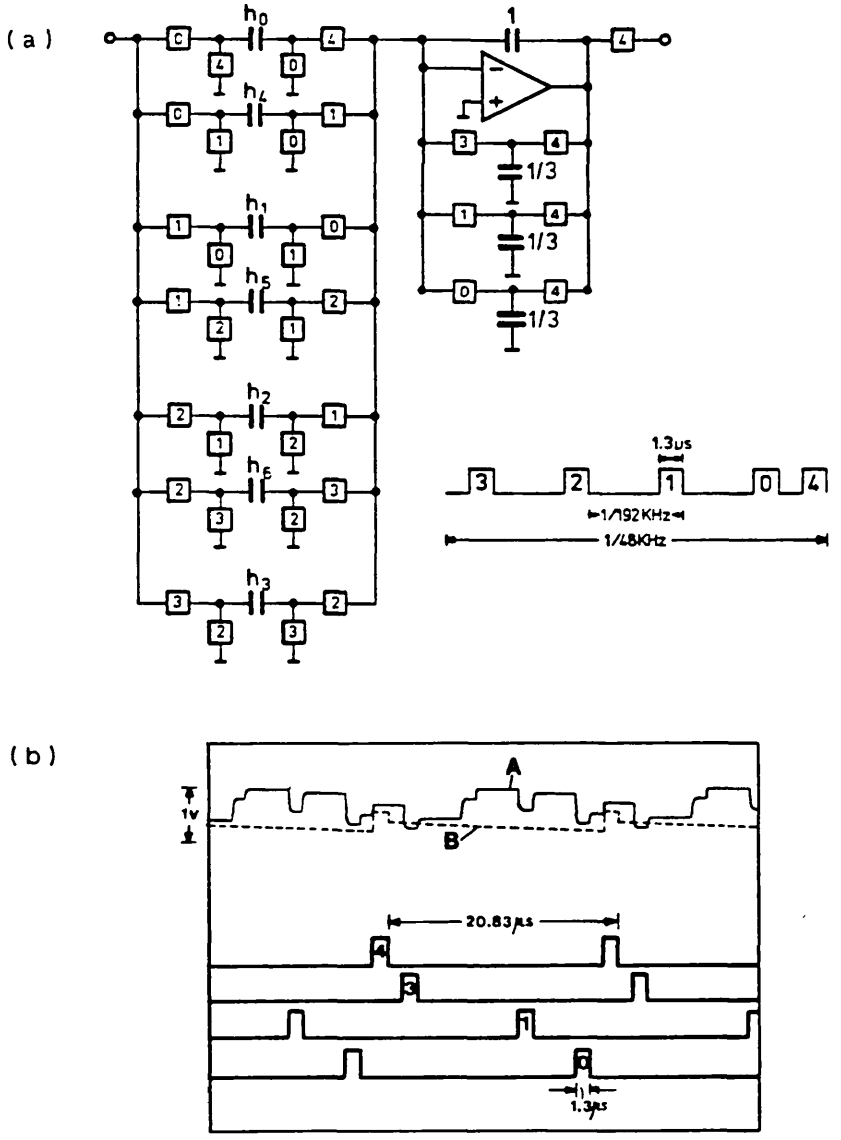


Fig.A4.9: (a) Fast reset scheme using a chain of three TSC feedback branches; (b) Waveforms showing reduced output voltage swing during the three reset slots 3, 1, and 0

CHAPTER 5

DESIGN AND EVALUATION OF SC BANDPASS FILTER SYSTEMS WITH BASEBAND AND FREQUENCY-TRANSLATED OPERATING MODES

5.1 INTRODUCTION

This Chapter is concerned with the practical realisation of SC bandpass filter systems with narrow relative bandwidths between 10% and 1%, and with very narrow relative bandwidths below 1%, and which embody the ideas and circuits presented previously.

For bandpass responses with relative bandwidths between 10% and 1%, we propose an SC bandpass filter system operating in a baseband filtering mode, with optimised capacitance spread, and suitable decimators and interpolators for rejection of unwanted frequency-translated components. The SC bandpass filter in the system, considered in Section 5.2, is designed using the concept of optimum switching frequency introduced in Section 3.6, leading to absolute minimum capacitance spread, thus minimising capacitance ratio errors and maximising the accuracy of the amplitude response. The low value of the optimum switching frequency gives rise to unwanted alias and image frequency-translated components at low frequencies, which have to be attenuated using an Anti-Aliasing Filter (AAF) and an Anti-Imaging Filter (AIF), respectively, with increased selectivity. Hence, in Section 5.3, we consider FIR SC lowpass decimators and interpolators, respectively, which are optimally designed in order to maximise the rejection of those unwanted alias and image signals which can not be attenuated by low-selectivity continuous-time filters. A practical discrete component model of the complete SC bandpass filter system

is experimentally evaluated.

For the realisation of bandpass responses with very narrow relative bandwidths of less than 1%, we propose Single-Path Frequency-Translated (SPFT) SC bandpass filter systems. These systems also employ an SC bandpass filter with optimised capacitance spread, together with more sophisticated AAF and AIF with bandpass responses. As it is experimentally demonstrated, the dynamic range of SPFT systems is similar to that of the conventional SC bandpass filter employed in the system, which has a much wider relative bandwidth, thus offering a solution for very high selectivity filtering applications requiring high dynamic range. The design, implementation, and experimental evaluation of SPFT systems for very narrow bandpass filtering applications, constitute the core of this Chapter, from Section 5.4 to Section 5.7.

Firstly, in Section 5.4, we examine the selectivity requirements of the bandpass AAF and AIF in SPFT systems, as well as the implications concerning the factor of sampling rate alteration of the SC decimator and interpolator in such systems. Alternative architectures for decimation and interpolation in SPFT systems are then discussed in Sections 5.5, 5.6, and 5.7, employing different types of SC circuits with FIR and IIR transfer functions. Such architectures are compared with respect to capacitance spread and total capacitor area required for implementation, operating speed, and degree of rejection of the unwanted alias and image signals with acceptable system

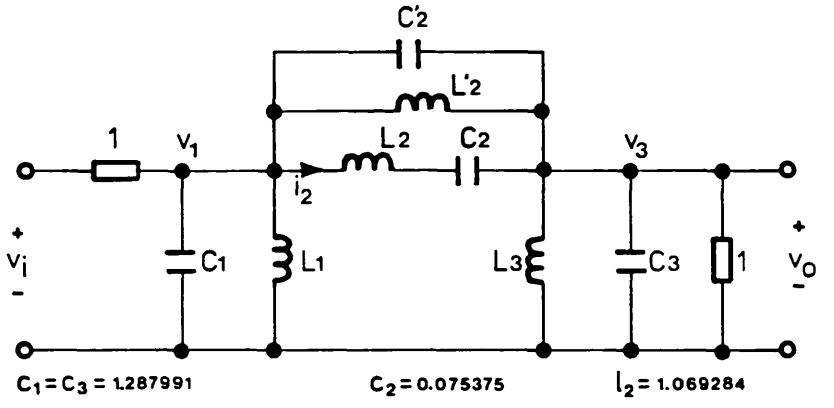
complexity. Practical discrete component models of SPFT systems are also considered for experimental evaluation.

Finally, in Section 5.8, we demonstrate further applications of SPFT systems, which include filtering with programmable Q-factor, and also Single Sideband (SSB) generation and detection. In Section 5.9 we present a summary of the Chapter.

5.2 DESIGN AND EVALUATION OF AN SC BANDPASS FILTER

5.2.1 Coupled SC biquad structure

At the heart of the SC filter systems that we shall describe in this Chapter there is a 6th. order elliptic SC bandpass filter derived by operational simulation of the LCR ladder prototype filter shown in Fig.5.1, using the bilinear s̃-to-Z transformation [5.1]. The bandpass ladder



$C_1 = c_1/2\pi\tilde{f}_0\tilde{B}$ $\quad L_1 = (1/c_1).(\tilde{B}/2\pi\tilde{f}_0)$

$C_2 = (1/l_2).(\tilde{B}/2\pi\tilde{f}_0)$ $\quad L_2 = l_2/2\pi\tilde{f}_0\tilde{B}$

$C'_2 = c_2/2\pi\tilde{f}_0\tilde{B}$ $\quad L'_2 = (1/c_2).(\tilde{B}/2\pi\tilde{f}_0)$

$C_3 = c_3/2\pi\tilde{f}_0\tilde{B}$ $\quad L_3 = (1/c_3).(\tilde{B}/2\pi\tilde{f}_0)$

Fig.5.1: 6th. order elliptic LCR ladder bandpass prototype filter

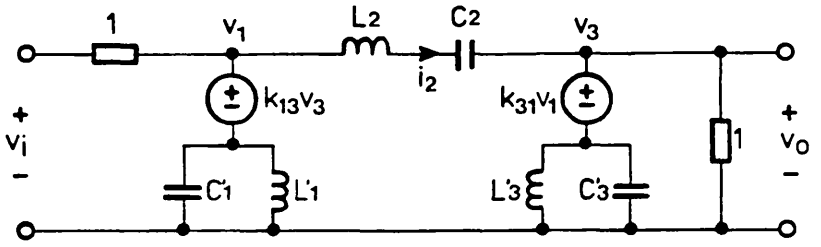
prototype filter is obtained by the lowpass-to-bandpass transformation from the lowpass filter type CO3/25/19 (passband ripple of 0.28dB and minimum stopband attenuation of 40dB) [5.2]. The bilinear prewarped midband frequency $\tilde{f}_o$ and passband relative bandwidth $\tilde{B}$ are obtained from

$$(5.1\text{-a}) \quad \ldots \quad \tilde{f}_o = \frac{F_s}{\pi}\left[\tan\frac{\pi fp2}{F_s} \cdot \tan\frac{\pi fp1}{F_s}\right]^{1/2}, \quad f_o = \left[fp_1 . fp_2\right]^{1/2}$$

and

$$(5.1\text{-b}) \quad \ldots \quad \tilde{B} = \frac{F_s}{\pi}\,\frac{\tan(\pi fp2/F_s)-\tan(\pi fp1/F_s)}{\tilde{f}_o}, \quad B = \frac{fp2-fp1}{f_o}$$

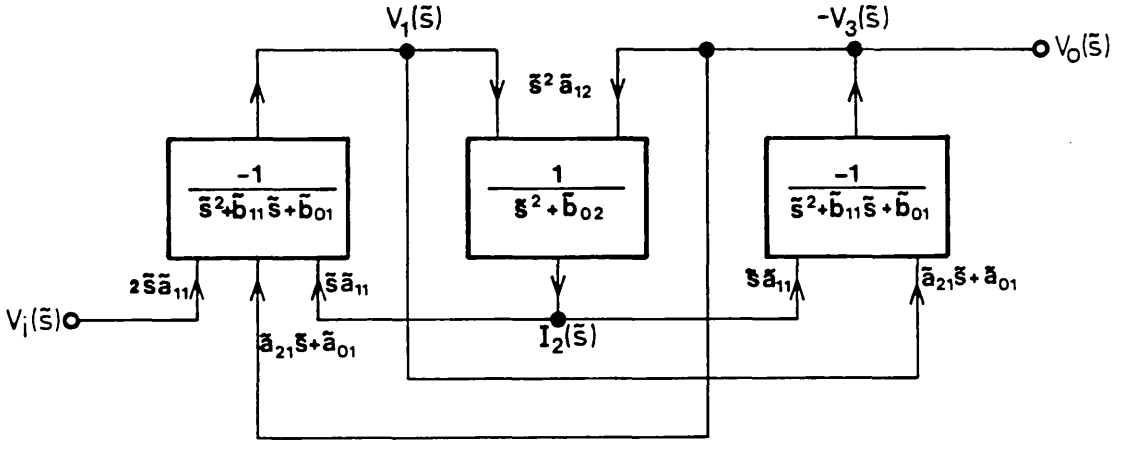
where f_{p1} and f_{p2} are the edges of the passband of the SC bandpass filter for maximum ripple 0.28dB. The desired midband frequency and relative bandwidth are f_o=20KHz and B=2%, respectively, and the corresponding -3dB bandwidth is BW=480Hz [5.2]. A modification of the original ladder in Fig.5.1 is required in order to remove the capacitive and inductive loops formed by the capacitors C_1-C'_2-C_3 and inductors L_1-L'_2-L_3, respectively, and which may give rise to DC instability [5.3]-[5.5]. By applying Thevenin's theorem to the parallel resonant branches $L_1//C_1$, $L'_2//C'_2$ and $L_3//C_3$ having the same resonant frequency, i.e. $L_1.C_1=L'_2.C'_2=L_3.C_3$, the modified circuit of Fig.5.2-a results, with two Voltage Controlled Voltage Sources (VCVS). It was observed by computer simulation analysis [5.6] that the characteristics of the modified circuit with



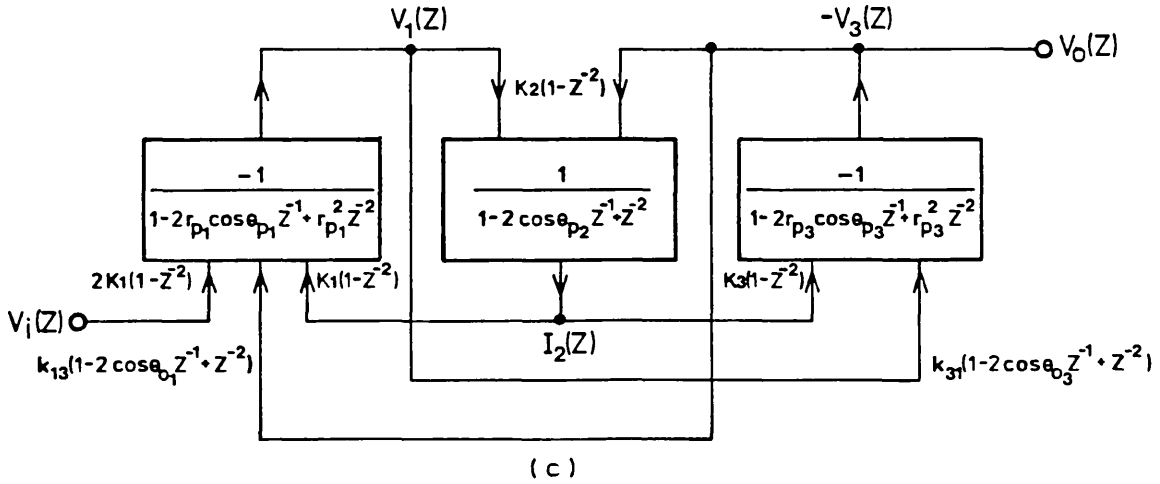
$k_{13}=C'_2/(C_1+C'_2)$ $\quad C'_1=C_1+C'_2$ $\quad L'_1=L_1.L'_2/(L_1+L'_2)$

$k_{31}=C'_2/(C_3+C'_2)$ $\quad C'_3=C_3+C'_2$ $\quad L'_3=L_3.L'_2/(L_3+L'_2)$

(a)



(b)



(c)

Fig.5.2: (a) Modified LCR prototype filter; (b) Continuous-time operational block diagram; (c) Bilinear discrete-time block diagram

respect to the variation of the passband response with variations of the component values are similar to those of the original LCR ladder prototype filter. On the one hand, variations of the transmission gain factors of the VCVS, which determine the transmission zeroes of the amplitude response, do not affect the response of the filter in the passband. On the other hand, the passband variability with respect to the shunt capacitors and inductors is only slightly higher than in the original LCR prototype filter, whereas variations of the series capacitor and inductor produce the same variations of the passband as in the original LCR ladder prototype. In the modified circuit in Fig.5.2-a, the nodal voltages $V_1(\tilde{s})$ and $V_3(\tilde{s})$ and the branch current $I_2(\tilde{s})$ can be expressed as

$$(5.2\text{-a}) \quad V_1(\tilde{s}) = \frac{-1}{\tilde{s}^2 L_1' C_1' + \tilde{s} L_1' + 1} \left\{ \tilde{s} L_1' \left[-V_i(\tilde{s}) \right] + \tilde{s} L_1' I_2(\tilde{s}) + k_{13} \left(\tilde{s}^2 L_1' C_1' + 1 \right) \left[-V_3(\tilde{s}) \right] \right\}$$

$$(5.2\text{-b}) \quad I_2(\tilde{s}) = \frac{1}{\tilde{s}^2 L_2 C_2 + 1} \left\{ V_1(\tilde{s}) + \left[-V_3(\tilde{s}) \right] \right\}$$

$$(5.2\text{-c}) \quad -V_3(\tilde{s}) = \frac{-1}{\tilde{s}^2 L_3' C_3' + \tilde{s} L_3' + 1} \left[\tilde{s} L_3' I_2(\tilde{s}) + k_{31} \left(\tilde{s} L_3' C_3' + 1 \right) V_1(\tilde{s}) \right]$$

leading to the block diagram realisation shown in Fig.5.2-b. The gain factor of two in the input branch is required in order to obtain OdB gain at midband frequency. After applying the bilinear $\tilde{s}$-to-Z transformation to the block diagram in Fig.5.2-b, we obtain the corresponding discrete-time realisation given in Fig.5.2-c. Each section

of this block diagram is implemented using SC biquads with multiple input branches corresponding to different quadratic numerator functions. Such SC biquads, derived from Chapter 3, are shown in Fig.5.3-a. The terminating SC

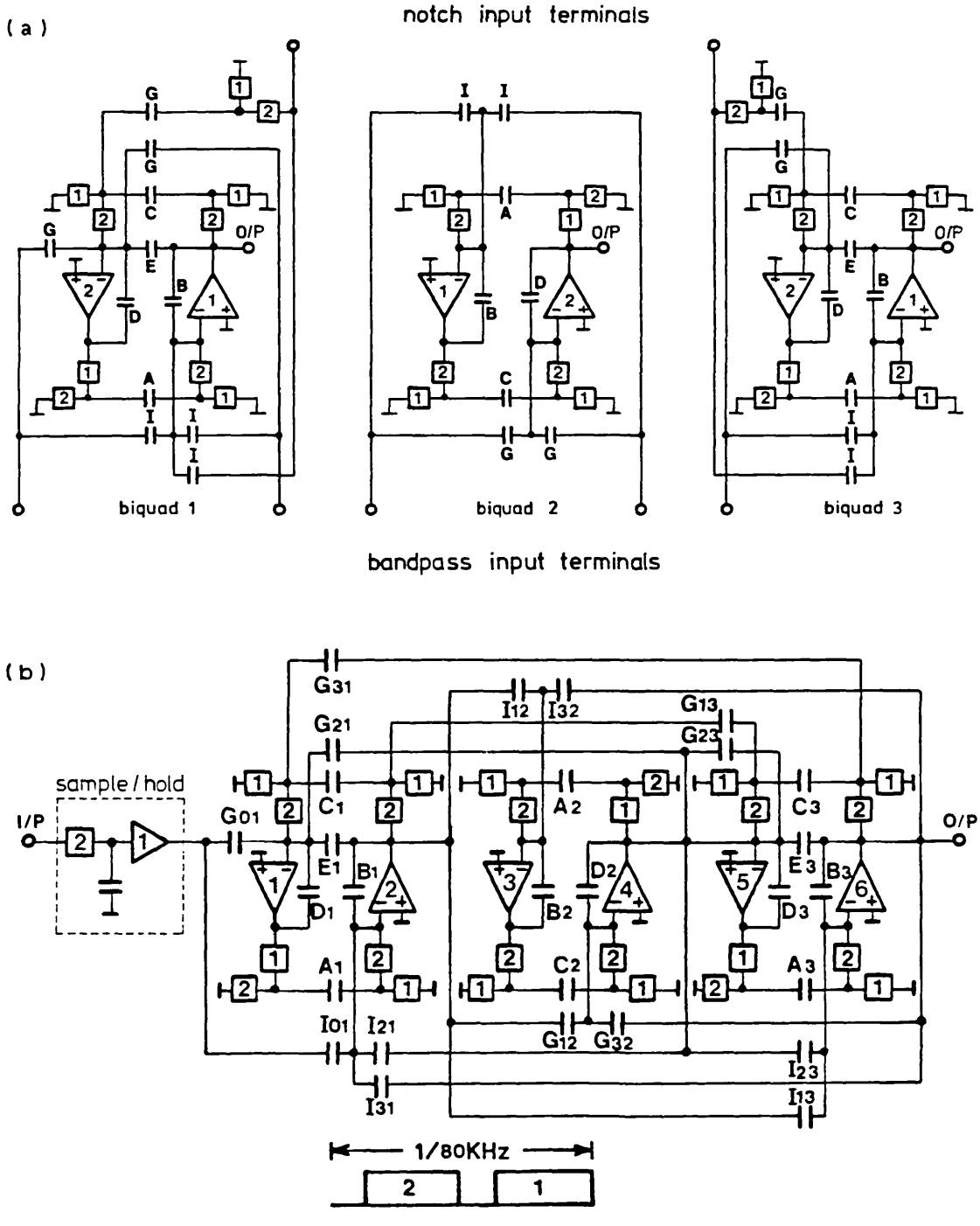


Fig.5.3: (a) SC biquads with multiple input terminals; (b) SC Coupled biquad bandpass filter with Type-B switching

biquads 1 and 3, with E-damping, and output terminal from OA1, implement bandpass and notch transfer functions with negative gain factors. The undamped resonator SC biquad 2, with output terminal from OA2, implements bandpass transfer functions with positive gain factors. The complete coupled SC biquad structure is shown in Fig.5.3-b, where the output voltages of the SC biquads simulate the discrete-time variables $V_1(Z)$, $I_2(Z)$ and $V_3(Z)$ of the block diagram in Fig.5.2-c. As we shall see later on, the adoption of Type-B switching may be advantageous for interfacing the SC filter with other SC circuits in a complete filter system, in which case the input sample and hold circuit may be eliminated.

5.2.2 Design with optimum switching frequency yielding minimum capacitance spread

By employing the strategy for capacitance spread analysis described in Chapter 3, we find that the maximum capacitance spread in the SC filter arises in the terminating biquads in realising the bandpass inputs. This spread is minimised by designing the SC filter with the optimum switching frequency

(5.3) ... $$F_{s_{opt.}} = 4f_o = 80KHz$$

giving the normalised capacitance values in Table 5.1.

	BIQUAD 1		BIQUAD 2		BIQUAD 3	
ICS-1	A_1	87.796	A_2	68.075	A_3	87.796
	B_1	87.796	B_2	34.037	B_3	87.796
	I_{01}	2	I_{12}	1	I_{13}	4.798
	I_{21}	1	I_{32}	1	I_{23}	1
	I_{31}	4.798				
ICS-2	C_1	86.787	C_2	68.075	C_3	86.787
	D_1	43.898	D_2	68.075	D_3	43.898
	E_1	1	G_{12}	1	E_3	1
	G_{01}	2	G_{32}	1	G_{13}	4.798
	G_{21}	1			G_{23}	1
	G_{31}	4.798				
C-spread		87.796		68.075		87.796
Total C		322.873		242.262		318.873
C-spread = 87.796 Total C =884.008						

Table 5.1: Normalised capacitance values for the SC bandpass filter with optimum switching frequency

The maximum capacitance spread is 87.8, and the total normalised capacitance is 884. As discussed in Section 3.6, the adoption of the optimum switching frequency produces an internal voltage magnification of 3dB in the terminating SC biquads. In order to determine the voltage magnifications which arise at the output of all the OA's, we have to carry-out a computer simulation analysis [5.7] of the complete coupled SC biquad structure. The results, given in Fig.5.4, indicate a maximum voltage magnification

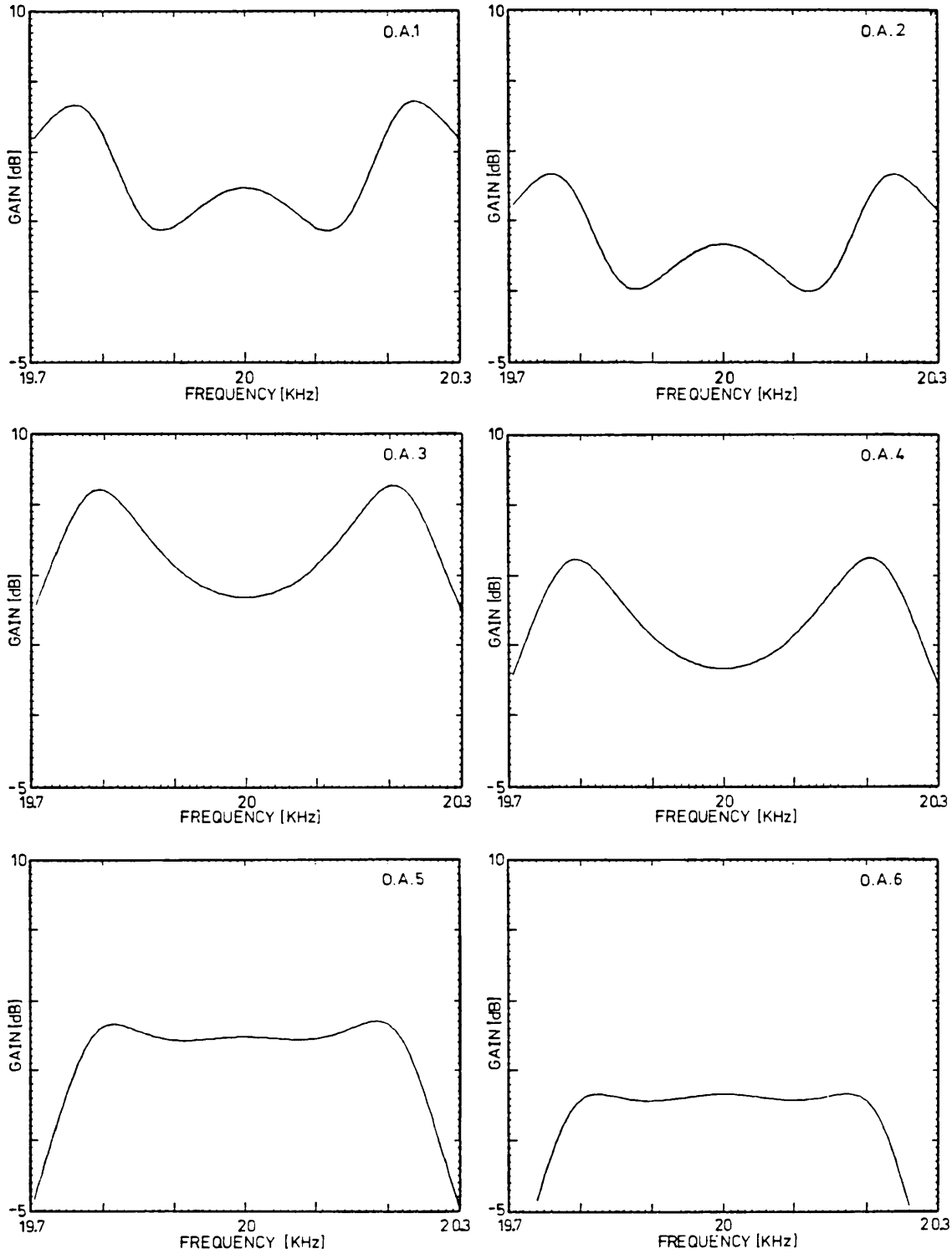


Fig. 5.4: Computer simulated voltage magnifications at the output of the amplifiers

of about 8dB at the output of OA3. A fully voltage scaled design of this filter would have yielded an increased maximum capacitance spread of 151.1, and total normalised capacitance of 1002.3. In view of the stringent requirements with respect to the accuracy of the capacitance ratios in the SC filter, which we shall examine next, we adopted the solution with minimum capacitance spread. This implies a reduction of 8dB of the signal handling capability of the SC filter.

5.2.3 Evaluation by computer simulation

The nominal overall amplitude response of the SC bandpass filter is plotted in Fig.5.5-a, together with the nominal amplitude response of the original LCR ladder prototype with a gain shift of +6.02dB. Because of the bilinear s̃-to-z transformation, the transmission zeroes at infinity in the continuous-time domain yield transmission zeroes at half the switching frequency in the discrete-time domain, and thus the selectivity of the upper stopband of the SC filter is increased. On the other hand, the warping effect of the bilinear transformation leads to a slight expansion of the lower stopband compared to the original LCR ladder filter. The passband amplitude responses in Fig.5.5-b show that the SC filter preserves the equiripple characteristic of the LCR ladder prototype filter, and thus will have similar sensitivity properties.

The variability of the passband amplitude response of the SC bandpass filter was evaluated by means of a computer simulation analysis using SCNAP program [5.7], where we

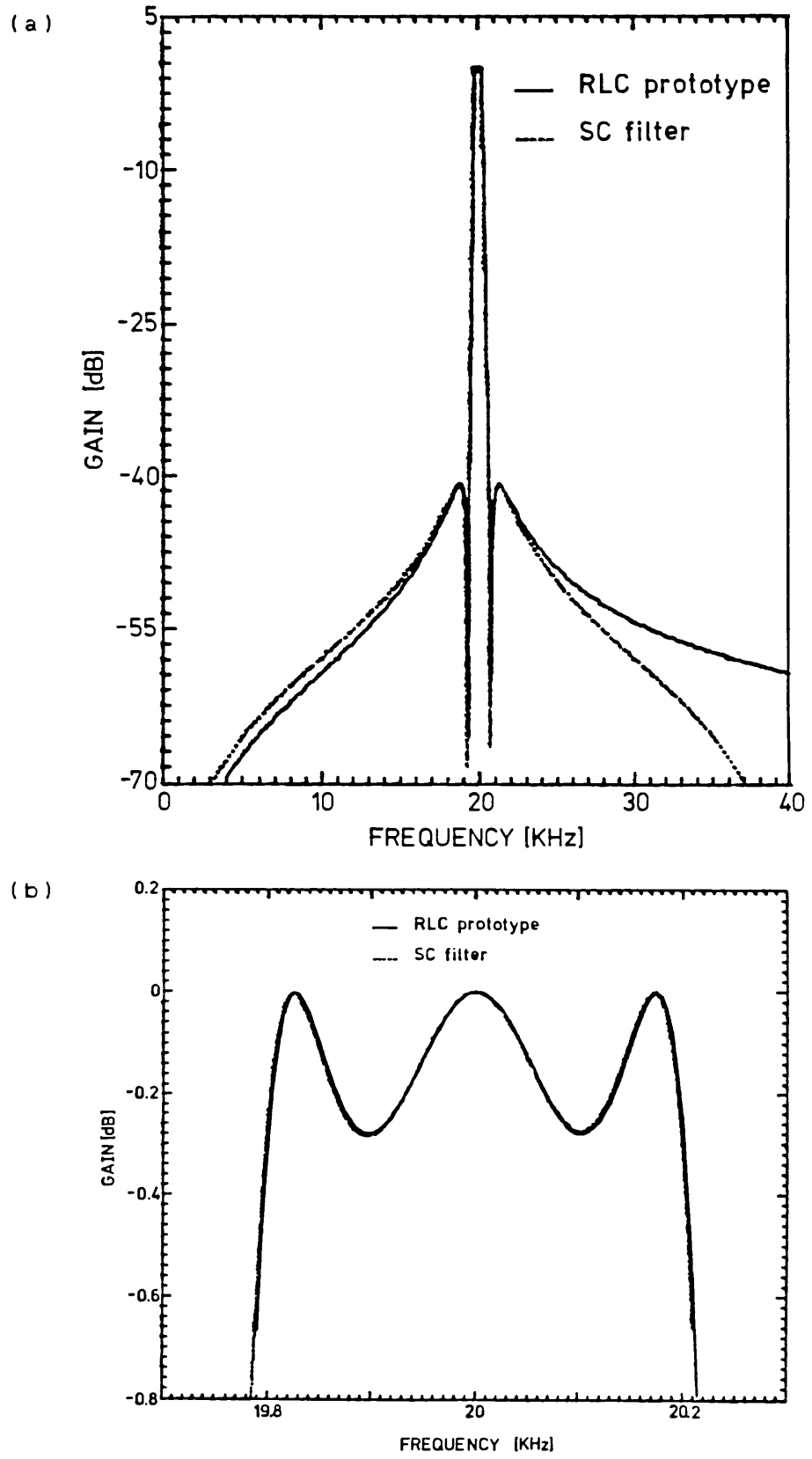


Fig.5.5: Computer simulated (a) overall, and (b) passband, nominal amplitude responses of the SC filter, and of the LCR prototype ladder filter

changed by ±0.25% the nominal capacitance values of each capacitor in the circuit. The critical capacitors in the SC filter are the capacitors A, B, C, and D, in the loop of each SC biquad, which determine the corresponding pole frequency. As we can see in Fig.5.6, such capacitors produce variations of the passband ripple of the SC filter of the order of 2.4dB for 1% variation of the corresponding capacitance values, which are similar to the variations produced by the reactive components in the original LCR ladder prototype filter, and modified prototype filter.

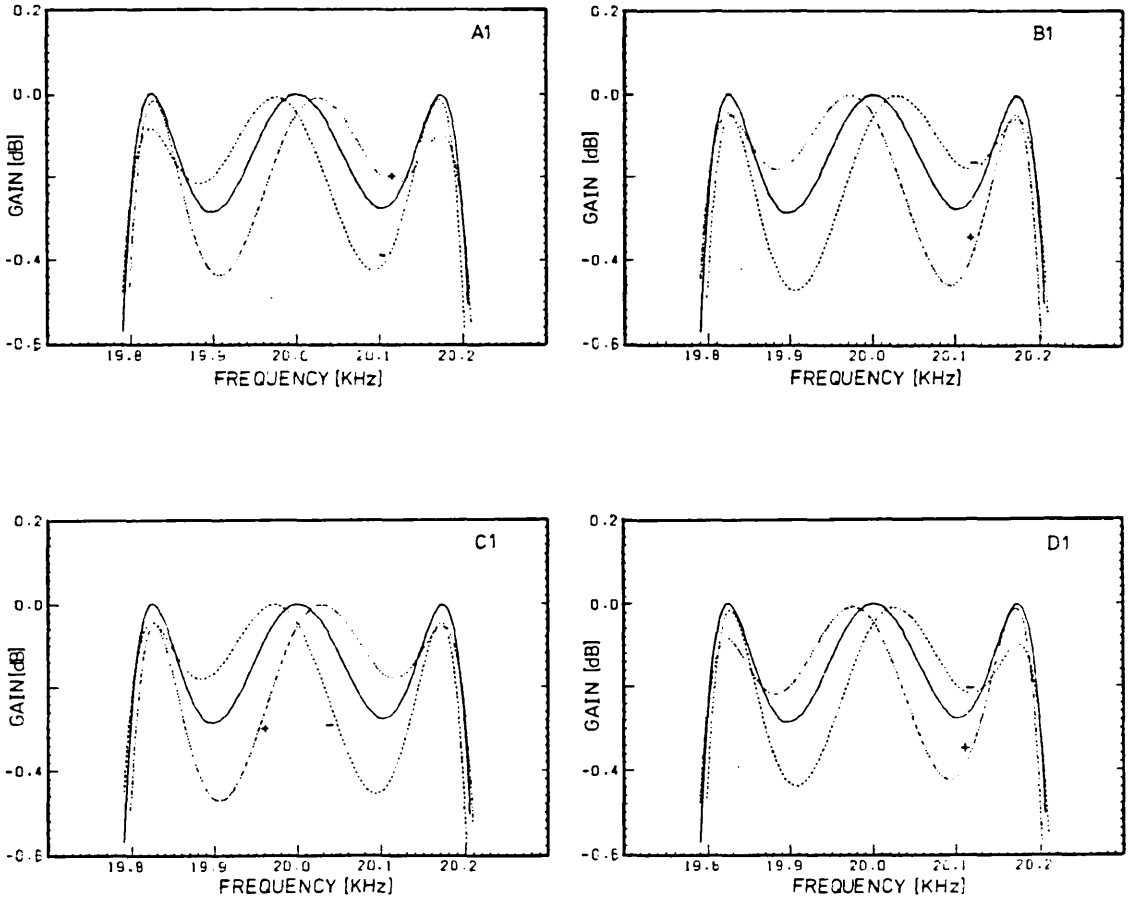


Fig.5.6: Computer simulated analysis of the passband variability of the SC bandpass filter (±0.25% variation of the capacitance values)

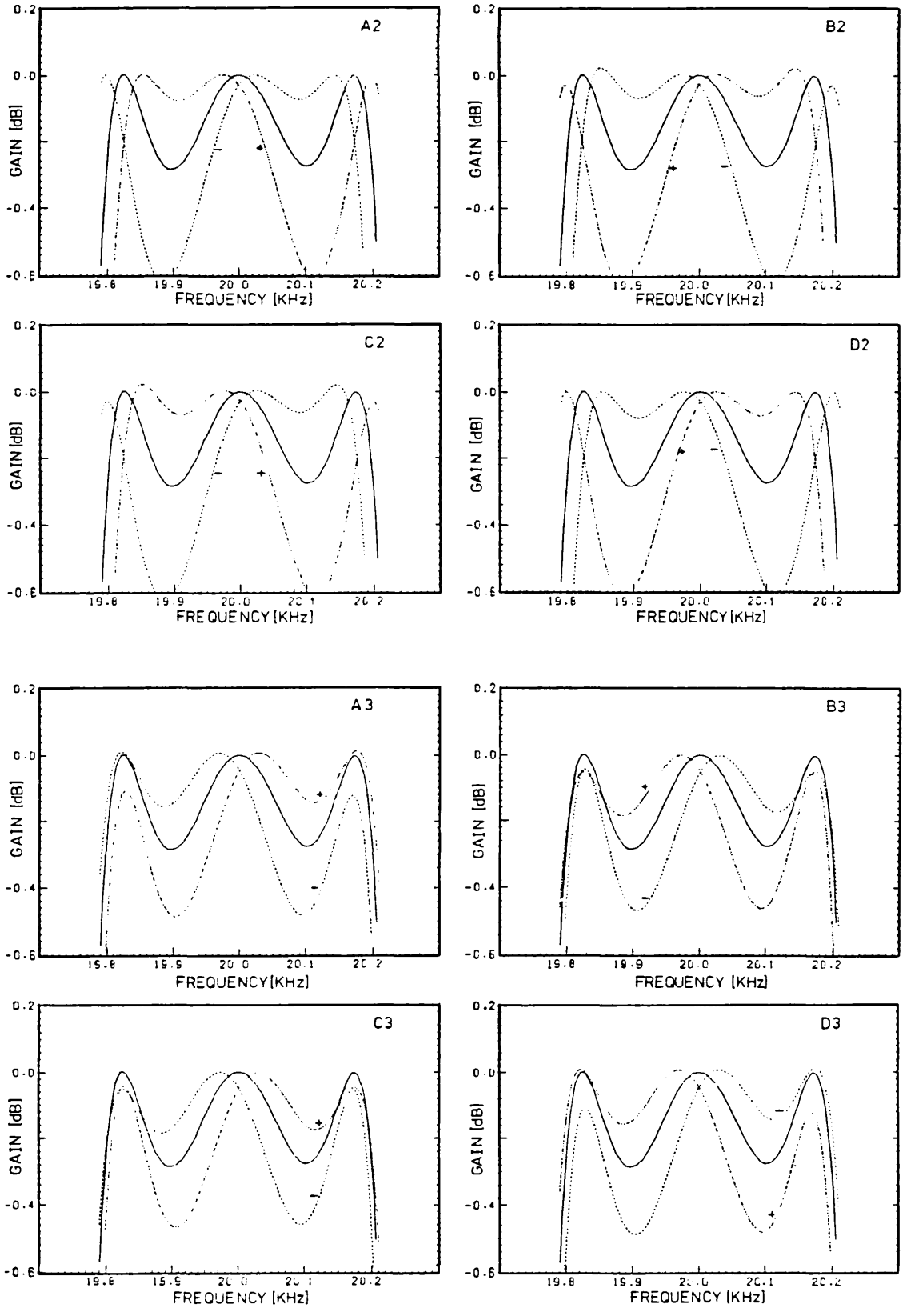


Fig.5.6 (continued)

Because of the adoption of the optimum switching frequency, the capacitance ratios in the loop of the SC biquads are very small, i.e.

$$(5.4)\ \ldots \qquad \frac{A1}{B1} = \frac{C2}{D2} = \frac{A3}{B3} = 1 \quad ; \quad \frac{A2}{B2} = 2$$

$$\frac{C1}{D1} = \frac{C3}{D3} = 1.977$$

In an integrated circuit realisation, the precision of such ratios can be better than 0.1% and therefore we could expect to achieve a good accuracy of the amplitude response. On the other hand, in the discrete component models that we build for experimental evaluation, we estimate that the achievable accuracy of such ratios may be of the order of 0.2% to 0.5%, and thus we antecipate larger errors in the amplitude response for such models.

5.3 SC BANDPASS FILTER SYSTEM WITH BASEBAND OPERATING MODE

5.3.1 System architecture and circuits

The general architecture of an SC bandpass filter system operating in the baseband filtering mode is shown in Fig.5.7, with lowpass AAF and AIF. The implementation of such a system employing the SC bandpass filter considered before implies designing lowpass AAF and AIF which have to provide adequate rejection of the alias and image signals, respectively, at a minimum frequency of $F_s - f_o = 60KHz$. The appropriate technological solution to this problem is, as

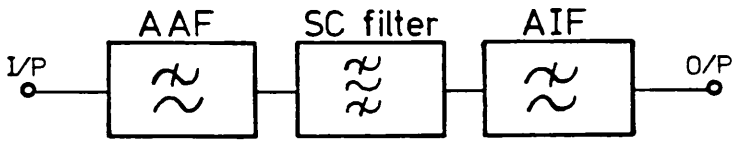


Fig.5.7: General architecture of an SC bandpass filter system with baseband operating mode

we saw in Chapter 2, to decompose the AAF and the AIF into low selectivity continuous-time filters, together with an SC decimator and an SC interpolator, respectively, for sampling rate alteration.

For conciseness, we shall consider now a 3rd. order lowpass continuous-time filter in the AAF, the response of which, shown in Fig.5.8-a, ensures a minimum rejection of 40dB of the alias signals with minimum frequency $f_{min.}$=300KHz. Below $f_{min.}$, the frequency bands of the input continuous-time spectrum that relate to the desired system passband have to be attenuated, also by a minimum of 40dB, by an SC lowpass decimator. The remaining portions of the spectrum below $f_{min.}$ are not of concern since they correspond to the stopband of the SC bandpass filter and are thereby attenuated. Hence, the SC decimator is required to have a minimum factor of sampling rate reduction of $M=(f_{min.}+f_o)/F_s=4$. For the SC lowpass interpolator in the AIF, we adopt also a factor L=4 for sampling rate increase yielding the same sampling rate of 320KHz, both at the input, and at the output, of the system. However, because of the extra attenuation provided by the sample and hold function, it suffices, in this case, to have a simpler 2nd.

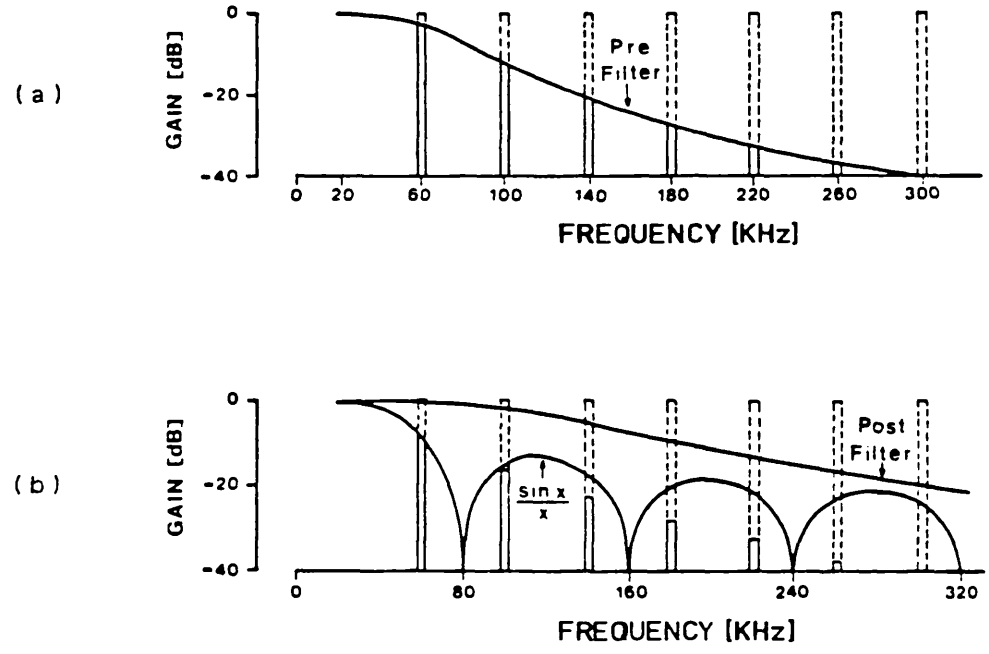


Fig.5.8: (a) Aliasing spectrum, and 3rd. order continuous-time filter with stopband frequency at 300KHz (nominal cut-off frequency at 60KHz); (b) Imaging spectrum, with sample and hold attenuation, and 2nd. order continuous-time filter (cut-off frequency at 115KHz)

order lowpass continuous-time filter at the output of the system, the response of which is illustrated in Fig.5.8-b.

For the above requirements of the decimator and interpolator we adopt an optimum multinotch stopband approximation which produces notch frequencies at 80KHz±20KHz, 160KHz±20KHz and 240KHz±20KHz. The optimised impulse responses of the FIR transfer functions are given in Fig.5.9, for a cascade approach using circuits for sampling rate alteration M=L=2. In order to implement the

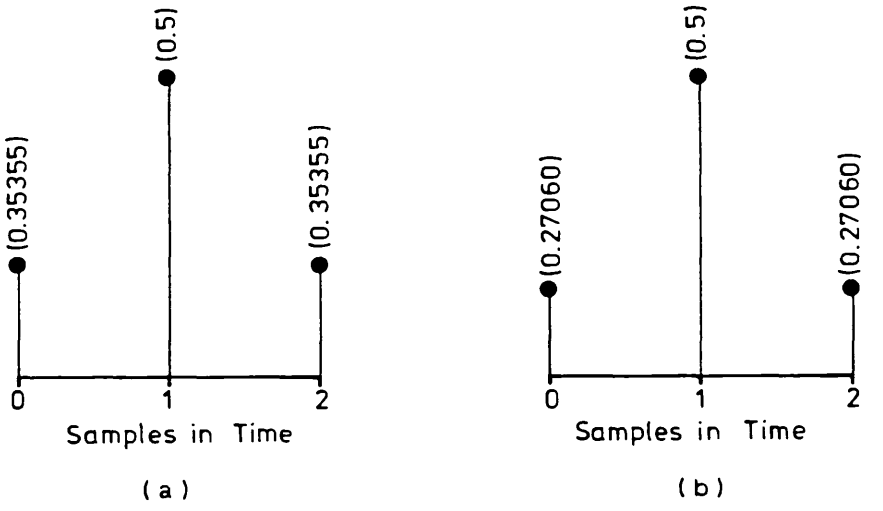
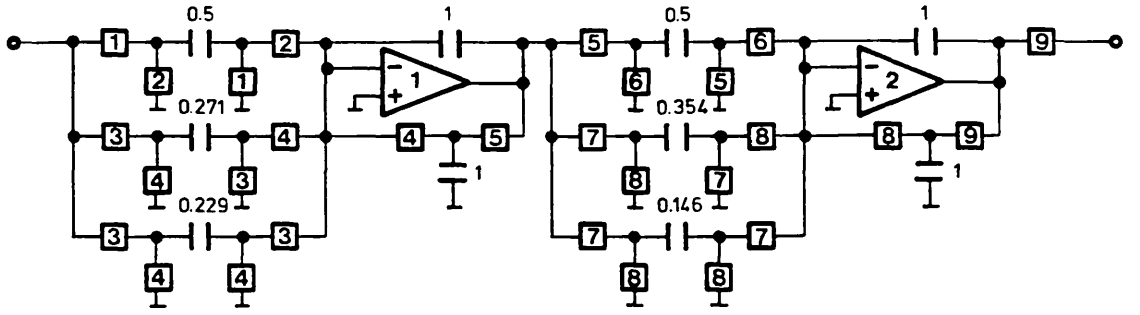
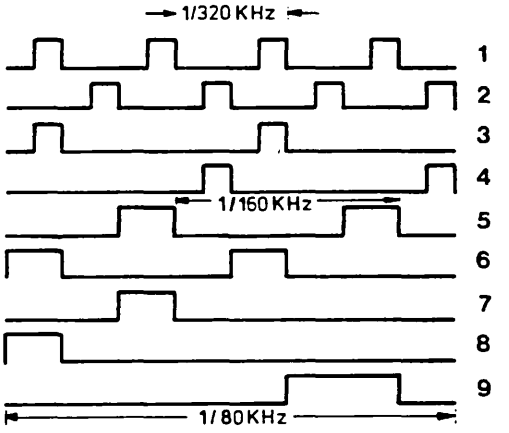


Fig.5.9: Optimised impulse responses for cascaded FIR SC lowpass decimator, and interpolator. (a) 80KHz ⇄ 160KHz; (b) 160KHz ⇄ 320KHz

FIR transfer functions with such impulse responses we consider the solutions of SC decimator and interpolator circuits shown in Fig.5.10 and in Fig.5.11, respectively, together with their computed baseband amplitude responses, and the corresponding measured responses of discrete component models. The FIR SC lowpass decimator employs non-recursive polyphase SC structures with multiplexed SC elements; the FIR SC lowpass interpolator with SC biquads corresponds to an example illustrated in the previous Chapter (Section 4.2, Fig.4.2 and Fig.4.3), which we repeated here for convenience.



(a)



(b)

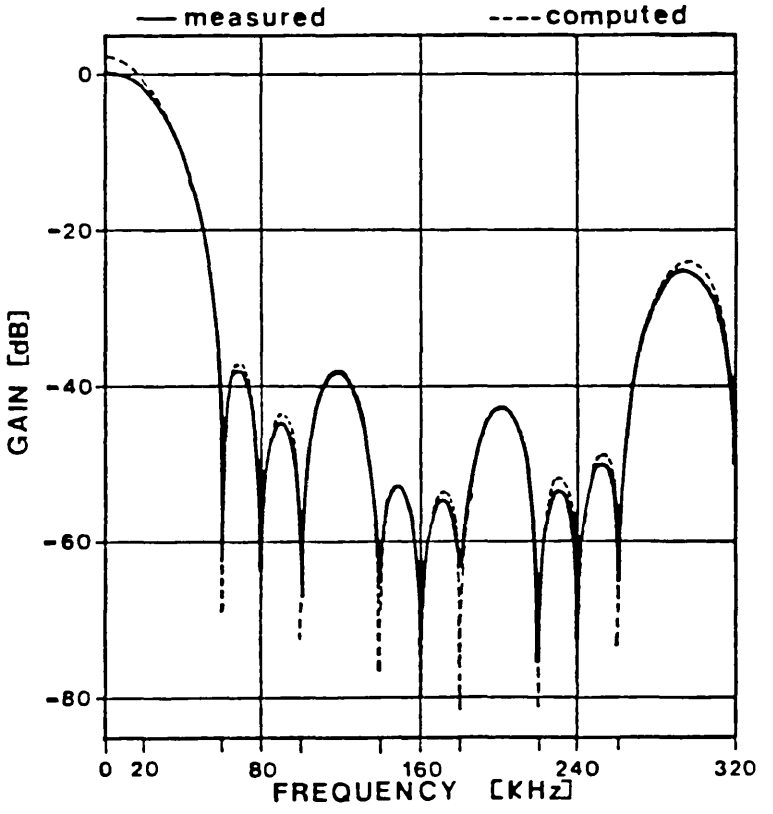


Fig.5.10: (a) Cascade FIR SC lowpass decimator M=4, with non-recursive polyphase structure (multiplexed SC elements); (b) Measured, and computed, baseband amplitude response

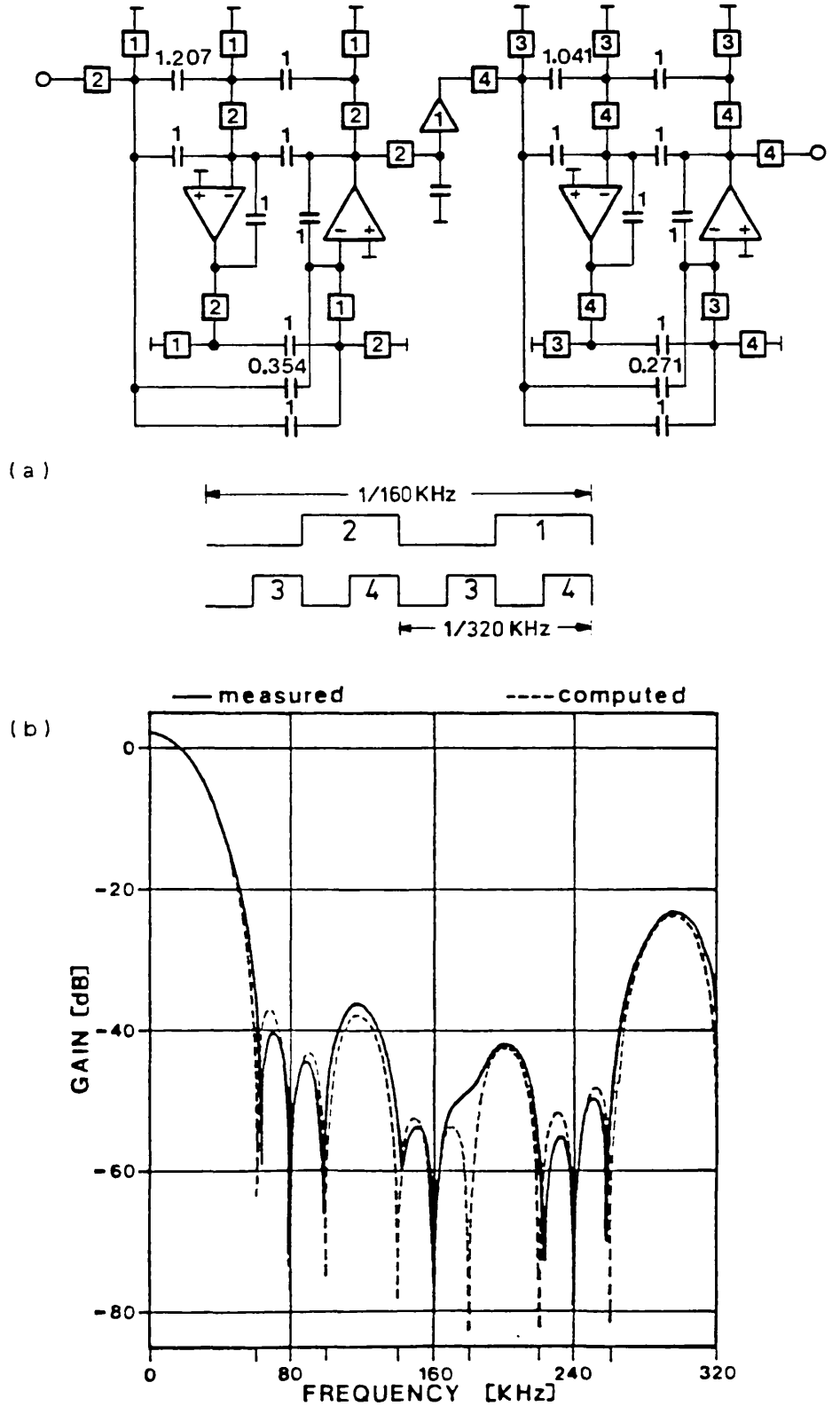


Fig.5.11: (a) Cascade FIR SC lowpass interpolator M=4, using FIR SC biquads with Type-A switching; (b) Measured, and computed, baseband amplitude response

Non-recursive polyphase SC decimators and interpolators had not been fully developed at the time the SC bandpass filter system considered in this Section was designed and tested. For completeness, we show in Fig.5.12-a and in Fig.5.13-a the state-of-the-art of such FIR SC decimator and interpolator circuits, for the same requirement as above. Both the single-stage FIR SC decimator circuit with M=4 (as in Fig.4.24), and the cascade FIR SC interpolator circuits with L=2 (as in Fig.4.28), employ direct-form SC elements, and, together, they need only half of the number of OA's required in the previous realisations. The computed baseband amplitude responses, and the corresponding measured amplitude responses of discrete component models are shown in Fig.5.12-b, for the SC decimator in Fig.5.12-a, and in Fig.5.13-b, for the SC interpolator in Fig.5.13-a. The performance of the SC interpolator, which is comparable to that of the SC decimator, is significantly better than the performance of the biquad cascade realisation shown in Fig.5.11.

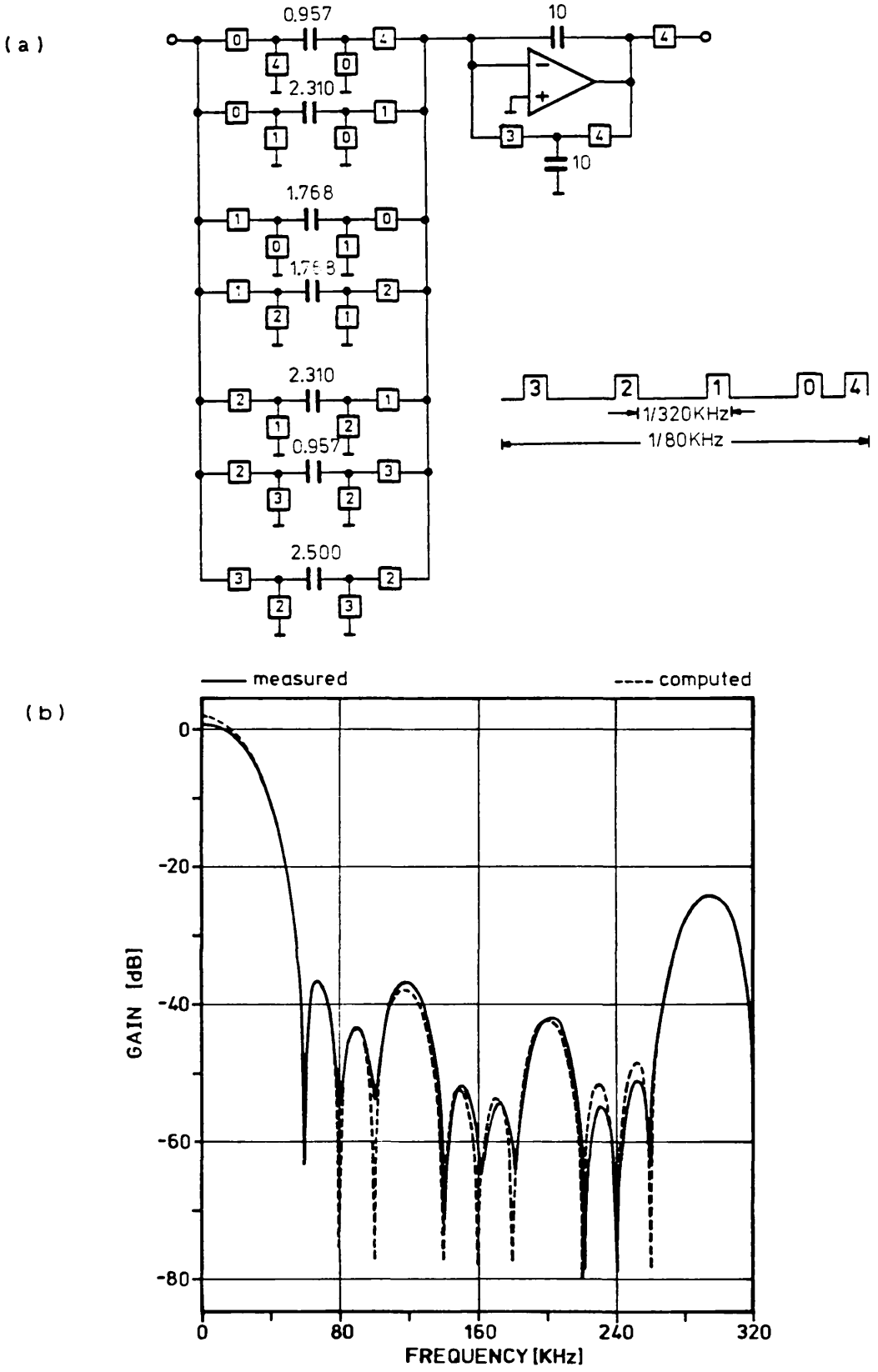
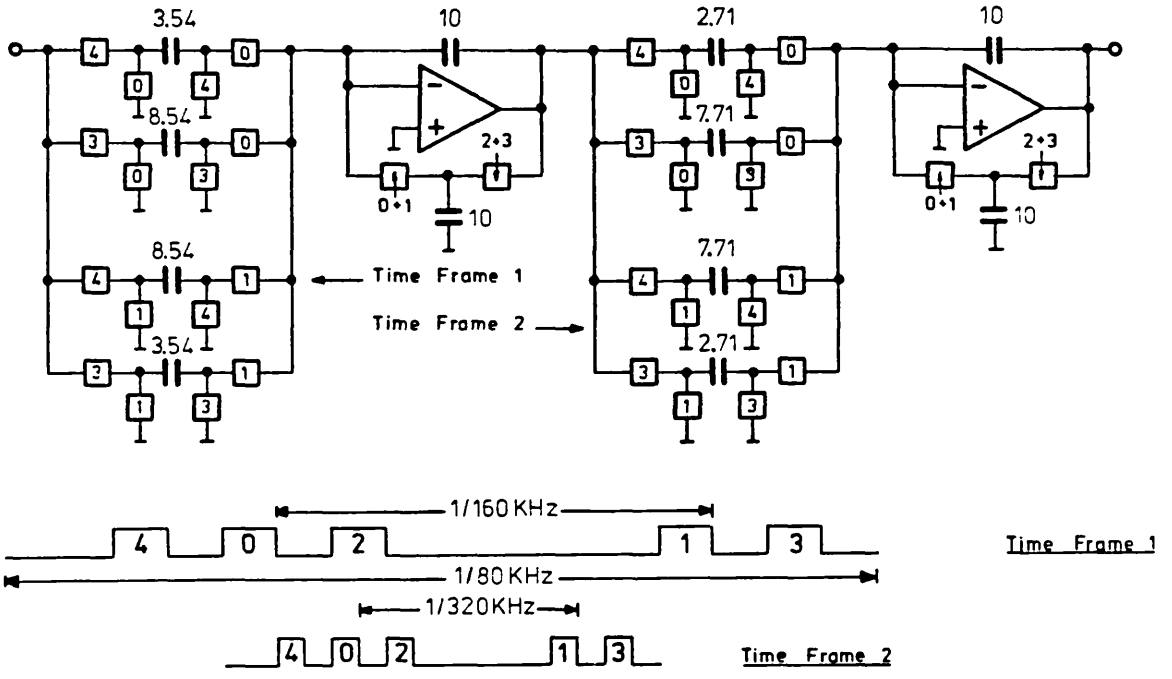
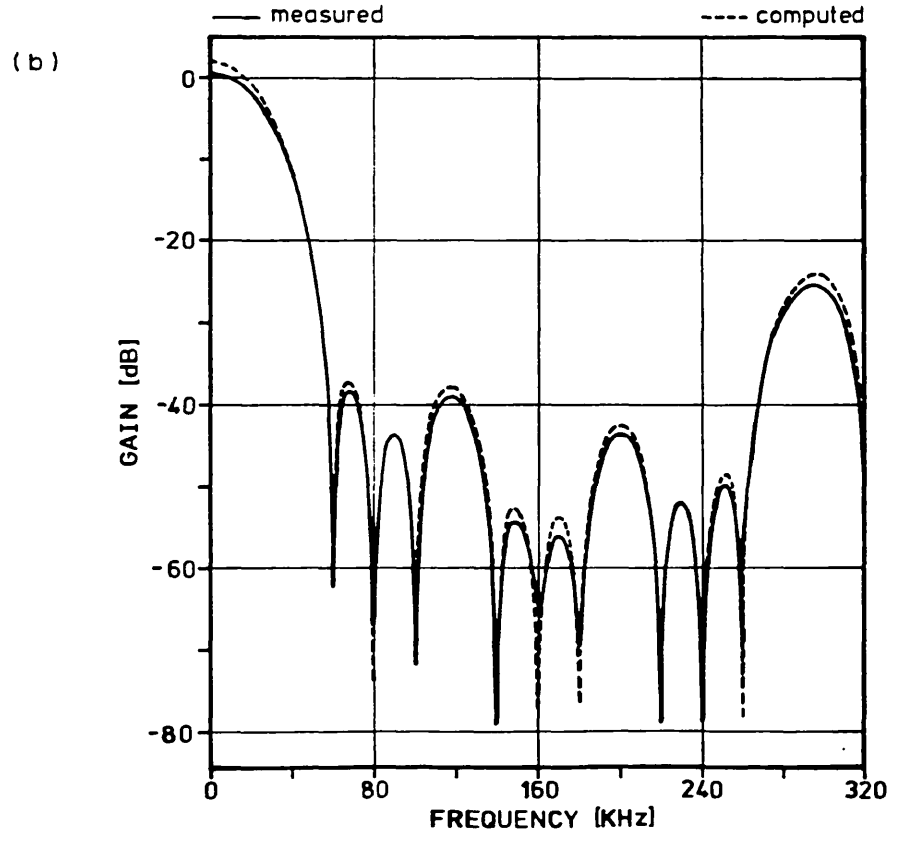


Fig.5.12: (a) Single-stage FIR SC lowpass decimator M=4, with non-recursive polyphase direct-form structure; (b) Measured, and computed, baseband amplitude response



(a)



(b)

Fig.5.13: (a) Cascade FIR SC lowpass interpolator L=4, with non-recursive polyphase direct-form structure; (b) Measured, and computed, baseband amplitude response

5.3.2 Experimental evaluation

The schematic of the complete SC bandpass filter system (the continuous-time filters are not included) is shown in Fig.5.14, comprising the SC bandpass filter designed in the previous Section, and the SC decimator and interpolator circuits of Fig.5.10 and Fig.5.11, respectively. The synchronised switching scheme of the system allows the interface between the two stages of the SC decimator, as well as the interface between the SC decimator and the SC bandpass filter to be provided by series sampling switches. The interstage sample and hold circuit in the SC interpolator is required because the FIR SC biquads employ Type-A switching. The switching scheme for the system is implemented using a distributed modular clock generator, whereby the switching waveforms required for each SC circuit are locally generated from a reduced clock bus with only four clock lines. Otherwise, it would have been necessary to route as many as fifteen clock lines throughout the system, which would have rendered the layout more complex, and would have also increased the digital noise coupled onto the analogue lines. A discrete component model of this system was constructed using a printed circuit. It employs CMOS 4016 analogue switches, CMOS 7611 OA's for the SC bandpass filter, JFET LF355 OA's for the SC decimator and interpolator, and standard CMOS digital components for the switching circuitry. The capacitance spread and total normalised capacitance of each SC circuit in the system are summarised in Table 5.2.

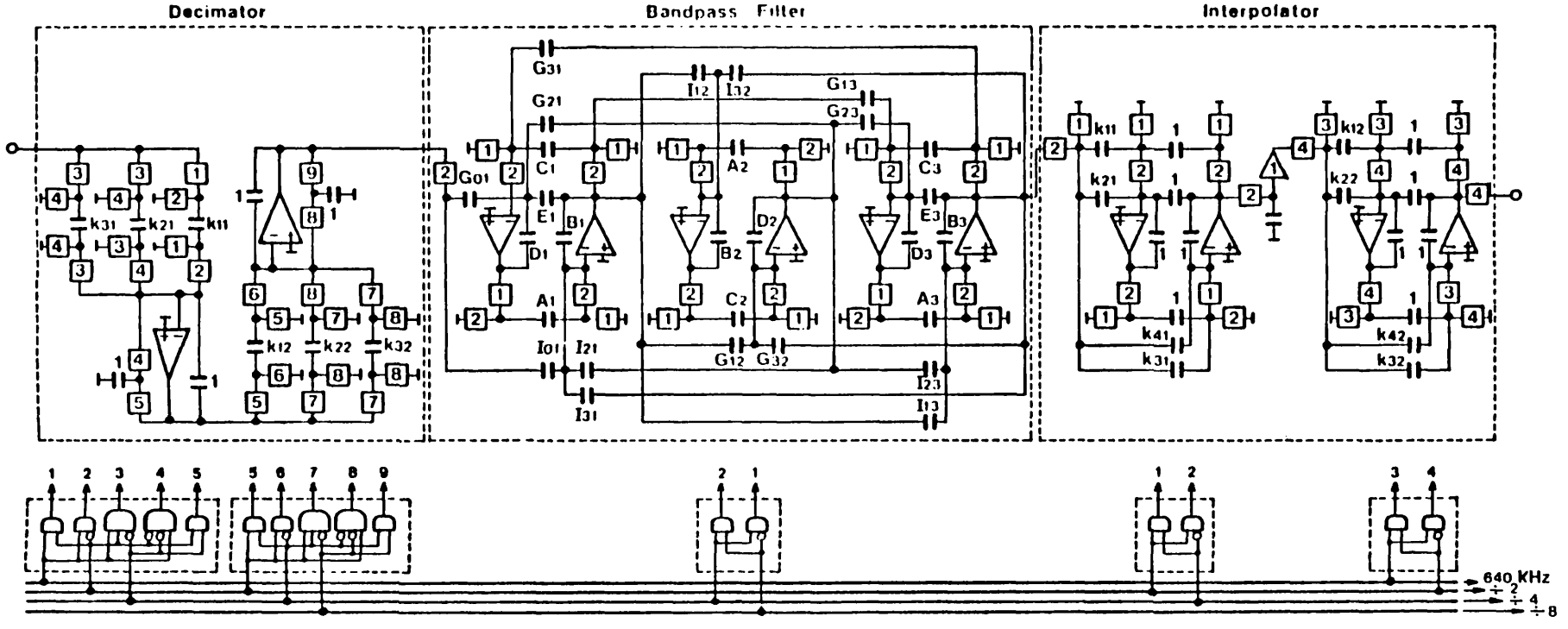


Fig.5.14: Schematic of the SC bandpass filter system with baseband operating mode showing the distributed modular clock generation scheme

	SC DECIMATOR M=4		SC	SC INTERPOLATOR L=4		SC BANDPASS
	1st stage	2nd stage	FILTER	1st stage	2nd stage	FILTER SYSTEM
C-spread	4.359	6.828	87.8	2.828	3.695	87.8
Total C	13.078	20.484	884	24.210	30.716	972.5

Table 5.2: Capacitance spread and total normalised capacitance in the SC bandpass filter system

Overall and expanded measured baseband amplitude responses of the filter system are shown in Fig.5.15-a and in Fig.5.15-b, respectively.

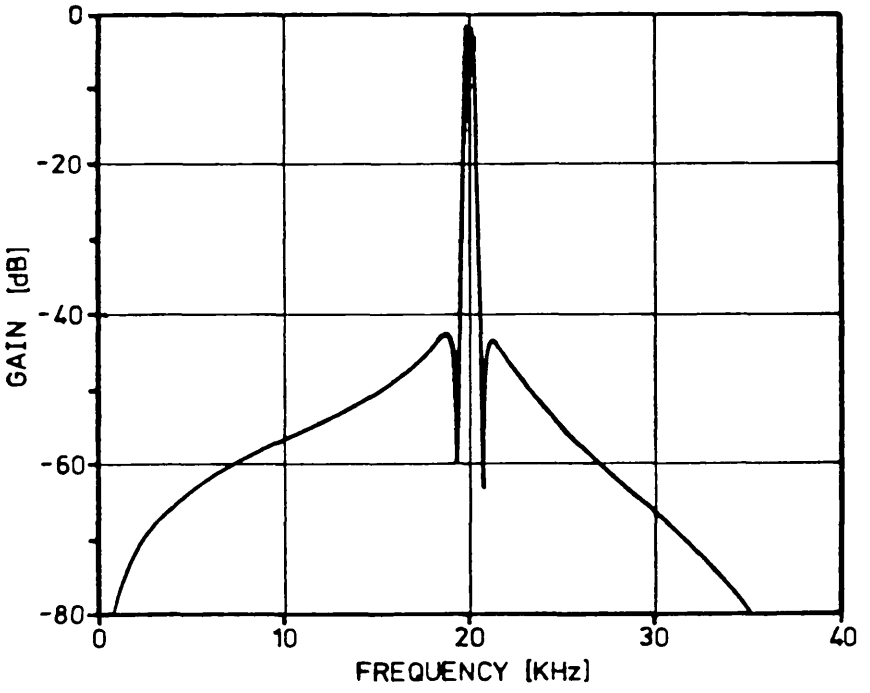


Fig.5.15: (a) Measured overall baseband amplitude response of the SC bandpass filter system

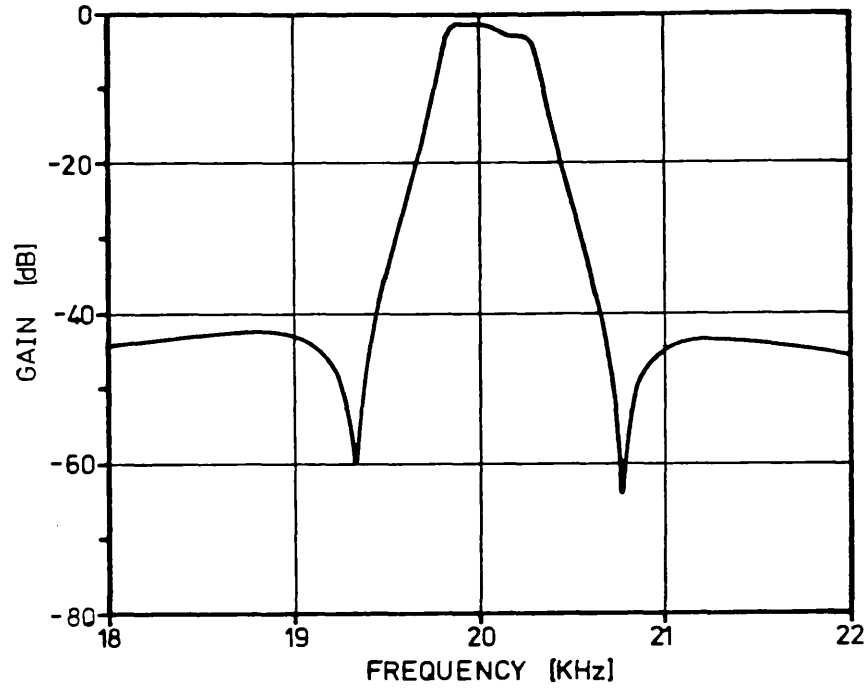


Fig.5.15: (b) Measured expanded baseband amplitude response of the SC bandpass filter system

The noise performance of the system, measured with a detector bandwidth of 100Hz, is shown in Fig.5.16.

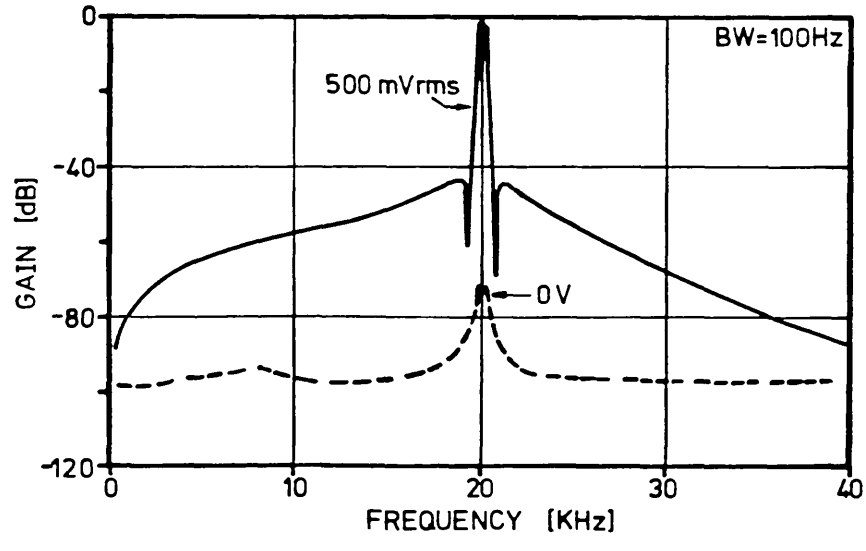


Fig.5.16: Measured noise performance of the SC bandpass filter system

Other relevant measured results of the SC bandpass filter system are given in Table 5.3. As we can see, both the SC decimator and SC interpolator provide the required rejection of 40dB of the alias and image signals below 300KHz. However, we should mention that the sample and hold effect contributes to a great extent to the attenuation of the image signals at 140KHz (17.8dB) and at 180KHz (20dB) because, as we discussed in Section 4.2, and can see in Fig.5.11-b, the SC interpolator has poor performance at such critical frequencies.

Centre frequency	20.058KHz
Gain (includes sinc x)	-1.55dB
-3dB Bandwidth	480Hz
Stopband Rejection	>41dB
Power Supply	±5V
Maximum Input Signal	800mVrms
Dynamic Range	75dB
Aliasing Rejection (<300KHz)	>40dB
Imaging Rejection (<300KHz)	>50dB

Table 5.3: Experimental results of the SC bandpass filter system

The results above indicate that narrow bandpass responses can be realised using conventional SC bandpass filters, provided the switching frequency is chosen according to the optimum criterion discussed in Chapter 3, and the sophisticated SC decimators and interpolators developed in Chapter 4 are introduced to reject the

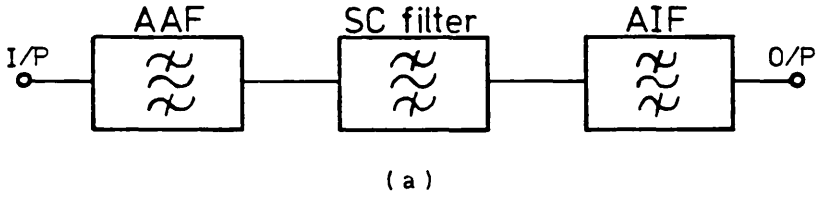
unwanted alias and image frequency-translated components at low frequency. In order to realise very narrow bandpass responses, this type of system is no longer applicable, not only because of the large capacitance spread that would arise in the SC bandpass filter, even if an optimum switching frequency is employed, but mainly because of the resulting extremely high sensitivity of the amplitude response to capacitance ratio errors. For such applications, we have to employ instead an SC bandpass filter system operating in a different mode.

5.4 SINGLE-PATH FREQUENCY-TRANSLATED (SPFT) SC BANDPASS FILTER SYSTEMS

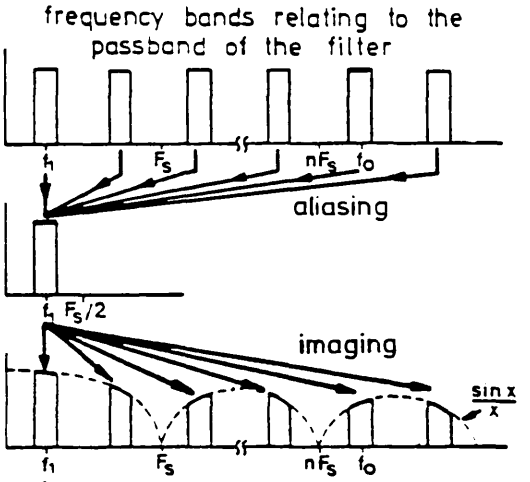
5.4.1 Architecture, operating mode, and properties

The idea of Single-Path Frequency-Translated (SPFT) SC systems was introduced in Section 2.3. In such systems, the alias and image frequency-translated responses of SC filters can be efficiently utilised in order to implement operations of downwards frequency-translation, upwards frequency-translation, and frequency-translated filtering. SPFT SC systems implementing downwards and upwards frequency-translated operations will be demonstrated in Section 5.8. This, and the following Sections, will study the application of SPFT SC filter systems for the realisation of bandpass responses with very narrow relative bandwidths of less than 1%.

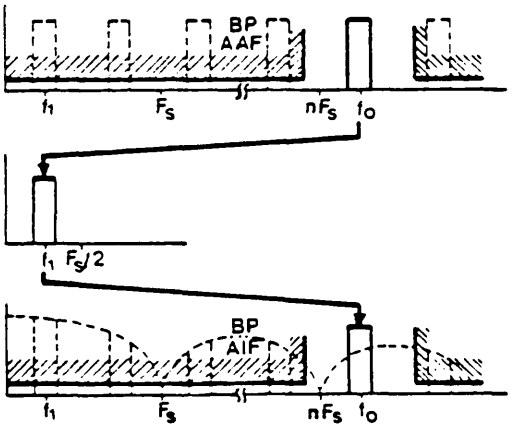
The general architecture of an SPFT SC bandpass filter system is shown in Fig.5.17-a. The SC bandpass filter with midband frequency f_1, switching frequency $F_s=mf_1$ and bandwidth BW_1 (Q-factor $Q_1=f_1/BW_1$) possesses the frequency-translated alias and image responses symbolically



(a)



(b)



(c)

Fig.5.17: Architecture, and operating mode, of an SPFT SC bandpass filter system

represented as in Fig.5.17-b. The bandpass AAF and AIF select one specified frequency band around a multiple n of the switching frequency and reject the remaining unwanted frequency bands according to the anti-aliasing and anti-imaging specifications. The selection of the upper sideband (n^+) in Fig.5.17-c yields an SPFT system with midband frequency $f_o=nF_s+f_1$ and Q-factor $Q_o=K.Q_1$, where $K=m.n+1$ is the Q-enhancement factor of the system ($m=F_s/f_1$ is the sampling ratio of the SC bandpass filter). The selection of the lower sideband (n^-) would have yielded the system midband frequency $f_o=nF_s-f_1$ and the corresponding Q-enhancement factor $K=m.n-1$.

There are two fundamental aspects which characterise the above operation of an SPFT SC bandpass filter system, compared to a conventional SC bandpass filter system with baseband operating mode. Firstly, for a given midband frequency f_o of the SC filter system, the actual filtering operation in the system which produces the desired response is performed by an SC bandpass filter with much lower midband frequency f_1, and operating with correspondingly lower switching frequency F_s. Therefore, the speed requirements for the OA's in the SC filter can be substantially relaxed, which simplifies their design, and also leads to a reduction in power consumption. The second important aspect of an SPFT SC bandpass filter system is the lower selectivity of the SC bandpass filter in the system, compared to the much higher selectivity that would be required for an SC bandpass filter in a conventional SC

filter system operating in a baseband filtering mode, with the same overall selectivity. This implies much smaller capacitance ratios, and thus smaller capacitor area, in the SC bandpass filter, on the one hand, and, on the other hand, much lower sensitivity of the bandpass response to capacitance ratio errors. Overall, these characteristics of SPFT SC bandpass filter systems make them very attractive for implementing very narrow bandpass responses. From a system point of view there is, of course, the requirement for more sophisticated AAF and AIF, whose fundamental characteristics will be examined next.

5.4.2 Anti-aliasing filter

In an SPFT SC bandpass filter system, in order to achieve a given Q-enhancement factor $K=m.n\pm1$ we have available, besides the sideband selection, the key system parameters m and n whose values determine the characteristics of the AAF and AIF, and hence the complexity of the SPFT system. The selectivity of the AAF depends on the sampling ratio $m=F_s/f_1$ of the SC bandpass filter, as shown in Fig.5.18 for the example of selecting an upper frequency-translated sideband. If the SC bandpass filter is oversampled, i.e. $m>>1$, then, the frequency-translated bands are close to nF_s, which implies an AAF with high selectivity of the lower transition band, as in Fig.5.18-a. When the SC bandpass filter is critically sampled, i.e. $m\simeq2$, the frequency-translated bands are close to the odd multiples of $F_s/2$ and, as we can see in Fig.5.18-b, the AAF requires high selectivity of the upper

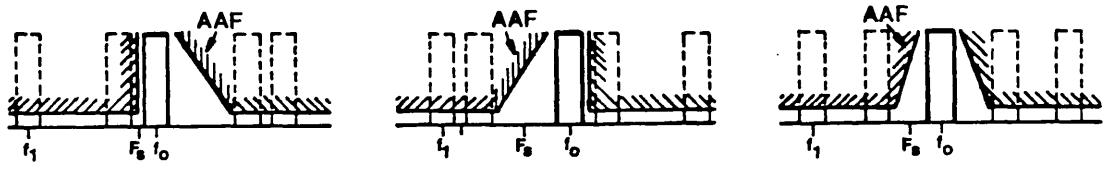


Fig.5.18: Selectivity of the AAF versus the sampling ratio $m=F_s/f_o$ of the SC bandpass filter. (a) Oversampling; (b) Critical sampling; (c) Sampling with m=4 for uniformely spaced frequency-translated bands

transition band. For m=4, the frequency-translated bands are uniformly spaced, and, then, the AAF may have a bandpass response with symmetrical transition bands, as illustrated in Fig.5.18-c. Adoption of the sampling ratio m=4 offers the additional benefits of minimum capacitance spread, and also minimum capacitor area taken up by the SC bandpass filter, as we saw in Section 5.2.

5.4.3 Anti-imaging filter

The sampled and held nature of the signal at the output of the SC bandpass filter implies the multiplication of the image response by the function $\sin(\pi f/F_s)/(\pi f/F_s)$. This introduces a differential gain error over the passband, which is negligible for narrow bandwidth applications, and a larger midband gain error which is expressed in terms of K and m as

$$\alpha(dB) = -20\log\left|\frac{(\pi K/m)}{\sin(\pi K/m)}\right| \qquad (5.5)\ \ldots$$

For m=4, this gives $\alpha(dB)\tilde{-}-20\log(K/0.9)$, for 0dB reference at DC. In order to compensate such sample and hold effect, the AIF is required to have greater selectivity, and higher midband gain, than its AAF counterpart. This is explained in Fig.5.19 for the example of the selected image $n=1^{+}$.

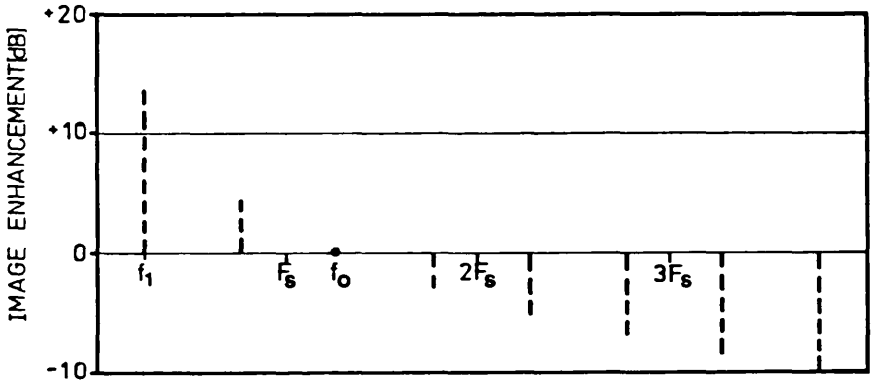


Fig.5.19: Illustration of the amplitude enhancement of the image signals due to the sample and hold effect

A flat gain of +14.89dB is required for compensation of the midband gain error of $\alpha=-14.89$dB at $f_o=F_s+f_1$. The amplitude of the image signals whose frequencies are below f_o are enhanced by +14dB, at f_1, and by +4.4dB, at F_s-f_1, due to a much smaller sample and hold attenuation. Therefore, for the same anti-imaging and anti-aliasing specifications, such image enhancement factors indicate the extra attenuation that the AIF is required to provide, in comparison with the AAF. On the other hand, for the signals above the selected image, the selectivity of the AIF may be lower than that of the AAF due to the extra attenuation provided by the sample and hold function, as is also illustrated in Fig.5.19.

5.4.4 Sampling rate alteration

In order to employ continuous-time filters in the AAF and AIF of a similar complexity as in the system described in the Section 5.3, it is required that $F_s \geq 16f_o$. Therefore, the minimum factor of sampling rate reduction required for the SC decimator in the AAF is $M=16(n\pm 1/m)$, i.e. $M=16n\pm 4$, for m=4. For the SC interpolator in the AIF, the factor of sampling rate increase is L=M. A factor of sampling rate alteration higher than the minimum $M=L=16n\pm 4$ will relax the requirements of the continuous-time filters, at the expense of some additional complexity of the SC decimator and SC interpolator.

5.4.5 Characteristics of an SPFT system for design and implementation

In order to describe aspects of the design of SPFT systems, particularly with respect to the decimator and interpolator architectures, we shall consider the SC bandpass filter in Section 5.2 with switching frequency F_s=16KHz, thus midband frequency f_1=4KHz (m=4) and -3dB bandwidth BW_1=96Hz. For the realisation of a bandpass response with -3dB relative bandwidth of 0.48% at midband frequency f_o=20KHz, the SPFT system requires a Q-enhancement factor of K=5, implying $n=1^+$, and thus a minimum factor of sampling rate alteration M=L=20. We shall consider M=L=24, in which case the spectrum of the frequency-translated signals (alias or image) for the design of the decimator and interpolator is schematically illustrated in Fig.5.20. The attenuation of the alias and

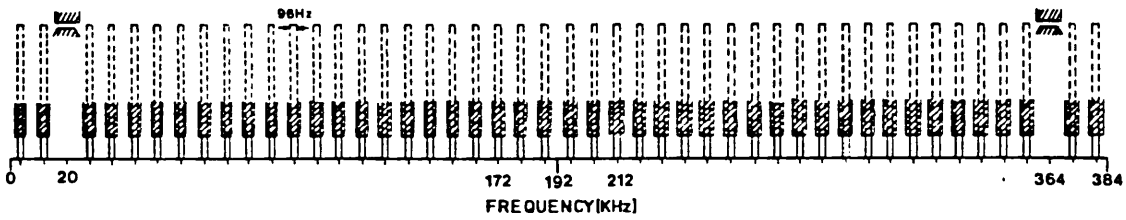


Fig.5.20: Schematic representation of the frequency-translated bands, in the SPFT system, that relate to the passband of the SC bandpass filter

image signals at 364KHz, and above, can be achieved by continuous-time filters with more relaxed specifications than those considered before, e.g. higher nominal cut-off frequency allowing greater tolerances. On the other hand, the attenuation below 364KHz has to be provided by decimators and interpolators with more complex architectures than those considered previously. In the following Sections we shall consider, in the first place, decimator and interpolator architectures employing only FIR SC circuits. Then, we shall also consider alternative decimator and interpolator architectures with different combinations of FIR and IIR SC circuits.

5.5 SPFT SC BANDPASS FILTER SYSTEM 1: A case study using fully FIR decimator and interpolator

The architecture of the SPFT system to be considered in this case study is shown in Fig.5.21, employing an FIR SC bandpass decimator and a complementary FIR SC bandpass interpolator. For both the SC decimator and interpolator,

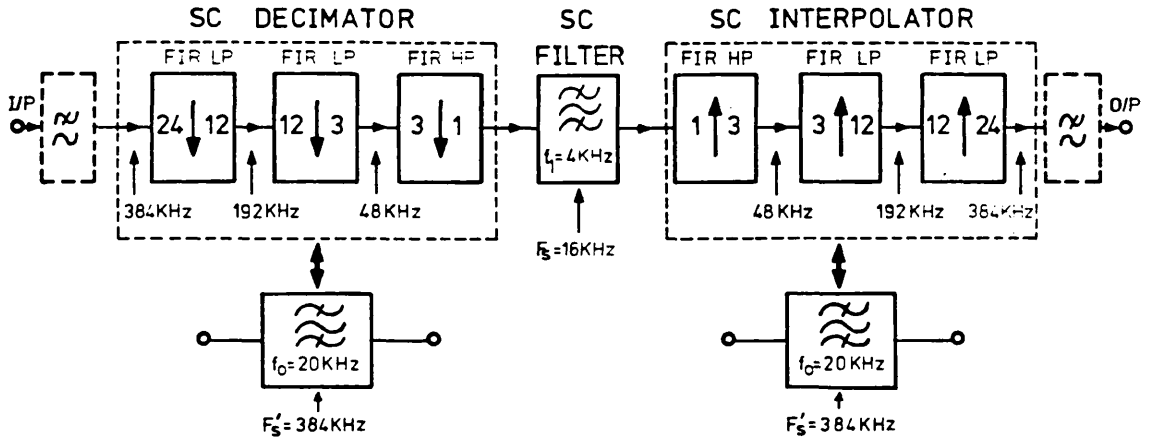


Fig.5.21: Architecture of the SPFT system 1, employing FIR SC bandpass decimator and interpolator

we consider three stages of sampling rate conversion, namely decimation from the system input by factors of M=2, M=4, and M=3, and complementary interpolation to the system output by factors of L=3, L=4, and L=2. The optimisation of the transfer functions of the SC decimator circuits, for example, will be explained with reference to Fig.5.22. The FIR SC highpass decimator with M=3, and with baseband from DC to $3F_S/2$=24KHz, introduces notch frequencies at 4KHz (alias frequency band A) and at 12KHz (alias frequency band B), which are periodically repeated above 24KHz, as shown in Fig.5.22-a. In Fig.5.22-b, the FIR SC lowpass decimator with M=4, and with baseband from DC to $6F_S$=96KHz, introduces notch frequencies at 28KHz (alias frequency band C), at 68KHz (alias frequency band D) and at 76KHz (alias frequency band E), which are periodically repeated above 96KHz. In Fig.5.22-c, the other FIR SC lowpass decimator,

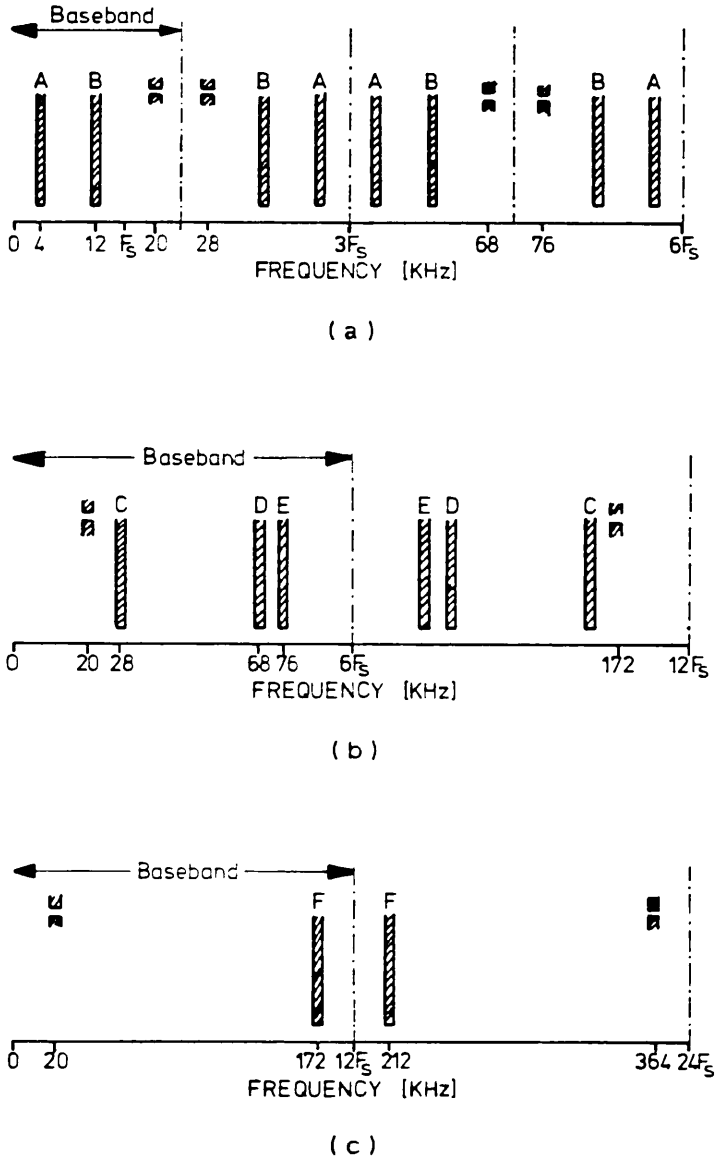


Fig.5.22: Illustration of the multinotch requirements for the FIR SC decimator circuits. (a) Highpass decimator for sampling rate reduction from 48KHz to 16KHz (M=3); (b) Lowpass decimator for sampling rate reduction from 192KHz to 48KHz (M=4); (c) Lowpass decimator for sampling rate reduction from 384KHz to 192KHz (M=2)

with M=2, and baseband from DC to $12F_S$=192KHz, introduces a notch frequency at 172KHz (alias frequency band F), which is repeated at 212KHz. The optimised impulse responses of each SC decimator are given in Fig.5.23, which can then be

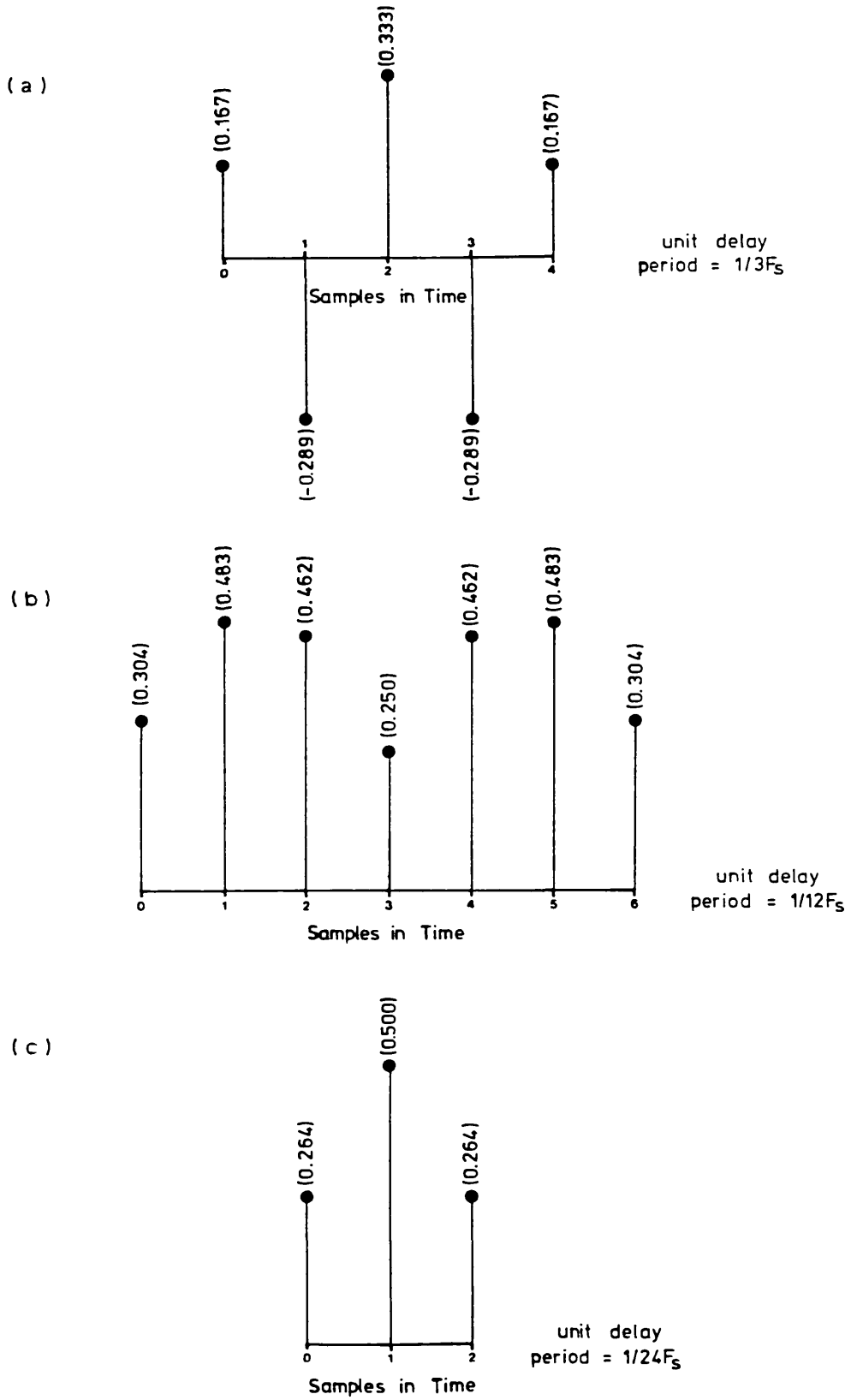


Fig.5.23: Optimised impulse responses for the FIR SC decimator circuits. (a) Highpass decimator M=3; (b) Lowpass decimator M=4; (c) Lowpass decimator M=2

implemented using the non-recursive polyphase direct-form SC decimator circuits shown in Fig.5.24.

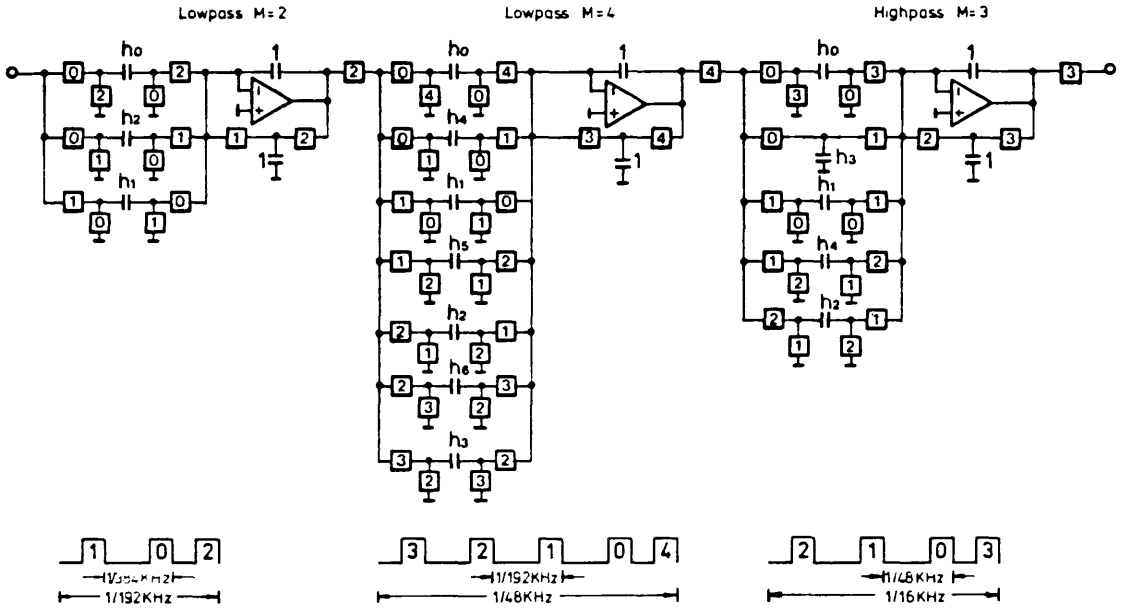


Fig.5.24: FIR SC bandpass decimator M=24

The theoretical alias amplitude response of the complete FIR SC bandpass decimator is shown in Fig. 5.25-a (only the baseband from DC to 192KHz is shown). Fig.5.25-b shows expanded amplitude responses in the vicinity of the critical notch frequencies which are closest to the midband frequency f_0=20KHz of the system, i.e. at 4KHz, 12KHz, 28KHz, and 36KHz. The rejection achieved in the vicinity of the notch frequencies decreases as the required notch stopband bandwidth increases. In this system, the minimum notch stopband bandwidth must be 96Hz, which encompasses the -3dB bandwidth of the SC bandpass filter. In practice, however, we have to consider a much wider notch stopband bandwidth in order to take into account the unavoidable

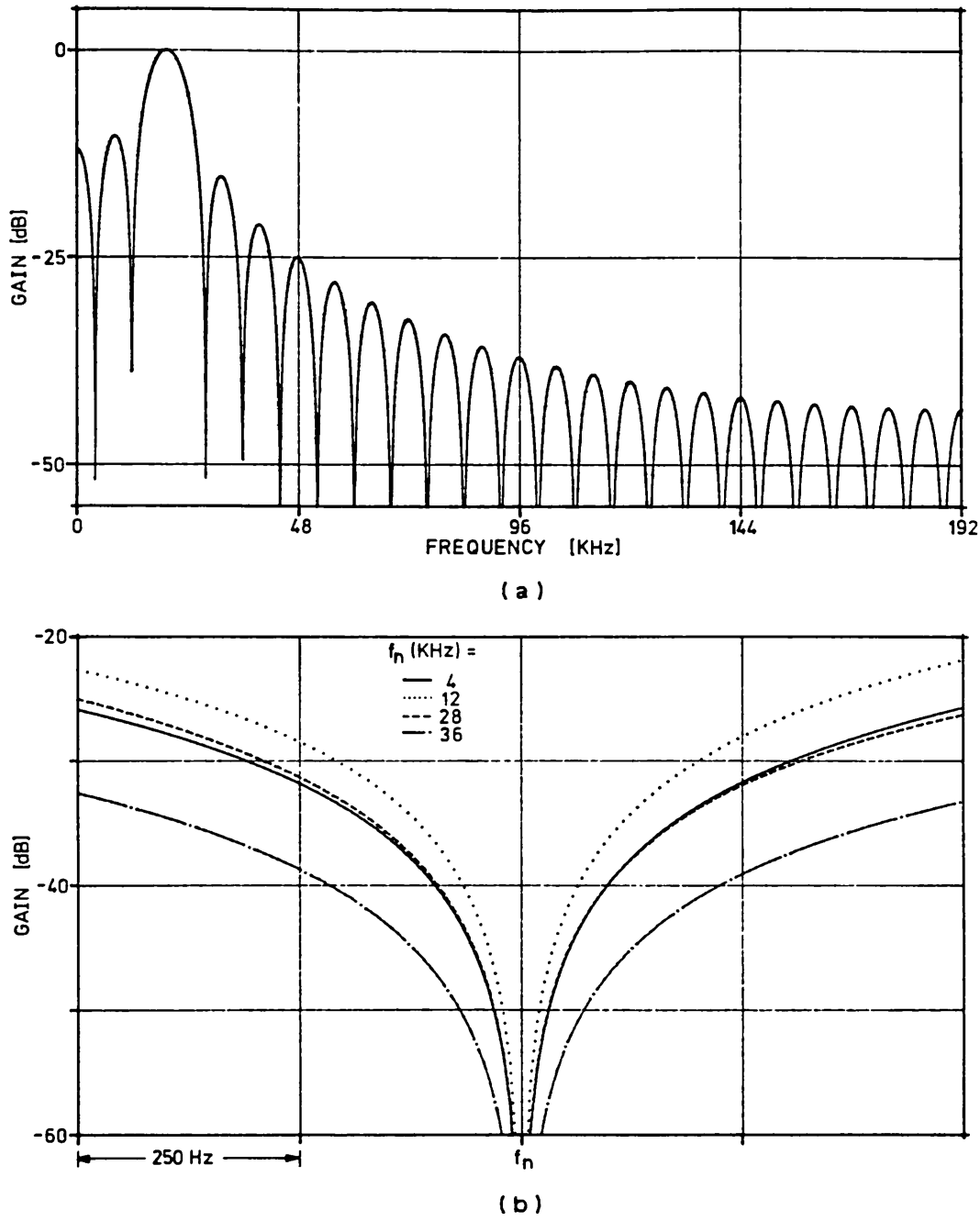


Fig.5.25: (a) Theoretical amplitude response of the FIR SC bandpass decimator M=24; (b) Expanded amplitude responses around the critical notch frequencies

variability of the amplitude responses both of the SC decimator and of the SC bandpass filter itself, such as illustrated in the example of Fig.5.26. Fig.5.26-a represents the ideal situation, with nominal notch frequencies f_n of the SC decimator, and nominal midband

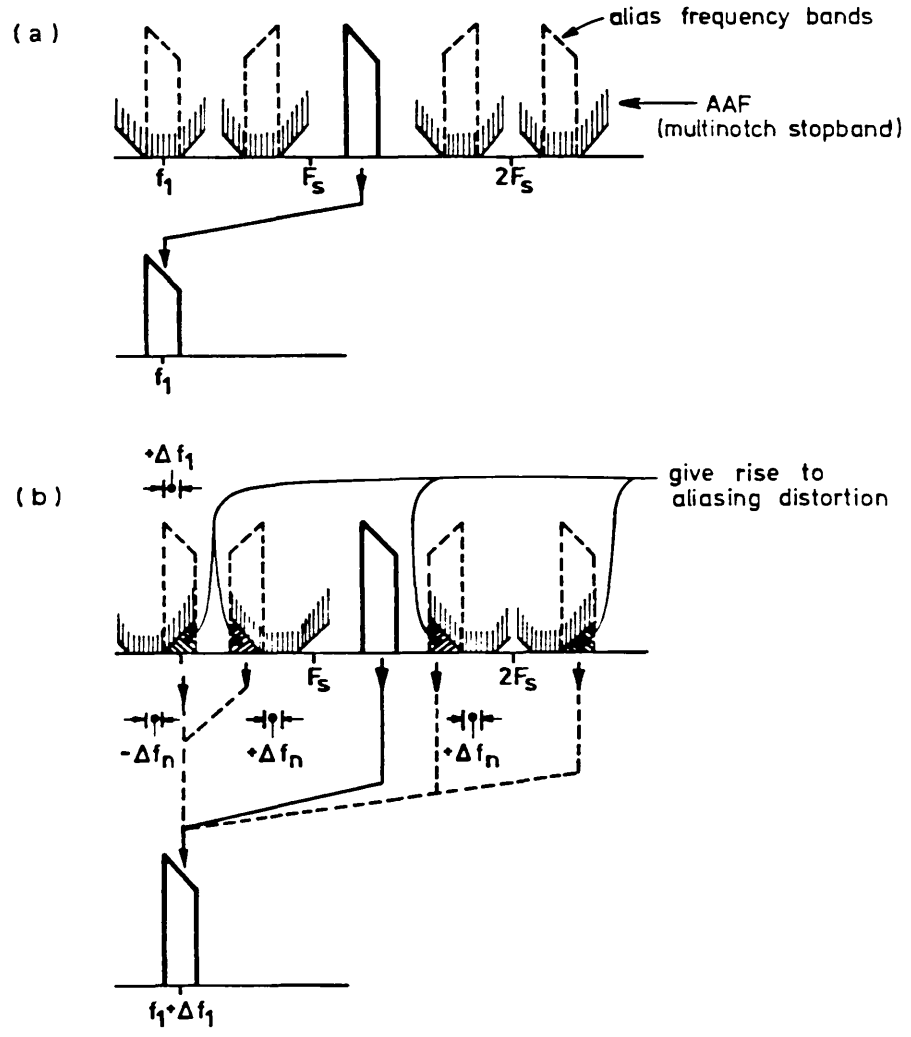


Fig.5.26: Effect of amplitude response variability on the rejection of alias signals. (a) Ideal situation corresponding to the SC bandpass filter and the SC decimator with nominal amplitude responses; (b) Worst case variations of midband frequency f_1, and notch frequencies f_n

frequency f_1 of the SC bandpass filter. For variations of $-\Delta f_n$ and $+\Delta f_1$ of the notch frequency and midband frequency, respectively, the rejection of the alias signals will be affected as shown in Fig.6.26-b. If we assume for this simple example $\left|\Delta f_n/f_n\right|=\left|\Delta f_1/f_1\right|=0.5\%$ then, the required notch stopband bandwidths at the more critical frequencies

are 136Hz at 4KHz, 176Hz at 12KHz, 256Hz at 28KHz, and 296Hz at 36KHz. Hence, from the curves in Fig.5.25-b, the maximum rejection that may be achieved using this FIR SC bandpass decimator is about 42dB at 4KHz, and about 37dB at 12KHz. For the complementary FIR SC bandpass interpolator, which could be obtained in a similar manner as was the decimator, we have to consider, in addition to the above constraints, the effect of the sample and hold attenuation. As a result, the practical anti-imaging performance is reduced by 14dB at 4KHz, and by 4.4dB at 12KHz, which gives a maximum rejection of the image signals of about 28dB at 4KHz, and about 32dB at 12KHz.

One possible solution for increasing the selectivity of the above FIR SC decimator (and of the corresponding interpolator) would be, for example, to introduce extra notch frequencies in the FIR SC highpass decimator M=3, e.g. at 8KHz. This implies increasing the length of the corresponding impulse response which, in turn, leads to more complex SC circuits because of the sophistication of the switching schemes. An alternative possible solution consists of utilising the SC highpass notch decimator M=3, as well as the complementary SC interpolator L=3, with SC biquad-polyphase structures, which we described in Section 4.6. An even simpler solution consists of employing solely an IIR SC highpass notch biquad, which we shall describe in the next Section.

5.6. SPFT SC BANDPASS FILTER SYSTEM 2: Experimental demonstration using a simplified architecture

For a preliminary experimental demonstration of the SPFT system, we shall consider the architecture shown in Fig.5.27. This system provides a specified rejection of

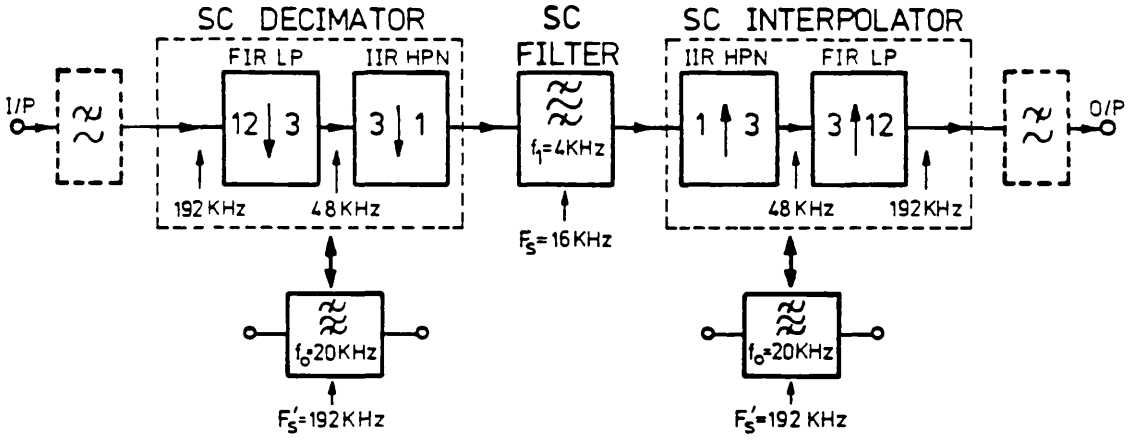


Fig.5.27: Simplified architecture for SPFT system 2, with combined FIR and IIR SC circuits for decimation and interpolation

unwanted alias and image frequency-translated components up to only 192KHz. In practical terms, this means that the selectivity of the continuous-time filters in the AAF and AIF would have to be increased in order to provide the extra attenuation that, otherwise, would have been achieved by the FIR SC lowpass decimator and interpolator circuits with M=L=2. The IIR SC circuits, which replace the FIR SC highpass circuits in the previous system, are based on the SC highpass notch (HPN) biquad shown in Fig.5.28. Both the SC biquads for the decimator and for the interpolator, with

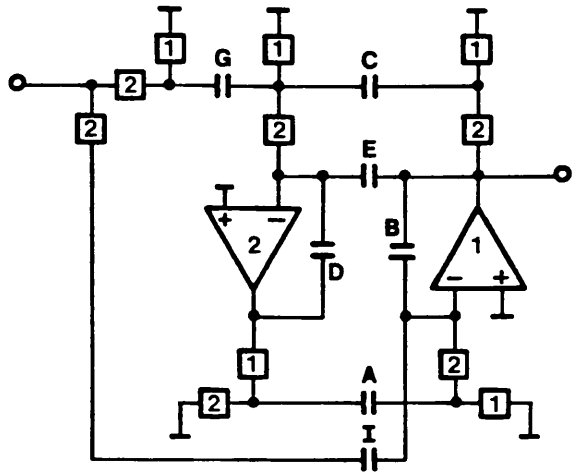


Fig.5.28: SC highpass notch biquad with Type-B switching

switching frequency $3F_s$=48KHz, pole frequency f_p=20KHz, notch frequency f_z=8KHz, and maximum signal handling capability, have their discrete-time biquadratic transfer functions obtained from the continuous-time domain using the bilinear s̃-to-Z transformation. The SC HPN biquad for interpolation is designed with pole quality-factor Q_p=50, and a gain of 14.89dB, in order to compensate for the midband gain error of the desired image at f_o=20KHz, and to provide a minimum rejection of 32dB of the image signals at 4KHz and 12KHz. The resulting normalised capacitance values are given in Table 5.4. The SC HPN biquad for decimation has a lower selectivity corresponding to Q_p=20, because in the decimator it is not necessary to compensate for the sample and hold attenuation. The design of this SC biquad with a gain of 0dB would give a very large capacitance spread of 153; instead, based on the discussion in Section 3.6, we design it with the minimum capacitance

spread of 28.1 yielding a gain of 14.75dB in the SC decimator, and in the system. The resulting normalised capacitance values are also given in Table 5.4.

	HPN-Q_p=50		HPN-Q_p=20	
ICS-1	A	24.5274	A	15.0080
	B	12.8618	B	8.0227
	I	1	I	1
ICS-2	C	71.1027	C	28.0752
	D	37.2853	D	15.0080
	E	1	E	1
	G	1.5	G	1

Table 5.4: Normalised capacitance values for the SC HPN biquads in the SPFT system 2

The measured frequency responses of both SC HPN biquads realised with discrete component models are shown in Fig.5.29. The FIR SC lowpass decimator M=4 and the FIR SC lowpass interpolator L=4 employing non-recursive polyphase direct-form structures were experimentally demonstrated in

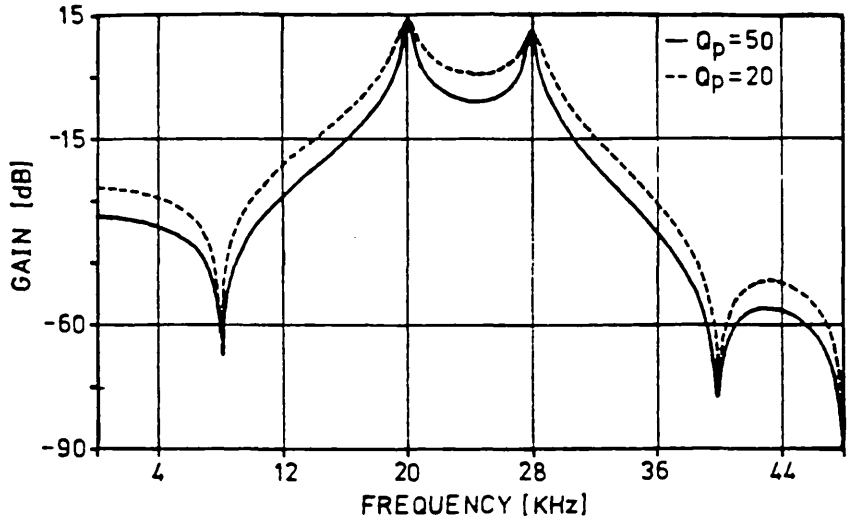


Fig.5.29: Measured baseband amplitude responses of the SC HPN biquads

the previous Chapter (respectively in Fig.4.25, and Fig.4.30, in Section 4.5). The measured baseband amplitude response of the FIR SC lowpass decimator, for example, is repeated in Fig.5.30. The resulting measured overall amplitude response of the complete SC bandpass decimator M=12 is given in Fig.5.31. A similar bandpass amplitude response is obtained for the interpolator.

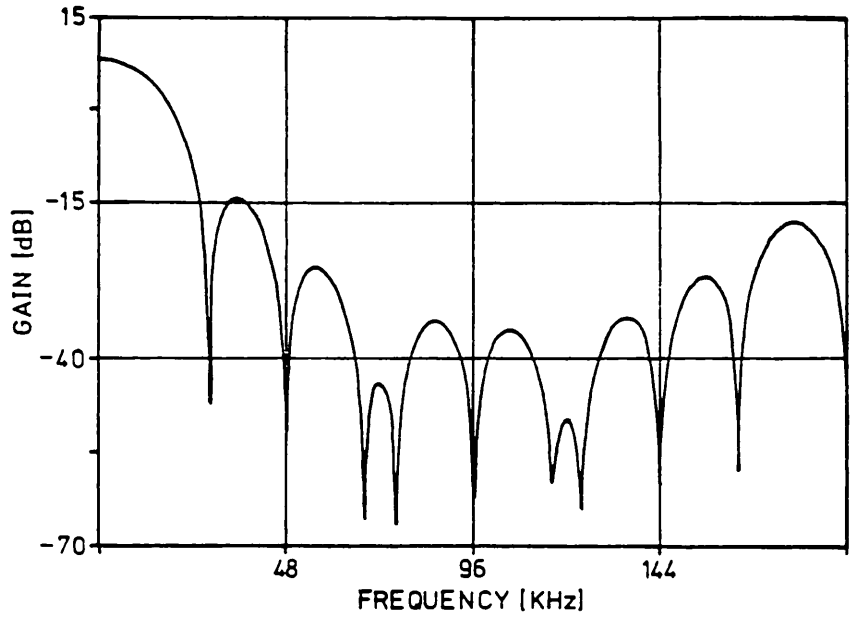


Fig.5.30: Measured baseband amplitude response of the FIR SC lowpass decimator M=4

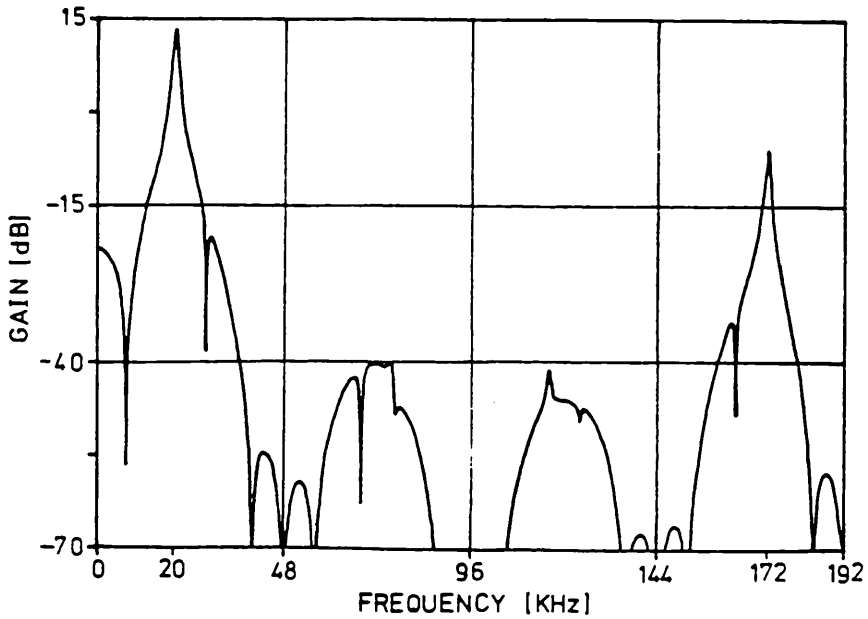


Fig.5.31: Measured overall baseband amplitude response of the complete SC bandpass decimator M=12

The complete schematic of the demonstration SPFT SC bandpass filter system is given in Fig.5.32-a; Fig.5.32-b shows the periodic time frames, with time slots, that represent the switching waveforms of each SC circuit in the system. The synchronisation of the time frames, which ensures the proper operation of the various SC circuits, illustrates the decimation and interpolation processes in the time domain. For example, the FIR SC lowpass decimator with time frame TF1 samples the input signal in time slots 1,2,3 and 4 (thus at a rate 192KHz) and produces only one output sample in time slot 5, which is sampled by the subsequent SC HPN biquad. Then, one in each three output samples of the SC HPN biquad, at 48KHz, are sampled by the SC bandpass filter at 16KHz. For interpolation, we can easily observe the converse process of producing twelve samples for each sample taken at the output of the SC bandpass filter. A discrete component model of the SPFT system of Fig.5.32 was built using CMOS 4016 analogue switches, CMOS 7611 OA's for the bandpass filter, BiMOS 3140 OA's for the decimator and interpolator and standard CMOS digital circuits for the switching circuitry. A summary of the capacitance spread and total normalised capacitance of each SC circuit in the system are given in Table 5.5.

For an input signal level of 100mV rms, we obtained the measured amplitude response of the SPFT filter system with midband frequency of 20KHz shown in Fig.5.33, which is compared with the frequency response of the SC bandpass

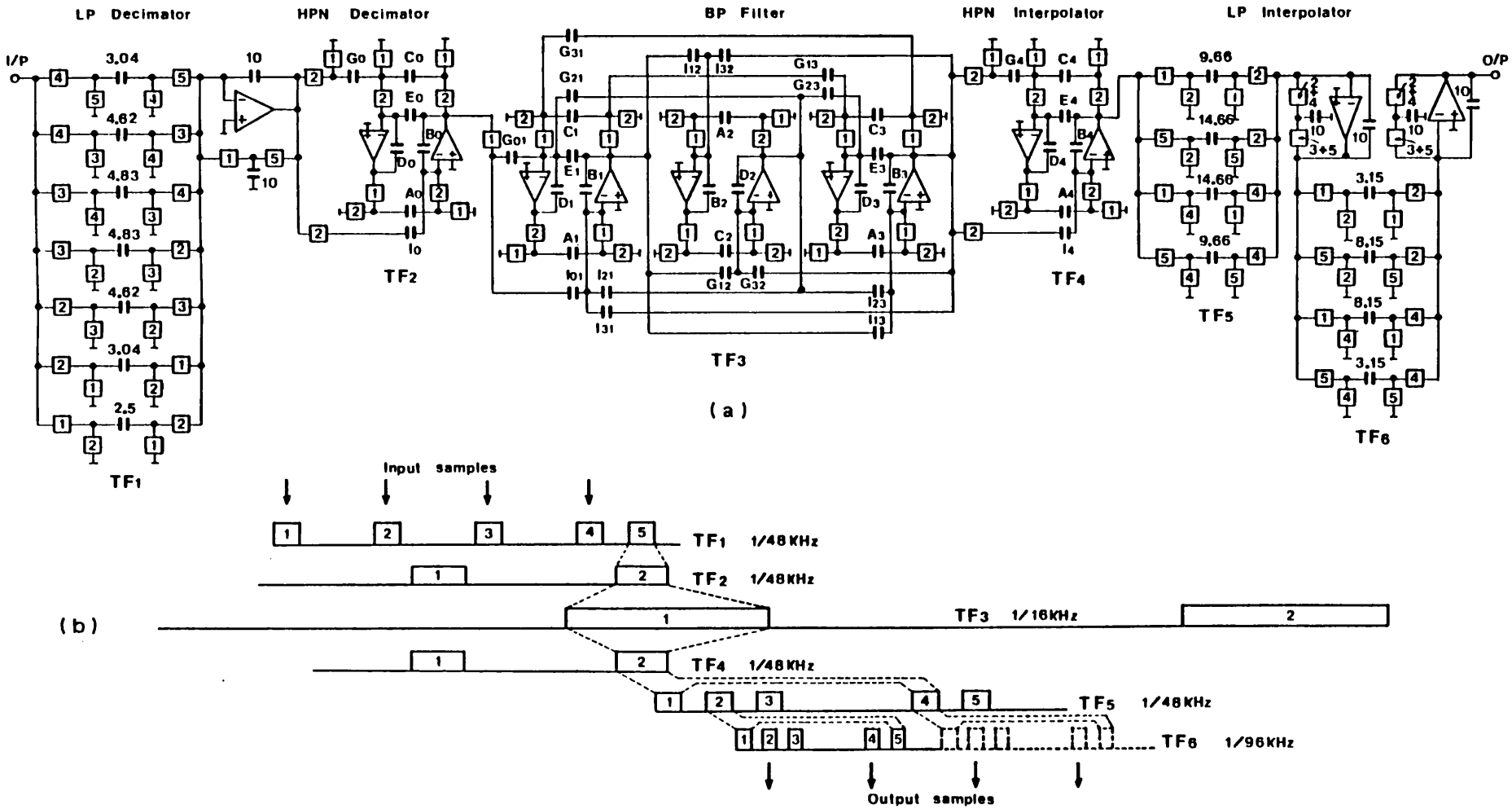


Fig.5.32: (a) Schematic of the demonstration SPFT SC bandpass filter system 2; (b) Time frames of SC circuits, illustrating the processes of decimation and interpolation in the time-domain

	Decimator		Bandpass	Interpolator		SPFT
	LP	HPN	Filter	HPN	LP	System
C-spread	4	28.1	87.8	71.1	3.2	87.8
Total-C	19	69.2	884	149.3	26.1	1147.6

Table 5.5: Capacitance spread, and total normalised capacitance of the SPFT filter system 2

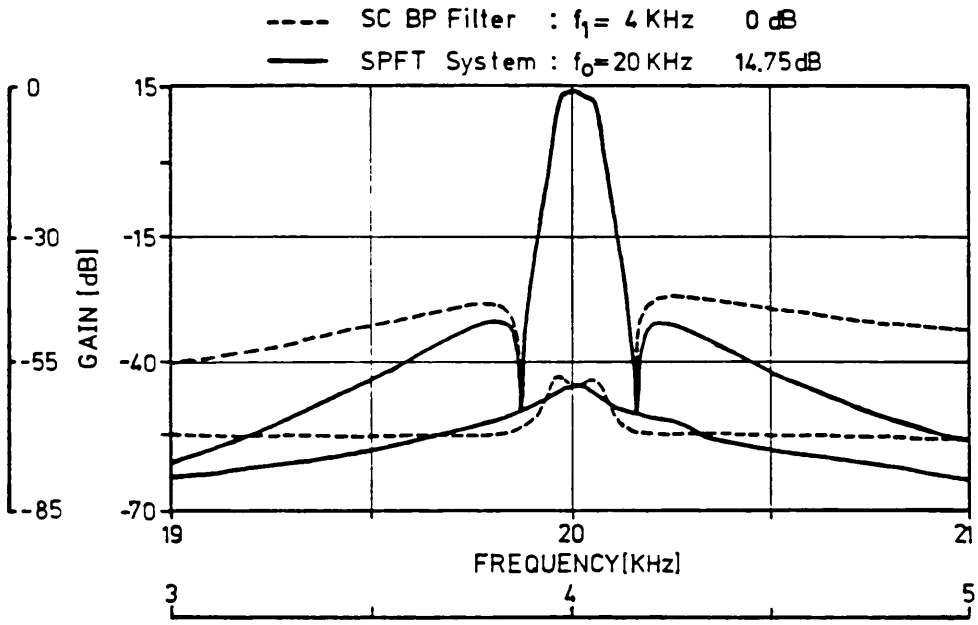


Fig.5.33: Measured amplitude responses, and noise performances, of the SPFT system 2, and of the SC bandpass filter alone at 4KHz

filter alone with midband frequency of 4KHz. The increased stopband attenuation of the SPFT system is due to the attenuation of the SC decimator and interpolator. The noise measurements of the SC bandpass filter alone, and of the SPFT filter system are also shown for comparison (measuring bandwidth of 10Hz). The passband noise of the SC bandpass filter is preserved in the passband of the SPFT filter system, which corresponds to a dynamic range of about 75dB. In the frequency bands corresponding to the

transition bands of the SC decimator and interpolator there is an expected increase of the noise in the SPFT system, but in the stopband of the system it reduces to a lower floor than in the SC bandpass filter alone, as was also expected. The measured worst-case levels of frequency translated signals were -32dB for aliasing at 12KHz and -34dB for imaging at 12KHz, as we expected from the design of this SC decimator and of this SC interpolator.

5.7 SPFT SC BANDPASS FILTER SYSTEM 3: Efficient design for high quality filtering applications

5.7.1 FIR versus IIR SC circuits for decimation and interpolation

The relative merit of FIR and IIR SC circuits for decimation and interpolation can be summarised as follows: FIR SC circuits offer the most economical implementation of decimators and interpolators, both with respect to capacitance spread, and total capacitor area, and with respect to the number of OA's that are needed. However, they have a practical drawback in the sophistication of their switching schemes. For acceptable complexity of the switching circuitry, the selectivity of FIR SC circuits is adequate for applications where it is sufficient to place single notch frequencies at the centre of the unwanted alias and image signals, such as when the frequencies of such signals are close to the stopband of the continuous-time filters. Hence, FIR SC circuits are especially attractive as front end stages in complex decimator and

interpolator architectures. Such a requirement for high operating speed can be achieved without too much difficulty because of the non-recursive nature of FIR SC circuits available for implementation.

The advantage of IIR SC circuits results from their recursive nature, which allows high selectivity amplitude responses to be achieved with low order circuits using much simpler switching schemes. But, on the other hand, IIR SC circuits need more OA's, and occupy much larger areas of silicon than FIR SC circuits. Besides, they are also more affected by amplifier imperfections. Therefore, IIR SC circuits will be employed for operation below the operating frequency range of FIR SC circuits, where their selectivity advantage easily complements the poorer selectivity of simple FIR SC circuits.

5.7.2 System architecture

Bearing in mind the above characteristics of the FIR and IIR SC circuits, we shall now consider an SPFT system with the architecture shown in Fig.5.34. As in the architecture of SPFT system 1, we consider an FIR SC lowpass decimator M=2 and an FIR SC lowpass interpolator L=2, in order to obtain a high sampling rate of 384KHz at the input and at the output of the system. With respect to the previous architectures for decimation, for example, we have now replaced the cascade of SC lowpass and highpass decimators with sampling rate reduction factors of M=4 and M=3, respectively, by one SC bandpass decimator with factor M=12 of sampling rate reduction. In complement to this

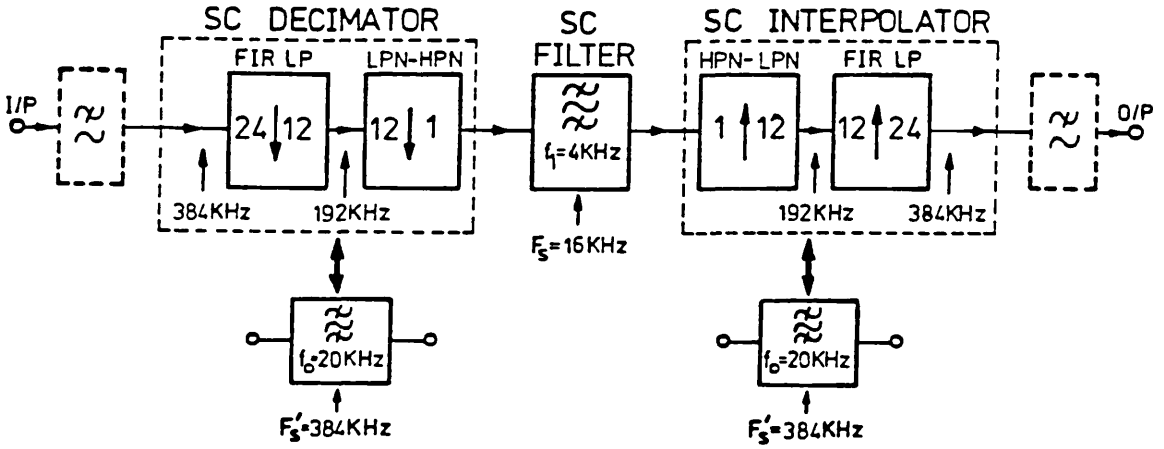


Fig.5.34: Architecture of SPFT system 3, for high operating speed, and improved rejection of the unwanted alias and image signals

decimator, we have also an SC bandpass interpolator with a factor L=12 of sampling rate increase. Such decimator and interpolator are implemented using IIR SC circuits consisting of the cascade of a highpass notch (HPN) biquad and a lowpass notch (LPN) biquad, as shown in Fig.5.35.

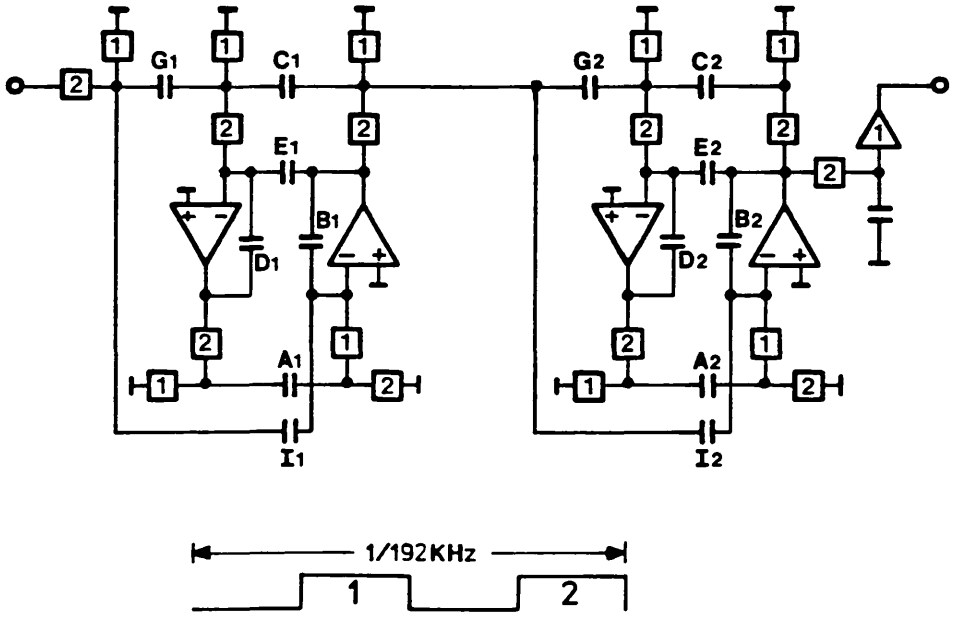


Fig.5.35: Cascade of an SC HPN biquad and an SC LPN biquad, with Type-A switching

The transfer functions of the SC biquads are optimised in order to achieve a minimum rejection of 50dB of the unwanted alias and image signals in the baseband from DC to 96KHz, and the corresponding repetitions above 96KHz. The steps required to derive these transfer functions are summarised below.

We start with a complex conjugate pole-pair in the continuous-time domain, Fig.5.36-a, corresponding to a 2nd. order Chebyshev polynomial T/02/15/b, with normalised pole frequency and maximum passband ripple of 0.1dB [5.2]. By using a lowpass-to-bandpass frequency transformation [5.2], we obtain two complex conjugate pole-pairs, shown in Fig.5.36-b, as a function of the equivalent Q-factor Q of the bandpass response. The midband frequency f_o coincides with the system midband frequency. Then, for the switching frequency $12F_s$=192KHz required for the SC biquads, we obtain the corresponding complex conjugate pole-pairs in the discrete-time domain via the $\tilde{s}$-to-Z bilinear transformation, in order to ensure accurate mapping of the passband response. This is illustrated in Fig.5.36-c, where each complex conjugate pole-pair corresponds to the quadratic denominator function of each SC biquad. Finally, in Fig.5.36-d, we introduce the notch frequencies producing the quadratic numerator functions. A notch frequency below the pole frequency gives the transfer function for the HPN SC biquad, whereas a notch frequency above the pole frequency gives the transfer function for the LPN SC biquad. As in (3.1), Section 3.3, the general discrete-time

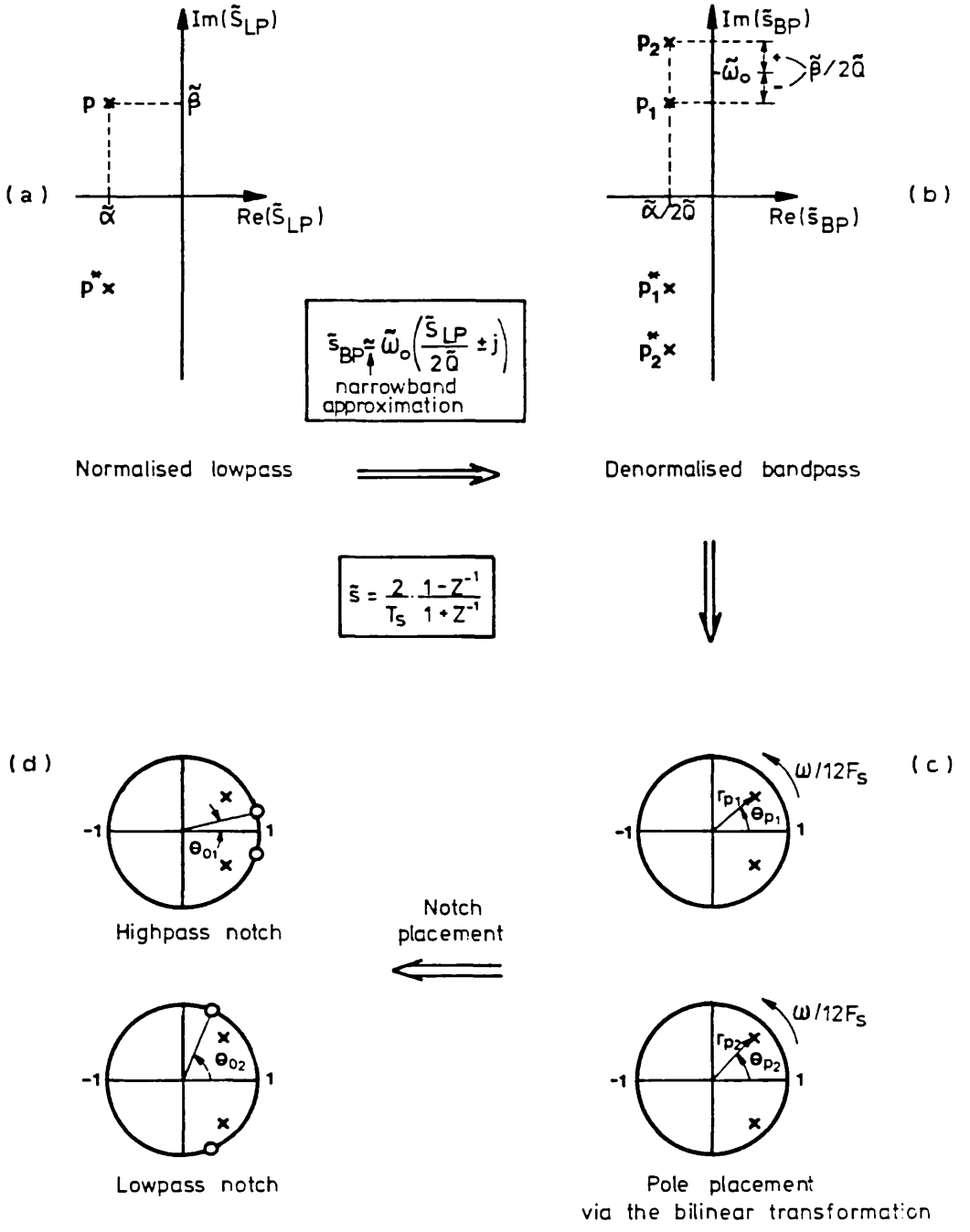


Fig.5.36: Derivation of the IIR transfer functions for decimation and interpolation in the SPFT system 3. In the continuous-time domain, the original complex conjugate pole-pair (a) is transformed into the complex conjugate pole-pairs (b) using a lowpass-to-bandpass frequency transformation; (c) Corresponding bilinear transformed complex conjugate pole-pairs; (d) Notch placement to form the lowpass notch, and the highpass notch biquadratic transfer functions

biquadratic transfer function for the SC biquads is

$$(5.6)\ \ldots \qquad H(Z) = K \frac{1-2r_o \cos\theta_o Z^{-1}+r_o^2 Z^{-2}}{1-2rp \cos\theta_p Z^{-1}+r_p^2 Z^{-2}}$$

The optimised discrete-time biquadratic parameters given in Table 5.6 for the SC biquads in the decimator and interpolator, are obtained by trial-and-error whereby we adjust the selectivity of the corresponding bandpass responses (Q-factor), as well as the placement of the notch frequencies. Here, we have to take into account the higher selectivity for the interpolator, which is required to compensate for the midband gain error of α=-14.89dB due to the sample and hold attenuation of the selected image.

	DECIMATION		INTERPOLATION	
	LPN	HPN	LPN	HPN
K	0.070862	0.057194	0.069894	0.098008
$2r_o\cos\theta_o$	1.111141	1.893860	1.931852	0.825414
r_o^2	1	1	1	1
$2r_p\cos\theta_p$	1.548121	1.584208	1.557692	1.584886
r_p^2	0.974497	0.974237	0.980786	0.980639

Table 5.6: Optimised discrete-time biquadratic parameters for the IIR transfer functions for decimation and interpolation, in the SPFT system 3

Overall, the IIR SC decimator and interpolator circuits have 4th. order bandpass amplitude responses with the characteristics indicated in Table 5.7. Both SC biquads in decimator, on the one hand, and both SC biquads in the interpolator, on the other hand, are designed with equal

	LPN-HPN SC Decimator	HPN-LPN SC Interpolator
Midband frequency	20KHz	20KHz
Gain	0dB	14.89dB
-3dB bandwidth	1300Hz	1000Hz
Lower notch frequency	10KHz	8KHz
Upper notch frequency	30KHz	35KHz

Table 5.7: Characteristics of the IIR SC circuits for decimation and interpolation

capacitance spread, which we achieve by adjusting the gain factors of the respective cascade sections. The resulting normalised capacitance values of the SC HPN biquads and of the SC LPN biquads for the decimator and interpolator are given in Table 5.8.

		DECIMATION		INTERPOLATION	
		LPN	HPN	HPN	LPN
ICS-1	A	24.88	4.0442	2.5438	23.4824
	B	38.103	6.4756	3.9108	37.3276
	I	1	1	1	1
ICS-2	C	18.2775	23.796	24.2800	20.4414
	D	27.991	38.103	37.3276	32.4937
	E	1.093	1.5718	1.1026	1
	G	1	1	1	1.6253

Table 5.8: Normalised capacitance values for the SC HPN biquads and the SC LPN biquads

5.7.3 Experimental evaluation

The schematic of this SPFT SC bandpass filter system (apart from the continuous-time filters) is given in

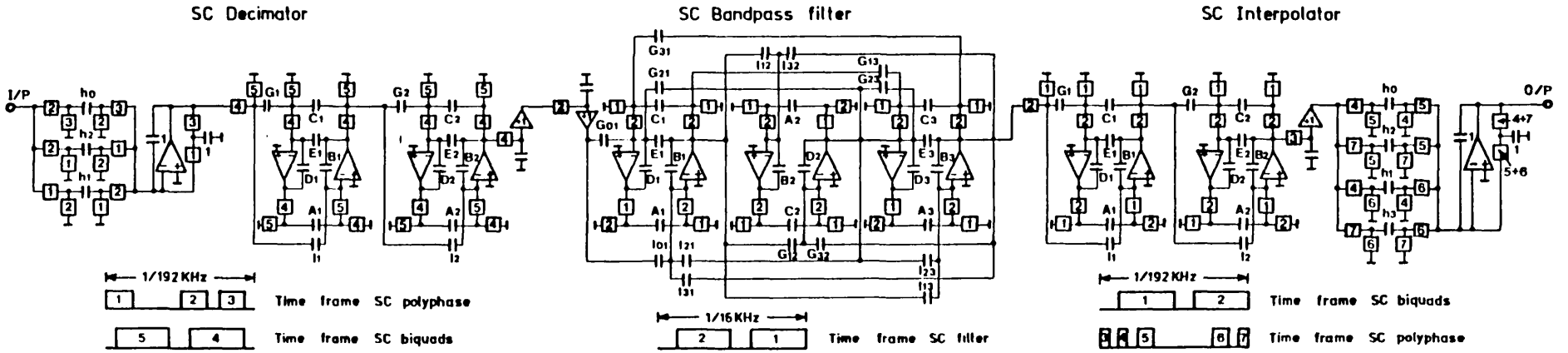


Fig.5.37: Schematic of the SPFT SC bandpass filter system 3, using an efficient architecture for decimation and interpolation giving a minimum of 50dB rejection of all unwanted alias and image signals up to 364KHz

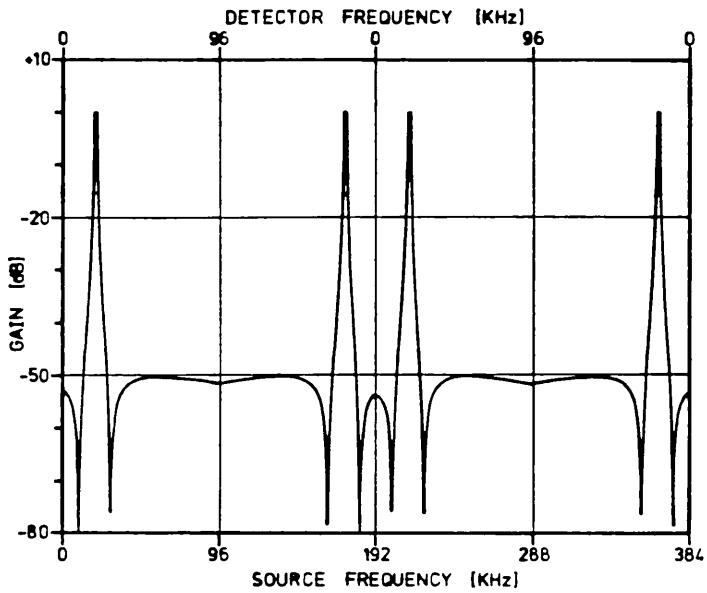
Fig.5.37. The two interstage sample and hold circuits are needed in order to guarantee the required input and output sampling conditions of the SC circuits. A fully synchronised switching scheme would have eliminated such sample and hold circuits but, on the other hand, it would not have provided a capability for independent programming of the switching frequency of the SC decimator and of the SC interpolator, which we require for demonstrating further applications of the SPFT system in the next Section. A discrete component model of the system was constructed using CMOS 4016 analogue switches, CMOS 7611 OA's for the SC bandpass filter and for the IIR SC decimator and interpolator circuits, BiMOS 3140 OA's for the FIR SC circuits and standard CMOS digital components for the switching circuitry. The capacitance spread and total normalised capacitance for each SC circuit, and for the complete system, are given in Table 5.9.

	SC Decimator			SC Bandpass	SC Interpolator			SPFT
	FIR	LPN	HPN	Filter	HPN	LPN	FIR	System
C-spread	3.8	38.1	38.1	87.8	37.3	37.3	3.8	87.8
Total C	11.5	112.3	76.0	884.0	71.2	117.4	15.4	1287.8

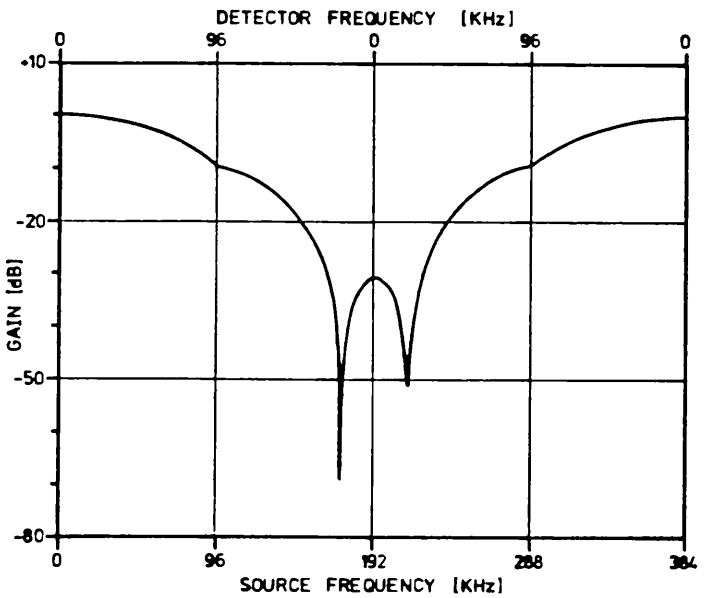
Table 5.9: Capacitance spread, and total normalised capacitance in the SPFT filter system 3

The anti-aliasing performance of the complete SC bandpass decimator M=24 in the SPFT system, which is measured using an appropriate alias sweeping mode, is shown in Fig.5.38. Fig.5.38-a shows the measured alias response

of the IIR SC bandpass decimator M=12, which selects the desired alias frequency-translated band at f_o=20KHz, and rejects the unwanted alias signals in the baseband up to 96KHz, and the corresponding repetitions above 96KHz. The FIR SC lowpass decimator M=2, with the measured alias

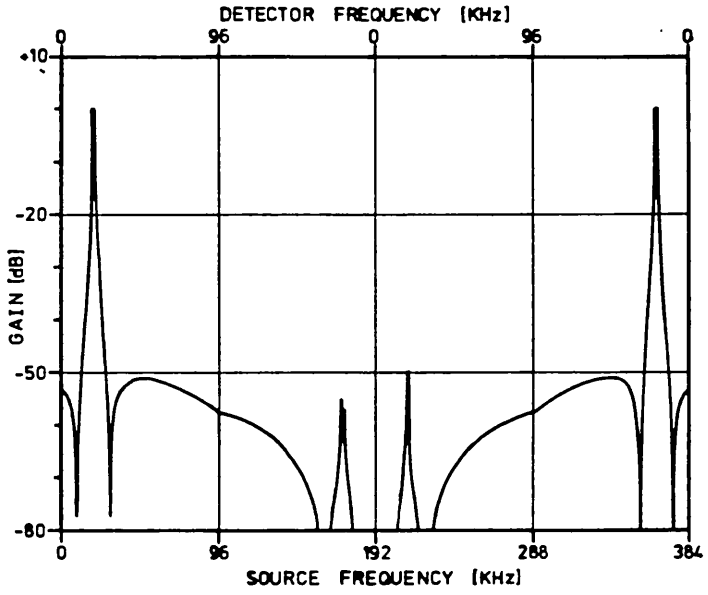


(a)



(b)

Fig.5.38: Measured anti-aliasing characteristics of the (a) IIR SC bandpass decimator M=12, and (b) FIR SC lowpass decimator M=2



(c)

Fig.5.38: (c) Measured overall anti-aliasing characteristic of the complete SC bandpass decimator M=24

response shown in Fig.5.38-b, rejects the remaining alias signals at 172KHZ, and at 212KHz. The overall anti-aliasing characteristic of this SC decimator is shown in Fig.5.38-c. In such measurements, the sample and hold function affects only the detection of the signals in the baseband from DC to 96KHz, and thus no notch frequencies appear at 192KHz or at 384KHz. The overall anti-imaging characteristic of the IIR SC bandpass interpolator L=24, which is measured using an appropriate image sweeping mode, is shown in Fig.5.39. This is shaped by the sample and hold function corresponding at the high rate $12F_s$=192KHz, which produces the notch frequencies at 192KHz and at 384KHz. The gain of 14.89dB at midband frequency f_o=20KHz is required for compensation of the sample and hold effect at lower sampling rate F_s=16KHz. Such effect also contributes to

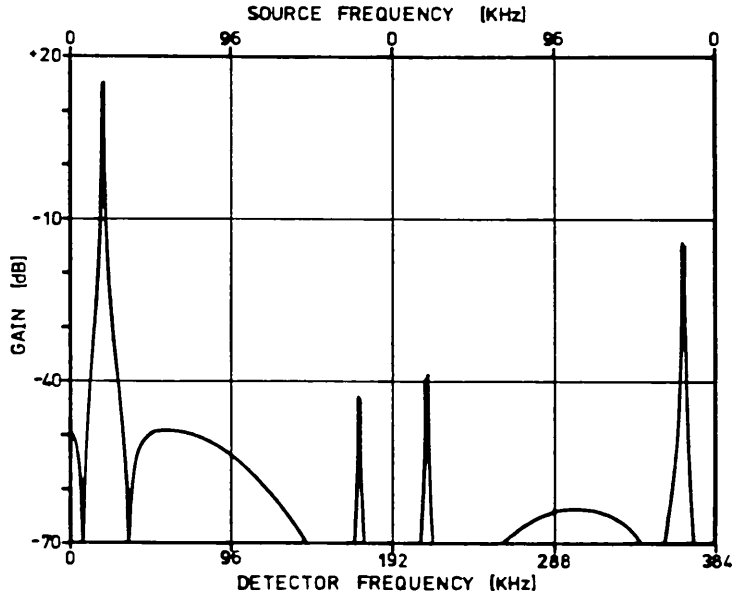


Fig.5.39: Measured overall anti-imaging characteristic of the complete SC bandpass interpolator L=24

attenuate all the image frequency-translated components above the midband frequency, yielding a minimum rejection of 55dB. Overall and expanded measured amplitude responses, and noise performance, of the SPFT system at 20KHz are given in Fig.5.40 and in Fig.5.41, respectively.

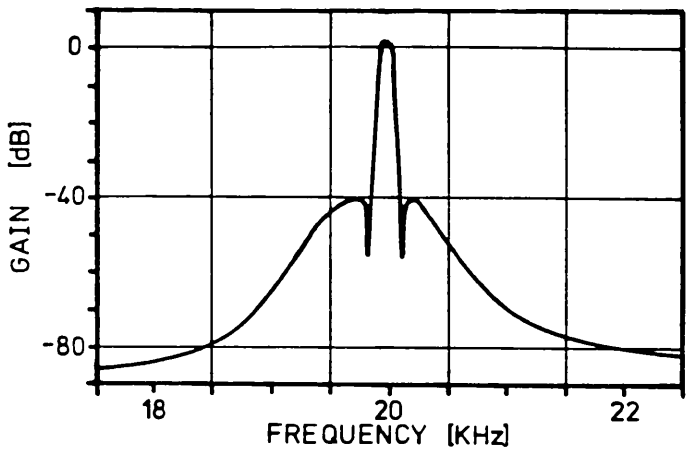


Fig.5.40: (a) Measured overall amplitude response of the SPFT filter system 3

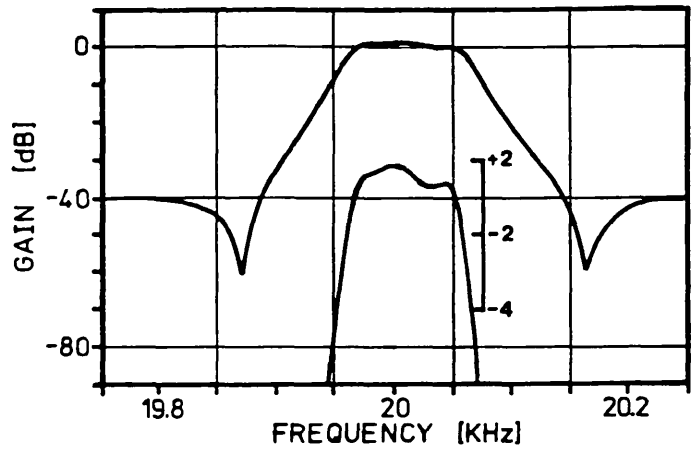


Fig.5.40: (b) Measured expanded amplitude responses

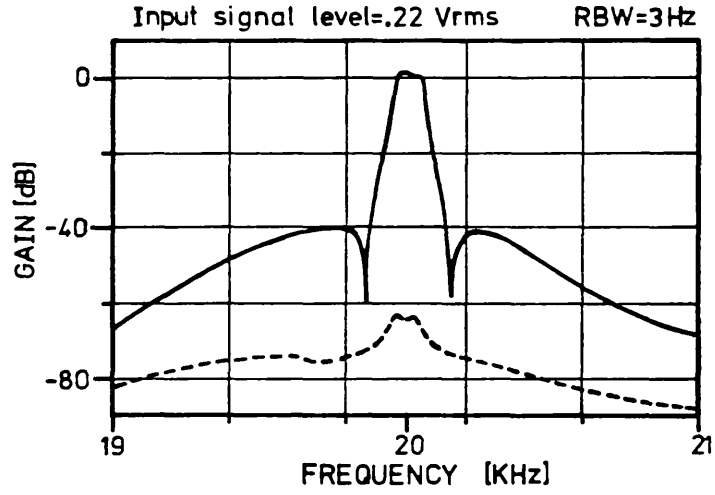


Fig.5.41: Measured noise performance of the SPFT filter system 3

As was also observed in the demonstration system described in the previous Section, the noise floor in the passband of the system is very similar to that of the SC bandpass filter alone, despite the reduction of the relative bandwidth. Table 5.10 summarises the measured results obtained for this SPFT SC bandpass filter system, showing the good performance both with respect to the accuracy of the bandpass response, and with respect to the dynamic range. Those results also demonstrate that the SC decimator and SC interpolator perform according to the

Midband frequency	20.007KHz
Gain	1.7dB
-3dB bandwidth	97Hz
Stopband rejection	>42dB
Power supply	±5V
Maximum input signal	1Vrms
Dynamic range	78dB
Aliasing rejection (<364KHz)	>50dB
Imaging rejection (<364KHz)	>50dB

Table 5.10: Experimental results of the SPFT SC bandpass filter system 3

anti-aliasing and anti-imaging specifications, as was also shown with their measured responses.

5.8 FURTHER APPLICATIONS OF SPFT SYSTEMS

5.8.1 Programmable Q-enhancement factor

We can program the SPFT filter system considered in the previous Section for a Q-enhancement factor K=3, as illustrated in Fig.5.42. The switching frequency of the SC bandpass decimator and interpolator has been reduced by a factor of 3/5, from 384KHz to 230.4KHz, in order to select the system midband frequency f_o=12KHz. The corresponding -3dB relative bandwidth is 0.8%. The two consecutive frequency translations with spectral inversion lead to a direct correspondence between the spectra at the input and at the output of the system, but the shape of the bandpass amplitude response corresponding to the inverted image at 12KHz will be inverted. Since we do not provide the means for adjusting the gain of the SC interpolator, the sample

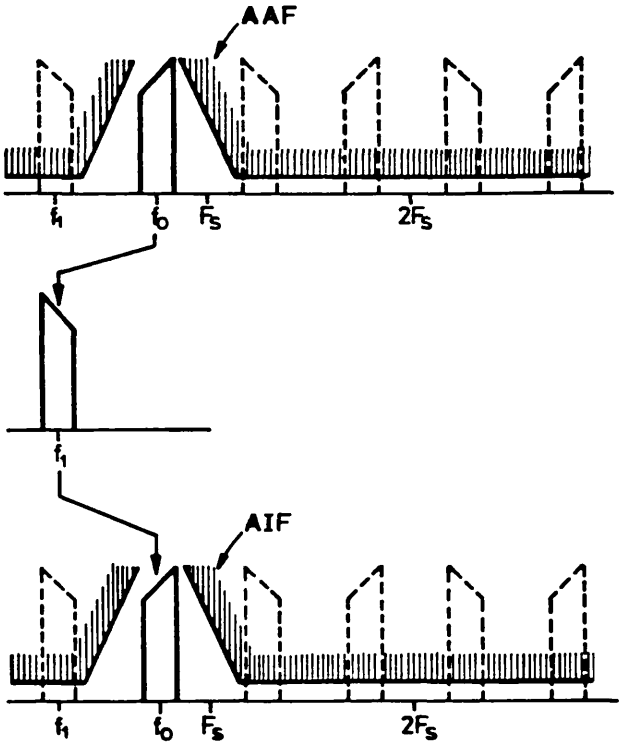


Fig.5.42: Illustration of the operation of the SPFT filter system with K=3: frequency-translated filtering with double spectral inversion

and hold effect will be overcompensated, which gives a midband gain of +4.4dB for the filter system. An expanded amplitude response, and the noise performance, of the SPFT SC bandpass filter system at 12KHz are shown in Fig.5.43. The 50dB rejection of the alias and image signals is obtained up to 230.4KHz-12KHz.

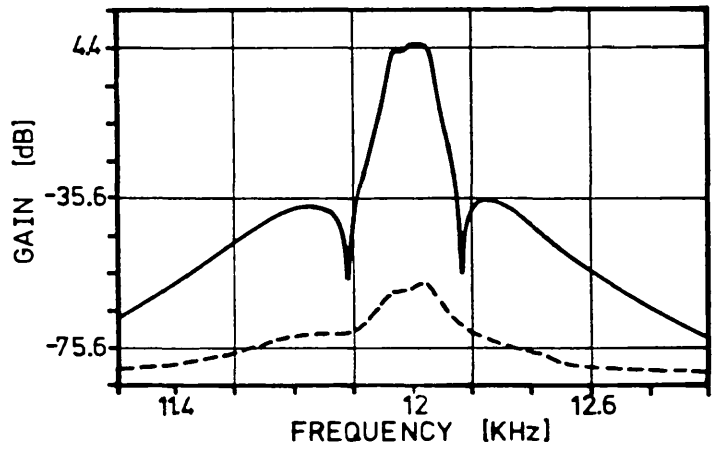


Fig.5.43: Measured amplitude response, and noise performance of the SPFT SC bandpass filter system at 12KHz, with -3dB relative bandwidth of 0.8%

5.8.2 SSB generator and detector

An SPFT system can operate also as an SSB generator and detector by selecting different frequency-translated bands at the input and at the output of the system. For example, in the SPFT system under consideration we can select the 12KHz alias frequency band at the input and the 20KHz image frequency band at the output, as illustrated in Fig.5.44-a. The single-path with upwards frequency-translation from 12KHz to 20KHz, with spectral inversion, is equivalent to an SSB generator, i.e. a modulator followed by an upper sideband filter. An SSB detector with complementary operation is illustrated in Fig.5.44-b, showing the generation of a single-path with downwards frequency-translation from 20KHz to 12KHz, also with spectral inversion. In the latter case, there will be also an increased gain of +4.4dB in the system, because of the overcompensated sample and hold effect. Expanded measured

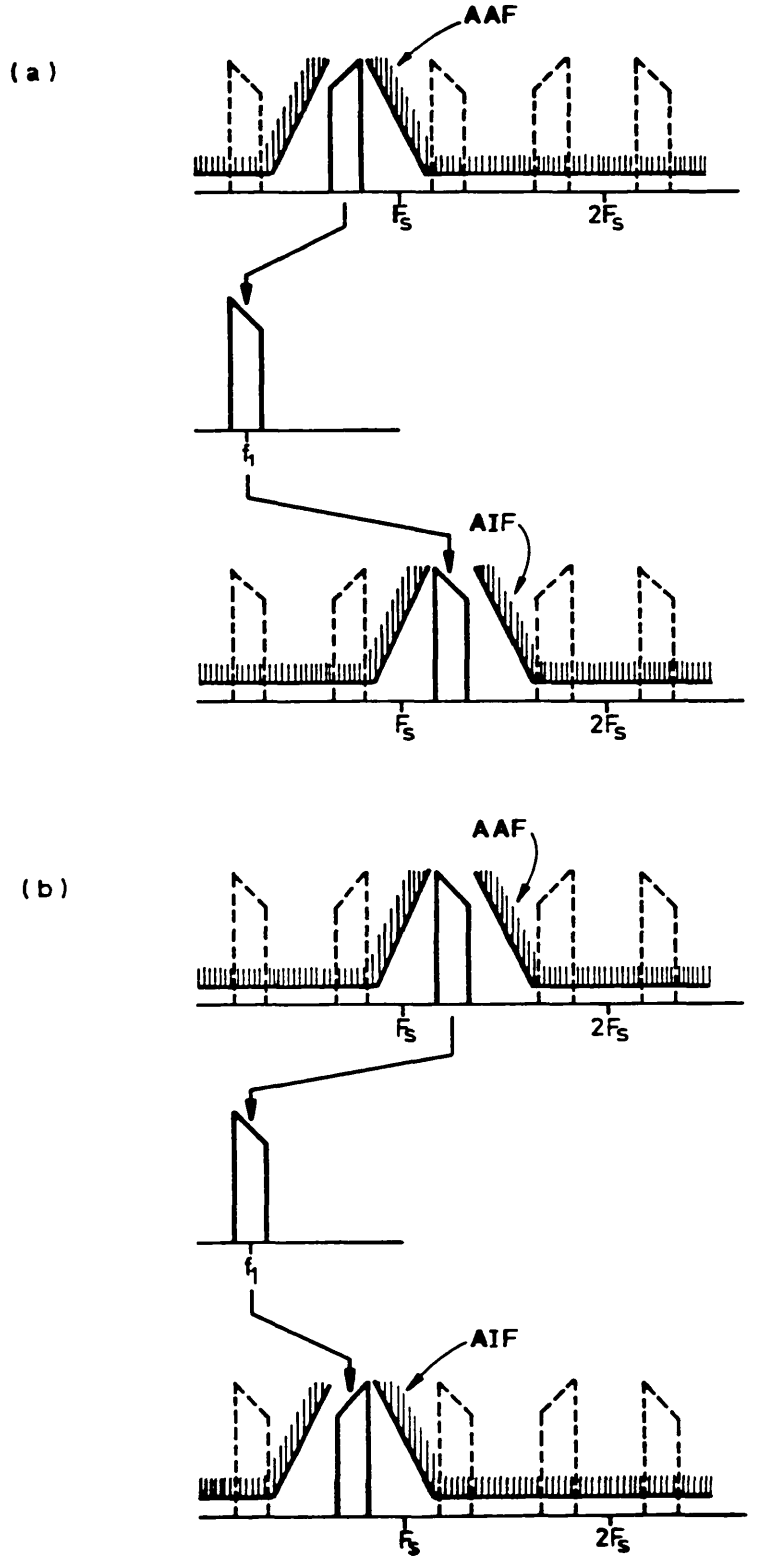


Fig.5.44: Schematic illustration of the operation of the SPFT SC system (a) as an SSB generator, corresponding to an upwards frequency-translation with spectral inversion, and (b) as an SSB detector, corresponding to a downwards frequency-translation also with spectral inversion

responses of the SPFT system in such operating modes are illustrated in Fig.5.45. For the response of the SSB generator, shown in Fig.5.45-a, the synthesised signal generator sweeps upwards from 11.5KHz to 12.5KHz corresponding to the input frequency band of the system, while the synthesised spectrum analyser sweeps downwards from 20.5KHz to 19.5KHz corresponding to the output

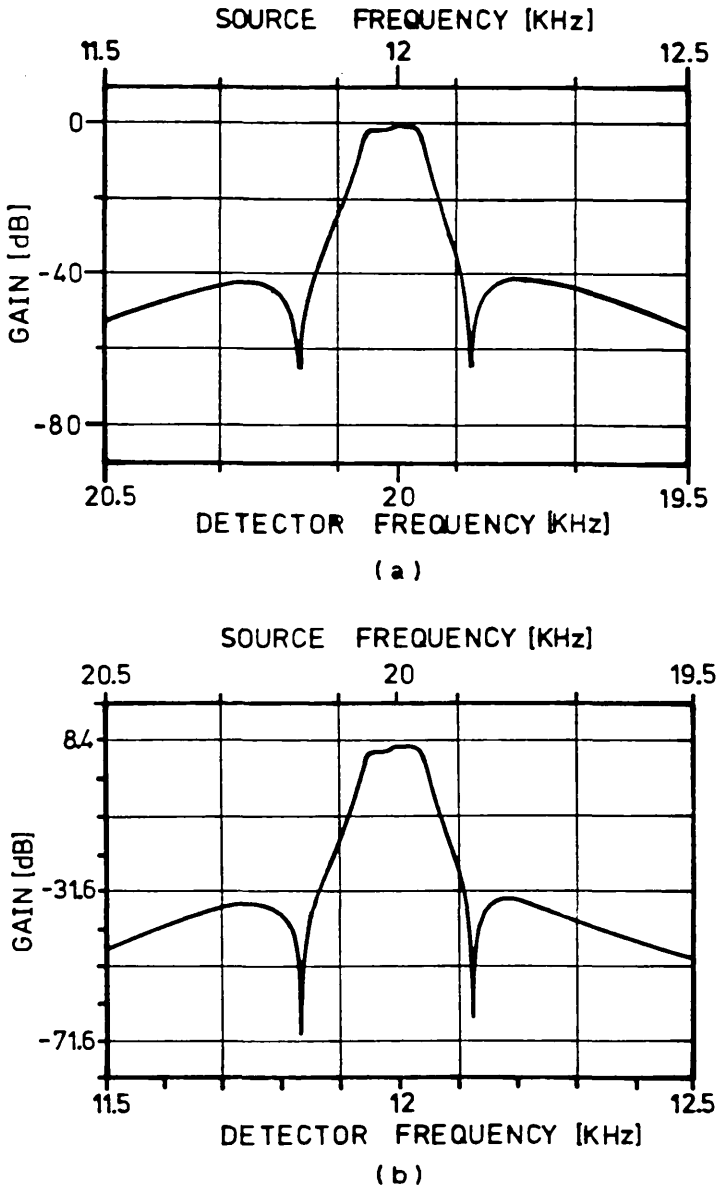


Fig.5.45: Measured amplitude responses of the SPFT SC system operating (a) as an SSB generator, and (b) as an SSB detector

frequency band of the system. Interchange of the sweeping modes of the signal generator and spectrum analyser gives the response of the SSB detector, shown in Fig.5.45-b. The combined wideband alias and image responses shown in Fig.5.46-a and in Fig.5.46-b, respectively, for the SSB generator, and, in Fig.5.47-a and in Fig.5.47-b for the SSB detector, show that the unwanted alias and image signals are less than 50dB below the passband signals, as expected from the design of the SC decimator and interpolator in the system.

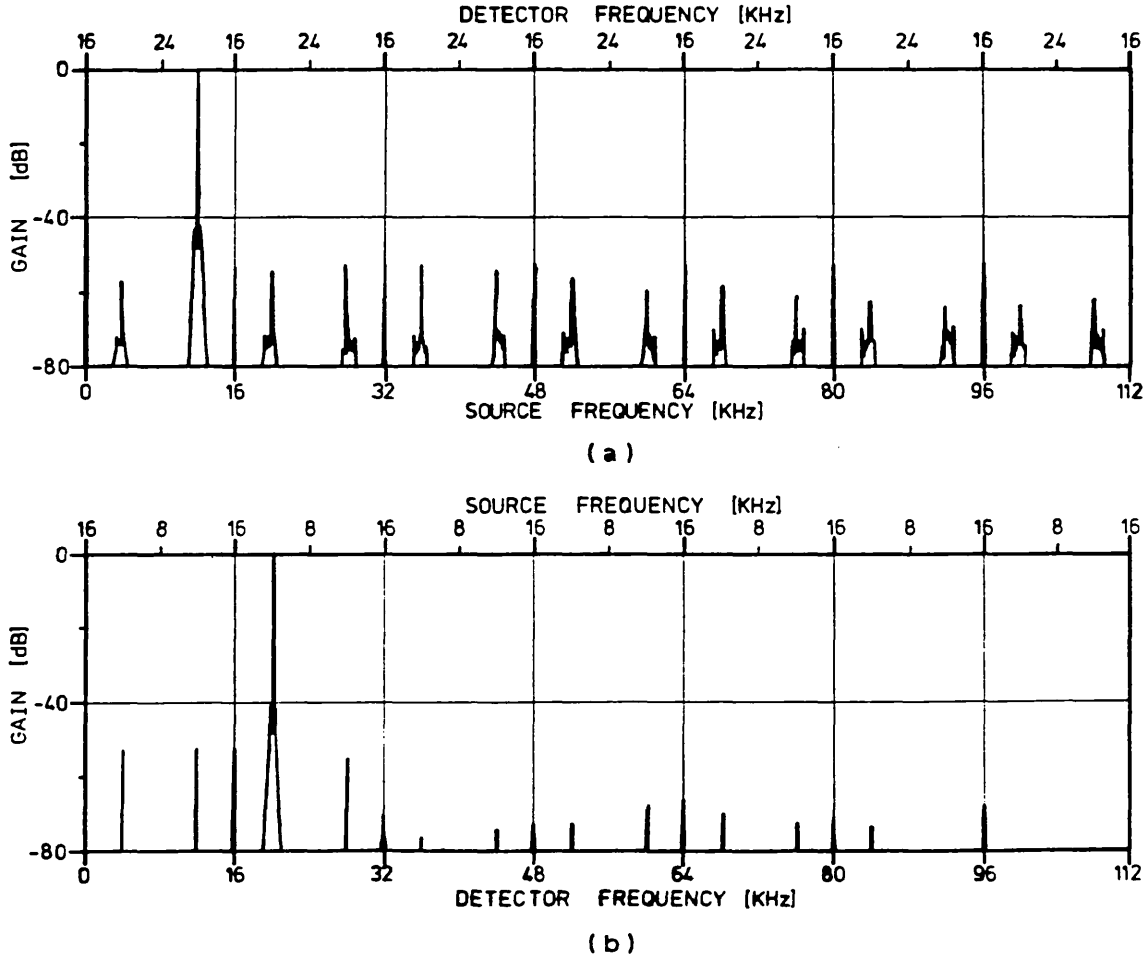


Fig.5.46: Measured wideband (a) alias, and (b) image responses of the SPFT SC system operating as an SSB generator

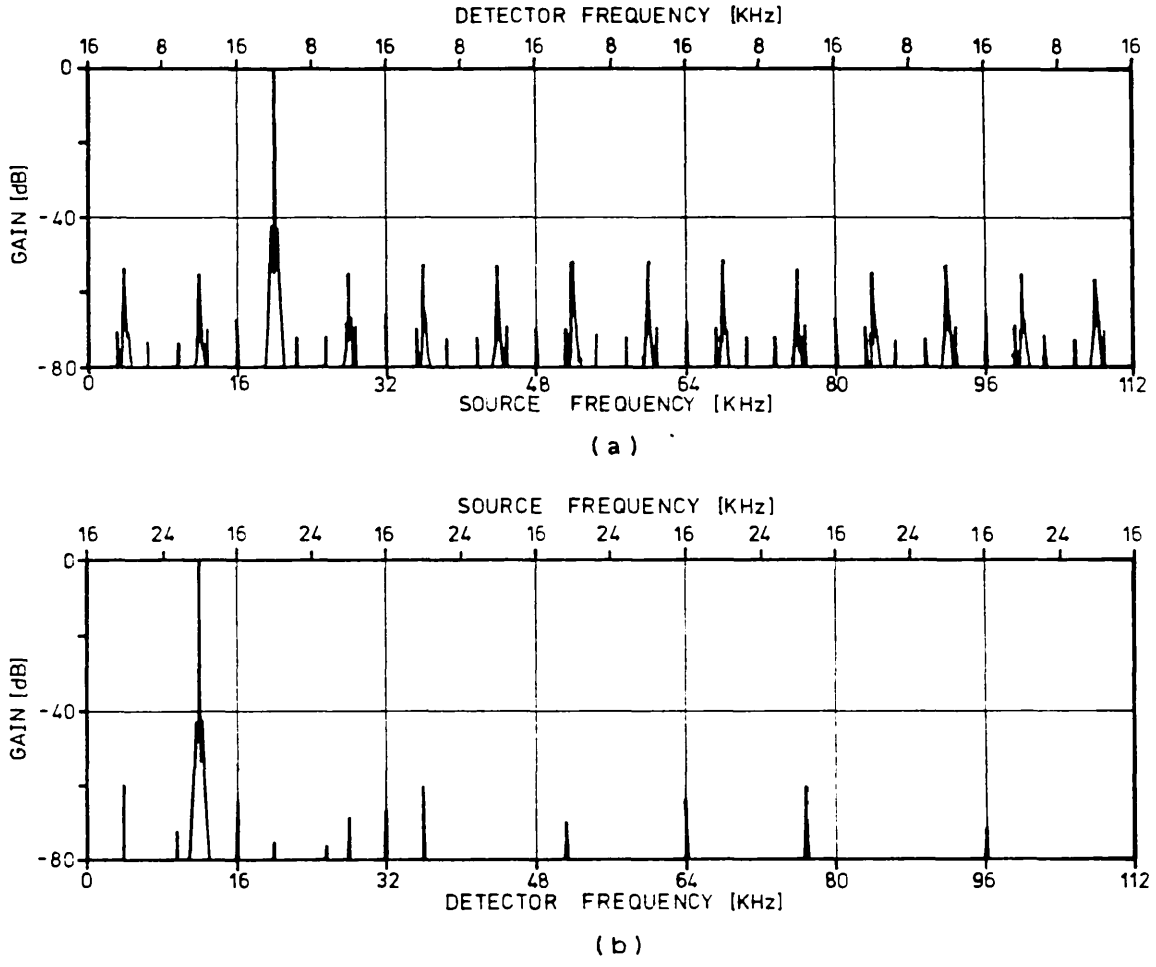


Fig.5.47: Measured wideband (a) alias, and (b) image responses of the SPFT SC system operating as an SSB detector

5.9 SUMMARY

This Chapter was concerned with the design and implementation of single-path SC bandpass filter systems with relative bandwidths below 10%. Narrow bandpass responses are realised using SC bandpass filter systems operating in a baseband filtering mode. For such systems, we proposed employing an SC bandpass filter with optimised capacitance spread, in combination with FIR SC lowpass

decimators and interpolators, which are optimally designed for maximum rejection of those unwanted alias and image signals which can not be attenuated by low selectivity continuous-time filters in the AAF and AIF, respectively. Experimental results demonstrated the feasibility of the proposed SC bandpass filter system yielding, overall, good performance with respect to amplitude response accuracy, dynamic range, and anti-aliasing and anti-imaging characteristics.

SPFT SC bandpass filter systems were proposed for the realisation of very narrow bandpass responses. In SPFT systems, we deliberately employ the alias and image frequency-translated responses of an SC bandpass filter, also with optimised capacitance spread, in order to produce the required bandpass response at a much higher frequency, and having a correspondingly smaller relative bandwidth. In spite of such a reduction of the relative bandwidth, it was demonstrated that the maximum noise floor of the SC bandpass filter is preserved in the SPFT system, thus offering a solution for very high selectivity filtering applications which also require high dynamic range. The specifications for rejection of the unwanted alias and image signals in SPFT systems are entirely met by suitable design of bandpass AAF and AIF. The AIF is required to have higher selectivity than the AAF in order to compensate for the sample and hold attenuation of the desired image, which, although preventing unlimited applicability of SPFT systems, can be achieved in practice for a wide range of

filtering specifications. For example, for a maximum realistic Q-enhancement factor of about K=28 (α=-30dB), and employing an SC bandpass filter with a minimum relative bandwidth of 1% for acceptable capacitance spread and tolerable sensitivity to capacitance ratio errors, we can obtain a very narrow bandpass response with a minimum effective relative bandwidth of about 0.036%. This means a bandpass response with a maximum passband bandwidth of 7Hz at midband frequency of 20KHz. Therefore, SPFT systems virtually cover all potential bandpass filtering applications in the audio-frequency range.

The optimum architecture for the AAF and AIF in SPFT systems comprises IIR SC circuits for high levels of rejection of the signals whose frequencies are closer to the system midband frequency, in combination with FIR SC lowpass circuits for extending such rejection to the signals at higher frequencies. This allows the use of low selectivity continuous-time filters at the input and at the output of the system. The principle of operation of SPFT systems, and their good performance, were experimentally demonstrated by means of discrete component models.

Besides filtering applications with very narrow relative bandwidths, in which we can program the required Q-enhancement factor of the system, we also demonstrated in practice the operation of SPFT systems as SSB generators and detectors, which correspond to the selection of different input and output frequency bands.

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CHAPTER 6

PRELIMINARY INVESTIGATION OF N-PATH SC FILTER SYSTEM ARCHITECTURES FOR ULTRA NARROW BANDPASS RESPONSES

6.1 INTRODUCTION

The SPFT SC systems proposed in the previous Chapter are suitable for a wide range of very narrow bandpass filtering applications with relative bandwidths as low as 0.036%. For bandpass responses with relative bandwidths of less than 0.036%, which, for convenience, we designate as Ultra Narrow Band (UNB), the resulting midband gain error (α<-30dB) due to the sample and hold effect at the output of the conventional SC bandpass filter becomes difficult to compensate for, with acceptable system complexity. This problem is not so serious in N-Path (NP) systems using the SC NP filters that we reviewed in Section 1.6, which possess an inherently lower sample and hold effect than conventional SC bandpass filters. However, as we saw there, the conventional SC NP filters using lowpass and highpass path filters suffer from the problem of generation of unwanted frequency-translated components which are in the passband, and, therefore, in contrast to the situation in SPFT systems, can not be attenuated by suitable design of the AAF (Anti-Aliasing Filter) and AIF (Anti-Imaging Filter). This Chapter is concerned with a preliminary investigation of a new type of NP SC filter system using bandpass, rather than lowpass and highpass, path filters, which are regarded as an extension of SPFT systems, but which have the advantage of the lower sample and hold attenuation of conventional NP systems. We shall discuss the application of these systems for the realisation of UNB bandpass responses.

In order to understand the operating principles of NP SC filter systems using bandpass path filters, we shall review first, in Section 6.2, the spectral characteristics of SC NP filters, using the common background introduced in Chapter 2 to describe the alias and image frequency-translated responses of SC filters. In Section 6.3, we explain the two basic methods of providing rejection of the alias and image frequency components in such systems, namely, by outphasing in the SC NP filter and by attenuation by means of the AAF and AIF. The combination of these two methods for eliminating the alias and image frequency components has important implications concerning the system architecture, mainly with respect to the characteristics of the AAF and of the AIF, some of which are explored in a preliminary way in Section 6.4. Section 6.5 summarises the Chapter.

6.2 SPECTRAL CHARACTERISTICS OF SC NP FILTERS

As we saw in Section 1.6, an SC NP filter is formed by N identical SC path filters with switching frequency F_s, which are sequentially connected between the input and output terminals during a fraction $1/NF_s$ of the switching period $1/F_s$, as shown in the model for N=3 in Fig.6.1. Each SC path filter possesses the alias and image frequency-translated responses symbolically illustrated in Fig.6.2, where the sample and hold function $(1/N)(\sin(\pi f/NF_s)/(\pi f/NF_s))$ reflects the reduced hold time interval $1/NF_s$ of the output signal.

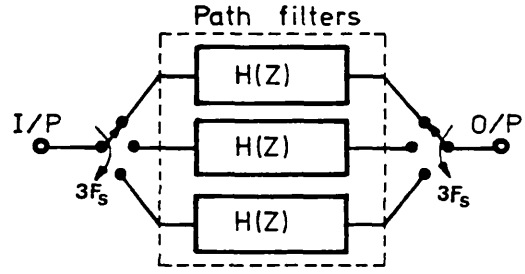

Fig.6.1: SC N-path filter model (N=3)

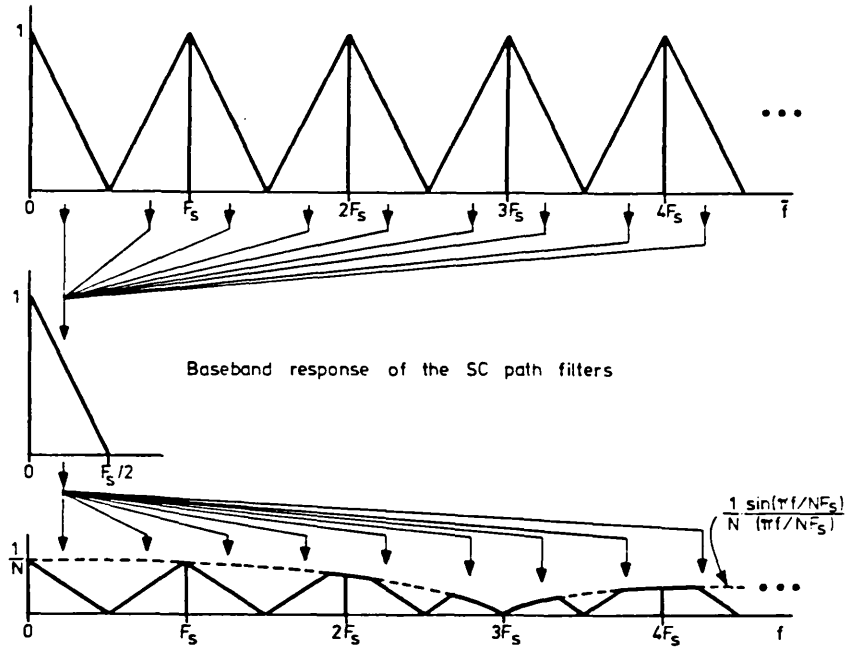

Fig.6.2: Symbolical representation of the alias and image frequency-translated responses of an SC path filter with switching frequency F_s and hold time interval $1/NF_s$

In order to obtain, for example, the overall alias response of the SC 3-path filter we consider N=3 aliasing measurements. In the first one of these measurements, we employ the alias sweeping mode given in Fig.6.3-a corresponding to the detection of output discrete-time frequency components f_1 in the frequency band from DC to

$F_s/2$. From the NP filtering theory [6.1],[6.2], it can be shown that the relative phasing of the discrete-time frequency components f_1 produced by the SC path filters are as represented schematically in Fig.6.3-b. When the input continuous-time frequency components $\tilde{f}$ are such that $\tilde{f}=3lF_s\pm f_1$ $(l=0,1,2,...)$, the resulting output discrete-time frequency components f_1 of the SC path filters are in phase, and, therefore, are summed together at the output of the SC 3-path filter. On the contrary, the input continuous-time frequency components such that $\tilde{f}\neq 3lF_s\pm f_1$ give rise to outphased discrete-time frequency components f_1 of the SC path filters, which form a polygon with zero resultant, and are therefore cancelled at the output of the SC 3-path filter. In this way, we obtain the amplitude response of the SC 3-path filter from DC to $F_s/2$ $(l=0)$, and the corresponding alias frequency-translated responses above $3F_s/2$ $(l\geq 1)$, as shown in Fig.6.3-c. The second aliasing measurement, illustrated in Fig.6.4, corresponds to the detection of output discrete-time frequency components f_2 in the frequency band from $F_s/2$ to F_s. The input continuous-time frequency components such that $\tilde{f}=3lF_s\pm f_2$ $(l=0,1,2,...)$ produce the amplitude response of the 3-path SC filter from $F_s/2$ to F_s $(l=0)$ and the corresponding alias frequency-translated responses above $3F_s/2$ $(l\geq 1)$, whereas the remaining input continuous-time frequency components give rise to unwanted discrete-time frequency components which are ideally eliminated by outphasing. Similarly, we obtain the responses illustrated in Fig.6.5 for the detection of the output discrete-time

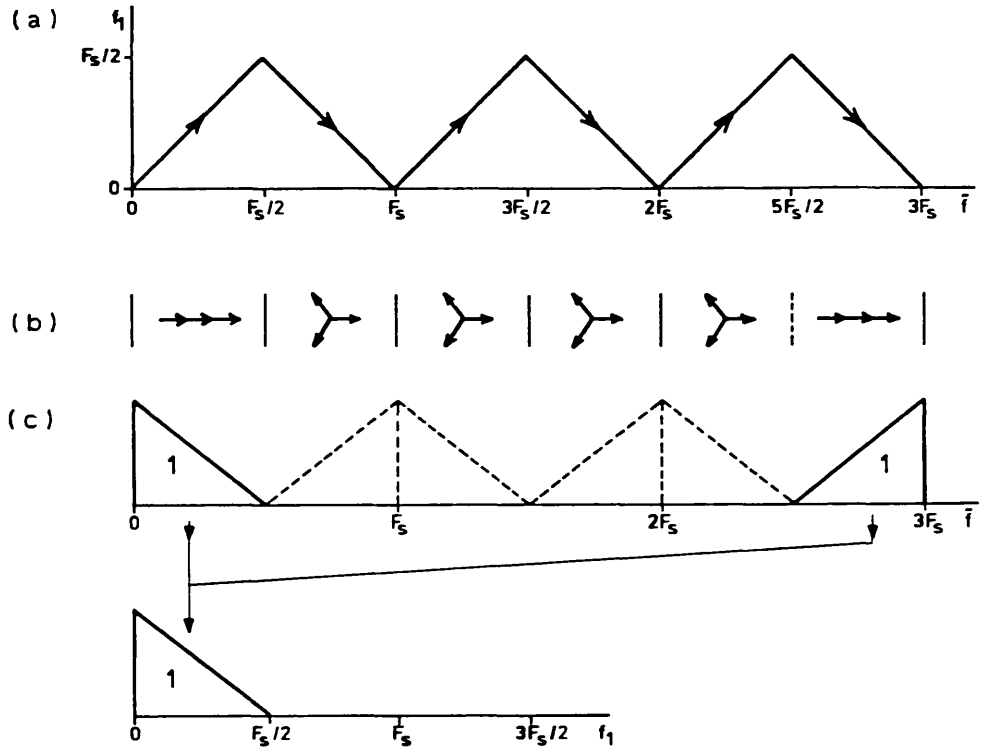

Fig.6.3: Alias response of the SC 3-path filter in the frequency band from DC to $F_s/2$. (a) Alias sweeping mode; (b) Relative phasing of the output discrete-time frequency components of the SC path filters; (c) Alias response

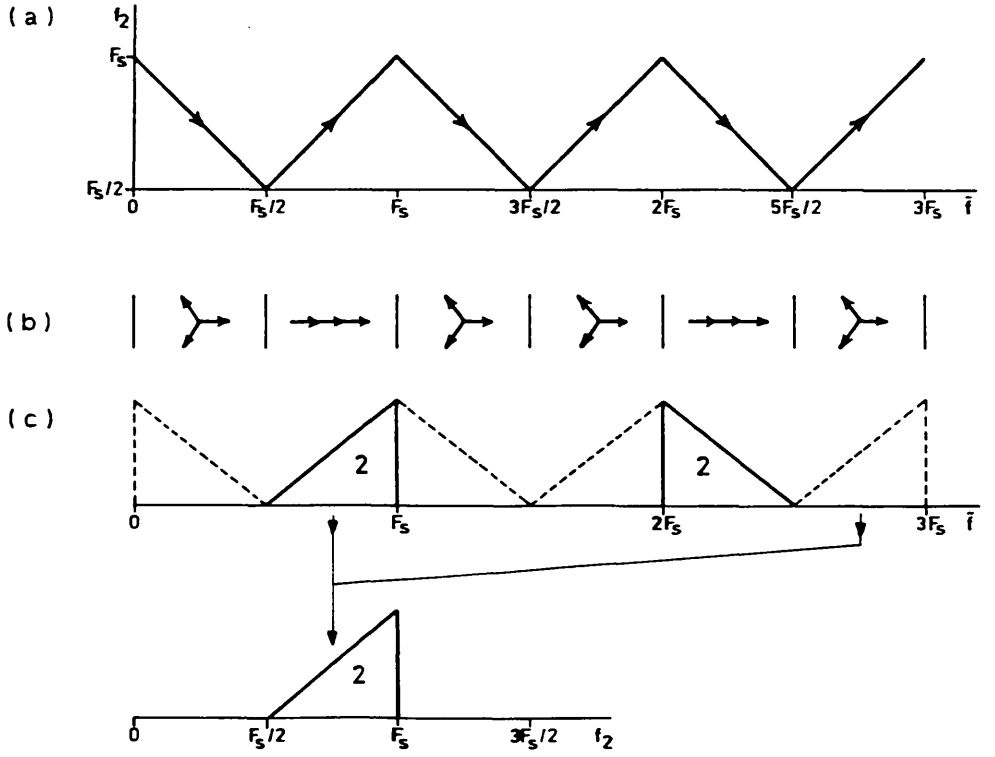

Fig.6.4: Alias response of the SC 3-path filter in the frequency band from $F_s/2$ to F_s

frequency components f_3 in the frequency band from F_s to $3F_s/2$. By combining Fig.6.3, Fig.6.4 and Fig.6.5, we can represent symbolically the overall alias response of the SC 3-path filter as illustrated in Fig.6.6, showing the multiband baseband response below the Nyquist frequency $3F_s/2$ and the corresponding frequency-translated multiband responses above $3F_s/2$.

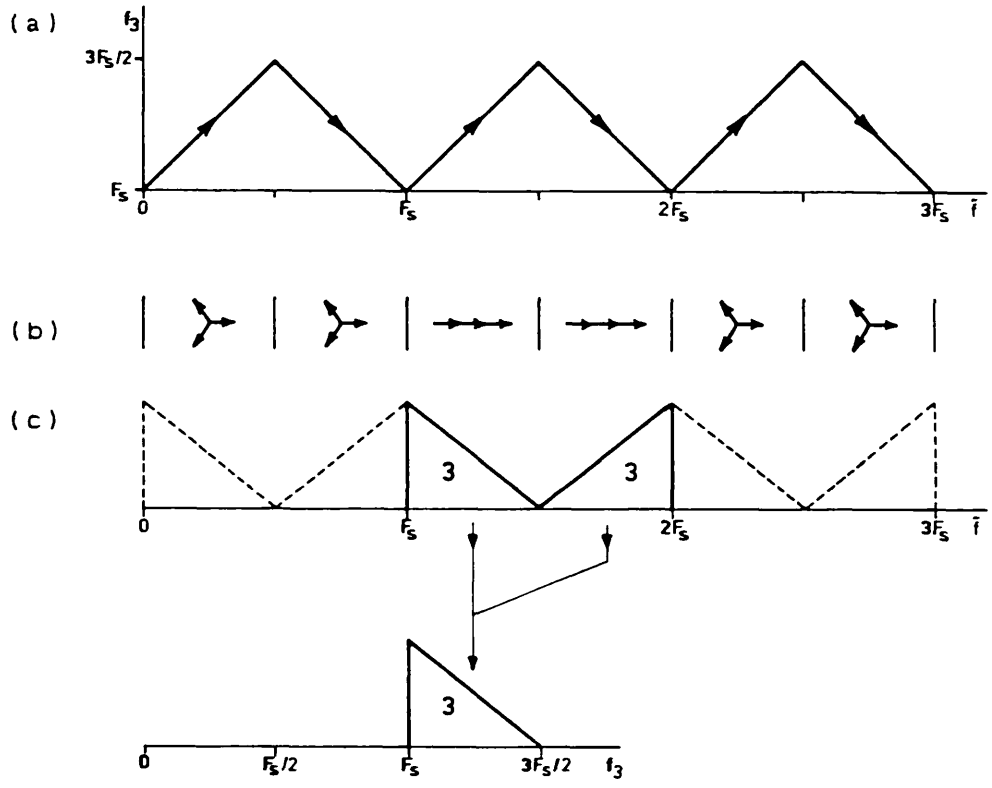

Fig.6.5: Alias response of the SC 3-path SC filter in the frequency band from F_s to $3F_s/2$

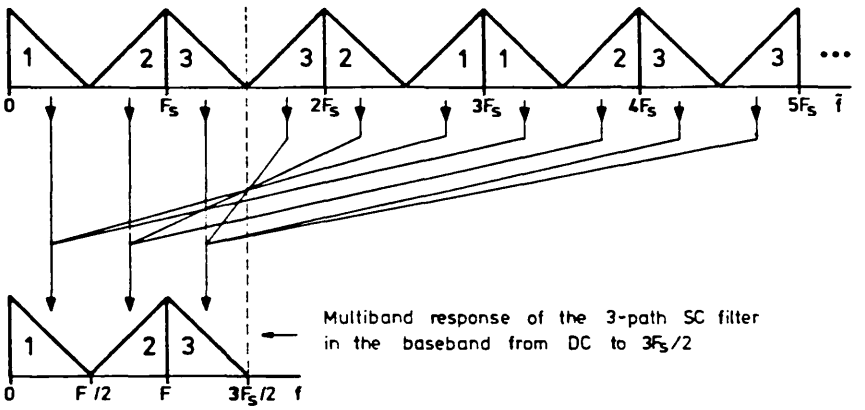

Fig.6.6: Overall alias response of the SC 3-path filter

The image response of the SC 3-path filter is obtained by interchanging the sweeping modes of the detector and of the signal generator. In this manner, we relate the input continuous-time frequency components $\tilde{f}_1$, $\tilde{f}_2$ and $\tilde{f}_3$ in the frequency bands from DC to $F_s/2$, from $F_s/2$ to F_s and from F_s to $3F_s/2$, respectively, to the output discrete-time frequency components f in the baseband below $3F_s/2$ and the corresponding image frequency-translated components above $3F_s/2$, as represented in Fig.6.7.

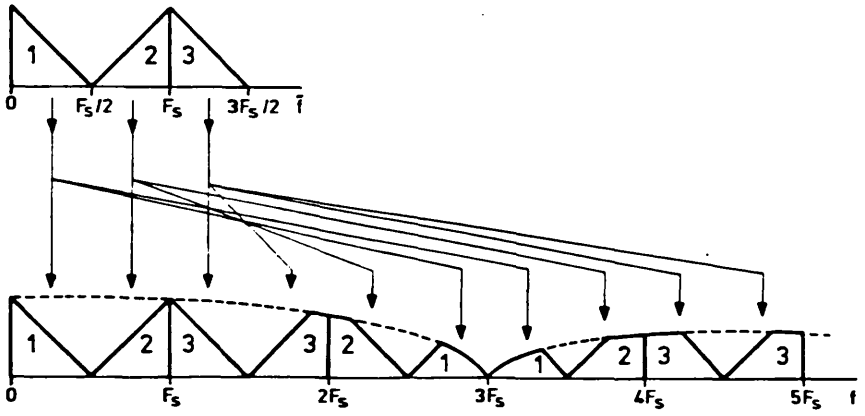

Fig.6.7: Overall image response of the SC 3-path filter

6.3 PRINCIPLES OF OPERATION OF NP SC FILTER SYSTEMS USING BANDPASS PATH FILTERS

6.3.1 General principle

In the conventional SC NP filters reviewed in Section 1.6, using lowpass and highpass path filters, the desired bandpass response is formed by the joining of two frequency-translated bands around F_s (or multiples of F_s) and around $F_s/2$ (or odd multiples of $F_s/2$), respectively. Because of the problem of path mismatch, and, consequently, incomplete cancellation of unwanted frequency-translated components, this manner of producing the desired bandpass response is subject to the effect of mirror frequency components arising in the passband. As we illustrated in Fig.1.18, and Fig.1.20, this consists of signals in one half of the passband generating unwanted frequency-translated signals in the other half of the passband, which, therefore, can not be attenuated by an AAF and an AIF.

NP filters using bandpass path filters were proposed in the context of time-varying active-RC networks in order to overcome the undesirable effect of inband mirror frequency components [6.3]-[6.5]. In the case of bandpass path filters, the bandpass response is formed by only one frequency-translated band, rather than the joining of two frequency-translated bands as before. Therefore, the resulting inband unwanted frequency-translated components which are generated due to imperfect cancellation in the N-path network are produced by frequency components which

lie outside the passband. In the context of an NP SC filter system, to which this principle has not been applied before, such unwanted frequency-translated components can be attenuated by the AAF and by the AIF in a similar manner as in the case of the SPFT systems described in the previous Chapter. This is explained below.

6.3.2 Single-path operation: rejection of alias and image frequency components provided by outphasing and by attenuation

The system given in Fig.6.8 comprises an SC 3-path filter using bandpass path filters, each with midband frequency f_1, Q-factor Q_1 and switching frequency $F_s=mf_1$.

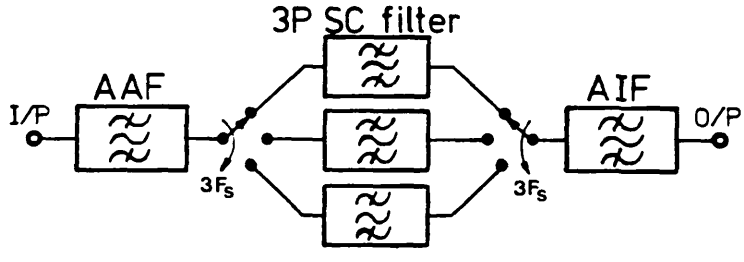

Fig.6.8: Architecture of an NP SC bandpass filter system using an SC NP filter with bandpass path filters

The corresponding multiband response of the SC 3-path filter below the Nyquist frequency $3F_s/2$, illustrated in Fig.6.9, consists of N=3 separated bandpass responses with midband frequencies at f_1, F_s-f_1, and F_s+f_1. In order to explain the requirements for rejection of the alias and image frequency components for single-path operation of this system, i.e. to obtain one single bandpass response,

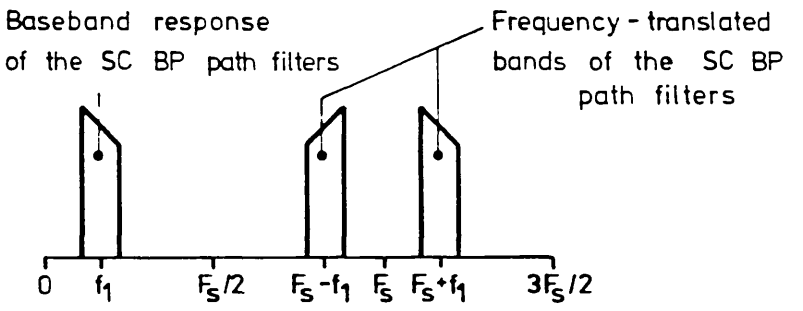

Fig.6.9: Multiband response of an SC NP filter with N=3 bandpass path filters

we shall consider an example corresponding to the selection of the bandpass response with midband frequency $f_o=F_s+f_1$. Firstly, let us consider the elimination of the unwanted alias frequency bands at the input of the SC 3-path filter, using the example illustrated in Fig.6.10. The input continuous-time frequency bands that relate to the desired passband are symbolically represented as in Fig.6.10-a. From the spectral characteristics explained before, the unwanted frequency bands centred at f_1 and F_s-f_1, and, also, at $lF_s\pm f_1$ and $lF_s\pm(F_s-f_1)$ $(l=1,2,...)$, are ideally eliminated by the mechanism of cancellation in the SC 3-path filter itself, leaving the remaining unwanted frequency bands in Fig.6.10-b, i.e. centred at $lF_s\pm f_o$, to be attenuated by the AAF. In practice, however, the AAF should be designed to give also some attenuation at the other frequency bands, on account of incomplete cancellation provided by the SC 3-path filter due to path mismatch. This is schematically represented as in Fig.6.10-c.

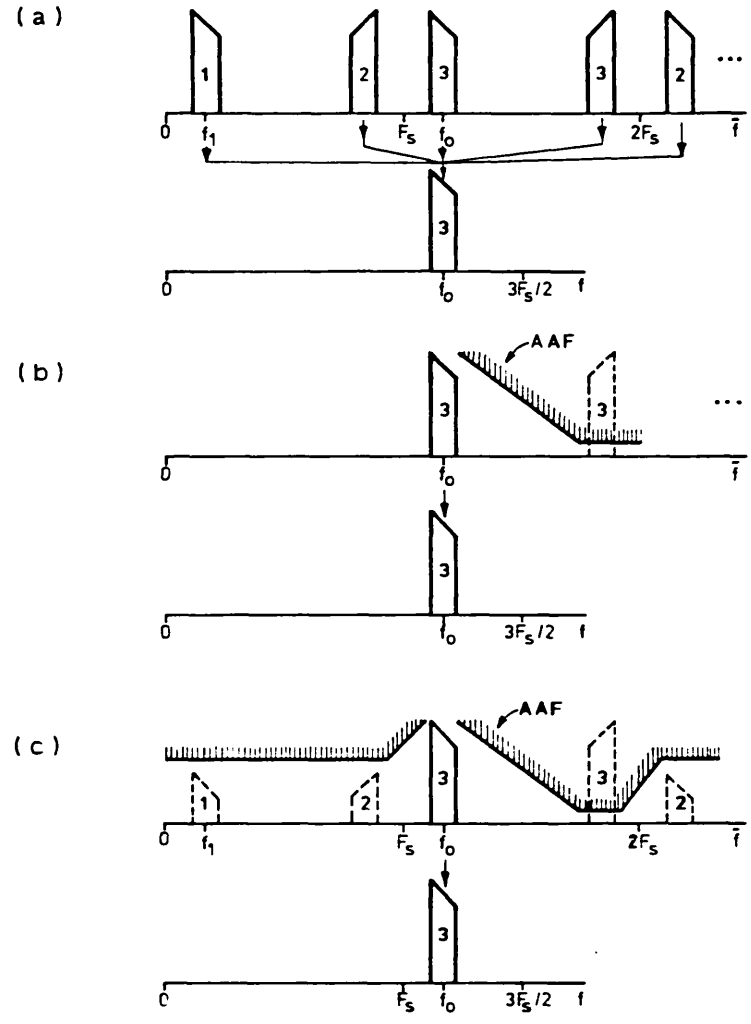

Fig.6.10: (a) Input frequency bands relating to the desired passband; (b) AAF with ideal cancellation of alias frequency-translated components corresponding to frequency bands 1 and 2; (c) AAF with residual alias frequency-translated components in frequency bands 1 and 2 resulting from path mismatch

The selection of the desired output frequency-translated image at f_o is obtained, as illustrated in Fig.6.11, by means of the AIF, which, from the point of view of the spectral characteristics of the SC 3-path filter, has two functions. Firstly, it has to reject the unwanted frequency-translated images above $3F_s/2$ relating to f_o. Secondly, because of the requirement for single-

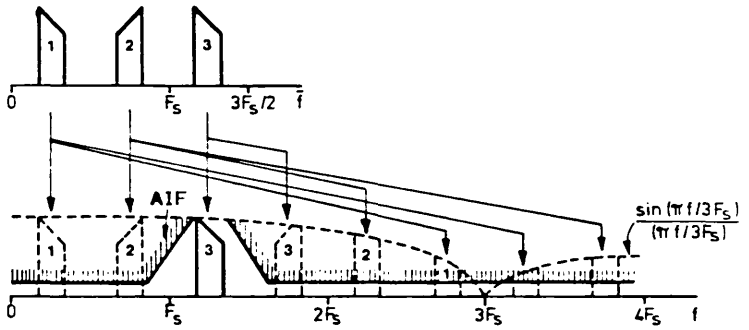

Fig.6.11: Characteristic of the AIF to shape the frequency-translated multiband image response of the SC NP filter with N=3 bandpass path filters

path operation, it has to reject also the other N-1 bandpass responses below $3F_s/2$, as well as the corresponding repetitions above $3F_s/2$. The shape of this AIF is, therefore, similar to that in an SPFT system, but it requires lower selectivity because of the reduced sample and hold effect.

An alternative possible solution for the design of the AAF and AIF consists of increasing the attenuation provided by the AAF at the frequencies which are partly eliminated by cancellation, as a means of reducing accordingly the attenuation required for the AIF at those frequencies. For the sake of simplicity, this solution will not be considered here. Rather, in the following Section, we shall explore possible architectures for the type of SC NP filter system given in Fig.6.8, in which the AAF and AIF are designed as we explained in Fig.6.10 and Fig.6.11, respectively.

6.4 EXAMINATION OF POSSIBLE SYSTEM REQUIREMENTS

6.4.1 Baseband operating mode

In the system given in Fig.6.8, with N arbitrary, the purpose of the bandpass AAF and AIF is to select a desired bandpass response at some specified midband frequency $f_o=nF_s\pm f_1$, which, as in the case of an SPFT system, corresponds to a Q-enhancement factor $K=n.m\pm 1$ ($m=F_s/f_1$ is the sampling ratio of the SC bandpass path filters). The resulting midband gain error of the selected bandpass response, relating to the sampling rate NF_s of the SC NP filter, is given by $\alpha(dB)=-20\log\left|(\pi K/mN)/\sin(\pi K/mN)\right|$. Therefore, the selectivity requirements for the AAF and for the AIF in this type of system depend not only on the parameters m and n, which determine the architecture and complexity of SPFT systems, but also on the number of paths N of the SC NP filter. Next, we shall examine some of the trade-offs involved in the design of this type of system.

Anti-imaging filter: The selectivity of the AIF is determined by the characteristics of the multiband response of the SC NP filter, which depend on the sampling ratio of the SC bandpass path filters in a similar way as in SPFT systems. As we saw in Section 5.4, a sampling ratio m=4 produces uniformly spaced bandpass responses, in which case the AIF may have symmetrical transition bands. In this application of an NP system, the additional benefits of minimum capacitance spread and minimum capacitor area of the SC bandpass path filters with m=4 are even more important than in the case of SPFT systems, owing to the

inherently larger capacitor area required for the SC NP filter. For m=4, the midband gain error of the selected bandpass response is $\alpha(dB)=-20\log\left|(\pi K/4N)/\sin(\pi K/4N)\right|$, from which we can determine the required gain of the AIF, for given K, and N.

Anti-aliasing filter: As we saw before, the anti-aliasing specifications in this type of NP system are provided in two ways, namely by cancellation in the SC NP filter itself, and by attenuation in the AAF. The following discussion will show how the combination of these methods of providing rejection of the alias frequency components, on the one hand, together with the system parameters n and N, determines the overall selectivity of the AAF. For a system midband frequency at $f_o=Kf_1$, the corresponding alias frequency-translated bands above $NF_s/2$ are centred at $NlF_s\pm f_o$ (l=1,2,...), the first one of which at NF_s-f_o (l=1) implies an upper transition band of the AAF given by NF_s-2f_o, i.e. $(N.m-2K)f_1$. At the remaining unwanted frequency bands, which are partly eliminated by cancellation in the SC NP filter, the AAF is required to have much less attenuation. Therefore, for the optimum sampling ratio m=4, the selectivity of the AAF is primarily determined by the multiple n of the switching frequency F_s giving the desired bandpass response as well as by the number of paths N, as illustrated in the example of Fig.6.12 with N=4. For the system midband frequency at $f_o=F_s-f_1$ shown in Fig.6.12-a, with Q-enhancement factor K=3, the AAF can have a wide upper transition band of $4F_s-2f_o=10f_1$. On the other hand, for the system midband

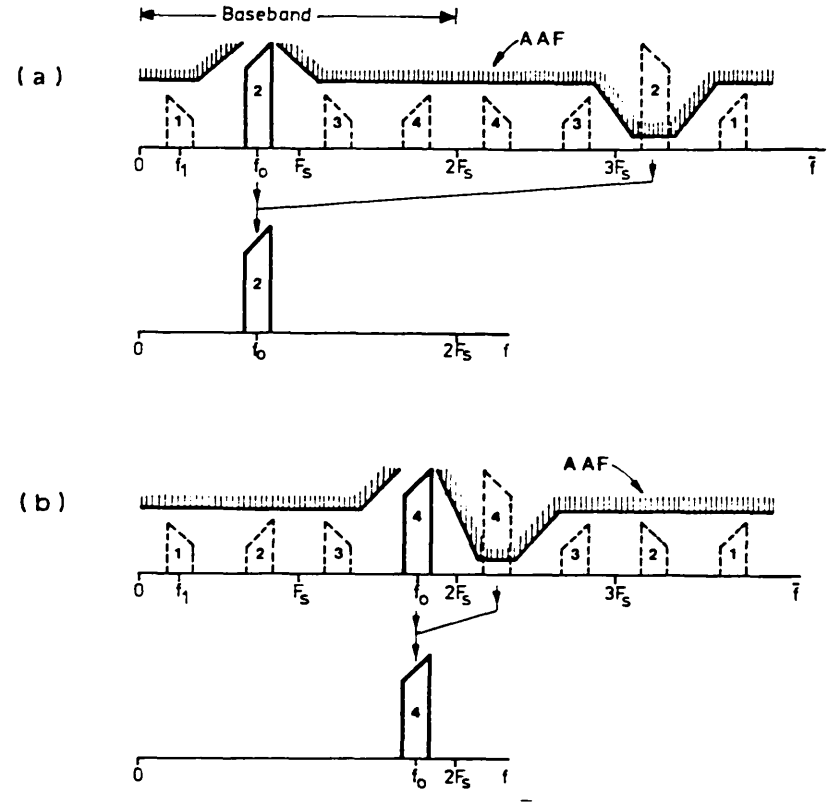

Fig.6.12: Selectivity of the AAF for baseband operation, as a function of the multiple n of the switching frequency and of the number of paths N

frequency at $f_o=2F_s-f_1$, with a larger Q-enhancement factor K=7, the AAF is required to have a much narrower transition band of only $2f_1$, as shown in Fig.6.12-b.

6.4.2 Frequency-translated filtering mode

As we mentioned previously, NP SC bandpass filter systems with bandpass path filters are envisaged, primarily, for UNB filtering applications requiring very large Q-enhancement factors, typically K>28, which can not be achieved employing SPFT systems with realistic complexity. For such Q-enhancement factors, assuming the optimum sampling ratio m=4, the NP system is required to operate above the multiple n=7 of the switching frequency.

For the operation in the conventional baseband filtering mode below $NF_s/2$, as in the previous examples, the SC NP filter in the system is required to have a minimum number of paths N=15. Such a combination of system parameters guarantees a small sample and hold attenuation, at the expense of greatly increased complexity of the SC NP filter with large number of paths, and, above all, a very large amount of silicon area required for implementation. Alternatively, we can operate the NP system in a frequency-translated mode whereby the desired bandpass response is above the Nyquist frequency $NF_s/2$, as in the case of SPFT systems. For such operation of an NP system, the key parameters n, m and N imply other constraints on the AAF and AIF, as we show next.

One parameter that determines the selectivity of the AIF is, as before, the sampling ratio m of the SC bandpass path filters. The previous considerations also apply to the operation of the NP system in a frequency-translated mode, and hence we should choose the optimum sampling ratio m=4 in order to have symmetrical transition bands of the AIF. In this operating mode, the midband gain error due to the sample and hold attenuation becomes an additional important aspect to consider. This error is not only a function of the multiple n giving the desired frequency-translated band, as in SPFT systems, but it is also a function of the number of paths N. This is shown in Fig.6.13, for an example with the optimum sampling ratio m=4. As we can see, there is an important trade-off between the midband gain

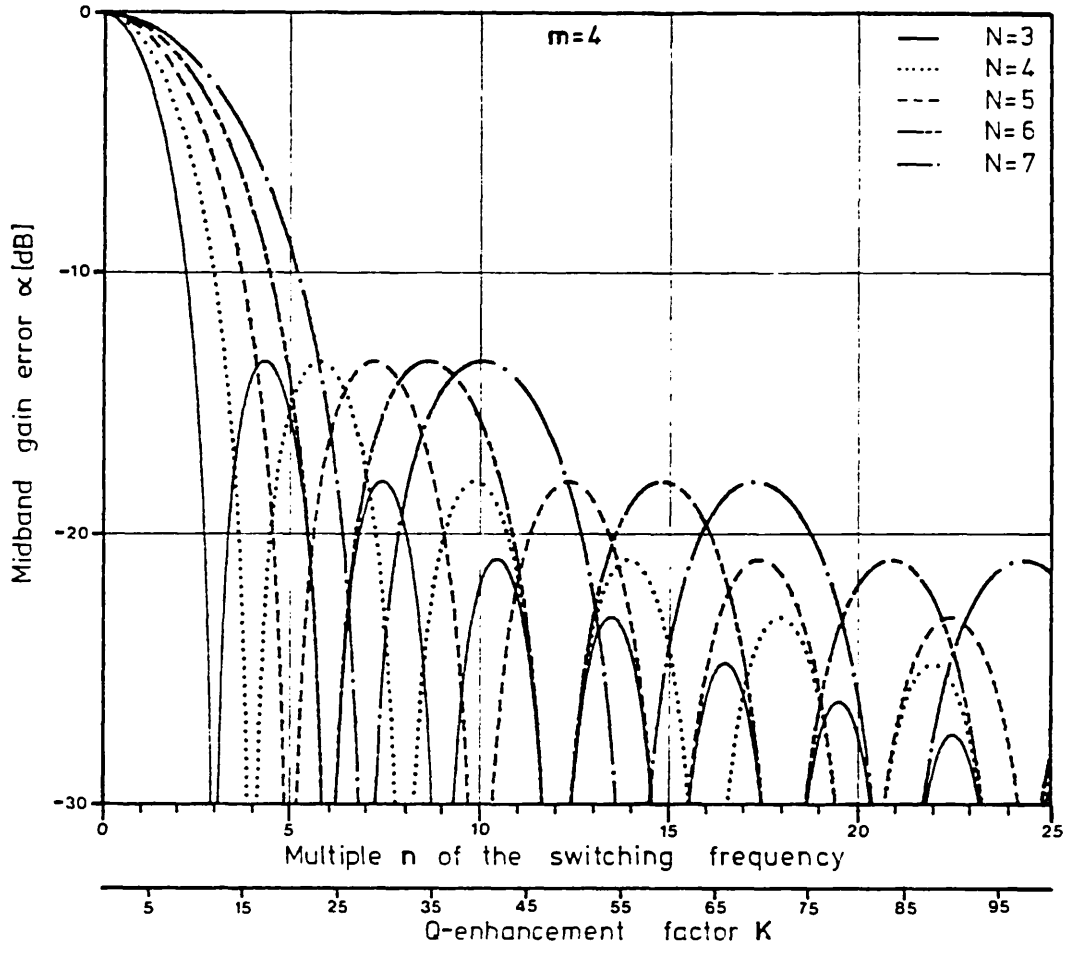

Fig.6.13: Midband gain error of the desired frequency-translated image as a function of the system parameters n and N

error α, and thus the selectivity of the AIF, and the number of paths N, which determines the complexity and total capacitor area of the NP SC filter in the system. If we consider, for example, the realisation of an NP system with a Q-enhancement factor K=29, corresponding to the selection of the upper frequency-translated band for n=7, the adoption of N=3 produces a lower midband gain error than in the case of having N=4, or N=7. Designing the SC NP filter with N=5, or N=6 paths, gives an even lower midband gain error, which, however, may not be significant enough

(a reduction of only a few dB) in order to justify the increased complexity, and increased capacitor area. The adoption of a specific value of N for the design of the SC NP filter will depend also on the characteristics of the AAF, as for the case of an NP system operating in a baseband frequency mode explained before. An example is illustrated below.

Let us consider the realisation of an NP system with a Q-enhancement factor K=55 corresponding to the selection of the lower frequency-translated band for n=14. We can see in Fig.6.13 that the solutions with N=4, N=5 and N=6 paths, all yield approximately the same midband gain error, i.e. α=-20.8dB, α=-21.8dB and α=-19.1dB, respectively, and hence a similar complexity of the AIF. However, the characteristics of the AAF can be rather different bearing in mind the fact that some of the unwanted frequency-translated bands are partly attenuated by outphasing of the SC NP filter. This is illustrated in Fig.6.14. If we choose N=4, as in Fig.6.14-a, the AAF is required to have a narrow upper transition band of only $2f_1$, and a much wider lower transition band of $14f_1$. For N=5, we obtain an AAF with symmetrical transition bands with bandwidth $10f_1$, as shown in Fig.6.14-b. Finally, for the solution with N=6, illustrated in Fig.6.14-c, we obtain a lower transition band with bandwidth $14f_1$, and also a wide upper transition band with bandwidth $10f_1$.

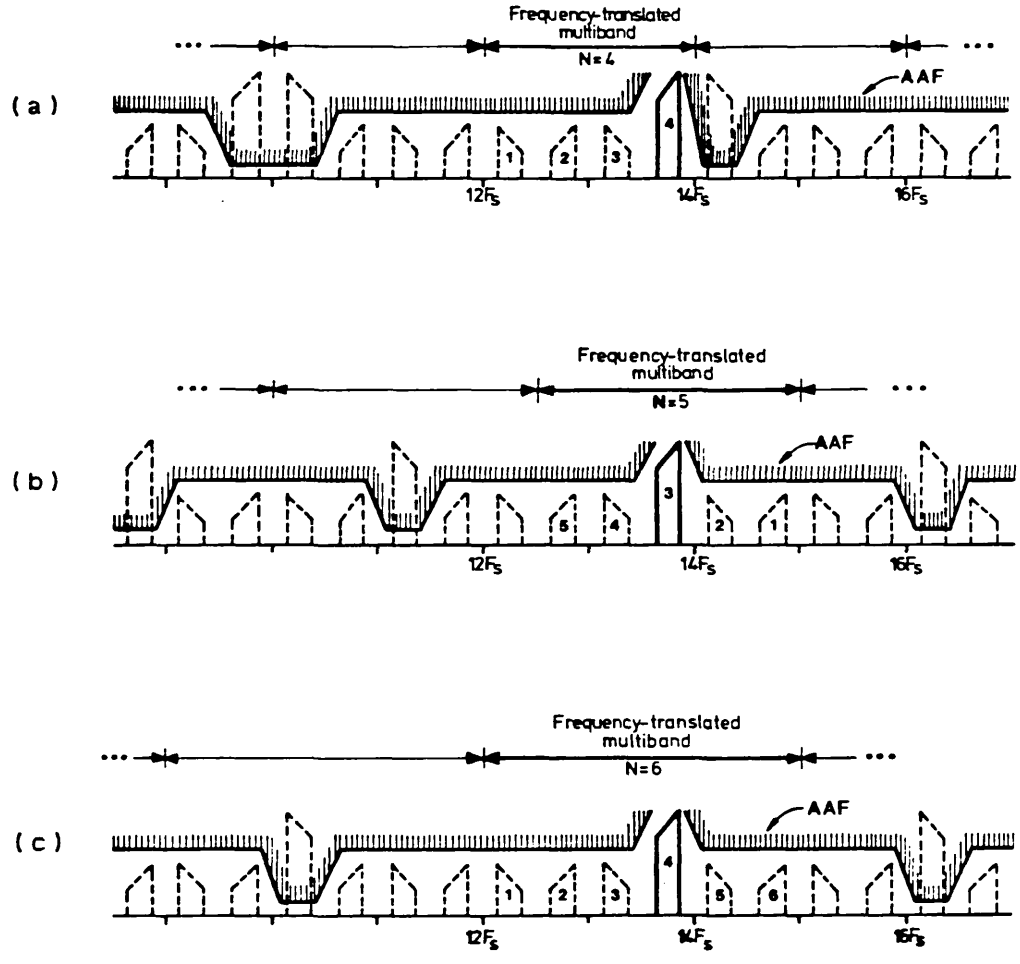

Fig.6.14: Selectivity of the AAF for frequency-translated operation, as a function of the number of paths (a) N=4; (b) N=5; (c) N=6

6.5 SUMMARY

In this Chapter we presented a preliminary investigation of new types of NP SC filter systems, whose operating principles combine the ideas of (i) NP filters with bandpass path filters, (ii) conventional SC NP filters, and (iii) SPFT systems. The general architecture of these systems is obtained by a simple modification to the architecture of SPFT systems, which consists of replacing the conventional SC bandpass filter by an SC NP filter using bandpass path filters. In SC NP filters with bandpass path filters, the desired bandpass response is formed by only one frequency-translated band of the path filters, rather than the joining of two frequency-translated bands, as in conventional SC NP filters using lowpass and highpass path filters. This provides a means to overcome the problem of inband generation of unwanted frequency-translated components, which, in contrast to the situation in conventional NP systems, can now be attenuated by design of appropriate AAF and AIF, as in SPFT systems. On the other hand, the problem of sample and hold attenuation that exists in SPFT systems, is here much less important, as is in conventional SC NP filters. This reduces the selectivity requirements for the AIF, and, hence, renders this type of systems attractive for implementation of ultra narrow bandpass responses, which can not be achieved using SPFT systems with acceptable complexity.

The specified rejection of the alias and image frequency components in NP SC systems using bandpass path filters are obtained, partly by cancellation of outphased frequency-translated components in the SC NP filter, and, partly by attenuation in the AAF and AIF. The combination of these two methods of obtaining the anti-aliasing and anti-imaging requirements in the system, together with the selection of the number of paths N of the SC NP filter, the sampling ratio m of the SC bandpass path filters, and of the multiple n of the switching frequency giving the desired frequency-translated bandpass response, determines the overall characteristics, and complexity, of such systems. The selection of these system parameters depends, in turn, on whether the system operates in a conventional baseband frequency mode below the Nyquist frequency $NF_s/2$, or, alternatively, in a frequency-translated mode above the Nyquist frequency $NF_s/2$. Overall, these aspects lead to a variety of solutions for the design of such systems, trading-off the complexity of the SC NP filter, on the one hand, with the selectivity of the AAF, and of the AIF, on the other hand. These solutions, some of which we explored in a preliminary way, have to be examined in a case-by-case basis, in order to design with the optimum system parameters N, m and n for reduced complexity of the SC NP filter, as well as of the AAF and AIF. Further research is needed in order to investigate alternative solutions for designing such systems, and, also, to explore more fully their potentialities, such as for the realisation of filter systems with multiband responses, i.e. filter banks.

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CHAPTER 7

CONCLUSIONS AND SUGGESTIONS FOR POSSIBLE FURTHER WORK

7.1 Discussion of Results

The objective of this work was to study design techniques for narrow and very narrow bandpass filtering applications realisable using state-of-the-art MOS technology. It was not possible to assess the SC circuits, and systems, developed in this thesis by implementing them in integrated circuit form, which would have been of considerable interest. Instead, they were assessed using practical discrete component models, which amply confirmed the feasibility of the approaches. The proposal of SC systems with frequency-translated operating modes -a view of the implications of the discrete-time nature of SC filters, which is radically different from the view considered hitherto- played a crucial role in the development of high-quality SC bandpass filter systems with very narrow relative bandwidths of less than 1%, which, so far, had not been achieved in SC form. These systems are the subject of a Patent Application which has been filed by the Ministry of Defence [J.E.FRANCA, "Switched-Capacitor Circuits", British Patent Application No.8411547, 4th.May 1984]. An augmented new British Patent Application No.8511218 was filed on the 2nd. May 1985, claiming priority from the above mentioned patent

application. The results of the work will now be summarised below.

After a general introduction in Chapter 1, we presented a discussion, in Chapter 2, of the fundamental operating principles of SC systems, based on a careful examination of the spectral characteristics of SC filters. The operating mode of an SC filter system is determined by the combination of an Anti-Aliasing Filter (AAF), before the SC filter, and of an Anti-Imaging Filter (AIF), after the SC filter, which have to be designed to satisfy the bandlimiting constraints imposed on such spectral characteristics in order to avoid the effects of aliasing distortion and imaging, respectively. Typically, conventional SC bandpass filter systems operating below the Nyquist frequency $F_s/2$ -baseband filtering- employ lowpass AAF and AIF to reject the unwanted frequency-translated signal components above $F_s/2$. On the contrary, the proposed frequency-translated systems employ bandpass AAF and AIF for selecting a specified frequency-translated band above $F_s/2$, and, consequently, rejecting the remaining unwanted frequency-translated bands, including the baseband below $F_s/2$. In order to be realised in a form suitable for integrated circuit fabrication, the AAF and AIF comprise low selectivity continuous-time filters, together with sophisticated SC decimators and SC interpolators, respectively. SC decimators and interpolators are regarded as specialised SC filters, operating at different sampling rates, whose frequency responses are tailored in order to

eliminate the unwanted alias and image signals that are not adequately attenuated by the continuous-time filters. For SC decimators and interpolators with FIR transfer functions, which are particularly suitable for narrow band SC filter system applications, we employed a simple optimisation technique in order to obtain an exact placement of the notch frequencies for maximum rejection of the unwanted alias and image signals in the system.

Chapter 3 and Chapter 4, were both concerned with the development of SC circuits needed for implementation of the new SC filter systems. In Chapter 3, we developed general SC biquad building blocks employed in various parts of the systems. For decimation and interpolation applications, we utilised cascade SC biquad structures with moderate sensitivity of the frequency response to capacitance ratio errors. For the more critical application of the high-quality SC bandpass filter at the heart of the system, we employed, instead, coupled-SC biquad structures with low sensitivty of the frequency response to capacitance ratio errors. The problem of large capacitance ratios in SC biquads with high Q-factors, which arise in the high-selectivity filtering applications considered in this thesis, was analysed in detail. Based on this analysis, we introduced the concept of optimum switching frequency which leads to the design of SC biquads with absolute minimum capacitance spread. This minimises capacitance ratio errors and reduces the total capacitor area, thus increasing the yield and hence reducing the cost of

manufacture.

In Chapter 4, we developed SC decimator and interpolator circuits suitable for applications with optimum multinotch stopband approximations. The first solution considered was based on SC biquad realisations of FIR quadratic transfer functions. Experimentally, we showed that this type of FIR SC circuit was rather sensitive to the imperfections of the amplifiers, which impaired the accuracy of the amplitude responses, particularly at high frequency. This was attributed to the recursive nature of the SC circuits. An alternative solution was then pursued, consisting of the development of non-recursive polyphase structures for SC decimators and interpolators, typically used in digital signal processing. The resulting SC circuits were shown to be very attractive from the points of view of low capacitance ratios, reduced number of amplifiers, and high operating speed, at the expense of a requirement for more switching phases than the SC biquad implementations. The efficient design techniques developed for these circuits produced very accurate multinotch amplitude responses, even at high frequency, in spite of their inherent high sensitivity to capacitance ratio and timing errors. In our mind, this new family of SC circuits represents a successful result of the use of SC techniques in order to implement basic concepts of digital signal processing, where previous attempts have suffered from serious practical limitations (see Section 1.5 and Reference [1.48]). Another interesting type of SC

decimator and interpolator circuit developed in this Chapter was based on a combination of SC biquad and SC polyphase structures, as a means of obtaining the desired selectivity of the optimum multinotch amplitude responses, using switching schemes with acceptable complexity.

In Chapter 5, we described the design, implementation, and testing, of SC bandpass filter systems with narrow and with very narrow relative bandpass responses, embodying the ideas and circuits presented earlier. For narrow bandpass responses, we designed an SC bandpass filter system (2.4% relative bandwidth, at midband frequency of 20KHz) with baseband operating mode. For the conventional SC bandpass filter in the system, we adopted the criterion of designing with an optimum low value of the switching frequency leading to an absolute minimum capacitance spread. In order to accomodate such a low value of the switching frequency, we designed efficient FIR SC lowpass decimator and interpolator circuits maximising the rejection of the unwanted alias and image signals at low frequency. An experimental system was built in discrete component form, showing good performance with respect to the accuracy of the amplitude response, dynamic range, and, also, anti-aliasing and anti-imaging characteristics.

For the realisation of bandpass responses with relative bandwidths of less than 1%, we considered the solution of an SPFT SC filter system. Firstly, we discussed the general architecture and requirements for such systems, paying special attention to the selectivity of the bandpass AAF

and AIF. The AIF is required to have higher selectivity than the AAF in order to compensate for the sample and hold effect at the output of the SC filter, which produces an undesirable attenuation of the frequency-translated images, especially at high frequency. For the architectures of the SC decimator and SC interpolator in the AAF and AIF, respectively, we proposed a solution employing a combination of FIR SC lowpass polyphase decimators and interpolators, for the rejection of frequency-translated signals at high frequency, together with IIR SC bandpass biquad decimators and interpolators for the rejection of frequency-translated signals whose frequencies are closest to the desired bandpass response of the system. The practical realisation of a high-quality SPFT SC bandpass filter system, was demonstrated for an example corresponding to a very narrow relative bandwidth of 0.48%, also at midband frequency of 20KHz, employing an SC bandpass filter, with 2.4% relative bandwidth at midband frequency of 4KHz, and switching frequency of 16KHz. Experimental results confirmed the operating principle of the system. They also showed good accuracy of the amplitude response, as well as good anti-aliasing and anti-imaging performance, as expected from the design of the decimator and interpolator in the system. An important result of this experimental work showed that the dynamic range of the conventional SC bandpass filter was preserved in the system, despite the significant reduction of the relative bandwidth. Hence, SPFT SC bandpass filter systems also offer a solution for very narrow bandpass filtering

applications requiring high dynamic range.

In addition to very narrow bandpass filtering, we demonstrated further applications of SPFT SC systems, including their operation as single sideband generators and detectors, corresponding to the selection of different frequency-translated bands at the input and at the output of the system.

The idea presented in Chapter 6, consisted, basically, of embedding an NP filter with bandpass path filters, proposed in the context of active-RC filters, in the typical architecture of an SPFT system, with bandpass AAF and AIF. In this manner, SC NP filter systems with bandpass path filters overcome the problem of mirror frequency components of conventional SC NP systems, where two adjacent frequency-translated bands, rather than only one as in SPFT systems, are needed to form the desired bandpass response. On the other hand, this type of systems also offer a solution to the problem of sample and hold attenuation of SPFT systems, because this is reduced in SC NP filters compared with in conventional SC bandpass filters. This makes these systems particularly attractive for ultra narrow bandpass filtering applications, which are beyond the reach of practical SPFT systems. The architectures for SC NP filter systems with bandpass path filters reflect the combined methods of eliminating unwanted frequency components, namely by outphasing, in the SC NP filter, and by attenuation, in the AAF and AIF. Some possible solutions to meet those requirements were

examined. Many other possible solutions have to be explored in order to fully assess the potential of these systems.

7.2 Suggestions for Possible Further Work

With respect to the design of SC decimator and interpolator circuits, we suggest the following possible aspects for further research:

1. Study of the problems associated with clock feedthrough in non-recursive polyphase SC structures. We envisage two possible directions for research which may be either the development of techniques which eliminate clock feedthrough (e.g. research at the device level, including aspects of switching), or the development of suitable techniques which compensate for the undesirable DC output voltage produced by clock feedthrough. For example, this may be the idea of using an extra input SC branch to sample a DC voltage in order to produce the required amount of charge to cancel out the charge injected by clock feedthrough. In order to implement this idea, which was verified in practice, it is required to provide additional circuitry in order to produce the desired input DC voltage.
2. Increase of operating speed of the SC circuits. This requires further development of fast reset schemes, such as those presented in the Appendix to Chapter 4 [4.21].
3. Development of IIR decimators and interpolators employing single amplifier SC structures with multiphase switching schemes, based on the ideas utilised for the FIR SC polyphase decimator and interpolator circuits. This requires the development of suitable feedback SC branches

for implementing the denominator of the IIR transfer functions, the numerator of such transfer functions being implemented in a similar way as for non-recursive polyphase structures. This new family of IIR SC decimator and interpolator circuits will require more sophisticated switching schemes than the SC biquad implementations employed in this thesis, but, on the other hand, they would be rather attractive from the points of view of reducing the capacitance ratios, and the total number of amplifiers required.

With respect to SC systems for narrow bandpass filtering, we can suggest two possible directions for further research:

4. Firstly, it would be important to study solutions to overcome the problem of sample and hold attenuation in SPFT systems. One possible solution consists of employing a sample-hold-and-return-to-zero format for the output signal of the SC bandpass filter. This has the effect of equalising the level of the image signals produced by the SC filter, which would then require an AIF with similar complexity as the AAF. It is even possible to find an optimum hold time interval in such a way that the resulting notches will attenuate some of the unwanted frequency-translated images. The side effect of such a signal format would be to reduce the overall level of the image response, which, however, implies only an increase of the gain factor, rather than increased selectivity.

5. A further possible SC system architecture for narrow

bandpass filtering consists of employing solely SC decimator and interpolator circuits, i.e. to eliminate the SC bandpass filter in the system, which is a well known filtering technique in digital signal processing [4.2],[4.3]. Besides the improvement of the SC circuits for implementation, along the lines mentioned above, this would require further research concerning the derivation of appropriate transfer functions, both FIR and IIR. It is anticipated that a close approach to the techniques already established for digital signal processing would be extremely advantageous.

Among the potential applications for SPFT systems, it would be of interest to investigate the following:

6. High-frequency filtering applications, in order to explore the operation of the high-quality SC bandpass filter at a much lower frequency. This would be related to the design of high-frequency SC decimator and interpolator circuits, on the one hand, and, on the other hand, to the development of practical solutions to reduce the sample and hold attenuation, such as the one mentioned above. In addition, it is necessary to investigate detailed aspects of SC circuits, particularly of analogue switches, which may limit the accuracy of high-frequency alias frequency-translated responses. Some experimental results in the systems developed in this thesis showed accurate alias responses up to about 2MHz, using commercially available CMOS 4016 analogue switches.

7. In general, applications requiring the translation of

signals between different frequency bands, such as in the area of FDM/TDM and TDM/FDM transmultiplexing, are potentially attractive for implementation using SPFT systems.

SC NP systems using bandpass path filters are still in their infancy. As was clearily illustrated in this thesis, the design of such systems is not an easy task, bearing in mind the many system parameters, and related trade-offs. Further research is required in this area. Additionally, we think that this type of system may be extremely useful for bank filtering applications, i.e. the realisation of a set of bandpass channel filters with identical response shape but different relative bandwidths, such as required in many data transmission systems and speech processing applications. This also requires the development of new system architectures in order to take full advantage of the multiband response of the SC NP filter in the system.