Next Generation Neural Interfaces for low-power multichannel spike sorting

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Aims. Advances in chronic electrode arrays allow stable recordings of action potentials from large numbers of neurons in freely-behaving subjects, opening new possibilities for both neuroscience studies and neural prosthetics applications. However, as channel counts increase, the high bandwidth of data precludes long-term transmission or data-logging by wireless implants. Deinterleaving the signals from multiple neurons (spike sorting) enables massive data reduction and is a critical signal processing bottle-neck in many applications. We are developing low-power, multichannel Next Generation Neural Interfaces (NGNIs) as a platform technology for real-time on-chip spike sorting.

Methods. We use a two-stage approach in which spike templates are first identified off-line with feature extraction and clustering using established software (Wave_Clus), before being uploaded to custom template matching hard-ware implemented by an Igloo FPGA. The template-matching algorithm was designed to provide an optimal balance between power consumption (i.e. complexity) and performance.

Results. Our first generation hardware (NGNI v0; Fig. 1A) provides 32 channels of spike amplification, filtering and sorting (4 templates/channel) with a total power consumption of 34mW. Spike times are streamed via USB to a PC running a custom GUI (Fig. 1B). We have successfully tested the system to obtain real-time spike recordings from monkey cortex (Fig. 1C).

Conclusions. The scalable architecture will in future allow up to 192 channels of spike sorting at less than 0.25mW per channel, and will incorporate an SPI bus for local streaming/storing of data. We anticipate this will provide a key component enabling future high-channel wireless recording systems and implantable closed-loop neuroprostheses.

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