THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR-CERMET CONTACTS

by

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ABSTRACT

Cermet films were deposited by R.F. co-sputtering of a gold and silicon dioxide target. The conduction mechanisms of such films are discussed with the aid of an energy band model, and are treated as with the case of amorphous insulators with high defect density of states due to the metal inclusions. Films deposited onto n-type silicon wafers gave rise to space charge regions at the silicon surfaces. C-V measurements showed that a very large interface state density was present so that the Fermi level was pinned at the cermet/silicon junction. When a dc bias voltage was applied on samples with conductive cermets, the characteristics depended greatly on whether the current was limited by the cermet resistance or the space charge region. At forward and low reverse bias, the I-V and C-V properties approached that of the cermet, but at high reverse bias, the current was limited by the barrier height of the interface and C^{-2} increased linearly with V. With insulating cermets, surface inversion occured to a certain extent so that minority carriers (holes) were accumulated at the interface. These minority carriers have a typical response time of 10^{-4} to 10^{-2} seconds. Under forward bias, more holes were driven to the interface due to the leaky nature of the cermet, whereas at reverse bias, they leaked away through it. The variation of their densities with bias and the MIS-like configuration of the specimens resulted in large dispersions of the differential capacitance and conductance with frequency, bias voltage as well as the metal fraction of the cermet.

Schottky barriers made on evaporated CdSe films were found to be of poor quality and were too irreproducible for any quantitative analysis.

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CHAPTER 1

INTRODUCTION

A cermet film is generally visualised as a random matrix of metal particles embedded in an insulator such as silicon dioxide. This structure has many similar electrical properties as that of the ultra thin discontinuous metal films in which the metal particles are formed on the surface of an insulator. It is easy to accept that qualitatively they exhibit metallic-like conduction when the metal fraction in the cermet is high, and insulator-like conduction when it is low. Thus they show positive temperature coefficient of resistance (TCR) when the metal fraction is greater than about 0.4, and become negative when below this value. Therefore for a given temperature range, there is an optimum value of metal fraction in which these films exhibit very low TCR. This feature may be exploited commercially for manufacturing high quality resistors.

Ever since the structure of discontinuous metal films were observed with the help of electron microscopes, there have been constant attmepts to identify the mechanisms responsible for their electrical properties such as conductivity, capacitance and activation energy. However, despite much efforts, it appears that a completely satisfactory theory has yet to be found. This is not too surprising especailly in the case of cermet films, because their structure may probably be much more complex

microscopically than the simple picture sketched above.

This project was started with the intention of of investigating the effects of the semiconductor space charge region when a cermet is put in contact with it. Such a configuration may have the possibility of being used as a novel vidicon target. Essentially, the idea of such a target is that each of the metal particles in the cermet would form a tiny Schottky barrier when in contact with the semiconductor surface. Since the size of the metal particles is extremely small ($\sim$2 nm) they therefore provide a large matrix of diodes which is far smaller than any diode arrays that can be produced with the conventional technology of semiconductor fabrication. Furthermore since these metal contacts are physically separated from one another by the insulator, their lateral resistivity would be high enough to meet the requirements of a vidicon target. It therefore has the attraction of being easy to produce and probably has much higher resolutions than the conventional vidicon targets.

The semiconductor material used is mainly silicon single crystal wafer. Attempts were also made in which evaporated cadmium selenide films were used. However it was found that their properties were very irreproducible and no quantitative analysis could be carried out.

Chapter 2 is devoted to the theories of the interface and space charge region of semiconductors. It begins by presenting the relevant equations under thermal equilibrium

conditions. Next the theory of the MIS structure is discussed with emphasis on the effects of interface charges. This structure is closely similar to the insulating cermet-semiconductor contacts. The carrier transport mechanisms across the space charge region is then discussed. This is the conventional Schottky barrier theory and applies for the case of conductive (metallic) cermet-semiconductor contacts.

Chapter 3 begins with a brief outline of the electronic processes in amorphous insulators. The published theories of cermet conductions are then surveyed. Electron micrographs of cermets are presented and discussed. Finally, a general discussion is presented in which it is pointed out that insulating cermets exhibit many similar ac properties as those of amorphous insulators. Deviations occur as a result of the presence of metal inclusions, and may be treated as introducing additional energy levels of the order of 0.1 eV around the Fermi level. This situation is again similar to that of amorphous insulators in which the presence of such levels is identified as due to some specific imperfections in the structure.

Chapter 4 describes the apparatus and procedures used to fabricate the samples and the instruments used in the measurements. The CdSe crystal structure is briefly described. Electron micrographs and x-ray diffraction patterns of CdSe and gold films are also presented.

Chapter 5 deals with the experimental results and interpretations of cermet-silicon contacts.

Chapter 6 discusses the experiments with evaporated CdSe films. Much attention was paid in trying to achieve reproducibility as well as improving the characteristics of Au/CdSe Schottky barriers. The results were rather disappointing and therefore they are discussed in a very general way, pointing out the possible causes of such undesirable consequences. The conclusions of the project are also presented in chapter 6.

CHAPTER 2

THE SPACE CHARGE REGION OF A SEMICONDUCTOR SURFACE

2.1 INTRODUCTION

In order to investigate the effects of an external material placed on the surface of a semiconductor, it is necessary to understand the nature of the semiconductor surface region, i.e. the space charge region. It is generally assumed that the free carriers, namely electrons and holes, still retain their properties as in the bulk. Thus they behave as running waves with effective masses and they occupy the extended states in their well-defined conduction and valence bands. The scattering effects in their motions give rise to their respective finite mobilities as in the bulk, and can be described by the drift and diffusion equations, etc. This is true only if the electric field in the region is not too high, i.e. the doping density is not excessive.

This chapter is mainly concerned with extrinsic, non-degenerate, trap free, homogeneous single crystal semiconductors with fully ionized and uniformly distributed impurities. The extent of the surface (area) and bulk (depth) are assumed to be semi-infinite so that edge effects can be ignored and one-dimensional equations can be used. Although many of the equations and discussions are applicable for both conductivity types, specific reference is to an n-type silicon crystal for the sake of convenience.

Section 2.2 outlines some possible sources for the formation of the space charge, and in Section 2.3 the mathematics of the region is described. This is for the case of thermal equilibrium situation only, i.e. there is no conductive current flow.

Section 2.4 is about the C-V characteristics of the MIS structure. The main focus is on the effects of interface charges since the successful operation of a surface effect device depends on the ability in controlling them and understanding their effects. The next section is about Schottky barriers. Here, the general I-V characteristics are briefly surveyed and possible deviation factors are pointed out. The C-V characteristic is also mentioned.

2.2 FORMATION OF THE SPACE CHARGE REGION

The space charge region of a semiconductor surface is formed because of the requirement of charge balance. Consider the case of an extrinsic n-type semiconductor. In the presence of a certain quantity of negative, say, charges at the surface, the conduction (free) electrons near the surface region of the semiconductor will be repelled. This results in exposing the positively charged donor ions which are immobile, i.e. fixed in space. Equilibrium is established when these un-neutralised donors or space charges equal the negative charges on the surface. Because of the low density of these donors, and hence the conduction electrons, compared with that of the free electrons in a metal, these space charges extend to a certain depth into the bulk of the semiconductor. Therefore a space charge region is created. The existence of this net charged region gives rise to an electrostatic field F_s inside the semiconductor just below the surface given by

$$Q_{sc} = - Q_s = \varepsilon_o \varepsilon_s F_s \qquad (2.1)$$

where Q_{sc} is the total net charge per unit surface area. Q_s is the counter charge outside the surface, and ε_s is the dielectric constant of the semiconductor. The negative sign is introduced for Q_s so that the electric field is positive when directed outwards from the surface. The re-distribution of charges within the space charge

region also results in a net charge which sets up a potential across the region. This potential is generally known as the contact potential.

We now turn our attention to the possible origins of the surface charges. These charges may be due to one or more of the following situations:

(a) Intimate contact is made with a metal having a different work function. (Fig. 2.1)

Initially, charge transfer occurs between the metal and semiconductor until their Fermi levels are at the same level as required for thermal equilibrium conditions. In the case where the Fermi level of the semiconductor is higher than that of the metal, electrons flow from the former into the latter. The contact potential V_{bi} in the space charge region is therefore given by the difference in their initial Fermi levels, i.e. their work functions W_m, W_s. Thus

$$-qV_{bi} = W_m - W_s \qquad (2.2)$$

A negative sign is used before V_{bi} to indicate that the energy bands at the surface bend upwards with respect to their positions in the bulk. This kind of contact barrier is known as a Schottky barrier, more details of which will be discussed in a later section. The energy diagram of this is shown in Fig. 2.1.

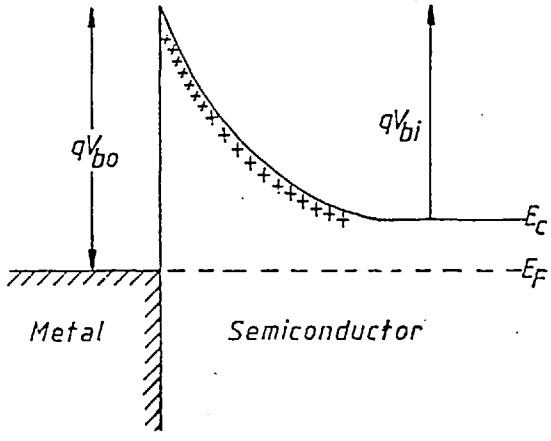

Fig.2.1 Intimate metal-semiconductor contact.

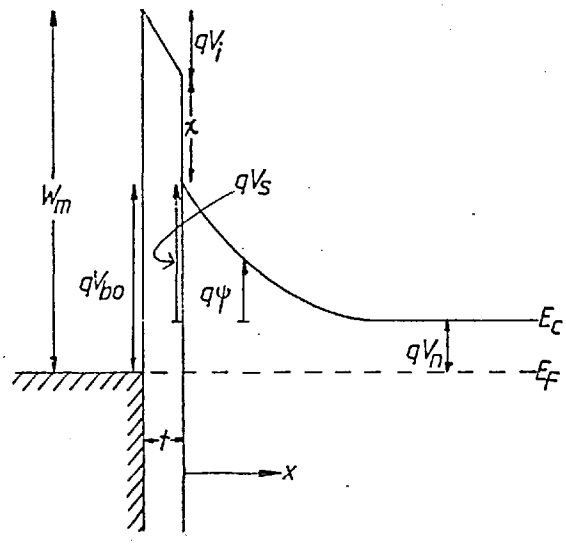

Fig.2.2 Non-intimate metal-semiconductor contact.

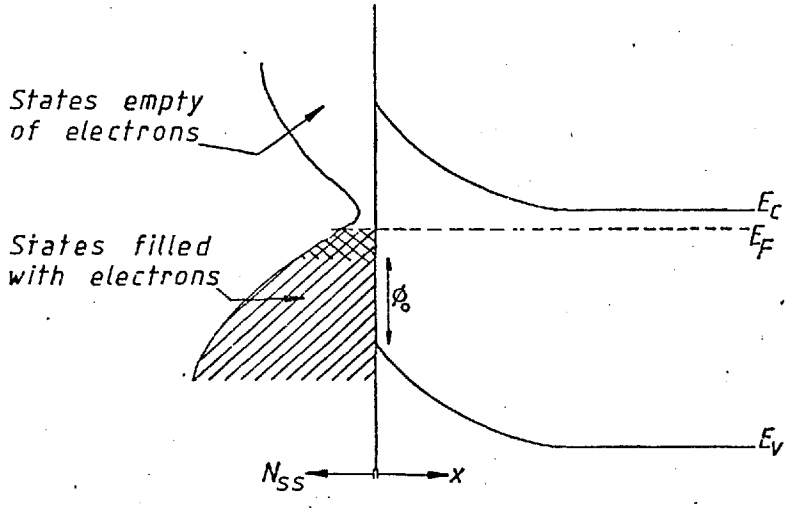

Fig.2.3 Intrinsic surface state density.

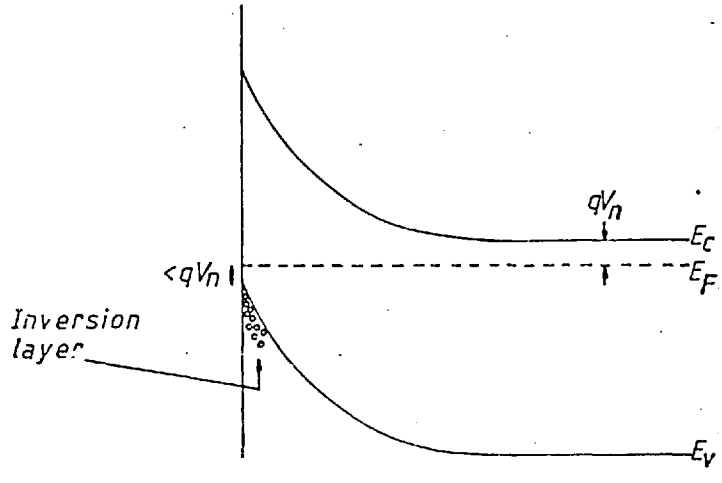

Fig.2.4 Inverted semiconductor surface.

(b) The contact between the metal and the semiconductor is separated by an empty space or insulator of thickness t (Fig. 2.2).

In this case, we still have the Fermi levels at the same height at thermal equilibrium but a finite electric field F_i, and hence a voltage drop V_i, exists within the insulating space. These are given by

$$Q_{sc} = - Q_m = \varepsilon_o \varepsilon_i F_i = \varepsilon_o \varepsilon_s F_s \tag{2.3}$$

$$V_i = - F_i t \tag{2.4}$$

where ε_i and ε_s are the dielectric constants of the insulator spacing and semiconductor respectively, and Q_m is the charge density on the metal. As a result, eqn. (2.2) should be modified to

$$- q(V_{bi} + V_i) = W_m - W_s \tag{2.5}$$

(c) Some charge species present near the semiconductor surface.

For instance, sodium atoms on the surface may give up electrons to the conduction band and form sodium ions. Also, the surface would inevitably have an oxide layer which may contain some charged ions or energy states capable of trapping electrons or holes.

(d) It is the intrinsic nature of the semiconductor surface to have some energy states capable of trapping charges.

These are the so-called surface states associated with the unfilled orbitals or dangling bonds of the surface atoms. Generally, the energy bands of a single crystal are derived with the assumption that semi-infinite periodic potential energy exists within the bulk. But since this periodicity is lost at the surface, the energy bands are no longer identical here. However it can be shown[1] that additional energy states known as Tamm states and Schottky states are introduced into the energy structure as a result of this departure from periodicity. These states are localised in the sense that electrons here are confined to the surface atoms rather than being shared with the entire crystal. On the energy diagram, these are represented as energy states or traps in the forbidden gap. They are generally distributed in energy and are quoted in number of states per unit area per eV. By analogy with the doping impurity states in the bulk, the surface states can also be termed as donor-like or acceptor-like states depending on their charge conditions when filled or empty of electrons. Also, a Fermi level may be ascribed to described the occupation statistics of these states. Fig. 2.3 shows an energy

diagram with a hypothetical distribution of surface state density N_{ss} in thermal equilibrium with the bulk. The net charges of these surface states are neutral when the Fermi level is positioned at an energy ϕ_o above the valence band edge at the surface. However, in the situation shown, in order for the Fermi level to get into a horizontal position throughout the system, the cross-hatched portion above ϕ_o of the surface states also has to be filled with electrons. Hence a positive space charge region is formed at the semiconductor surface to balance these negative surface charges.

2.3 EQUATIONS RELATED TO THE SPACE CHARGE REGION UNDER THERMAL EQUILIBRIUM

2.3.1 General Equations

Consider a homogeneous, semi-infinite semiconductor single crystal under thermal equilibrium. Let there be a uniform, fully ionized net doping density, N which can be of either donors or acceptors. It is good enough for our purpose to use Boltzmann's statistics to describe the occupation of energy levels by carriers since in most cases, these levels are more than several kT from the Fermi level.

The free electron and hole densities in the conduction and valence bands are given by

$$n = N_c \exp(-\beta(V_n - \psi(x))) \tag{2.6}$$

$$p = N_v \exp(-\beta(V_g - V_n + \psi(x))) \tag{2.7}$$

Where $\beta = q/kT$

The symbols are as indicated in Fig. 2.2. Using n_b and p_b as their densities in the bulk, then

$$n = n_b \exp(\beta\psi(x)) \tag{2.8}$$

$$p = p_b \exp(\beta\psi(x)) \tag{2.9}$$

with

$$n_b p_b = n_i^2 = N_c N_v$$

and (2.10)

$$N = n_b - p_b$$

where N is the net donor density. The net charge density at position x is

$$\rho(x) = q\ (N + p - n) \tag{2.11}$$

The potential at x is given by Poisson's equation

$$\frac{d^2\psi}{dx^2} = - \frac{\rho}{\varepsilon_o \varepsilon_s} \tag{2.12}$$

and the electric field is

$$F(x) = - \frac{d\psi}{dx} \tag{2.13}$$

The appropriate boundary conditions are that, at the surface (x = 0) and in the bulk ($x \to \infty$), one has $\psi(0) = V_s$ and $\psi(\infty) = 0$ respectively.

Putting eqns. (2.8) - (2.11) into (2.12) and then multiplying both sides by $2d\psi/dx$ before integrating, one obtains

$$\left(\frac{d\psi}{dx}\right)^2 = \frac{2q}{\beta\varepsilon_o\varepsilon_s}\left[p_b(\exp(-\beta\psi) + \beta\psi - 1) + n_b(\exp(\beta\psi) - \beta\psi - 1) \right] \tag{2.14}$$

when the boundary condition of $d\psi/dx = 0$ at $\psi = 0$ is used. Eqn.(2.14) cannot be solved in closed form for the general case, and a numerical method has to be used[1]. The electrostatic field F_s at the surface is obtained by putting $\psi = V_s$. From this, the space charge density Q_{sc} as given by eqn. (2.1) can be derived, thus

$$Q_{sc} = \varepsilon_o \varepsilon_s F_s$$

$$= \pm \left(\frac{2q\varepsilon_o\varepsilon_s}{\beta}\right)^{\frac{1}{2}} \left[p_b(\exp(-\beta V_s) + \beta V_s - 1) + n_b(\exp(\beta V_s) - \beta V_s - 1) \right]^{\frac{1}{2}}$$

$$= \pm \left(\frac{2q\varepsilon_o\varepsilon_s}{\beta}\right)^{\frac{1}{2}} H \qquad (2.15)$$

The upper sign (+) refers to $V_s < 0$ and the lower sign (-) is for $V_s > 0$. One can see from eqn. (2.15) that the former term in the square bracket is the contribution from holes, i.e. minority carriers for n-type semiconductor, whereas the latter term is due to electrons.

A space charge capacitance can be defined as the change in space charge density as a result of a change in the potential V_s. Thus

$$C_{sc} = \left| \frac{d\, Q_{sc}}{d\, V_s} \right|$$

$$= \left(\frac{q\varepsilon_o\varepsilon_s\beta}{2}\right)^{\frac{1}{2}} \frac{\left| p_b(\exp(-\beta V_s) + 1) + n_b(\exp(\beta V_s) - 1) \right|}{H} \qquad (2.16)$$

The above solutions are quite general and many simplifications can be made for an extrinsic semiconductor. We are concerned with n-type materials so that $N \sim n_b >> P_b$. The following cases can be identified for different space charge conditions.

2.3.2 Accumulation Region

This is the case when $\beta V_s >> 1$, i.e. the surface potential bends downwards and electrons accumulate on the surface. The space charge density is then mainly due to these electrons in the conduction band. Eqns. (2.15) and (2.16) then become

$$Q_{sc} = - \left(\frac{2q\varepsilon_o\varepsilon_s n_b}{\beta} \right)^{\frac{1}{2}} \exp\left(\frac{1}{2} \beta V_s\right) \qquad (2.17)$$

$$C_{sc} = \left(\frac{q\varepsilon_o\varepsilon_s \beta n_b}{2} \right)^{\frac{1}{2}} \exp\left(\frac{1}{2} \beta V_s\right) \qquad (2.18)$$

The approximate potential in the space charge region can also be derived from eqn. (2.14). Thus

$$\exp\left(\frac{-1}{2}\beta V_s\right) - \exp\left(\frac{-1}{2} \beta\psi\right) = \left(\frac{q\beta n_b}{2\varepsilon_o\varepsilon_s} \right)^{\frac{1}{2}} x \qquad (2.19)$$

2.3.3 Depletion Region

When βV_s is moderately large and negative so that both free carriers in the conduction and valence bands in the space charge region are negligible, the space charge density is made up mainly of the un-neutralised net donors. It is convenient to write $V_d = |V_s|$ so that a positive value, V_d, the diffusion potential, also known as the depletion potential in this case, can be used. Eqns. (2.15), (2.16) and (2.14) become

$$Q_{sc} = \left[2q\varepsilon_o\varepsilon_s n_b (V_d - \frac{kT}{q}) \right]^{\frac{1}{2}} \tag{2.20}$$

$$C_{sc} = \left[\frac{q\varepsilon_o\varepsilon_s n_b}{2(V_d - kT/q)} \right]^{\frac{1}{2}} = \frac{\varepsilon_o\varepsilon_s}{\ell} \tag{2.21}$$

$$\psi_{(x)} = - \frac{qn_b}{2\varepsilon_o\varepsilon_s} (\ell - x)^2 \tag{2.22}$$

where

$$\ell = \left(\frac{2\varepsilon_o\varepsilon_s V_d}{qn_b} \right)^{\frac{1}{2}} \tag{2.23}$$

ℓ is known as the depletion layer width. The maximum electric field which occurs at the surface is given by $d\psi/dx\big|_{x=0}$. Thus

$$F_s = F_m = \left(\frac{2qn_b V_d}{\varepsilon_o\varepsilon_s} \right)^{\frac{1}{2}} = \frac{qn_b\ell}{\varepsilon_o\varepsilon_s} \tag{2.24}$$

2.3.4 Inversion Region (Fig. 2.4)

For this case, the energy bands in the space charge region have bent to such a great extent that the minority (hole) carriers dominate in contributing to the space charge density. We still use $V_d = |V_s|$. From eqn. (2.15) one sees that the condition for inversion to take place is

$$p_b \exp(\beta V_d) >> n_b . \tag{2.25}$$

i.e. the hole density at the surface becomes much larger than the free electron density in the bulk. This corresponds

to

$$V_d > V_g - 2\,V_n \tag{2.26}$$

This situation is shown in Fig. 2.4. Eqns. (2.15), (2.16) and (2.14) become

$$Q_{sc} = \left(\frac{2q\varepsilon_o\varepsilon_s p_b}{\beta} \right)^{\frac{1}{2}} \exp\left(\frac{1}{2}\,\beta V_d\right) \tag{2.27}$$

$$C_{sc} = \left(\frac{q\varepsilon_o\varepsilon_s\beta p_b}{2} \right)^{\frac{1}{2}} \exp\left(\frac{1}{2}\,\beta V_d\right) \tag{2.28}$$

$$\exp\left(\frac{1}{2}\,\beta\psi\right) - \exp\left(\frac{-1}{2}\,\beta V_d\right) = \left(\frac{q\beta p_b}{2\varepsilon_o\varepsilon_s} \right)^{\frac{1}{2}} x \tag{2.29}$$

Beware that ψ is negative. Note the similarities of these equations with those for the accumulation region.

2.4 METAL-INSULATOR-SEMICONDUCTOR [2-5]

Consider the case of a perfect insulator with no trapped charges and no interfacial states at the semiconductor surface. The capacitance of such a system is made up of two components in series, one is the insulator capacitance C_o and the other is the space charge capacitance C_{sc} of the semiconductor. Therefore

$$C = \frac{C_o C_{sc}}{C_o + C_{sc}} \tag{2.30}$$

C_{sc} is a function of bias voltage but C_i is assumed not to be. Assuming that at zero bias, no space charge is formed at the semiconductor surface, i.e. the work functions of the metal and semiconductor are equal. C_{sc} is then given by eqn. (2.16) with $V_s \to 0$. This is the flat-band value $C_{FB}=(q\varepsilon_o\varepsilon_s\beta N)^{\frac{1}{2}}$. When a voltage V_a is applied on the metal with respect to the semiconductor, it is shared between the insulator and the semiconductor space charge such that the electrostatic field is given by eqn. (2.3). If the voltage across the insulator is V_i, which is given by eqn. (2.4), then $V_a = V_i + V_s$. Since there is no current flow due to V_a the semiconductor space charge region can be considered as at thermal equilibrium with the bulk so that the analysis given in section 2.3 applies. When V_a is positive, V_s is also positive and electrons accumulate at the semiconductor surface, resulting in an accumulation region. From eqns. (2.17) and (2.18) both Q_{sc} and C_{sc} increase exponentially with V_s so that the change in V_i is about equal to the change in V_a.

C_{sc} soon becomes much greater than C_o and from eqn. (2.30) we have $C \sim C_o$. When V_a goes negative, a depleted space charge region is formed. From eqn. (2.21) C_{sc} decreases parabolically with V_d where $V_d = |V_s|$. Thus the measured capacitance C also decreases. When V_a is increased further, minority carriers soon begin to accumulate at the semiconductor surface, resulting in the formation of an inversion region. C_{sc} again increases exponentially according to eqn. (2.28) and once again we have $C \sim C_o$. A sketch of the C-V_a curve is given in Fig. 2.5 (solid line). Many authors [2-5] have given extensive discussions on this subject. Here, we only discuss a few factors which are most likely to cause deviations from such C-V_a curves. The energy diagram referred to in the discussions is shown in Fig. 2.6.

(a) <u>Difference in work functions between metal and semiconductor:</u>

This results in a formation of a space charge potential (the contact potential V_{bi}) and a potential dropped across the insulator as given by eqn. (2.5) even before a voltage is applied. Consequently, the C-V_a curve would be shifted along the V-axis by $V_{FB} = (W_m - W_s)/q$, which is known as the flat-band voltage.

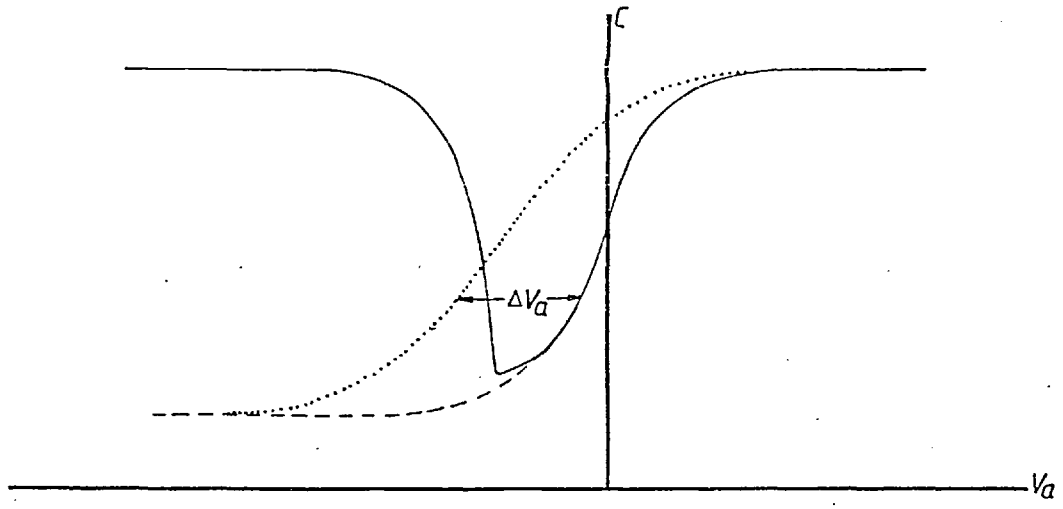

Fig. 2.5 C - V curves of a MIS structure: ideal curves at (full line) low frequency, (dash line) high frequency, and (dotted line) from high frequency experimental results.

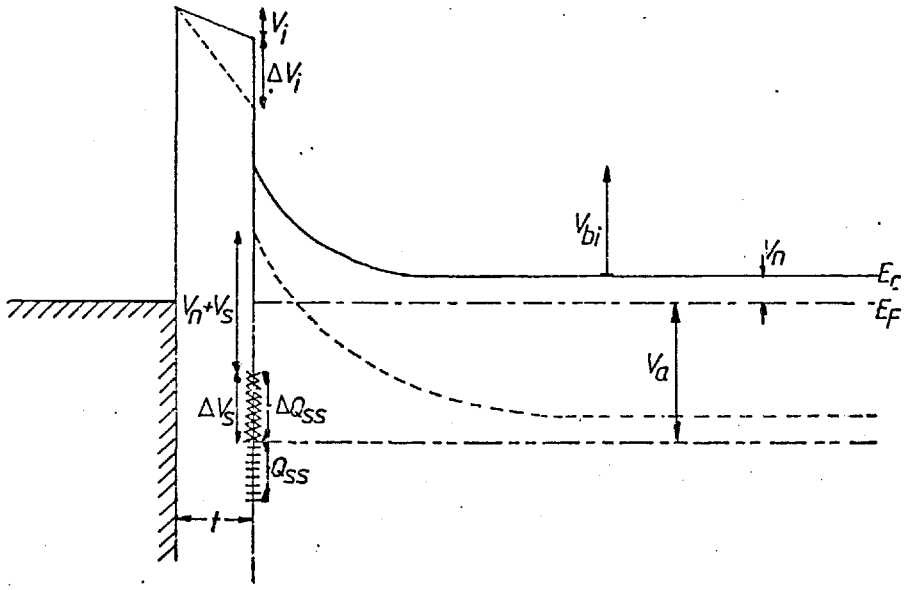

Fig. 2.6 Energy (in electron volts) diagram of a MIS structure: (full line) at zero bias, (dash line) at negative bias.

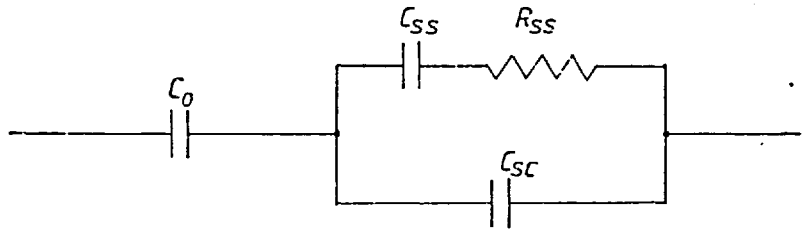

Fig. 2.7 Equivalent circuit of a MIS structure.

(b) Fixed charges in the insulator:

This again results in a different V_{bi} and V_i before an applied bias and therefore a new value of V_{FB}. If these charges remain fixed irrespective of the applied bias, then the shape of C-V_a is not altered.

(c) Response of minority carriers:

The above discussions assumed that both majority and minority carriers are able to follow the measuring signal. However, this may not be so for the minority carriers in the inversion region because, if they have to go through the semiconductor bulk in order to arrive at the surface to form the inversion layer, then the path is very resistive due to the very low minority carrier density. This may be considered as the charging of the insulator capacitance $C_o = \varepsilon_o \varepsilon_i / t$ through the valence band resistance $R_p = d/p_b q \mu_p$ where d is the epitaxial layer thickness. Using $p_b \sim 10^{11} m^{-3}$ ($n_b \sim 2 \times 10^{21}\ m^{-3}$), $d \sim 9\ \mu m$, $t = .1\ \mu m$ and $\varepsilon_i \sim 4\varepsilon_o$, these give the time constant $\tau \sim C_o R_p \sim 2s$. However these carriers may also be generated thermally or through Shockley-Read-Hall centers[6] so that the effective time constant normally observed is $\sim 10^{-2} s$. As a result, these minority carriers, though able to follow the dc bias voltage, are

unable to follow signal frequency of greater than about 100 Hz. Therefore the measured space charge capacitance C_{sc} would be due to the response of the majority carriers only. This can be derived from eqn. (2.16) by ignoring p_b (for n-type material). Thus

$$C_{sc} = \left(\frac{q\varepsilon_o\varepsilon_s\beta}{2}\right)^{\frac{1}{2}} \left[\frac{\exp(\beta V_s) - 1}{n_b^{\frac{1}{2}}[\, \exp(\beta V_s) - \beta V_s - 1\,]^{\frac{1}{2}}} \right] \qquad (2.31)$$

However the space charge density Q_{sc} and surface potential V_s are related by eqn. (2.15) since these values are set by the dc bias. The resultant MIS capacitance curve is shown in Fig. 2.5 with a dash line.

(d) Surface charges:

We differentiate surface charges from those of case (b) above by identifying these as charges that are able to come into thermal equilibrium, within a short time after the applied bias V_a is changed, with the semiconductor bulk. By a short time, it is meant the time between the change of the dc bias voltage and when the capacitance reading is taken. Therefore the Fermi-level used to describe the occupancy statistics of these states coincides with that for the free carriers in the semiconductor.

These charges are due not only to the instrinsic surface states but also include charges which are at about a nano-meter in the insulator from the actual semiconductor/insulator interface. It is therefore perhaps more appropriate to call them interface states. In general, these states are distributed in space as well as energy. They can communicate with the semiconductor bulk through the free carriers in the conduction and valence bands at the surface. Since the densities of these free carriers are finite, each set of the interface states has a finite response time or life time. For those states situated at the semiconductor surface proper, the rate equation of a single level or state can be derived in a similar way as with Shockley-Read-Hall center. Hence we we may write the response time as[7]

$$\tau_t = \frac{1}{c_n(n_s + n_1) + c_p(p_s + p_1)} \qquad (2.32)$$

where c_n and c_p are the capture constants of the centres for electrons and holes, n_s and p_s are the free electron and hole densities at the surface, n_1 and p_1 are given by

$$n_1 = N_c \exp(-(E_c - E_t)/kT)$$
$$p_1 = N_v \exp(-(E_t - E_v)/kT \qquad (2.33)$$

with E_t the energy position of the centre, respectively. It is seen that the response time is a very sensitive function of the energy position of the centre as well as the Fermi level. For those centres that are at some distance away from the semiconductor, the matter is more complicated because a tunnelling probability factor has to be considered[8].

In general, one may expect that the effective time constant is a function of the applied voltage as well as the signal frequency used to measure the capacitance. Consequently, the C-V_a plot can be very misleading and care should be taken in interpreting them. However, in practice, it is found that almost all interface states have response times greater than about 1 μs so that if the signal frequency is higher than about 1 MHz, one may assume that no interface states are able to follow it. These states can therefore be ignored as far as the capacitance measured with the ac signal is concerned. But the free majority carriers would still be able to follow the ac signal since their response time is the dielectric relaxation time which is of the order of 10^{-12} second. The capacitance measured at any particular dc bias voltage V_a is therefore given by the series combination of the insulator

capacitance C_o and space charge capacitance C_{sc} due to the majority carriers. Knowing C_o, one can calculate C_{sc} and from eqns. (2.15) and (2.31), Q_{sc} and V_s can be derived. Note that eqn. (2.31) instead of eqn. (2.16) is used to derive V_s because the signal frequency is so high that the minority carriers are normally unable to respond. However eqn. (2.15) should be used to determine Q_{sc} since this is set by the dc bias. In this way, both V_s and Q_{sc} as a function of V_a is obtained. Now, charge balance requires that

$$-Q_m = Q_{sc} + Q_{ss} + Q_o \qquad (2.34)$$

where Q_{ss} is the interface charge density and Q_o is the fixed charge density (per unit area) in the insulator. If the difference in work functions between the metal and the semiconductor bulk is V_{ms}, then one has $V_a + V_{ms} = V_i + V_s$ where V_i is the voltage across the insulator. The charge density on the metal plate is given by $Q_m = C_o V_i = C_o(V_a + V_{ms} - V_s)$. Thus, from eqn. (2.34), we obtain

$$- C_o(V_a + V_{ms} - V_s) = Q_{sc} + Q_{ss} + Q_o \qquad (2.35)$$

Therefore, if we know C_o and V_{ms}, and also Q_{sc} and V_s as a function of V_a, we are able to

plot $Q_{ss} + Q_o$ against V_s. It is usually more useful to know the interface state density in terms of $qN_{ss} = dQ_{ss}/dV_s$ (states m^{-2} eV^{-1}). This can be obtained from the slope of the plot since Q_o is a constant. Eqn. (2.35) also indicates the extent of the screening effect of the interface charges. By differentiating it with respect to V_s, one obtains

$$\left| \frac{dV_a}{dV_s} \right| = \frac{1}{C_o} \left(\frac{dQ_{sc}}{dV_s} + \frac{dQ_{ss}}{dV_s} \right) + 1$$

$$= \frac{1}{C_o} (C_{sc} + qN_{ss}) + 1 \qquad (2.36)$$

$$= \frac{t}{\varepsilon_o \varepsilon_i} \left(\frac{\varepsilon_o \varepsilon_s}{\ell} + qN_{ss} \right) + 1 \qquad (2.37)$$

In order to obtain N_{ss} over a wide energy distance, say 0.5 eV, across the energy gap, V_s should change by the same amount as a result of the change in an applied voltage V_a by, say, 10 volts. Assuming that N_{ss} is constant, then it requires that $dV_a/dV_s < 20$. For a semiconductor with $N \sim 2 \times 10^{21}$ m^{-3} and diffusion potential $V_d \sim 0.5$ eV, eqn. (2.23) gives $\ell \sim 0.5$ μm. If the insulator thickness $t = 0.1$ μm and $\varepsilon_i \sim 4\varepsilon_o$ for SiO_2, then putting these values into eqn. (2.37) shows that N_{ss} must be less than about 2×10^{16} states m^{-2} eV^{-1}. In other words, if $N_{ss} > 2 \times 10^{16}$ states m^{-2} eV^{-1}, then the surface potential of the

semiconductor is hardly changed by any applied bias, i.e. the measured capacitance remains virtually constant.

The charge density $Q_{ss} + Q_o$ against V_s can also be obtained graphically by noting that if there were no Q_{ss} and Q_o then eqn. (2.35) becomes

$$- C_o(V'_a + V_{ms} - V_s) = Q_{sc}$$

Subtracting this from eqn. (2.35) gives

$$- C_o(V_a - V'_a) = Q_{ss} + Q_o$$

V'_a is of course the applied voltage for an ideal MIS structure. Referring to Fig. 2.5, at any particular measured C, V_s can be found as before and $\Delta V_a = V_a - V'_a$ is the additional applied voltage required to bring $C_i \Delta V_a$ charges to balance the total surface charges $Q_{ss} + Q_o$.

We now turn our attention to the situation when the signal frequency is low enough that the interface charges are able to follow it. The charging and discharging current of these interface states gives rise to a capacitive component. This capacitance is given by

$$C_{ss} = \frac{dQ_{ss}}{dV_s} = q\, N_{ss} \qquad (2.38)$$

The finite response time of these states can be accounted for by putting a resistance R_{ss} in series. This RC equivalent circuit can be considered as shunted across the space charge capacitance C_{sc}[2] as shown in Fig. 2.7. Since, in general, there are many kinds of centres with different response time constants, a corresponding number of RC circuits have to be introduced into the equivalent circuit. This results in a frequency dispersion of the observed time constant. However, if the surface state density is not too high, then if one were to carry out the analysis as outlined previously by ignoring their response to the signal frequency, the variations of Q_{ss} with different signal frequencies thus obtained would give one an idea of the spread in time constants involved. Otherwise, in order to have a more quantitative analysis, it is of course necessary to know the variation of V_s with V_a. This can be obtained with high frequency measurements as before. But if high frequency is inaccessible, perhaps due to the presence of very fast interface states, a low frequency method can be used as follows. Returning to eqn. (2.36), this can be rearranged to give

$$\frac{dV_s}{dV_a} = \frac{C_o}{C_{sc} + C_{ss} + C_o} = 1 - \frac{C}{C_o} \qquad (2.39)$$

where C is the total (measured) capacitance for a circuit shown in Fig. 2.7 with $R_{ss} = 0$ (or $R_{ss} << {}^{1}/_{wC_{ss}}$); in other words, C is the capacitance obtained with a signal frequency so low that all the interface states as well as the minority carriers are able to follow it. Integrating eqn. (2.39) gives

$$V_s(V_2) - V_s(V_1) = \int_{V_1}^{V_2} \left(1 - \frac{C}{C_o}\right) dV_a \qquad (2.40)$$

Hence, the relationship of V_s against V_a can be obtained to within a constant. This expression has also been obtained by Berglund[9].

2.5 SCHOTTKY BARRIER[10]

2.5.1 Introduction

Ideally, for an n-type semiconductor, this is formed when a metal of higher work function is brought into contact with it. The resultant diffusion potential is given by eqn. (2.2). However, in practice, it is found that this expression is far from being abeyed. The reason is not only that the work function of a metal is not a well defined value, being affected by the actual circumstances in which it is being prepared and measured, but also to a much greater extent, is due to the presence of surface states on the semiconductor surface. If these surface state densities are extremely high, it effectively screens off the semiconductor from any material put on its surface. Thus, initially, the diffusion potential would be determined by the nature of these surface states as discussed in section 2.2. When a metal is brought close to the surface, the Fermi level at the surface needs only have to shift by a comparatively small amount to accommodate enough change in surface charges so as to balance the charges on the metal plate. As a result the potential due to the difference in work functions of the metal and the semiconductor with surface states is mainly dropped across an interfacial layer of atomic thickness (order of a nano-meter). This situation was considered by Cowley and Sze[11] who showed that the barrier height V_{bo} which is given by $V_{bo} = V_{bi} + V_n$

is related approximately to the work function W_m of the metal by $qV_{bo} = C_2 W_m + C_3$ where C_2 and C_3 are functions of surface state density and the interfacial layer thickness.

From this short discussion, it is clear that the barrier height of any particular Schottky barrier system is expected to vary with different conditions of preparation which may introduce different densities and natures of surface states. By surface states here, we are not confined to intrinsic surface states alone which applies only in the case of ultra-high vacuum cleavage of the semiconductor crystal and immediate deposition of the metal before the surface is contaminated by residual gas molecules. We are more concerned with real surface which would include an interfacial layer with energy states due to foreign matters. There are various methods available for determining the barrier height[12]. The more easily performed ones, with equipments readily available in any standard science laboratory, are perhaps the I-V and C-V measurements.

2.5.2 I-V Characteristics

When an external voltage is applied on the metal with respect to the semiconductor bulk, a current would flow. The energy diagram showing a forward bias voltage V across the space charge region is given in Fig. 2.8. The passage of an electron through the barrier encounters two limiting mechanisms in series. One is governed by the drift and diffusion process in the space charge

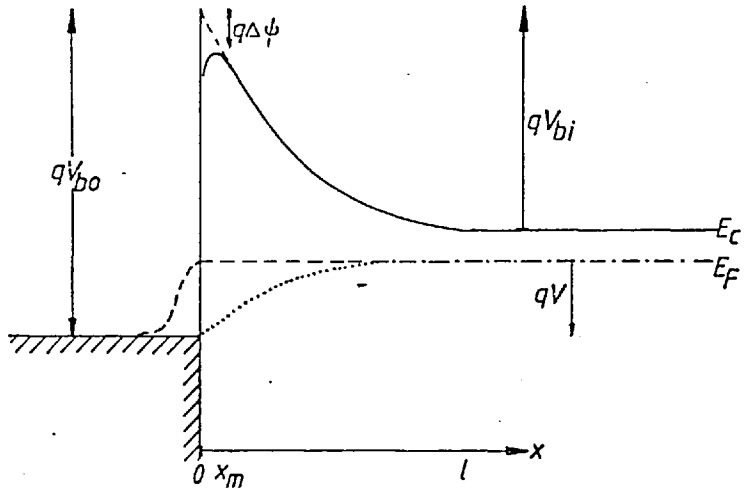

Fig. 2.8 Energy diagram of a Schottky barrier under forward bias for: (dash line) thermionic model, (dotted line) diffusion model.

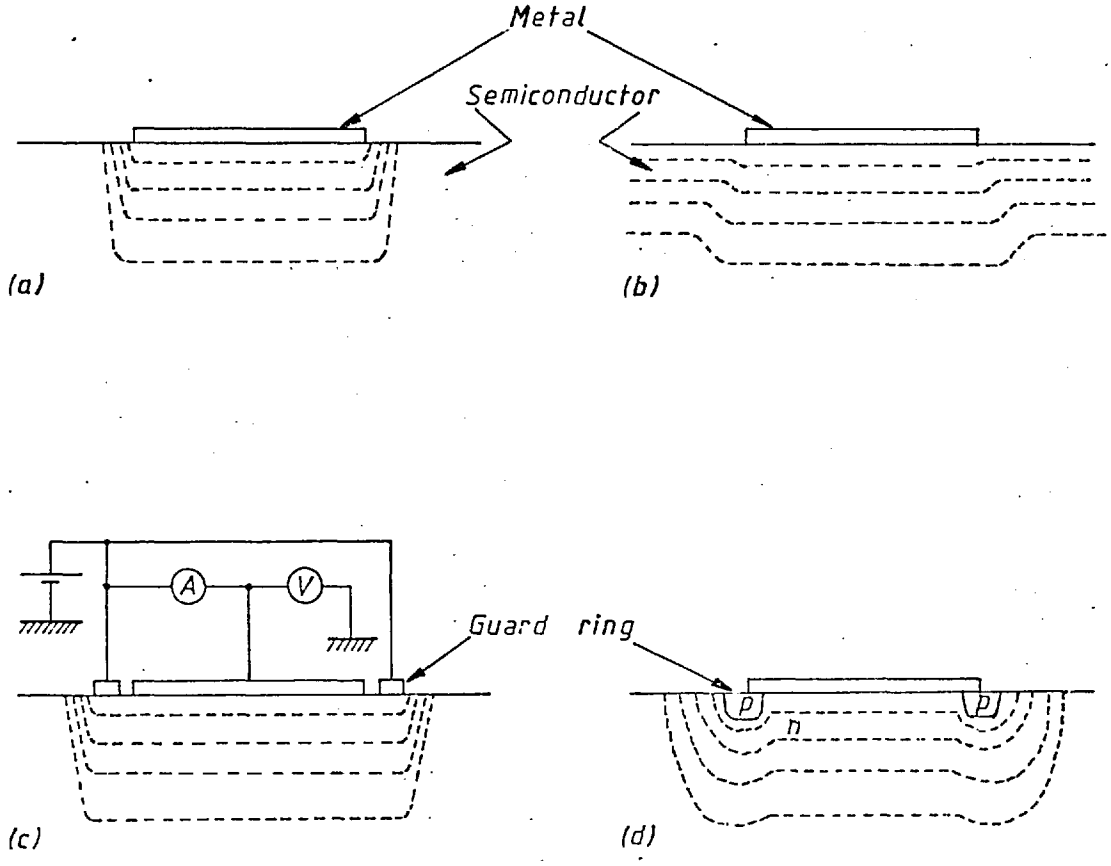

Fig. 2.9 Equipotential lines (dash lines) showing edge effects: (a) flat band surface, (b) depleted surface, (c) Schottky barrier guard ring, (d) diffused p-n junction guard ring.

region and is generally known as the diffusion model. The other is the emission process when it reaches the metal-semiconductor interface. This is the thermionic-emission model proposed by Bethe[13]. For the former case the electron current can be written as

$$J = q\mu n \frac{dE_{Fn}}{dx} \tag{2.41}$$

One sees from this equation that the driving force of the current is the bending of the electron quasi-Fermi level E_{Fn}. In the bulk, E_{Fn} remains at its thermal-equilibrium position since the free electron density n is high. On approaching the surface, n decreases and hence dE_{Fn}/dx has to increase so as to maintain current continuity. At the interface, one may assume that E_{Fn} has bent so much as to coincide with the metal Fermi-level, i.e. electrons at the semiconductors side of the interface are in thermal-equilibrium with those in the metal. In Fig. 2.8 the dotted line is used to indicate E_{Fn} for this situation.

For the case of the thermionic-emission model, basically, in order that an electron is able to cross the interface, it must possess enough kinetic energy to surmount the barrier height. The barrier height encountered by the approaching electron is actually lowered by the image charge it induces in the metal. This image charge, being positive, sets up an attractive force on the electron and hence effectively lowers its

potential energy. As a result, the barrier height is lowered by

$$\Delta\phi = \left(\frac{q}{4\pi\varepsilon_o\varepsilon_d}\right)^{\frac{1}{2}} \left(\frac{2qN}{\varepsilon_o\varepsilon_s}\right)^{\frac{1}{4}} (V_{bi}-V-kT/q)^{\frac{1}{4}} \qquad (2.42)$$

where ε_d is an image force dielectric constant and the maximum potential occurs at some distance x_m inside the semiconductor from the interface. ε_d is a function of the electron transit time between $x = 0$ and $x = x_m$ and the dielectric relaxation time of the semiconductor. If the transit time is greater than the relaxation time, then $\varepsilon_d = \varepsilon_s$. Otherwise ε_d approaches unity. Since this model assumes that there is no scattering process within the space charge region, it means that the electron mobility μ is very high so that, from eqn. (2.41), the quasi-Fermi level bends little across this region. On the limit, E_{Fn} is assumed to remain horizontal right up to the interface, shown as a dash line in Fig. 2.8. This implies that the electrons at the potential maximum is at thermal equilibrium with the semiconductor bulk. Any electrons emitted into the metal may be treated as hot electrons, or that the metal behaves like a p-type semiconductor so that 'excess' of electrons are being injected into it[14].

Since these two processes occur in series, it should be possible to combine them[15]. Effectively this involves finding the position of the quasi-Fermi level at the interface so that the current flow due to

each process are equal[16]. By introducing the concept of a collection velocity v_c which describes the net electron current flowing into the metal across the potential maximum and an effective diffusion velocity v_d which describes the transport of electrons in the space charge region and hence is a function of the actual potential energy $\psi(x)$ that the electrons encounter in this region, Crowell and Sze[15] showed that the current density can be written as

$$J = \frac{qN_c v_c}{1 + v_c/v_d} \exp(-\beta(V_{bo} - \Delta\phi))[\exp(\beta V) - 1] \quad (2.43)$$

The dominant process which limits the current is therefore determined by the ratio v_c/v_d. If it is assumed that all electrons with enough energy to surmount the potential maximum would be collected by the metal with none being scattered back into the semiconductor, then the collection velocity is[17]

$$v_c = A^* T^2/qN_c = \bar{v}/4$$

where $\bar{v} = (8\ kT/\pi m^*)^{\frac{1}{2}}$ is the average thermal velocity of the electrons in the semiconductor. A^* is an effective Richardson constant for thermionic-emission and is given by $4\pi m^* qk^2/h^3 = 120 \times 10^4 (m^*/m)\ A/m^2k^2$. Since m^* is proportional to the radius of curvature of the constant-energy surface, it would differ for different directions of electron motion for an anisotropic surface. Calculations made by Crowell[18] showed that

the values for silicon are m^*/m = 2.05 for <100> and 2.15 for <111> directions. However, the theory of quantum mechanics indicates that there is a finite probability of an energetic electron being reflected while crossing a barrier of lower energy, and that an electron of lower energy may be able to tunnel through a barrier of higher energy. Furthermore, since the potential maximum occurs at some distance x_m inside the semiconductor, then, even after an electron has crossed this potential maximum, it may still be scattered back by the absorption or emission of a phonon while still in the region x = 0 and x = x_m. Crowell and Sze[15] showed that these phenomena can be accounted for by replacing A^* with A^{**}. Andrew and Lepselter[19] showed that A^{**} varies with the maximum electric field and has a mean value of 110 x 10^4 A/m^2k^2 for electrons in n-type and 32 x 10^4 A/m^2k^2 for holes in p-type silicon. Hence, if thermionic-emission process is mainly responsible for the electron transport, then eqn. (2.43) reduces to

$$J = A^{**} T^2 \exp(-\beta(V_{bo} - \Delta\phi))[\exp(\beta V) - 1] \quad (2.44)$$

The diffusion velocity v_d in eqn. (2.43) can be derived if suitable approximation of the space charge potential energy $\psi(x)$ (example, eqn. (2.22)) is used and that the electron mobility, μ is assumed to be independent of electric field[16]. The result shows that $v_d \simeq \mu F_m$ where F_m is the maximum electric field in the barrier as given by eqn. (2.24). Hence, the current

predicted by the diffusion model, i.e. with $v_d << v_c$ is

$$J \simeq qN_c\mu F_m \exp(-\beta(V_{bo} - \Delta\phi))[\exp(\beta V) - 1] \quad (2.45)$$

This shows that the pre-exponential term depends slightly upon the applied bias, since $F_m \alpha (V_{bi} - V)^{\frac{1}{2}}$. But its effect on the saturation current actually observed is relatively small compared with that due to the barrier height lowering $\Delta\phi$.

Now, according to Bethe, the condition for the validity of the thermionic-emission model is that the mean-free-path ℓ of the electron must be longer than the distance in which the potential maximum has decreased by kT/q. If the maximum field is F_m, then the potential drops by kT/q in a distance $d = kT/qF_m$ and Bethe's criterion requires that $\ell > d$. For silicon with $N = 2.5 \times 10^{21}$ m^{-3} and typically $V_{bo} = 0.8$ eV, we have, from eqn. (2.24), $F_m \sim 2 \times 10^6$ Vm^{-1}. Thus, the criterion requires that $\ell > 5$ nm. Since $\tau = \mu m^*/q \sim 3 \times 10^{-13}$ s and $\bar{v} = (8\ kT/\pi m^*)^{\frac{1}{2}} \sim 2 \times 10^5$ ms^{-1} for $m^* = 0.3$ m, we have $\ell = \bar{v}\tau \sim 60$ nm. Therefore we may assume that the thermionic-emission process dominates the carrier transport even for moderately high forward bias[16,20].

2.5.3 Other Effects Affecting the I-V Characteristics

(a) Minority Carrier Injection:

So far we have neglected the minority carriers (holes in n-type semiconductors). Assuming that the hole quasi-Fermi level coincides with the metal Fermi level[20], then the hole diffusion current density is given by

$$J_h = \frac{qD_h p_b}{L} \left[\exp(\beta V) - 1 \right] , \quad L \ll L_p \qquad (2.46)$$

where L is the thickness of the neutral region in the epitaxial layer. Defining the hole injection ratio as $\gamma = J_h/J_e$ we have, from eqns. (2.44) and (2.46)

$$\gamma = \frac{qD_h n_i^2}{L\ N\ A^{**}\ T^2 \exp(-\beta V_{bo})} , \quad L \ll L_p \qquad (2.47)$$

Using values of $N = 2.5 \times 10^{21}\ m^{-3}$, $V_{bo} = 0.8$ eV, $D_h \sim 1.5 \times 10^{-3}\ m^2\ s^{-1}$, $A^{**} = 110 \times 10^4\ A/m^2k^2$ and $L = 9\ \mu m$, the injection ratio is $\gamma \sim 10^{-3}$. Therefore we may assume that minority carrier injection is low for an ordinary Au-nSi Schottky diode[21].

(b) Generation and Recombination of Carriers [22,23]:

If there is a uniform spatial distribution of trapping centres with life-time τ_t situated at the middle of the energy gap, additional current arises due to recombination under forward bias

given by $J_r = qn_i\ell[\ \exp(\beta V/2) - 1\ ]/\tau_t$ and generation current under reverse bias given by $J_g = qn_i\ell/2\tau_t$ where ℓ is the width of the space charge region.

(c) Tunnelling through the Space Charge Region[24-27]:

Tunnelling can take place if the barrier thickness is less than about 1.5 nm. Therefore this effect is serious only for highly doped ($>10^{24}$ m^{-3}) semiconductors and/or under high reverse bias conditions. For such a degenerate semiconductor, the I-V relationship for both forward and reverse bias voltage $|V|$ is given by $J = J_s \exp(|V|/E_o)$ where J_s depends only very slightly upon $|V|$ and E_o is a constant. Both J_o and E_o are different for different bias directions.

(d) Interfacial (Oxide) Layer:

A practical Schottky diode will inevitably have an oxide layer at the interface. This layer is usually so thin that electrons are able to tunnel through it quite easily. Assuming that there are no charged states present in this interfacial layer, the electric field in it and the voltage V_i dropped across it are given by eqns. (2.3) and (2.4) where F_s is equal to the maximum field F_m at the semiconductor surface. The change in barrier height $\Delta\phi$ is

equal to the change in V_i. Since $F_m \alpha (V_{bi}-V_a-\Delta\phi)^{\frac{1}{2}}$ from eqn. (2.24) and $\Delta\phi << (V_{bi}-V_a)$, we then have $\Delta\phi\alpha \ (V_{bi}-V_a)^{\frac{1}{2}}$, i.e. $\Delta\phi\alpha \ F_m$. But if there is a space charge density ρ per unit area in the oxide at distance x from the semiconductor surface, this is equivalent to a charge Q_s reflected on the semiconductor surface given by $Q_s = \rho(t-x)/t$ where t is the oxide thickness. As a result Q_s must be added to eqns. (2.3) and (2.4) to obtain the potential dropped across the oxide layer. If Q_s is independent of the bias voltage, then the change in barrier height is still given by $\Delta\phi\alpha \ (V_{bi}-V_a)^{\frac{1}{2}}$.

(e) Edge Effect:

If the surface area surrounding the metal contact remains neutral, then one may assume that the energy bands of the semiconductor remain flat at this surface region. The result of a depletion region underneath the metal plate and a flat band region surrounding it is that a steep potential gradient (i.e. high field region) is developed at the edges (Fig. 2.9a). Consequently the barrier height lowering and tunnelling effects become severe, leading to a high concentration of current at the edge. This may also account for a soft reverse characteristic. This effect is reduced if the surrounding area is depleted due to surface charges (Fig. 2.9b).

The converse is true if it is accumulating. The effect can also be minimised by using a guard ring (Fig. 2.9c) or a diffused p-type region (Fig. 2.9d) around the metal plate[23].

2.5.4 C-V Characteristics

The capacitance of a semiconductor junction is usually measured by superimposing a small ac signal voltage on the dc bias. A capacitance bridge may be used for this purpose.

When the bias voltage across a Schottky barrier changes, the net space charge also changes accordingly. This change of charges with voltage gives rise to a capacitance as given by eqn. (2.16). If free carriers in the space charge region can be neglected at the bias range of interest, then the charges are due solely to the un-neutralised net donors. The relevant equations related to such depleted region are given in section 2.3.3 with $V_d = V_{bi} - V$, where V is the bias voltage, V_{bi} is the contact potential and V_d is the total depletion voltage of the space charge region. From eqn. (2.21) we have

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_o\varepsilon_s N} \left(V_{bi} - V - \frac{kT}{q}\right) \qquad (2.48)$$

Therefore a plot of C^{-2} against V would give a straight line. From the gradient, the doping density N can be calculated. The intercept of the line on the V axis

gives (V_{bi} - kT/q). Thus the barrier height $V_{bo} = V_{bi} + V_n$ can also be obtained.

There are various factors which may cause departures from such simple straight line plots. Many of these have been discussed by Goodman[28]. The complications due to deep level traps in the band gap can be very serious[7,29-31]. Deviations may also occur if inversion takes place at the metal-semiconductor interface[32]. However if this does not take place at zero bias, then no minority carriers would accumulate at the interface even under high reverse bias since their quasi-Fermi level remains horizontal at that region and coincides with that of the metal[20]. Under high forward bias, the effect due to the majority carriers may also have to be considered.

2.6 SUMMARY

To sum up this chapter, we have shown that the space charge region of a semiconductor surface is formed as a result of some external charges which induce an electric field on the surface. Under thermal equilibrium condition, if the surface potential set up by this field is known, then the space charge region is completely defined, provided all physical constants such as doping density and dielectric constant are known. Thus, knowing the surface potential, one can calculate its depletion width, space charge capacitance, space charge density, potential distribution, etc. and vice versa. In a MIS structure, this fact is used to deduce the surface potential V_s from the measured capacitance of the structure. Since V_s can be changed readily by an externally applied voltage V, this effectively means that the Fermi level at the interface can be scanned across the energy position. By comparing the experimentally obtained V_s vs V plot with that of a theoretically calculated ideal model, the discrepancy may be treated as due to interface charges. This therefore makes the MIS C-V technique a very powerful tool in semiconductor surface characterisation.

For the case of metal-semiconductor contact, the conduction current flowing across such a barrier encounters two obstacles. One is the scattering process in the space charge region while the other is the emission process at the interface. Many deviations from ideality may occur, and these are mainly due to non-intimate contact and the high electric field involved in the region.

However, in most cases, the forward current density generally obeys the well known diode equation

$$J = J_o[\exp(\frac{qV}{\eta kT}) - 1] \qquad (2.49)$$

where J_o is the saturation current density. η is called an ideality factor with value ranging from 1 to 2. For an ideal diode, $\eta = 1$. But for a technically good diode, other effects usually cause deviations to give $\eta \sim 1.1$. When the conduction is limited by recombination process in the space charge region, η can be as high as 2.

The reverse current is usually much more difficult to analyse. This is mainly due to the high electric field at the imperfect interface, resulting in severe side effects such as tunnelling and barrier height lowering. Therefore it is usually extremely difficult to pin-point unambigiously the true mechanism responsible for the deviations from a perfectly saturated current.

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CHAPTER 3

CERMET CONDUCTIONS

3.1 INTRODUCTION

A cermet is a material composed of a matrix of metal embedded in an insulator. The fraction of metal may vary from zero to unity so that a large range of resistivity may be obtained. In this chapter, we are concerned primarily with samples in the dielectric regime, i.e. cermets with a low metal fraction and which show a negative temperature coefficient of resistance. Their conduction mechanisms have not yet been understood satisfactorily but they show many conduction properties similar to those of amorphous insulators. Therefore we begin the chapter with a brief outline of the conduction processes in amorphous materials. We then proceed to discuss the effects of an amorphous material with high defect density being used as the insulator in a MIS device. This is necessary because the configuration of the specimens used in the project is similar to that of the conventional MIS structure with the insulator being replaced by one with metal inclusions. Next a brief description of the structures of some cermet samples prepared under different environments is given. The conduction mechanisms, as proposed by some authors, are then outlined. The chapter ends with a discussion of a very simple conduction band model which can be used to describe the ac and dc conductance of the cermet. We do not distinguish cermets and discontinuous metal thin films

in the general treatment. This is not because there is no differences between them, but because some of their properties are similarly affected by the same factors. For example, whether or not their conduction processes are assisted by the dielectric/substrate medium would depend on the nature of these materials; the distribution of the metal particles may also have a profound and qualitatively similar effect on the characteristics observed on both types of samples.

3.2 AMORPHOUS INSULATOR

The fact that an amorphous material retains many of the physical and chemical properties of the crystalline state indicates that their microscopic structures must bear a lot of similarities. These similarities include the short-range atomic order, the angle between bonds and the binding forces. When describing the conduction processes of a cystalline material, one of the most important parameters one would require is the density of states (DOS). It is therefore of interest to enquire whether the idea of DOS is still applicable to amorphous materials or otherwise. Many calculations and experiments have ascertained that the form of the DOS indeed does not differ greatly from the corresponding form in crystalline structure. In the case of amorphous insulator and semiconductor, it is still possible to identify a conduction band and a valence band, except that finer features may be smeared out from the band tails into the forbidden energy range. These band tails are due to the lack of long-range atomic order. The main and very important difference between these band tail states and those in the original band is that, although both are continuous in energy, the latter is extended in that an electron here is shared throughout the whole material, i.e. it has a running wave function. The states in the tails are localised; i.e. the probability density decreases exponentially with distance from the centre of localisation for a sufficiently large distance. Mott interprets this as the vanishing of

dc conductivity at T = 0[1]. The carrier mobility also drops sharply from the extended states across to the localised states[2].

The band model for an amorphous insulator proposed by Cohen et al.[3] (CFO) is shown in Fig. 3.1. E_c and E_v mark the separation of localised states from the extended states in the conduction and valence bands respectively. The tails of these states overlap near the centre of the gap so that electrons at the top of the valence band tail fall into the lower states of the conduction band tail. The Fermi level is pinned in the region of overlap. Davis and Mott[4] modify this to the form shown in Fig. 3.2. The localised states between E_c and E_A (also E_v and E_B) are due to long range disorder. A fairly narrow band of localised states is also assumed to exist near the centre of the gap. These have sufficiently high DOS so as to effectively pin the Fermi level over a wide temperature range. The origin of these states is presumably due to some specific defects of the material, e.g. dangling bonds, and impurities. The general conclusion of the two models is therefore that there is a fairly high DOS at the Fermi energy level, of the order of 10^{25} m^{-3} eV^{-1}. This is the reason that blocking (Schottky) barriers are not observed in metal/a-semiconductor contacts[5].

The conduction processes of such a system have been discussed by Mott and Davis[6]. Here, we would just point out the three distinct conduction paths that the

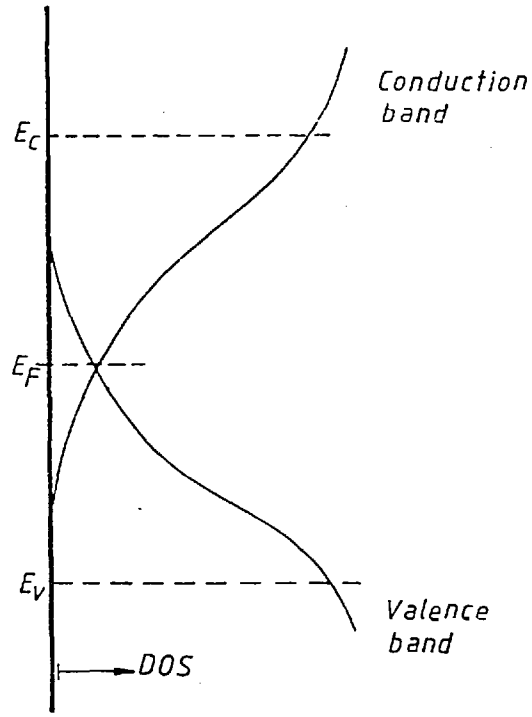

Fig. 3·1

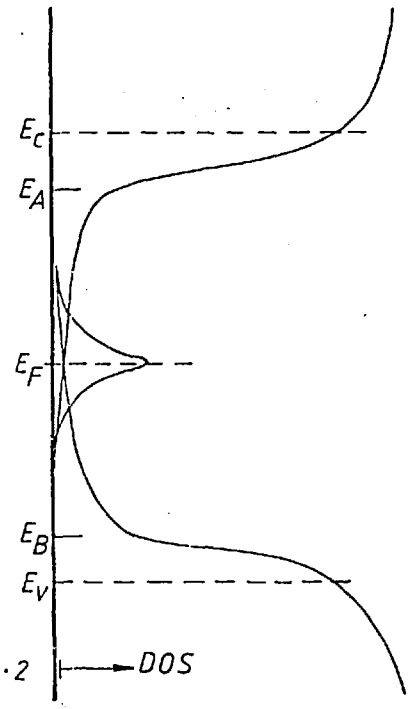

Fig. 3·2

The energy band diagrams of amorphous insulators proposed by (Fig. 3·1) Cohen, Fritzche and Ovshinsky, (Fig. 3·2) Mott and Davis.

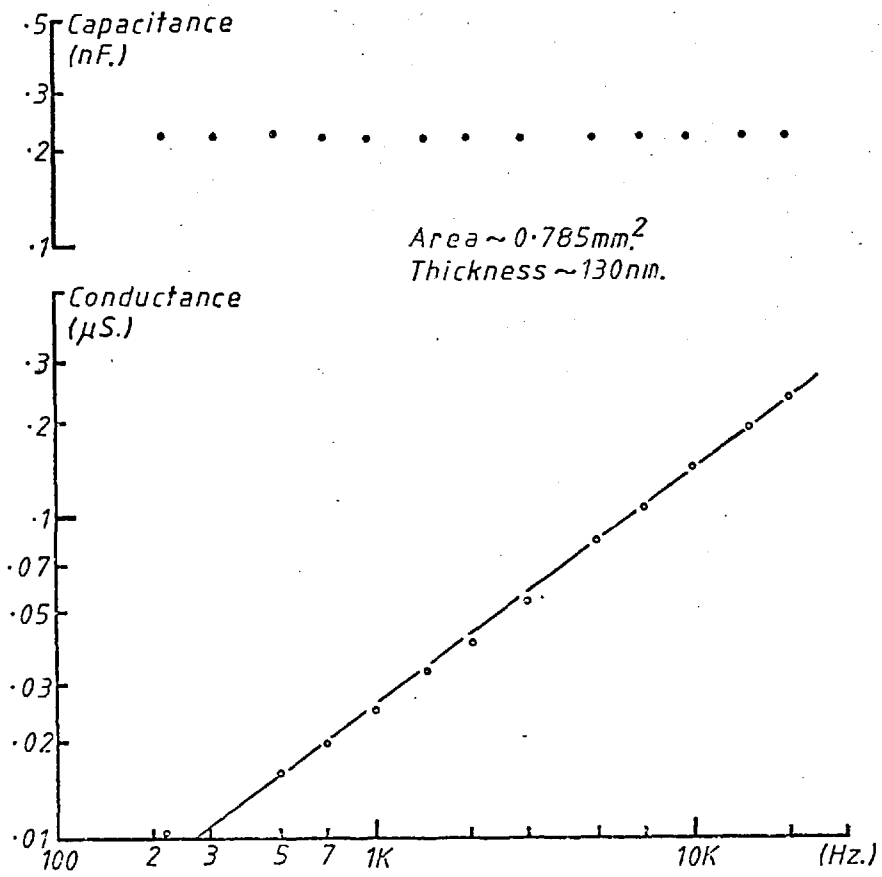

Fig. 3·3 A.C. capacitance and conductance of a R.F. sputtered SiO_2 film.

carriers may move:

(a) Electrons excited to E_c or holes to E_v. The conductivity is given by

$$\sigma = \sigma_o \exp\left(-\frac{E_c - E_F}{kT}\right) \qquad (3.1)$$

with $\sigma_o = qN(E_c)\, kT\, \mu_o \sim 3 \times 10^4\ (\Omega m)^{-1}$ and $\mu_o \sim 0.001 - 0.005\ m^2/Vs$.

(b) Electrons excited to E_A or holes to E_B. Since the states here are localised, carrier motion is possible only through phonon assisted hopping. The conductivity is

$$\sigma = \sigma_1 \exp\left(-\frac{E_A - E_F + \Delta W_1}{kT}\right) \qquad (3.2)$$

where ΔW_1 is the hopping energy, $\Delta W_1 << \Delta E_c$, and also $\sigma_1/\sigma_o \sim 1/1000$.

(c) Conduction due to hopping of electrons with energies near the Fermi level E_F. The conductivity is

$$\sigma = \sigma_2 \exp\left(-\frac{\Delta W_2}{kT}\right) \qquad (3.3)$$

where $\sigma_2 << \sigma_1$ and W_2 is about half the width of the defect band. At low temperature, there are more electrons tunnelling to a farther site which has a lower ΔW_2 than hopping to a nearest neighbour. By optimising the tunnelling term, $\exp(-2\alpha R)$, and the activated energy term, $\exp(-\Delta W_2/kT)$, an optimum distance R_o (radius of a spherical

shell) is obtained such that

$$\sigma \propto \exp(B/T^{\frac{1}{4}}) \qquad (3.4)$$

where B is a constant. This is Mott's model of variable range hopping.

The total conductivity of such a system is the sum of all these mechanisms. As a result, a plot of log σ vs. $^{1}/T$ may not be a straight line. But if the band edges are abrupt, different conduction processes may dominate at different temperature range giving straight line plot with abrupt change of slopes at the corresponding temperature range. For the case of a wide gap insulator like SiO_2 at normal temperatures, there is a negligible number of darriers excited into the states around the mobility edges. Therefore conduction would be mainly due to electrons hopping near the Fermi level.

Turning our attention to the ac conductivity, as mentioned above, the conduction process is mainly due to electrons hopping in localised states around the Fermi level. This will be briefly described as follows. A pair of sites with an electron jumping between them induced by an externally applied ac field is like a rotating dipole. Because of the finite probability of tunnelling from one site to the other, there is a time constant τ associated with it. Therefore a time lag is incurred between the rotating dipole and the applied ac field. This gives rise to a conductive current. Since there is a vast number of pairs of such centres, each with

its own characteristic time τ, the observed conductivity $\sigma(w)$ is integrated over all values of τ[7]. The result is that

$$\sigma(w) = \frac{1}{3}\,\pi q^2\, kT\, [N(E_F)]^2\, \alpha^{-5}\, w\left[\ell n(\tfrac{\nu}{w})\right]^4 \qquad (3.5)$$

where α^{-1} is the decay distance of the wave function, $\nu = \nu_{ph} \sim 10^{12}$ Hz is the phonon frequency, and w is the angular frequency of the applied field. The term $\ell n(\nu/w)$ varies slowly with w. In fact, it can be shown easily that $\sigma(w) \alpha w^n$ where n varies between 0.85 and 0.7 as the frequency changes between 10 Hz and 1MHz respectively.

3.3 INSULATOR EFFECTS ON MIS DEVICES

The insulator in a MIS system is usually amorphous. This is true for most methods of insulator preparation, e.g. oxidation, evaporation or sputtering deposition. Therefore, according to the model of Mott and Davis, the Fermi level would be pinned at a localised defect band. At the interfaces with the metal and the semiconductor, two insulator space charge regions are formed. Their thicknesses are very thin ($\sim$5 nm) because of the high defect DOS. In the analysis of MIS C-V characteristics, it is generally assumed that the voltage drops linearly across the insulator. This is justifiable only if the insulator thickness is large compared with its space charge regions, and that neutrality is preserved within the insulator bulk. The insulator space charge regions can then be treated as part of the interfacial layers. If it is assumed that the surface of the insulator has the same defect DOS as that in the bulk, which has about 10^{25} m^{-3} eV^{-1}, then this is equivalent to a surface density N_{ss} of about 5×10^{16} m^{-2} eV^{-1}. From the discussions in Section 2.4 it was shown that this value is high enough to effectively screen off the semiconductor space charge region. Therefore in order to have an operational MIS device, a much better interface has to be obtained. This can be achieved by reducing the number of dangling bonds at the interface with suitable choice of crystal faces to minimise lattice mismatch, (e.g. for silicon,

the (100) planes produces the least interface states with SiO_2) and by reducing strained regions in the insulator by optimizing insulator growth or deposition conditions, avoiding impurities and post-baking, etc.

It is seen that, as far as changing the surface potential of the semiconductor space charge with an externally applied voltage is concerned, what matters most is the interfacial states. The presence of high defect densities in the insulator bulk is relatively immaterial because of their poor communication with the outside world. Although these defect centres may trap a net charge,(say, during device fabrication) but the probability for them to be neutralised or altered by capturing the mobile carriers in the conduction or valence bands is very small because of the low carrier densities in the insulator. Charge interchange with the metal or semiconductor electrodes by tunnelling is negligible and confined to a very thin region, i.e. the interfacial layer, only. However, the presence of fixed charges in the insulator would shift the characteristics along the voltage axis (e.g. change the threshold voltage) which of course is undesirable.

Another serious effect is the presence of mobile (ionic) charges in the insulator. Since charges at different positions in the insulator reflect different amounts of charge on the semiconductor surface, the characteristics would change under different bias conditions.

It is also usually assumed in the literature that the insulator is a good one, i.e. one whose capacitance is independent of bias and frequency, and with zero conductance. The former assumption is probably easier to satisfy for most reasonably pure insulators. But an insulator with zero or negligible conductivity may not be so realistic especially at high frequency. This is because the hopping process between localised states near the Fermi level would give rise to an ac conductivity given by eqn. (3.5). In order to demonstrate this point, a sample with the configuration $Au/SiO_2/A\ell$ was prepared. The $A\ell$ electrode was evaporated onto a glass slide. The SiO_2, about 130 nm thick, was prepared by sputtering, and so was the Au counter electrode. Plots of capacitance and conductance vs. frequency are shown in Fig. 3.3. As was expected, a straight line plot of log $\sigma(w)$ vs. log w was obtained which gave $\sigma(w) \alpha w^{0.75}$. From eqn. (3.5) the DOS, $N(E_F)$, at the Fermi level may be estimated. Using $\alpha^{-1} = .8$ nm, $\nu_{ph} = 2\pi \times 10^{12}$ rad. s^{-1} and at $w = 2\pi \times 10^4$ Hz, $N(E_F)$ was found to be about 1.5×10^{24} m^{-3} eV^{-1}. This is a reasonable value for a wide mobility gap insulator[4]. Now, the conductance is given by $G = \sigma/t$ (per unit area) for a sample of thickness t. The reactance of the geometrical capacitance is $wc = w\varepsilon_o\varepsilon_i/t$. So the ratio is $G/wc = \sigma(w)/w\varepsilon_o\varepsilon_i \sim kT \left[N(E_F)\right]^2 \alpha^{-5} \left[\ell n(\nu/w)\right]^4/\varepsilon_o\varepsilon_i$. The q^2 term is omitted since we would express $N(E_F)$ in m^{-3} eV^{-1}. Using the criterion that the conductance is negligible if G/wc is less than 0.1, then this requires that $N(E_F) < 4 \times 10^{24}$ m^{-3} eV^{-1} for $w \sim 2\pi \times 10^3$ s^{-1}. Thus the sputtered SiO_2 might just satisfy the requirement.

3.4 CERMETS AND DISCONTINUOUS METAL FILMS

3.4.1 Structures

Discontinuous metal films are very thin metal films ($\lesssim$ 10 nm) deposited on smooth substrates. These films consist of individual metal nuclei (islands) with radii of the order of 1 to 10 nm. The islands appear to be distributed randomly. If more metal atoms are added, the islands grow until they coalesce with one another to form continuous films. Cermets are produced by co-sputtering[8], co-evaporation, plasma spray, etc. of a metal and an insulator material. The sizes of the granular metal particles depend on the deposition conditions and on the nature of each component. In general, for low metal fraction ($\lesssim$ 40%), the metal islands are restricted in their growth by the presence of the insulating material, and hence are prevented from touching one another even as the deposited film grows very thick. Some electron micrographs of Au-SiO_2 cermets with various metal fractions are shown in Fig. 3.4. These samples were obtained by sputtering the cermets onto carbon films held on electron microscope copper grids. The cermet thicknesses were about 20 nm. Three distinctive regions are clearly visible. These consisted of the dark circular patches which are believed to be corresponding to the gold islands; surrounding these were the grey labyrinth which might be the SiO_2 because, having a lower electron scattering factor, it was expected to produce a grey tone image compared with that of the gold; the white areas which showed no detailed

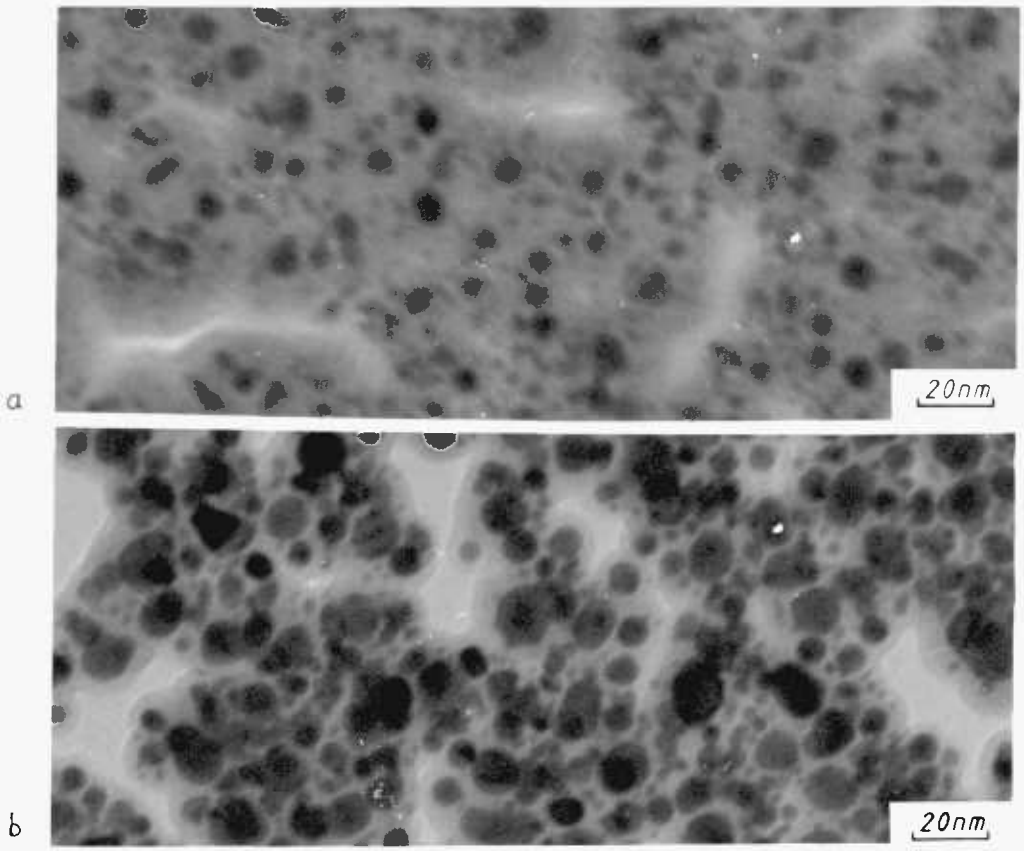

Fig. 3·4 Electron micrographs (X500,000) of cermet films deposited onto heated substrates, thickness ~ 20nm

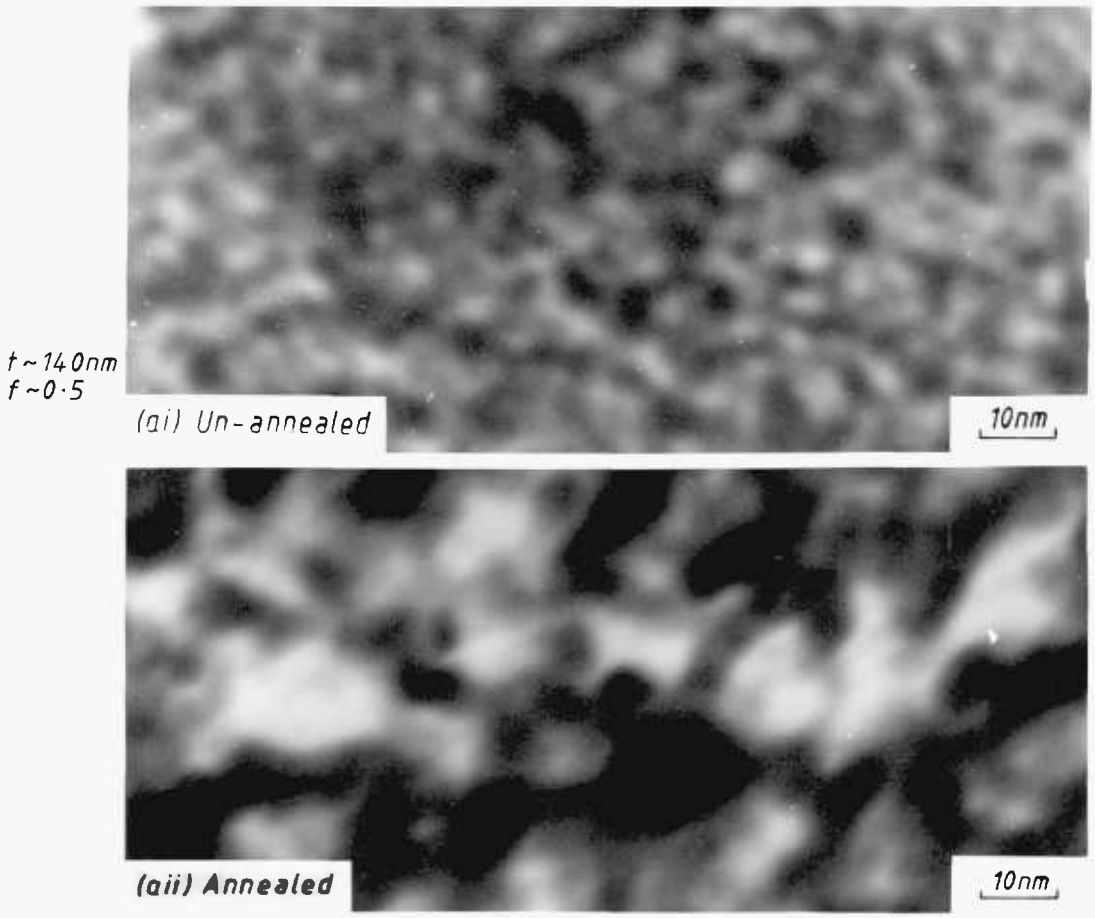

Fig. 3·5 Electron micrographs (X1,000,000) of cermet films deposited onto cool substrates. [Thickness = t, Metal fraction = f]

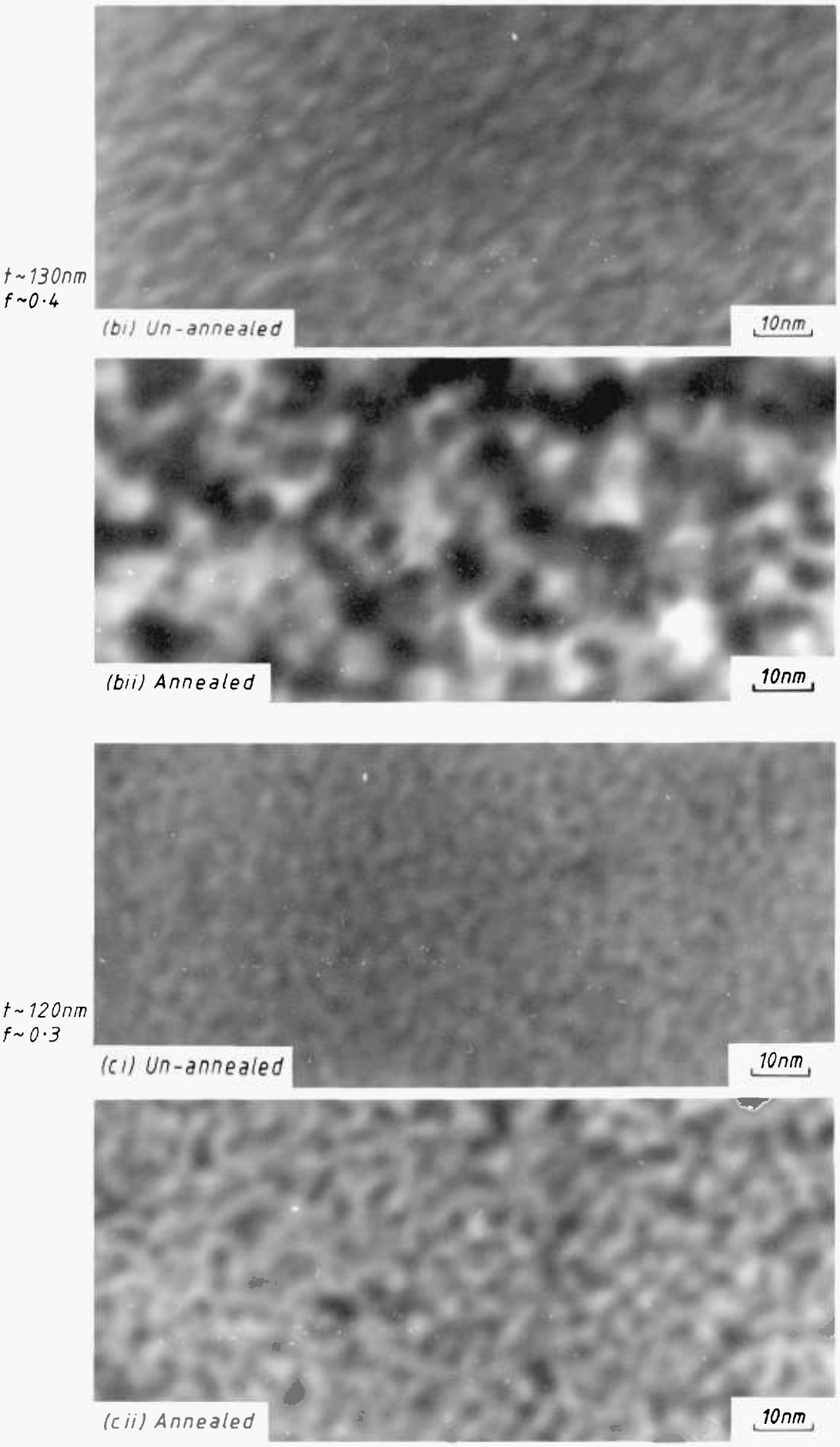

Fig. 3·5 Electron micrographs (X1,000,000) of cermet films deposited onto cool substrates. [Thickness = t, Metal fraction = f]

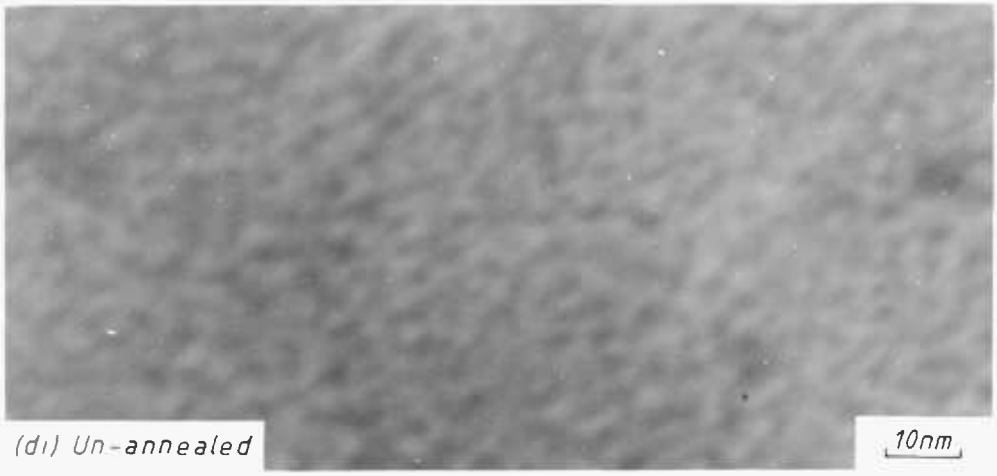

Fig. 3·5 Electron micrographs (X1,000,000) of cermet films deposited onto cool substrates. [Thickness = t, Metal fraction = f]

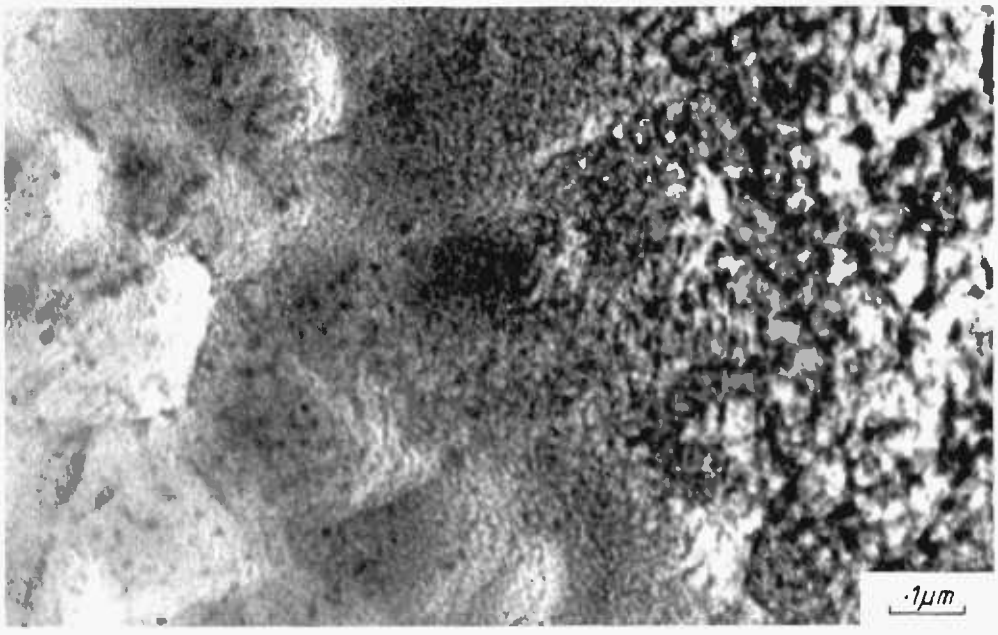

Fig. 3·6 Electron micrograph (X100,000) of a cermet showing the effect of annealing by electron beam.

features in them were probably just empty spaces. On some samples (Fig. 3.4b) the sizes of the gold islands may be differentiated into two groups, in one the diameter is about 10 nm and in the other about 2 nm. These are similar to the sample produced by Tick et al.[9]. Another batch of samples was prepared by sputtering the cermets onto aluminium coated glass slides placed on a water cooled substrate table. These samples were more than 100 nm thick. They were lifted out of the glass slides by dissolving away the Aℓ underlay with sodium hydroxide solution. High magnification (10^6 times) electron micrographs obtained with an 1 MeV electron microscope are shown in Fig. 3.5. Also shown are sample areas which have been annealed by the electron beam. Examinations of the un-annealed samples show large differences from those of Fig. 3.4. Firstly, the metal islands are no longer clearly distinguishable. Instead, there are mottled dark spots which look like high concentrations of metal atoms, and have low contrast with the surrounding SiO_2. This may indicate that there are no abrupt transitional boundaries between the gold and SiO_2 phases. But it is more likely to be due to the limit of resolution of the microscope and multiple scattering as the electron beam passed through the thick samples. Referring especially to Fig. 3.5c which shows the least astigmatism effect, many of the dark mottled spots can be clearly distinguished from their surroundings. If it is assumed that each of these was the projection image of a gold island from the bulk of

the cermet 100 nm thick onto the plane, an estimate shows that there were about 500 to 1000 islands projected over an area of $(100\ nm)^2$ ($(100\ mm)^2$ on the micrographs). Taking the upper limit, then there were about 1000 islands in a volume of $(100\ nm)^3 = 10^{-21}\ m^3$, i.e. 10^{24} islands m^{-3}. Each island has a diameter of 2 to 3 nm giving a volume of about $2 \times 10^{-26}\ m^3$. Hence the total volume of gold islands was about $2 \times 10^{-2}\ m^3$ in every meter cube of the sample. Therefore there were just about 2% volume of gold shown out as islands, compared with about 20% estimated by microprobe analysis discussed in chapter 4. This was the same as the conclusion arrived at by Devenyi et al.[30], i.e. only about 10% of the metal actually formed metal islands. Furthermore, the islands were also much smaller than those shown in Fig. 3.4. This is because in those samples, the carbon films held on the microscope grids were thermally insulated so that the heat generated during cermet deposition gave rise to very high temperature. The gold atoms were therefore very mobile and, since the deposited cermets were thin and discontinuous, surface migration could still occur even after the deposition process had stopped, resulting in the formation of large spherical islands. The effects of annealing by the electron beam were also clearly demonstrated in Fig. 3.5. Larger gold islands were formed by the coalescence of smaller islands. The recrystallisation process might be similar to that described by Lomniczy et al.[10] where agglomeration of Au occurred on the surface of the sample.

The micrograph (Fig. 3.6) showing the annealed and un-annealed areas also review the bubbling-like appearance of the samples. Most of them were circular but a very few were triangular in shape. Their sizes range from about 100 to 500 nm. Micrographs obtained with the sample tilted at different angles showed that a triangular 'bubble' of side length 200 nm was about 250 nm high. Their origin is not clear, but the high shadowing effect may indicate that they were due to the surface irregularities of the Aℓ underlay so that preferential accumulations of gold occurred on the face of the irregularities facing the Au target. They might also be due to the force exerted by the gas bubbles when the Aℓ was being dissolved away in the NaOH solution, resulting in a buckled cermet film.

3.4.2 Conduction Mechanisms

For large metal fractions, most of the metal islands are touching one another to form continuous paths so that the conduction properties are metallic. As the metal fraction is reduced, the paths become fewer and thinner and meander longer distances before connecting the electrodes. The surface scattering also becomes important. The resistivity of the cermet therefore increases and the temperature coefficient of resistance (TCR), although still positive, decreases. Further reduction in metal fraction would lead to an eventual breaking up of the continuous paths to form

isolated metal islands. The transport of electrons from one island to another would then have to go through the dielectric separating them. It is therefore expected that the cermet would exhibit many properties similar to those of dielectrics, notably high resistivity and negative TCR. At the transition regime both the metallic and dielectric processes are going on together, but one may dominate over the other at certain temperature ranges. As a result, a transition temperature T_c may occur below which the TCR is negative (dielectric limited) and above which the TCR changes to positive (metallic limited). Therefore if a cermet resistor is designed with a correct composition to give T_c at the working temperature range, a very small TCR resistor is obtained.

In the discussions below, we deal only with conductions in the dielectric regime. A common feature of this type of films is that an activation energy of between 0.01 to 0.2 eV is observed. Various models have been proposed to account for their conduction properties. Most of these are based on the idea of activated charge carrier creation and tunnelling[8,9,11-14]. This was first suggested by Neugabaur and Webb[11] to explain the activation energy observed. Their model is as follows. In order to remove an electron from a neutral island, a charging energy $E = q^2/C$ where C is the capacitance of the island is required. For a spherical island of radius r, this energy is given by $q^2/4\pi\varepsilon_o\varepsilon_i r$ where ε_i is the dielectric constant of the surrounding medium. For a

system with N such islands uniformly distributed, the number of negatively charged islands at thermal equilibrium is given by $n = \frac{1}{2} N \exp(-E/2\ kT)$ provided $E > 3\ kT$. It is considered that this is the number of carriers available for carrying the current. The electrons of the charged islands move to neighbouring neutral islands by tunnelling. The mobility μ is therefore proportional to $\exp(-2\alpha s)$ where s is the island separation and α describes the decay distance of the wave-function from the island. Under an applied electric field, there is a net electron movement in the field direction giving rise to a current. The conductivity σ is proportional to $n\mu$. Thus,

$$\sigma \alpha \quad \exp(-2\alpha s - \frac{E}{kT}) \qquad (3.6)$$

By plotting $\log \sigma$ vs $^{1}/T$, several authors found that the activation energy obtained from the slope agrees with the calculated value when an average r as determined from micrographs of the sample is used. When the applied electric field between the islands is high, the potential encountered by an emitting electron is lowered by the Poole-Frenkel effect. This results in a reduction of the activation energy by an amount proportional to $F^{\frac{1}{2}}$ where F is the applied electric field. Hence, the conductivity is given by $\sigma \alpha \exp(\beta_p V^{\frac{1}{2}})$ where β_p is a constant and V the applied voltage. Qualitative agreement with this expression (Fig. 3.7) is found for Au-SiO_2 samples made by the author.

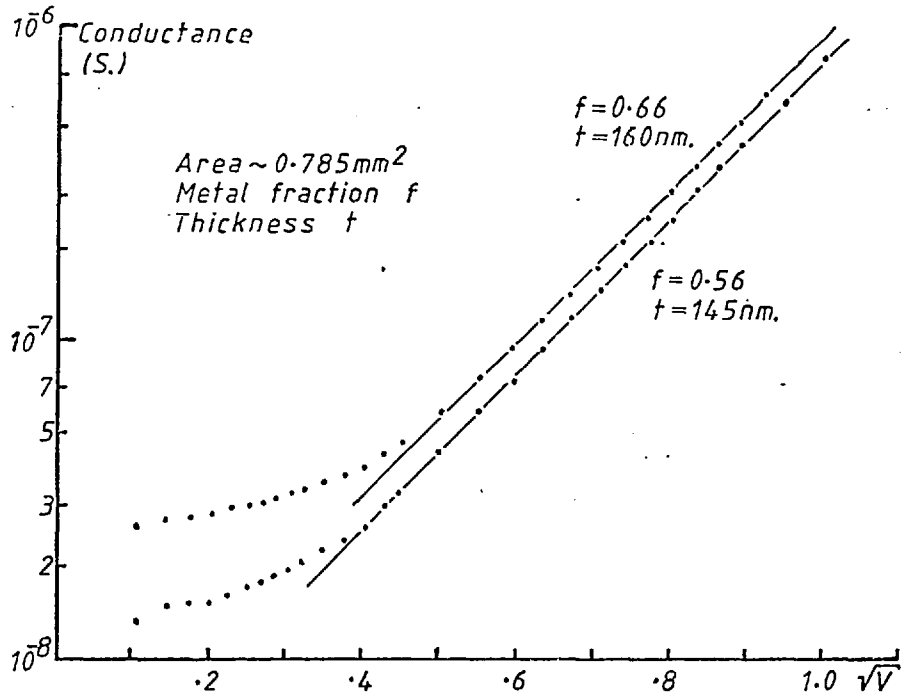

Fig. 3·7 Poole Frenkel type conduction of $Au-SiO_2$ cermet films.

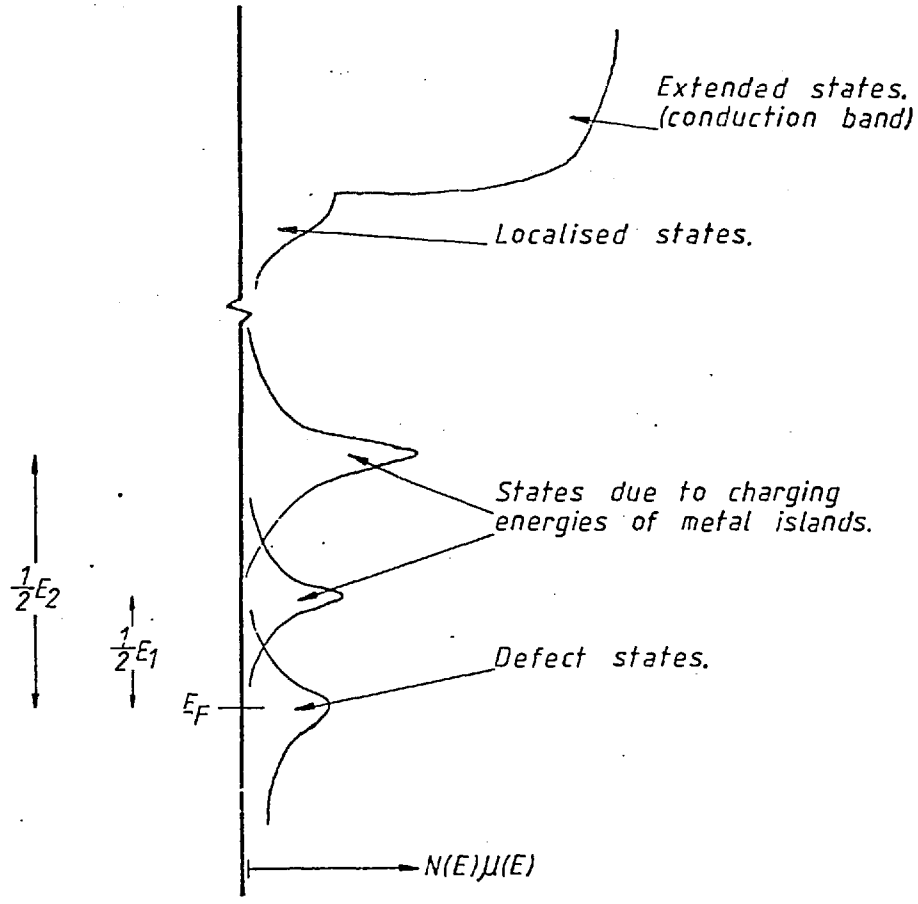

Fig. 3·8 Simple N(E)μ(E) diagram for a cermet film.

There are others who found that the Arrhenius plot does not always produce a unique activation energy. Instead, many found that log σ is proportional to $T^{-\frac{1}{2}(15-20)}$. This was explained by Abeles et al.[19] as due to the fact that the island sizes and separations, and hence their charging energy E, are not constant. Therefore a distributed E is expected. Their model is as follows. The cermet is imagined to be made up of elementary volumes of about $(10\ nm)^3$ and it is assumed that the metal island size in each volume is uniform but varies from one volume to another, and that all volumes contain equal metal fractions. This implies that the island separations s are proportional to their sizes r. Since $E \alpha {}^{1}/r$, they argued that sE = constant. Now, regions of small r have higher E so that electrons tend to go through regions with larger r. But these correspond to regions of large separations s which have low tunnelling probabilities. Therefore electron motion is mainly confined to optimum paths, the percolation paths. Putting sE = constant into eqn. (3.6), the total conductance σ can be found by integrating over all possible percolation paths. The result is that $\sigma \alpha \exp(-As_m)$ where A is a constant and s_m is the value of s when the exponent of eqn. (3.6) has a maximum value. Thus it is found that $\sigma \alpha \exp(-A/T^{\frac{1}{2}})$. At high field, thermal equilibrium no longer exists; carriers are being generated by the applied field. If the energy to remove an electron from

a neutral island and put it on a neutral neighbour distance s away is E, and if the field between the islands is ΔF, then electron transfer can occur (at T = 0) when $qs\Delta F \geq E$. Since the rate of tunnelling is proportional to $\exp(-2\alpha s)$, the carrier generation rate and hence the conductivity is proportional to $\exp(-F_o/\Delta F)$. But ΔF is proportional to the applied field, F, therefore $\sigma \alpha \exp(-F_o/F)$.

Some authors have attempted to evaluate a more accurate charging energy value by taking into account the effects of the surrounding islands and the non-spherical shapes of the islands[19,21]. The effective value of dielectric constant has also been considered since the tunnelling time of an electron between two islands may be shorter than the response time of the dielectric polarisation of the surrounding medium[22,23]. The quantisation effect of energy in small volume islands has also been discussed[24]. Furthermore, the tunnelling process may also be assisted by traps in the insulator[25-28].

3.5 DISCUSSION OF A SIMPLE CONDUCTION BAND MODEL FOR CERMETS

3.5.1 D.C. Conductivity

In considering the conduction processes of an amorphous insulator (a cermet with no metal) in section 3.2, it was pointed out that this is mainly due to phonon assisted hopping of carriers near the Fermi level. When a very small amount of metal is introduced into the insulator, the situation is similar to the doping of a semiconductor. The metal atoms are more likely to be randomly and individually distributed rather than coalesce to form metal islands. But most of these metal atoms are electrically inactive, i.e. they do not increase dramatically the free carrier densities of the amorphous material. However the presence of foreign atoms introduces additional strains and defects into the insulator. As a result, more localised states or traps are added into the mobility gap. This may modify the density of states near the Fermi level, but the overall picture of amorphous insulator conduction processes should be retained. As more metal atoms are added, islands would eventually be formed. We then have a 'conventional' cermet film, the low field conduction processes of which are widely accepted as due to activated charge carrier creation and tunnelling. When an electron leaves a neutral island to charge another one negatively, it leaves behind a positively charged island. So the energy is actually

shared between these two islands. This is similar to the process of carrier generation in semiconductors whereby an electron is excited to the conduction band and leaves behind a hole in the valence band. Therefore, in a limited sense, a cermet may be considered as having a narrow band gap of width E_1 equal to the charging energy of the islands of the order of .01-.2 eV. The Fermi level E_F is situated at the middle of the gap, with electrons occupying a region of localised 'conduction' band at an energy $\frac{1}{2}E_1$ above E_F and 'holes' at $\frac{1}{2}E_1$ below E_F. The motion of electrons is of course by tunnelling from one site (island) to the next rather than the running-wave like nature in crystalline solids. The energy spread of this 'conduction band' is of the order of the spread in island sizes (charging energies). The conduction paths of the carriers through this energy band, i.e. through the islands, may be considered to be in parallel with that through the defect states around the Fermi level. Whichever path would play a dominant role would depend on their respective number of carriers available and their mobilities as well as temperature and energy positions. Hence if conduction is through the charged islands, a constant activation energy may be observed. Otherwise, the log σ vs $^1/T$ plot would be a smooth curve; at low temperature variable range hopping of carriers around the Fermi level may dominate and a plot of log σ vs $T^{-\frac{1}{4}}$ (eqn. 3.4) would be a straight line. The situation with Abeles et al.[19]

is due to the fact that although conduction is through the metal islands, there is a finite spread in their sizes and hence their charging energies. Consequently the carriers would tend to tunnel to a state at about the same energy level. However, because of the effect of the finite physical sizes of the islands, the electrons are not able to jump to an island which is much farther than the nearest neighbours even though it may be energetically more favourable to do so. As a result, the jump is limited to a nearest neighbour and in an optimum direction. Thus the temperature dependent of the conductivity is a one-dimensional version of Mott's three-dimensional variable range hopping, i.e. $\log \sigma \propto T^{-\frac{1}{2}}$. If there are two (or more) distinct sets of island sizes with activation energies E_1 and E_2 fairly widely separated compared with their spread in energies Δ, then one may expect to see two regions of straight lines in an Arrhenius plot. This was observed by Tick and Francis[9]. The energy diagram may thus be drawn as shown in Fig. 3.8. Actually we have drawn the product of DOS and mobility against energy, i.e. $N(E)\mu(E)$ vs. E. This is closely related to the conductivity expression due to Kubo-Greenwood[29],

$$\sigma = -\int \sigma(E) \frac{\partial f}{\partial E} \, dE$$

$$= q \int N(E)\mu(E)f(E) \, dE$$

where f is a distribution function (the Fermi-Dirac function). From this equation, one sees that a constant slope Arrhenius plot, i.e. a unique activation energy, is obtained only if there is a sharp change (a high peak value) in the product $N(E)\mu(E)$ at E_1, say. This corresponds to identical island sizes and uniform separations. Otherwise, if the island sizes have a wide distribution, the energy width Δ is broadened and a plot of log σ vs $^1/T$ becomes a smooth curve. From an experimental plot, it is therefore possible to deduce a crude expression of $N(E)\mu(E)$ as a function of E, as was done by Devenyi et al.[30].

The result of increasing the metal fraction is to increase the island sizes and decrease their spacings. On the $N(E)\mu(E)$ vs E diagram, this correponds to lowering the peak towards the Fermi level and at the same time, the peak height is increased because of the exponential dependence of tunnelling probability $\mu \propto \exp(-2\alpha s)$. So one may expect a roughly exponential increase of conductivity against volume fraction. As the metal fraction is increased still further, delocalisation may occur so that the localised states become extended and metallic conduction sets in. Accompanying this is a change to positive temperature coefficient of resistance. It is of interest to note that many of the published data[8,18,19,31] show that this occurs at a conductivity of about 10^4 $(\Omega m)^{-1}$. This agrees with Mott's argument for a minimum metallic

conductivity which is the value of σ_o in eqn. (3.1)[32]. Another point to be noted is that the magnitude of the activation energy is of the same order as the spread in the defect states around the Fermi level, about 0.1 eV. Therefore there is a strong possibility that the transport processes between two metal islands are assisted by the states in the insulator.

3.5.2 A.C. Conductance

Another feature that is likely to become dominant in a system with an energy diagram as in Fig. 3.8, is the ac conductivity of the states around the Fermi level. At high frequency, the ac hopping process through these states may become important compared with the conductance between metal islands. This is because the jumping, induced by an external ac electric field, of an electron between a pair of neighbouring sites situated far away from any dc conduction (percolation) paths is similar to a rotating dipole, and hence may contribute to the ac conductance. Since there is a vast number of pairs of such centres, each with its own characteristic time constant, the observed conductivity-frequency ($\sigma(w)$ - w) relationship is given by eqn. (3.5). Thus a plot of log σ (w) vs log w would roughly be a straight line of slope about 0.8. This was observed by Tick et al.[9]. Similar plots for some Au-SiO_2 cermet samples used in this project are shown in Fig. 3.9. At high frequencies all the slopes approach to a gradient of about 0.8. Taking the plot of the sample with a metal fraction of 0.2

and using the same parameters as we have used in section 3.3 in eqn. (3.5), i.e. $\alpha^{-1} = 0.8$ nm, $\nu_{ph} = 2\pi \times 10^{12}$ rad/s and at $w = 2\pi \times 10^{4}$ Hz, $N(E_F)$ is estimated to be about 3.4×10^{24} m^{-3} eV^{-1}. This is slightly higher than the value obtained for the pure sputtered SiO_2 in that section. Hence it is consistent with our argument that the introduction of metals into the amorphous insulator creates a higher density of defect states. The deviation from linearity at lower frequencies is believed to be due to the presence of metal islands. Consider two such islands separated by a distance s. The jumping frequency of an electron between them can be written as[32]

$$\nu = \nu_o \exp(-2\alpha s) \qquad (3.7)$$

Therefore a time constant can be associated with it, whose value is $\tau \propto \exp(2\alpha s)$. Similar to the arguments with the defect states, this pair of islands need not be part of or even near to a dc conduction path. Their contribution to the ac conductivity is independent of such percolation paths, and is expected to follow the Debye equation $\sigma(w) \propto w^2\tau/(1 + w^2\tau^2)$. However, in general, there is a spread in the time constant for different island pairs due to the variations in their sizes and separations. So, the empirical formula for complex dielectric constant ε^* given by Cole and Cole[33] may be used. Thus, $\varepsilon^* = \varepsilon_\infty + (\varepsilon_s - \varepsilon_\infty)/(1 + (iw\tau_o)^\beta)$ where

τ_o and β are constants with β in the range between 0 and 1, and describes the spread in the time constants of the system. Using the general expression of $\varepsilon^* = \varepsilon' - i\varepsilon''$, the conductivity $\sigma(w)$ is given by

$$\sigma(w) = Aw\varepsilon'' = \frac{Aw(w\tau_o)^{\beta} \sin(\beta\pi/2)}{1 + (w\tau_o)^{2\beta} \sin^2(\beta\pi/2)} \qquad (3.8)$$

where A is constant.

A series of ac measurements were carried out on Pt-SiO_2 cermet samples by Mr. N.D. Moyo*. Three of the ac conductance results for increasing metal fractions are shown in Fig. 3.9. The metal fractions of these samples have not yet been determined, but it is certain that even sample (a) has a higher metal fraction than those of the Au-SiO_2 samples shown in the same figure. These plots show that the presence of dc conductance dominated the low frequency range. At intermediate frequencies, between 100 and 10^5 Hz, the role of ac hopping between metal islands becomes important. The transition frequency that this occurs increases with increasing metal fraction in accordance with eqn. (3.7). By summing the dc conductance and the ac conductance given in eqn. (3.8) the theoretical points are plotted for curve (a) in that figure. The parameters used are: dc conductance $= 2.35 \times 10^{-6}\ \Omega^{-1}$; $A = 1.0\,42 \times 10^{-8}\ \Omega^{-1}$, $\beta = 0.7$, $\tau_o = 4.692 \times 10^{-5}$ s. At still higher frequencies, the

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*Mr. N.D. Moyo is currently with the Electrical Engineering Department of Imperial College.

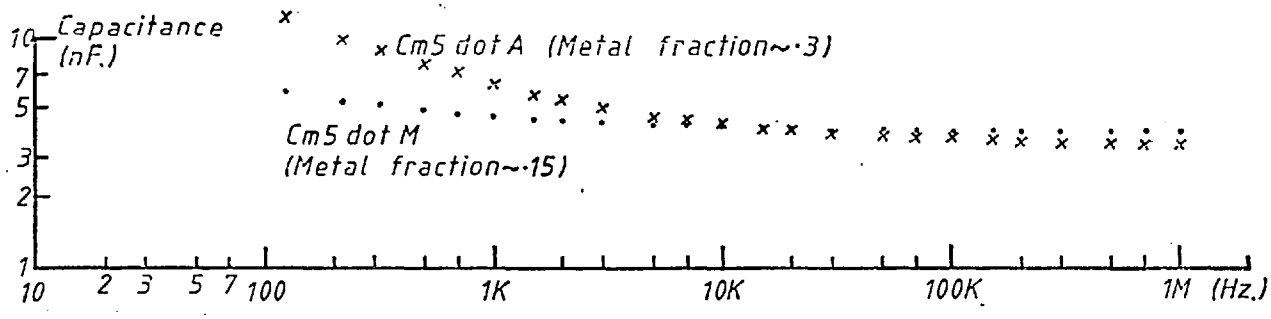

Fig. 3·9a AC capacitance of Au-SiO cermet films, thickness ~ 70nm.

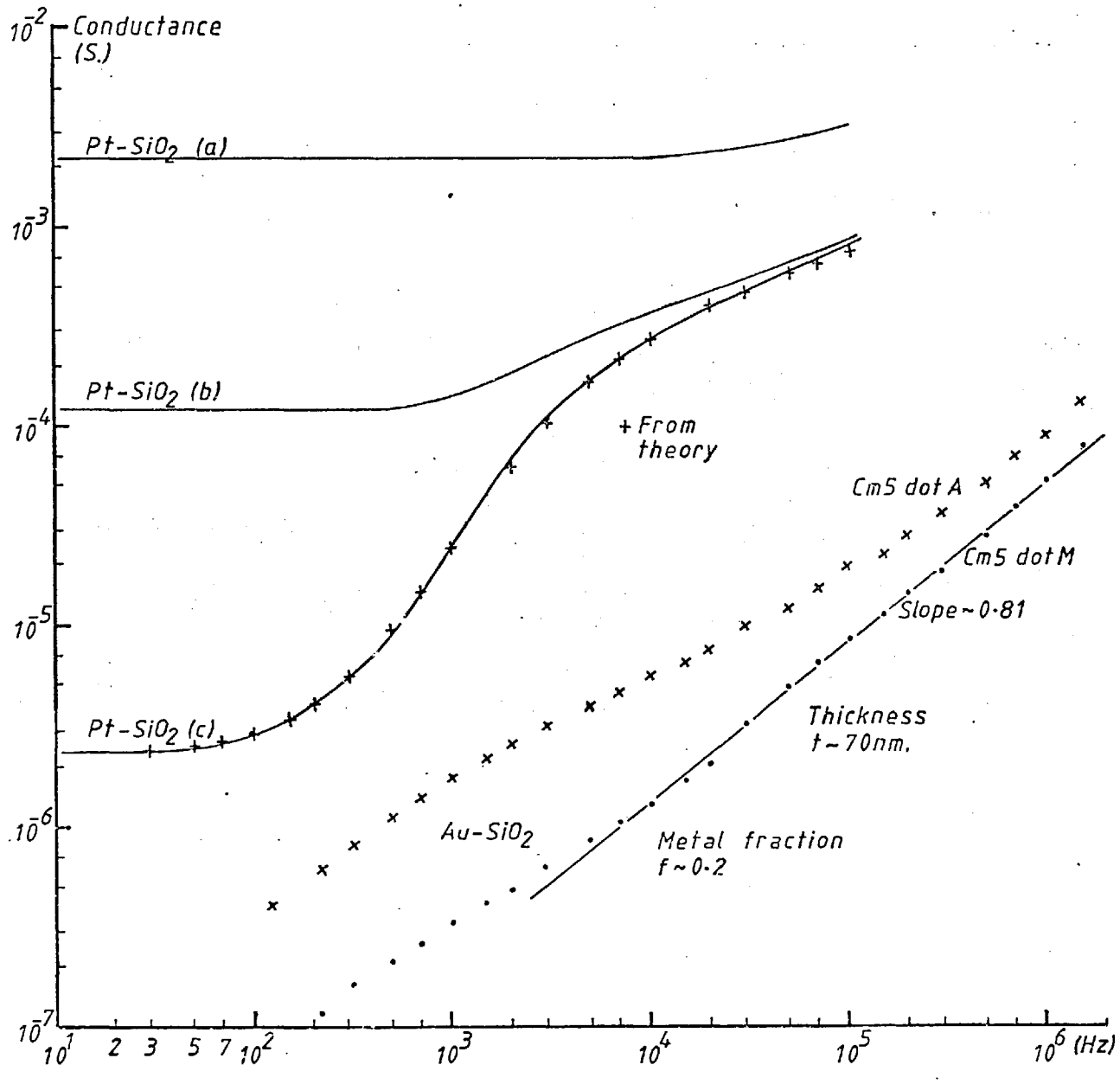

Fig. 3·9b AC conductance of cermet films. (a), (b), (c) are with decreasing metal fractions.

curves approached the expression of $\sigma(w) \quad \alpha w^{0.8}$ which is due to hopping between defect states around the Fermi level. These three processes, i.e. dc conduction through percolation paths, ac hopping between metal islands, and hopping between defect states, take place in parallel so that the total conductivity may be summed up in an equation

$$\sigma(w) = \sigma_o + \sigma_1 \frac{w(w\tau)^{\beta} \sin(\beta\pi/2)}{1 + (w\tau)^{2\beta} \sin(\beta\pi/2)} + \sigma_2 w^n$$

where w is the angular frequency of the applied electric field, $\sigma_o, \sigma_1, \sigma_2$ and τ are constants, β is a constant between 0 and 1, and n is about 0.8.

3.6 SUMMARY

The importance of producing a good insulator for a MIS device was recognised. Some sputtered SiO_2 insulator samples were examined experimentally in order to assess the suitability of as-sputtered SiO_2 for use as the insulating material of MIS devices. The results showed that the defect density of states near the Fermi level is about 1.5×10^{24} m^{-3} eV^{-1}. The ac conductivity, which was assumed to be due to these defect states, might have some effect on the performance of the device, but might not be too serious, provided that there was no dc leakage and the semiconductor behaved properly as a surface device. If this value of bulk defect density is continued up to the surface, then the surface state density is about 1.3×10^{16} m^{-2} eV^{-1} which again may be just low enough to allow some bending of the semiconductor space charge potential by an externally applied bias voltage. But this assumes that the surface states (or interface states) are solely due to the insulator defects only. In practice, the semiconductor surface itself would have been damaged by the sputtering process, and there is also plenty of foreign matter present there before depositing the insulator. These are likely to add many more states into the interface so that the situation may be much worse than originally envisaged.

For the case of cermet conduction, it was realised that no definite single model has been agreed by different

workers. This is not too surprising because samples prepared under different equipments can have very different structures. This was illustrated in the micrographs (Fig. 3.4 and Fig. 3.5) of two sets of cermet films prepared under different substrate conditions. The samples deposited with high substrate temperatures not only have larger islands but also have larger distribution in size. Cermets deposited onto cooler substrates have much more evenly distributed islands and uniform sizes. There is also the possibility of forming compounds like oxides or silicides between the metal and the constituents of the insulator if a reactive metal is used. All these factors contribute towards the difficulties of giving a universal model for cermet conduction. Furthermore, it is very likely that a large quantity of the metal atoms are embedded substitutionally or interstitially into the insulator material. In view of the nature of amorphous materials that a large amount of foreign materials may be incorporated into their structure without substantially altering their electrical characteristics, it is not surprising that cermets with low metal fractions show many similar characteristics as those of amorphous insulators. We therefore attempted to describe their conduction processes with an energy band diagram. This energy diagram is of course a very crude one and is also closely related to the actual structure of the cermet concerned, just as one for a semiconductor is closely

related to its own structure. But displaying the energy diagram of a system is a much clearer and more useful way than describing its structure for many practical and experimental purposes.

We also deduced that the frequency dependent conductivity $\sigma(w)$ of a cermet may be divided into three regions, each is dominated by a different mechanism. At the low frequency range, the conduction is through dc percolation paths connecting the two electrodes. At intermediate frequency, hopping between isolated pairs of metal islands becomes important, and at high frequencies hopping between defect centres around the Fermi level is the dominant process.

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CHAPTER 4

SAMPLE PREPARATIONS

4.1 INTRODUCTION

This chapter describes the vacuum system and its components used for film depositions. This system was the one used to dc sputter pure gold contact electrodes and for the evaporations of cadmium selenide (CdSe) and chromium films during the latter stage of the project. Cermet films were deposited by R.F. sputtering in another but similar vacuum system. Evaporation sources and sputtering target constructions are given. The procedures of fabricating the specimens, electrical measuring circuits and thickness measurements are described. The structures of the CdSe and gold films are also presented.

4.2 VACUUM SYSTEM (FIG. 4.1)

The vacuum system consisted of an oil diffusion pump and a mechanical pump which was used for roughing the system vacuum and subsequently for backing the diffusion pump. The backing pressure was about 0.01 torr and the ultimate chamber pressure that could be attained by the diffusion pump was 1×10^{-6} torr.

In the connector between the vacuum chamber and the diffusion pump was a cold trap. This trap, when filled with liquid nitrogen, not only helped to improve the vacuum by trapping any water vapour that might have remained in the vacuum chamber, but it also reduced the back-diffusion of pump oil. The sputtering gas inlet was situated underneath the cold trap. Two pirani gauges were used to monitor pressure greater than 0.001 torr. One measured the backing/roughing line pressure and the other measured the chamber pressure. For chamber pressure lower than 0.001 torr, an ionisation gauge was used. When using this, proper out-gassing was carried out before taking its reading.

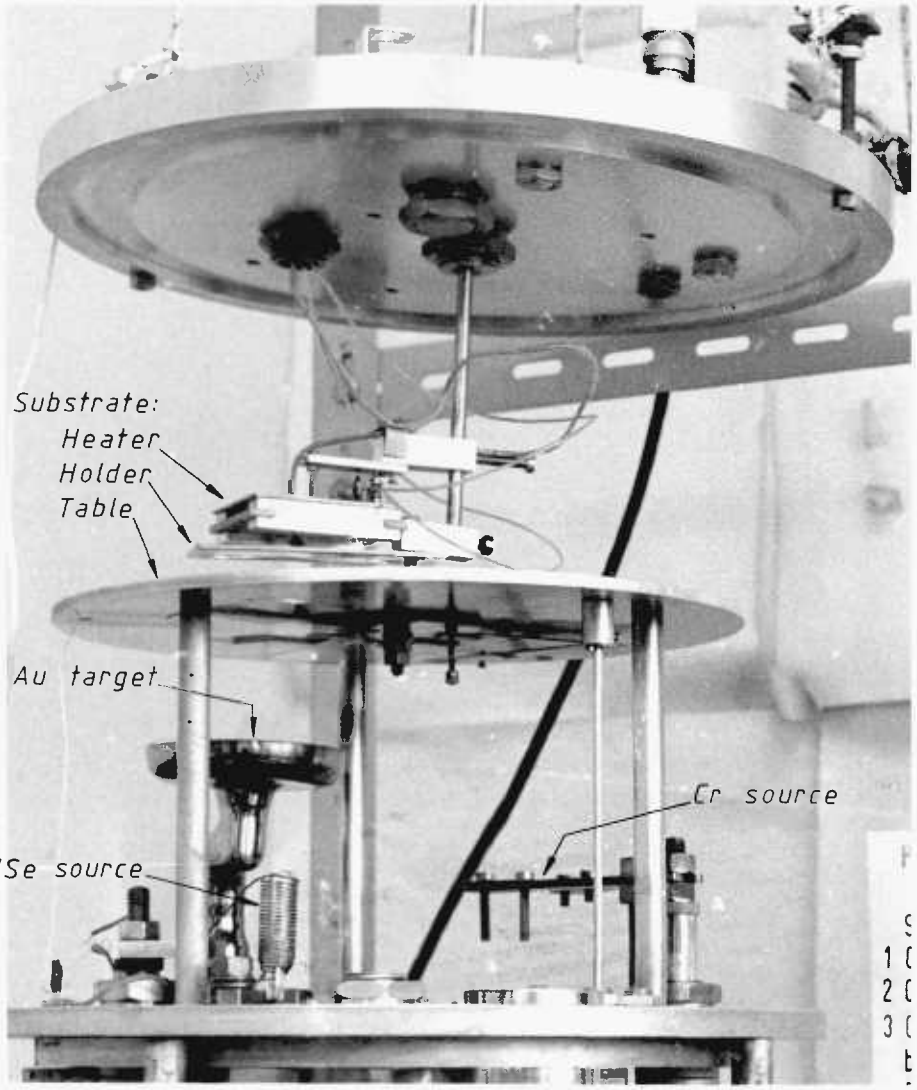

Fig. 4·2 The vacuum chamber.

Fig. 4·1 The vacuum system.

4.3 VACUUM CHAMBER (FIG. 4.2)

The vacuum chamber was made up of a pyrex glass cylinder of diameter 30 cm and height 30 cm. The top and bottom plates were made of Duralumin (an Aluminium alloy) fixed with appropriate electrical and mechanical rotary lead-throughs.

In order to ensure that the films were deposited with the least surface contamination the vacuum chamber was designed in such a way that the three processes of sputtering the gold electrode, thermal evaporation of the CdSe and chromium films could be carried out without the necessity of breaking the vacuum. To achieve this, the gold target and the CdSe and Cr evaporation sources, were placed at the circumference of a circle about 20 cm diameter. Approximately 15 cm above the vacuum base cover was a circular Duralumin plate of 27 cm diameter. Holes directly above the target and sources were cut in this plate which acted as a table for holding the appropriate masks horizontally. Three stainless steel shutters were provided immediately under these holes so that pre-sputtering and pre-evaporation could be carried out before actual deposition took place. The substrate was held in a substrate holder which in turn was held on a rotary lead-through by an extender. This lead-through passed through the centre of the top chamber cover. In this way, the substrate could be carried from one source position to another without breaking the vacuum. Each mask, which was made by the standard photoresist and etching

technique, was held in its proper position over the holes in the substrate table by two alignment pins. Two holes were drilled at the corresponding positions of the substrate holder. In this way, good alignment of the substrate to the masks could be achieved by having the two alignment pins passing through the holes.

The substrate holder was allowed to have a slight freedom of movement in the horizontal plane by the loose connection of the joint to the extender. In this way, it was no longer necessary to have exact alignment between the centre of the top chamber cover to that of the mask table which was supported by three stainless steel rods standing on the bottom chamber cover.

A radiative heater made of molybdenum wire and held by the same lead-through as the substrate holder was placed on top of the substrate. This enabled the substrate temperature to be raised up to about 300^{o}C during deposition or for subsequent annealing of a sample in vacuum.

4.4 EVAPORATION SOURCES

(a) Chromium source: The chromium used for evaporation was in pellet form, roughly 2 to 3 mm diameter. Each pellet was crushed into two or three pieces. After cleaning with acetone, a few pieces of these were put on top of a tungsten strip filament about 10 mm wide, 50 mm long and 0.12 mm thick. This was situated at about 10 cm below the substrate table. To avoid contamination to the rest of the vacuum chamber during the chromium evaporation, the source was surrounded with stainless steel sheets on all sides except that towards the mask table.

(b) Cadmium selenide source*: The cadmium selenide material was in powder form of 99.999% purity. This was filled into a quartz evaporation boat until half full (Fig. 4.3). A small amount of quartz wool was put on top to prevent the CdSe powder from splattering during evaporation. The bottom of the boat has an appendix protruding into its centre. This provided a receptacle for a Chromel-Alumel thermocouple so that the temperature of the CdSe powder could be monitored more accurately during evaporation. The boat was then put into a coil basket heater made of molybdenum wire of 1 mm diameter. This was situated at about 10 cm below the mask table. As with the chromium source, this source was also properly shielded to avoid contamination.

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*This set up was devised by Dr. M.J. Lee (private communication)

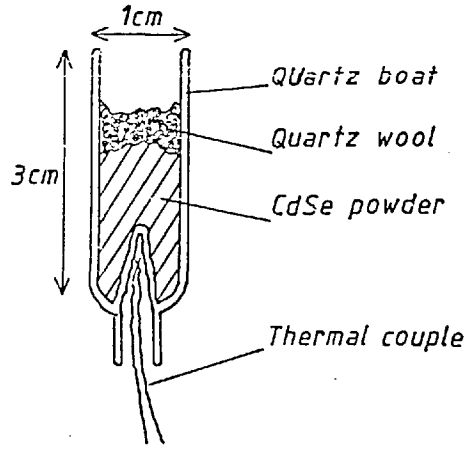


Fig. 4·3 CdSe evaporation source.

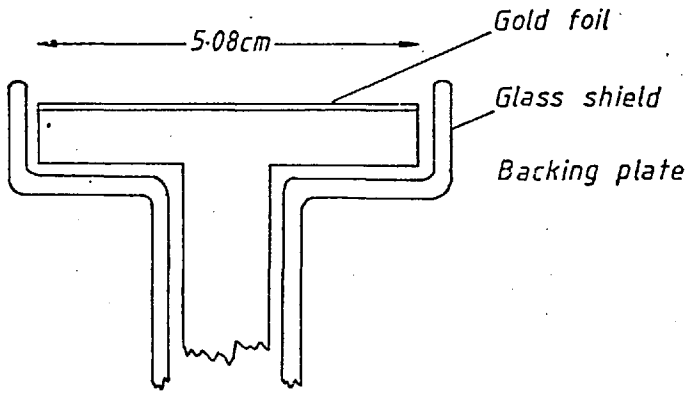


Fig. 4·4a DC sputtering gold target.

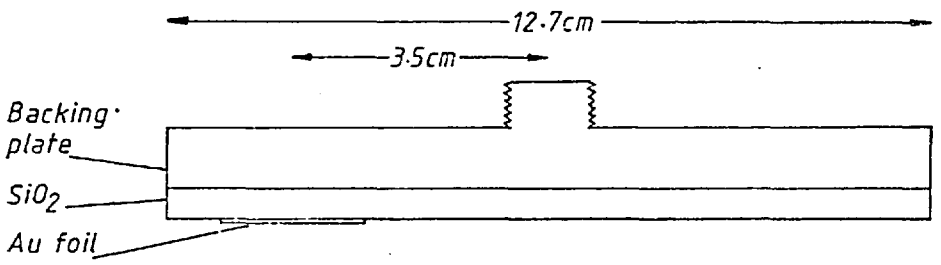


Fig. 4·4b RF co-sputtering cermet target.

4.5 SPUTTERING TARGETS

(a) Gold target:

The gold target (Fig. 4.4a) used for sputtering was made up of a circular disc of gold foil 50 mm diameter, 0.125 mm thick and 99.99+% purity. This gold foil was held on a stainless steel target backing plate with thermo-setting silver conductive araldite. Since dc was used to sputter this gold target, glass-ware could be used to envelope the target backing plate and its lead-through rather than a metal shield insulated from the target. When the sputtering plasma was first turned on, the glass envelop quickly charged up to the supply voltage, which prevented it from being sputtered away by the high energy sputtering ions. Hence this envelop acted as a dark space shield. Upward sputtering was used; the substrate was held facing downwards by a substrate holder with appropriate mask. A shutter was available so that pre-sputtering could be carried out.

(b) Cermet target:

Cermet films were deposited by co-sputtering gold and silicon dioxide (SiO_2). As there were no facilities for carrying out R.F. (ac) sputtering in the vacuum system described previously, it was necessary to do this in another system. The SiO_2 composite of this target was a 5 inch (12.7 cm) diameter, 0.25 inch (6.35 mm) thick slab of 99.99% purity. It was bonded to a Duralumin target backing plate with conductive araldite. In order to enable a wide range

of gold to SiO_2 ratios to be obtained from a single target, a circular gold foil of 25 mm diameter and 99.99+% purity was bonded off-centre on the face of the SiO_2 slab (Fig. 4.4b). The whole target was then screwed onto a water-cooled backing plate which was connected to the matching circuit of a R.F. sputtering machine. The sputtering frequency was 13.56 MHz. An aluminium dark space shield was constructed around the target and its lead-though. Downward sputtering was used. The substrate was placed on top of a water-cooled table 6 cm below the target. By varying the position of the substrate with respect to the gold foil (Fig. 4.5),a large range of metal (gold) fraction ranging from almost pure gold at places just underneath the gold foil to almost pure SiO_2 at the other end could be obtained.

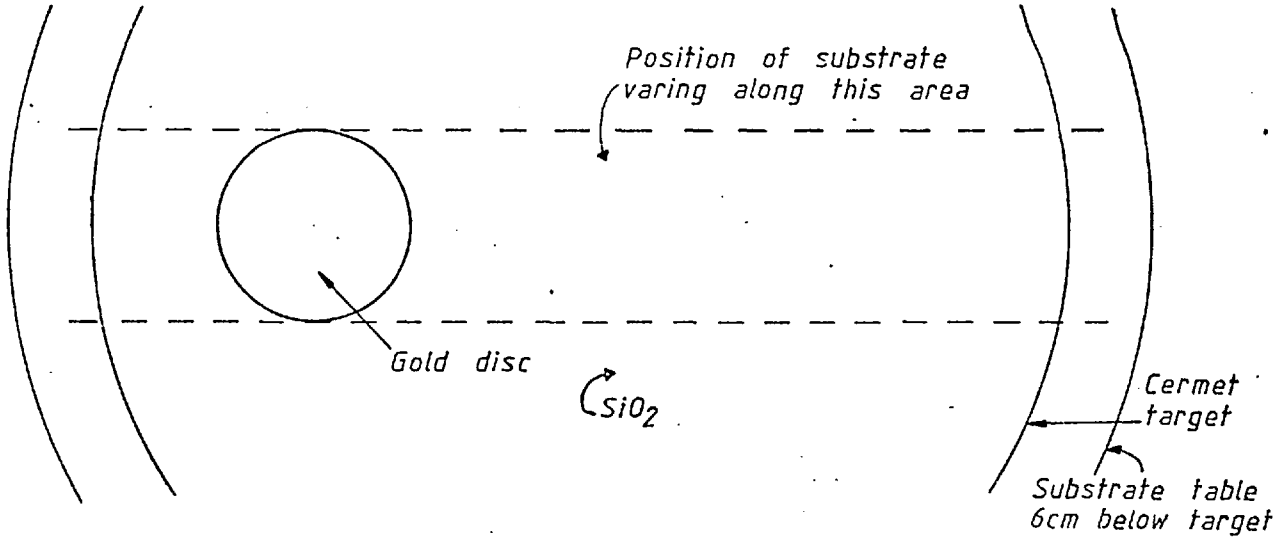


Fig. 4·5 Plan view of the cermet target and the substrate table.

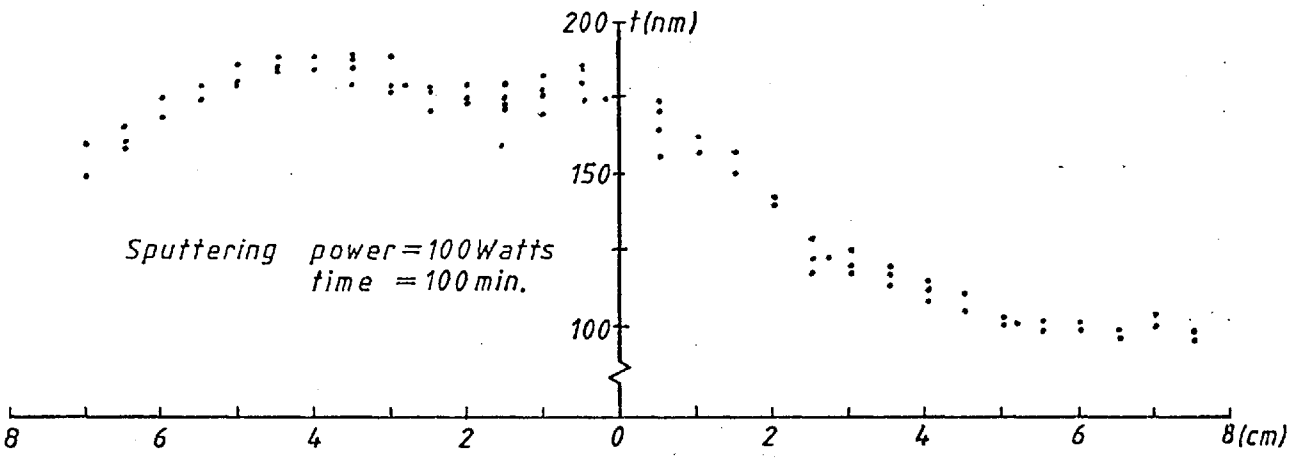


Fig. 4·6a Cermet thickness

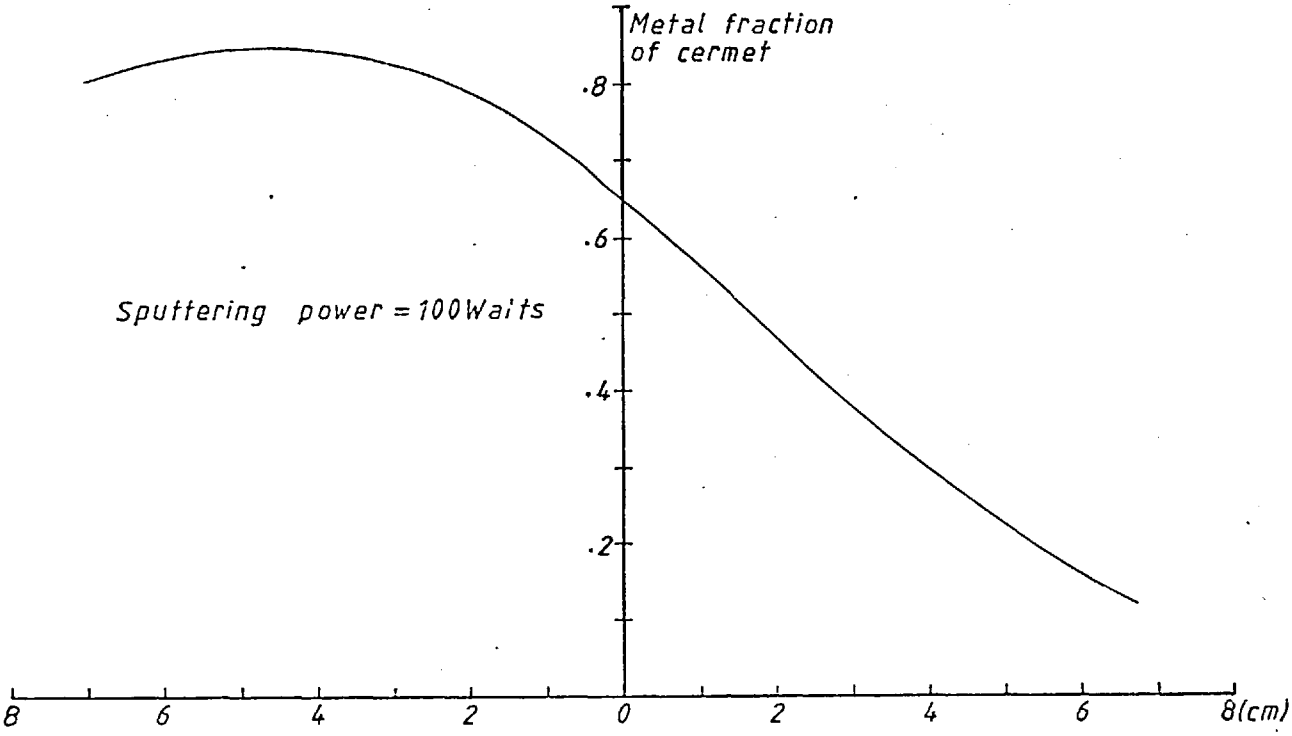


Fig. 4·6b Metal (gold) fraction in the cermet.

4.6 SAMPLE PREPARATIONS WITH SILICON WAFERS

Each of the silicon wafers consists of a heavily doped ($<10^{-5}$ Ωm) n-type substrate with an n-type epitaxial layer about 9 μm thick. The resistivity of this layer is quoted as 0.024-0.028 Ωm. Using the conductivity equation $\sigma = nq\mu$, with $\mu = .15\ m^2/Vs$, the doping density N which equals the carrier density n is about $1.7 \times 10^{21}\ m^{-3}$.

In order to remove the surface layer due to oxidation and contamination from foreign matter, the silicon wafer was first of all degreased with iso-propyl alcohol (IPA) in a vapour degreaser. It was then immersed into a dilute etchant made up of HF (40%) : HNO_3 : H_2O (distilled) in volume ratio of 5:3:100. The etching time was about 100 s, enough to remove about 15 nm of oxide[1]. The etchant was then infinitely diluted with distilled water without the wafer being exposed to air. It was then immediately transferred into the vacuum chamber.

For specimens with pure-gold contacts, the silicon wafer was put facing down in close contact over a metal mask in the dc sputtering system. The mask has a number of 1 mm diameter holes and was at about 50 mm above the gold target. The vacuum chamber was then pumped down to below 5×10^{-6} torr pressure and the cold trap was filled with liquid nitrogen. The sputtering process was carried out in high purity (99.999%) Argon gas pressure of about 0.015 torr at 3 kV and 4 mA. Pre-sputtering time

with the shutter closed was about three minutes, and deposition time (shutter open) twelve minutes. This gave a gold dot thickness of about 100 nm.

For specimens with gold-cermet-silicon configurations, the silicon surface was covered with a cermet film before gold dots were deposited in the same way as described in the above paragraph. The cleaned silicon wafer was transferred into the R.F. sputtering system and placed on top of the water-cooled substrate table at the appropriate position which would give the desired gold fraction. The vacuum chamber was then pumped down to about 10^{-5} torr and a liquid nitrogen cold trap was used. Sputtering was proceeded at 100 W in an atmosphere of 90% Argon, 10% oxygen gas mixture. About 10 minutes of pre-sputtering was made before actual deposition. Cermet thickness was predominantly about 100 nm for about 70 to 100 minutes of deposition time.

4.7 SAMPLE PREPARATIONS WITH CdSe

The following describes the procedures of producing a sample with gold electrode at the bottom, followed by a CdSe film and then chromium circular dots which provide ohmic contacts to the CdSe film.

The substrate was a soda-glass microscope slide of 76 x 26 x 1.0 mm. First of all, it was thoroughly cleaned with detergent (Teepol). After rinsing, it was immersed in a beaker of distilled water and put in an ultra-sonic cleaner for about three minutes. Then it was transferred into a vapour degreaser to ensure that any grease remaining on the slide was removed by the iso-propyl alcohol (IPA). It was then put onto the substrate holder in the vacuum chamber and evacuation started immediately.

The system was allowed to pump for at least 15 hours before any film deposition was carried out. This ensured that as much water or other volatile molecules adsorbed on the surfaces were removed. Then the cold trap was filled with liquid nitrogen. The ultimate pressure was 1×10^{-6} torr. By manupulating the rotary lead-though, the substrate holder was positioned onto the alignment pins on the substrate table facing the gold target. Sputtering was carried out as described in section 4.6. When this was completed, the gas inlet valve was closed and the vacuum chamber pressure decreased to 1×10^{-6} torr within a minute. However, the system was allowed to continue pumping for the next half an hour before the substrate holder was aligned with the pins on the table facing the CdSe source. The temperature of

this source was then increased gradually to the deposition temperature of between 700°C and 750°C in about five minutes. Pre-evaporation was continued for the next minute or so before the shutter was opened. During deposition, the pressure increased to about 10^{-5} torr.

When the CdSe deposition was completed, the shutter was closed and the source heating current was switched off. Half an hour later, the substrate was moved to the mask position where chromium contacts were evaporated. Since the chromium pellets absorbed a large quantity of gases, mainly hydrogen, during its purification by the manufacturers, fresh pellets were always out-gassed at about 1000°C for five minutes. This was done before the gold deposition in order to avoid contamination. Although chromium has a melting point of 1875°C, it has a high vapour pressure of 10^{-2} torr at 1400°C[2]. Therefore sublimation occurred readily at about 1500°C[1] which was the temperature used for evaporation. The chamber pressure rose to about 5×10^{-6} torr during evaporation. The thickness of this chromium contact was not important. Normally for a deposition time of five minutes, about 60 nm thick was achieved.

4.8 FILM THICKNESS MEASUREMENTS AND CERMET METAL FRACTIONS

A Talysurf was used to measure film thickness. A stylus in the instrument traverse across a step in the film, and its vertical movement was amplified electronically and recorded onto a chart. To obtain accurate readings, the films have to be hard enough so that minimal scratches were caused by the stylus. Repeated uses indicated that this was so with both the CdSe and cermet films. Fig. 4.6a is the thickness profile of a cermet film deposited on a glass slide plotted against position measured from the centre of the substrate table which coincides with the centre of the cermet target. The sputtering was carried out at 100 W for 100 minutes.

The gold fractions of cermet films were analysed with electron microprobe techniques by the Analytical Laboratories of Imperial College. The results are shown in Fig. 4.6b. Their accuracy is no better than ±10%.

4.9 ELECTRICAL MEASUREMENTS

(a) Contacts for Measurements:

In order to reduce the series resistance of the measuring leads and contacts, an aluminium film was evaporated over the gold underlay on the area not covered with CdSe for the case of Cr/CdSe/Au samples (see Fig. 6.1). A copper wire of diameter 0.1 mm and length about 40 mm was then soldered onto the aluminium film. For the case of silicon samples, the bottom of the silicon wafer was coated with silver dag paint first before the copper wire was soldered to the dag. Because of the large contact area between the dag and the n^+ silicon wafer, the parasitic contact impedance was negligible. The end of the copper wire was then soldered to the measuring lead. A light tight metal box was constructed to hold a spring loaded gold wire of 1 mm diameter. This gold probe was used to make contact with the dot electrodes on the surface of the specimen. A schematic diagram of the set-up is shown in Fig. 4.7. In this arrangement, measurements could be carried out with the sample in the dark to avoid any photo-effects, and the metal box also reduced noise levels.

(b) I-V Measurement Instruments:

Because of the small current and high resistivity of some samples that have to be measured, it was necessary to use a pico-ammeter and a very high input impedance voltmeter to make electrical measurements. For this

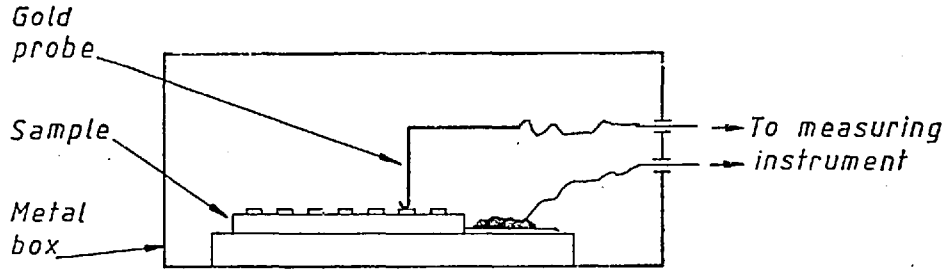


Fig. 4·7 Metal box for making electrical measurements.

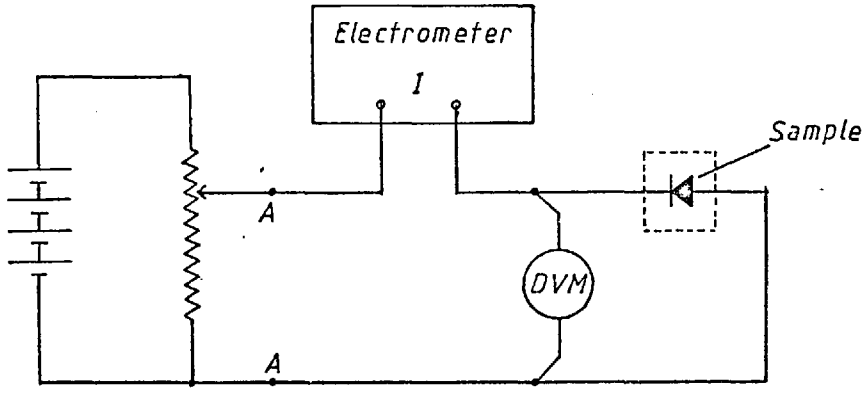


Fig. 4·8 I – V measurement circuit.

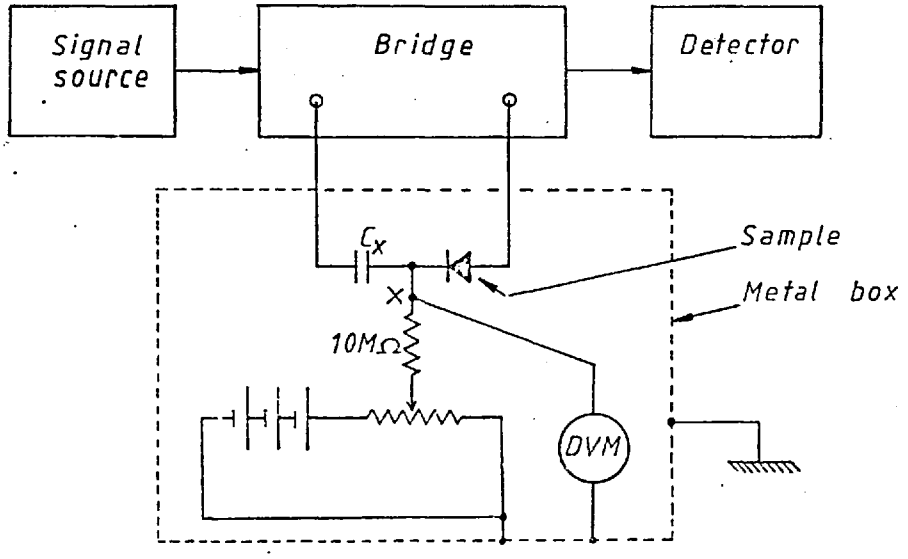


Fig. 4·9 C – V and G – V measurement circuit.

purpose, the Keithley electrometers (Model 602 analogue or Model 616 digital) were used. The input impedance of these meters in the voltage scale was about 10^{14} Ω. The set-up of the measuring circuit was as shown in Fig. 4.8. The voltage applied across the sample was varied with a decade potential divider supplied by a series of dry batteries. Screened wires were used in all external connections. The meters could be used in the 'fast' or feed-back mode during current measurements so that there was virtually zero voltage drop across its input terminals. In this way the voltmeter could be put across points A-A to avoid shunting the sample when very resistive ones were measured.

(c) C-V Measurement Instruments:

The capacitance of the samples was measured with Wayne Kerr bridges. (Model B221 for audio frequency and Model B601 for higher frequency from 15 KHz to 5 MHz.) These bridges also gave the ac conductance in parallel with the capacitance. They could also be used in such a way that a dc voltage could be applied across the sample. The circuit used for this purpose was as shown in Fig. 4.9. The voltmeter was connected across the point X to the neutral of the bridge. This neutral line was the centre tapping of the bridge output (current) transformer. Since the dc leakage current flowing through the sample was small, there was negligible voltage drop

across the transformer winding. Therefore the voltmeter effectively measured the bias voltage across the sample while at the same time it did not affect the readings of the bridge. C_X was a dc blocking capacitance whose value was chosen so that its impedance was less than that of the bias circuit (10 MΩ) and the sample. The whole circuit was built inside the metal box used for making electrical measurements.

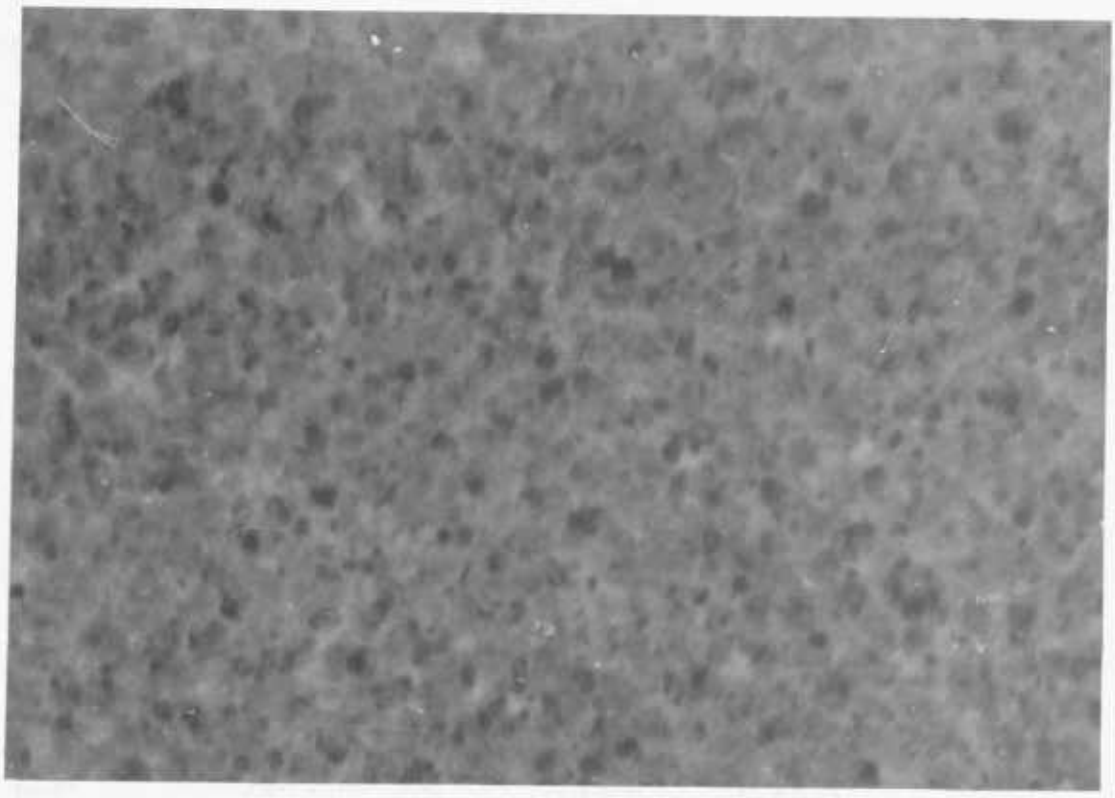


Fig. 4·10 Transmission electron micrograph showing the poly-crystalline nature of an evaporated CdSe film.

4.10 STRUCTURE OF CdSe FILMS

(a) Electron Microscopy:

Evaporated CdSe films are polycrystalline. Fig. 4.10 shows an electron micrograph of a CdSe film about 45 nm thick. The crystallites are about 40 nm in diameter. In order to find out the surface topography of these samples, some surface carbon replicas were made. The procedure was as follows (Fig. 4.11). A very thin aluminium film of about 10 nm was first of all evaporated onto the CdSe surface to be replicated. This was then shadowed with a very small amount of gold at an angle of 45°. A layer of carbon film was then deposited on top by arc-evaporation. Finally the sample was immersed into dilute HCℓ acid. The carbon film, together with the gold, floated off very quickly. The thin aluminium film was necessary because otherwise the carbon film could not be floated off the CdSe surface. Although this would limit the faithfulness of the surface reproductions, the resolution was in fact limited by the gold islands used to shadow the surface. Ideally, platinum should be used because this would produce much smaller island sizes. But because no platinum material was available for evaporation, gold was used instead. Fig. 4.12a is an electron micrograph of the surface replica of a CdSe sample deposited with the substrate at room temperature. The resolution was limited by the gold islands, and so it can only be said that no large surface feature

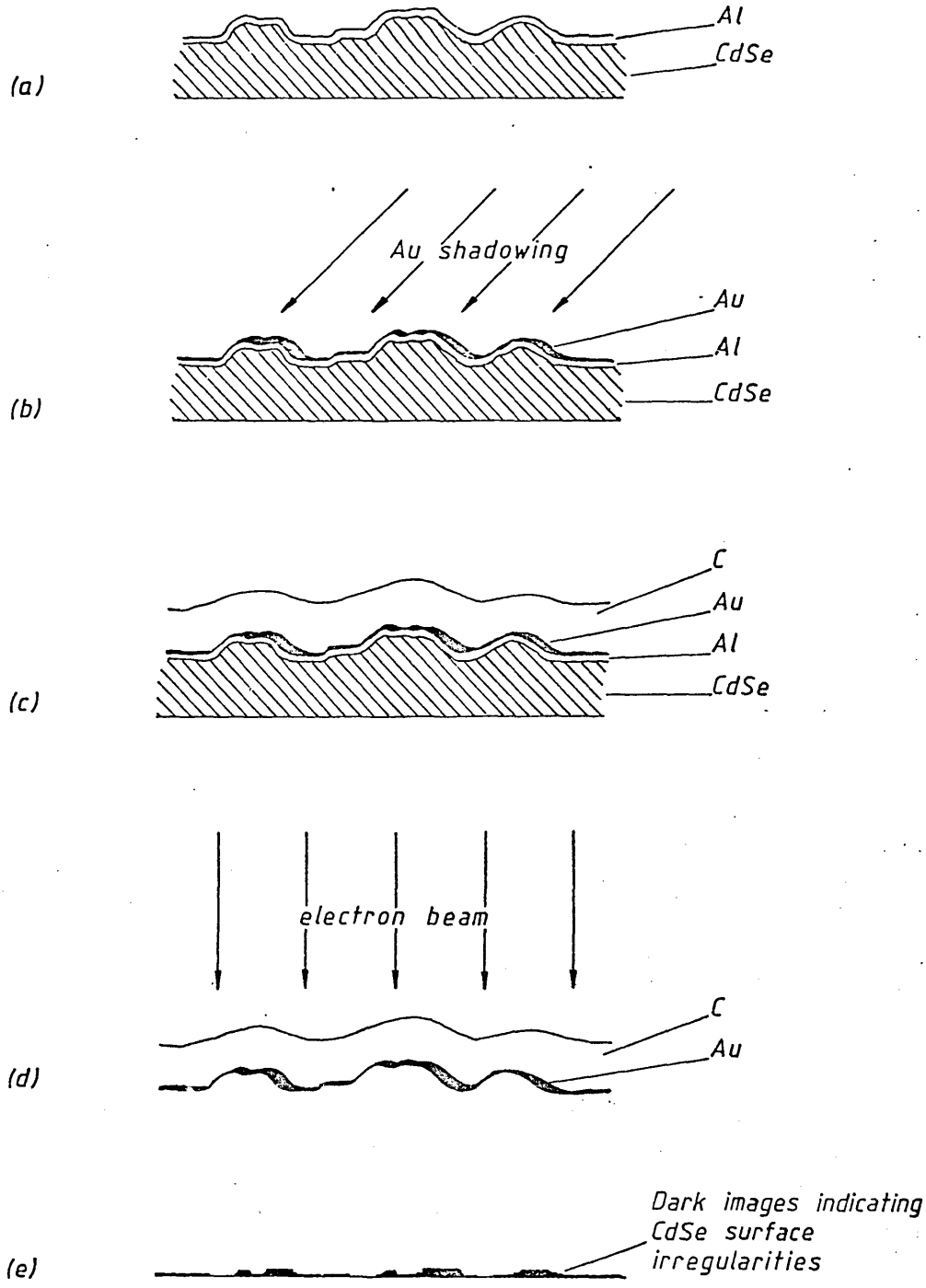


Fig. 4·11 Surface replication technique: (a) Al coating, (b) gold shadowing, (c) carbon support, (d) replica lifted off with dilute HCl, (e) electron micrograph of the replica.

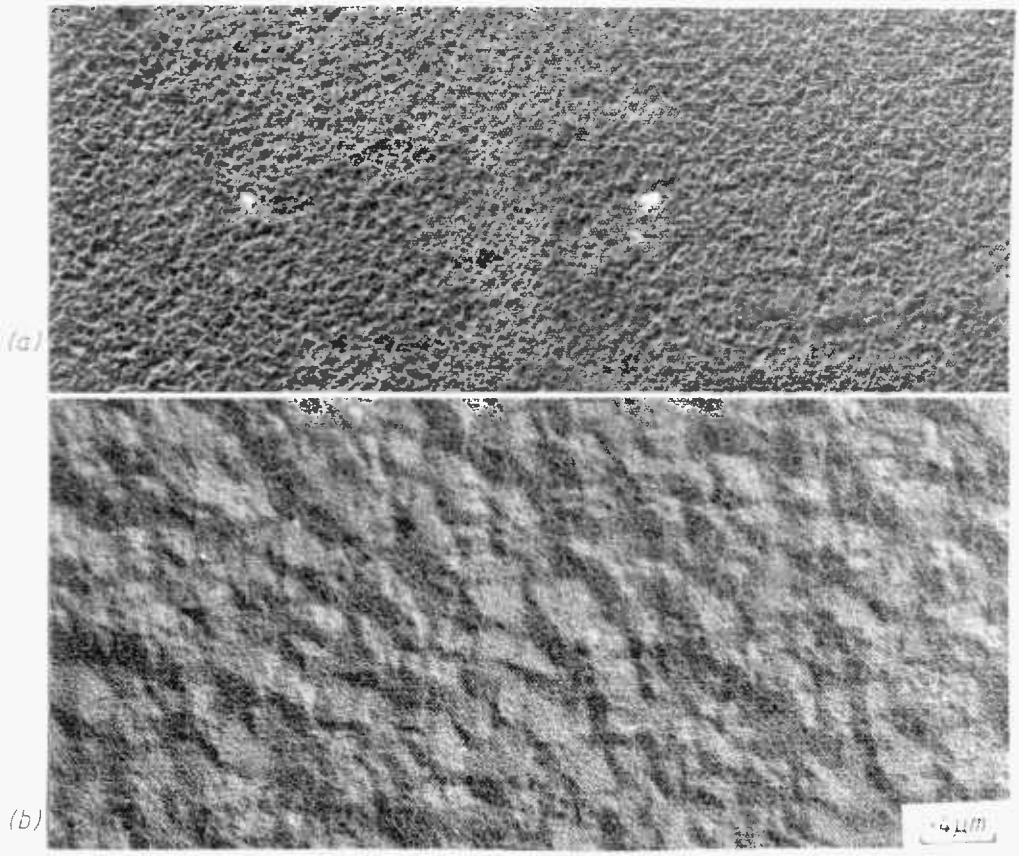


Fig. 4 12 Evaporated CdSe surface replicas with substrates at (a) room temperature, and (b) 200 °C.

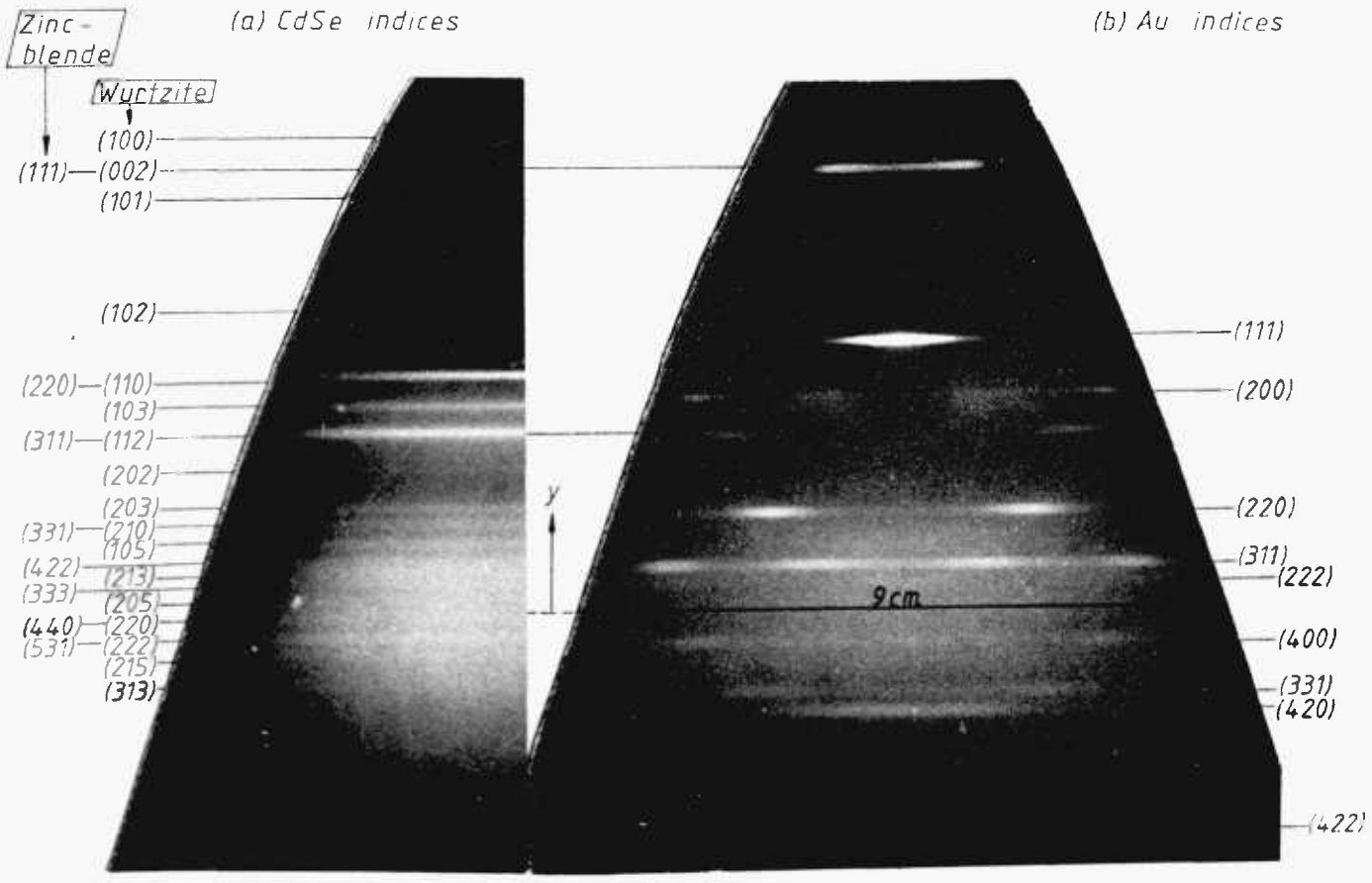


Fig. 4·13 Cylindrical texture X-ray diffraction of (a) CdSe powder pellet, and (b) evaporated CdSe on gold film.

was present. Fig. 4.12b is one with the substrate held at 200°C during CdSe deposition. This clearly shows large hilly features, indicating that the CdSe crystallites have grown to such a large extent (∿.5 μm) that the surface became microscopically rough.

(b) X-ray Crystallography:

The crystalline structure[3] of CdSe is tetrahedral in which each atom is surrounded by four equidistant nearest neighbours of the opposite type which lie at the corners of a tetrahedron. They may crystallise in two forms. One is the cubic zincblende or the diamond lattice which may be considered as two interpenetrating face-centred cubic lattices. The coordinates of the atoms are

Cd: 000 , $0\frac{1}{2}\frac{1}{2}$, $\frac{1}{2}0\frac{1}{2}$, $\frac{1}{2}\frac{1}{2}0$

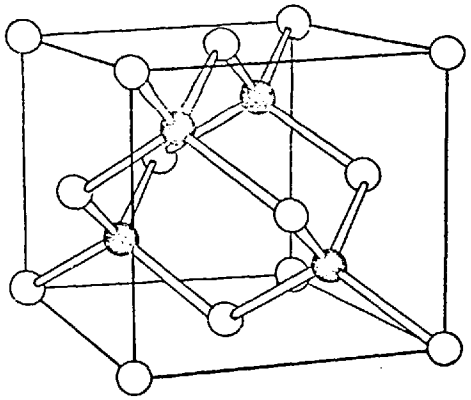
Se: $\frac{1}{4}\frac{1}{4}\frac{1}{4}$, $\frac{1}{4}\frac{3}{4}\frac{3}{4}$, $\frac{3}{4}\frac{1}{4}\frac{3}{4}$, $\frac{3}{4}\frac{3}{4}\frac{1}{4}$

and is shown in Fig. 4.14a. The lattice distance is a = 0.605 nm. The other form is the wurtzite or zincite (ZnO) arrangement with hexagonal unit cell. The coordinates of the atoms are

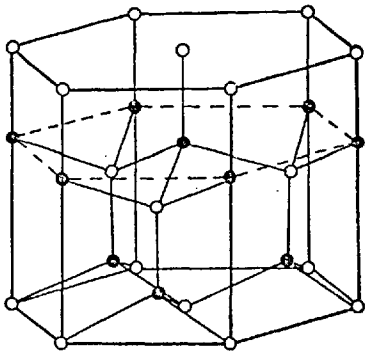
Cd: 000 , $\frac{2}{3}\frac{1}{3}\frac{1}{2}$

Se: $00u + \frac{1}{2}$, $\frac{2}{3}\frac{1}{3}u$

and is shown in Fig. 4.14b. The lattice distances are a = 0.4299 nm and c = 0.7015 nm[4,5].



(a) Zincblende



(b) Wurtzite

Fig. 4·14 Crystal structures of CdSe

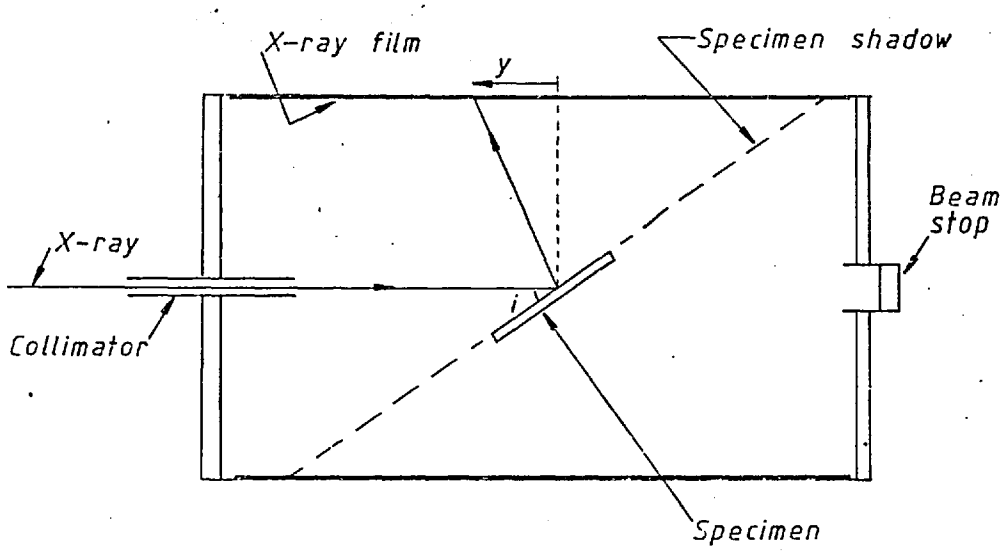


Fig 4 15 Cross sectional view of a X-ray cylindrical texture camera. Angle of incidence = i

In order to confirm that the deposition technique produced the wanted structure, some x-ray diffraction analyses were carried out on the evaporated CdSe samples using a cylindrical texture camera[6]. A cross-sectional view of the camera is shown in Fig. 4.15. An x-ray negative film was wrapped round the inside surface of the cylinder of radius R = 28.65 mm . The x-ray was produced from a water-cooled copper target. After passing through a nickel filter, the $K\alpha_1$ line was incident onto the surface of the sample at an angle i = 20°. Fig. 4.13 shows prints from the exposed negative. Fig. 4.13a is from a compressed CdSe pellet made from the source powder, and Fig. 4.13b is from a sample with evaporated CdSe on top of a gold underlay. Although the CdSe was about 1 μm thick, its small scattering factor permitted the x-ray to penetrate it and allowed diffraction from the gold film to be recorded. The origin of the y-axis in these prints are at the positions where the width of the x-ray cut-off shadow is πR or 90 mm. The positions of the lines, y, from the origin are related to the diffraction angles θ by

$$\tan 2\theta = \frac{R}{y}$$

and the interplanar spacing d from Bragg's law

$$d = \frac{\lambda}{2 \sin \theta}$$

where λ is the wavelength of the x-ray. For the Cu-$K\alpha_1$ this is 0.15405 nm. Therefore the plane spacings could

be calculated and compared with the ASTM index. They were found to be within ±0.001 nm of the values given in the ASTM index. The corresponding planes were indexed as shown in the prints. The sample with CdSe on top of gold, Fig. 4.13b, showed that various lines corresponding to the wurtzite structure were missing. The more prominent ones were the (100), (101) and (102) lines. Instead, the (002) wurtzite (or (111) zincblende) line in Fig. 4.13b appeared more relatively intense than the one in Fig. 4.13a. From these it may be inferred that evaporated CdSe crystallised mainly in zinc-blende structure. The other possibility is that it crystallised in wurtzite form but preferentially with the (00.1) planes parallel to the surface and therefore giving rise to extraordinarily high intensity[7]. Furthermore, the diffractions on Fig. 4.13b are closer to spots rather than lines. This indicates that the crystallites of the films were preferentially orientated. It can be shown[6] that a diffraction plane of Bragg angle θ inclined at an angle α to the specimen surface would diffract the x-ray according to the equation

$$\cos \alpha = \sin \theta \sin i + \cos \theta \cos i \cos \phi$$

where ϕ is the angle between the planes, parallel to the camera axis, containing the diffracted beam and the specimen surface normal, i.e. the x coordinate is equal to

$R\,\phi(\text{rad.})$ or $\theta = 180x/\pi R$ (deg.). Since R = 28.65 mm, we have $\theta(\text{deg.}) \simeq 2\,x$ (mm). This is the distance between the pairs of spots diffracted symmetrically about the y-axis. One may therefore calculate the orientations of the diffracting planes. When this was done for the diffractions due to the gold film, it was found that all spots could be identified as indicating that the (111) planes of the gold crystallites were parallel to the surface of the specimen. This shows the large degree of preferential orientations of gold film even when nucleation occurred on an amorphous surface held at room temperature.

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CHAPTER 5

EXPERIMENTAL RESULTS OF SILICON SAMPLES

5.1 INTRODUCTION

This chapter presents the results and discussion of the electrical measurements carried out on samples fabricated with silicon single crystal wafers. As mentioned in section 4.6, these wafers have n-type epitaxial layers of about 9 μm thick and resistivity of about 0.025 Ωm, which gives a free electron carrier density of about 1.7×10^{21} m^{-3}.

As a preliminary check on the experimental techniques, some electrical measurements were made on sputtered pure-gold/silicon contacts. Although evaporated gold/silicon contacts have been very extensively investigated, very little work has been reported on sputtered gold. This experiment should therefore ascertain the presence of a Schottky barrier and its properties can also be used to compare with those of cermet contacts.

Since a fairly wide range of metal fractions of cermet films were deposited, Table 5.1 is constructed to explain the labelling of the samples and also gives the actual cermet thickness and metal fraction as derived from Fig. 4.6. Each sample (Fig. 5.1) was given a symbol according to its configuration. As described in section 4.6, on top of the cermet was sputtered a number of gold dots 1 mm diameter. These gold dots provided contacts to the cermet and were labelled with letters from A to M.

The results for the cermet/silicon contacts are divided into two categories. One is for conductive cermets in which the space charge region of the silicon was very much influenced by the dc current flowing across the barrier. The other is for insulating cermets in which there was negligible current flow and the properties were largely affected by charges near the interface. Finally, the chapter concludes with a general discussion of these experimental observations.

Table 5·1

Symbol	Configuration	Metal fraction	Cermet thickness(nm.)
CmSi2	Au/cermet/Si		
dot A		0·66	160
dot G		0·56	145
dot M		0·47	125
CmAl2	Au/cermet/Al		
dot A		0·66	160
dot G		0·56	145
dot M		0·47	125
CmSi3	Au/cermet/Si		
dot A		0·47	85
dot G		0·38	75
dot M		0·30	70
CmSi4	Au/cermet/Si		
dot A		0·30	115
dot G		0·25	110
dot M		0·15	105

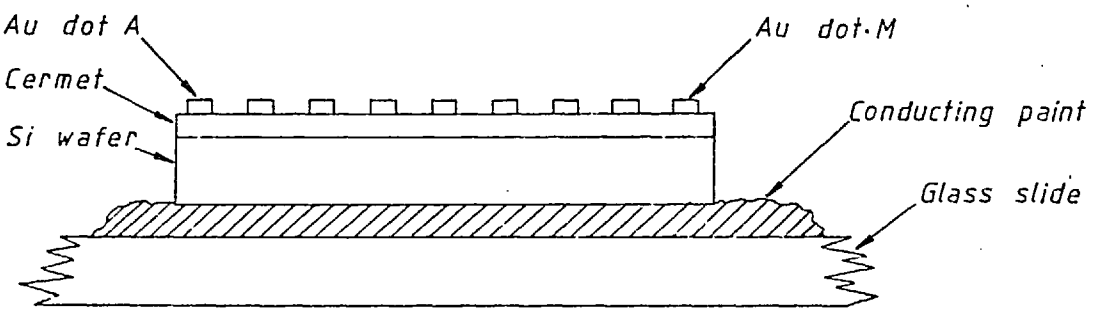


Fig. 5·1 Schematic diagram of a Au/cermet/Si sample.

5.2 SPUTTERED GOLD-SILICON SCHOTTKY BARRIER

5.2.1 I-V Characteristics

The current equation for a diode is generally written as $I = I_s[\exp(\beta V) - 1]$. This can be rearranged to give

$$\frac{I}{1 - \exp(-\beta V)} = I_s \exp(\beta V) \qquad (5.1)$$

where I_s is the saturation current. Therefore plotting $\log [I/(1 - \exp(-\beta V)]$ vs V should give a straight line. This procedure is carried out for the forward bias I-V measurements of the sputtered gold-silicon Schottky barriers. A typical result is shown in Fig. 5.2. A good straight line is obtained for low current values. The departure of the measured points at higher current from linearity can be accounted for by assuming that there is a resistance of 2.3 ohms in series with the Schottky barrier. This resistance, R_s, may be due to that of the contacts and measuring leads. The intercept on the y-axis gives the saturation current as 1.32×10^{-6} A (1.69 A/m^2). Assuming that the conduction process is by thermionic emission, then from eqn. (2.44), $I_s = A^{**} T^2 \exp(-\beta V_{bo})$. The barrier height lowering voltage is ignored; the value of V_{bo} obtained is treated as the barrier height at zero bias. Using $A^{**} = 110 \times 10^4$ A m^{-2} k^{-2} and T = 300 K, V_{bo} is found to be 0.642 eV. Comparing this value with those of

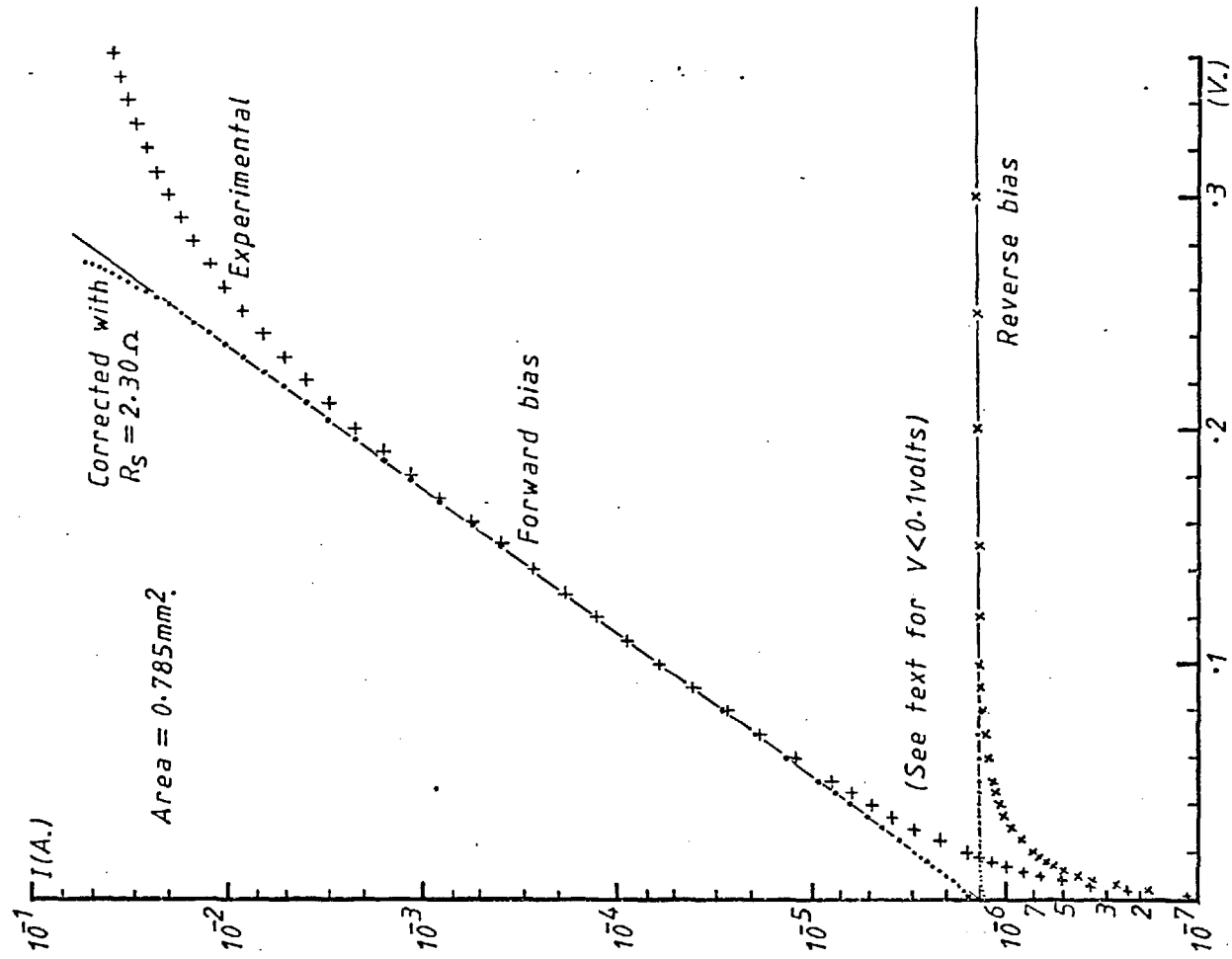


Fig. 5.2 I—V characteristics of sputtered Au—Si contact.

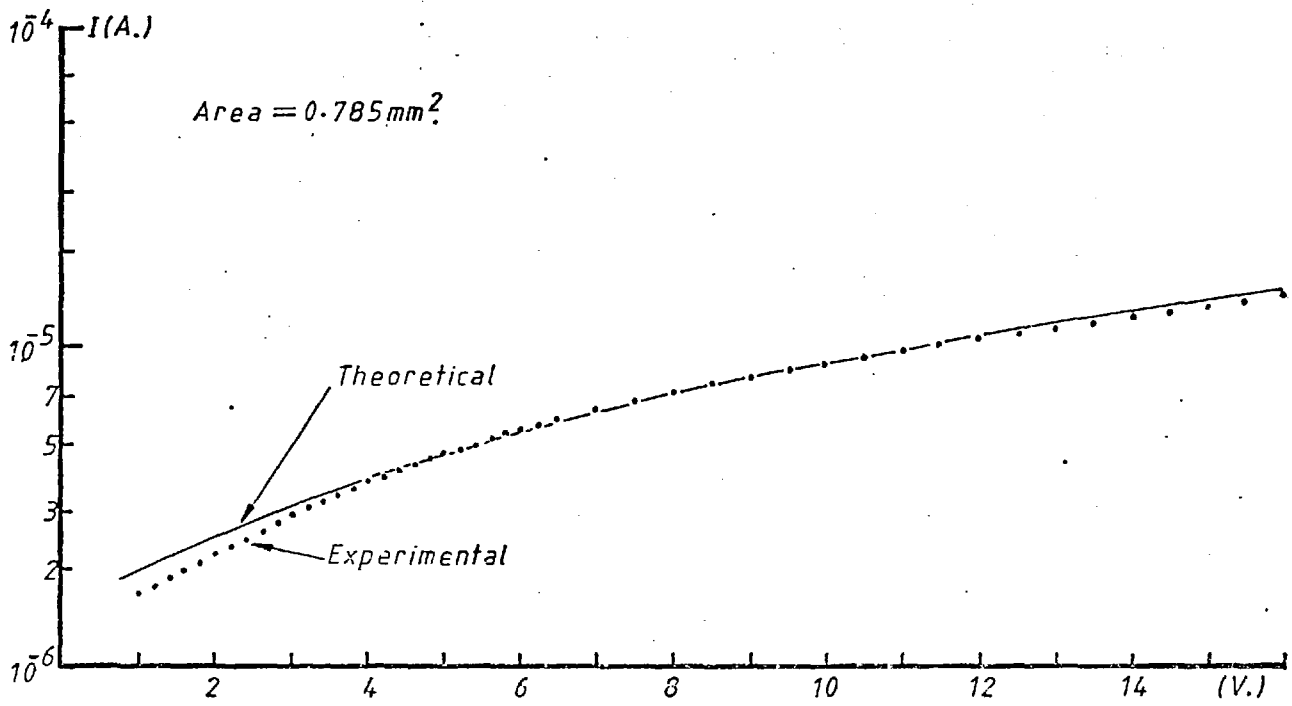


Fig. 5.3 Reverse bias I—V characteristics of a sputtered Au—Si contact.

evaporated gold contact which has a barrier height of 0.80 eV[1,2], the difference cannot be accounted for by the uncertainties in the values of A^{**}, T and contact area used.

For an ideal barrier, the slope of the plot should be equal to β, i.e. q/kT. However, for a practical barrier, the barrier height V_{bo} is a function of the diffusion potential as discussed in section 2.5. Therefore V_{bo} would change with the applied bias V. This change, $\Delta\phi$, may be expressed as a power series of V. But for small V, as with the case of forward bias, the higher order terms may be ignored. Consequently the barrier height lowering is proportional to V. This results in an exponential increase of I_s with V. The effect is to introduce a constant, η, into the general diode equation, thus $I = I_s \exp(qV/\eta kT)$ for $V > 3\ kT/q$. The value of η as determined from the slope of the experiment is 1.01 ± 0.02 when T = 300 K is used.

The reverse bias characteristic shows apparently good saturation at low bias (< 1 volt), but the current eventually increases by an order of magnitude at a bias voltage of 16 volts. This is shown in Fig. 5.3. In order to explain this large departure from ideality, it was initially assumed that the barrier height was being lowered by image forces. Thus, from eqn. (2.44) the reverse current can be written as

$$\frac{I}{1-\exp(-\beta V)} = I_s \exp(\beta \Delta\phi) \qquad (5.2)$$

From eqn. (2.42) we see that $\Delta\phi = A(V_{bi} + V - kT/q)^{\frac{1}{4}}$ where A is a proportionality constant. The value of V here is taken as the magnitude of the reverse bias voltage. The diffusion potential V_{bi} is given by $(V_{bo} - V_n)$. The potential, V_n, of the Fermi level below the conduction band can be obtained from the donor (free electron) density since $n = N_c \exp(-\beta V_n)$. Using $n = 1.7 \times 10^{21}$ m^{-3} and $N_c = 2.8 \times 10^{25}$ m^{-3}, we have $V_n = 0.251$ eV. The value of V_{bo} is taken as the one obtained under the forward bias condition, which is 0.64 eV. These give

$$V_{bi} = V_{bo} - V_n = 0.39 \text{ eV} \qquad (5.3)$$

Since $kT/q = 0.026$ eV, we have $\Delta\phi = A(.36 + V)^{\frac{1}{4}}$. In Fig. 5.4 is a plot of $\log[I/(1-\exp(-\beta V))]$ vs $(.36 + V)^{\frac{1}{4}}$. A straight line can approximately be drawn with a slope of about 2.32. This slope is βA and may be used to compare with the theoretical value as given by eqn. (2.42). As noted in section 2.5, it is doubtful as to what value of dielectric constant, ε_d, should be used for image forces. If it is taken as equal to the silicon static value of 11.8, then the slope calculated is $\beta A = 0.646$. However if the free space value, ε_o, is used, then the slope should be 2.22[3]. One sees that the latter value is closer to the experimental result.

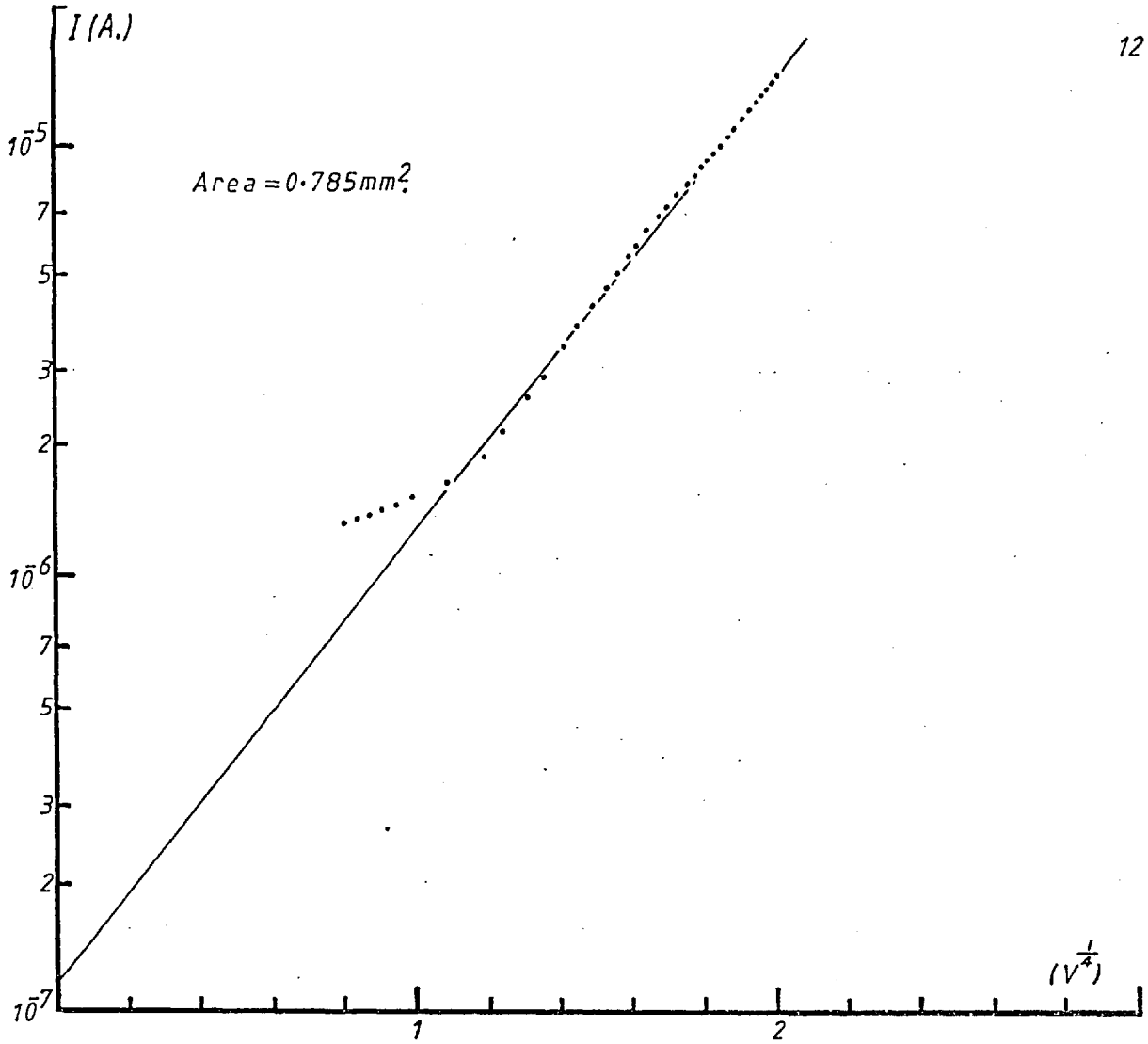


Fig. 5.4 Reverse bias current due to image forces lowering of the barrier height.

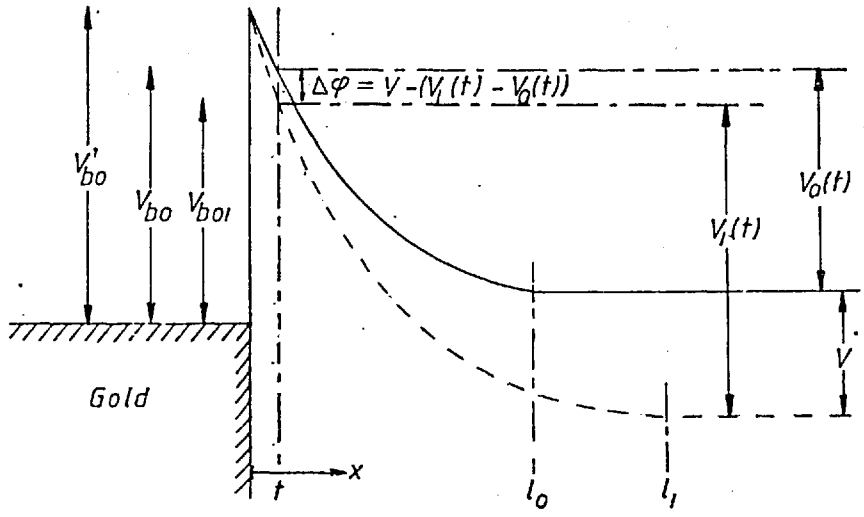


Fig. 5.5 Energy band diagram of a Schottky barrier with a damaged interfacial layer; (full line) zero bias, (dash line) reverse bias.

From eqn. (5.2) the intercept on the y-axis should give the saturation current. The value is 1.2×10^{-7} A ($.154$ A m^{-2}).which corresponds to a barrier height of 0.71 eV. This is the barrier height at zero field, i.e. zero diffusion potential and therefore is higher than the one obtained with the forward bias current.

Despite the reasonable parameters obtained, one should bear in mind that the reverse bias I-V characteristics have always been difficult to explain. The only Schottky barrier which was conclusively shown to obey the image-force effect was made by Arizumi and Hirose[4]. In most cases, other effects have to be taken into account. Indeed, as Hill and Coutts[5] pointed out, it is inappropriate to presume a constant power factor ($\frac{1}{4}$ in this case) in such logarithmic plots. Therefore an attempt will be made to fit the data in an alternative way. It is still assumed that the excess reverse current observed was due to barrier height lowering, which of course may not be true. Eqn. (5.2) is then used to find out how this barrier height varies with V. By plotting log $[I/(1 - \exp(-\beta V))]$ vs V, a straight line with a small but finite slope is obtained at small V (see Fig. 5.2). This shows that $\Delta\phi$ is proportional to V, as was assumed in the forward bias characteristics discussed previously. The intercept on the y-axis gives the value of I_s. This is equal to 1.32×10^{-6} A which is the same as was obtained in forward bias. With this value of I_s, the variation of $\Delta\phi$ with V

at higher voltage can be found by using eqn. (5.2). The result shows that $\Delta\phi \propto V^{\frac{1}{2}}$ when $V > 6$ volts. So, the relationship is such that at low bias, $\Delta\phi \propto V$; and at high bias, $\Delta\phi \propto V^{\frac{1}{2}}$. In order to explain this, the argument proceeds as follows.

Since the silicon surface has been bombarded with high energy atoms/ions during the sputter deposition process, it is not unreasonable to assume that a damaged surface layer is created. This surface layer should be quite leaky, i.e. carriers (electrons) can flow through it easily by whichever means the good forward I-V characteristics require.. Let this layer be of thickness t. The band diagram is as shown in Fig. 5.5 (full line). It is also assumed that the space charge potential V(x), being supported by donor impurities, has not been altered even within the damaged layer. However, since the layer is conductive, electrons need only have to surmount a potential of V_{bo} rather than V'_{bo} in order to cross the barrier. When a reverse bias V is applied, the energy diagram can be drawn as shown in dashed line in Fig. 5.5. Clearly, V_{bo} has been decreased by $\Delta\phi$ given by

$$\Delta\phi = V - (V_l(t) - V_o(t)) \tag{5.4}$$

From eqn. (2.22) then $V(x) = K(\ell - x)^2$ where $K = qN/2\varepsilon_s = 1.303 \times 10^{12}\ Vm^{-2}$. Thus these give

$$V_{bi} = K\ell_o \quad \text{and} \quad V_{bi} + V = K\ell_l$$

At $x = t$, $V_o(t) = K(\ell_o - t)^2$ and $V_1(t) = K(\ell_1 - t)^2$

Therefore $V_1(t) - V_o(t) = K[(\ell_1 - t)^2 - (\ell_o - t)^2]$

$$= K[\ell_1^2 - \ell_o^2 - 2t(\ell_1 - \ell_o)]$$

$$= V - 2tK\left[\left(\frac{V + V_{bi}}{K}\right)^{\frac{1}{2}} - \left(\frac{V_{bi}}{K}\right)^{\frac{1}{2}}\right]$$

$$= V - 2t(KV_{bi})^{\frac{1}{2}}\left[\left(1 + \frac{V}{V_{bi}}\right)^{\frac{1}{2}} - 1\right]$$

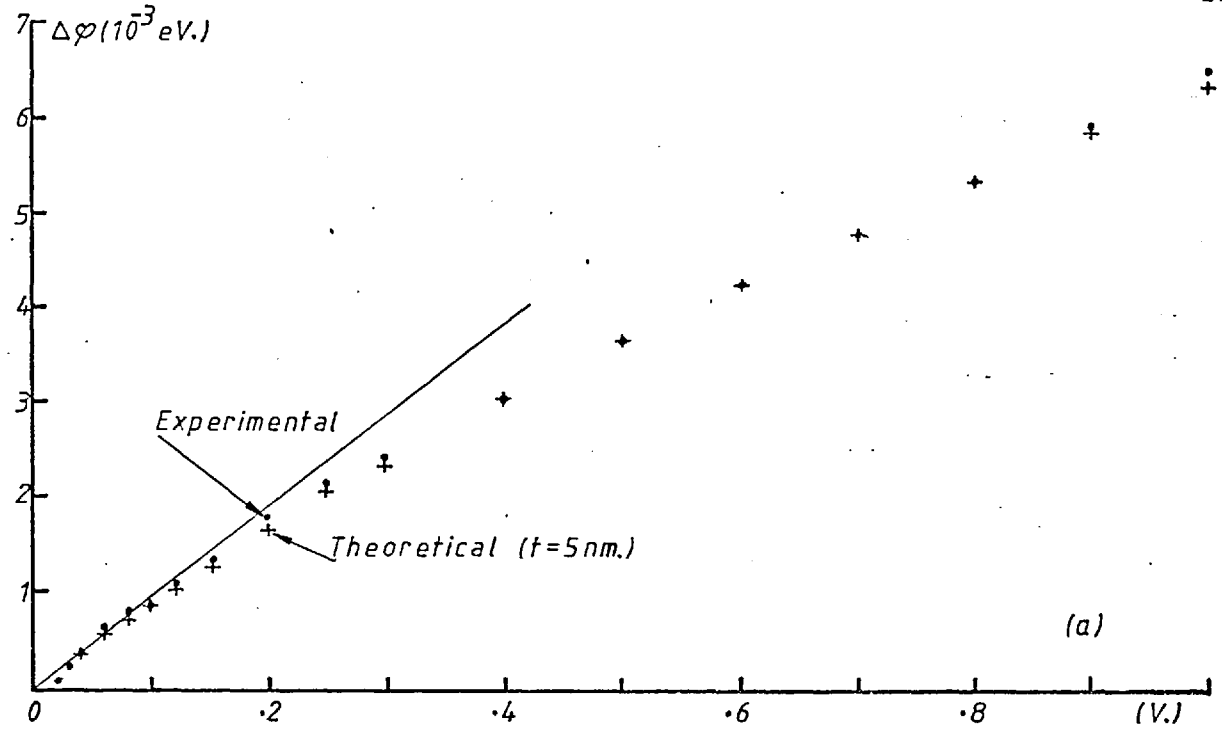
so the change in barrier height $\Delta\phi$ is, from eqn. (5.4),

$$\Delta\phi = 2t(KV_{bi})^{\frac{1}{2}}\left[\left(1 + \frac{V}{V_{bi}}\right)^{\frac{1}{2}} - 1\right] \qquad (5.5)$$

when $V << V_{bi}$,

$$\Delta\phi = t\left(\frac{K}{V_{bi}}\right)^{\frac{1}{2}} V \qquad (5.6)$$

From eqn. (5.6) the thickness t can be deduced from the experimental plot of $\Delta\phi$ vs V, the slope of which is found to be 0.0091 (Fig. 5.6a). Using $K = 1.304 \times 10^{12}\ Vm^{-2}$ and $V_{bi} = 0.39$ eV, t is found to be 5.0 nm at low bias. Actually the value of V_{bi} should be the build-in intrinsic diffusion potential $(V'_{bo} - V_n)$, i.e. one that is not lowered by any barrier height lowering mechanism. But this cannot be determined so the value of 0.39 eV (eqn. (5.3)), which is the value of $V_o(t)$ as shown in Fig. 5.5, is used. Nevertheless, the



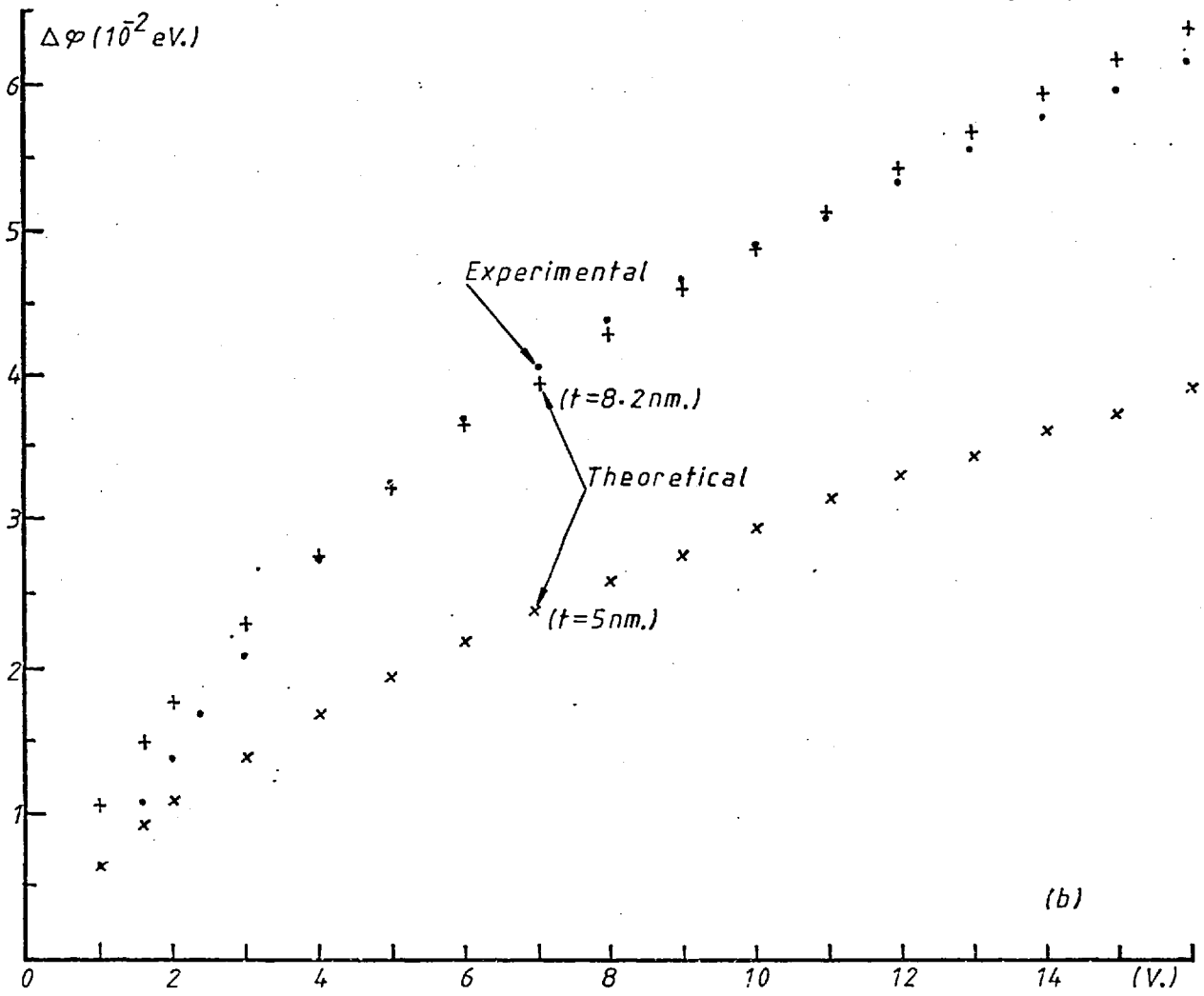


Fig. 5.6 Barrier height lowering effect of the damaged contact layer of a Schottky barrier. (a) low bias, (b) high bias.

precise value of V_{bi} used would not seriously affect the general behaviour of $\Delta\phi$. Knowing the value of t, eqn. (5.6) is then used to calculate $\Delta\phi$ vs V. This is displayed in Fig. 5.6b which shows large deviations at V > 2 volts. In fact it is found that t has to be increased to 8.2 nm in order to fit the value of $\Delta\phi$ at higher V. As shown in Fig. 5.6b the damaged layer thickness seems to have increased from 5.0 nm to 8.2 nm by the high electric field when the applied bias increases from 1.5 to 3 volts. Substituting $\Delta\phi$ from eqn. (5.5) with t = 8.2 nm into eqn. (5.2), I is plotted against V in Fig. 5.3 to compare with the raw data.

5.2.2 C-V Characteristics

The C-V characteristics are plotted in Fig. 5.7 as C^{-2} vs V. In accordance with eqn. (2.48), straight lines are obtained. However, the slopes are frequency dependent. This is not consistent with eqn. (2.48) which is derived by assuming that the capacitance is due only to the ability of the majority carriers (electrons) to follow the measuring signal. The frequency dependent behaviour therefore indicates the presence of deep traps which are also able to follow the signal. This is possible if the energy gap is filled with distributed traps which are positively charged when empty of electrons[6]. At high reverse bias (Fig. 5.8c) and high frequency so that the trapping states cannot follow the signal, the slope of the C^{-2} vs V plot approaches $2/q\varepsilon_o\varepsilon_s(N + N_t)$

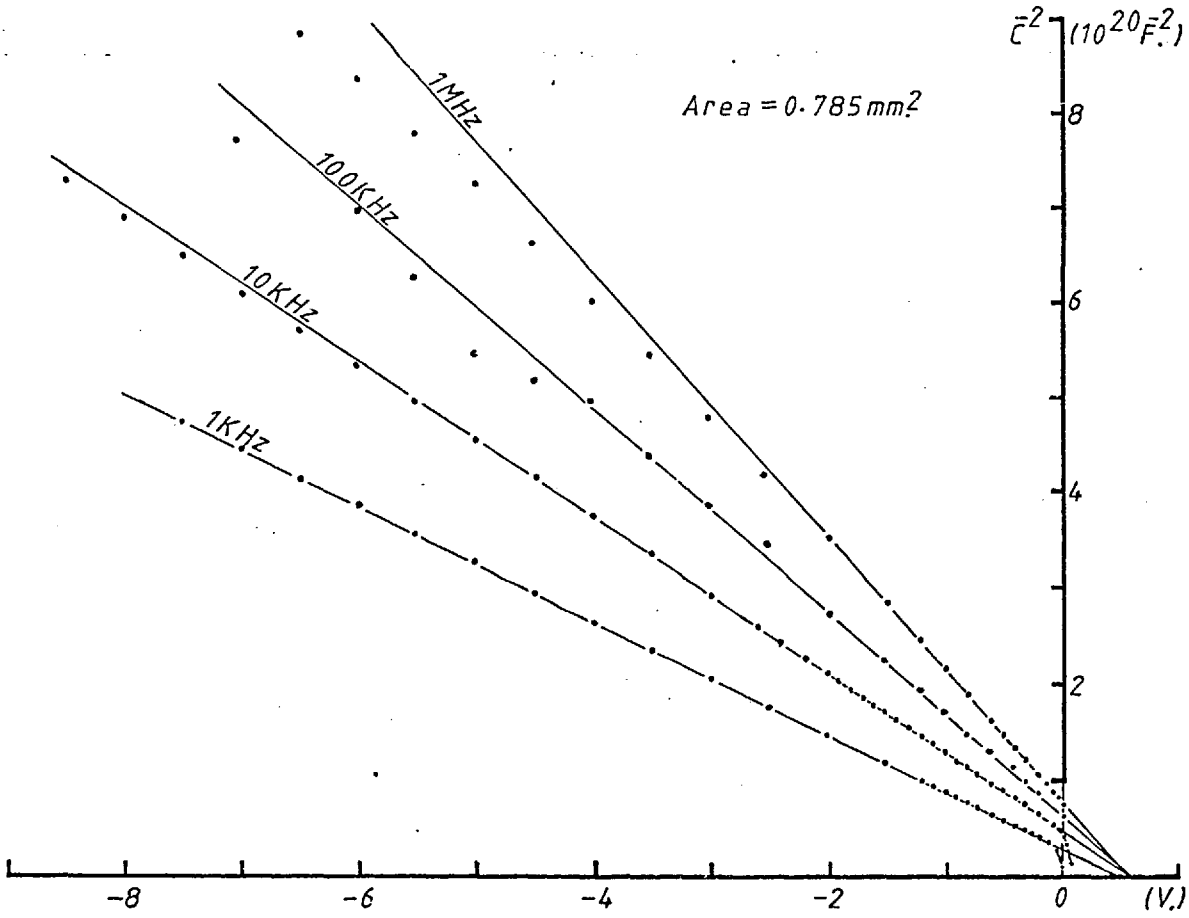


Fig. 5.7 C—V characteristics of a sputtered Au—Si contact.

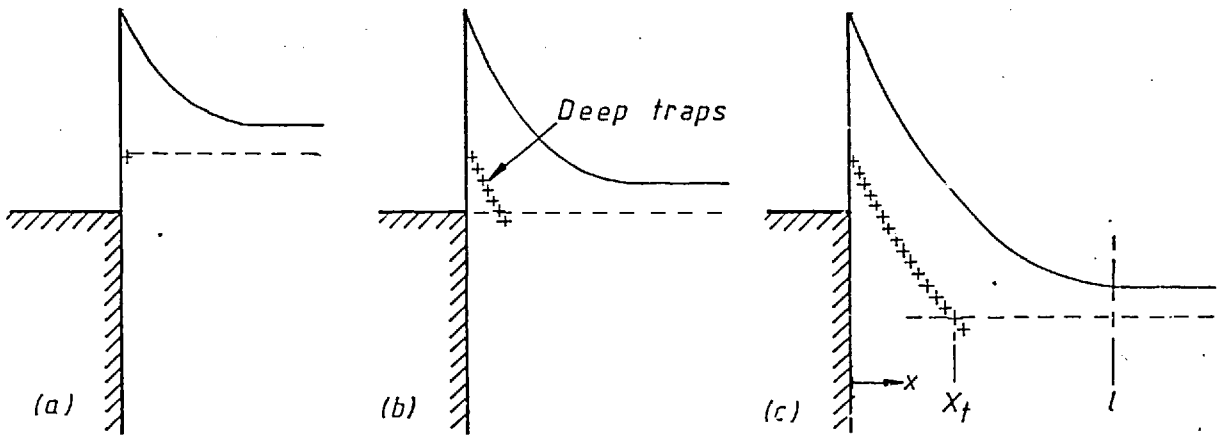


Fig. 5.8 Effects of deep traps in the space charge region. (a) forward bias, (b) zero bias, (c) revers bias.

where N is the donor density and N_t is the net positively charged trapping density. At small reverse and forward bias,(Fig. 5.8a),N_t decreases to zero so that the charge density obtained from the slope approaches the doping density. At lower frequency, some of the traps are able to follow the signal so that 'the other plate' of the capacitor is no longer located at ℓ, the edge of the space charge region, but is in between ℓ and x_t where x_t is the position where the trapping states (assuming, for the purpose of illustration, that there is just this single energy level of traps) cut the quasi-Fermi level. (Fig. 5.8c)[7]. Consequently, the observed capacitance increases with decreasing frequency at any particular reverse bias voltage. But since this frequency variation is slow and nearly as the square root of logarithm, it is likely that there is a wide distribution of trapping energy. At low frequency and near zero bias, the response of slow traps, probably in the damaged surface layer, give rise to a very large increase in measured capacitance. The effective net donor density can be calculated from the slopes of these plots according to eqn. (2.48). They are found to vary logarithmically from 3.27×10^{21} to 1.4×10^{21} m^{-3} for the frequency range from 1 KHz to 1 MHz respectively. It is seen that the high frequency value is near the value of 1.7×10^{21} m^{-3} quoted by the supplier. The intercepts of these lines on the V-axis give the values of $(V_{bi} - kT/q)$ from which the barrier

height $V_{bo} = V_{bi} + V_n$ may be deduced. The value of V_{bi} fluctuates from 0.48 to 0.56 eV depending on the frequency used. There is now an ambiguity in the value of V_n since the effective donor density is a function of the frequency. In Table 5.2, the value of V_n is calculated according to the expression $N = N_c \exp(-\beta V_n)$ where N is obtained from the slope at that frequency. It shows that the barrier height deduced varied from 0.71 to 0.81 eV.

Table 5·2

Freq (Hz.)	N ($10^{21} m^{-3}$)	V_{bi} (eV.)	V_n (eV.)	V_{bo} (eV.)
1K	3.27	0·48	0·234	0·71
10K	2·30	0·50	0·243	0·74
100K	1·81	0·56	0·249	0·81
1M	1·34	0·52	0·257	0·78

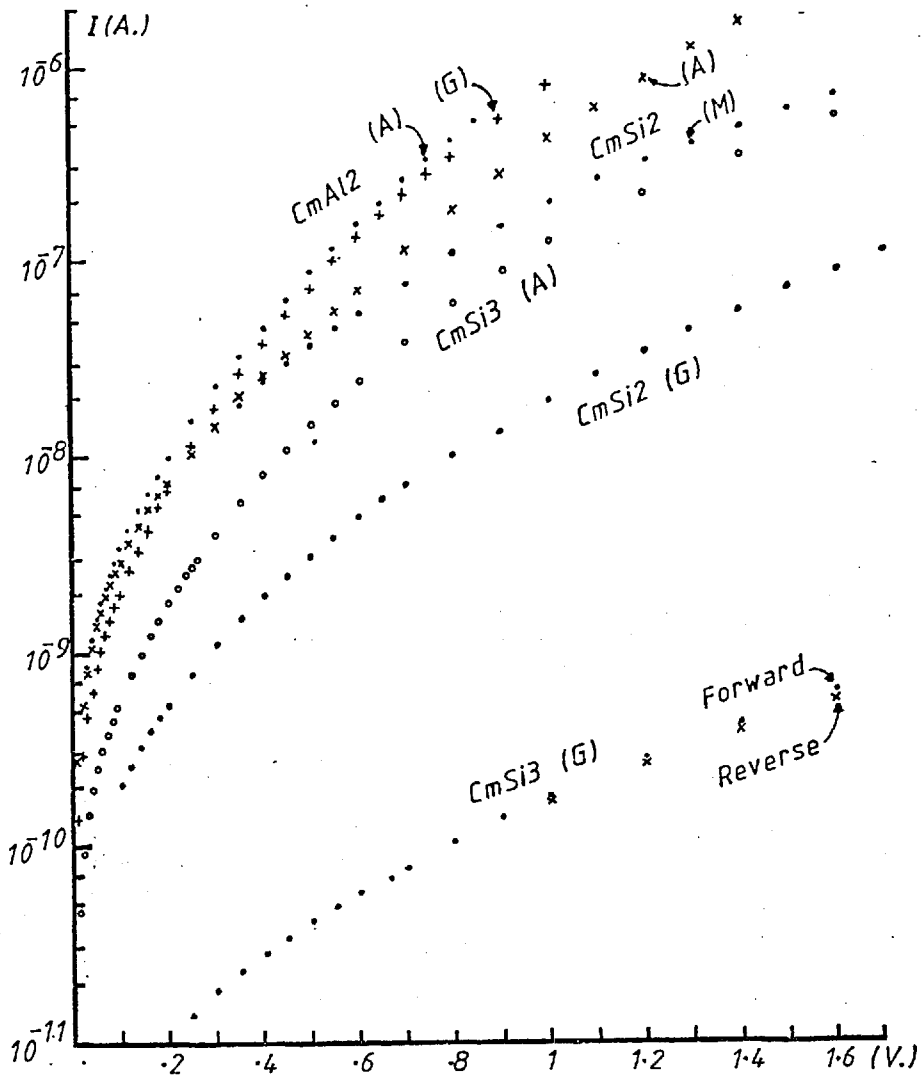


Fig. 5.9 Forward bias I–V characteristics of some Au/cermet/Si samples.

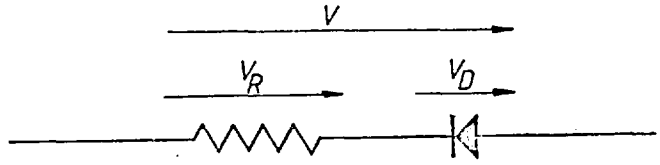


Fig. 5.10 Equivalent circuit of a Au/cermet/Si sample.

5.3 GOLD-CERMET-SILICON STRUCTURE WITH CONDUCTIVE CERMET

As mentioned in the Synopsis (chapter 1), samples of this configuration can be classified into two categories: (a) conductive if the current flowing through it, at a bias voltage of several kT but before breakdown of the cermet, is greater than the effective saturation current of the silicon/cermet interface barrier, and (b) insulating if otherwise. The labelling of the samples is listed in Table 5.1.

5.3.1 I-V Characteristics

The forward bias I-V curves of sample CmSi2 for dots A, G, M are plotted in Fig. 5.9. From these curves it is clear that the barrier height cannot be obtained directly as with the case of Au-Si Schottky barriers. A large portion of the applied voltage is dropped across the cermet. To correct for this it is necessary to know accurately the I-V characteristics of the cermet alone. This cannot be measured on the same dot. Therefore another sample CmAℓ2 consisting of Au/Cermet/Aℓ on glass was prepared with similar sputtering parameters as with CmSi2. The I-V curves of the corresponding dots A and G are then plotted on the same graph (Fig. 5.9). Assuming that these two samples have identical cermet thicknesses and electrical properties, and that sample CmSi2 can be represented by a circuit shown in Fig. 5.10, where V_R and V_D represent the voltages

dropped across the cermet and cermet/Si junction respectively, then in principle it should be possible to extract the I-V characteristics of the junction alone. However, since a rather large portion of the total voltage V is dropped across the cermet, the error in V_D thus obtained would be too high to give meaningful results. Furthermore, the current characteristics for different dots but with the same cermet metal fraction and on the same sample is found to vary by a factor of about three or more. The variations for different samples can be more than an order of magnitude. Therefore it is considered inappropriate to deduce the barrier height from the forward bias I-V characteristics.

The reverse bias I-V characteristics are shown in Fig. 5.11. It is seen that the currents appear to saturate only when the bias voltages are greater than about one volt. This differs greatly from the case with pure gold contact where current saturation occurs at about 0.1 volt. (Fig. 5.2). The reason is that below one volt the current is limited by the cermet, i.e. the dc resistance of the cermet is greater than that of the reverse biased gold/cermet interface, as will be shown later in this chapter. But as the bias voltage increases, the cermet current increases (cermet resistance drops) virtually exponentially whereas the barrier (interface) current tends to saturation. So, eventually the current is limited by the barrier. Furthermore, the apparent saturation currents of all the dots are about an order of

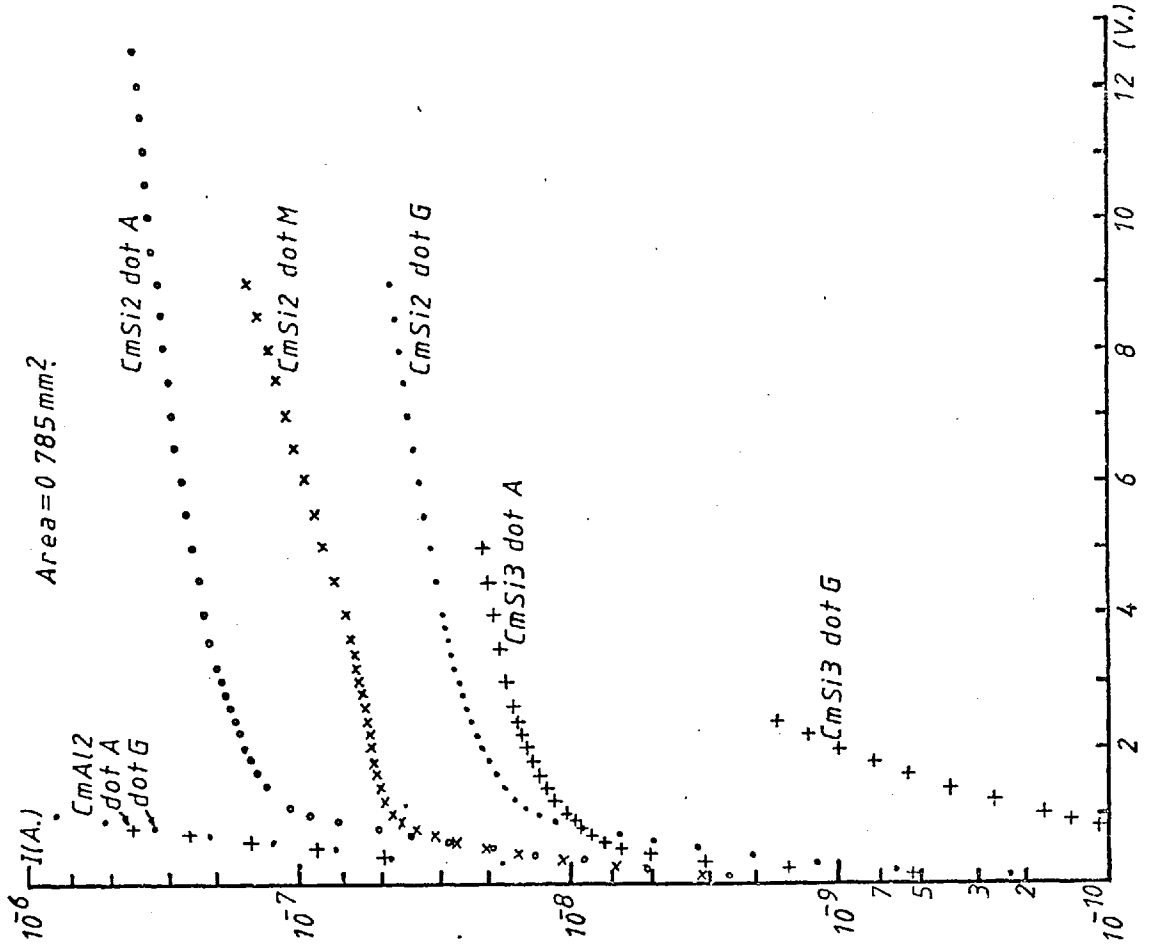


Fig. 5.11 Reverse bias I–V characteristics of some Au/cermet/Si samples.

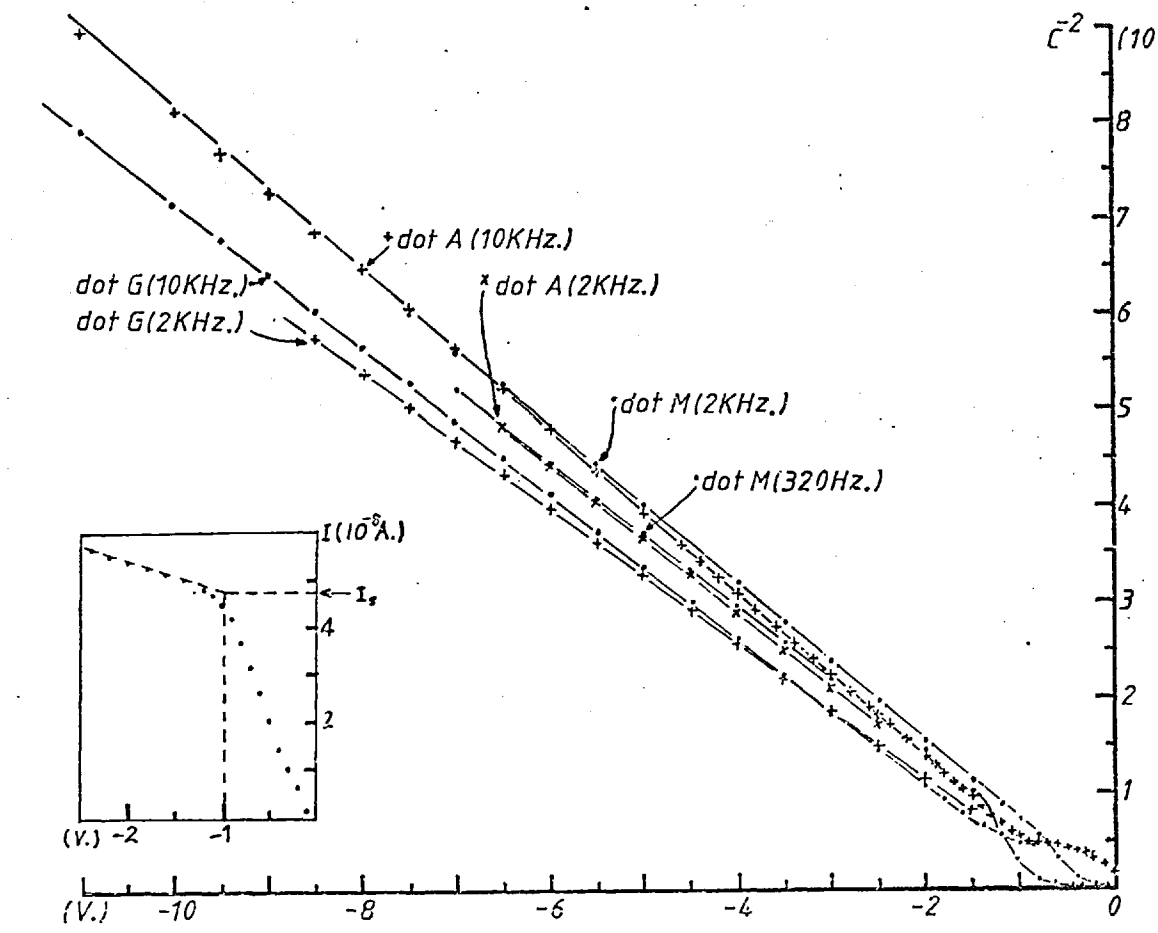


Fig. 5.12 C–V characteristics of a Au/cermet/Si sample (CmSi2).

magnitude less than that of pure gold contact shown in Fig. 5.2. These give barrier heights of between 0.7 and 0.75 eV compared with 0.64 eV with pure gold contact. This apparent increase of barrier height may be due to the fact that since a large portion of the contact area is between SiO_2 and Si, the barrier heights would be more likely to be determined by the interface states between SiO_2/Si rather than that of Au/Si. Also, most of the current crossing the interface would concentrate on the metal islands rather than the SiO_2 which are in contact with the silicon. This results in a reduction of the effective area in contact, which has not been allowed for in calculating the barrier heights.

5.3.2 C-V Characteristics

The C^{-2} against V curves of sample CmSi2 at reverse bias are shown in Fig. 5.12. It is seen that the slopes of these plots at different frequencies did not vary as much as those of the pure Au-Si contacts described in section 5.2.2. Furthermore, the capacitance remained fairly constant until the bias voltage was greater than about one volt. This latter observation is consistent with the I-V characteristics for which we argued that if the applied reverse voltage V was below one volt, it dropped mainly across the cermet. But when V was greater than about a volt, any further

increase in V would drop mainly across the depletion region of the silicon surface. Effectively this means that the reverse bias characteristics of the space charge region was being translated by about one volt along the V-axis. In order to find the diffusion potential V_{bi} accurately, it is necessary to know this translated voltage V_m to the same degree of accuracy. This means that the I-V characteristics of the cermet need to be known precisely. Unfortunately, as discussed above, this cannot be achieved. However, the fact that Fig. 5.12 shows linear increase of C^{-2} at V greater than a volt means that the voltage V' dropped across the space charge region must be increasing proportionally to the applied voltage V, i.e. $V' = KV$ where K is a constant. The slope would then have to be divided by K in order to calculate the net donor density. On comparison of the I-V characteristics of samples CmSi2 and CmAℓ2 as shown in Fig. 5.11, one realises that when V is greater than about a volt, the current of CmAℓ2 increases so rapidly compared with that of CmSi2 that K can be treated as unity, i.e. any further increase in bias voltage is dropped completely across the space charge region. Consequently, the extrapolated intercept V_i on the V-axis is given by

$$V_i = V_m + V_{bi} - kT/q$$

The value of V_m can be obtained approximately from the 'turning' point of the linear I-V plot of the dot. An example of this (for dot M) is shown in the insert of Fig. 5.12. This interpretation is strictly correct only if the 'Schottky' barrier is ideal, i.e. shows good current saturation. Knowing V_{bi}, one can then calculate the barrier height V_{bo} from $V_{bo} = V_n + V_{bi}$. The value of V_n is obtained from the net donor density which, from the slopes of these plots, is about 2.4×10^{21} m^{-3}. This gives $V_n = 0.242$ eV. The results are tabulated in Table 5.3. Also given are values of V_{bo} using the apparent saturation current I_s taken at V_m of the reverse I-V characteristic and using eqn. (2.44). The area used is that of the gold dot, i.e. 0.785 mm^2.

Similar plots of C^{-2} vs V for sample CmSi3 are shown in Fig. 5.13. This sample is only half as thick as CmSi2 and has a smaller metal fraction in the cermet (see Table 5.1). Clearly the curve for dot A is similar to that of dot M of CmSi2, except that the transition voltage V_m is about halved. But as the metal fraction decreases, the curves (dots G and M) exhibit increasing departure from linearity. The reason is that with decreasing metal fraction, a greater proportion of the applied voltage is dropped across the cermet while at the same time the current also decreases. As shown in Fig. 5.9, the conductivity of CmSi3 dot G is more than two decades less than that of CmSi2. The current at all bias voltages, except when cermet breakdown occurs, is less than the

Table 5·3

Sample CmSi2	Freq. (Hz.)	V_i (eV.)	V_m (eV.)	V_{bo}(C–V) (eV.)	I_S (10^{-8}A.)	V_{bo}(I–V) (eV.)
dot A	10K	−0·40	−1·1	0·97	13·0	0·70
dot A	2K	−0·27	−1·1	1·10	13·0	0·70
dot G	2K	−0·12	−1·0	1·15	1·5	0·76
dot G	320	−0·12	−1·0	1·15	1·5	0·76
dot M	10K	−0·55	−0·9	0·62	4·8	0·73
dot M	2K	−0·36	−0·9	0·81	4·8	0·73

$N = 2{\cdot}4 \times 10^{21}\ m^{-3}$.
$V_{bi} = 0{\cdot}242$ eV.

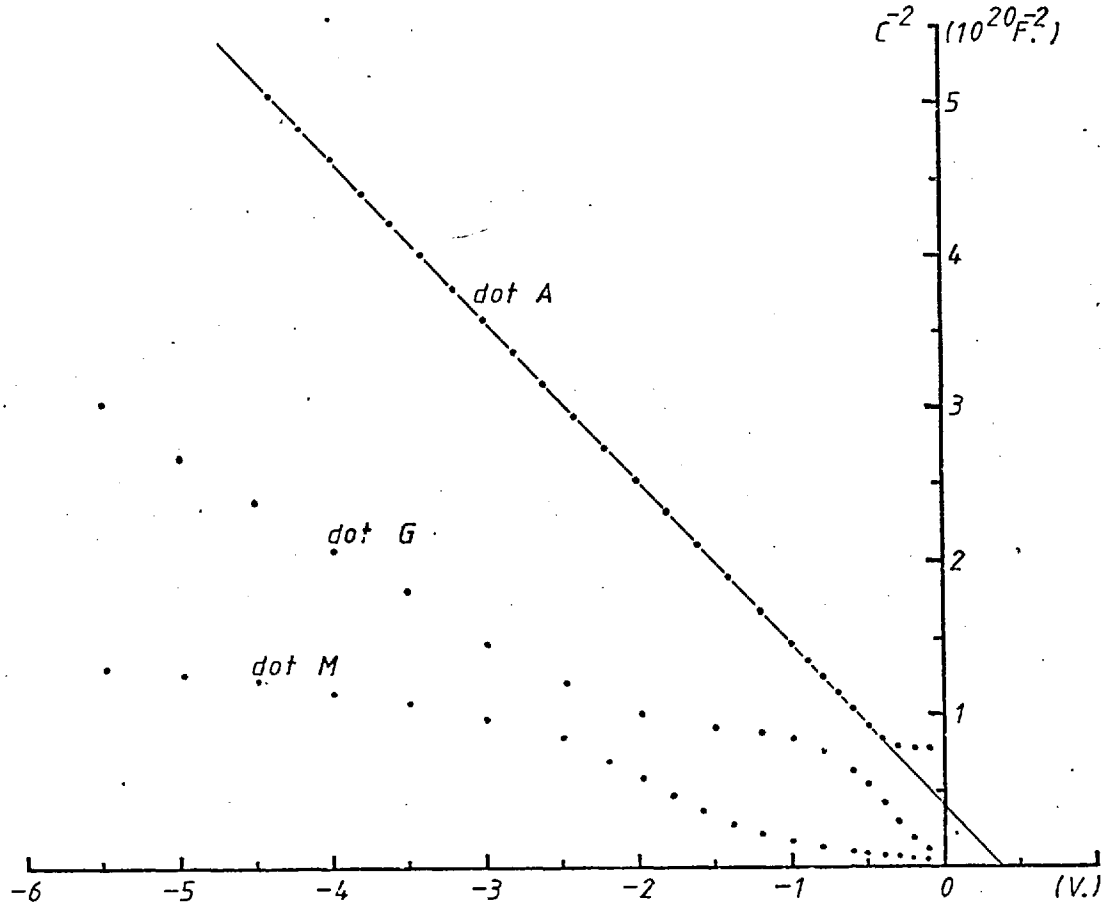


Fig. 5·13 C–V characteristics of a Au/cermet/Si sample (CmSi3) at 20KHz.

apparent saturation current of the barrier. It also exhibits symmetrical I-V characteristics for both bias directions up to 1V, showing that the current is limited mainly by the cermet resistance. Now, since the current I flowing across the space charge region is by drift and diffusion, it is given by $I = qn\mu dE_{Fn}/dx$ for the electron carriers. So when the current is small dE_{Fn}/dx would be small, i.e. the quasi-Fermi level across the space charge region bends only by a small amount from its equilibrium position. The system therefore behaves more as a MIS device than as a Schottky barrier. But since the silicon surface is highly damaged, it is not unreasonable to assume that there is an extremely high interfacial state density at the cermet/silicon interface. This results in the electron quasi-Fermi level at the interface being pinned irrespective of the electric field in the cermet. This feature was discussed in chapter 2. Consequently the diffusion potential in the space charge region need only change roughly by as much as the bending of the quasi-Fermi level. The situations for sample CmSi3 dots A and M can be illustrated with the energy diagrams shown in Fig. 5.14. The depletion capacitance of dot M remains virtually constant at high reverse bias and is greater than that of dot A since $C_d = \varepsilon/\ell$ and ℓ, the depletion width, increases with bias for dot A but remains constant for dot M. This effect is reflected in the measured capacitance which is a series combination of C_d and C_c, the cermet capacitance. From these

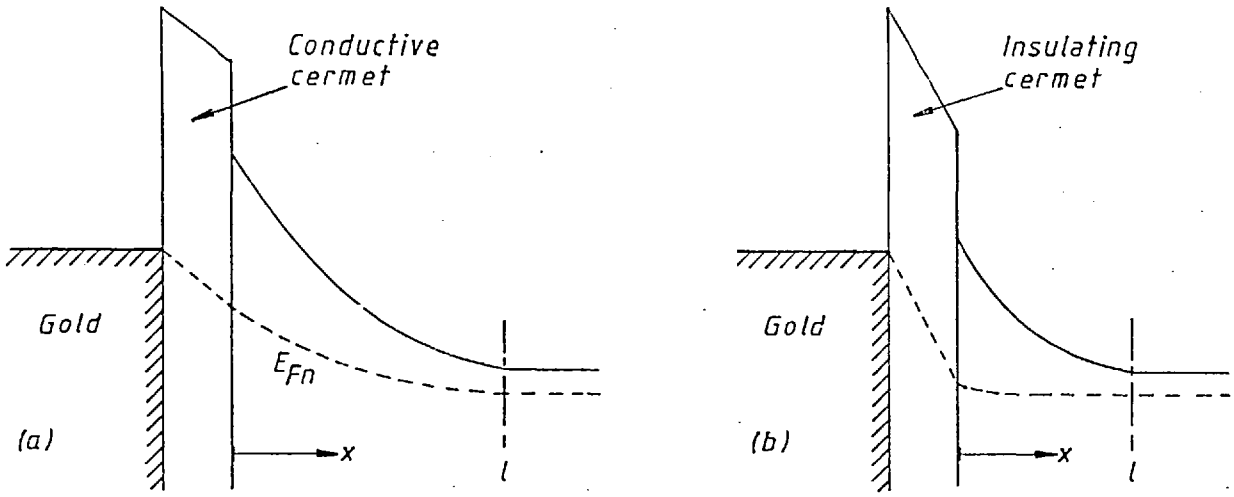


Fig. 5.14 Energy band diagrams of Au/cermet/Si samples under reverse bias.

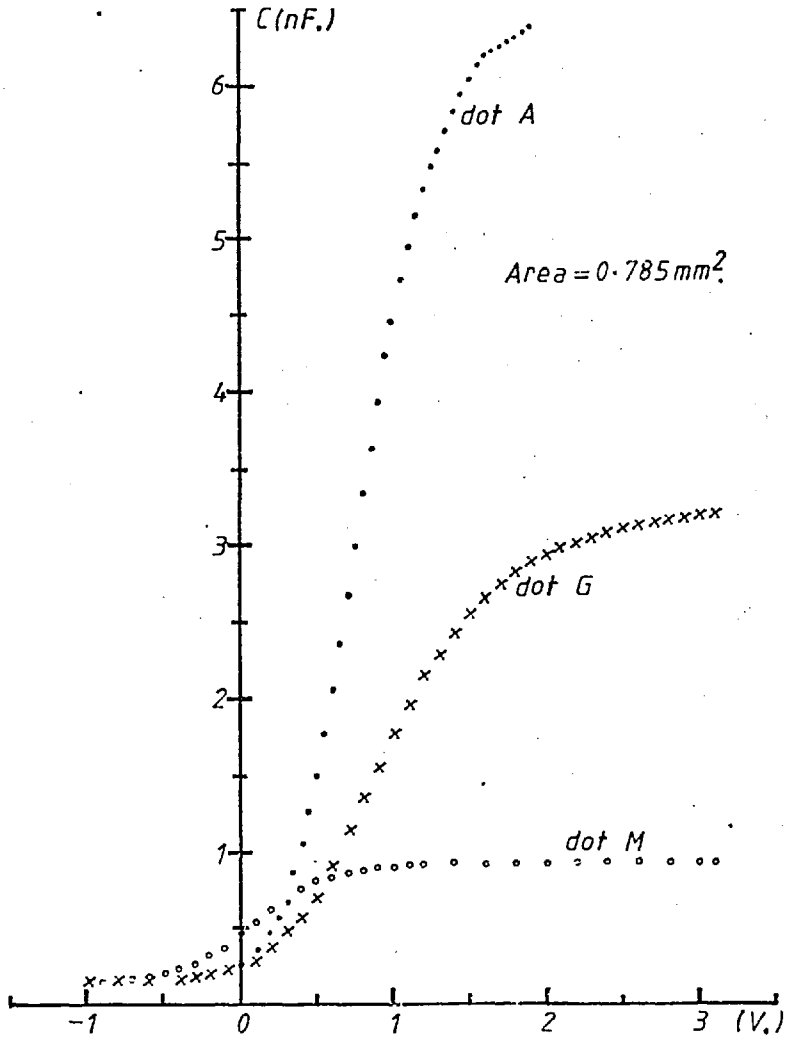
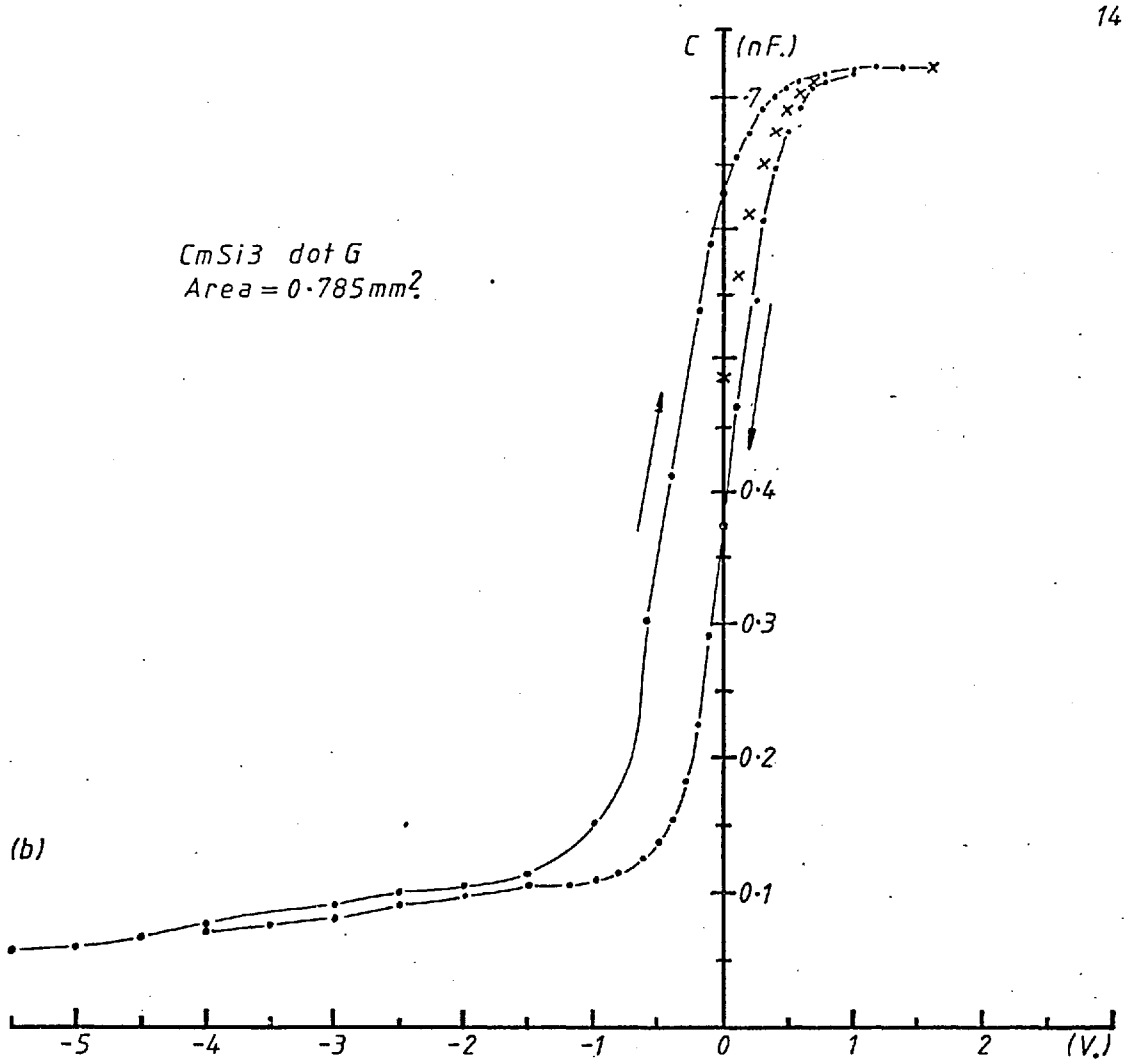


Fig. 5.15a C – V characteristics of a Au/cermet/Si sample (CmSi2) at 10 KHz.



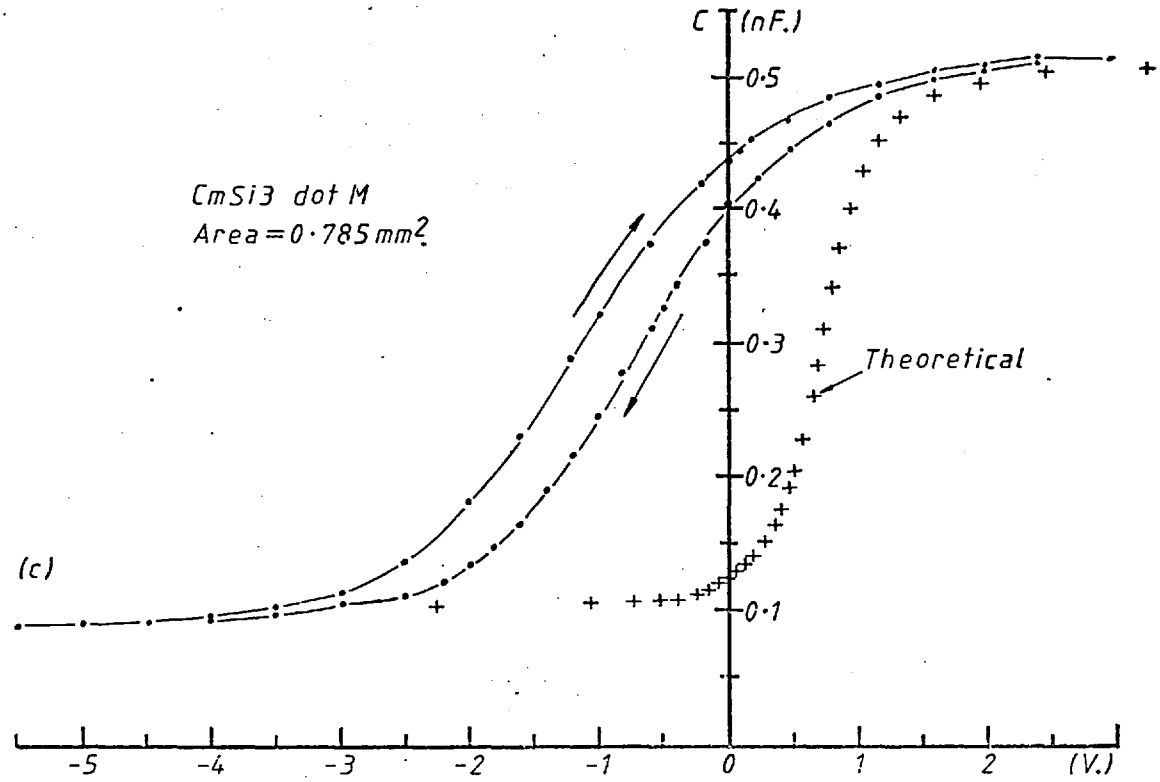


Fig. 5·15b,c C–V characteristics of a Au/cermet/Si sample (CmSi3) at 20KHz.

discussions, it therefore seems appropriate to consider dot G of sample CmSi3 as a 'transition' dot. The metal fraction in the cermet of this dot is about 0.4. Thus, those cermets with metal fraction less than 0.4 are termed conductive since the current flow due to an applied voltage is enough to cause appreciably large band bending of the semiconductor space charge potential. For those with smaller metal fraction, the space charge potential remains virtually constant even under fairly high applied bias and hence are termed insulating.

So far, we have only discussed the C-V characteristics in the reverse bias region. The complete linear C-V plots of these devices are shown in Fig. 5.15. It is apparent that they differ markedly from those of ordinary Schottky diodes, especially in the forward bias region which appears much more similar to that of the conventional MIS devices. With such devices, it is possible to bend the diffusion potential downwards with a high forward bias voltage so that free electrons can accumulate at the semiconductor surface. The measured capacitance would then approach the insulator capacitance. Later in this chapter it will be shown that, within the accuracy of measurement, the capacitance at high forward bias approaches the cermet capacitance, but the true mechanism responsible for this behaviour is uncertain. This is especially so for the insulating samples, in which we argued in the previous paragraph that the space charge

potential may not be so easily bent. Other mechanisms at the interface which may respond to the signal are minority carriers (when the surface is inverted) and charged traps. As shown in Fig. 5.7, the capacitance of a pure gold-silicon Schottky barrier may increase to a very high value at near zero bias even though a thick depleted space charge region is definitely present there. We attributed that behaviour to the response of traps in the damaged surface layer. More discussions on this will be given in a later section on insulating samples.

Table 5.4 shows the cermet capacitance C_o as estimated from the high forward bias value. The effective dielectric constant ε' of the cermet is calculated using the parallel plate formulae $\varepsilon' = C_o t/A\varepsilon_o$ where t and A are the cermet thickness and the area of the gold electrode respectively. The rather large uncertainties in estimating the cermet thickness (see chapter 4, section 4.8) imposes a rather high uncertainty on ε'. Despite this, the results obtained are enough to show that the cermet capacitance increases (ε' increases) with increasing metal fraction and decreases with increasing frequency. These are in accordance with the properties of cermets shown in Fig. 3.9a.

Another interesting feature of the curves shown in Fig. 5.15b and c is the hysteresis effect. This effect is most prominent for dots in the 'transition' region. Since C-V measurements made on cermet samples (Aℓ/cermet/Au)

Table 5·4

Sample	Thickness t (nm.)	Freq. (Hz.)	C_o (pF.)	$\varepsilon' = \frac{C_o t}{A\varepsilon_o}$
CmSi2				
dot A	160	10K	6800	160
dot G	145	10K	3250	68
dot M	125	130	1720	31
dot M	125	230	1500	27
dot M	125	10K	930	17
CmSi3				
dot A	85	20K	1000	12
dot G	75	20K	730	7·9
dot M	70	20K	520	5·2
CmSi4				
dot M	105	230	312	4·7
dot M	105	800	307	4·6
dot M	105	2K	301	4·5
dot M	105	20K	280	4·2
dot M	105	200K	275	4·2

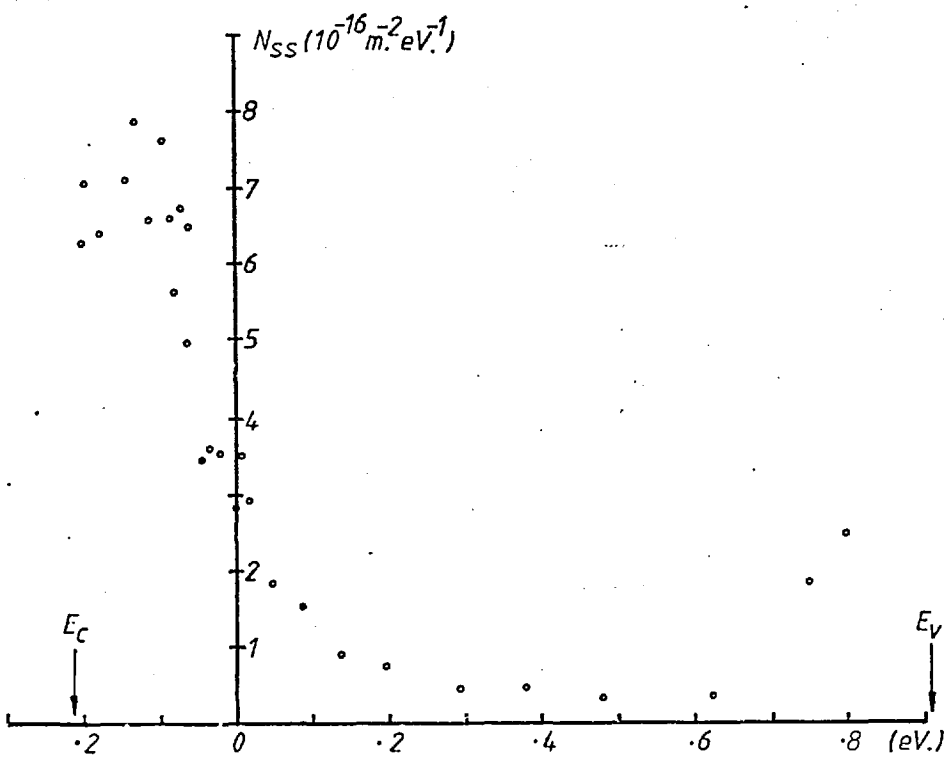


Fig. 5·16 The interface state density of a Au/cermet/Si sample (CmSi3 dot M).

showed that the capacitance is independent of the dc bias voltage (Fig. 5.19),one can therefore conclude that the effect is not due to the intrinsic properties of the cermet; nor can it be due to that of silicon space charge region since there is no hysteresis effect in the C-V measurements with Au-Si samples. It is therefore a consequence of depositing a cermet on the surface of the silicon. Also, at any fixed bias voltage, the capacitance may take more than five minutes to settle down to its constant value. The arrows put beside the loops in Fig. 5.15b and c indicate the direction of change in dc bias voltage. All samples showed that the zero bias capacitance became higher after a reversebias than after a forward bias voltage was applied, i.e. the loops go in a clockwise direction. This zero bias capacitance never crept back to its origin virgin value (i.e. the value when the sample was first measured before any bias voltage had been applied) even when it was left un-biased for a week.

5.4 GOLD-CERMET-SILICON STRUCTURE WITH INSULATING CERMET

5.4.1 The Characteristics of the Cermet-Silicon Interface

The similarities between the C-V curves of samples with insulating cermets and those of MIS structures led us to believe, at first, that the devices could be characterised using the C-V technique as outlined in section 2.4. The following analysis shows that this approach is not self-consistent. An ideal C-V curve for a trap-free MIS structure was computed using the following parameters which are suitable for comparison with dot M of CmSi3: insulator capacitance C_o = 0.52 nF; donor density N = 2.47 x 10^{21} m^{-3}; difference in work functions between gold and silicon V_{ms} = 0.8 eV[8]. The actual value of V_{ms} used is not important since it would not seriously affect the final conclusions. The result is plotted in Fig. 5.15c. The difference between this and the measured values was assumed to be due to the presence of interfacial states. By assuming that these states could not follow the signal frequency (20 KHz) their densities could then be deduced. This was done for the curve with negative-going bias voltage. Fig. 5.16 shows the interfacial state density N_{ss} plotted against energy in the silicon gap. This plot is remarkably similar to those of published data[9]. Since this analysis requires that the Fermi level at the interface is able to 'scan' across the whole energy gap with the external bias voltage, it means

that the interfacial state density has to be quite low. This is the case shown in Fig. 5.16. At the middle of the gap, $N_{ss} \sim 5 \times 10^{15}$ m^{-2} eV^{-1} and using eqn. (2.36), it shows that the surface potential V_s would be able to change by 0.4 volts per volt of applied bias. However this low value of interfacial state density does not seem to be very consistent with the general expectation that the silicon surface has been extensively damaged. In order to clarify this point, three silicon wafers of MIS structure were made with the cermet replaced by pure SiO_2 deposited using the same sputtering procedures. Typical C-V measurements are as shown in Fig. 5.17. All curves remain virtually constant showing that the space charge potential is hardly changed by the bias voltage. This indicates the presence of an extremely high interfacial state density. As described in section 2.4 eqn. (2.40), the change in space charge potential with bias may be found from dc capacitance measurements, or at frequency so low that all interfacial traps are able to follow. This was done with a circuit as shown in Fig. 5.18. The ramp generator was a simple integrator constructed with a 741 operational amplifier. The high input impedance operational amplifier was a Keithley-602 electrometer used in the fast mode, with a feedback resistor R equal to 10^{11} Ω. The output voltage V_o is given by $V_o = - \alpha CR$ where the input voltage ramp rate α was 0.005 Vs^{-1}. The capacitance of the MIS device at

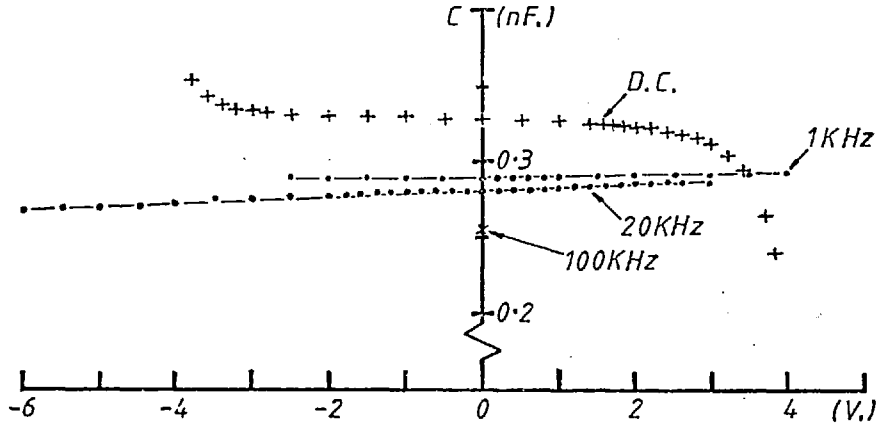


Fig. 5·17 C–V characteristics of a MIS sample with a sputtered insulator.

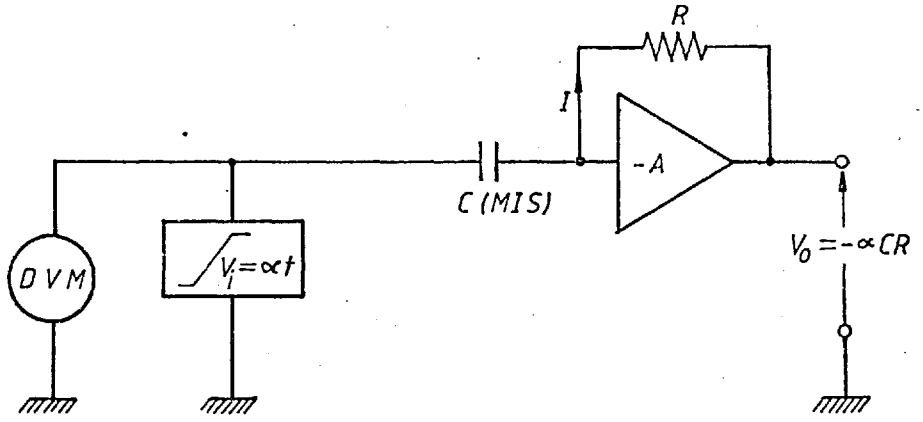


Fig. 5·18 Circuit used to measure the d.c. capacitance of MIS samples.

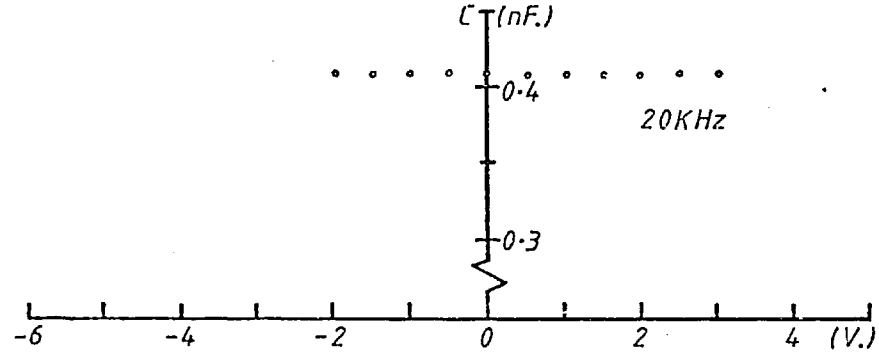


Fig. 5·19 C–V characteristics of a Au / cermet / Al sample.

any time can thus be calculated. The bias voltage at that moment is equal to V_i since the input of the electrometer is a virtual earth. The result is shown in Fig. 5.17. The slight variations in C with V can be completely accounted for by the dc leakage of the SiO_2 insulator. This can be checked by switching the ramp generator into hold mode ($\alpha = 0$) and V_o would then give the leakage current ($I = V_o/R$). It is found that I increases rapidly when V_i is greater than about 3 volts. At $V_i = 4$ volts, $I = 4 \times 10^{-13}$ A. This correponds to a SiO_2 resistivity of about 10^{14} Ωm, and is at least an order of magnitude smaller than that at lower voltages. It can therefore be concluded that the space charge potential of the silicon surface remains virtually fixed irrespective of the bias voltage. Also, from the equivalent circuit of a MIS structure in Fig. 2.7, when C_{ss}, the interface state density, is very high, the measured dc capacitance approaches the insulator value. This is observed as seen in Fig. 5.17. Another possibility for it to approach the insulator value is that inversion occurs at the silicon surface so that the accumulation of holes also presents a high capacitance shunted across the space charge region. Finally, to make certain that the bias dependent capacitance of the Au/cermet/Si samples is not due to that of the cermet characteristics, C-V measurements of some Au/cermet/Aℓ samples were made and one of these is shown in Fig. 5.19. They all show absolutely flat

(bias independent) capacitance. These therefore show that it is inappropriate to analyse the experimental results as with a good MIS device, as was done at the beginning of this section. More detailed measurements were then performed on other Au/cermet/Si samples.

5.4.2 An Equivalent Circuit for the Structure

Fig. 5.20 shows the results of C-V measurements at various signal frequencies on sample CmSi4. At intermediate frequencies the curves are exactly the same as before. Although it was not possible to use the integration method described in the previous sub-section to measure the dc capacitance becuase of the relatively high leakage current ($\sim 10^{-11}$ A at 1V) of the cermet, it is clear that at low frequency the capacitance approaches the cermet capacitance at all bias voltages. At high frequency (1 MHz) the capacitance again becomes bias independent but has a smaller value. Now, as discussed in section 2.4, the high frequency capacitance of a MIS structure is the series combination of the capacitance of the insulator and space charge region of the semiconductor, since the interfacial charge states are not able to follow the signal. The fact that the high frequency capacitance remains virtually constant therefore indicates that the depletion width also remains constant with bias. This is consistent with the deduction from the low frequency capacitance that the space charge potential is not altered

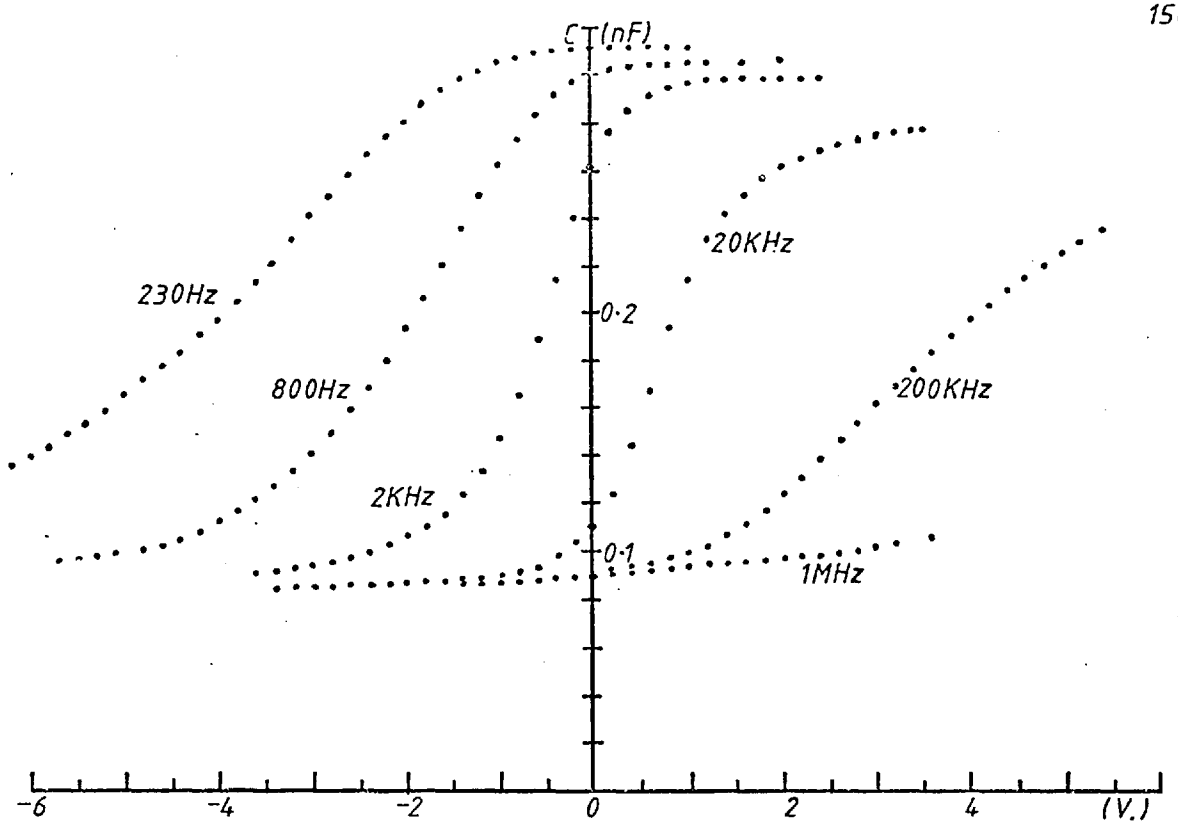


Fig. 5·20 C–V characteristics of a Au/cermet/Si sample (CmSi4).

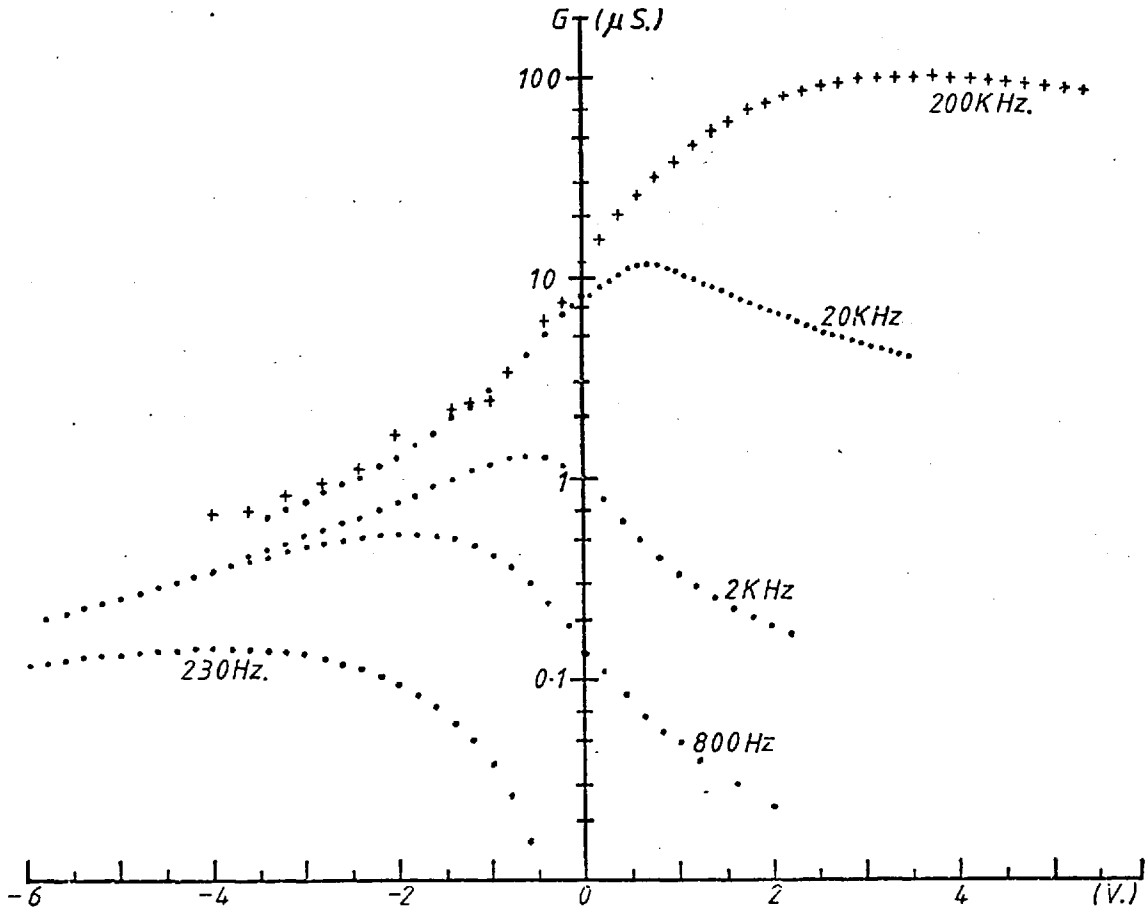


Fig. 5·21 G–V characteristics of a Au/cermet/Si sample (CmSi4).

by any applied voltage. It is therefore apparent that the behaviour at intermediate frequencies is due to the response of interfacial charges. By assuming that this can be represented by a resistance R_{ss} and a capacitance C_{ss} in series, the circuit shown in Fig. 2.7 can then be used to deduce the charge density ($C_{ss} = qN_{ss}$, eq. (2.38)) and their characteristic time constant ($\tau = R_{ss}C_{ss}$). To do this, another parameter, the ac conductance G against bias V needs to be known, and is shown for the same sample in Fig. 5.21. It must be remarked that this again is very similar to that of a good MIS structure with a real insulator[10]. (An ideal MIS structure of course shows zero conductance.) However, in view of the fact that the cermet has a finite ac conductance G_o which can become quite large at high frequencies, it is necessary to introduce this across C_o into the equivalent circuit. To simplify calculations, the series R_{ss} and C_{ss} components are converted into a parallel G_p, C_p equivalent circuit. These are given by

$$G_p = \frac{w^2\tau C_{ss}}{1 + w^2\tau^2} \qquad (5.7)$$

$$C_p = \frac{C_{ss}}{1 + w^2\tau^2} \qquad (5.8)$$

where $\tau = R_{ss}C_{ss}$. The complete equivalent circuit is thus as shown in Fig. 5.22. The cermet capacitance C_o can be estimated from the high forward bias measured value.

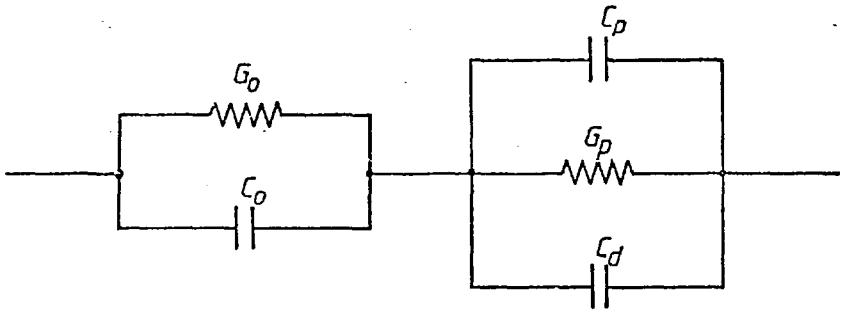


Fig. 5·22 Equivalent circuit of a Au/cermet/Si structure.

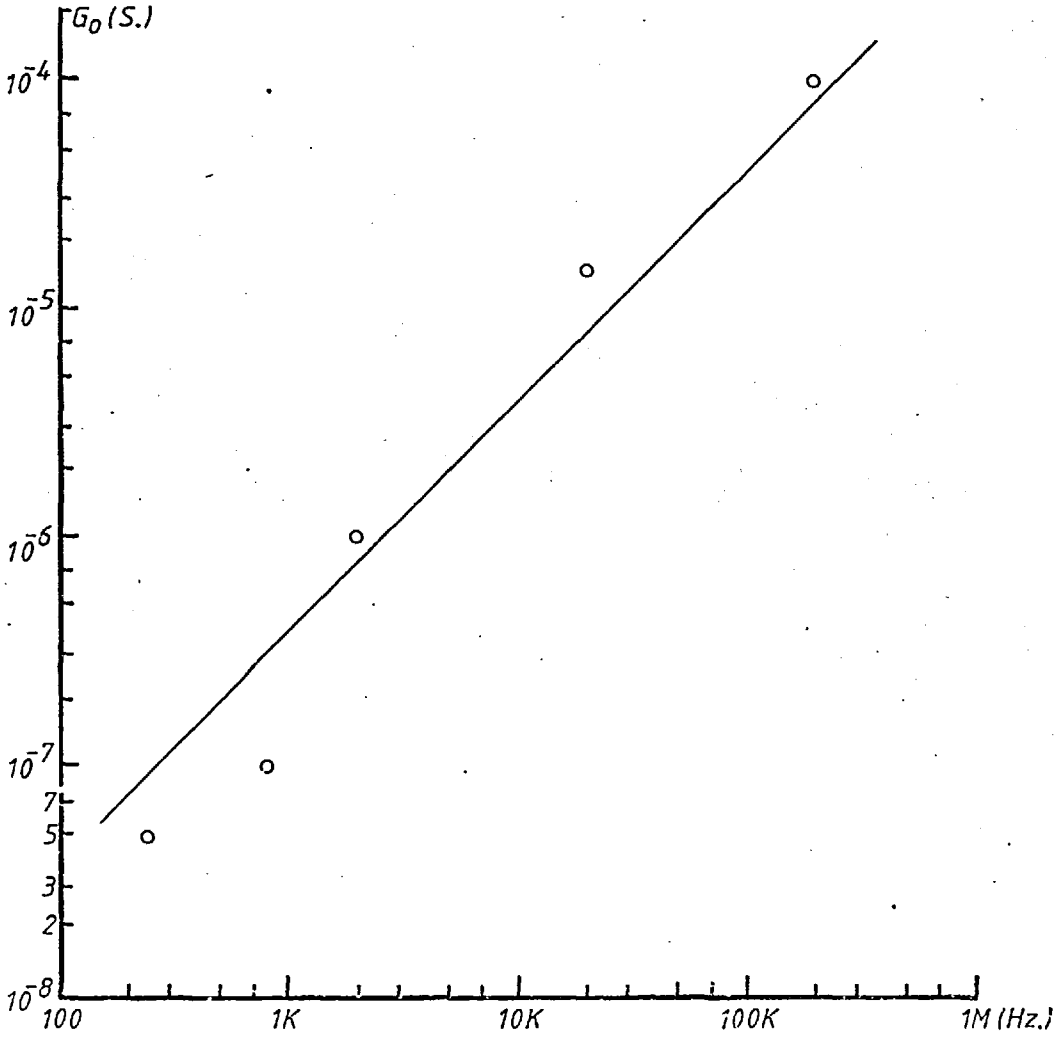


Fig. 5·23 G_o—f plot of the cermet of sample CmSi4.

It is a function of frequency and is shown in Table 5.4. The depletion capacitance C_d, which is assumed to be a constant, can be obtained from the high frequency and high reverse bias value since this is approximately a series combination of C_o and C_d; the value of G_o found later for this sample turns out to be about an order of magnitude smaller than the reactance wC_o at all frequencies. The value of C_d thus found is 118 pF (per area of 0.785 mm^2) for the same sample. With these values of C_o and C_d, it is found that by choosing suitable values of G_o, the value of G_p can be made virtually independent of frequency. This requires that $w\tau > 3$ which is found to be true later on in this section. The values of G_o are plotted against frequencies in Fig. 5.23. The relationship is roughly $G_o \alpha w$ which is about the same as what was observed in the cermet measurements on samples with low metal fraction composition (Fig. 3.9). G_o also has the same order of magnitude. It therefore seems that this circuit is a reasonably accurate representation of the insulating Au/cermet/Si samples. The values of G_p obtained are shown in Fig. 5.24.

5.4.3 Conduction Mechanisms of the Structure

The first model attempted in order to explain the presence of R_{ss} and C_{ss} is that these are due to the Schockley-Read-Hall centres present at the silicon surface. Such centres would have a response time constant as given in eqn. (2.32). For simplicity, the term due

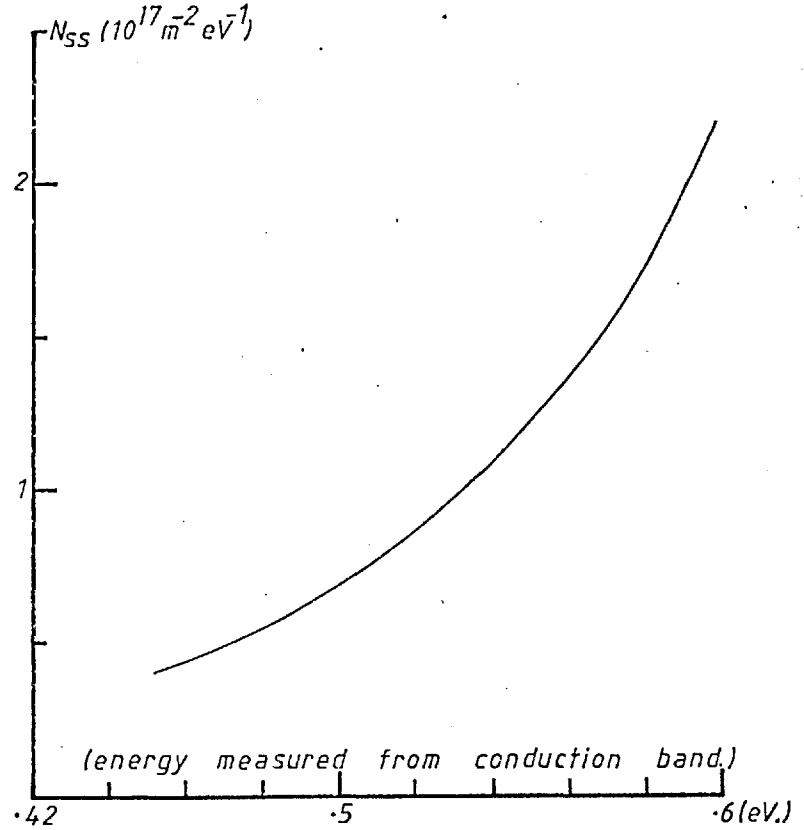


Fig. 5·25 Shockley–Read–Hall surface state density of sample CmSi4.

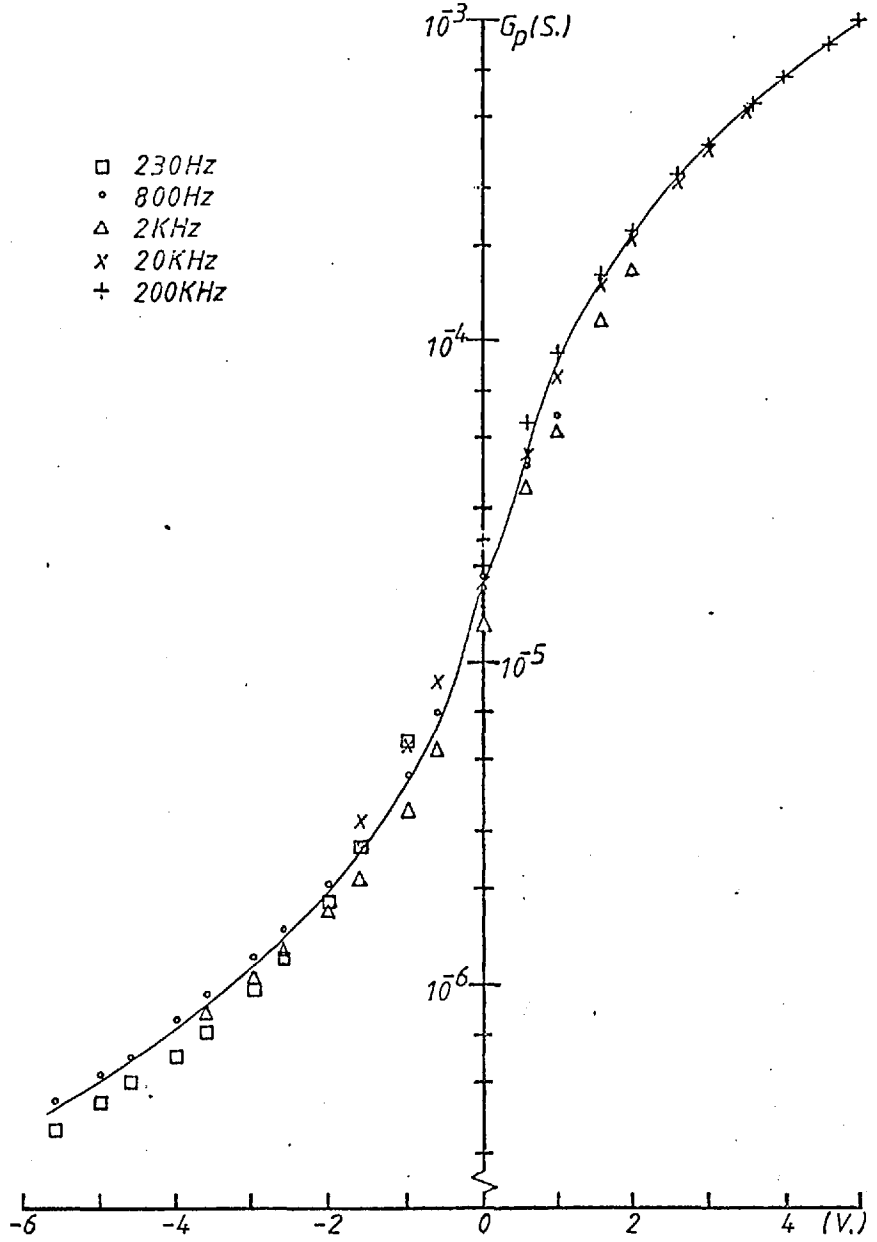


Fig. 5·24 $G_p - V$ plot of sample CmSi4.

to minority carriers (holes) is ignored so that it simplifies to

$$\tau = \frac{1}{c_n(n_s + n_1)} \tag{5.9}$$

The capture constant c_n is the product of the capture cross-section σ_n and the average thermal velocity v. The surface free electron density n_s is given by $n_s = n_b \exp(-\beta V_s)$. Since there is a distribution of traps across the whole energy gap, it is assumed that most contributions come from those states at the Fermi level. Then E_t of eqn. (2.33) may be set equal to E_F and so $n_1 = n_s$. From eqns. (5.7), $G_p \sim C_{ss}/\tau$, and also $C_{ss} = qN_{ss}$, therefore

$$\begin{aligned} G_p &\sim 2qN_{ss}\, c_n\, n_b \exp(-\beta V_s) \\ &\sim 8 \times 10^{-8}\, N_{ss} \exp(-\beta V_s) \end{aligned} \tag{5.10}$$

where we have used $\sigma_n = 10^{-19}\ m^2$, $v = 10^9\ ms^{-1}$ as obtained from the works of Nicollian et al.[11] and $n_b = 2.5 \times 10^{21}\ m^{-3}$. The change in interfacial charges (states) may be related to the bias voltage as follows. Charge balance requires that

$$N_g = \delta N_t + \delta N_d \tag{5.11}$$

where qN_t, qN_d are the interfacial and space charge densities respectively, and qN_g is the charge on the gate (gold electrode) and equals to $C_o V_i/q$. δ represents the change in each quantity due to an applied voltage V. Hence, from eqns. (5.11) and (2.20)

$$\frac{C_o V_i}{q} = \delta N_t + (2q\varepsilon_s n_b)^{\frac{1}{2}} \left(\sqrt{V_{so}} - \sqrt{V_{so} + \delta V_s}\right)$$

where V_{so} is the surface potential of the space charge in the absence of a bias voltage, and δV_s is the change in V_s due to applied voltage, thus $V = V_i + \delta V_s$. But since δV_s is small compared with V_i, we put $\delta V_s = 0$ and so $V_i = V$. Consequently,

$$N_{ss} = \frac{dN_t}{dV_s} = \frac{C_o}{q} \frac{dV}{dV_s} \qquad (5.12)$$

Using eqns. (5.10) and (5.12), iterative calculations can be carried out by first assuming a constant N_{ss} and calculate V_s against V using eqn. (5.10). From the gradient, new values of N_{ss} vs V_s can be found using eqn. (5.12). This is put back into eqn. (5.10) and so on. The result of this successive iteration shows that convergence is obtained only with the reverse bias voltage. This is shown in Fig. 5.25. Note that V_s changes by only about 0.2 eV for a change in applied voltage of 6V, which is consistent with the assumption that $V_o >> \delta V_s$.

The above calculation actually assumed that the charges giving rise to G_p (eqn. (5.10)) were also responsible in setting the value of V_s (eqn. (5.12)). However, this is not the case if there are many different kinds of trapping states. Consider the situation where there are two kinds of traps, one with density N_{s1} and $\tau_1 \sim 10^{-3}$ s, and one with density N_{s2} and $\tau_2 \sim 10$s. When the measuring signal frequency is in the KHz range, N_{s2} would not response so that $G_p \sim qNs_1/\tau_1$ for eqn. (5.10). But since readings are recorded only after the measured C and G values had settled down to constant values, i.e. after about 60s, both N_{s1} and N_{s2} are able to equilibrate with the bias voltage. Therefore N_{ss} in eqn. (5.12) equals to $(N_{s1} + N_{s2})$. Consequently, the value of V_s would change less than if only N_{s1} is used, resulting in a lower G_p in the case of forward bias (δV_s negative). The decrease in gradient (Fig. 5.24) with increasing forward bias voltage is the reason for the non-convergence in the above calculations.

The characteristic time constant τ can also be deduced from the calculated C_p and G_p. From eqns. (5.7) and (5.8), this is given by $\tau = G_p/w^2 C_p$ and is plotted in Fig. 5.26. The effect of a ±1% error in measured C is indicated for the 20 KHz curve. Despite the large uncertainties which may result from such a small error, the graph clearly shows that there is a group of traps with characteristic time ranging from 10^{-2}s to 10^{-3}s as

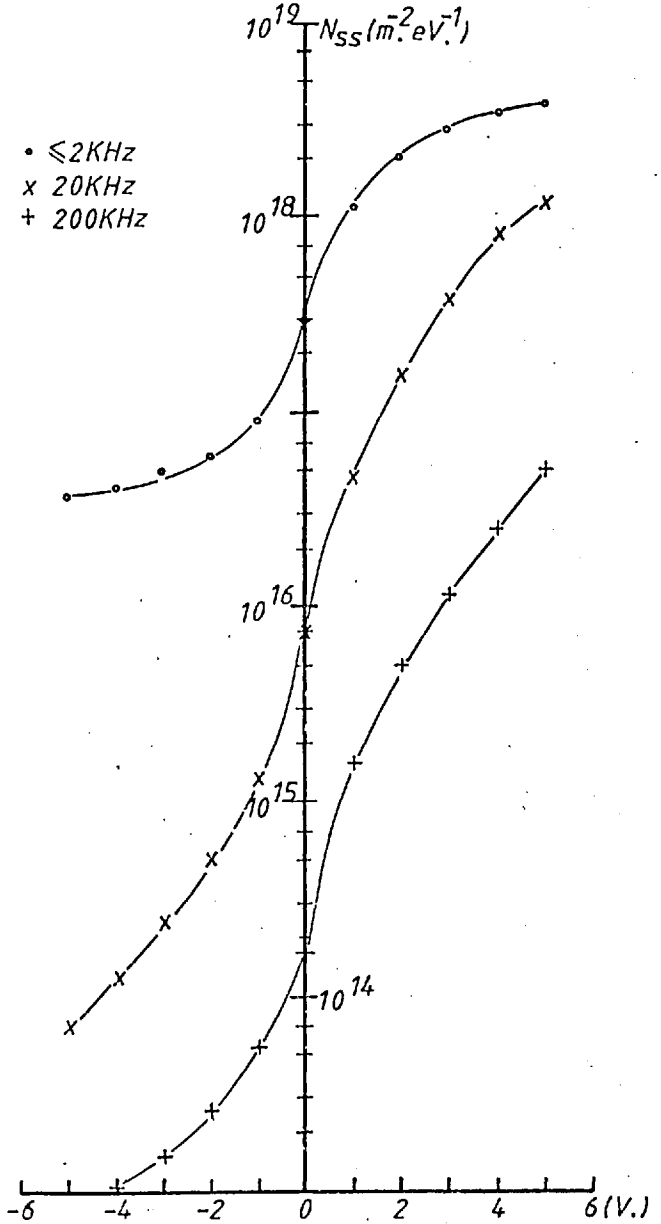


Fig. 5·27 Interface charge density of sample CmSi4.

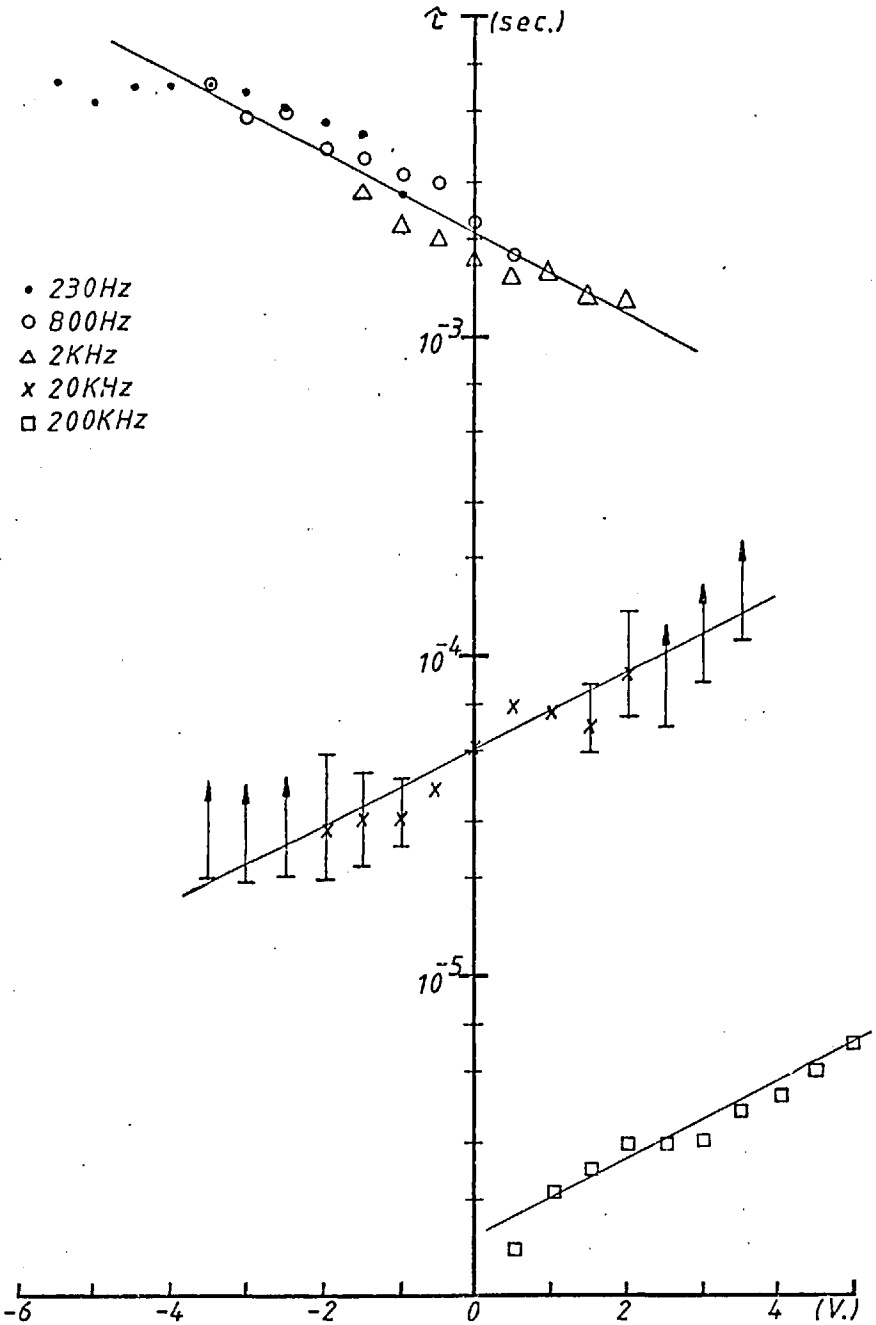


Fig. 5·26 Time constant of interface charges of sample CmSi4.

the bias voltage varies from -5 to + 5 volts. At low frequencies ($\lesssim$2 KHz) this group dominates over all other possible charge states so that there is no frequency dispersion in τ. But at higher signal frequencies these traps become unable to follow so that the observed time constant is gradually being dominated by the fast traps. Also, assuming that the mechanism giving rise to G_p and C_p can be represented by R_{ss} and C_{ss} in series, then eqn. (5.7) also indicates that for G_p to be independent of frequency, $\omega\tau$ must be greater than about 4. This is true at low frequency, but not quite so if the high frequency values are used. It therefore casts some doubt on the reliability of the high frequency values. The corresponding trapping densities can also be deduced from eqn. (5.7) and are shown in Fig. 5.27. The time constant at any particular bias is obtained from the straight line drawn through the data points. It is seen that at low frequencies, the trap density ranges from about 4×10^{16} to 4×10^{18} m^{-2} eV^{-1}. This group of traps alone would be big enough to pin the Fermi level so that V_s remains virtually constant with bias. Compare these values with those obtained from the surface states iterative calculations done above, one sees that the previous values are about an order of magnitude too small. It therefore seems that these traps are not simply due to the ordinary Shockley-Read-Hall centres.

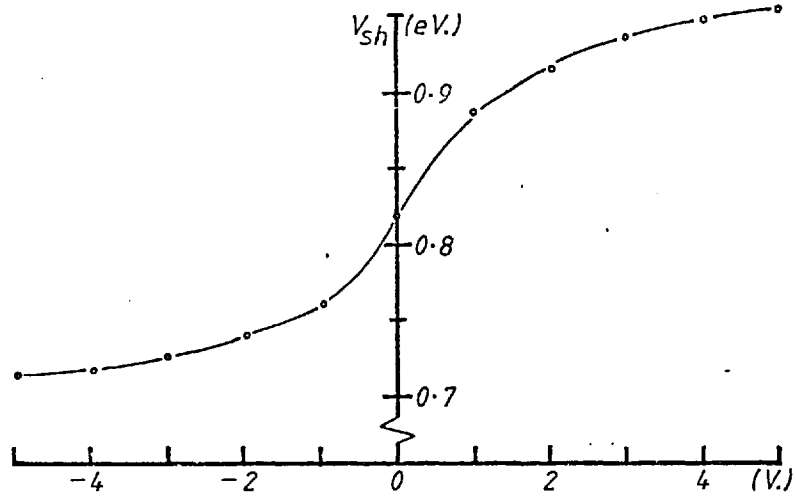


Fig. 5·28 Minority (hole) carrier quasi-Fermi level at the cermet–silicon interface.

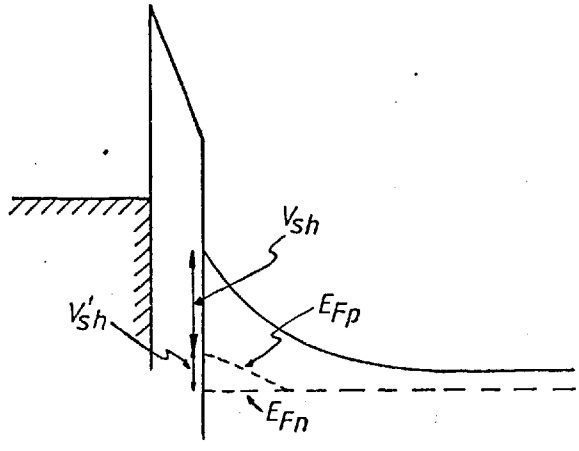


Fig. 5·29 Energy band diagram of a Au / cermet / Si sample.

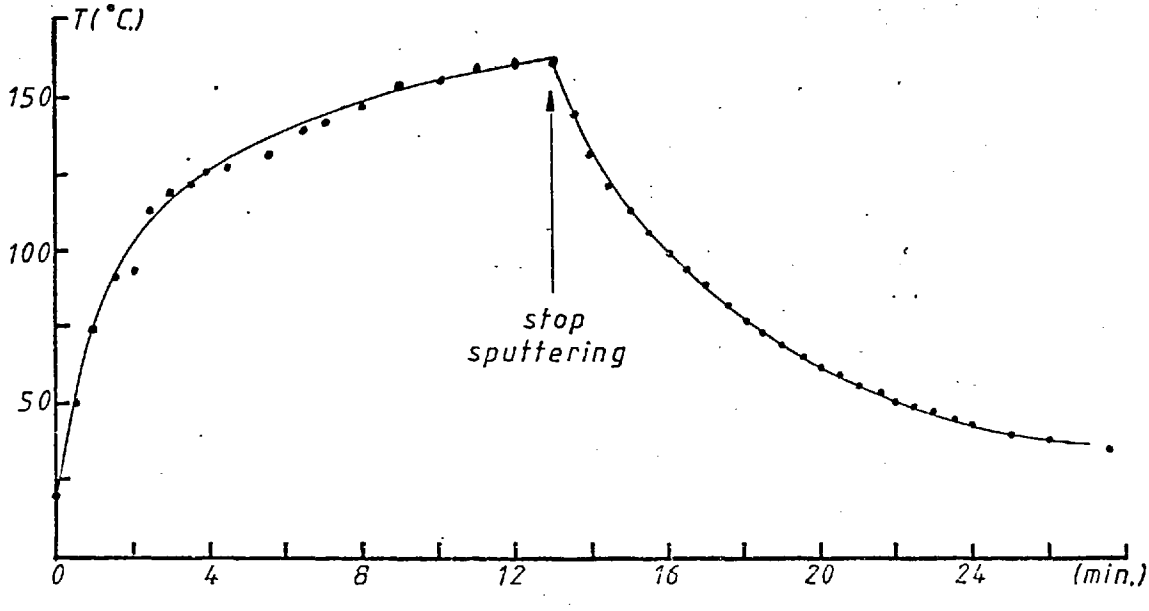


Fig. 5·30 Substrate temperature during the sputterig process.

Another possible source of the low frequency C_{ss} comes from the minority hole carriers. The value of space charge capacitance C_d used in the calculations was 0.118 nF (0.150 nFm^{-2}). Using the parallel plate formulae $C = \varepsilon_o\varepsilon_s/\ell$, this gives a depletion width ℓ of 0.695 μm. Since C_d comes from the majority electrons at the depletion edge, then, using eqn. (2.21), the diffusion potential V_{bi} which is also equal to the surface potential V_s is 0.88 eV. With V_n = 0.21 eV, the barrier height $V_{bo} = V_{bi} + V_n$ = 1.09 eV. Since the silicon energy gap is 1.12 eV, inversion must have taken place at the surface (see section 2.3.4). The minority carrier capacitance C_h is given by eqn. (2.28)

$$C_h = \left(\frac{\varepsilon_o\varepsilon_s q\beta p_b}{2} \right)^{\frac{1}{2}} \exp(\tfrac{1}{2}\beta V_{sh})$$

V_d there is replaced by V_{sh} here to indicate that it describes the hole density and may be different from the actual diffusion potential. By taking C_h to be equal to the low frequencies qN_{ss} in Fig. 5.27, V_{sh} may be calculated as a function of bias voltage. This is shown in Fig. 5.28. It is seen that at zero bias where thermal equilibrium exists so that $V_{sh} = V_s$, V_{sh} = 0.82 eV which is about the same as V_s = 0.88 eV evaluated from the majority electron capacitance C_d above. Comparing this with the value of 0.45 eV evaluated from the surface state model previously one sees

that the latter mechanism is more probable. The low frequency time constant τ shown in Fig. 5.26 is then equal to the response time of the holes. The value of τ between 10^{-3} and 10^{-2}s is about the same as those obtained by other workers on MIS devices[11]. The hole density as given by eqns. (2.27) and (2.28) is $Q_h = 2C_h/\beta$. Fig. 5.27 therefore shows that Q_h decreases in the reverse bias direction and increases with forward bias voltage. V_{sh} may then be regarded as indicating the position of the quasi-Fermi level for holes at the surface. This decrease (increase) of minority carrier density with increasing reverse (forward) bias may arise because of the small but finite dc current flowing through the cermet. In the semiconductor space charge region, this current may be mainly carried by the minority holes since the high barrier height gives rise to high minority carrier injection ratio. From eqn. (2.47), for $V_{bo} \sim 1$ eV, the ratio is $\gamma \sim 1.5$. Fig. 5.29 shows an energy diagram of such a system.

So far, the arguments presented in this sub-section are mainly based on the results of one sample only. Measurements made on other samples showed that they all behaved similarly, but the actual parameters (e.g. the characteristic time τ) observed may fluctuate by more than an order of magnitude from sample to sample.

5.5 GENERAL DISCUSSIONS AND CONCLUSIONS

The forward current of the sputtered Au-Si Schottky barrier is quite good in that it obeys fairly well the ideal diode equation, limited only by the series resistance. However, the barrier height obtained is only 0.65 eV, which is much less than the value of about 0.8 eV for evaporated gold contact. This lower value was in fact also obtained by Wronski[12]. The reason for this may be partly due to the damaged surface layer which is so conductive that it is not necessary for electrons to surmount the potential dropped across it in order to cross the barrier. It may also be partly due to the fact that since the surface potential of a practical semiconductor is always determined by surface charges due to impurities and imperfections rather than the difference in work functions between the contact metal and semiconductor, the sputtering process may have created just enough net surface charges to hold the space charge potential at the observed value. It is mainly because of these surface charges that even evaporated gold contacts on carefully cleaved silicon surfaces may give vastly varying barrier heights. Values as low as 0.67 eV have been reported[13]. It is also believed that this is the main reason for the large variation of characteristics from sample to sample in the experiments with Au/cermet/Si samples.

The reverse characteristics of the Au/Si samples exhibit very soft current saturation. This was interpreted as due to the presence of a conductive

interface layer which presumably is due to surface contaminations and damages. Even with such a simple model, it is necessary to know the trap distribution in this interface layer in order to do a more quantitative analysis of the potential dropped across it. In the lack of such information, we have to assume that its space charge density remains constant with bias voltage and equals the doping density of the silicon bulk. The result of such assumptions should not differ too greatly from the actual result if the true charge density in it was used, since the layer is thin compared with the thickness of the whole space charge region of the silicon (section 2.5.3d). Such theoretical calculations fit the experimental data to within about 5%. Actually the lowering of barrier height from the experimental data varies more closely with the square root of the applied voltage rather than according to eqn. (5.5). This kind of relationship has been observed by other workers[14] working on silicide-silicon Schottky barriers. But these contacts were free from any interfacial layers. Therefore the two mechanisms may be fundamentally different.

The effective doping density deduced from C-V measurements shows slight variation with frequency. This may be attributed to the presence of deep traps in the space charge region[15,16]. The origin of these traps is not known, but may possibly come from the diffusion of gold from the electrode. The substrate table which

held the silicon wafer during fabrication was not water cooled in the dc sputtering system used to deposit the pure gold contact electrode. By glueing a thermocouple with colloidal graphite onto a silicon wafer surface, it was found that the temperature increased to about 160°C at the end of the 12 minutes sputtering process (Fig. 5.30). Because of the high interstitial diffusion constant of gold in silicon ($D_i = 2.44 \times 10^{-8}$ exp (-0.387β) $m^2 s^{-1}$)[17], there is a possibility that some diffusion had occurred in the surface region to a depth of ∿1 μm thick. This also accounts for the characteristics of Au/cermet/Si samples which show a much less frequency dependent effective donor density since the amount of gold in contact with the silicon surface is much less. The barrier height V_{bo} obtained from the C-V measurements of Au/Si samples also flucturates with frequency, giving V_{bo}∿ .7 - .8 eV. These values are higher than that obtained from the I-V measurements where V_{bo}∿ 0.65 eV. This is consistent with the assumption of a conductive damaged silicon surface because the capacitance is a measure of the depletion width which includes the damaged layer and is a function of the total diffusion potential, whereas the current is independent of the potential dropped across the damaged layer, except that it provides a lower barrier height to the emitting electrons. In other words, referring to Fig. 5.5, the capacitance measures V'_{bo} whereas the current gives V_{bo}. Furthermore,

the capacitance at near zero and forward bias is much higher than the space charge capacitance. At zero volts, it has reached 16.5 nF at a frequency of 120 Hz. From $C = \varepsilon_o \varepsilon_s / t$, this gives $t \sim 4.97$ nm which is close to the thickness of the damaged layer estimated in section 5.2.1. It therefore seems likely that the effect is due to the response of charged states in the layer.

For the forward characteristics of the Au/cermet/Si structure, the cermet resistance plays an important part in limiting the current flow. As a result, it is necessary to know precisely the I-V characteristics of the cermet in order to be able to deduce the barrier height of the cermet/silicon junction. Although it was shown in section 3.4.2 that the cermet generally obeys the Poole-Frenkel equation, slight deviations do occur from sample to sample. Furthermore, because a larger portion of the applied voltage is dropped across the cermet than across the space charge region of the silicon, a plot of log I vs $V^{\frac{1}{2}}$ where V is the total applied voltage in fact also gives roughly a straight line. Therefore it is not feasible to deduce the barrier height in this way. For the reverse current, there is some sign of saturation occurring. This non-symmetrical I-V characteristic between forward and reverse bias therefore indicates that there is definitely a depleted space charge region on the silicon surface. But the apparent saturation current is lower than that of a sputtered pure

gold-silicon contact. This may be due to a higher barrier height because of the presence of SiO_2 on the silicon surface and also to a reduction of effective gold area in contact with the silicon where current flow takes place. The C-V measurements of such samples also reveal the importance of accounting for the voltage dropped across the cermet especially at low applied bias. Again the barrier heights deduced also show higher values than that of pure-Au/Si junction, although the uncertainty errors incurred are very large. At near zero and forward bias, the capacitance again increases very rapidly and so we draw the same conclusion as before, that there are plenty of interface charges which are able to follow the signal frequency. The hysteresis and slow drift (decay or rise of capacitance in response to a step change in applied voltage) is of interest. It had been observed[18] before that some cermet materials might exhibit such effects, and was attributed to ion-drift within the insulating material. However, in the case of the present experiments, such an effect is most serious for samples in the transition region. This is not consistent with the idea of ion drift within the SiO_2 since in that case, one would expect that the effects would be most serious for insulating cermets. Another possibility is the trapping or de-trapping of electronic charges in the SiO_2 near the cermet/Si interface. Consider a structure under reverse bias (gold electrode negative),

electrons would tend to be driven from the gate (gold electrode) towards the silicon interface. For a conductive cermet, there is a large number of conduction paths with a relatively small volume of SiO_2 so that electrons trapped inside the SiO_2 can very easily detrap themselves once the applied voltage is removed, by jumping into large metal particles which form the conduction paths. This leaves the interface charges unchanged so that there is no hysteresis loop. For the insulating cermets, hardly any electrons are driven from the gate to the interface so that the charged states in the SiO_2 again remain unchanged. But for cermets in the transition region, there are enough conduction paths to bring electrons to the interface. Under high electric field, electrons can easily be driven from such conduction paths into traps deep inside the SiO_2 by means of field-assisted tunnelling. When the field is removed, many of these trapped electrons would not be able to tunnel back into the conduction paths because of the long distance involved. Consequently a net negative charge piles up at the SiO_2 side of the interface. For charge balance, a corresponding positive charge would be attracted to the silicon surface. This may be in the form of minority hole carriers in the inverted surface, and therefore explains the increase of capacitance. As discussed in the previous section, the occurrence of an inverted silicon surface is very likely especially if the interface is dominantly between

SiO_2 (rather than gold) and silicon. The presence of minority holes was also used to explain the large frequency dispersion and bias variation of measured ac capacitance and conductance. The results show that the hole quasi-Fermi level can be deduced. The variation of surface hole density or $E_{Fp}|_{x=0}$ with voltage is a direct consequence of a leaky insulator, the cermet. The energy diagram may be drawn in a similar way as for a tunnel MIS structure in which minority carriers play an important role in the photo-voltaic characteristics[19,20]. There are various mechanisms that may assist the response of these minority carriers to the ac signal. Firstly, they can cross the space charge region by diffusive current. This is given by eqn. (2.46). Such mechanism would have a differential conductance given by

$$G_h = (q^2 D_h p_o / kTL) \exp(\beta V'_{sh}) \times \text{area}$$

$$\sim 3.5 \times 10^{-13} \exp(\beta V'_{sh})$$

Comparing this with the experimentally determined ac conductance (Fig. 5.24) we see that it is several orders of magnitude too small, although both vary roughly similarly with the applied voltage V or surface hole quasi-Fermi level V_{sh}. It therefore seems that the minority holes are transported to the interface by some other, faster, mechanism. The second possibility is that the presence of a large number of interface states provides a corresponding number of recombination centres for the holes. Also, any diffusion of gold into the

space charge region would greatly reduce the minority carrier life time. Finally, since the whole silicon surface is covered with cermet, inversion may have occurred throughout the surface. The minority carriers may then flow laterally on the inverted surface which provides a very conductive path[21].

In conclusion, the characteristics of Au/cermet/Si samples were found to be not very reproducible. This is believed to be due to contamination and damage on the silicon surface. As a result, any likely direct effects that the charging energy of the granular metal islands in the cermet would have on the diffusion potential of the semiconductor surface is completely obscured. Nevertheless, the presence of the cermets do greatly alter the C-V characteristics of such devices. For the case of a conductive cermet, the device behaves as a metal-semiconductor Schottky barrier, the cermet acting like a constant voltage barrier in series with it. For the case of an insulating cermet, the device behaves more like a MIS structure with an extremely large interface charge density. The quasi-Fermi level of the majority carriers is therefore being pinned at the surface. Since the dc current is very small, the depletion layer remains constant with bias, giving a constant depletion capacitance which is due to the majority carriers at the depletion edge. But it is also because of the small but finite dc current and high barrier height that large variations of minority carriers

with bias voltage may occur at the interface. Such variations and their response to the ac signal give rise to very large frequency and bias dependent capacitance.

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CHAPTER 6

EXPERIMENTAL RESULTS OF CdSe SAMPLES

6.1 INTRODUCTION

This chapter deals with the experiments carried out in which evaporated CdSe films were used as the semiconductor material. Evaporated pure CdSe films are always n-type, the donors of which are from Se vacancies[1]. It was hoped to find out the nature of the contact between gold and these films. The counter electrode was chromium. Experiments with samples in which a CdSe film was evaporated onto a chromium coated soda glass slide and followed by the evaporation of chromium dots on the CdSe surface showed linear I-V characteristics up to an electric field in the CdSe of about 10^6 Vm^{-1}. It was therefore concluded that the contact between chromium and CdSe could be considered as ohmic for the purposes of the experiments.

The technique of film depositions and cleaning of glass slides was described in chapter 4. Initially, measurements were made on samples produced by the following sequence: A thin layer (~100 nm) of chromium film was evaporated onto a glass slide, followed by the evaporation of a CdSe film (nominally 1 μm thick), and then gold dots of 1 mm diameter and about 100 nm thick were sputtered on top through a contact mask. (Fig. 6.1a). But it was found that the electrical properties of the

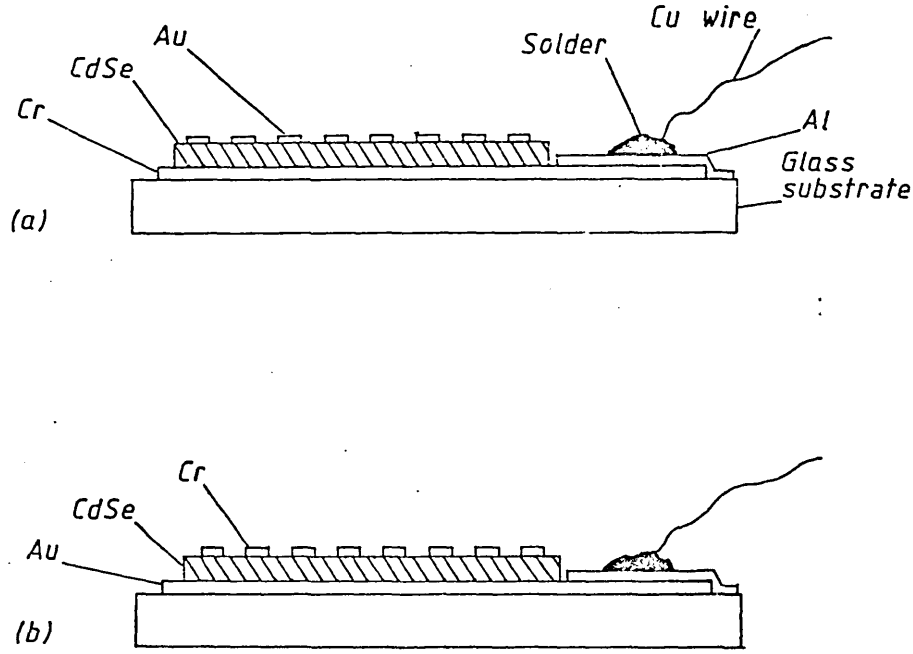

Fig. 6·1 Schematic cross section of CdSe samples.
(a) Au/CdSe/Cr (b) Cr/CdSe/Au

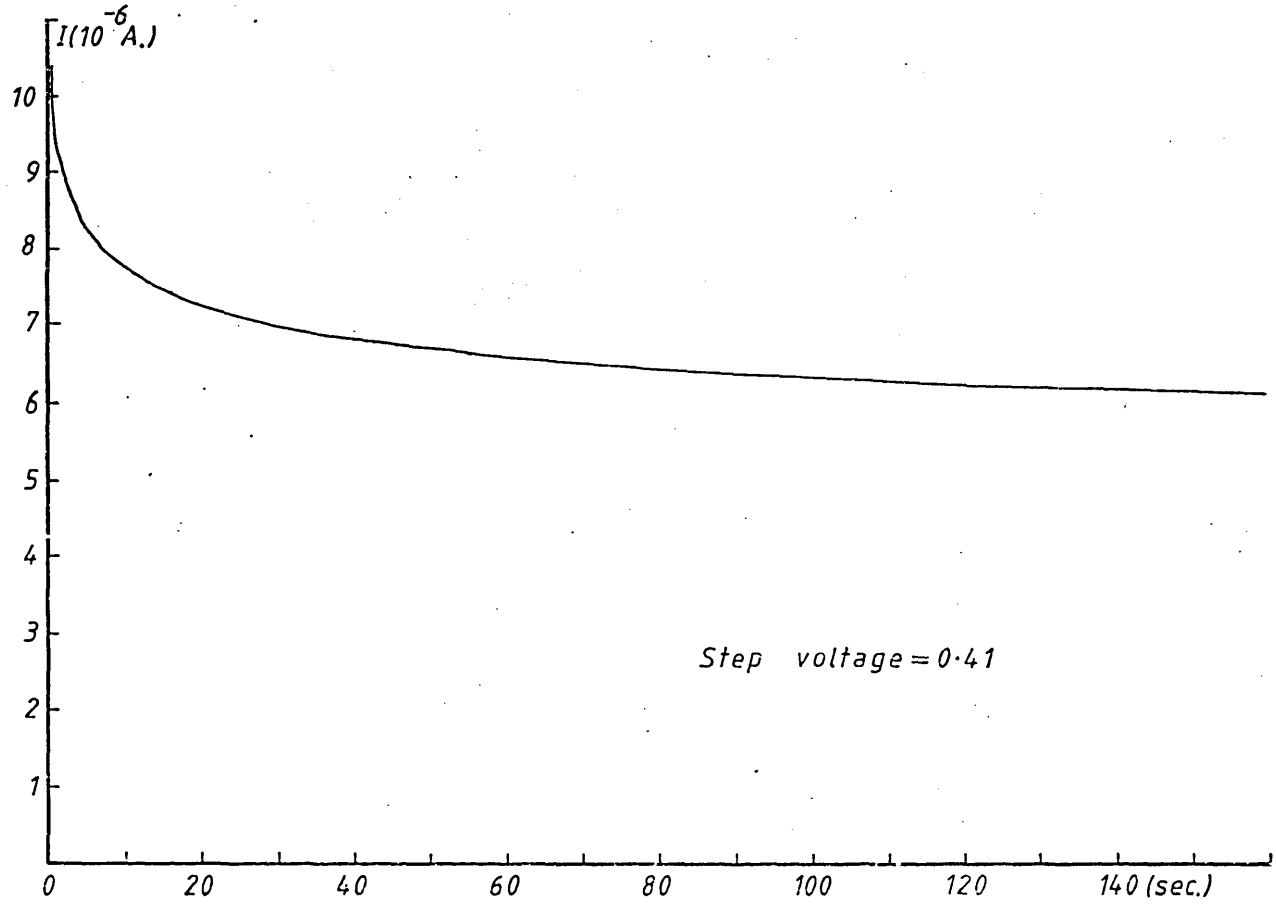

Fig. 6·2a Forward bias current vs time after a step voltage was applied.

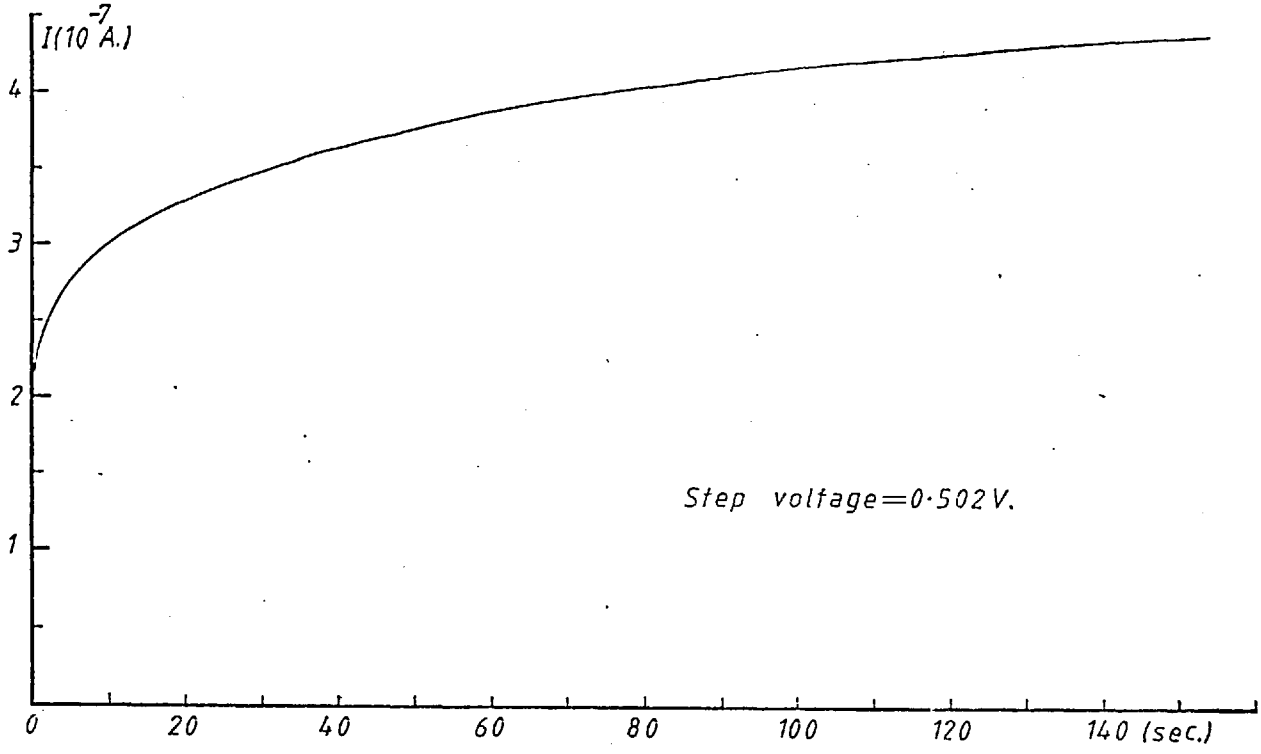

Fig. 6·2b Reverse bias current vs time after a step voltage was applied.

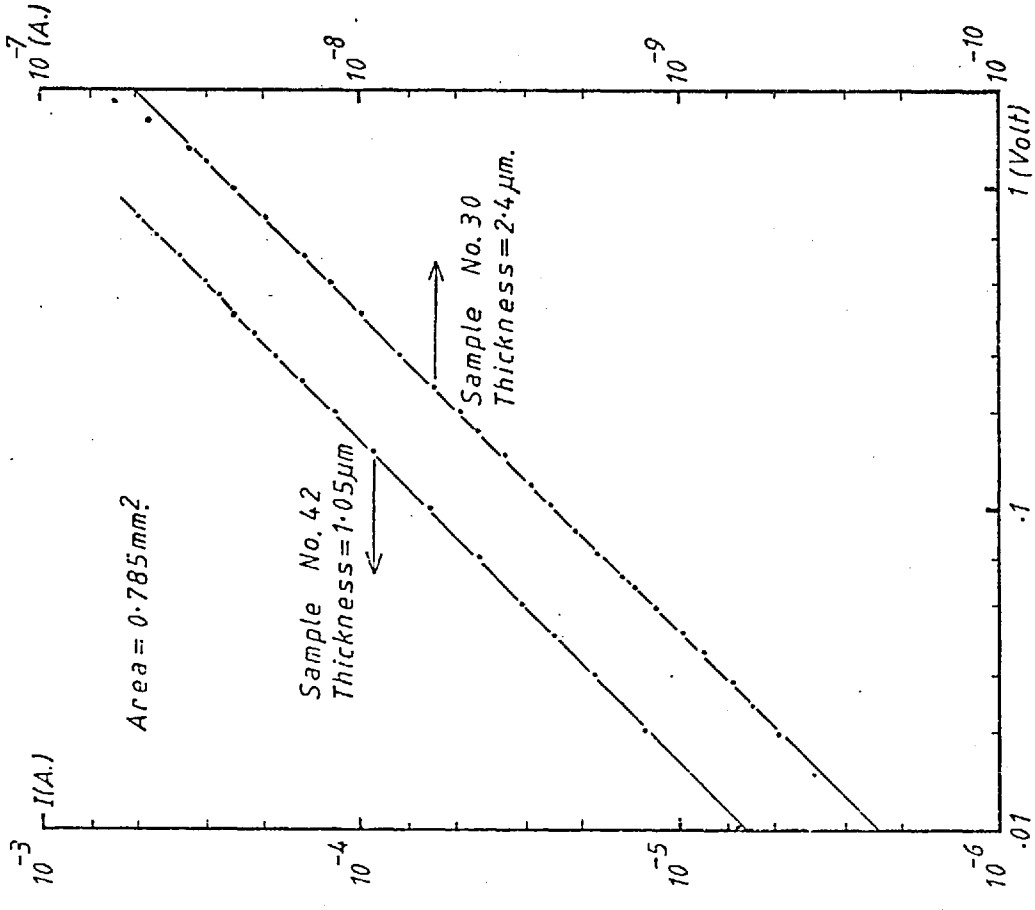

Fig. 6·3 DC I–V characteristics of some Au/CdSe/Cr samples.

CdSe film were very irreproducible, ranging from 10^2 Ωm to 10^6 Ωm, and also no decent Schottky barrier could be obtained. It was therefore decided that the sequence of chromium and gold depositions would have to be interchanged by first of all sputtering a gold film on a glass slide, followed by the CdSe and then the chromium dots. (Fig. 6.1b). This time, non-symmetrical I-V characteristics were obtained, indicating that a depleted space charge region was formed at the Au/CdSe junction. The resistivity of the CdSe films was also more reproducible, the majority of them were around 10^3 Ωm.

The electrical measurements of these specimens were made in the same way as described in section 4.9. In taking the dc I-V and C-V characteristics, the applied voltage was changed in steps. It was observed that the corresponding current and differential capacitance did not change in step with this applied voltage, but instead, very large drift occurred which might last for a few minutes before a steady state was established. This indicated the presence of slow traps in the sample. Fig. 6.2 shows the drift current in the forward (Fig. 6.2a) and reverse (Fig. 6.2b) directions. These were obtained by connecting the buffered output of the Keithley 602 electrometer used in the fast mode to an X-T plotter. The change was always such that the forward current decreased with time whilst the reverse current increased with time. The total change was as

much as one-half of the initial current flowing when the voltage was first applied. In order to have meaningful results, it was necessary that the readings were recorded either with pulsed voltage so that the trapping states remained in their thermal equilibrium condition, or, alternatively, at time so long after the applied voltage was changed that steady state constant current had been established. For a manually operated experiment, it was not possible to use the former method. Therefore readings were taken only after the drift rate had become so small that steady state condition was essentially reached. This meant that only one data point could be taken every five minutes or longer.

In referring to the applied bias in the following discussions, it is assumed that gold makes a rectifying barrier with the n-type CdSe film. Thus, the term forward bias refers to positive voltage applied on the gold with respect to the CdSe or chromium.

6.2 ELECTRICAL CHARACTERISTICS

6.2.1 Au/CdSe/Cr Samples (Fig. 6.1a)

Typical dc I-V characteristics are shown in Fig. 6.3. At low applied voltage, all samples showed ohmic and symmetrical behaviour in both bias directions. Assuming that the electric field was uniformly distributed across the CdSe, this was in the range below 10^6 V m^{-1}. Destructive breakdown usually occurred at an average field of less than 5×10^6 V m^{-1} and some samples showed switching effects. Furthermore, the resistivity of these samples fluctuated greatly and randomly from sample to sample. In extreme cases, they varied from 10^2 to 10^6 Ωm.

Some ac characteristics measured with a curve tracer are sketched in Fig. 6.4. Again, ohmic behaviour was observed at low field, but many showed loops especially at high field (Fig. 6.4a). Such loops were usually non-symmetrical with the reverse bias (gold negative) giving a larger current. Samples that were made by heating the substrate to a temperature of about 200°C during the CdSe deposition were very conductive. The current was limited only by the resistance (∿10 Ω) of the chromium underlay. A few of such samples showed a slight 'knee' at reverse bias of about 0.2 volt. (Fig. 6.4c).

Capacitance measurements could be made only on resistive samples (≳ 10^4 Ωm). For more conductive samples, the capacitance measured decreased very rapidly when the dc bias voltage was greater than about 0.1 volt (∿10^5 V m^{-1}). It was therefore considered that the C-V

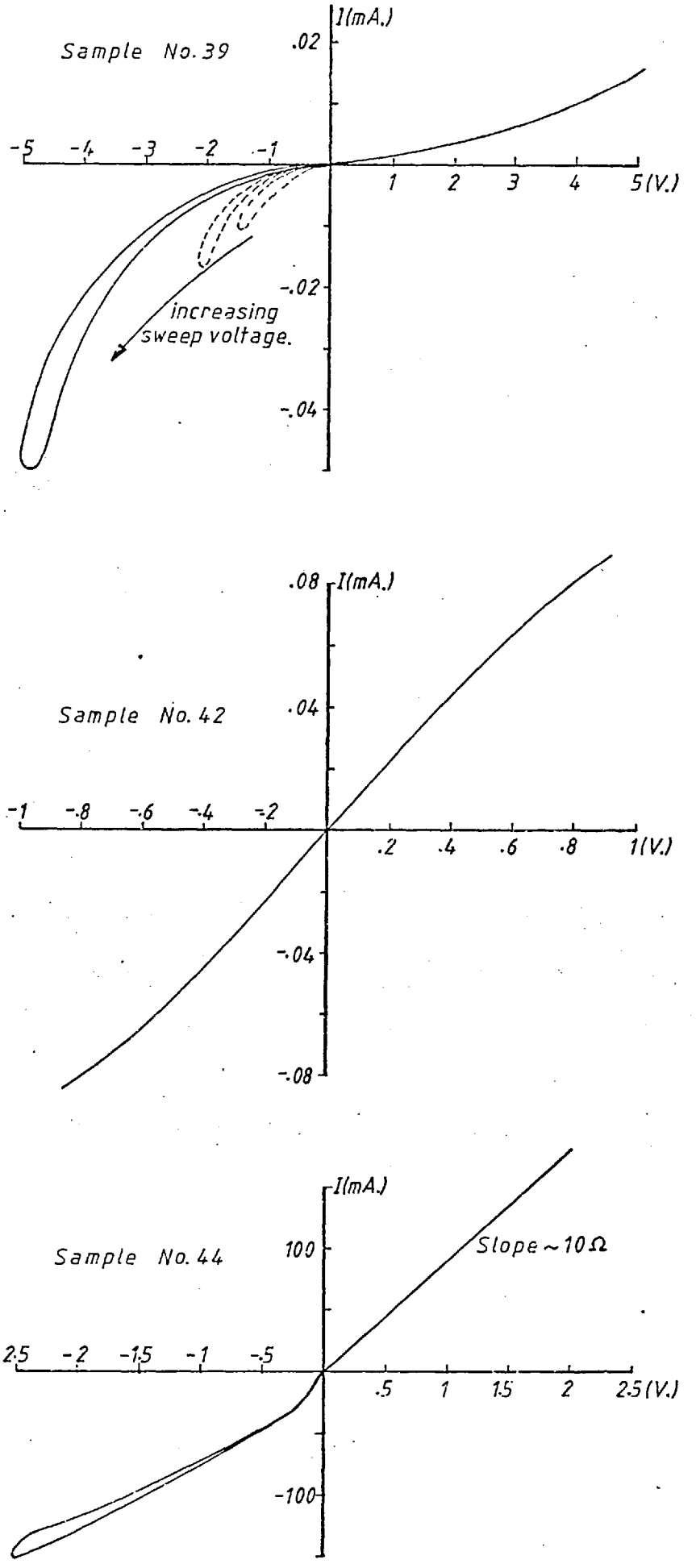

Fig. 6·4 I–V characteristics of some Au/CdSe/Cr samples taken with a curve tracer.

measurements for conductive samples were not meaningful. The capacitance-frequency (c-f) measurements for a resistive sample is shown in Fig. 6.5. At high frequencies the capacitance approached a constant (31 pF (i.e. 0.395 $\mu F\ m^{-2}$) for this sample which has a thickness of 2.4 μm). By assuming a parallel plate configuration, the dielectric constant computed for such samples were in the range of 11 ± 0.5 which is consistent with the value of 10 observed by others[2]. The low frequency C-V characteristics are shown in Fig. 6.6. Although the capacitance varied much more slowly than $V^{-\frac{1}{2}}$ (eq. (2.48)), it clearly showed the non-symmetrical behaviour. This indicated the presence of potential barriers and the measured capacitance was influenced by their changes in response to the applied voltage.

6.2.2 Cr/CdSe/Au Samples (Fig. 6.1b)

All samples with this configuration showed non-symmetrical I-V characteristics. The bias direction was such that it was more conductive (forward bias) when the gold electrode was at positive voltage with respect to the CdSe. This is the correct sense for an n-type semiconductor Schottky barrier. Typical dc I-V curves are shown in Fig. 6.7. Clearly they were far from obeying the ideal diode equation. Since the bulk resistivity of the CdSe was very high, one therefore expects that the forward bias current would be partly limited by it. Thus the model is one of a Schottky barrier in series with a resistance R_s. The value of R_s

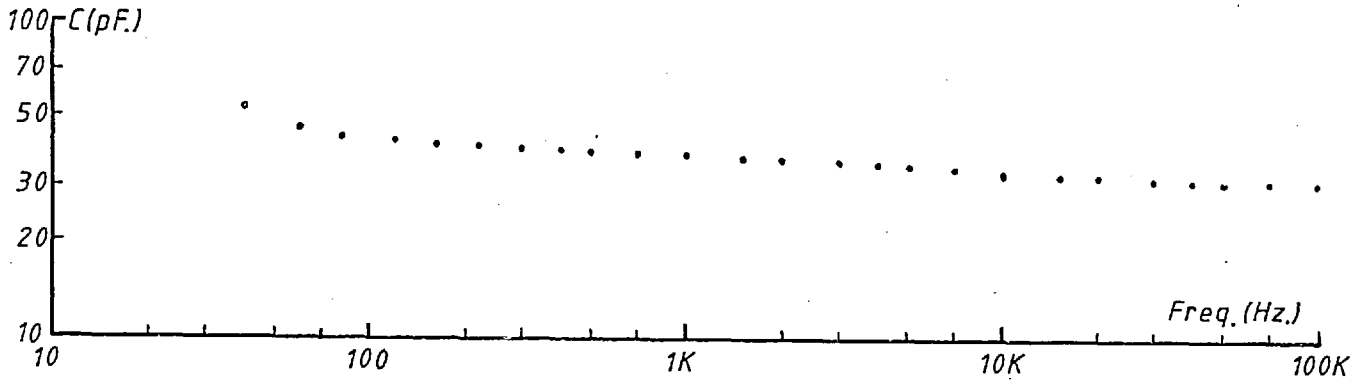

Fig. 6·5 C — f characteristics of sample No. 30

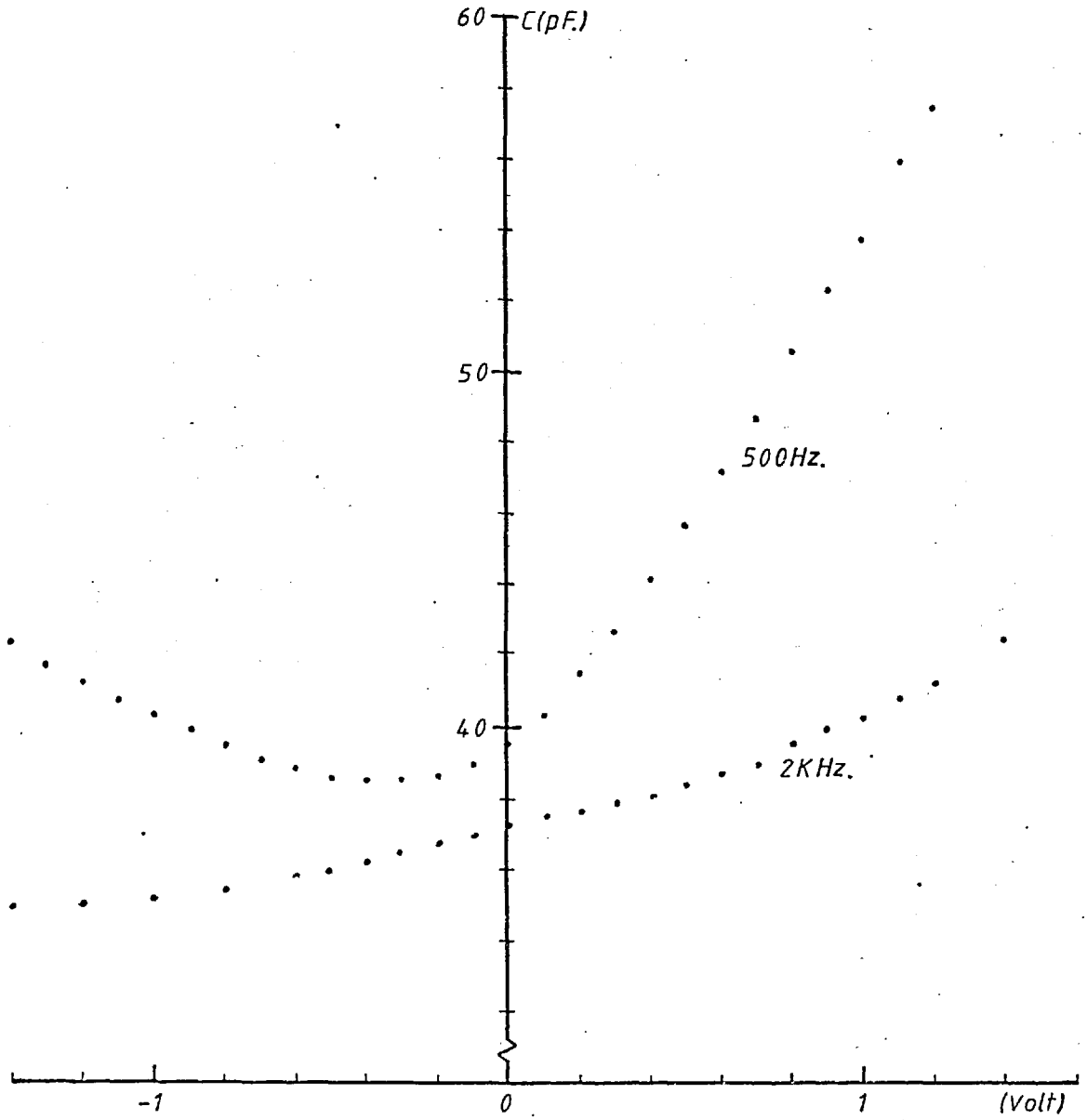

Fig. 6·6 C—V characteristics of sample No. 30

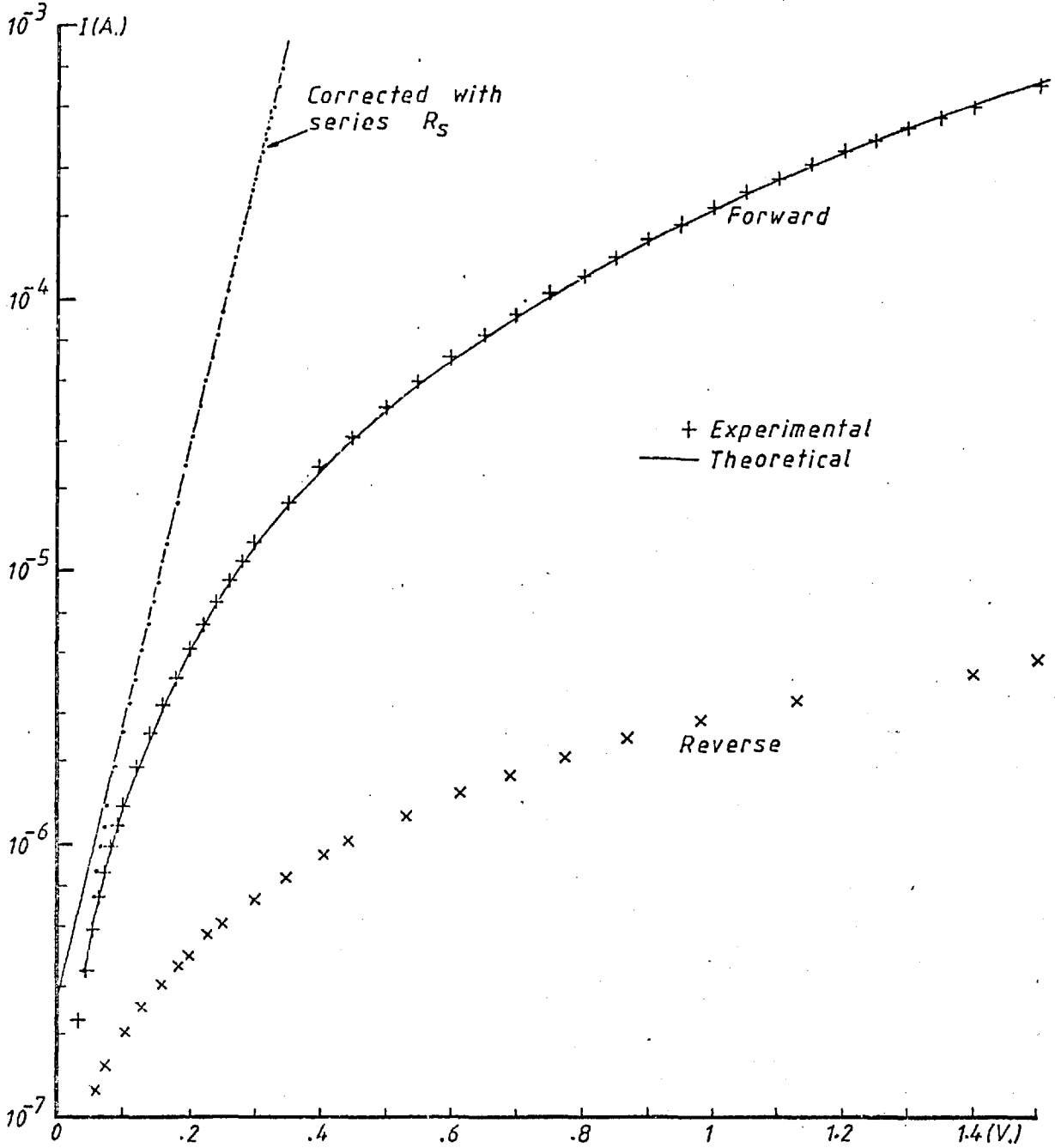

Fig. 6·8 I–V characteristics of sample No. 50

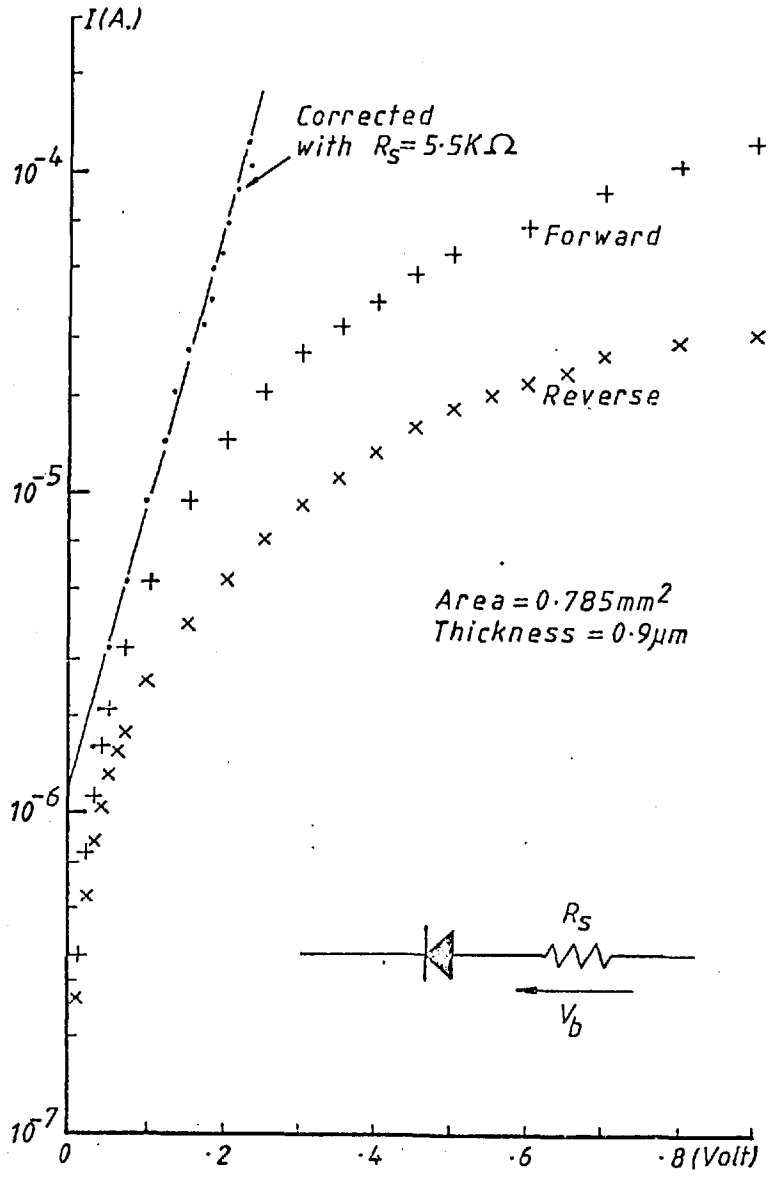

Fig. 6·7 I–V characteristics of sample No.40

was chosen in such a way that the resultant forward current of the barrier increased exponentially with the voltage across it. Fig. 6.7 shows the result of sample No. 40 corrected with R_s = 5.5 KΩ (4.8 K Ωm). The slope of the deduced log I-V curve gave an ideality factor η (eqn.(2.49)) of 1.9. The intercept on the log I axis gave the saturation current (I_s = 1.25 x 10^{-6} A), which from eqn. (2.44) gave a barrier height of 0.64 eV. Measurements on samples of differing resistivity showed that η was in the range of 1.5 to 2. R_s of course varied according to the bulk resistivity and ranged from a few 100 Ω to a few 10 KΩ. The barrier height also varied from 0.63 eV to 0.7 eV.

Actually, for many samples, R_s was not a constant especially at high applied voltage. Attempts made in order to find the relationship between R_s and V_b, the voltage dropped across R_s, showed that the following empirical formula was generally,but not always, obeyed:

$$I = A\ V_b\ \exp(B\sqrt{V_b}) \qquad (6.1)$$

where A and B are constants and I is the current through the sample. A particularly good fit was observed for one of the samples (No. 50). This is shown in Fig. 6.8 with values of A = 3.75 Ω^{-1}, and B = 2.445 $V^{-\frac{1}{2}}$. From these, it was deduced that η = 1.7 and gave a barrier height of 0.682 eV.

Some ac I-V sketches obtained with a curve tracer are shown in Fig. 6.9. All samples have very soft reverse bias current and hysteresis was present. This showed that trapping effects were very serious. Samples showing higher conductivity also had proportionately larger reverse current.

Because of the high reverse current, C-V measurements were difficult to make and the results might not be very meaningful as will be explained below Fig. 6.10 is a typical plot of C^{-2} vs V. A straight line was obtained, in accordance with eqn. (2.48), but only at very low bias values of less than 0.1 volt for this sample. The slope of this line gives a doping density of 6×10^{21} m^{-3}. However, because the voltage range covered was so narrow, it is doubtful that the capacitance was due directly to the variation of the depletion width. Furthermore, the intercept on the V axis gives a barrier height of 0.05 eV whereas the forward dc I-V gives a value of 0.64 eV. Also, at a reverse bias of -0.4 volt, the capacitance as observed on the bridge indicated zero value. This is not reasonable because the least capacitance expected would be the geometrical capacitance due to the area A (0.785 mm^2) of the electrodes and the thickness d ($\sim$1 μm) of the CdSe film which should have a value of $C = \varepsilon_s A/d \sim 70$ pF.

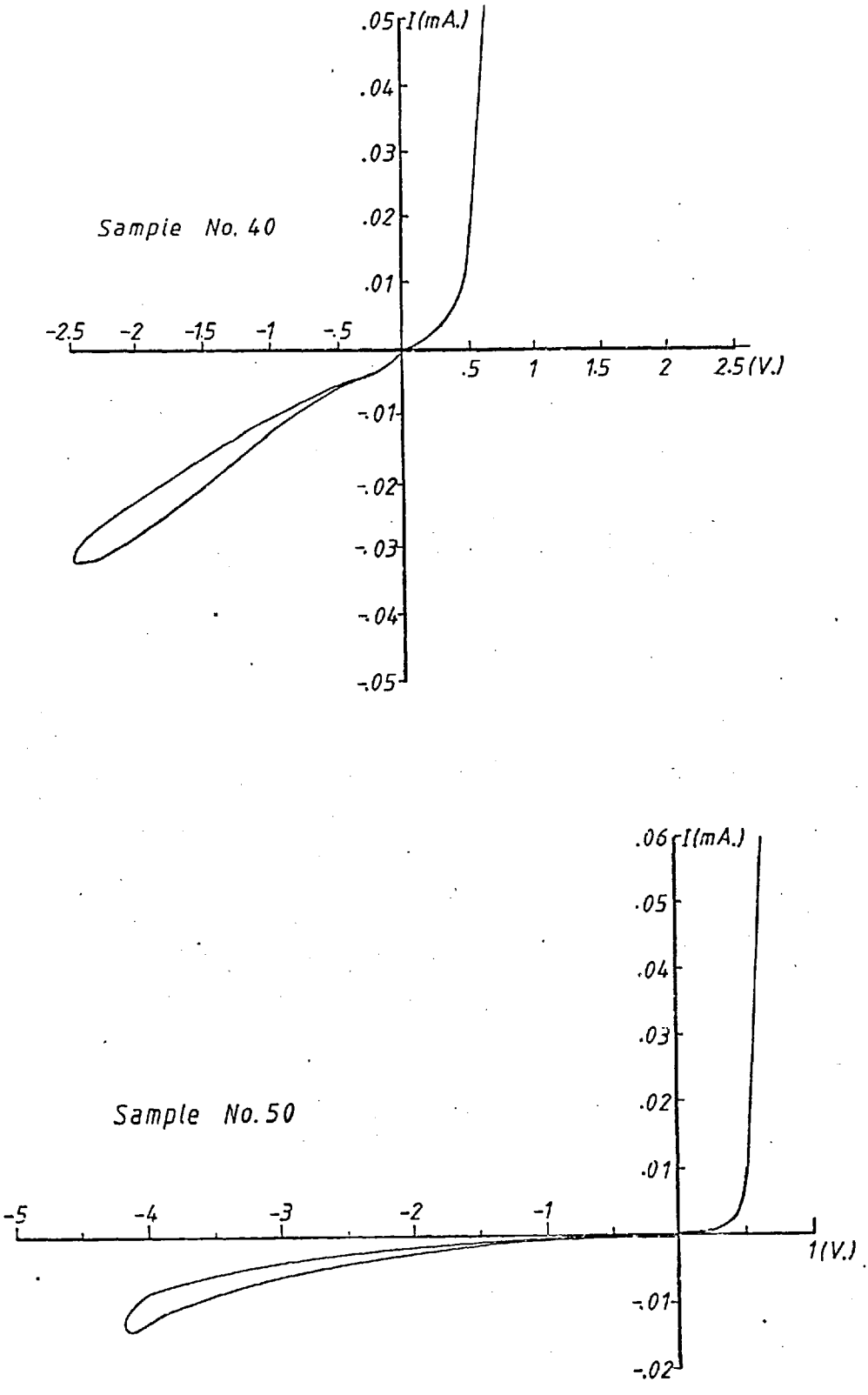

Fig. 6-9 I–V characteristics of some Cr/CdSe/Au samples taken with a curve tracer.

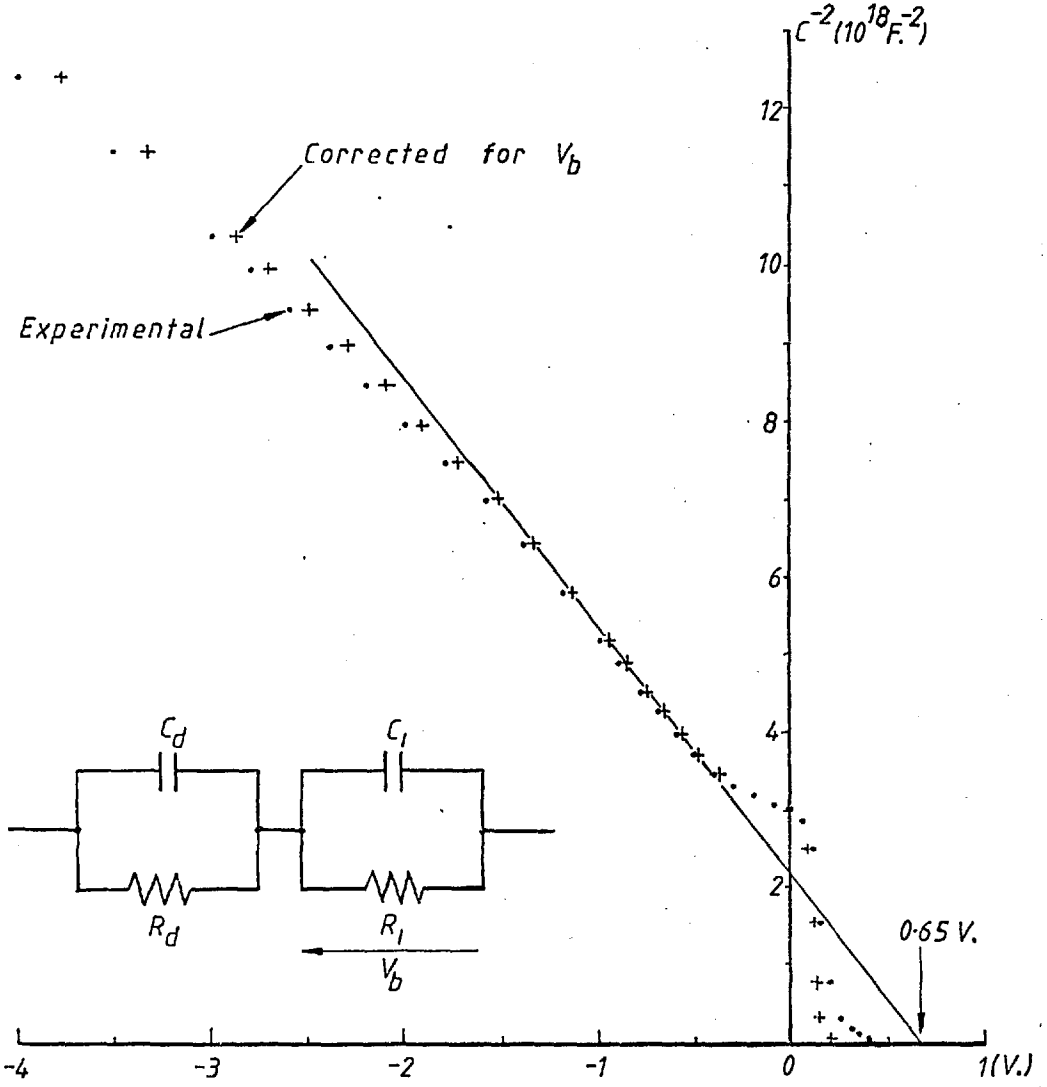

Fig. 6·11 $C^{-2}-V$ plot of sample No. 50

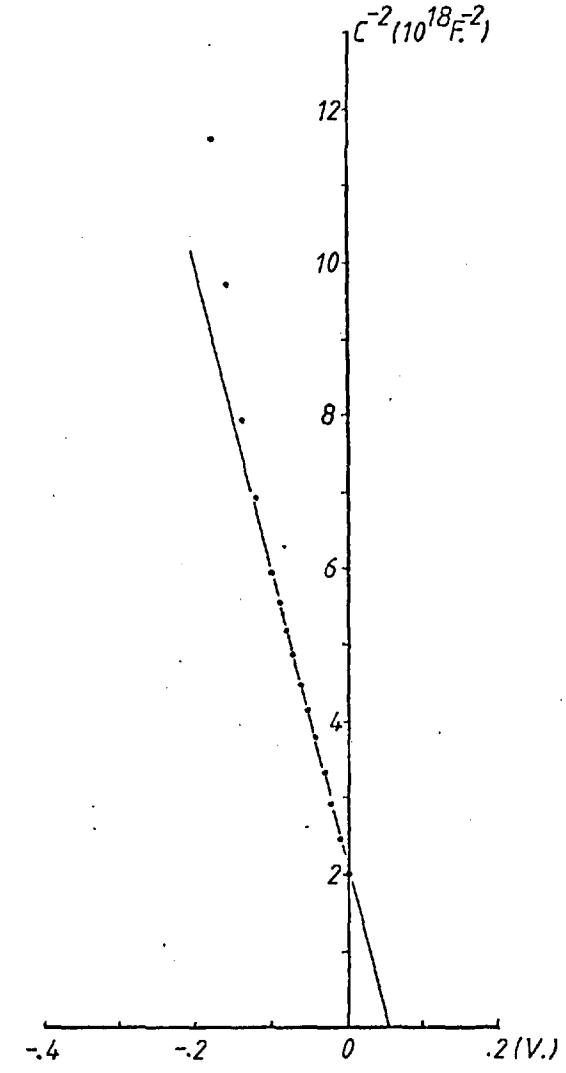

Fig. 6 10 $C^{-2}-V$ plot of sample No. 40

The C-V characteristics of the sample (No. 50) which has a harder reverse bias current (Fig. 4.6b) is shown in Fig. 6.11. The reverse bias capacitance behaved much more 'normally'. Because of the large bulk CdSe resistance, it is necessary to make a correction for the dc voltage across it according to eqn. (6.1). This is done and shown in Fig. 6.11. The corrected points give an approximately straight line at low reverse bias which cuts the V axis at 0.65 V. This is about the same as the barrier height of 0.68 eV deduced from the forward I-V characteristics. The slope of this line gives an effective doping density of 7×10^{22} m^{-3}. However, there are several points that need to be discussed. Firstly, the ac equivalent circuit should be represented as in the insert of Fig. 6.11 where R_l is the bulk differential resistance given by (from eq. (6.1)) $R_l = dV_b/dI$; C_l is the capacitance between the chromium contact and the edge of the depletion space charge region, $C_l = \varepsilon A/d \sim 2.6 \times 10^{-10}$F ($d \sim 0.3$ μm); R_d is the conduction differential resistance of the barrier given by (from eqn. (2.44)) $R_d = dV/dI = \beta I_o \exp(\beta V)$; and C_d is the depletion capacitance which as estimated from the barrier height, has a value of about 5×10^{-10}F for this sample. The measuring frequency was 5 KHz, and with appropriate values substituted into these parameters, it was found that $R_l < 30\ \Omega$, $1/wC_l \sim 130$ KΩ, $R_d > 100$ KΩ, and $1/wC_d > 70$ KΩ. Examining these, one sees that the combined impedance of R_d and C_d was always greater than that of R_l and C_l. Therefore the measured impedance might be considered as dominated by R_d and C_d but with small deviations due to R_l

and C_1.

The other serious deviation was the behaviour of the capacitance near zero bias which showed that the depletion width was pinned irrespective of the bias voltage. This effect might be due to the presence of traps in the grain boundaries. These traps would pin the Fermi level so that the width of the Au/CdSe space charge region was no longer increasing smoothly as the square root of the reverse bias voltage. In general, the presence of trapping states would seriously affect the measured capacitance of the samples. Also, the polycrystalline nature of the CdSe film means that it is necessary to use a 3-dimensional model to solve the Poisson's equation (eqn.(2.12)) rather than the simple 1-dimensional method described in chapter 2. Despite these possible deviations, the experimental fact that C^{-2} increased roughly linearly with the reverse bias voltage encouraged one to interpret it as with a single crystal semiconductor Schottky barrier.

6.3 ATTEMPTS TO IMPROVE THE CHARACTERISTICS

When samples are produced under similar environments and conditions, one normally expects that their characteristics should not differ too greatly from one to another. In the present case, not only was the reproducibility poor, but also virtually all samples showed I-V characteristics which were considered not good enough for our purposes. Therefore it was hoped that if reproducibility could be achieved, then more quantitative analysis could be carried out to identify the conduction mechanism, which in turn should enable one to find ways of improving the characteristics. The most critical factors which affect the electrical properties of a semiconductor are its structure and impurity contents. CdSe films evaporated on a glass surface are polycrystalline, the structure of which is seriously affected by the evaporation conditions. Since no impurities were deliberately introduced, the net doping density was mainly from structural defects such as vacancies and interstitials, etc. It had been shown[3] that Se vacancies give n-type conductivity whilst Cd vacancies act as compensating acceptors. Therefore the stoichiometry of the condensed films has a great influence on its conductivity. When the CdSe source powder is heated to above 600°C, it dissociates into Cd and Se atoms[4] which recombine on the cooler substrate surface. Since these elements have different vapour pressures, the stoichiometry of the condensed film is affected by the substrate temperature, source temperature, evaporation

rate and total (accumulated) time of evaporation since the source was refilled.

Various authors[1,5] have observed the dependence of conductivity on the evaporation rate. This rate is directly controlled by factors such as:

(a) the source-substrate distance:
This was kept constant in these experiments.

(b) the source temperature:
Initially, a few samples were deposited with different source temperatures. However it was found that the irreproducibility could not be directly related to this, so subsequent samples were deposited with a source temperature held at 720°C.

(c) the amount of quartz wool and the way it was packed on top of the source powder:

Although it could not be absolutely certain that this was being done in exactly the same way for all refills of the source, experience showed that with all other parameters kept constant, the rate of deposition remained fairly constant for different batches, being in the range of 2 to 2.5 nm s^{-1}.

The total time of evaporation since the crucible was refilled would affect the stoichiometry because the constituent with a higher vapour pressure (Se in this case [5,6]) would leave the compound more readily than the other so that samples from a freshly charged source would be more stoichiometric while subsequent samples would be rich in Cd since the source was depleted of Se. For each refill of the crucible about six films could be deposited. One would then expect that the conductivity of the films should change systematically from one sample to the next[8]. However, this was not observed, for instead their conductivity varied randomly.

Generally, the substrate temperature affects the condensation rate, crystal sizes and stoichiometry. At a temperature of about 200°C, a stoichiometric compound would be expected[7] so that the conductivity should be much lower[1,9] than that below 160°C which would give a Se deficient film. However, in our case, CdSe films deposited onto heated substrates were always more conductive than those deposited at room temperature. For a substrate temperature T_s of less than 200°C during deposition and decreased to room temperature within about 30 minutes after that, softer forward and reverse characteristics were observed on Cr/CdSe/Au samples. But if T_s was held for a further hour before being decreased to room temperature, the CdSe film became essentially a short circuit with no asymmetry in the I-V characteristics.

If T_s was above 200°C, the CdSe surface appeared milky; the electron micrograph of the surface replica was shown in Fig. 4.12b. These samples were again very conductive and non-rectifying. It was therefore apparent that although a heated substrate greatly altered the effective conductivity of the CdSe, no improvement in its rectifying characteristics could be achieved.

Annealing a sample should generally assist grain growth and reduce strains[20], resulting in a more stable sample, and so it was hoped that this would improve reproducibility. The annealing atmosphere was either pure Ar, N_2, 90% Ar/10% O_2 mixture or in vacuum. The annealing temperature T_a was from 200°C to 350°C. For most samples, the CdSe films peeled off if T_a was greater than 350°C. For T_a below 350°C, it was necessary to increase it slowly over a period of an hour so as to prevent peeling off. The specimens were removed from the oven after annealing only when it had cooled down to room temperature. The cooling down period lasted for more than two hours and the specimens were usually left overnight. The actual annealing time was from 2 to 6 hours. The results of the annealing procedure showed that irrespective of the type of gas used, the samples became very conductive and non-rectifying.

It was also suspected that contamination from foreign matter might have been unintentionally introduced into the CdSe films. These impurities might then seriously affect their conductivity. The most likely origin of these impurities was from dirty components in the vacuum system. These components were the stainless steel sheets used to shield the evaporation and sputtering sources and used to make other items such as the shutters, the Duralumin substrate table, and electrical lead-throughs. These were all thoroughly scrubbed and cleaned constantly throughout the project. To minimise gaseous inclusion, the evaporation crucible (with no CdSe powder) was out-gassed at 850^{o}C for more than an hour (actual CdSe deposition was carried out at 720^{o}C and lasted for only 7 minutes) and then held at 150^{o}C for more than 15 hours while the whole vacuum chamber wall was baked at 70^{o}C with heating tape. Even after these procedures, there was still no sign of any improvement in the CdSe characteristics.

6.4 GENERAL DISCUSSION

The absence of rectifying behaviour when the gold film was put on the top surface of the CdSe film obviously indicates that there were differences between the interfaces on the top and the bottom of the CdSe. It was quite possible that for the case of gold deposited on top of the CdSe, the CdSe surface might be damaged by the sputtering process. However, a few samples were made in which the gold contacts were deposited by evaporation also showed no rectifying behaviour. Similar problems were also encountered by Nakai et al.[10]. One of the most likely explanations for this difference is that surface contamination from residual gases in the vacuum system might have occurred. According to the kinetic theory of gases, the impingement rate of gas molecules onto a surface is $P/(2\pi MkT)^{\frac{1}{2}}$ where P is the pressure and M is the mass of the molecule. Since the chamber pressure was only 10^{-6} torr, a surface would therefore be covered with a monolayer of oxygen in about two seconds. (This assumes unity sticking coefficient and that the residual gas consisted of oxygen only, which of course are both not true. However this gives a general idea of the rate involved.) It is therefore very likely that the CdSe surface had been very much contaminated and was accumulated with majority carriers so that the contact potential became independent of any external metal put over the surface subsequently. In the case of the gold surfaces, since gold is relatively

inert, either they remained relatively clean or the adsorbates were of acceptor-like species which did not cause the CdSe surface to be accumulated with majority carriers when it came into contact with them. To test this hypothesis directly, it is necessary to reduce the chamber pressure to below 10^{-8} torr. Unfortunately this could not be done in the system used.

Another possibility is that there were differences in the electric nature of the two CdSe faces due perhaps to the crystallographic orientations of the poly-crystals. For instance, one interface may be mainly between gold and cadmium atoms whereas the other is mainly between gold and selenium atoms. Because of the difference in work functions and surface states of the two elements, this would therefore give rise to different interfacial properties. Some evidence of preferential orientations of the evaporated CdSe films were found in the crystallography work described in section 4.10 in which it was mentioned that the CdSe might crystallise preferentially with the (OO.1) (wurtzite) plane parallel to the substrate surface. The third possible cause of different interfaces is due to the crystallite orientations of the underlay electrode. Fig. 4.13b showed that the deposited gold film was highly preferentially orientated in the (111) planes. The gold film was thus not very much different from a single crystal film and so the CdSe film might tend to

grow epitaxially at least in the initial stage of growth. A cross-sectional view of the sample may thus be as shown in Fig. 6.12. This resulted in a better crystallised CdSe film which was able to support a thicker space charge region. Consequently the tunnelling effect on the bottom interface was very much reduced compared with that of the top. A.C. measurements showed signs of slight current saturation in both bias directions for some of the Au/CdSe/Cr samples (Fig. 6.4b). This may be taken as due to the presence of depleted space charge regions at both the Au and the Cr interfaces. However, their thicknesses were so small that the conduction processes were completely dominated by tunnelling assisted by trapping states at the level of the metal Fermi level, and hence no blocking effect was observed in the dc measurements.

For those films deposited on heated substrates or annealed after the depositions, the consequences were contrary to expectations that the rectifying characteristics would improve since this might result in a more perfect film with larger grains and less defects[11]. Instead all heat treated CdSe samples became very conductive. Though this might be due to the fact that the decrease in structural imperfections also meant a reduction in trapping sites, and also the carriers need to cross fewer grain boundaries. However, it is believed that the reason is more likely to be due to the high diffusivity of the contact metals along the grain boundaries of the CdSe[12]. High diffusivity was demonstrated by the following experiment. A very thin

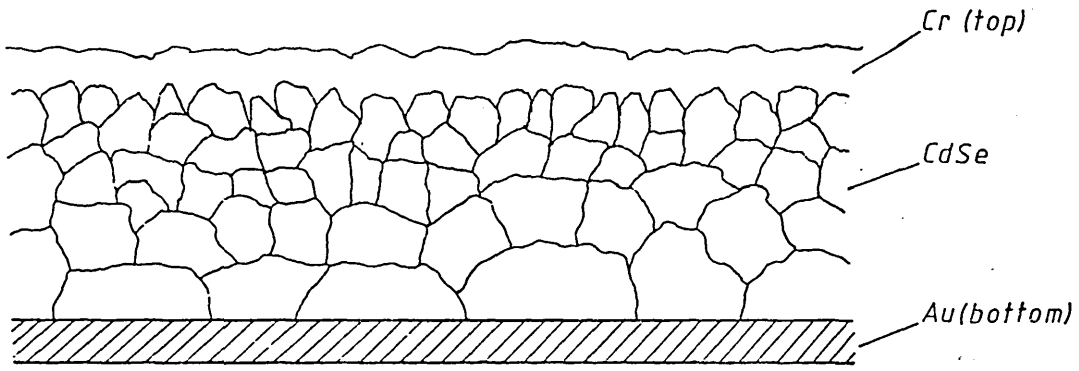

Fig. 6·12 Cross-sectional view of a Cr/CdSe/Au sample.

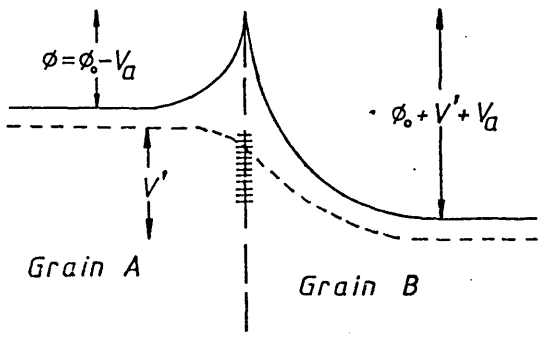

Fig. 6·13 The energy band diagram for grain boundary conduction.

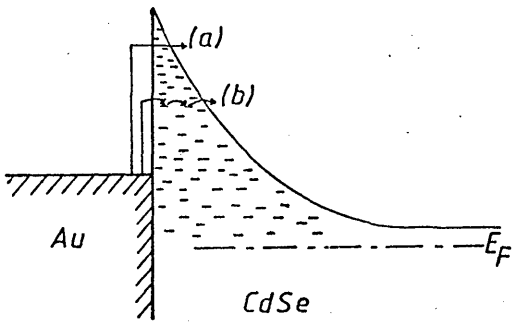

Fig. 6·14 Tunnelling mechanisms: (a)Thermally assisted, (b)Trap assisted.

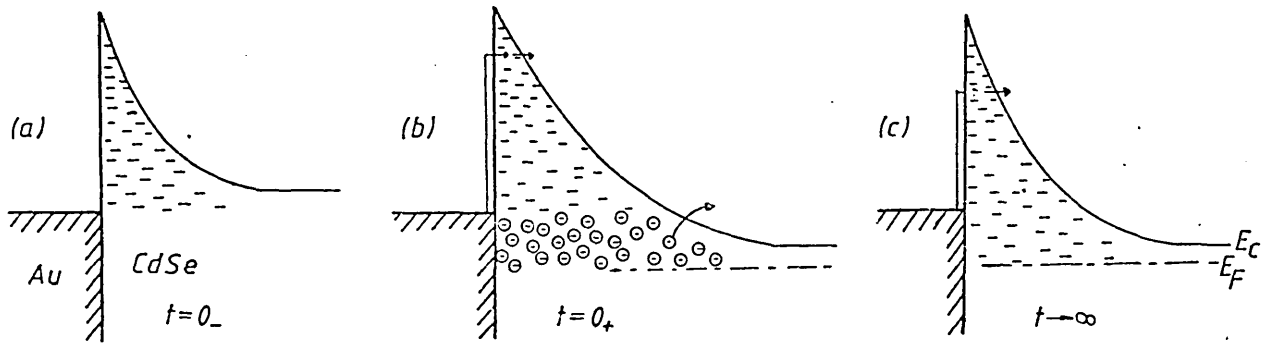

Fig. 6·15 Energy band diagram showing the increase of current with time under a reverse bias step voltage.

gold film (~10 nm thick and area 10 x 20 mm^2) was deposited on top of the CdSe surface. This film was clearly visible before annealing, but after annealing in pure N_2 at 200°C for about an hour, it completely disappeared from the surface. Since it was unlikely to have evaporated, it was concluded that it must have diffused into the CdSe bulk.

For those samples showing rectifying characteristics (gold contact on the bottom surface of the CdSe film), the forward current was very much limited by the bulk resistance of the CdSe. The conductivity of the bulk was not always constant but appeared to vary approximately exponentially with bias voltage. There are many mechanisms which may give rise to this variation. Because of the polycrystalline nature of the films, the most obvious one is that the transport of free electrons in the conduction band is limited by the grain boundaries[13,14]. The electron micrograph of Fig. 4.10 showed that the grain size was around 40 nm. Assuming spherical grains, then for a CdSe film thickness of 1 μm, there would be about 20 grain boundaries across the thickness. The energy band diagram of two crystallites separated by a grain boundary may be drawn as in Fig. 6.13. The trapping states in the boundary are assumed to be acceptor-like so that two space charge regions are set up. Using the model of thermionic emission of carriers over the potential boundary as discussed in section 2.5, it can be shown that the net current density is given by[13]

$$J = \frac{1}{4} \bar{v}\, n\, q \exp(-\beta\phi_o) \exp(\beta V_a) \left[1 - \exp(-\beta V')\right]$$

where $\bar{v}$ is the carrier velocity, n is the density, ϕ is the potential height of the grain boundary, ϕ_o is the value at equilibrium and V_a is the change in ϕ on grain A due to bias voltage V' across the grain boundary. The term in the square bracket is either increasing linearly with V' when small or is unity when V' is large. Therefore the current or conductance increases approximately exponentially with applied voltage since V_a is likely to vary slowly with V'. However, this model assumes that each grain is a perfect single crystal so that the transport of free electrons is limited only by the idealised grain boundary potentials (apart from the normal scattering processes of free carriers in a semiconductor). It is also possible that the carrier movement is limited by traps. Each of these traps may sit in a potential well so that the trapped carrier needs to climb the potential in order to leave it. Under an applied voltage, V, the potential height will be lowered by an amount proportional to the square root of V. This is the Poole-Frenkel model[15] which gives

$$I = CV \exp(\beta_{PF} (\frac{V}{d})^{\frac{1}{2}}/2kT)$$

This expression is similar to the experimentally observed one of eqn. (6.1). The value of β_{PF} is $(q^3/\pi\varepsilon_o\varepsilon_s)^{\frac{1}{2}} = 3.8\times10^{-24}$ $m^{\frac{1}{2}}V^{\frac{1}{2}}$. Taking d, the bulk thickness of the CdSe, equals to 0.3 μm, the slope of log I/V vs $V^{\frac{1}{2}}$ should be 0.85, which is close to the value generally observed. Another possible

mechanism which might give rise to such low forward current is due to the charging of trapping centres in the space charge region of the Schottky barrier, and this will be discussed in the next paragraph. For the moment, it is worth pointing out that the ideality factors η (eqn. (2.49) deduced were all close to 2. As discussed in section 2.5.3, this high value of η indicates the dominations of a recombination process in the space charge region.

The extremely soft reverse current is believed to be due to a combination of a number of factors such as tunnelling, interfacial layer, and image force lowering. The effect of tunnelling is especially severe because (a) the effective donor density of the CdSe film is very high. The C-V measurement of the 'best' diode showed that this was about 7×10^{22} m^{-3} and might be much higher for others. Therefore the depletion width is very thin so that electrons from the gold electrode need not have to surmount the whole barrier height (Fig. 6.14a, thermally assisted tunnelling). (b) The presence of trapping sites in the CdSe may assist the electrons to tunnel in steps (Fig. 6.14b, trap assisted tunnelling), effectively increases the tunnelling distance. (c) This mechanism is inferred from the drift effect of the current when V was applied. Under reverse bias, the current always increases with time. This may be due to detrapping of trapped charges in the space charge region.

Fig. 6.15 shows the presence of charged traps which might be in the grain boundaries, the crystallite bulk, or in the interfacial layer which exists between the gold and CdSe interface, as treated by Thanailakis[16]. At zero bias, Fig. 6.15a, traps above the Fermi level are empty of electrons. Under a reverse bias step voltage, Fig. 6.15b, detrapping occurred so that the net positive charge density increases with time, resulting in a decreasing depletion width (Fig. 6.15c). This effectively resulted in a lower barrier height and hence an increased current. The converse is true for the case of a forward current in which the traps are being filled, giving rise to a lower net space charge density and a thicker depletion width. This, therefore, explains the decreasing forward current with time and hence the very poor rectification ratio.

6.5 SUMMARY AND CONCLUSION

In experimenting with evaporated CdSe films, the lack of rectifying characteristics when the gold contacts were put on the top surface meant that measurements have to be carried out on samples with gold contacts on the bottom. This latter configuration is not suitable for the ultimate aim of fabricating vidicon targets. Furthermore, their rectifying I-V characteristics were very similar to those of the early day rectifiers[17]. Such poor rectifications were the consequence of large impurity densities and highly defective crystalline structures whose presence in a semiconductor material give rise to thin space charge region and high density of trapping states. For the case of evaporated CdSe thin films, they always exhibit n-type conductivity. This suggests that their electrical properties are much more seriously affected by intrinsic defects of the film rather than by foreign contaminents. These defects include non-stoichiometry and other imperfections such as interstitials, vacancies,strained atomic bonds and grain boundaries. These factors are very sensitive functions of the film growth conditions. In particular, films grown on cool substrates are more likely to be in a highly meta-stable state with small grains and high strains within the grains. This is a direct result of the lack of atomic mobility. Such films may therefore be very unstable and give rise to large variations in characteristics (conductivity) as were observed in the experiments. These large fluctuations

effectively prevented one from carrying out any quantitative analysis on their characteristics because even if a certain mechanism could be identified for a particular sample, it could not be verified with other samples. Attention was therefore paid in trying to improve the reproducibility. It was hoped that these undesirable effects could be reduced by depositing the films onto heated substrates and/or through annealing after the deposition. This may then also lead to a more useful or better I-V characteristic from which the conduction mechanism may be deduced. Unfortunately the configurations of the specimens were such that heat treatments had to be carried out with at least the underlay metal in contact with the CdSe. As a result, the very high diffusion rate of the metal atoms along the grain boundaries caused the thin CdSe film to be effectively shorted from top to bottom after only a few minutes of annealing at a temperature as low as 200°C. This problem of high diffusion rate of the contact metal may be overcome if a diffusion barrier can be created at the interface[12]. This may be in the form of a very thin material which is mutually immiscible with both the metal and the CdSe and has very low grain boundary diffusivity in the CdSe. Wronski et al[18,19] have been experimenting with vidicon targets made from CdSe films evaporated onto SnO_2 conducting glass. Their samples were baked in air at 350°C for 30 minutes. They showed that the dark current was decreased by more than

an order of magnitude as a result of such heat treatment, and apparently showing no sign of tin diffusion from the SnO_2 into the CdSe film. This might be due to the high bonding energy between tin and oxygen atoms in the SnO_2 which therefore prevented the tin atoms from leaving the SnO_2 material. Oxidation might also have taken place on the CdSe surface thus forming a diffusion barrier against subsequent materials deposited on top. Therefore such films were not only free of metallic conducting paths in the grain boundaries but also have fewer defects within the grains. Annealing therefore improved their characteristics of being used as vidicon targets. This seems to suggest that pure metal is inappropriate for use as the backing contacts. However, about 15 samples were made by the present author in which the underlay material was indium-tin-oxide conducting glass R.F. sputtered from an In_2O_3 (16 atomic percent): SnO_2 mixture target onto soda glass slides. The characteristics of such samples showed no differences from others. As a consequence of the unsuccessful attempts to improve their characteristics, it was decided that the main experiments of cermet contacts on semiconductor could not be performed on such samples.

With the silicon wafers, the characteristics were found to be critically affected by surface effects. This problem is common to all semiconductor devices whose operations rely partly or wholly upon surface actions. With such devices, the nature of the surface must be properly controlled during the fabrication processes.

Electronically, the surface state density is the most important parameter that influences the device behaviour. These surface states arise from three sources: (i) sudden termination of the periodic crystal potential, (ii) presence of foreign impurities, and (iii) surface damage. Conventional MOS devices are successful because of the ability to produce them with very low surface state density. This is achieved by well-controlled oxidation of the silicon surface. The essential of cleanliness of the environments in which the devices are fabricated is well known. The oxidation procedure and the necessity of post-baking at high temperature ($\sim 500^{o}C$) ensure that surface (or interface) damage is reduced to a minimum. The change in crystal potential in going from the silicon single crystal into the SiO_2 also may not be so abrupt because of the good lattice bonding at the interface, resulting in a reduction in the intrinsic surface states. This technology and the almost unique interface nature of $Si-SiO_2$ contribute towards the fast pace of progress in silicon devices compared with those made from other semiconductor materials.

For the case of the specimens used in this project, the procedures with which they were prepared were not favourable for fulfilling the above-mentioned requirements. The process of sputter deposition of the

surface films (SiO_2 or cermet) could do nothing but cause severe damage to the surface of the silicon wafer. The cleaning procedure of the silicon wafers was also rather crude. Although it was intended for removing grease, surface oxides and other foreign impurities in order to provide more intimate contact between the silicon and the deposited film, more contamination could be inadvertently introduced either from the etchant or during the drying time when the vacuum system was pumping down. The cleanliness of the vacuum system was also not particularly good, for contaminants were likely to come from the pump oil and other impurities adhering to the parts inside the chamber. These impurities might come off fairly easily when struck by the impinging sputtering plasma gas. The presence of gold atoms with cermet films may also be considered as impurities as far as the silicon surface is concerned.

The operation of a vidicon target requires that the lateral sheet resistivity of the cermet to be $>10^{13}$ Ω/square[19]. For a 100 nm thick cermet film, this corresponds to a resistivity of $>10^{6}$ Ωm which is one with a metal fraction of about 15%. This is in the range of resistive cermets in which the electrical characteristics of the contact is dominated by the response of the interface charges. The difficulty of bending the semiconductor surface potential and the large frequency dispersion both make the device as it is unsuitable for

vidicon application. On the other hand, the large variation of the capacitance against frequency in a range which can be easily shifted by the bias voltage and altered by using different metal fractions in the cermet is a very interesting feature which may have useful utilisation in electronic circuit designs.

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