SLOW STATES

IN

THIN FILM TRANSISTORS

by

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A B S T R A C T

Slow state instability effects have been investigated in thin film field effect transistors in which the insulator was radio-frequency sputtered silicon dioxide and the semiconductor evaporated cadmium selenide. Capacitance-voltage, mobility, thermopower and resistivity measurements have been performed on the polycrystalline semiconductor film of the transistor, and the results obtained interpreted in terms of the effects of trapping states at grain boundaries in the material.

The degree of slow state instability in the devices has been measured as a function of gate field, and the effects of annealing treatments examined. The time decay characteristics of the process have been observed and shown to fit a direct tunneling model for charge transfer across the semiconductor-insulator interface to insulator trapping states. The capture cross-section and volume density of the insulator trapping states responsible for the instability have been determined.

The low frequency noise behaviour of the devices has been examined, and the results related to the trapping behaviour. Also, the infra-red absorption spectra of the insulator film has been examined and certain conclusions as to the structure and composition of the material have been drawn. Identification of the state responsible for the slow trapping with electrically active oxygen vacancies in the insulator has been made.

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I N D E X

CHAPTER 1 INTRODUCTION

This thesis reports an investigation of the electrical properties of a thin sputtered insulator film which are of relevance to its use in thin film field effect devices, otherwise called thin film transistors (TFTs). In this chapter the thin film transistor will be introduced, after briefly mentioning the more familiar silicon-based equivalent device, the MOSFET. The similarities and differences between the two types of device will be discussed together with their different areas of application. Previous work on the electrical properties of insulators and the semiconductor-insulator interface is briefly described and the approach followed in the present experiments is explained. Finally, the organisation and layout of this thesis will be described.

1.1 THE SILICON MOSFET

The metal-oxide-semiconductor field effect transistor (MOSFET) has been known, in principle, for fifty years, and during the last twenty years MOSFETS built on a substrate of single crystal silicon have attained great technological and commercial importance. The technology has now advanced to the point where tens of thousands of transistors can be manufactured on a piece of silicon a few millimetres square, and interconnected to form, for example, the major part of a small computer system.

Because of the commercial importance of this technology a vast amount of effort has been applied to both the fundamental science and practical technology of every aspect of these devices. Fundamental to their manufacture is the

technique of the thermal oxidation of the surface of a silicon crystal, the resulting silicon dioxide serving as the insulator in a MOSFET. The electrical properties of the bulk of this insulator material, and its interface with the silicon are crucial to the performance and long term stability of the devices. A variety of processing methods have been determined to produce suitable electrical and physical characteristics for successful device operation.

1.2 THE THIN FILM TRANSISTOR

As originally conceived, the field effect transistor was to be made in thin film form, its active layers consisting of evaporated metal, semiconductor and insulator films. In the 1950s the great advances in silicon technology overshadowed that of thin films, and the thin film transistor has not as yet been developed to the point where it has found commercial application. Development work on these devices still continues however.

The thin film transistor consists of thin layers of material deposited generally by evaporation or sputtering in a vacuum system, in patterns delineated by thin metal aperture masks. A sequence of some half-dozen depositions is necessary to produce a completed transistor and, in the same way as for the MOSFET, a number of thin film transistors can be connected up by a final interconnection pattern to form a complete circuit.

The transistors under investigation were made with evaporated semiconductor and conductor layers, and a sputtered insulator film. The structure and deposition of the devices will be described in detail in a subsequent chapter.

1.3 COMPARISON BETWEEN MOSFET AND TFT

The MOSFET and the TFT are basically similar in that they both work by modulating the conductivity of a semiconductor by means of an electric field applied by a control electrode (the gate). There are considerable differences however, because the semiconductor has a different form in each of the two devices. In the MOSFET, where the semiconductor is a single crystal, the conduction process is well understood theoretically, and excellent agreement between theory and experiment is found.

In the TFT on the other hand the semiconductor consists of a thin polycrystalline film. The conduction process in these films is dominated by the effects of the boundary regions between the grains. The grain boundaries disrupt the crystal lattice of the semiconductor, interrupting the flow of charge carriers. The transport process in the material is in fact very complicated and not yet fully understood. The conduction of the TFT is controlled by a complicated interaction between the semiconductor surface, the grain boundaries and the gate field.[1]

As stated previously, MOSFETS have found important uses in many applications but there are certain limitations which prevent their use for some purposes. Some of these limitations do not apply to the TFT, which opens up new areas of application.

Silicon single crystal wafers are limited to a few inches in diameter which for electronic devices is ample. For some devices however, for example, display devices which have to interact with human beings, this is rather

small. One projected area of application of TFTs is in the manufacture of display devices (e.g. the "flat TV screen"). Here it would be necessary to deposit thin film transistors over the complete area of the display, and connect them up to form a circuit. Since the device is to be viewed, it has to be large, and depositing TFTs on a large substrate is perfectly possible.

MOSFETS, on the other hand, can be packed extremely densely onto the silicon wafer, but to make large silicon crystals is prohibitively expensive. There is a dividing line therefore between small, very densely packed, circuitry for which silicon MOSFET technology is eminently suitable, and large area devices of moderate density for which thin film techniques are perhaps more suitable.

In recent years, experimental display panels have been fabricated[2] involving many thousands of thin film transistors deposited over an area of many square inches, and extension of the principle to very much larger arrays would appear to be feasible.

1.4 INSULATOR INVESTIGATION IN MOSFETS

The thermal silicon dioxide of the MOSFET, and its interface with the silicon surface, have been intensively studied during the past 20 years. The volume of literature generated is so great that a complete survey is not possible. Many reviews of the subject have been made, and the reader is referred to two recent such by Williams[3] and Nicollian[4].

The conditions under which the silicon surface is oxidised, and subsequent annealing of the device, are

crucial to the fabrication of material with good electrical characteristics. The electrical behaviour of the interface is closely connected with the stoichiometry of the silicon dioxide. The highly stable characteristics of the silicon-silicon dioxide interface are due to the very close degree of control of the material composition which is obtainable by the thermal oxidation technique.

The charge centres in the insulator and at the semiconductor-insulator interface can be divided into two broad groups - fixed charge centres, and those which are capable of trapping and localising charge. The fixed charge centres are those whose occupancy does not change under the influence of the gate electric field, while the latter group of states do so change their occupancy. These states are located close to or at the interface, where they can exchange charge with the semiconductor with varying degrees of probability. It is these states which tend to change the characteristics of the transistor when in operation.

1.4.1 Effects of Silicon Dioxide on MOSFET Performance

Early MOSFET devices were very prone to drift of their characteristics on varying timescales - from seconds to hours. It was discovered that much of the instability was caused by charge movement in the insulator material caused by the operational gate field, movement of charge initially "built-in" to the insulators, and charge injected into the insulator across the semiconductor-insulator interface. Technological processing steps have been found which reduces such effects to a level sufficient for the operation of the devices, and considerable theoretical

understanding of the underlying physical process has been achieved.

Among the main causes of variation of MOSFET characteristics were found to be charged ion drift in the insulator, and trapping (localisation) of charge in defect states in the insulator material and at the interface.

The transistor characteristic which is of most importance, and is also easily measurable, is the threshold voltage. This is the voltage which must be applied to the gate of a MOSFET to initiate conduction in the semiconductor. The effect of processes described above is to cause short or long term changes of this parameter to varying extents. These changes can drastically upset the operation of circuits incorporating MOSFETs and even cause them to cease working.

The simplest way of measuring the changes of threshold voltage is by examining the capacitance-voltage characteristics of an MOS capacitor[5]. This method has the advantage that it is not necessary to fabricate a complete MOSFET, which requires source and drain diffusion steps, but the experiment can be simply performed on the oxidised silicon slice with a metal gate deposited on top.

The threshold voltage is perhaps the most important, but not the only, parameter of the MOSFET which is influenced by charge trapping. Among others so influenced are the transconductance (gain) of the device, the low frequency noise behaviour and the drain and source junction breakdown voltages. The effect on the transconductance is caused by variation of electron or hole mobility in the conducting channel region between source and drain, caused

by the non-uniform potential of the charge localised in states close to the interface. The regular periodicity of the crystal lattice is disturbed by the random component of the potential, so scattering carriers out of the single crystal Bloch wave functions, and reducing their mobility, in much the same way as for impurity scattering. When the occupancy of the centres is changed by the gate field, the mobility changes correspondingly.

Noise, that is, random fluctuations of the current flow in the transistor, is caused by, among other mechanisms, the random capture and re-emission of charges by trapping states. In the process, the phase information carried by the electron or hole is lost, resulting in the production of random noise. Trapping centres have a wide spread of time constants, so the noise spectrum covers a correspondingly wide frequency range.

The junction breakdown voltages are changed by trap occupancy because the field due to charged trapping centres causes accumulation or depletion regions to form in addition to those caused by the field across the reverse biased electrode-substrate p-n junction.

1.4.2 Control of Silicon Dioxide Properties

The aim of controlling the processing conditions of MOSFET devices is to reduce the density of both fixed charge states and interface states to a sufficiently low level that the device characteristics are not adversely affected by them. The means for achieving this end is control of the oxidation process (temperature, time, gaseous ambient) and post-oxidation annealing treatments.

To reduce interface state densities either a low ($350^{o}C$) or high ($1000^{o}C$) temperature anneal is used, the former after an aluminium layer has been deposited to the gates of the MOSFETs. In the low temperature anneal, it is thought that atomic hydrogen, formed by the reaction of water in the oxide with the aluminium, chemically reacts with the interface states to annihilate them. In the high temperature anneal direct thermal reduction of the centres occurs.

Fixed charge density is affected considerably by the conditions of oxidation, it being generally found that a high oxidation temperature ($1200^{o}C$) in dry oxygen results in the lowest density of fixed charge in the oxide.

Effects similar to those of trapping state charging are caused by drift of mobile charged ions, principally sodium, in the insulator material under the influence of the gate field. Sodium is the most troublesome both because it has a high mobility in silica and because it is a very common environmental contaminant. The only solution to this problem is scrupulous cleanliness during manufacture of the devices, almost surgically-clean conditions being necessary. The reason for this will be obvious when it is realised that the airborne bacteria on the surface of a silicon wafer can supply sufficient sodium to cause considerable instability in the device. It has also been found that a thin layer of phosphosilicate glass on the surface of the oxidised silicon wafer can act as a "getter", immobilising any sodium present.

The actual physical nature of the trapping centres in

the oxide and in the interface has not been discussed yet. Various defects and impurities in the silicon dioxide have been identified as being such trapping states. Amongst these are oxygen and silicon oxygen vacancies in the insulator[6], broken and strained interatomic bonds in the material[7], and impurity atoms and ions, such as sodium[8] and tungsten[9]. Identification of electrically active trapping states with optically active centres which appear upon irradiation of SiO_2 has been made[10]. The physical nature of defect states will be discussed further subsequently.

1.5 INSULATOR INVESTIGATION IN THIN FILM TRANSISTORS

In this section the basic philosophy of insulator investigation in thin film devices is discussed, corresponding to the preceding section on single crystal silicon thermal oxide investigations.

Thin film transistors have long been known to suffer from short and long term changes in their characteristics. Such changes are analagous to the processes which occurred in silicon before it was learned how to control the oxidation process sufficiently precisely, and indeed similar causes have been established to be the root cause of these changes.

There are of course considerable differences between silicon MOSFETs and TFTs. In the former an interface between semiconductor and insulator is formed in the bulk of the material, under carefully controlled conditions, both the semiconductor and insulator materials being virtually defect free. In thin film devices, on the other

hand, two amorphous or polycrystalline materials are placed together one on top of the other. At the interfaces between the materials, and between grains, there exists a large population of localised states of the "Tamm" or "Schockley" type. Additionally there are defect states of various origins in the semiconductor and insulator.

The long term drift of characteristics which occurs in thin film transistors - the slow state drift - has been connected with the existence of trapping states in the insulator which capture and localise charges[11] [12]. These localised charges reduce the effective electric field strength at the semiconductor-insulator interface. One way of looking at this is to say that a proportion of the electric field lines from the gate are terminated by the trapped charges, alternatively the trapped charge can be considered as setting up an opposing field to the gate field. The very long time constants associated with the slow trapping effects are due to trapping states with a very low probability of capturing charge. Localised states in the insulator material are the only states which have a sufficient spread of time constants.

There also exist in thin film devices many localised states in the semiconductor material and at the interface. These states are in close communication with the charge carriers of the semiconductor, and will therefore capture and release charge much more rapidly. The effect of these states is to immobilise a proportion of the charge induced in the semiconductor by the gate field, thereby reducing the degree of modulation attainable by the gate - that is,

the transconductance. The gain of thin film devices would therefore always be less than that of single-crystal devices, because of the grain boundary trapping states. In fact, however, the situation is not so simple, because the potential barriers between the grains are also modulated by the gate field, so altering the charge carrier mobility. It is found that the overall transconductance of thin film transistors can therefore be as great as, or even greater than, that of the single crystal device[1].

The investigation of insulator charge-trapping properties in thin film devices broadly parallels that of the thermal SiO_2 in silicon technology. There exist fixed charges, which determines the threshold voltage, and trapping states which capture and release charge. The fastest responding of these are considered to be located at the interface, while similar states located in the insulator bulk will have longer response times and cause the slow state effects.

The distinction is essentially arbitrary between "slow" and "fixed" charge states, although there certainly exists truly fixed charge. Depending on the timescale of a particular measurement, some states will appear as fixed charge which under other conditions are charged or discharged. This will be seen in some of the experiments to be described, where insulator states are initially charged, that is, their occupancy is changed. A quick measurement of the device threshold voltage is then made, during which the same states appear as fixed charge. Their occupancy level can then be altered and the measurement repeated.

The method of deposition of the insulator material determines to a considerable degree the properties of the charge trapping centres in the material. In the present work, the materials under investigation are deposited by radio-frequency sputtering. The conditions under which this deposition occurs correspond to the oxidation conditions in silicon technology.

As in silicon technology, annealing in various ways affects the trapping state properties. In this matter however there is an additional difficulty. The evaporated polycrystalline semiconductor material is not in an equilibrium state, unlike a single crystal, and annealing at even moderate temperatures can have drastic effects on the semiconductor film. Indeed, annealing of the semiconductor to obtain the required properties, such as grain size, is frequently essential. This means that it is not possible to determine treatments to produce optimum insulator properties, as in the case of silicon technology - rather, the semiconductor and insulator must be considered as a whole. There exists considerably less freedom therefore in post-manufacture annealing treatments which may be used.

The measurements carried out to examine the insulator trapping properties are similar to those described in the previous section. The most important characteristic measured is the threshold voltage of thin film transistors, which provides information on the quantity and physical location of charge trapped in the insulator film. By further measurements it is possible to determine certain other characteristics of the trapping states.

1.6 ORGANISATION OF THESIS

The contents of this thesis are arranged as follows. Following this introduction, Chapter 2 describes the thin film transistors used in this work in greater detail and the method of making the devices. The measurements performed in order to determine the semiconductor properties for later use are related in the same chapter, together with the results obtained therefrom.

The next chapter, Chapter 3, contains a description of the first measurements made of the slow state instability in these thin film transistors. The results of these experiments are described and discussed.

Chapter 4 contains an account of measurements performed in order to determine the capture cross-section of the trapping states which cause the slow threshold voltage drift in these devices. Having obtained these results some discussion is given of the possible identities for the trapping states in the insulator.

The final experimental chapter is Chapter 5, and consists of a description of experiments and results of four separate phenomena. First, and most important of these, are measurements of the time response of the trapping states when filling with and emptying of charge. From the results of these measurements a charge capture mechanism for the trapping states is determined.

The next section of this chapter contains the results of low frequency noise measurements made on the TFTs. The data obtained from these measurements is then related to that of the previous section.

Following this, the results of some measurements obtained on thin film transistors manufactured using a different insulator material are presented; the material chosen for this was yttrium oxide (Y_2O_3).

Finally in this chapter are the results of measurements of the infra-red absorption spectra of the silicon dioxide insulator material, from which can be drawn certain conclusions regarding the material's structure.

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CHAPTER 2 THE THIN FILM TRANSISTOR

2.1 INTRODUCTION

The thin film transistor is a field effect transistor, that is to say, it works by modulation of the conductivity of a thin semiconductor film by the application of a capacitatively coupled transverse electric field. This field is applied by a gate electrode insulated from the semiconductor by a thin dielectric film, and the semiconductor is provided with two non rectifying contacts, the source and drain.

The thin film transistor was invented in 1926 and patented by Lilienfeld. The idea appears then to have been forgotten for many years.

With the greatly increased interest in semiconductors some years later, the field effect was revived as a means of examining the surface properties of semiconductors. In 1948, Bardeen and Brattain[1] measured the field effect in a germanium crystal, using as insulator a thin mica sheet. The degree of field effect modulation was found, however, to be only about one-tenth of that predicted from theory.

This discrepancy was attributed to the existence of trapping states on the surface of the crystal, which reduced the modulation by trapping and immobilising most of the charge carriers induced by the field plate voltage. The existence of such trapping states due to the interruption of the crystal periodicity at the crystal surface had been predicted previously on theoretical grounds by Tamm[2] and Shockley[3]. They may be thought of as being the

"dangling bonds" (unsatisfied valency bonds) left at the surface of the crystal.

Obviously, to produce a useful field effect device it is necessary to make a semiconductor-insulator interface with very few surface states. One method of doing so was discovered by Atalla et al[4] who found that the interface between silicon and thermally produced silicon dioxide has a very low trapping state density. This discovery was the key to the production of a workable field effect device on silicon.

Such a M-O-S (metal-oxide-semiconductor) device was produced by Hofstein and Heiman[5] on single-crystal silicon in 1962. At about the same time, the first thin film transistor (TFT) was produced by Weimer[6]. This used an evaporated polycrystalline semiconductor layer and an evaporated insulating layer, both about 1000 Å thick. Many semiconductor-insulator material combinations have since been found suitable for the manufacture of TFTs.

2.2 STRUCTURE & MANUFACTURE OF TFTs

A TFT consists of a thin film of semiconductor material, provided with two closely spaced non-rectifying contacts, named the source and drain. Overlying the semiconductor is an insulator film, which separates the third electrode, the gate, from the semiconductor. The gate is a thin strip of metal placed opposite to the gap between source and drain. Fig. 2.1 is a generalised representation of the device.

There are several ways of arranging these component parts of the device, and the four basic arrangements have been described by Weimer[7] as staggered or co-planar

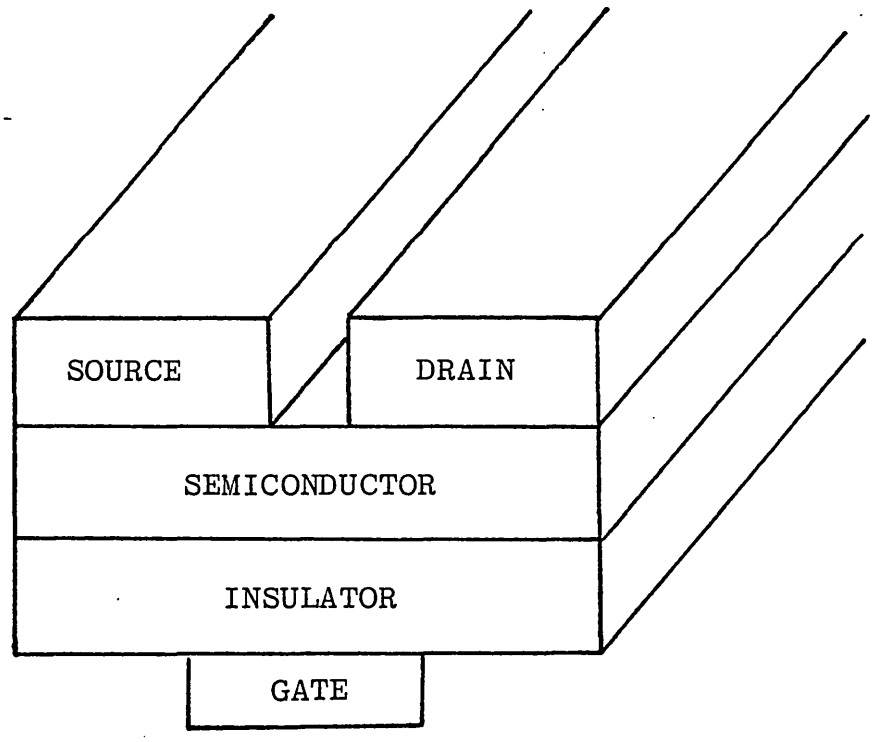


FIG. 2.1 STRUCTURE OF A TFT (not to scale)

electrode, inverted or non-inverted structures. These four arrangements are shown in Fig. 2.2. There are advantages and disadvantages to each configuration, the choice of which to use being governed by material properties and fabrication methods.

The early TFTs were made with all the layers being thermally evaporated, using cadmium sulphide or selenide as the semiconductor, silicon monoxide as the insulator and gold or aluminium as the metal electrodes. Certain disadvantages of evaporated insulator layers, due to the difficulty of controlling the process so as to get a stoichiometric insulator film, led to the use of anodised or r.f. sputtered dielectric materials, since both of these methods enable better control of the insulator properties to be obtained. With modern electron-beam evaporation sources, however, satisfactory insulator layers can now be produced by evaporation of oxide dielectrics.

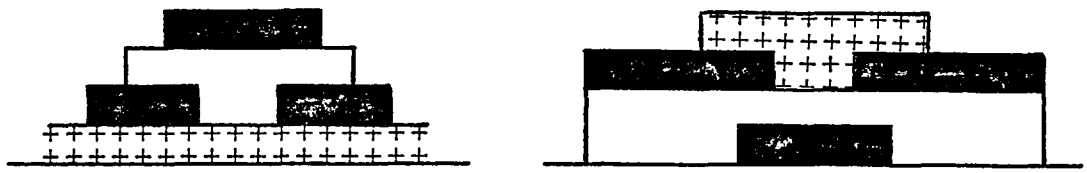
2.3 OPERATION OF THE TFT

From the description of the TFT it will be realised that it is a parallel-plate capacitor, one of the plates being a metal and one a semiconductor. If charge is placed on the metal plate by changing its potential an equal charge, opposite in sign, is induced in the semiconductor. The charge in the semiconductor forms a space charge layer which penetrates a certain distance into the depth of the semiconductor because of its low charge carrier concentration. Charge in the semiconductor is mobile, so the conductivity of the semiconductor is thereby altered.

NORMAL INVERTED

STAGGERED

CO-PLANAR



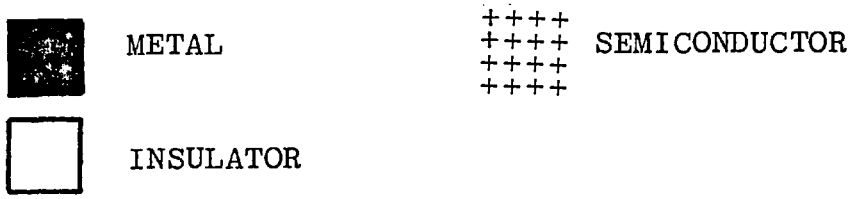


FIG. 2.2 DIAGRAMMATIC REPRESENTATION OF TFT STRUCTURES

In operation, a voltage is applied between the source and drain terminals and a drain current flows, modulated by the voltage applied between the gate and source terminals.

Overall, then, a change in gate voltage induces free carriers into the semiconductor which modulate the current flowing from drain to source of the device. If the induced carriers have the same sign as those initially present in the semiconductor an accumulation region is formed and the drain current increases; conversely, charges of opposite sign, induced by a gate voltage of reverse polarity form a depletion region and reduce the drain current.

The process may be represented on energy level diagram which shows how the electrical potential changes throughout a system such as a TFT, or alternatively by a diagram showing the charge density in the various regions of the device. These are shown in Figs. 2.3a and 2.3b respectively. The device shown here has an n-type semiconductor (electrons are the majority carriers) which means that it requires a positive gate voltage to increase the drain current, and a negative voltage to reduce it. The effects of trapped charge at the semiconductor/insulator interface are, at this stage, neglected.

The relationship between drain current and gate-source voltage will now be obtained under the simplifying assumption that the drain-source voltage is small, that is, very much less than the gate-source voltage. This restriction ensures that the voltage across the dielectric is essentially constant over the whole area of the device. This in turn means that the charge induced by the gate is uniform over the surface of the semiconductor.

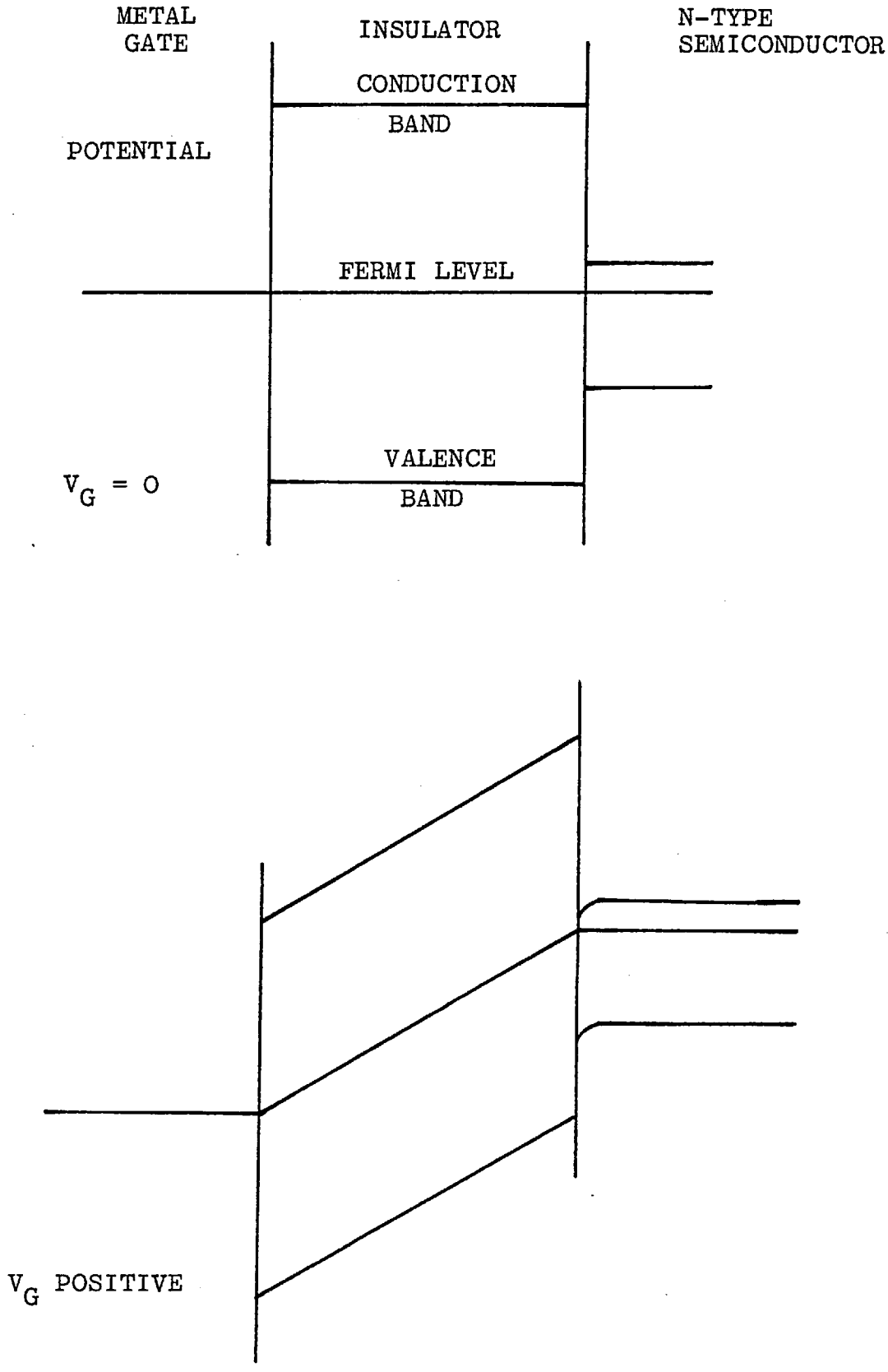


FIG. 2.3a TFT ENERGY LEVEL DIAGRAM

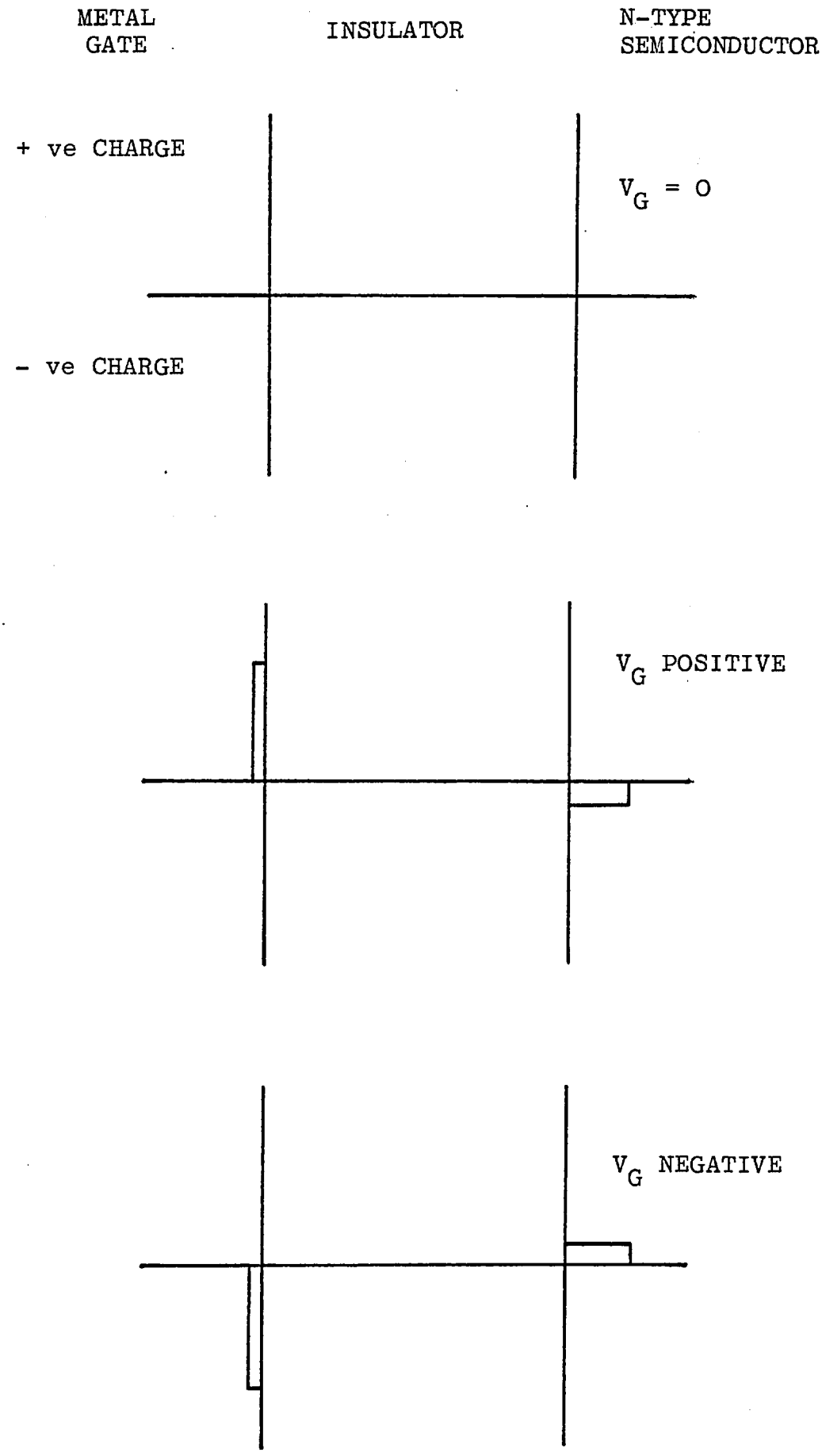


FIG. 2.3b TFT CHARGE DENSITY DIAGRAMS

2.3.1 Simplified Analysis

The starting point in the analysis is the definition of drain current I_D

$$I_D = W \int_0^d J(x)\, dx$$

$J(x)$ - current density in semiconductor

x - distance into depth of semiconductor

W - width of device

d - thickness of semiconductor film

Ohm's Law states:

$$J(x) = \sigma(x)\, F$$

$\sigma(x)$ - conductivity

F - electric field between source and drain.

The conductivity is given by

$$\sigma(x) = n(x)\, q\, \mu$$

$n(x)$ - charge carrier density/unit volume

μ - carrier mobility

q - electronic charge

Taking these equations together

$$I_D = W\, F\, \mu\, q \int_0^d n(x)\, dx$$

The last term is the integral of the distribution of charge carriers through the depth of the semiconductor - that is, it is the area density of charge carriers.

Because the device is a capacitor, the charge

transferred to the semiconductor by a gate voltage V_G is:

$$Q_G = C_o V_G = q \int_o^d n(x)\, dx$$

substituting for the integral in the previous equation therefore:

$$I_D = W F \mu C_o V_G$$

the source-drain field F is equal to the drain potential V_D divided by the source-drain spacing L, and so the final equation is:

$$I_D = \frac{W}{L} \mu C_o V_D V_G$$

or in terms of conductance:

$$G_{SD} = \frac{W}{L} \mu C_o V_G$$

This simple analysis predicts therefore that the conductance of the device is a linear function of gate voltage. This is found in fact to be the case. In Fig. 2.4 conductance is plotted as a function of gate voltage for a TFT of the type used in this work. A straight line relationship is indeed observed, except at low gate voltages where the assumption of a uniform electric field across the insulator is not correct (because of the effect of the drain voltage).

2.3.2 The Threshold Voltage

It will be observed from Fig. 2.4 that the linear portion of the curve does not pass through the origin but rather a certain gate voltage is required to initiate conduction. This voltage is called the threshold voltage and is a very important parameter of a TFT. The threshold voltage is caused by the presence of fixed electric charge

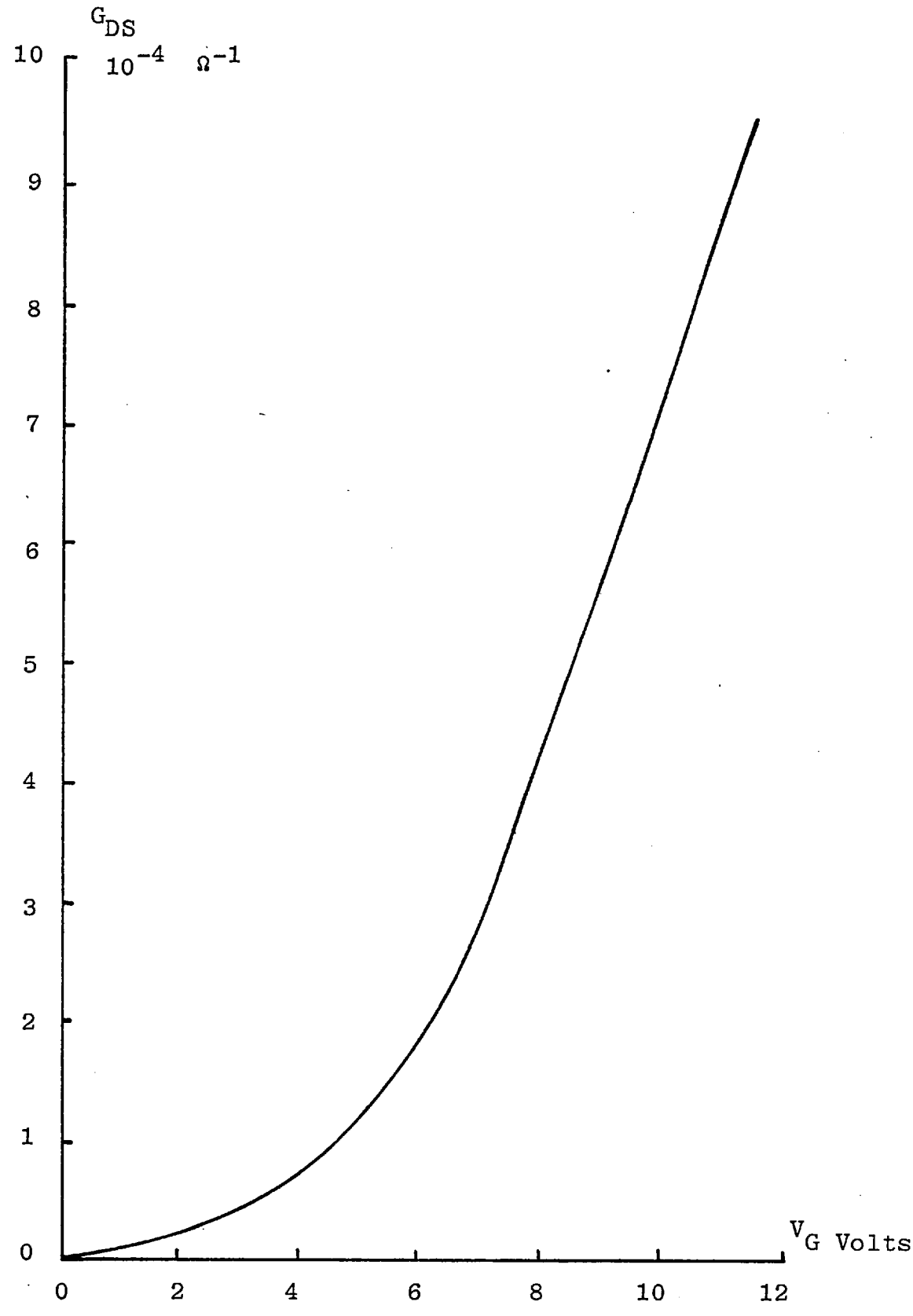


FIG. 2.4 TFT CONDUCTANCE - GATE VOLTAGE CHARACTERISTICS

in the insulator or at the insulator/semiconductor interface, incorporated at the time of manufacture. This charge induces a corresponding charge in the semiconductor which, if opposite in sign to the majority carriers forms a depletion region.

Before the carrier concentration can be increased and conduction occur this depletion must be cancelled out. The threshold voltage supplies the necessary amount of charge to do this.

The relation between the charge in the insulator, the charge in the semiconductor and the threshold voltage was derived by Snow et al[8] and will be briefly reviewed at this point.

Consider an arbitrary distribution of charge carriers varying throughout the depth of the insulator, as in Fig.2.5 The shaded region of charge, width dx and distance x from the semiconductor induces a charge in the semiconductor

$$dQ_s = -\left(\frac{x_o - x}{x_o}\right) q\ n_t(x)\ dx$$

where $n_t(x)$ is the volume density of charge carriers; this result follows immediately from Gauss's Law. The total charge induced in the semiconductor is obtained by integrating:

$$Q_s = -\frac{q}{x_o}\int_o^{x_o}\left(x_o - x\right) n_t(x)\ dx$$

The gate voltage which would cause this quantity of charge in the semiconductor is:

$$V = -\frac{Q_s}{C_o}$$

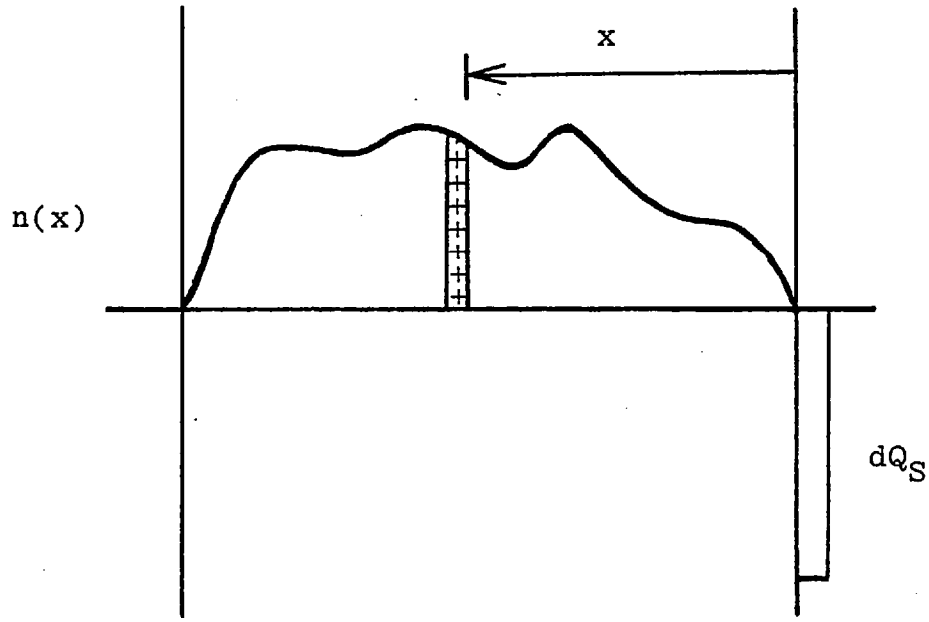


FIG. 2.5 CHARGE DISTRIBUTION IN AN INSULATOR

Where C_o is the insulator capacitance/unit area
Therefore the threshold voltage corresponding to the insulator charge is:

$$V_t = \frac{q}{C_o x_o} \int_o^{x_o} (x_o - x)\, n(x)\, dx \qquad \ldots (2.1)$$

This expression may alternatively be expressed in the form:

$$V_t = \frac{q}{C_o}\left(1 - \frac{\bar{x}}{x_o}\right) \int_o^{x_o} n(x)\, dx$$

Where $\bar{x}$ is the centroid of the charge distribution.

It is found that the threshold voltage of thin film transistors varies on a time scale of seconds to hours. This effect, often called slow state drift, is deleterious to the performance of circuits using TFTs because the operating conditions of the circuit will be upset, possibly causing the circuit to cease working. For this reason it is important that means of reducing these effects be found. Similar problems were encountered in the early days of silicon field effect transistor manufacture. The key to the problem was found to be the achievement of an insulator-semiconductor interface virtually free of defects. This was found to be possible by the thermal oxidation of single-crystal silicon.

Various mechanisms were found to be responsible for the drifts in threshold voltage which afflicted silicon devices and it is very likely that similar processes occur in TFTs. One of the mechanisms found to occur was movement of charged ionic species, principally sodium, in

the insulator material under the influence of the gate field[8]. Another was trapping of carriers from the semiconductor at sites inside the insulator material, carriers interacting with traps by quantum mechanical tunneling[9]. Hot electron injection from the semiconductor into the insulator can also give rise to trapped charge[10].

The factor common to all the possible mechanisms is that a slow change occurs in the distribution of charge in the insulator causing a change of threshold voltage in the way previously explained.

Apart from the practical purpose of improving the TFT, the device is also a sensitive means of examining charge transport phenomena in thin insulator layers, which is both a theoretically and technologically interesting subject.

2.4 MANUFACTURE OF EXPERIMENTAL TFTs

In this section the method of manufacture of the thin film transistors is described. The structure and function of the devices made are explained. A set of measurements of certain properties of the semiconductor and insulator layers is described, and the results presented.

The devices used throughout this work were made in the Thin Film Laboratory at Imperial College as part of a continuing programme of thin film transistor development, under the direction of Dr. M.J. Lee and were made available by him for this work.

2.4.1 Manufacture of Thin Film Transistors

The TFTs used in this work were of the inverted, staggered structure (Fig.2.4). They were made on a substrate of Corning 7059 glass cleaned by vapour degreasing in isopropyl-alcohol. A layer of silicon dioxide was first sputtered on to the substrate to form a clean smooth surface for deposition of subsequent layers. The aluminium gate was then evaporated to a thickness of 0.1 micron. Following the gate the dielectric was deposited by sputtering.

The material used for the transistor dielectric layer was silicon dioxide. The material was r.f. sputtered in a 95% argon-5% oxygen gas mixture at a pressure of 1 micron and a sputtering rate of 0.1 microns per hour from a fused silica target. This process gives a smooth pinhole-free high quality dielectric layer. The insulator thickness was 0.1 micron.

Following a cooling down period, the semiconductor layer was evaporated. The material used was high purity Cadmium Selenide in powder form, evaporated from a resistance heated silica boat at a rate of 0.025 microns per minute. The semiconductor thickness generally used was 0.12 microns. Cadmium selenide is an n-type semiconductor when made, no deliberate doping being necessary.

The final two depositions are an evaporated chromium layer to form an ohmic contact with the cadmium selenide, and an evaporated aluminium layer to interconnect the devices on the slide.

For each evaporation control of thickness and deposition rate was by a quartz crystal ratemeter (Edwards

Speedivac FTM1), calibrated by film thickness measurements by a Talysurf stylus instrument. The thickness of the sputtered layers was measured in the same way and was constant for a constant sputtering power and time. The substrate was unheated during the deposition process.

Each deposition was done through a different mask so as to form the required pattern. Between depositions the substrate holder was moved to the next mask at the appropriate deposition station. The whole process was completed in a single pump down of the vacuum system. The manufacturing process has been described in detail elsewhere[11], [12].

2.4.2 Annealing

As evaporated the thin film transistors perform very poorly, little modulation being possible. To produce devices with good characteristics it is necessary to anneal them. The standard anneal used was one of 1½ hours at 380°C in a flowing dry nitrogen ambient. Some devices were annealed under different conditions to determine the effects on device performance.

The annealing process is known to cause a considerable increase in the mean crystallite size of the semiconductor film[13] and therefore a decrease in the area of the grain boundary of the material. The grain boundary region is similar to the surface region of the semiconductor in that it is disordered and contains many trapping states. The grain growth on annealing will reduce the density of trapping states at grain boundaries, so increasing the fraction of the charge that is mobile.

It is found that annealing greatly increases the resistivity of the semiconductor, which is thought to be due to a reduction in bulk crystallite carrier density as a consequence of diffusion of impurities and defects during the anneal[13].

2.5 DESCRIPTION OF DEVICES ON SUBSTRATE

The layout of the devices on one half of the substrate is shown in Fig. 2.6, and the construction of a thin film transistor in Fig. 2.7. The channel length L and width W are marked on the drawing. The layout of the slide was symmetrical about the centre line in order to provide two halves prepared identically for certain experiments on post-deposition treatments, one half being used as a control.

The devices deposited on each half of the slide are as follows (the numbering refers to the designations on Fig. 2.6):

i. 9 thin film transistors, 8 small and 1 large

ii. 3 Al-SiO_2Al metal-insulator-metal capacitors.

iii. Semiconductor bar for resistivity measurement.

iv. Semiconductor sample for Hall effect measurement.

v. Device for measurement of carrier mobility.

vi. A semiconductor slab for thermopower measurement.

vii. A metal-insulator-semiconductor structure (MIS). for capacitance vs voltage measurements.

A brief description of each of these structures will now be given and the measurements done with each explained.

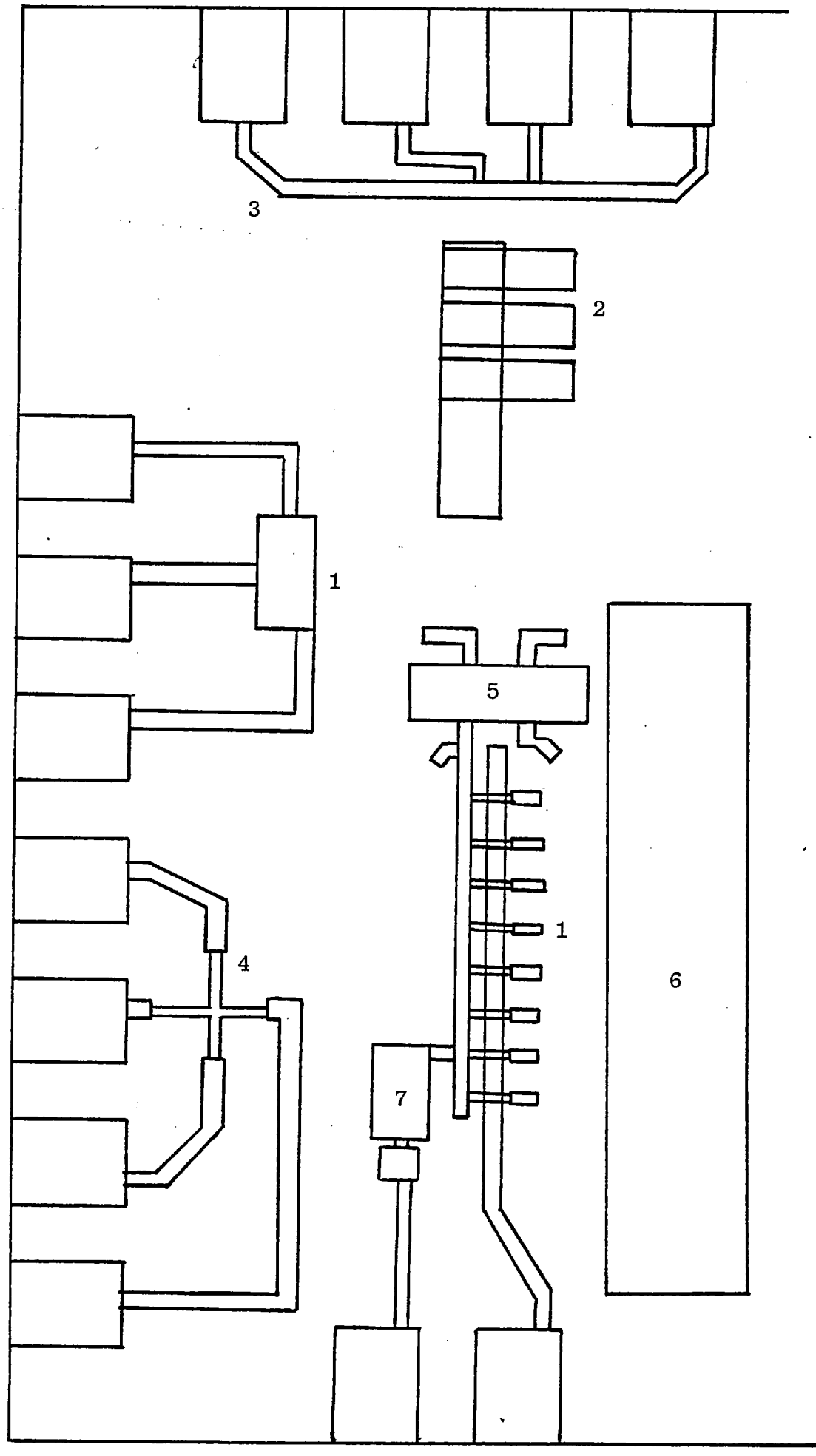
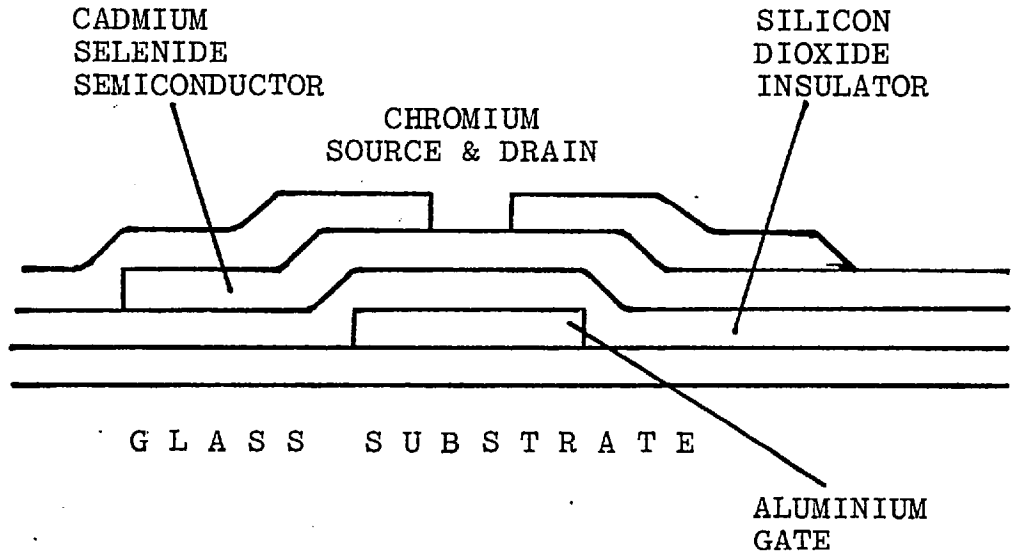


FIG. 2.6 LAYOUT OF SLIDE



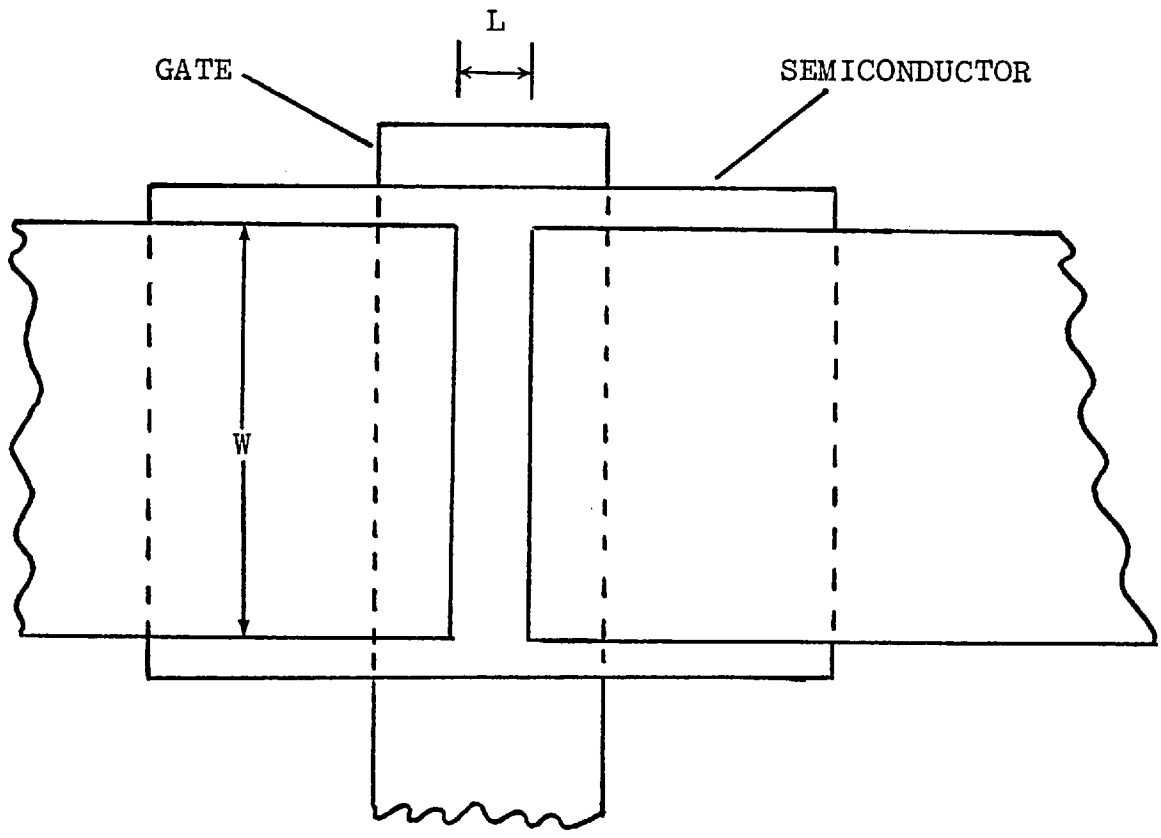


FIG. 2.7 A THIN FILM TRANSISTOR

i. Thin Film Transistors - Apart from the individual experiments described subsequently, the drain current vs gate and drain voltage characteristics were measured on a curve tracer (Tektronix Type 575). A typical characteristic is shown in Fig. 2.8.

ii. M-I-M Capacitors - These devices were used to check the quality of the insulator layer on each slide, and to measure the insulator capacitance per unit area for subsequent use in analysing experimental results.

iii. Resistivity Measurement - This is a conventional four point measurement of the resistivity of the semiconductor film.

iv. Hall Effect - This measurement proved impossible because of the very high resistivity of the annealed cadmium selenide film. The measurement is however possible on unannealed films.

v. Carrier Mobility - The carrier mobility in the annealed semiconductor film was measured by a method due to Van Heek[14]. This is a modification of the usual Hall effect experiment to enable measurements to be done on very high resistivity semiconductor films.

vi. Thermoelectric (Seebeck) Effect - This is simply a rectangular area of cadmium selenide film to which contact may be made by hot and cold probes, between which a thermoelectric potential is developed. From this result the charge carrier density in the film may be calculated.

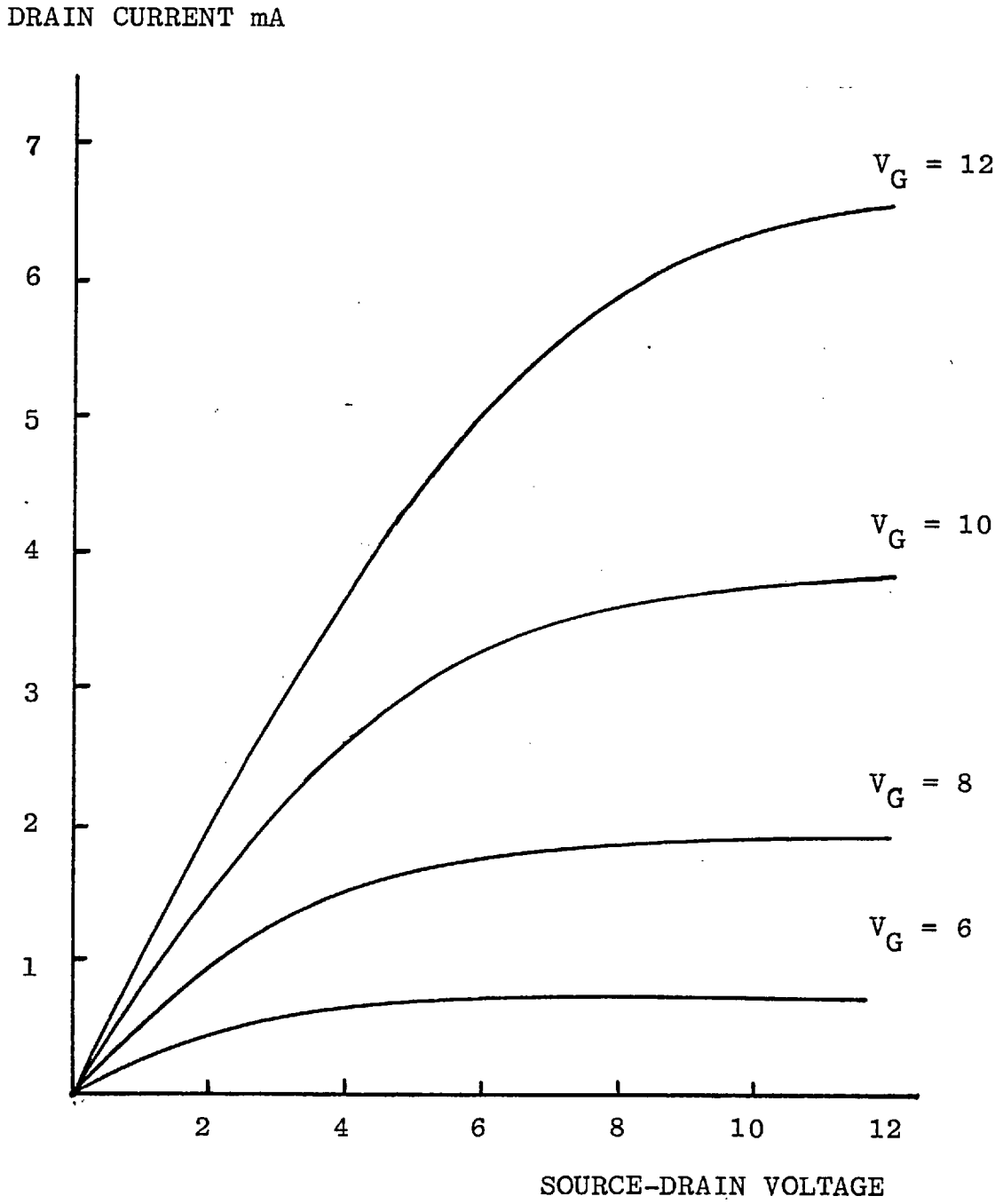


FIG. 2.8 TFT CHARACTERISTICS

vii. Metal-insulator Semiconductor Device - This structure is used to measure the variation of space-charge capacitance with field plate voltage, which is a well tried technique for determining the semiconductor doping density[15].

2.6 MEASUREMENTS OF SEMICONDUCTOR PROPERTIES

This section describes the results of measurements made on the evaporated, annealed, cadmium selenide semiconductor which is the current-carrying layer in the completed thin film transistor. These measurements were done for the following reason. The original measurements of the trap density in the insulator of a TFT, described by Anderson,[16] used certain properties of the semiconductor in the interpretation of the results. Specifically, the variation of energy of the conduction-band edge at the semiconductor-insulator interface with gate field was required. This is a straightforward calculation (see for example Many, Goldstein and Grover[17] or Frankl[18]). To carry out the calculation it is necessary to know the free carrier density in the bulk of the semiconductor. It was in order to measure this quantity accurately in the semiconductor films of the present devices that these measurements were made.

Evaporated semiconductor films such as these are of course polycrystalline, whereas the mathematical treatment used in the calculations was derived under the assumption of a single crystal material. It was at first thought that errors due to this difference would not be too severe; this was however found not to be the case.

2.6.1 Measurements and Results

The measurements performed using the different structures deposited on the substrate have been listed in Section 2.5. The measurements and their results will now be described in greater detail.

A well tried method of determining the bulk free carrier density is by measurement of the variation of space charge capacitance with applied gate voltage of a metal-insulator-semiconductor three layer structure. By a simple analysis it is possible to deduce the value of the carrier density in the semiconductor. The methods have been described in detail, and the necessary equations are given in graphical form, by Zaininger and Heiman[15]. A high carrier density results in a small variation of capacitance with gate voltage.

A measured capacitance-voltage curve is shown in Fig. 2.9. Also plotted are theoretical curves for different values of carrier density. The experimentally measured curve is seen to exhibit very little variation of capacitance, indicating a high carrier density in the cadmium selenide film. A full analysis of the experimental data shows that the semiconductor carrier density is greater than $10^{24} m^{-3}$, which would mean that the semiconductor is degenerate.

A further means of determining the density of carriers in the semiconductor is to measure the thermoelectric power, or Seebeck co-efficient. The Seebeck effect is the phenomenon whereby a thermal gradient maintained in a semiconductor causes the appearance of an electric field. The

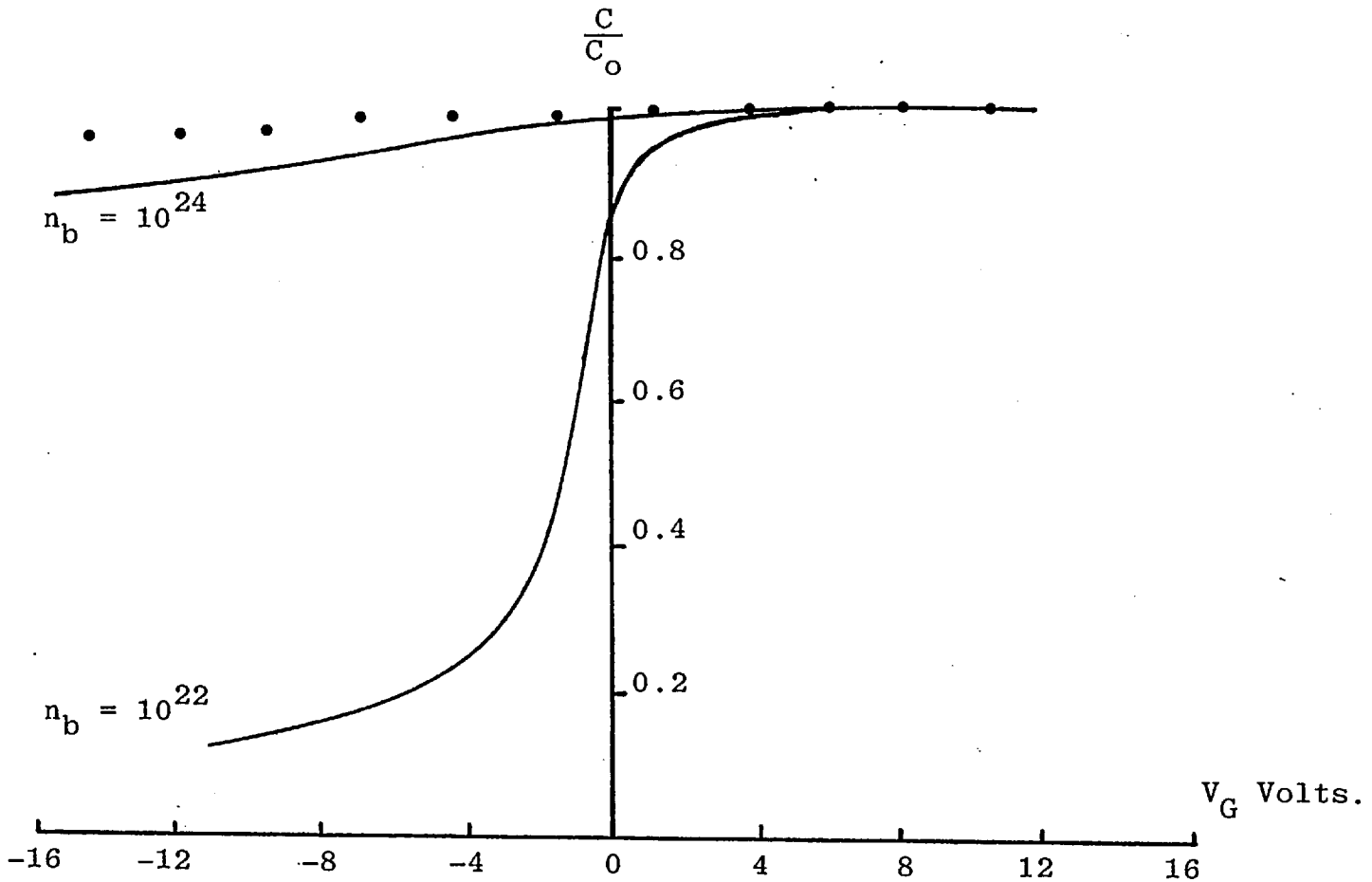


FIG. 2.9 CAPACITANCE-VOLTAGE CURVES

effect is due to the increased thermal energy of the charge carriers in the material at the higher temperature compared to those at the lower. Some of the higher energy carriers drift along the thermal gradient, the concentration gradient of charge thereby produced setting up a counteracting electric field.

The measurement was carried out by fixing two thermocouples to the ends of a sample of semiconductor on the substrate, with a heated block being clamped to one end. A temperature difference is then set up across the sample and measured with the thermocouples. The potential difference set up across the sample is also measured using the thermocouple wires, a correction being made for the Seebeck effect in the thermocouple wire. The quotient of the two quantities, temperature drop and potential difference, is the Seebeck coefficient.

The Seebeck coefficient Q_s is related to the bulk carrier density n_b and the conduction band density of states N_c by the formula:

$$Q_s = - \frac{k}{q} \left[\ln \frac{N_c}{n_b} + \varepsilon \right]$$

k is Boltzmann's constant, q the electronic charge and ε a parameter which depends on the scattering process in the semiconductor, having a value in the range zero to two. Lacking any better knowledge, the value of ε is taken as one. For cadmium selenide the value of N_c is $1.17 \times 10^{24} m^{-3}$.

The Seebeck coefficient was measured on many samples. In all cases the observed values were in the range 0.5 - 1.0mV/K. Using the equation above, these values correspond

to carrier densities in the range $3 \times 10^{19} - 10^{22} m^{-3}$.

It will be noticed that these values are very different from those obtained from the C-V measurement.

It is clear that all is not well with these results. A further pair of measurements was made in an attempt to clarify the situation.

The first of these is measurement of the resistivity of the semiconductor film. This was done with a standard four point measurement using the structure deposited for this purpose on the substrate. The current in the sample was supplied by a dry battery, the voltage across the second pair of contacts being measured with a Keithley 616 electrometer. Because of the sample resistance, the high input impedance of the electrometer was essential.

The majority of the samples measured were found to have a resistivity in the range $10^2 - 10^3$ ohm metre. The conductivity (reciprocal of resistivity) is the product of the carrier density, the carrier mobility and the charge on the electron. From the resistivity the product of carrier density and mobility may therefore be found, and for the range of values measured is of order 10^{21}-10^{22} (S.I. units).

It is necessary to measure the carrier mobility in order to obtain the carrier density. The usual way would be to utilise the Hall effect in conjunction with a measurement of resistivity, to obtain both mobility and density of charge carriers separately. The annealed cadmium selenide is however of such a high resistivity that the current density that can be achieved with

reasonable voltages is very small. Consequently the Hall voltage to be expected is also small. It was found in practice that the Hall voltage was immeasurably small, being far below the system noise level.

One way around this problem is to use a more sensitive but more complicated method, the A.C. Hall effect. This allows detection of very much smaller Hall voltages which would be noise-dominated in a conventional D.C. measurement. This approach was considered and indeed some preliminary experiments performed, but was abandoned in favour of a modified method, due to van Heek[14] which allows the measurement of mobility in high resistivity materials. The modification consists essentially of transforming the circuit so that currents rather than voltages are measured, currents being much easier to measure in a high impedance circuit than voltages. The method of measurement is described in the paper by van Heek to which the reader is referred for further details.

Using this method the mobility of the charge carriers in the semiconductor films has been measured on many samples. The values of mobility found have generally been in the range 10^{-3}-$10^{-2} m^2/V$ sec. Taken with the results of the resistivity measurements, these figures give a range of values for the carrier density of 10^{18}-$10^{20} m^{-3}$.

Several different measurements of the carrier density in thin semiconductor films have been described, and the results obtained from each given. The reason for the concentration on charge carrier density in these experiments and discussions is that it is the fundamental quantity in

any calculations based on the properties of a semiconductor. A considerable variation in the values of carrier density has been found, and in the next section the reasons for this and the consequences will be discussed.

2.6.2 Discussion of Results

To sum up the results of the experiments described in the preceding section, measurements of the semiconductor free carrier density were made by various methods. The results of these measurements were not consistent with one another, the C-V method giving a carrier density of approximately $10^{24}m^{-3}$, with the other methods giving results in the range 10^{18}-$10^{22}m^{-3}$. For single crystal semiconductor samples the results would be expected to be in good agreement with one another, so these inconsistencies are an indication that the single crystal semiconductor ideas and analysis are not applicable to evaporated thin films. This means that the calculation of the position in the energy gap of the semiconductor conduction band edge with gate field cannot be expected to give usable results, since a treatment assuming single crystal behaviour was used.

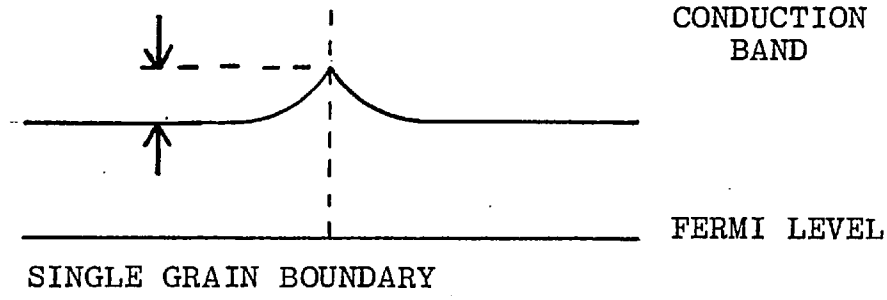
This in turn means that the interpretation of experiments on the trapping process in thin film transistors, which uses such calculations, will not be justified. Consequently the type of trap density measurements at first performed were abandoned, and an alternative method of obtaining the trap density sought. An attempt was made nevertheless, to interpret the results of the semiconductor measurements.

Evaporated semiconductor films are polycrystalline, that is, they consist of many individual grains, the regions of contact between the grains constituting the grain boundary region. The properties of the grain boundaries are vastly different from those of the bulk, central region of the crystallites, so it is in these grain boundaries that the reasons for the behaviour of the material must be sought.

At the grain boundary, just as at the free surface of a semiconductor, their exists a high density of trapping states. Many of the charge carriers near the surface of the crystallite will become trapped at these sites, and a depletion space-charge region will be set up, extending back from the surface into the bulk of the crystallite. At each grain boundary there will be two such depletion regions, one in the crystallite on each site of the boundary. When drawn on an energy level diagram, the situation at a grain boundary is as shown in Fig. 2.10a.

A polycrystalline film consists of many such regions as in Fig. 2.10b. The conduction process and the modulation of conductivity by a gate field in such a material have been examined by Anderson[19]. The discussion of these processes which follows is based on this work. Following this, a possible explanation of the results of the measurements made is given.

For conduction to occur in such a semiconductor film, charge carriers must travel through the material, traversing many such double-depletion regions in so doing. The intergranular depletion regions are energy barriers to the carriers in the semiconductor, and impede their progress



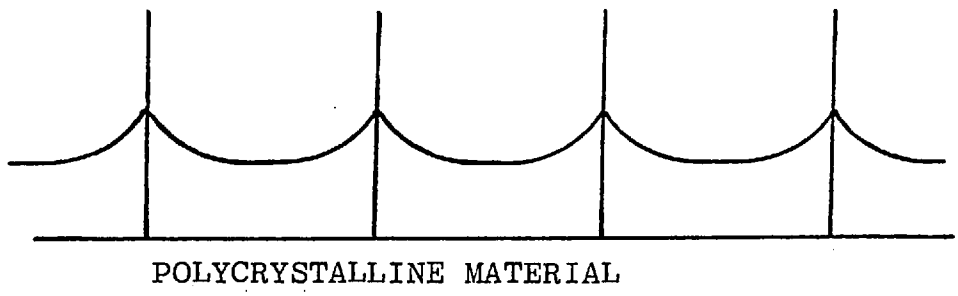


FIG.2.10 GRAIN BOUNDARY ENERGY BARRIERS

drastically. The result is that the carrier mobility in the polycrystalline film is much reduced from that found in a single crystal material.

For current flow in the material an electric field must be present. The field will increase the barrier height on one side of the boundary and reduce it on the other. The effects of many such barriers must be summed to fully understand the conduction process.

When a transverse electric field is applied, as in the thin film transistor, to modulate the current flowing, the situation becomes more complicated. Such a field deposits additional charge into the semiconductor. In single crystal material, the whole of this charge is mobile and so enhances the conductivity of the semiconductor. In the polycrystalline film, several processes occur.

The first is that some of the charges may be immobilised by trapping at the semiconductor-insulator interface (this also happens in a single crystal). Secondly, some of the charge will be immobilised in the traps at the grain boundaries. Being immobile, this charge does not contribute to the conductivity of the material. The remainder of the induced charge is free and so enhances the semiconductor conductance.

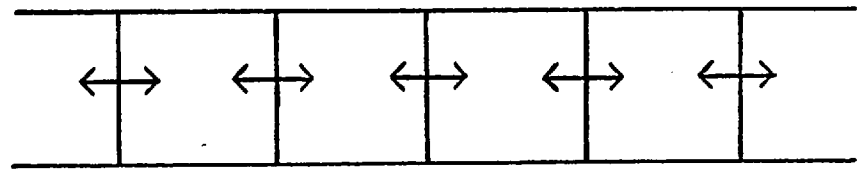
The extra charge trapped at the grain boundary is not only immobile, it also alters the charge distribution in the space charge region. In other words, the barrier height between crystallites is altered by the fraction of the induced charge that is trapped. The degree to which the motion of the carriers is impeded by the barriers is

therefore altered, that is, the mobility is changed. This of course, changes the conductivity.

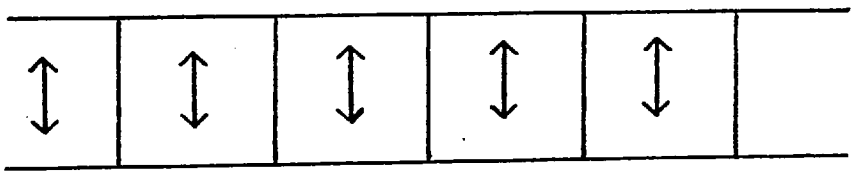
There are therefore two ways in which the conductivity of a polycrystalline semiconductor film is modulated; the usual modulation of carrier density and a modulation of mobility by variation of the height of the intergranular barriers. It will be realised therefore that the process is much more complex than for a single crystal material, and that to interpret the results of trapping experiments on the basis of the present understanding would be unjustified.

A possible explanation of the variations in the results of the different measurements of carrier concentration is suggested by these ideas. It will be recalled that the measurement by the C-V method resulted in a much higher value than either the resistivity or thermopower measurements. A fundamental difference between the C-V measurement and the others is that, with respect to the grain boundaries, the former is a 'parallel' measurement while the latter are 'series' measurements. The meanings of these terms are explained below with reference to Fig. 2.11.

Since the semiconductor is in the form of a thin film the number of crystallites down through its thickness is very much smaller than the number along the length of the film. In fact, it is often the case that the grain size in such films is approximately equal to the film thickness, so that there are then no grain boundaries through the depth of the film.



S E R I E S



P A R A L L E L

FIG. 2.11 SERIES AND PARALLEL CURRENT FLOW

In the C-V measurement, where the capacitance is measured between the semiconductor and the gate electrode, the current flow is perpendicular to the plane of the film, parallel to the grain boundaries and so no current flows across the grain boundaries. The semiconductor with grain boundaries can be considered as two capacitors in parallel, one consisting of bulk semiconductor and the other of the grain boundary depletion regions. The capacitance of two capacitors in parallel is their sum, which means that the greater capacitance dominates the measurement. In the case of the semiconductor the higher capacitance is associated with the higher carrier density, which means the bulk material rather than the depletion regions. The value of carrier density obtained is therefore that of the bulk region of thecrystallites.

In the measurements of resistivity and thermopower on the other hand, current or charge flow is in the plane of the semiconductor film, and carriers have to cross the intergrain energy barriers. In these cases the semiconductor can be regarded as a series circuit of two components, one for the semiconductor bulk and one for the depletion regions. In the case of the resistivity measurement the components are resistances, and for the Seebeck measurement they are voltage sources. When measuring a series circuit of either resistances or voltage sources, the result is the sum of the individual components. Therefore, the larger component dominates.

In the case of the resistivity, this means the most resistive material, which is the depletion region. This

means that the carrier density value obtained is that in the depletion region, which is much less than that in the bulk.

In the case of the thermopower measurement, the material with the highest thermopower is again the depletion region, because of the inverse relationship between thermopower and carrier density. Consequently the carrier density measured will again be that of the depletion region.

This discussion has necessarily been entirely qualitative; to analyse properly the results of the experiments using these concepts it is necessary to consider mathematically the way in which the contributions of the different regions in the semiconductor sum to give the overall effect. This has been investigated by Anderson.[22]

If the values of carrier density of $10^{24} m^{-3}$ and 18^{18}-$10^{22} m^{-3}$ are taken as being the carrier densities in the bulk and at the top of the barrier respectively, it is possible to estimate the barrier height. The carrier density at the top of the barrier n_g and in the bulk n_b are related by

$$n_g = n_b \exp\left(-\frac{E_b}{kt}\right)$$

where E_b is the barrier height (Fig. 2.10). For the carrier density values given above, the corresponding range of barrier heights is 0.12 - 0.35 eV.

Values quoted in the literature for barrier heights are generally considerably less than this. Barna et al[20] measured barrier heights of 0.01 - 0.025 eV in evaporated amorphous germanium films. Okuyama[21], working with tellurium films, found barrier heights between 0.009 and

0.035 eV. Anderson[22], in measurements on CdSe thin film transistors of the type used in the present work, calculated a barrier height of 0.15 - 0.2 eV, which is in reasonable agreement with the value obtained above.

In conclusion, the properties of the evaporated semiconductor are still not completely understood, and a considerable amount of work remains to be done.

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CHAPTER 3 SLOW STATE DENSITY MEASUREMENTS

3.1 INTRODUCTION

In this chapter are described the measurements made of the density of slow trapping states in the insulator of thin film transistors. Originally the results of these experiments were used to calculate the actual density of trapping states and their distribution in energy. For the reasons explained in the previous chapter this technique cannot be relied on, but the method used will be briefly described for the sake of completeness.

The first measurements of slow state density reported here were done using transistors of the type used by Anderson in the original slow trapping measurements[1]. The bulk of the present work however was done on the later generation of thin film transistors which were described in the previous chapter. The effects of changes in the fabrication conditions and annealing treatments on the slow trapping state density were investigated.

3.2 EFFECT OF TRAPPING

As was shown in Section 2.3.2 of the previous chapter, charge trapping in the insulator of a TFT has the effect of altering the threshold voltage. This is the slow state trapping - slow in this context meaning that the time scale on which the trapping occurs is seconds or minutes.

The direction of shift of threshold voltage is that a positive gate voltage causes the threshold voltage to shift to a greater positive voltage, while a negative gate voltage reverses the process, causing a shift towards

negative values. This is illustrated in Fig. 3.1 in which the source-drain conductance G_{sd} is plotted against gate voltage after three different gate voltages had been applied; zero, a positive and a negative voltage.

A threshold voltage shift in this direction indicates, for a device with an n-type semiconductor, that electrons are being trapped in the insulator when the gate voltage is positive and detrapped with a negative applied gate voltage.

3.3 MEASUREMENT OF SLOW-STATE DENSITY

In this section the way in which the slow state density is measured is explained. By density of slow trapping states is meant the area density of charges lost from the semiconductor. This is not a fixed density of trapping states which are filled before trapping ceases (the trapping has been observed to continue for at least 10 hours and was still continuing) so the number of trapped charges is measured in a certain fixed time.

The density of charge trapped is found by measuring the change in the threshold voltage of the TFT in the measurement time.

3.3.1 Experimental Method

There are two possible ways of measuring the change in threshold voltage, either gate voltage or source-drain conductance being maintained constant and the variation of the other quantity observed. In the former method as trapping occurs the conductance of the device falls. This change is measured and converted into a corresponding threshold voltage change by the use of the slope of the

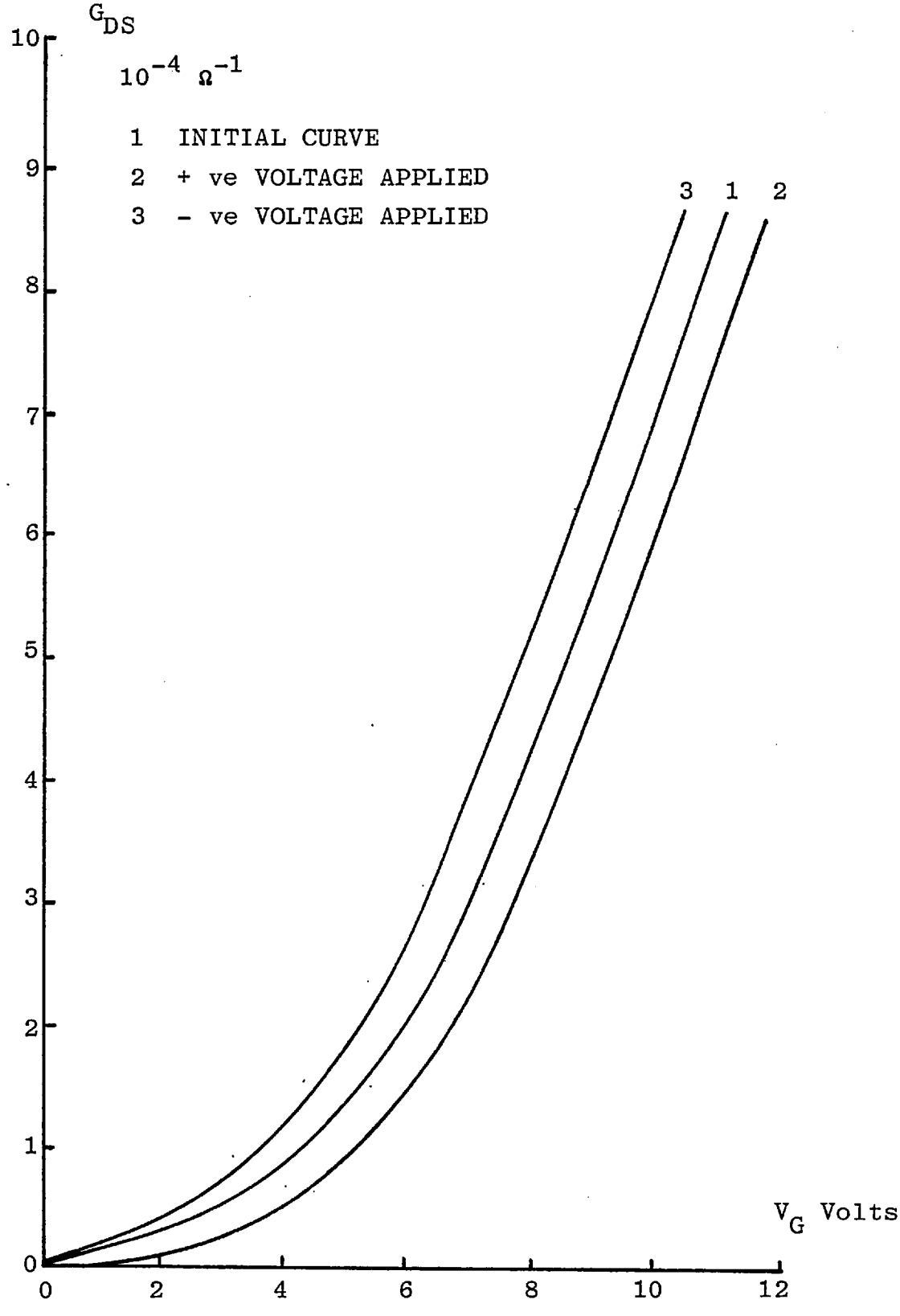


FIG. 3.1 EFFECT OF SLOW STATE DRIFT ON TFT CHARACTERISTICS

conductance-voltage graph. The alternative method is to adjust the gate voltage so as to maintain a constant conductance, the change in voltage necessary to achieve this being the threshold voltage shift. The latter method was used for these measurements. The measurement was carried out at different gate voltages, so enabling a plot of the variation of the density of trapped charge with gate voltage to be drawn.

The experiment consisted of applying a certain increment in gate voltage, V_{step}, to the device and noting the drain current thereby caused to flow. The effect of trapping is to cause the drain current to reduce slowly following application of the gate voltage. The fall in drain current is counteracted by increasing the gate voltage as necessary to maintain the drain current at its initial value. The process of replacing the trapped charge in this way is continued for a fixed time, five minutes in these experiments. The change in gate voltage over this time is the threshold voltage shift caused by the trapping process. The gate voltage is then incremented by another step, the new drain current noted and the procedure repeated. The process is illustrated in Fig. 3.2 which shows the manner in which the gate voltage is varied with time.

In these experiments the initial gate voltage was zero and the maximum approximately twenty volts, this being the full range over which the transistors would be used. Measurements with negative gate voltages are not possible because the drain current is too small to be measured reliably. The uses made of the experimental data are detailed in the following sections.

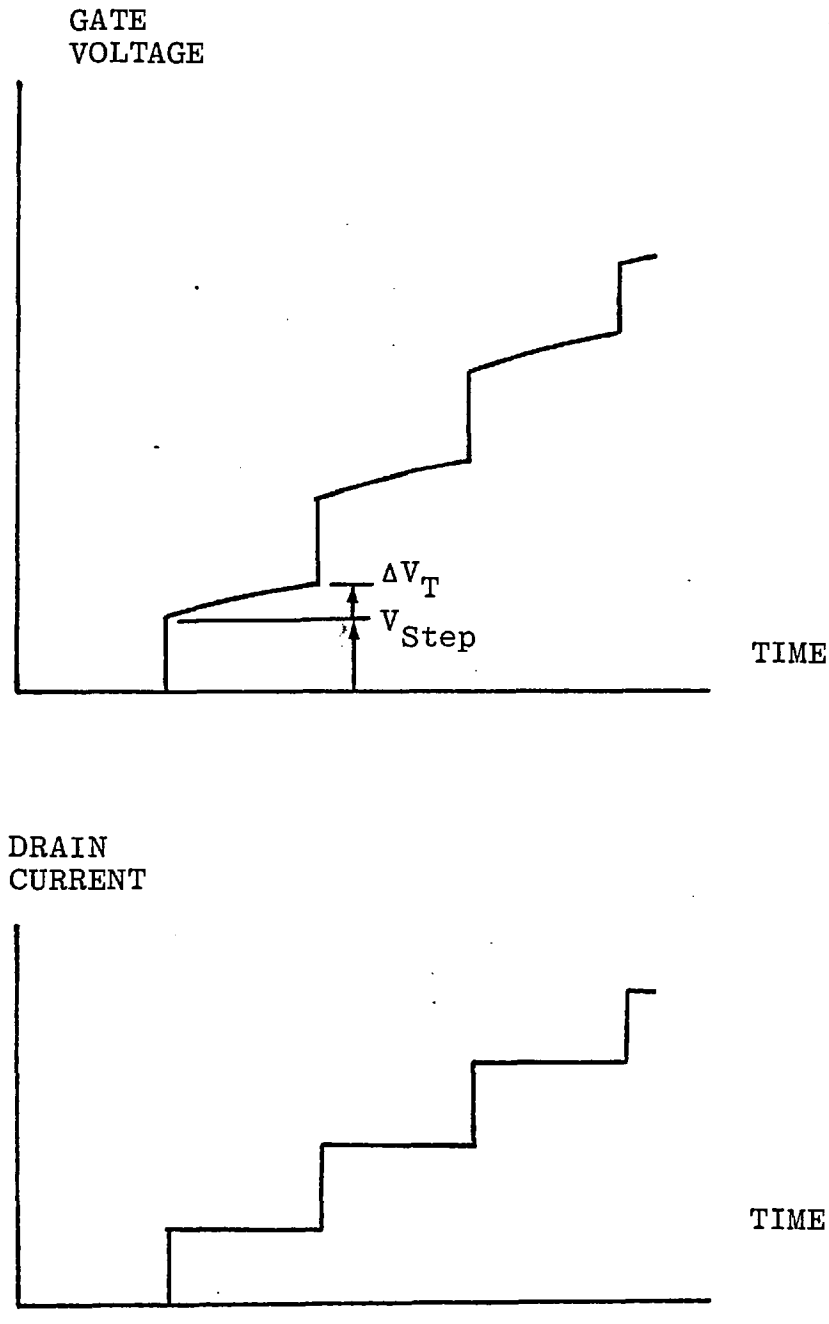


FIG. 3.2 GATE VOLTAGE-TIME SEQUENCE FOR SLOW STATE MEASUREMENT

3.3.2 Display of Results

The raw results of the experiment are measurements of the change in threshold voltage ΔV_T and the corresponding gate voltage increment V_{step}. The first of these has supplied charge to be trapped in the trapping states, while the second has supplied charge to the semiconductor which is untrapped and supports conduction through the device.

The change in threshold voltage is converted into a change in trapped charge density by the usual equation:

$$\Delta n = C_o \Delta V_T / q$$

C_o being the insulator capacitance.

Each threshold voltage is converted into a density of trapping states in this way. This quantity is then normalised by division by the appropriate gate voltage increment V_{step}. This is then the area density of trapped charges per unit gate voltage, and is called the slow state density n_{ss}.

$$n_{ss} = \frac{C_o}{q} \frac{\Delta V_T}{V_{step}}$$

This is plotted as a function of the total active gate voltage. By this term is meant the gate voltage which has gone into supplying untrapped charge. This is simply the sum of the voltage increments V_{step}. Finally this is expressed in terms of insulator electric field to remove the dependence on insulator thickness.

3.3.3 Calculation of Trap Density

The initial reason for instituting these measurements was to use the results for the calculation of the density and distribution in energy of traps in the insulator.

From the measurement the area density per gate volt is obtained, and is to be converted into the volume density per electron volt (eV). To do this it is necessary to know the relationship between gate voltage and semiconductor surface potential, and the depth in the insulator to which traps are filled. The former is a standard semiconductor calculation and the latter was calculated assuming that charge reaches the insulator traps by a tunneling process.

The mathematical treatment necessary to derive the relation between trap density and charge trapped in a certain time is fairly lengthy and so will not be given here. The basis of the theory is given in the paper by Anderson already cited, and the final result only will be given here. The equation which relates n_{ss} to the trap distribution in energy $K(E_t)$ is:

$$n_{ss} = K(E_t)\left[\frac{x_m^2}{2x_o} + \frac{\Delta V_s}{V_{step}} L_t \left\{1 - \exp\left(-\frac{x_m}{L_t}\right)\right\}\right]$$

where $$x_m = \frac{1}{2K_o} \ln (n_s \bar{v} S t)$$

$$L_t^2 = \frac{\varepsilon_i \varepsilon_o kT}{q^2 K(E_t) \Delta V_s}$$

and $$K_o^2 = \frac{2m^*}{h^2} (\Psi - E)$$

where Ψ is the height of the energy barrier between semiconductor and insulator, and E the kinetic energy of the electrons in the semiconductor. K_o is the wave-function decay constant, and is a characteristic length describing the electron wave-function in the insulator. K_o has a

slight dependence on gate field, through the variation in the energy barrier. This is sufficiently small as to be negligible.

x_o in these equations is the insulator thickness, and x_m is the maximum depth to which charge has been trapped in the time t. It is seen that it has a logarithmic dependence on time - this is a characteristic of the tunnelling process used in this model of the trapping. L_t is a characteristic length related to the trapped charge distribution in the insulator, $K(E_t)$ the trapping state density as a function of energy and ΔV_s the change in semiconductor surface potential caused by the gate voltage increment V_{step}. K_o is the wave function decay constant for electrons tunnelling into the insulator, n_s is the semiconductor surface charge carrier density, and $\bar{v}$ the mean thermal velocity of the carriers in the insulator. The remaining symbols have their usual meanings.

3.4 RESULTS OF SLOW STATE MEASUREMENTS

In the following sections the results of the measurements of slow state trapping density are described. The first of these experiments were done on transistors of the type used by Anderson in his work. The bulk of the work was done with the later devices, which were described in Chapter 2. Using these devices, experiments were performed to see whether any dependence of the slow trapping effect in the transistor on the manner in which it was fabricated could be found. The aim of these experiments was to determine what deposition conditions produced devices with the least degree of slow drift of characteristics.

In the single crystal silicon insulated gate field effect transistor, the same problems of drift were found when the first devices were made. In order to reduce these effects to acceptable levels, it was found to be necessary to control the conditions under which the silicon dioxide insulator was produced extremely closely. Precise control of post-deposition treatments, principally annealing in certain gaseous ambients at specific temperatures was also found to be essential. It seemed possible that similar solutions to the problem of slow state effects in thin film transistors might be found, which was the motivation for the measurements to be described.

3.4.1 Initial Slow State Results

A slow state density curve measured in one of the early experiments is shown in Fig.3.3. Many such measurements were made - the example shown was chosen as being typical. A prominent feature of the results of slow state measurements on these devices was the peak in the slow state density at high gate fields ($1.5\text{-}2\times10^{7} Vm^{-1}$). This feature was present in the slow state results of all these devices. It was interpreted as being due to a peak in the distribution of trapping states with energy. Using the method referred to in Section 3.3.3 the trap energy distribution calculated for this particular device is shown in Fig.3.4. The peak in the trap density is clearly seen.

When further investigation of the semiconductor indicated the uncertainties in the calculation of trap densities, the procedure was discontinued. The example shown is simply to give an indication of the results obtained.

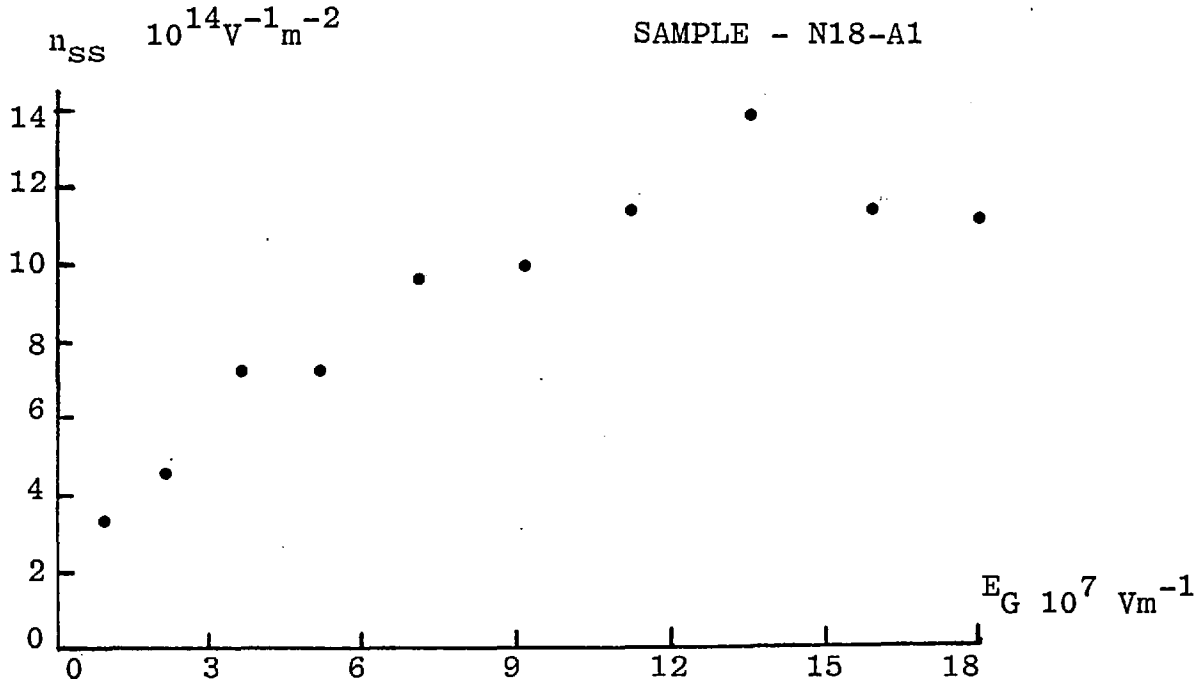


FIG. 3.3 SLOW STATE CURVE

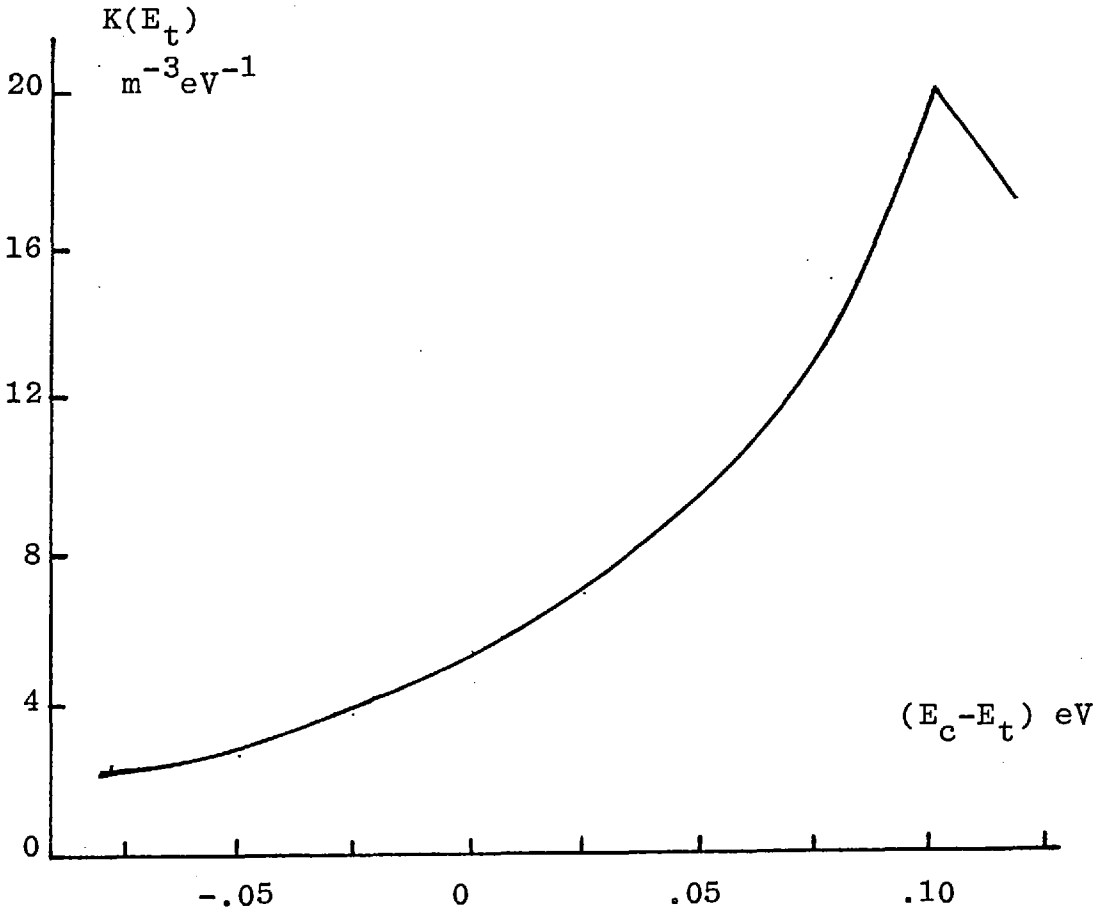


FIG. 3.4 TRAPPING STATE ENERGY DISTRIBUTION

3.4.2 Reproducibility and Repeatibility of Results

For a measurement of any kind to be of value it must be possible to repeat it and obtain a result which does not greatly differ from the original. Measurements were made to check that the slow state density was a repeatable measurement and are described in this section. Measurements were also made to examine the variation of slow state density between transistors on the same substrate, and between different substrates.

Some of the measurements to be described in Sections 3.4.3 and 3.4.4 were made to determine the effects of various procedures on the slow state densities in thin film transistors. Before doing this it is necessary to determine the variation of slow state density in devices made under nominally identical conditions. Only if the difference between two dissimilar devices is greater than the variations found between nominally identical devices can the effects be ascribed to the treatment under investigation.

To investigate the first point, the reproducibility of the measurements, the slow state density of a number of devices was measured several times in the manner described. The results of two such measurements are shown in Figs.3.5 and 3.6. Examination of the results shows that, over most of the curve, the differences between measurements made on the same device are small.

The largest discrepancy between the measurements is found in the first data points, at low gate fields, and is probably due to different quantities of trapped charge

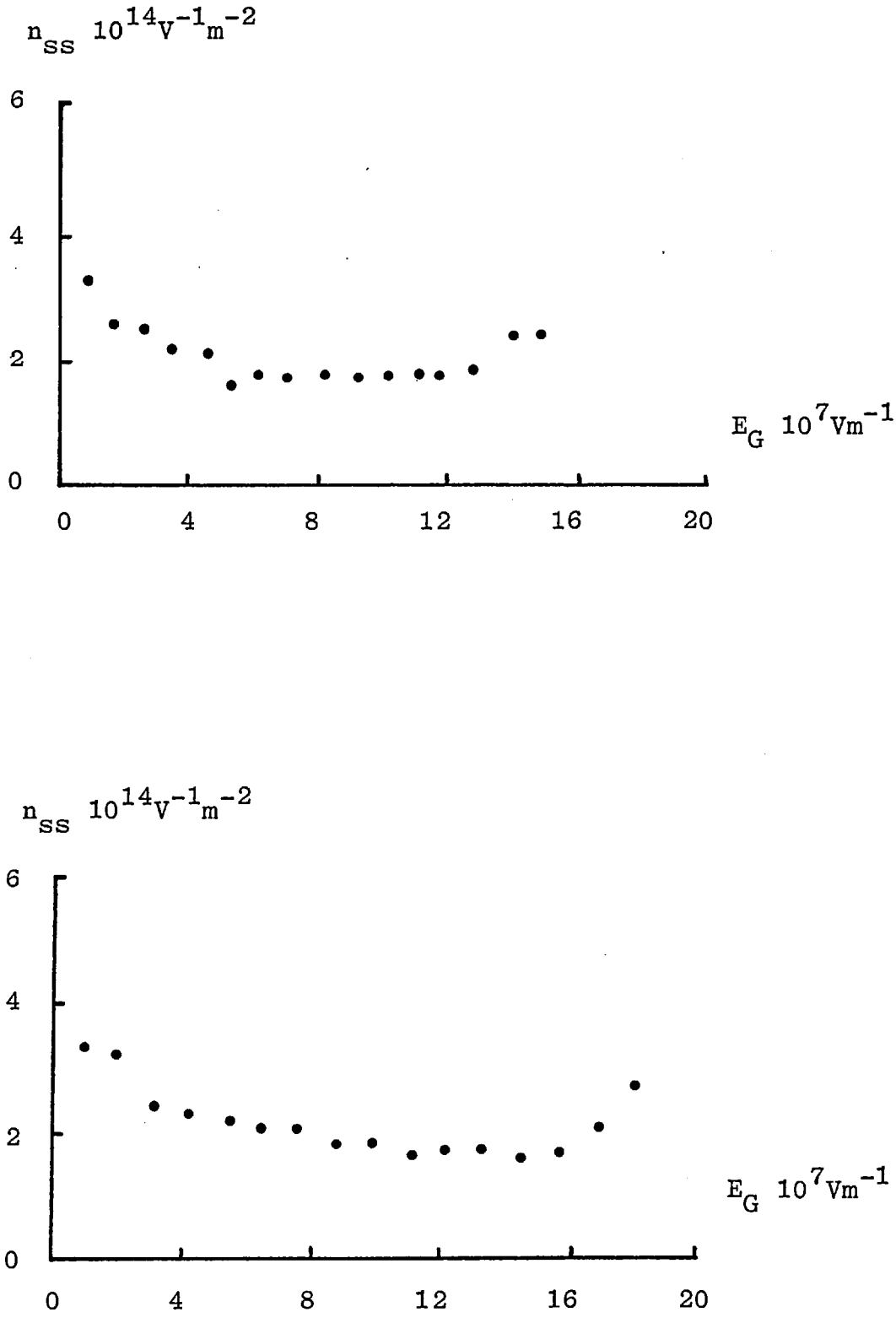


FIG. 3.5 SLOW STATE CURVES

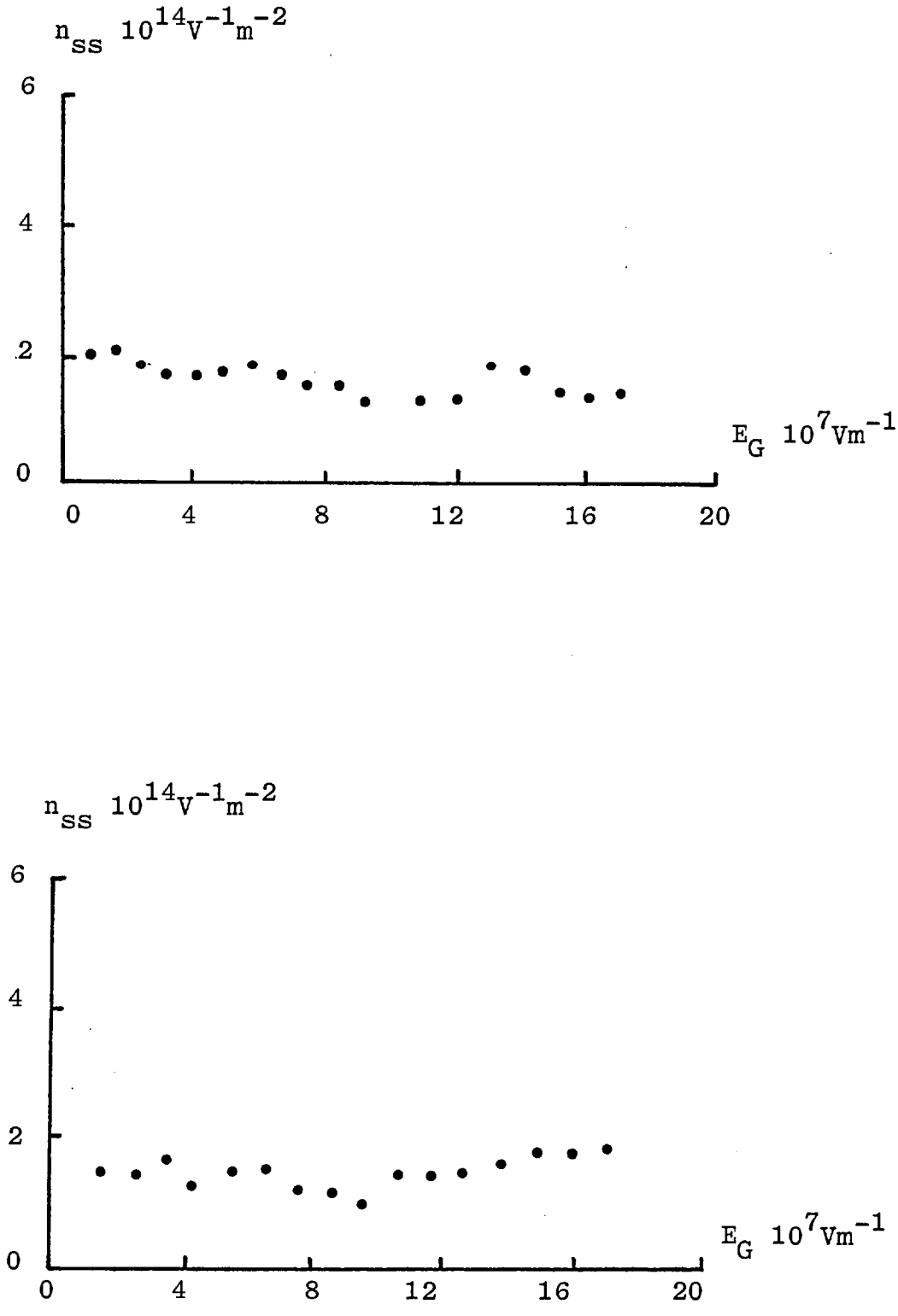


FIG. 3.6 SLOW STATE CURVES

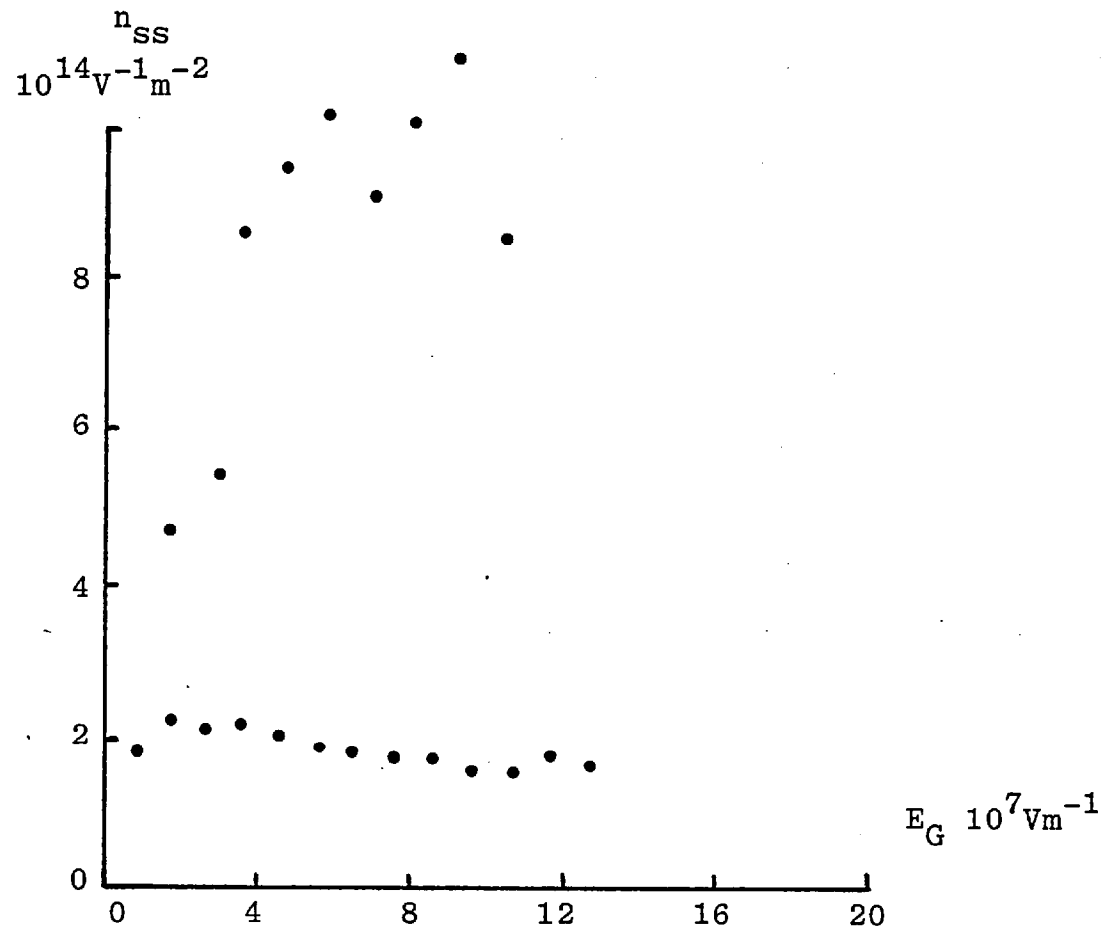
being present in the insulator of the device before each measurement was begun. When the first measurement voltage steps are applied the trapped charge so induced swamps the effect of the initial charge.

This effect means that in the experiments to be described where differences in the slow state density curves of different devices are being investigated, apparent variations in slow state density at low gate fields cannot be considered to be genuine effects unless of large magnitude. With this exception, the agreement between successive slow-state measurements on the same device was found to be excellent.

These results show that the slow state density of thin-film transistors is a quantity that may be validly measured, and that a single measurement on a device gives a reproducible result. The slow state density is therefore in this sense a 'good' measurable quantity.

To examine the variation from device to device, the slow state density was measured on several devices on the same substrate. The results of three such measurements are shown in Figs.3.7, 3.8 and 3.9. It is seen that generally the differences between devices on a substrate are quite small.

One obvious exception is seen in Fig.3.7 where one transistor has a slow state density considerably different from that of the other devices. The reason for some devices having anomalous slow state densities is not clear. On some such devices the transistor with a high slow state density was found to have a visible defect of some kind



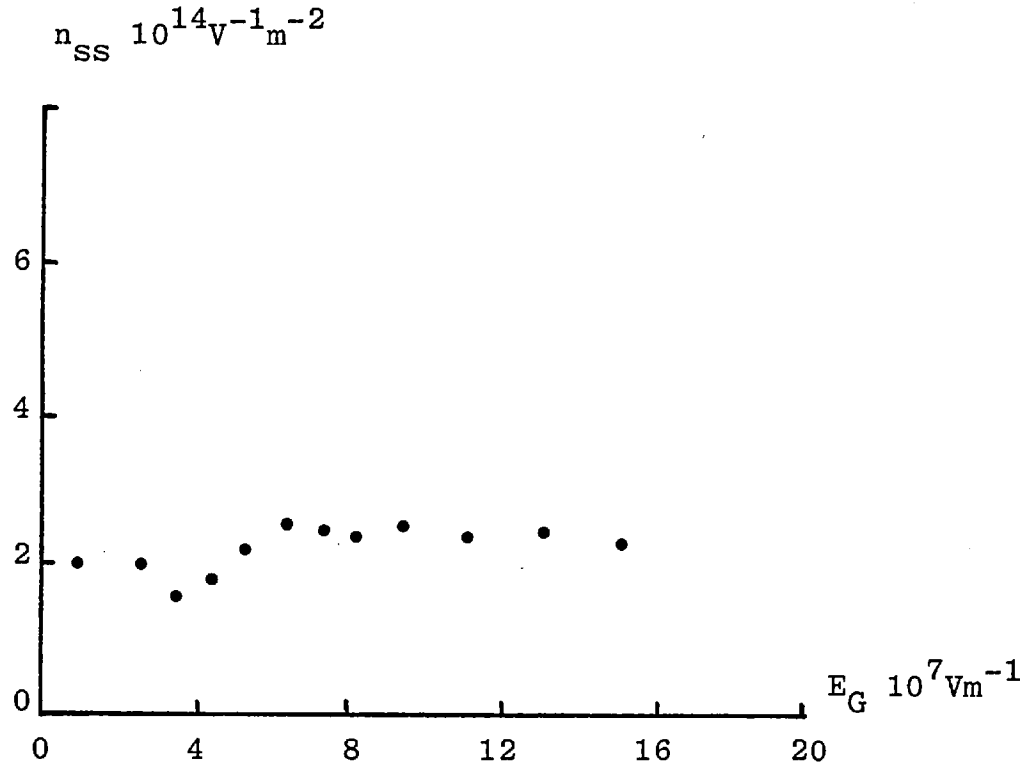


FIG. 3.7 SLOW STATE CURVES

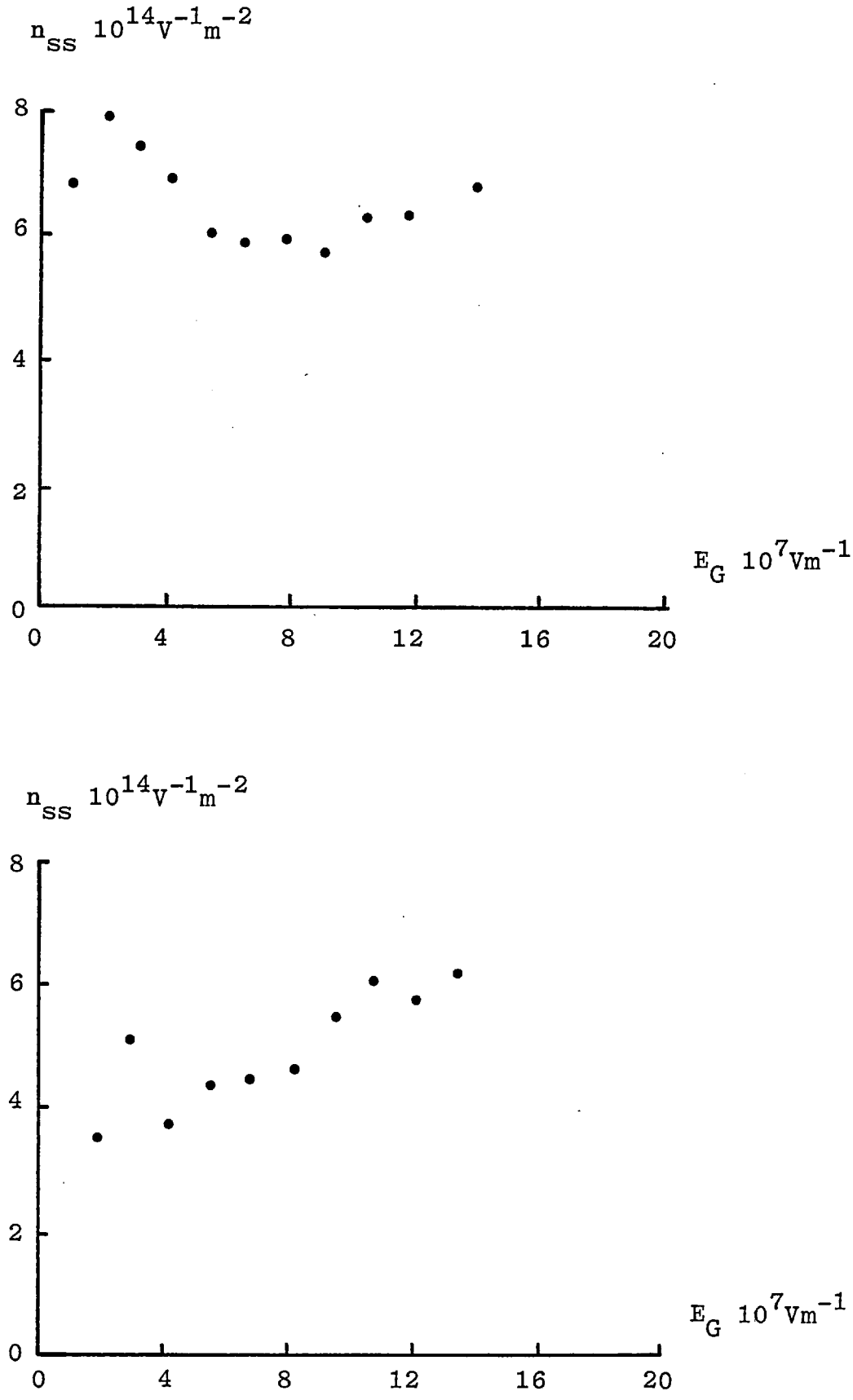


FIG. 3.8 SLOW STATE CURVES

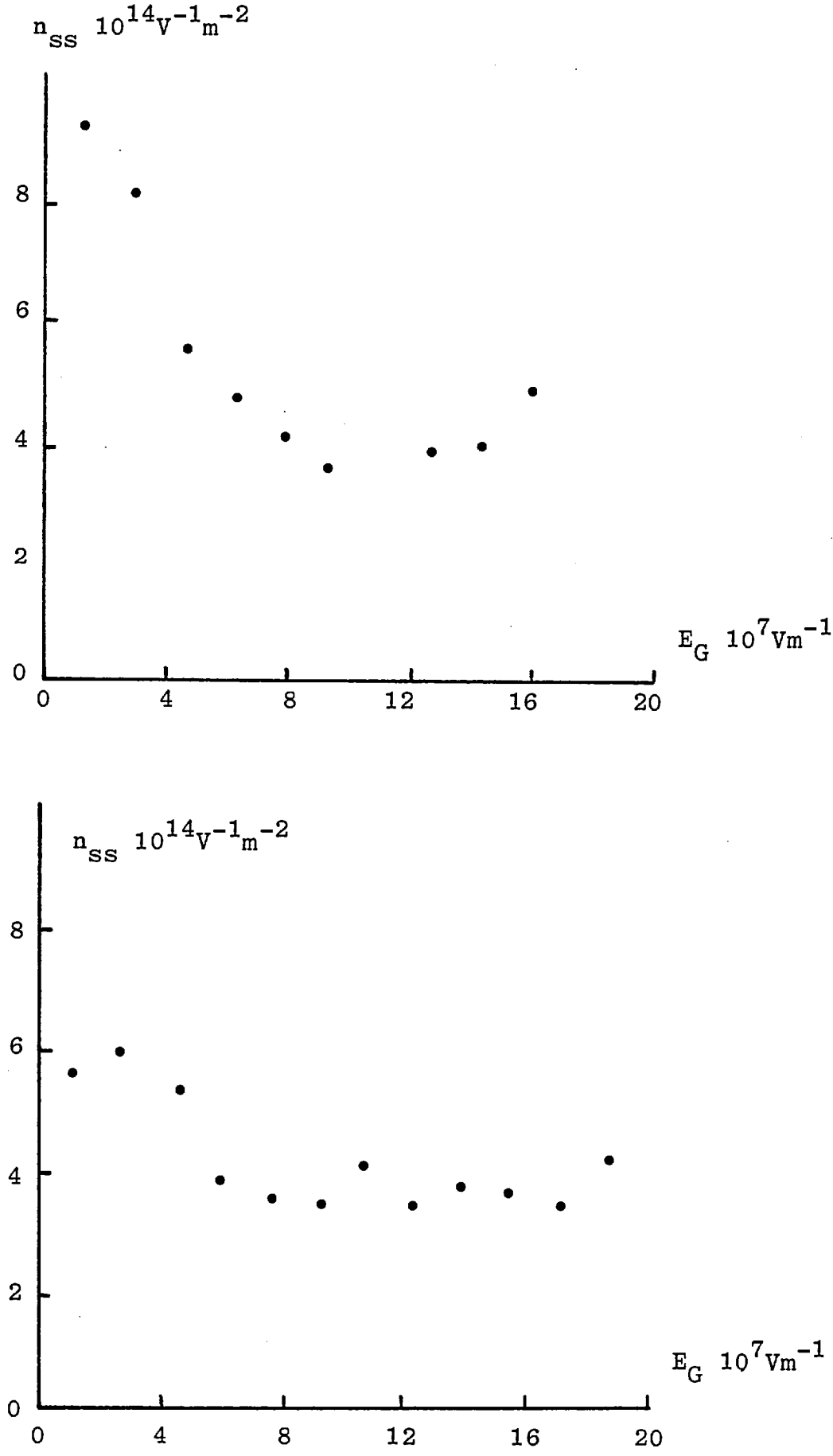


FIG. 3.9 SLOW STATE CURVES

when examined under the microscope. Such transistors were frequently also found to have a high gate leakage current, which is presumed to be due to a defect in the insulator. On the other hand some devices had a high slow state density with no such defect being visible.

From the measurements it was concluded that the difference between nominally identical devices are such that only fairly large differences between devices which have been subjected to different treatments are detectable. Any small variations are liable to be masked by the intrinsic variability of the slow state density of the thin film transistors.

3.4.3 Effects of Deposition Conditions

The deposition process of importance to the slow trapping properties of the completed transistor is that of the insulator, which is radio frequency sputtered. This is to be expected if the trapping species are located in the insulator. Many measurements of the slow state density in a large number of devices have been made, in an attempt to link the threshold voltage drift of the transistors with the manner in which they were made, and hopefully to identify the trapping species.

A connection was found in that it was observed that devices for which the sputtering gas was less pure had higher slow state densities than those sputtered in a pure gas mixture. Fig.3.10 shows the result of a slow state measurement on a device for which the sputtering gas was highly impure, owing to an equipment fault admitting air to the chamber.

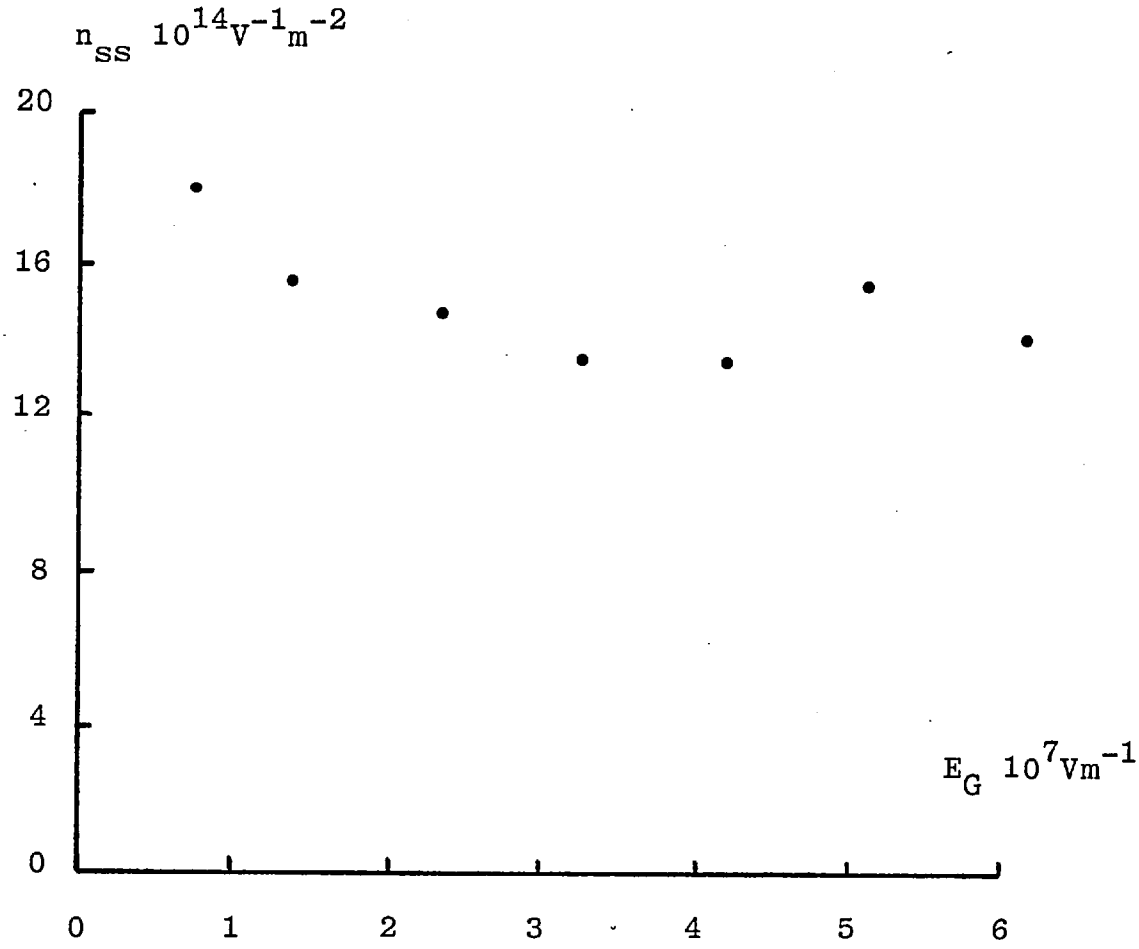


FIG. 3.10 SLOW STATE CURVE
(Note Scale Change)

The density of slow states is seen to be very much higher than in the standard devices of Figs.3.6 and 3.7. This finding suggests that an impurity in the sputtering gas mixture may be incorporated into the insulator film as it is deposited and form a charge trapping centre. No quantitative relationship between the slow state density in transistors and the composition of the sputtering gas can be given at this stage, but the general qualitative relationship of an increased slow state density in devices where the sputtering gas was less pure can be stated.

There are several possibilities for the source of the trapping species. Since the sputtering gas was contaminated with atmospheric air, the principal contaminants will be nitrogen, oxygen and water vapour, together with small quantities of the rare gases. Oxygen is of course, present in the sputtering gas mixture anyway. Water is known to form a trapping state in thermally grown silicon dioxide[2] and so is a possibility as a candidate for the trapping species.

To investigate this possibility an attempt was made to influence the quantity of water vapour present in the system during sputtering, and thus the amount of water incorporated into the film. This was done in the following way. The vacuum system incorporates a cold trap, which was normally maintained at a temperature of approximately $-40^{\circ}C$. For a series of fabrication runs however, the cold trap was cooled with liquid nitrogen to approximately $-196^{\circ}C$. Since the vapour pressure of water is a very strong function of temperature, the quantity of water in

the vacuum chamber should be much reduced.

The transistors were fabricated and the slow state densities measured. The results for the devices made with the cold trap at the standard temperature, immediately preceding and following those made with liquid nitrogen, were compared. The measured slow state curves for two of the devices are shown in Figs.3.11 and 3.12 for a standard and 'liquid nitrogen' device respectively. No significant difference was found between any of the devices in these experiments. This result suggests that water vapour does not play a part in forming trapping states. Since lowering the cold trap temperature will also reduce further the backstreaming of the vacuum system pumps below that usually present, it is also unlikely that vacuum pump oil or its breakdown products play an important part in the formation of trapping states.

Nitrogen is considered to be the most likely cause of the increased slow state density in the insulator of these devices. In the presence of nitrogen in the sputtering gas, silicon nitride would be expected to be formed in the silicon dioxide as an impurity.

Silicon nitride is used as the insulator in some forms of silicon MIS device, and it is generally found that the trapping state density is rather higher in silicon nitride than silicon dioxide. A double layer of silicon nitride and silicon dioxide is used in the MNOS memory devices where deliberate use is made of the high trapping state density at the oxide-nitride interface to store charge as the basic mechanism of the memory.

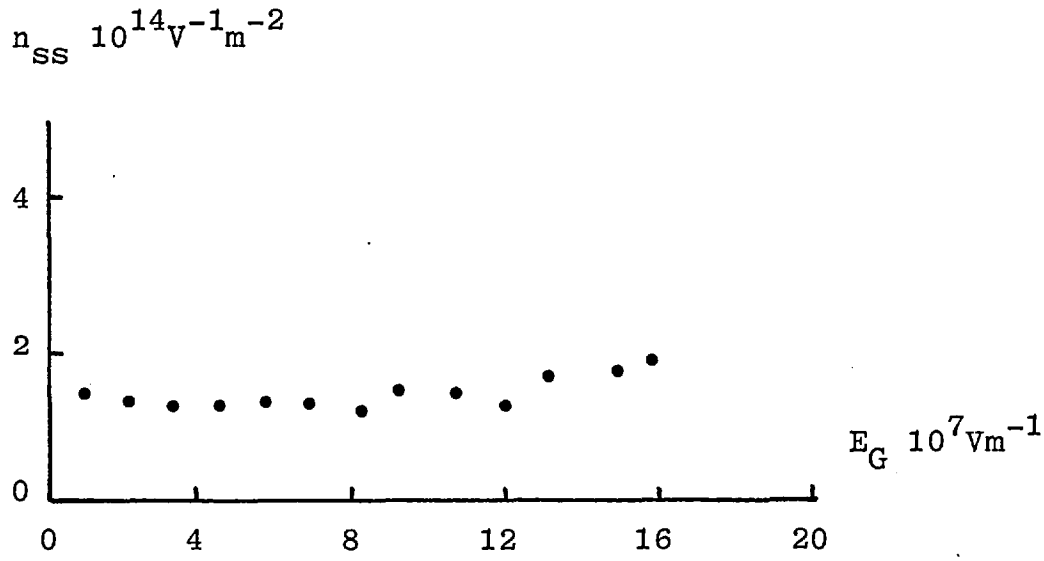


FIG. 3.11 STANDARD DEVICE
SLOW STATE CURVE

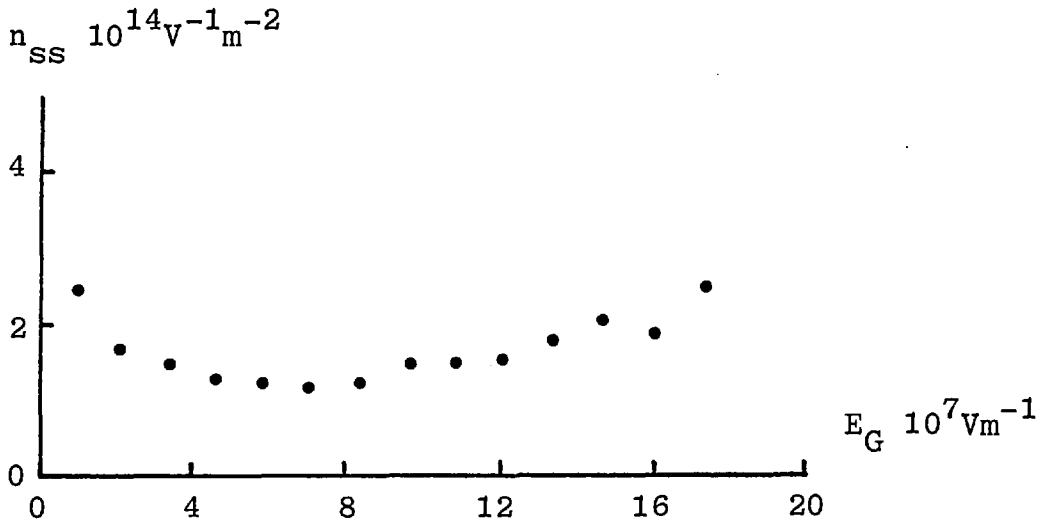


FIG. 3.12 "LIQUID NITROGEN" DEVICE
SLOW STATE CURVE

The presence of a foreign material in the TFT insulator will of course alter the energetic structure of the insulator and thereby introduce additional trapping states, which will be reflected in the slow state density of these devices. The forbidden energy gap of silicon nitride is rather less than that of silicon dioxide, so that a considerable disturbance to the structure of the silicon dioxide will occur from incorporation of some nitrogen into the material, even if macroscopic regions of silicon nitride are not formed.

It is also necessary to ask whether the same species may not be the cause of the slow state effects in all the devices. Infra red absorption spectra measurements (Chapter 5), however, showed no evidence of Si-N bonds in the standard material, which suggests that incorporation of nitrogen in the standard material does not occur to any significant extent. This is to be expected, since the quantity of residual nitrogen in the vacuum system during sputtering will be extremely small. The origin of the trapping states in the standard devices is considered further in subsequent chapters.

3.4.4 Annealing of Slow States

The silicon-thermal silicon dioxide interface is very strongly influenced in its charge trapping properties by the way in which it is annealed. A great deal of work has been done finding the best annealing treatment to reduce the density of trapping states at the interface and in the bulk to the minimum. A list of references to such work would be lengthy - the works of Kooi[3], Fowkes and Hess[4] and Hickmott[5] are given as examples. These treatments

consist of annealing at temperatures between 400^{o}C and 1000^{o}C in various gaseous ambients, for example H_2, He, H_2/N_2, CO/N_2, H_2O/N_2. In general, to achieve a low surface and trapping state density requires a high temperature anneal in an inert gas, or an anneal at a lower temperature in a reactive gas. These procedures reduce surface states in various ways - thermal anneal of physical defects, chemical reaction and saturation of dangling bonds.

Since annealing in silicon based devices has been found to have such profound effects on the semiconductor-insulator interface, the use of similar procedures in the manufacture of the thin film transistor is an obvious extension. Unfortunately, however, the situation is not the same as in the single crystal silicon device. A silicon crystal is unchanged by high temperature annealing, apart from the redistribution of doping impurities which can be allowed for in manufacture. Silicon devices may therefore be annealed at whatever temperature is found to be necessary for achieving the optimum insulator properties, without affecting the semiconductor. The polycrystalline semiconductor in the TFT on the other hand is greatly affected by even relatively low temperature treatments, since the polycrystalline material is not in an equilibrium state. Upon anneal, grain growth occurs in the semiconductor which, as was seen earlier, has a considerable effect on the characteristics of the semiconductor.

It is in fact necessary to anneal the completed substrate as described earlier, in order to obtain working transistors. The purpose of this anneal is to obtain

semiconductor properties which result in good quality TFTs. This does mean, however, that it is not possible to anneal the completed device over a wide range of temperatures in order to investigate the effects on the insulator. For this reason a full investigation of the effects of post-deposition anneals on the insulator, such as has been done for MOS devices, has not been possible for the thin film transistor.

There is another difference between silicon and thin film transistors, which is their physical structure. The TFTs used in this work have an inverted structure, that is the gate is the bottom electrode rather than being on top as in silicon devices. This is because sputtering the insulator on top of the semiconductor would damage it; the insulator therefore has to be deposited first. This structure means that annealing of the device is necessarily done with the aluminium gate electrode in position beneath the insulator. If annealing is done at a high temperature there is the possibility of diffusion of the gate metal through the insulator, causing a gate-channel short circuit. In the silicon MOS device on the other hand, annealing at a high temperature can be carried out before the gate electrode is deposited, if necessary.

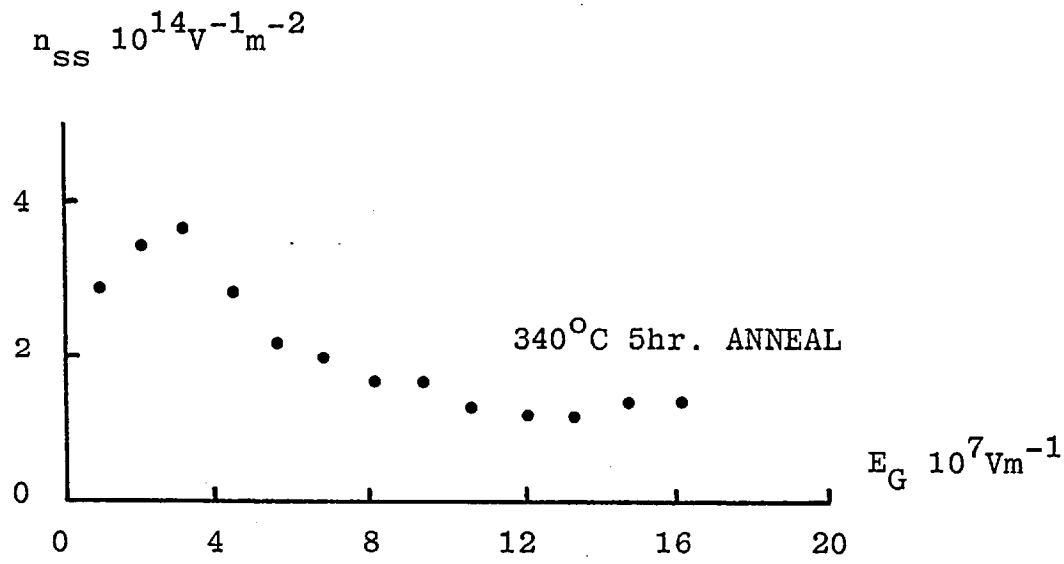
These considerations severely limit the scope of the investigation of the annealing process that is possible. The TFT anneal procedure described was empirically determined to give good transistor characteristics. During an investigation to determine whether modification of the anneal procedure would enable the production of better transistors

the opportunity was taken to measure slow state densities in the devices used.

Slow state densities were measured on devices which had been annealed at temperatures of 340°C and 415°C. In each experiment the substrate was split into two halves, one receiving an anneal at 380°C (a standard anneal) while the other half was annealed at 340°C or 415°C. It is therefore the difference in slow state densities between the curves for the two halves which is of importance, rather than the absolute values. At each temperature an anneal time which gave good TFT characteristics was used. The times were 5 hours at 340°C and 5 minutes at 415°C.

Fig.3.13 shows slow state density curves measured on a device annealed at the lower temperature, 340°C for 5 hours, together with that measured on a device on the control half of the substrate. Similar results were obtained on all such devices. The difference between the two curves is greatest at low gate fields, but as explained above, this difference cannot be considered to be significant. Over the remainder of the plot, the difference between the slow state densities of the two devices is not large enough to be significant. Annealing devices at these two temperatures does not, therefore, cause appreciable changes in slow state density.

A typical slow state density of a transistor annealed at the higher temperature of 415°C for 5 minutes is shown in Fig.3.14, again with that of a corresponding control device. As before, the differences between the two curves are not great enough, compared with the uncertainties, to



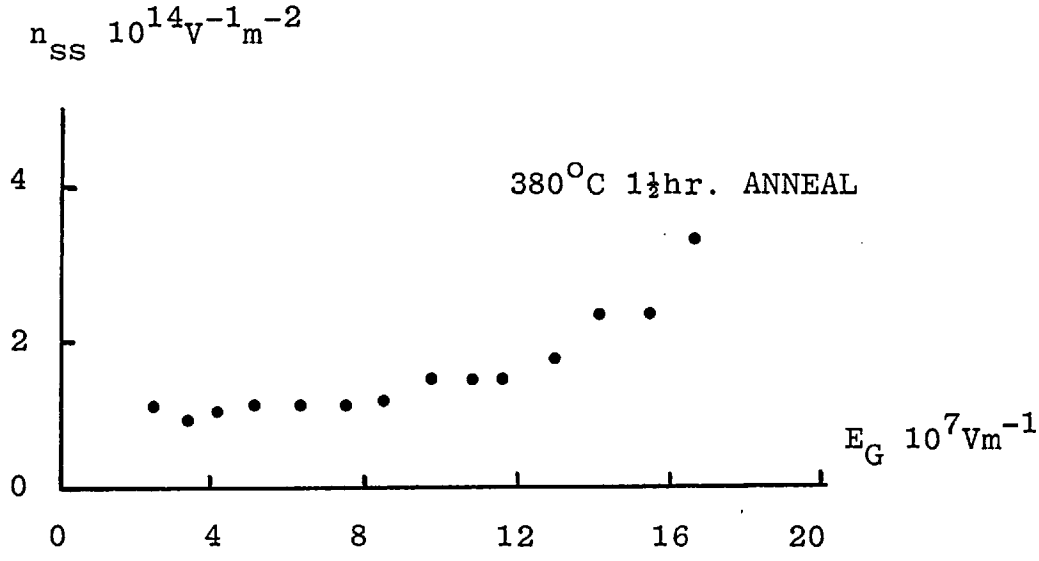


FIG. 3.13 SLOW STATE CURVES

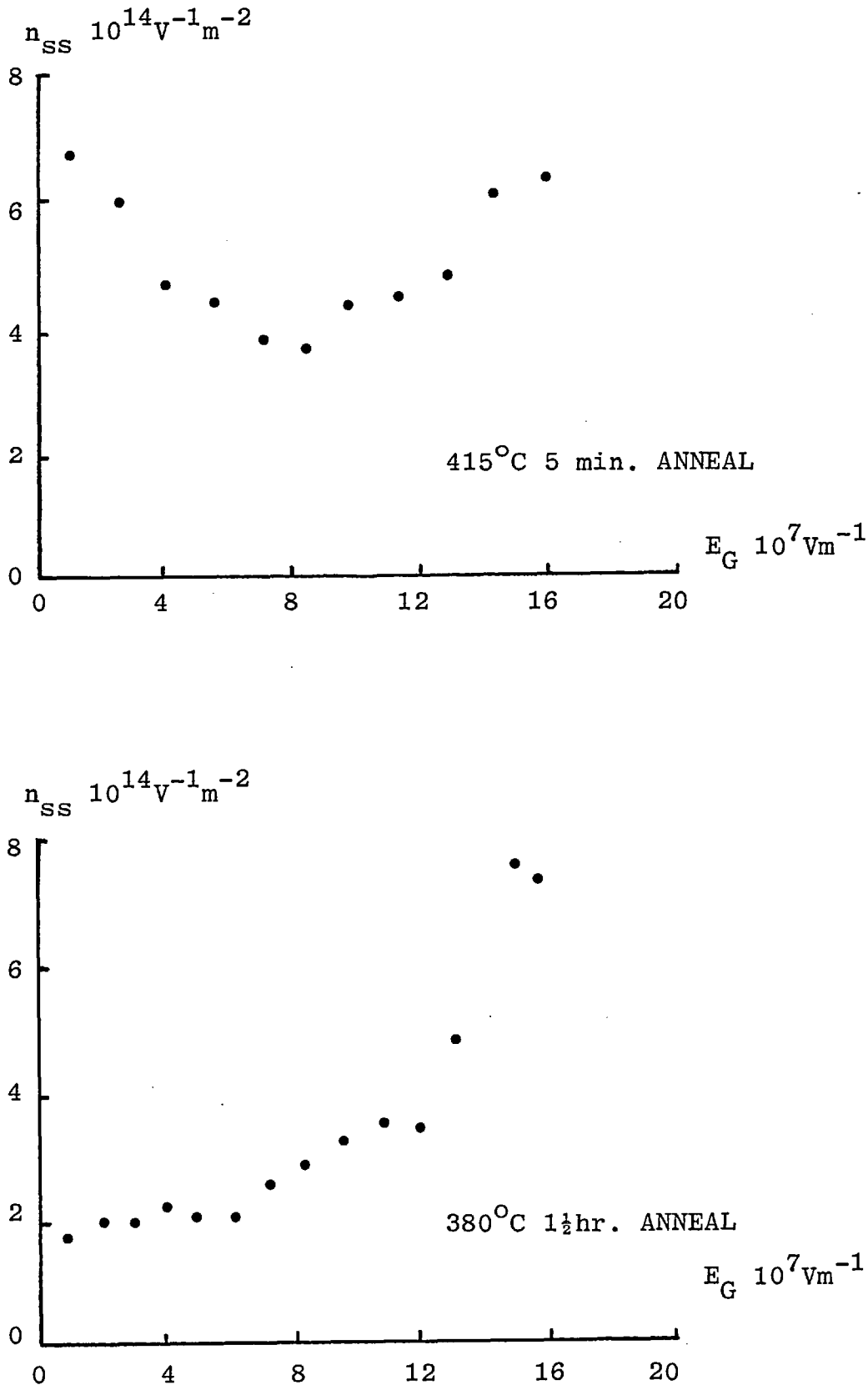


FIG. 3.14 SLOW STATE CURVES

show any difference of slow state density in the device.

The results of the two sets of annealing experiments are both negative, therefore, no significant difference in slow state density due to post-fabrication annealing treatment being observed.

Annealing MOS devices in a wet gaseous nitrogen ambient was found by Kooi [3] to reduce the slow state density in these devices. A 30 minute 450°C anneal was found to be effective. Some thin film transistors were annealed in wet nitrogen to see whether this would be effective in reducing slow state densities in the same way.

The devices were annealed at the standard temperature for the usual time (380°C, 1¼ hrs.). The nitrogen gas was passed through water at room temperature before passing into the furnace. The other half of each substrate so treated received a standard anneal in dry nitrogen, the gas from a cylinder being dried by passage over a molecular sieve at room temperature before reaching the furnace.

The results of one such experiment are shown in Fig.3.15. Discounting as before the differences at low gate fields, the slow state densities in the devices are similar. The result of this experiment is therefore negative, in that the different treatments applied to the device have not been found to alter the densities of slow states.

This concludes the limited investigation of the effects of the annealing procedure on the slow trapping state density in thin film transistors. Within the limited range of anneals possible, little effect has been

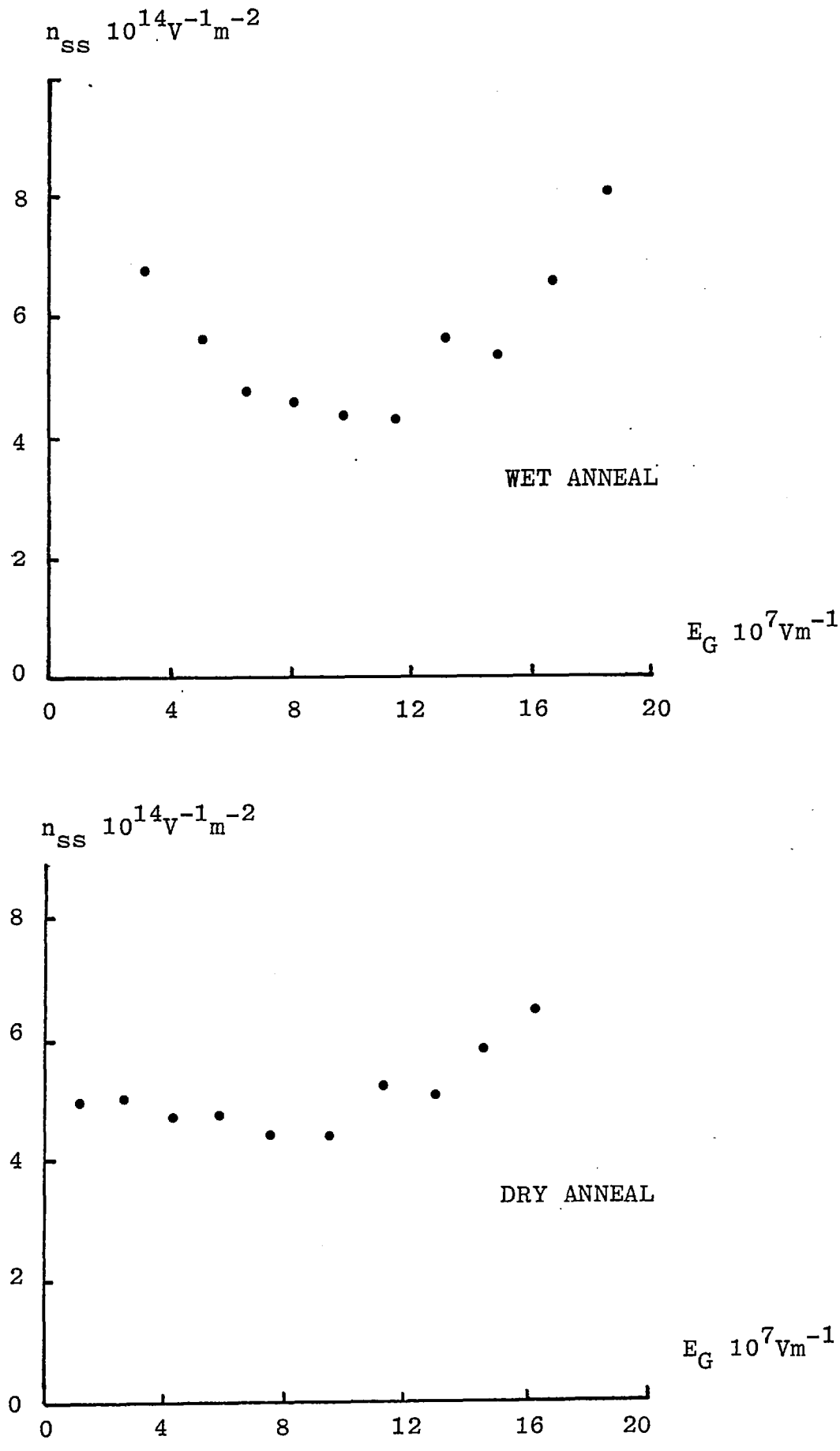


FIG. 3.15 SLOW STATE CURVES

found on the density of slow states. When the low temperatures used are considered and compared with those used in other work, it is seen that the maximum temperature used in these experiments is at the lower end of the range found to be effective when investigating thermal silicon dioxide, so the negative results are not unexpected.

3.5 DISCUSSION

The results of these experiments are largely negative. To summarise, annealing of thin film transistors has been found to have little effect on the density of slow trapping states. The purity of the sputtering gas does affect the slow state density, while no variation in slow state density has been observed when an attempt was made to influence the water vapour concentration in the vacuum system.

The negative results of the annealing procedures are not surprising in view of the low temperatures used, compared with those used in the production of single crystal silicon devices. Because of the sensitivity of the polycrystalline semiconductor film to heat treatment, high temperature anneals are not possible. One possible way around this difficulty would be to anneal the insulator at a high temperature before the semiconductor was deposited. It would be necessary to do this in the vacuum system so that the insulator surface was not exposed to the atmosphere before deposition of the semiconductor. Such exposure would lead to the adsorption of a layer of, for example, water vapour which might form trapping states at the semiconductor-insulator interface.

The dependence of the slow state density on sputter gas purity suggests that trapping species may be incorporated in the insulator during deposition. There are many possible species which are known or thought to behave as trapping centres, so that identification of the trap is not yet possible. Possibilities are oxygen vacancies, excess silicon, sodium or other alkali metal ions and water related centres. Further work will be necessary before a full identification can be made.

The observation that there was no change in slow state densities when the vacuum system cold trap temperature was reduced, in order to reduce the quantity of water in the sputtering gas, was surprising, since water related trapping centres are known to exist. A possible explanation for this is as follows. The cold trap is at the bottom of the vacuum system, directly above the pumps. The sputtering gas is continuously bled in to the system, and pumped out. There is thus a gas flow towards the cold trap and away from the sputtering region. The cold trap will therefore only remove water from the gas after it has passed through the sputtering region. There will be no great effect on the water concentration in the gas from which the insulator material is sputtered. Some other means of altering the water concentration is therefore necessary in order to determine whether moisture-related traps are present in the sputtered TFT insulator, for example admitting known quantities of water into the sputtering gas and examining the variation, if any, in the slow trapping behaviour of the completed device.

As was stated, no difference was found when the transistors were annealed in wet, rather than dry, nitrogen. Since the water vapour content of gas was not measured in either case this is a qualitative assessment only. Annealing in gas of measured and controlled water content would be a logical extension of the experiment. In the present experiments the dry gas would still contain a certain amount of water.

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CHAPTER 4 TRAP CAPTURE CROSS-SECTION MEASUREMENT

4.1 INTRODUCTION

As discussed in the previous chapter, the problem with the interpretation of the slow-state measurements arises because of the difficulty of obtaining the necessary information about the electronic properties of the semiconductor. This difficulty could be overcome if it were possible to measure experimentally the availability of electrons from the semiconductor for trapping in the insulator, removing the necessity of calculating this quantity.

Such an experiment has been described by Ning and Yu[1] and Ning[2]. The role of the semiconductor in the measurement is merely that of acting as a detector of charge trapped in the insulator of the device by its effect on the threshold voltage. This part of the experiment is similar to the measurement of slow-state density.

The availability of electrons for trapping is measured in the following way. Those electrons which avoid capture by the trapping states in the insulator travel through the full thickness of the insulator and reach the gate electrode, where they form the gate current in the external circuit, which is directly measurable. The time integral of the gate current density is then the charge density passing across the semiconductor-insulator interface, less that charge that has been trapped. Knowing these two pieces of information the analysis may now proceed.

4.2 TRAPPING KINETICS

As a first step to determining the properties of the trapping species in the insulator it is necessary to consider the kinetics of the trapping process. The rate equations governing trapping relate the density of trapped electrons to the density of trapping sites, their capture cross-section for the trapping process and the flux of electrons available for trapping. By measuring the density of trapped electrons and the electron flux it is possible to determine the trapping state density and capture cross-section.

The mechanism by which electrons from the semiconductor reach the trapping states in the insulator and hence become available for trapping is not at this stage known. The mechanism will affect the rate of transfer of electrons across the interface and hence the rate of trapping. Because both quantities are measured in this experiment however, it is possible to determine the trapping parameters without any knowledge of the charge transfer mechanism.

4.3 EXPERIMENTAL DETAILS

The experiment consists of the simultaneous measurement of the drain-source conductance and gate current of a TFT when a voltage is applied to the gate terminal. A detailed description of the measurement follows.

4.3.1 Measurement of Threshold Voltage Change

In the slow state density measurements described previously the change in threshold voltage was measured by so adjusting the gate voltage of the device under test as to maintain a constant drain current. When all that was required was a measurement of the change in threshold voltage after a certain time this method was adequate but where, as in the present experiments, a continuous record of the changing threshold voltage is needed a different method is required.

The means adopted was to make use of the linearity of the conductance/gate-voltage relationship. If the change in conductance between the source and drain terminals (due to loss of electrons into the insulator) is measured continuously at constant gate voltage, the corresponding threshold voltage change is found by using the gradient of the graph of this conductance against V_G, which may be measured. This procedure is only valid, of course, at gate voltages sufficiently high that operation on the linear portion of the I_D-V_G characteristic is ensured.

The conductance was measured by measuring the drain current flowing with a voltage of approximately 1.5 volts applied between source and drain of the device. The drain current was recorded on a chart recorder as a function of time. A calibration curve of the dependence of drain current on gate voltage was also recorded during each experiment for use in converting the drain current variation into a plot of threshold voltage change.

4.3.2 Measurement of Gate Current

The gate current to be measured is extremely small - less than 10^{-12}A. It was measured by a Keithley 616 digital electrometer in the gate circuit, between the gate and source electrodes in series with the gate voltage supply. The electrometer was used in the 'Fast' mode to obtain the shortest response time. The gate current was recorded on a chart recorder driven from the analogue output of the electrometer.

The response time of the system is limited to that of the chart recorder. When the gate voltage is applied there is an initial step in gate current followed by a continuous fall. The response time of the recorder is such that the initial rise in gate current is not faithfully recorded. After about one second however, the discrepency becomes negligible. This causes no serious loss of information.

4.3.3 Measurement System

The circuit used for the measurement is shown in Fig.4.1. Because the gate current is so small the system is very sensitive to stray charge movement close to it. It was therefore found necessary to enclose the circuitry in a continuous metal shield. This was achieved by placing the wiring and the device under test in a metal box and using screened leads for all connections. For the same reason the gate and drain voltages were both supplied by batteries also enclosed in the box.

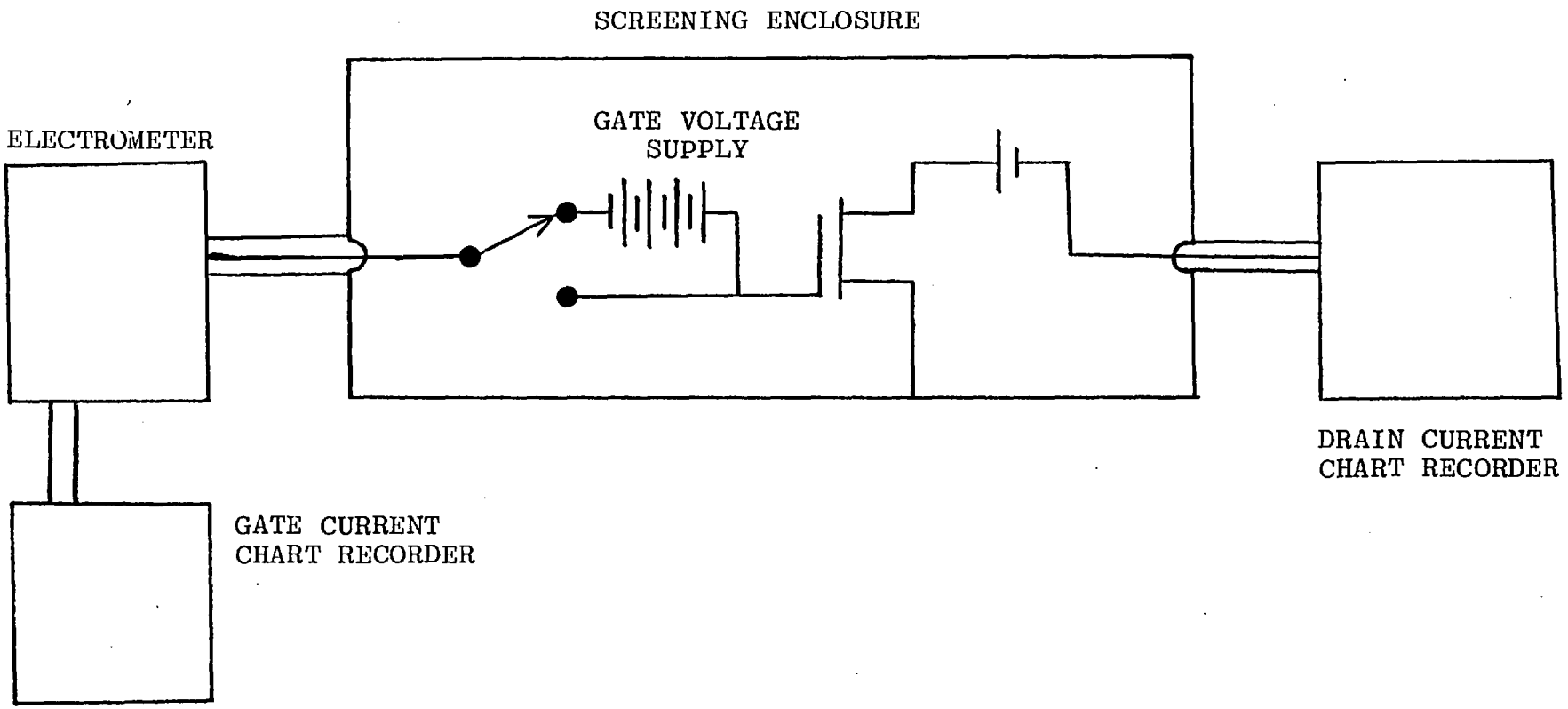

FIG. 4.1 MEASUREMENT CIRCUIT

It was found to be essential to prevent movement of any part of the apparatus during use, including the screened connecting cables. This is because such movement changes the capacitance of the circuit, and altering the capacitance of a charged system causes current to flow. Such spurious current flow is in addition to the actual gate current, and must be prevented. This was satisfactorily achieved by rigidly mounting every component of the system so as to prevent relative movement.

The stray capacitance of the wiring became charged when the gate voltage was applied, this charging current being additional to the true gate current. By measuring this current with no transistor connected in the circuit, it was found to be less than 5% of the transistor gate current. This stray charging current causes most error in the early part of the gate current decay characteristic.

The raw results from the experiment are two graphs from the chart recorders, one of drain current and one of gate current as a function of time. From these results are calculated the density of trapping states in the insulator and their capture cross-section. A mathematical treatment of the theory of the experiment is necessary before a complete description of the processing of the data to yield the desired results is given.

4.4 THEORY OF THE METHOD

The theoretical treatment to be described is due to Ning and Yu[1] and Ning[2]. Two cases are distinguished in the analysis, one being a special case of the other. The mathematically simpler situation occurs when only a small fraction of the available electrons are trapped. The other case is the general situation when no restriction is placed on the degree of trapping.

The general analysis will be treated in detail in the following sections. The analysis of the case for a small degree of trapping is given in full in the paper by Ning and Yu and will not be detailed here. The result only is given in section 4.4.3.

In the first case, the mathematics is such that from the experimental data direct calculation of the effective density of trapping states and their capture cross-section may be made. This method is only applicable to those experiments in which the degree of trapping occuring is small.

The general analysis is applicable to all experiments, and must be used for some. The result of the treatment is such that a direct calculation of the trapping density and cross-section is not possible. It is instead necessary to fit a plot of the experimental data to the equation describing it, adjusting the values of the two unknowns to obtain the best fit between theory and experiment.

4.4.1 Limitations in the Analysis Methods

The first method of calculating the results of the experiments has the advantage, when it is applicable, that a direct calculation of the trap properties is possible. The calculation requires, however, the differentiation of a measured graph, and such a procedure is at best uncertain. The "noise" introduced by differentiation introduces considerable uncertainty into the results obtained.

The alternative method, using curve fitting, involves much more arithmetical effort. However with the aid of a computer this is no real disadvantage. The results obtained will be more accurate because, instead of having to differentiate experimental results, integration of them is necessary. This procedure "smooths out" small data fluctuations.

These considerations led to the use of the curve fitting method of treating the results. A computer programme was written to facilitate the process of producing the large number of curves required.

Where possible the first method was used to calculate the trap parameters as well as the curve fitting method. For the reasons stated above, it is considerably less accurate. Within the limits of accuracy of both calculations, no difference was found in the results calculated by the two methods.

4.4.2 Mathematical Treatment

The co-ordinate system used is shown in Fig.4.2. This co-ordinate system is chosen to simplify the mathematics.

Two assumptions are made in the analysis, the first is that the density of trapping states in the insulator is spatially uniform and the second is that detrapping is unimportant compared to trapping. Both these assumptions will be considered further in later discussion.

The equations describing the rate of trapping as a function of time t and position x are:

$$-\frac{\partial n_t(x,t)}{\partial t} = \frac{1}{q}\frac{\partial j(x,t)}{\partial x} \qquad (4.1)$$

$$\frac{\partial n_t(x,t)}{\partial t} = S\,\frac{j(x,t)}{q}\,(N_T - n_t(x,t)) \qquad (4.2)$$

= cross-section x electron flux x empty trap density

$n_t(x,t)$ - Density of filled traps per unit volume

N_T - Trap density per unit volume

$j(x,t)$ - Current density in the insulator

S - Capture cross-section of the traps

The term on the left-hand side of each equation is the rate of change with time of the filled trap density. Equation 4.1 relates this to the spatial variation of the electron flux in the insulator, that is, the density of electrons available for trapping. Equation 4.2 relates

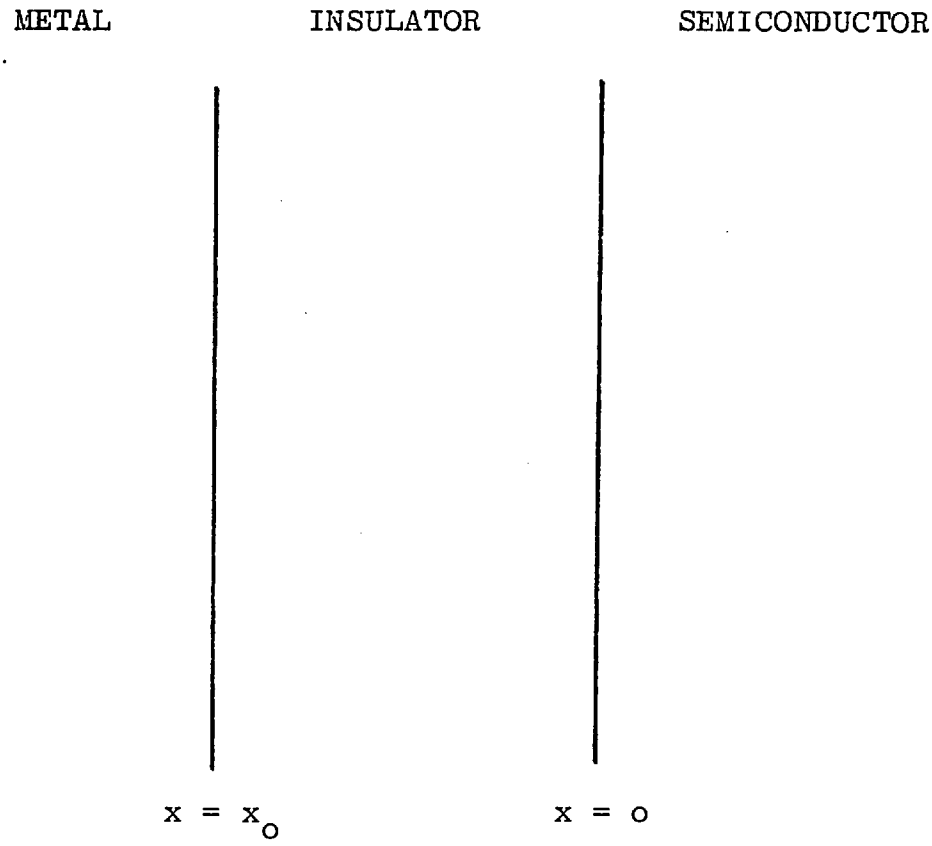

FIG. 4.2 CO-ORDINATES USED IN MATHEMATICAL ANALYSIS

the trapping rate to the density of empty traps, their capture cross-section and the electron flux.

Arnett and Yun[3] have solved these equations, the solution being:

$$n_t(x,t) = \frac{N_T(\exp(SN_i(t)) - 1)}{\exp(SN_i(t)) - 1 + \exp(SN_T x)} \qquad (4.3)$$

$$\text{where } N_i(t) = \int_o^t \frac{j(o,t')}{q}\, dt' \qquad (4.4)$$

and is the density of electrons crossing the plane at $x = o$ in time t.

Thus $qN_i(t)$ is the charge density per unit area injected across the interface between semiconductor and insulator in the experimental time t; it is the time integral of the current flowing across the interface.

It is necessary to relate $N_i(t)$ to quantities which are measurable. The current flowing across the interface $j(o,t)$ is not, of course, directly measurable. The gate current in the external circuit can, however, be measured.

The gate current density j_G is given by:

$$j_G(t) = j(x_o,t) + q\int_o^{x_o} \frac{x}{x_o} \frac{\partial n_t(x,t)}{\partial t}\, dx \qquad (4.5)$$

The first term on the right hand side in this equation is the current due to charge crossing the interface between the insulator and the gate electrode, and the second that

component caused by the rate of change of charge trapped throughout the bulk of the insulator.

If equation 4.1 is integrated with respect to the spatial co-ordinate x the result is:

$$\int_o^{x_o} \frac{\partial j(x,t)}{\partial x}\, dx = -q \int_o^{x_o} \frac{\partial n_t(x,t)}{\partial t}\, dx$$

$$j(x_o,t) - j(o,t) = -q \int_o^{x_o} \frac{\partial n_t(x,t)}{\partial t}\, dx$$

The resulting expression for $j(x_o,t)$ can now be substituted into equation 4.5 with the result:

$$j_G(t) = j(o,t) - q \int_o^{x_o} \frac{\partial n_t(x,t)}{\partial t}\, dx + q \int_o^{x_o} \frac{x}{x_o} \frac{\partial n_t(x,t)}{\partial t}\, dx$$

Now combining the last two terms on the right-hand side, integrating with respect to time, and dividing throughout by the electronic charge q:

$$\int_o^{t'} \frac{j_G(t)}{q}\, dt = \int_o^{t'} \frac{j(o,t)}{q}\, dt - \int_o^{t'} \int_o^{x_o} \left(1 - \frac{x}{x_o}\right) \frac{\partial n_t(x,t)}{\partial t}\, dx\, dt$$

The first term on the right-hand side is $N_i(t')$ from equation 4.4. Performing one integration in the second term on the right-hand side an expression for $N_i(t')$ is thus obtained:

$$N_i(t') = \int_o^{t'} \frac{j_G(t)}{q}\, dt + \int_o^{x_o} \left(1 - \frac{x}{x_o}\right) n_t(x,t')\, dx - \int_o^{x_o} \left(1 - \frac{x}{x_o}\right) n_t(x,o)\, dx$$

The second term will be recognised from Chapter 2 as equation 2.1 where it was seen that:

$$V_T(t) = \frac{q}{C_o} \int_o^{x_o} (1 - \frac{x}{x_o}) \, n_t(x,t) \, dx \qquad (4.6)$$

substituting for the integral in the previous equation the final expression is obtained.

$$N_i(t) = \int_o^t \frac{j_G(t')}{q} \, dt' + \frac{C_o}{q} \left[V_T(t) - V_T(0) \right] \qquad (4.7)$$

Thus $N_i(t)$, the density of electrons injected into the insulator is known in terms of measurable quantities only, and is therefore measurable itself.

It is now possible to relate the change in threshold voltage to the number of charges injected into the insulator by the use of equations 4.3 and 4.6, for any values of trap density N_T and capture cross-section S.

For given values of N_T and S, and for each required value of N_i, equation 4.3 is used to calculate the filled trap density as a function of position, $n_t(x)$. Equation 4.6 is then used to calculate the threshold voltage shift.

The integration in equation 4.6 cannot be carried out analytically, so numerical integration is used. The calculations were performed by a computer program written for the purpose, which calculated the threshold voltage shift for given values of trap density and cross-section, and for a range of values of N_i.

Subsequently, Chang[4] published approximations which enable direct calculation of the threshold voltage shift. The numerical integration procedure was used for all the results described in this work; in future work however the use of the direct calculation would be simpler.

If the experimental results are plotted in the form $\Delta V_T(t)$ versus $N_i(t)$, N_i being calculated using equation 4.7 the resulting curve may be compared with curves generated for various values of S and N_T using equations 4.3 and 4.5. N_T and S are determined by adjusting their values so as to obtain the closest fit between these calculated curves and the experimental results.

It is not in fact necessary to guess blindly at possible values for S and N_T to use in this process. This may be shown as follows:

Differentiation of equation 4.6 with respect to N_i gives:

$$\eta_e(N_i) = \frac{C_o}{q} \frac{d\Delta V_T(N_i)}{dN_i}$$

$$= \int_0^{x_o} \left(1 - \frac{x}{x_o}\right) \frac{\partial n_t(x,t)}{\partial N_i} \, dx$$

and from 4.3

$$\frac{\partial N_T(x,t)}{\partial N_i} = \frac{N_T S \exp(SN_i) \exp(SN_T x)}{(\exp(SN_i) - 1 + \exp(SN_T x))^2}$$

When $N_i = 0$ then this simplifies to:

$$\left[\frac{\partial n_t(x,t)}{\partial N_i}\right]_{N_i = 0} = N_T S \exp(-SN_T x)$$

so that:

$$\eta_e(0) = (1 - \frac{\bar{x}}{x_o}) \int_o^{x_o} N_T S \exp(-SN_T x) \, dx$$

this may be integrated by parts to give:

$$\eta_e(0) = 1 - \frac{1 - \exp(-SN_T x_o)}{SN_T x_o} \qquad (4.8)$$

$\eta_e(0)$ is proportional to the slope of the curve of ΔV_T against N_i taken at the origin, and is therefore known. Then, using 4.8 the quantity $SN_T x_o$ may be calculated, and knowing x_o, SN_T is known. In this way the product of the two unknowns is determined, leaving their individual values to be found by curve fitting.

4.4.3 Special Case of Low Trapping Efficiency

A brief description only is given of the simplifications in the analysis when only a small degree of trapping occurs. In this case, the electron flux is independent of position within the insulator, which means equation 4.1 is no longer required. The solution of equation 4.2 is then:

$$n_t(t) = N_T(1 - \exp(-SN_i(t))$$

where N_i is now defined by:

$$N_i(t) = \int_o^t \frac{j_G(t')}{q} \, dt'$$

The effective trapping efficiency is now defined

$$\eta_e = \frac{C_o}{j_G} \frac{d\Delta V_T}{dt}$$

and may be calculated from the experimental data.

It may be shown that the condition of a small degree of trapping means in fact a low effective trapping efficiency ($\eta_e \ll 1$), so it is easily ascertained whether a particular experiment satisfies this condition or not.

When η_e is obtained from equation 4.6 with the above definition of n_t, the result is:

$$\eta_e = \frac{x_o}{2} N_T S \exp(-SN_i)$$

Obviously both S and N_T may be found from a plot of the logarithm of η_e versus N_i. This then is the method of analysis for the case of low trapping efficiency.

4.5 RESULTS OF THE EXPERIMENT

In this section a full description of the results of the measurement described in the previous sections will be given. Firstly, the procedure used in the calculations will be illustrated with reference to one measurement on one device. For all the other measurements only the final results will be given, since the same method of obtaining the results was used in all cases.

4.5.1 Data Reduction

The results of one experiment will be taken as an example and the necessary calculations gone through step

by step. The device used was a standard sample as described previously. The measurements were made with the sample connected in the circuit of Fig.4.1. The raw data which results from the experiment is a set of three graphs. These are plots of drain current and gate current as a function of time, and a field effect curve, that is, a plot of the dependence of drain current on gate voltage. These are shown in Figs. 4.3, 4.4 and 4.5 respectively.

The first step is to convert the drain current curve of Fig.4.3 into a corresponding plot of threshold voltage change with time, the conversion between the two being done by using the field effect curve of Fig.4.5. This is in fact just the multiplication of Fig.4.3 by a constant, the constant being the slope of the field-effect curve (the transconductance of the device). The resulting curve of threshold voltage change against time for this device is shown in Fig.4.6.

The next step is to calculate the density of charge transferred across the semiconductor-insulator interface, using equation 4.7. The first term in equation 4.7, the integral of the gate current density curve, is found by graphical integration of the gate current curve of Fig.4.4. The second term is found by the multiplication of the threshold voltage curve, Fig.4.6, by the appropriate factor. Summation of these two terms gives the required quantity $N_i(t)$. This is plotted in Fig.4.7.

The final step is to take the data from the two curves of Figs. 4.6 and 4.7 and plot one as a function of the other. The result is shown in Fig.4.8 where the

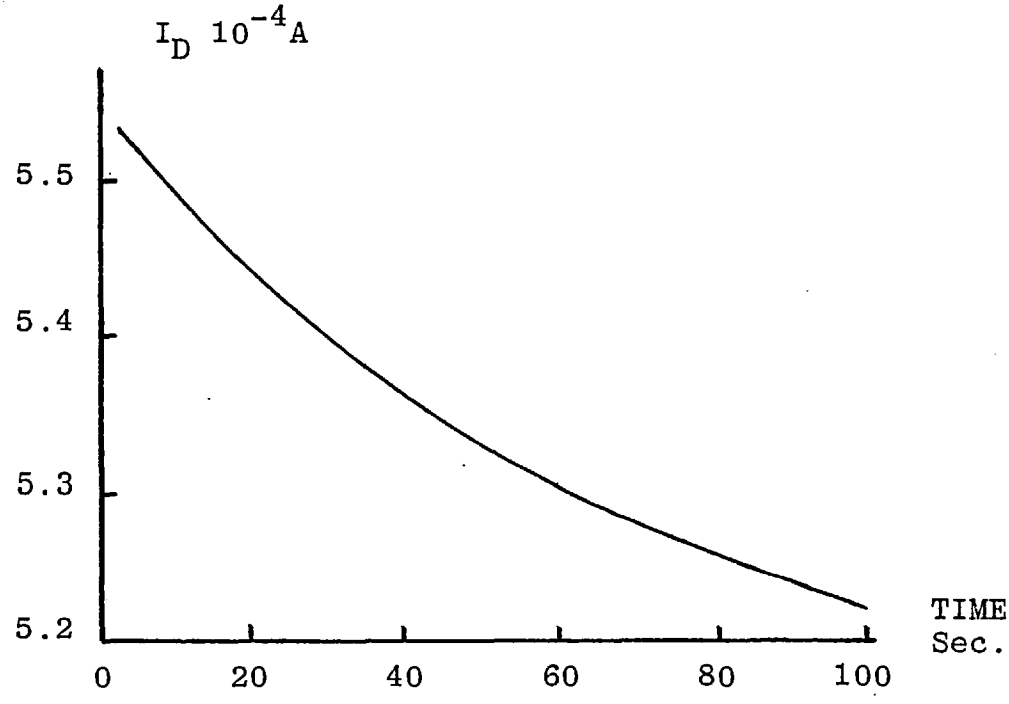

FIG. 4.3 MEASURED DRAIN CURRENT - TIME CURVE

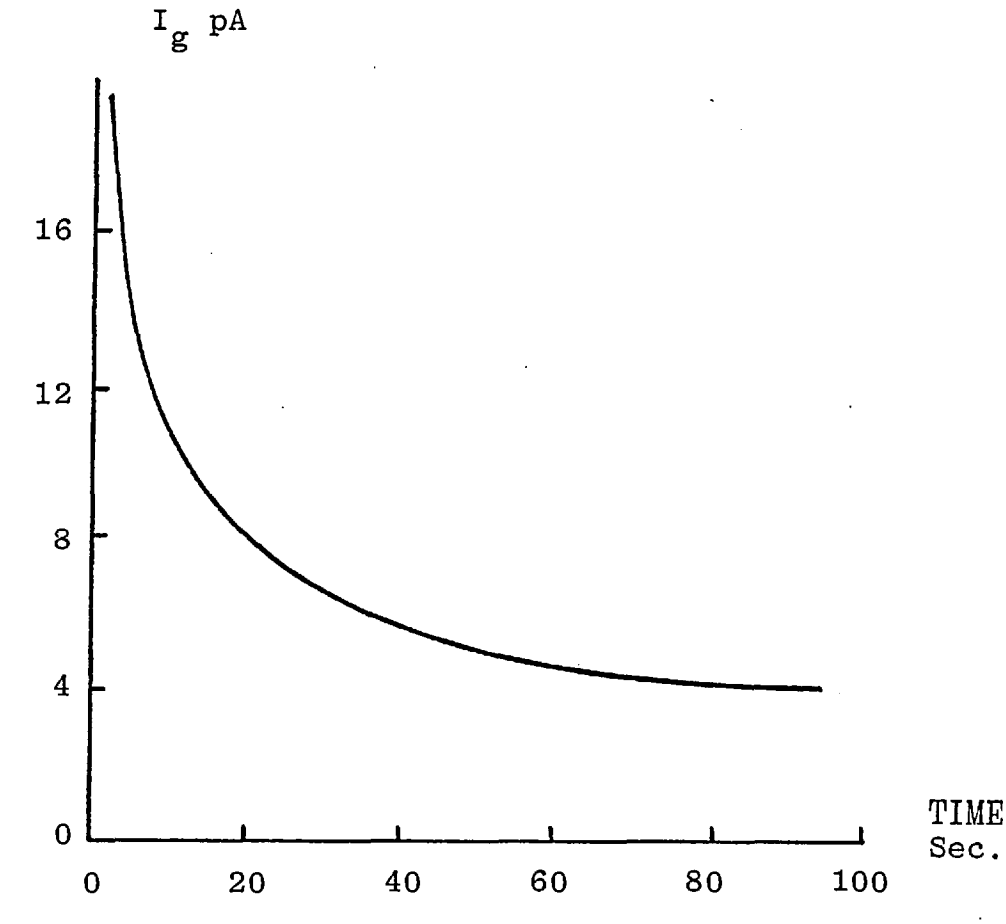

FIG. 4.4 MEASURED GATE CURRENT - TIME CURVE

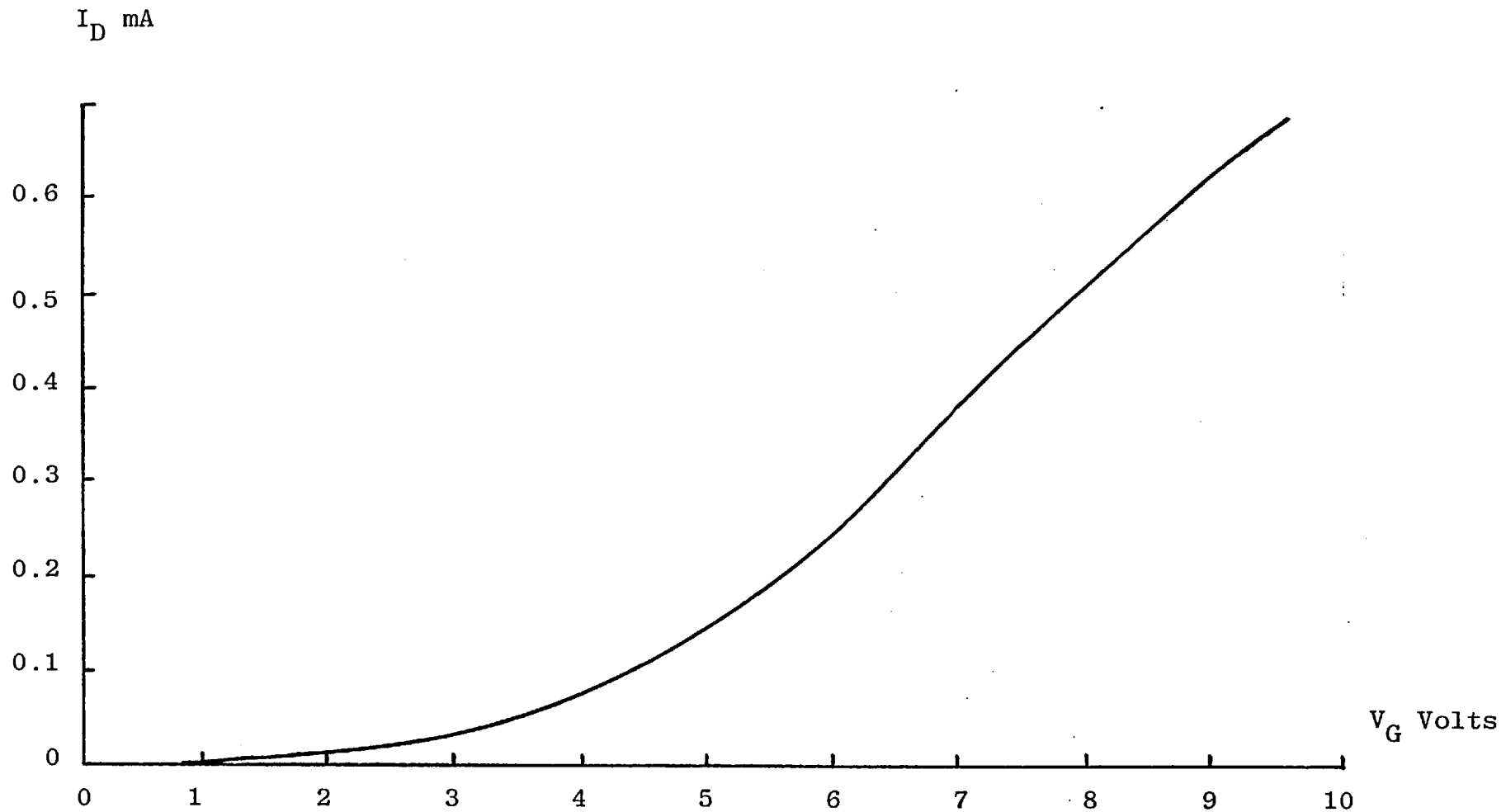

FIG. 4.5 MEASURED DRAIN CURRENT - GATE VOLTAGE CURVE

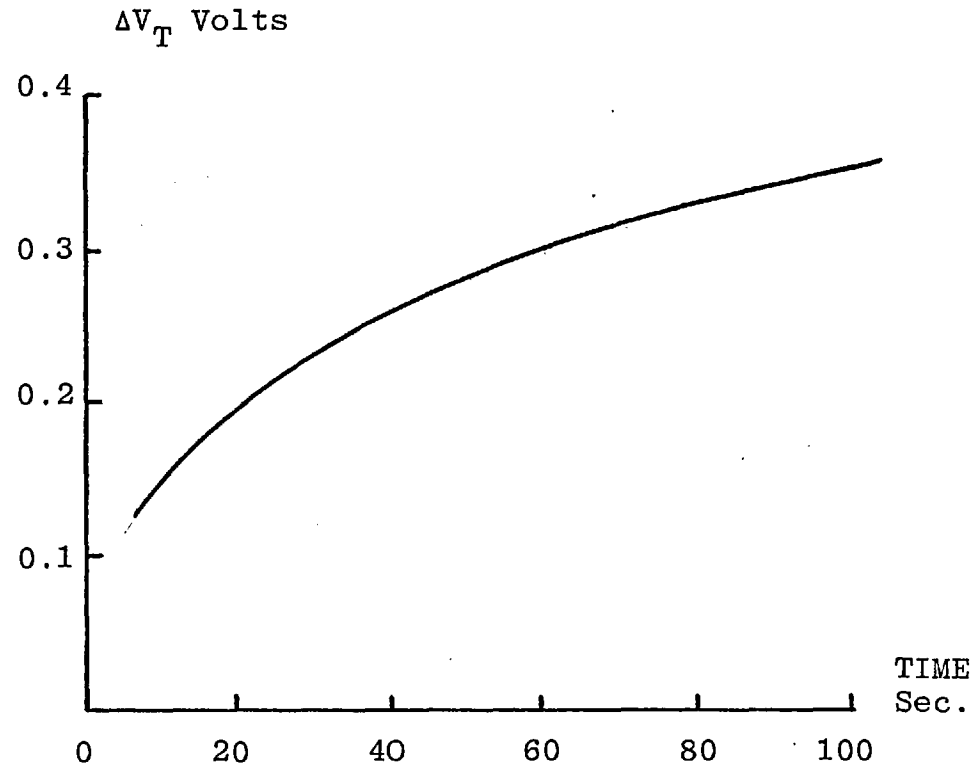

FIG. 4.6 THRESHOLD VOLTAGE - TIME CURVE

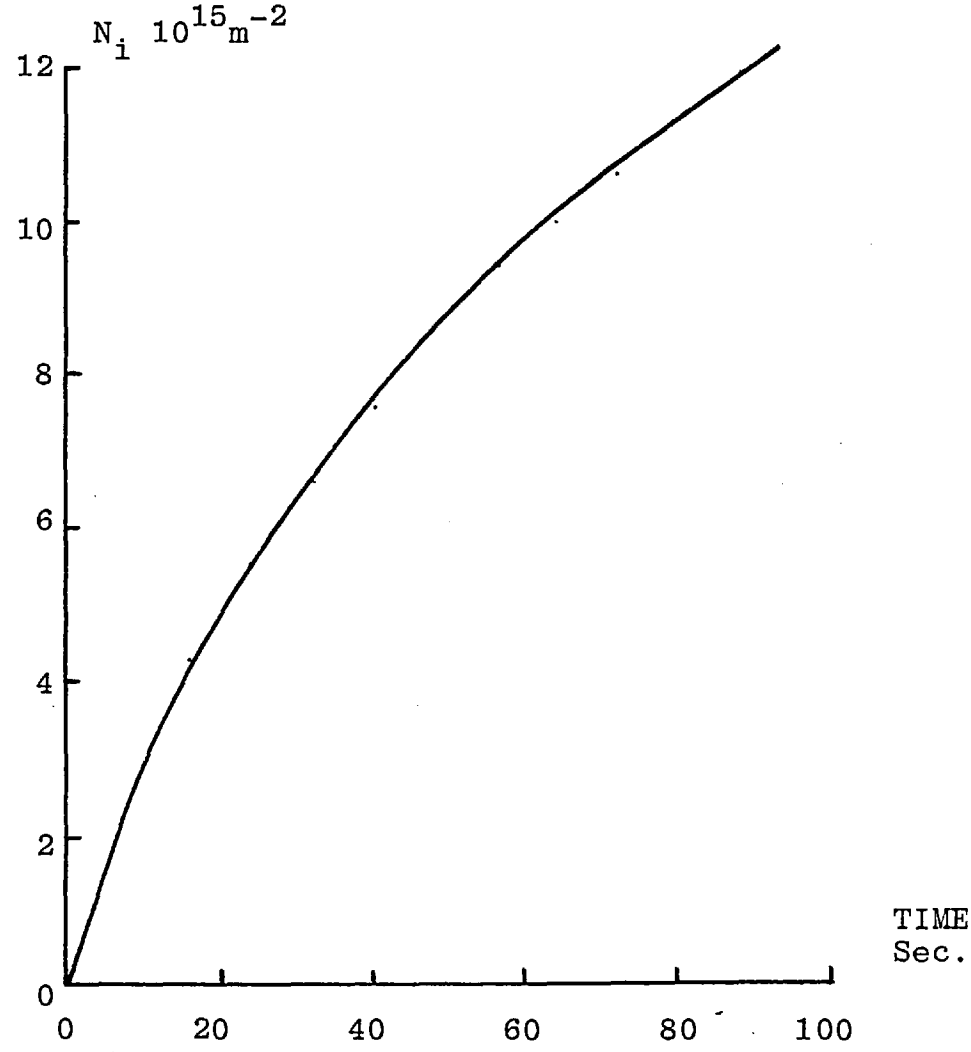

FIG. 4.7 CHARGE DENSITY - TIME CURVE

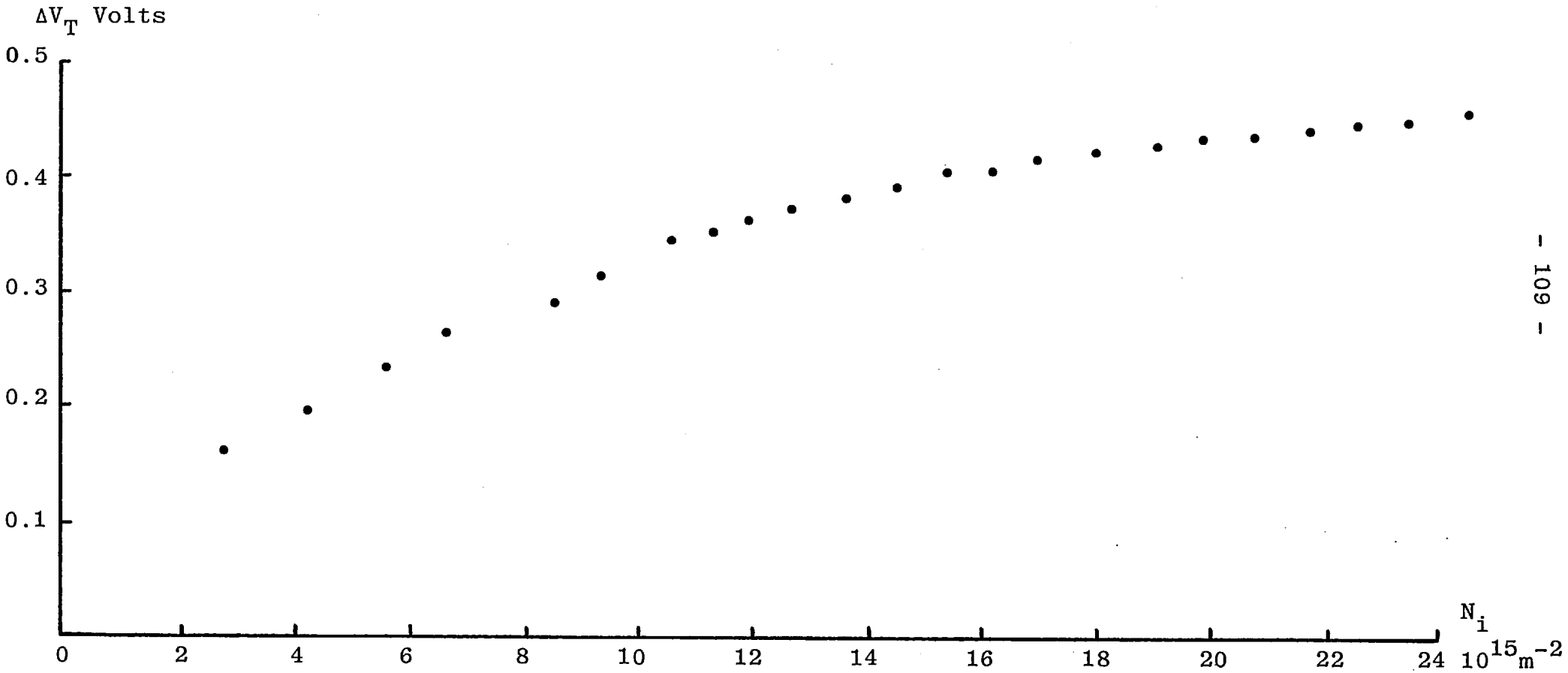

FIG. 4.8 EXPERIMENTAL THRESHOLD VOLTAGE-CHARGE DENSITY CURVE

threshold voltage shift is plotted as a function of N_i. This curve is the one that is required to be fitted to equation 4.6. In the next section the use made of this curve will be demonstrated.

4.5.2 Calculations on Reduced Data

As explained in Section 4.4.2, from the slope of the last curve at its origin it is possible to calculate the product of the two unknown quantities S and N_T. Equation 4.8 is used to find this product from the slope of the curve. This equation cannot be solved explicitly so a graphical method was used. When the calculation is performed for the curve of Fig.4.8, the value found for the product of the two quantities is: $SN_T = 4.3 \times 10^6 \ m^{-1}$.

With this constraint on the values of S and N_T the computer program was used to calculate curves as described in Section 4.4.2. Several such curves are shown in Fig.4.9 for different values of S and N_T, in each case the product SN_T being the same. These curves are then compared with the experimentally determined points of Fig.4.8 and which are also replotted in Fig.4.9. One curve is seen to give a very good fit to the experimental points, and this curve then gives the values of the trapping parameters:

Trap cross-section $S = 1.4 \times 10^{-16} m^2$

Trap density $N_T = 3.1 \times 10^{22} \ m^{-3}$

In the next section, the results of all such measurements made are given.

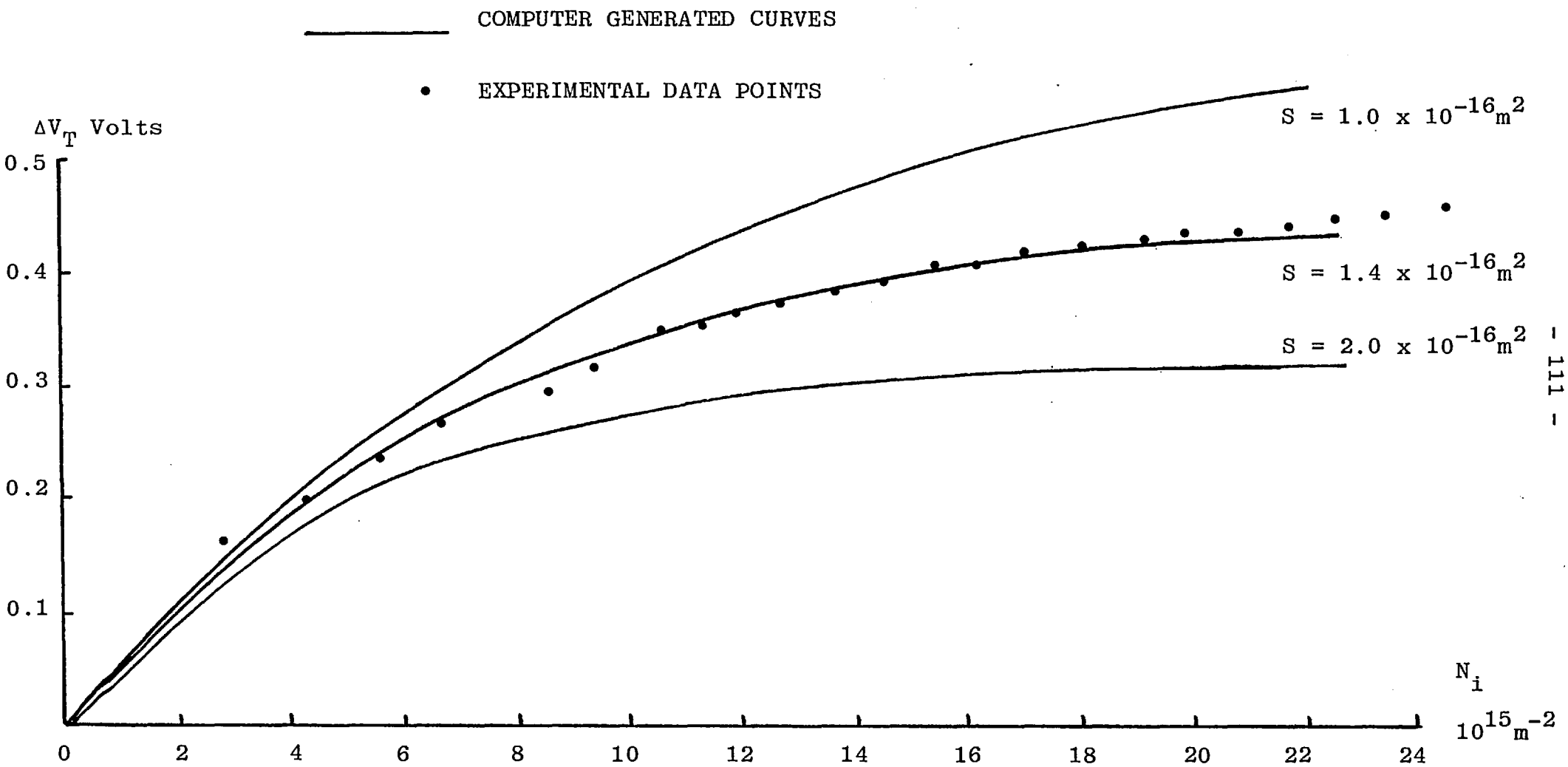

FIG. 4.9 EXPERIMENTAL AND THEORETICAL THRESHOLD VOLTAGE-CHARGE DENSITY CURVES

4.5.3 Results

In the previous sections the method of processing the experimental data to yield the required result has been illustrated. The experiment was done on other devices of the same type, with widely differing degrees of trapping occuring in each. The calculations were performed as for the example above; only the final results will be given. The values obtained for the trap capture cross-sections and trap densities are shown in Table 4.1.

Also included in the table is an estimate of the slow state density, obtained from the measurements described in Chapter 3. This is included in order to see what correlation, if any, may be found between the two sets of results. Devices with a low slow state density have very little trapping occuring, whereas devices with a high slow-state density have such an amount of trapping as to make them useless for practical purposes.

Table 4.1 shows the results obtained for every device measured, with one exception. The exception was a device where the gate current-time curve was markedly different from that usually found. Instead of manifesting a decay with time, the current was almost constant, and 10^3 -10^4 times higher than that for other devices. This behaviour was similar to that found when the insulator of the device had been broken down by applying a high voltage to the gate. It was therefore assumed that the device was defective and it was discarded.

T A B L E 4.1

TRAP DENSITY and CROSS-SECTION RESULTS

Sample No.	Cross Section	Density	Slow State Density
C 26 R	1.4×10^{-16}	3.1×10^{22}	Medium
C 43 L	1.6×10^{-15}	4.0×10^{22}	V. High
C 30 R	3.9×10^{-16}	6.2×10^{22}	Medium
C 35 L	3.1×10^{-16}	1.0×10^{22}	Low
C 34 L	1.5×10^{-15}	1.0×10^{23}	V. High
C 12 L	5.0×10^{-16}	5.0×10^{22}	Low

4.5.4 Discussion of Results

Upon examination it will be seen that the values obtained for the capture cross-section of the traps are of order 10^{-16} m^2, two devices giving a result an order of magnitude larger. These two devices are also the ones in which a very high slow state density was observed. The trap densities found are all within one order of magnitude of each other.

These values for the capture cross section are consistent with the trapping species being a coulombic attractive potential trapping state. The cross section for such a trap in a material of dielectric constant ϵ is given by Bube[5] as

$$S \sim \frac{10^{-14}}{\epsilon^2} \quad m^2$$

which for the case of silicon dioxide works out to be approximately 6×10^{-16} m^2, in fair agreement with the values measured.

Several conclusions may be inferred from the closeness of fit of the data to the theoretical curve concerning the properties of the traps.

In the mathematical analysis it was assumed that the density of traps was uniform, and that de-trapping was unimportant, and the equations derived incorporated these assumptions. The fact that a good fit is obtained suggests that those conditions are indeed fulfilled. Any difference between experimental and theoretical curves appears to be greatest at low values of N_i. However,

this is also the region of the curve where the experimental errors are greatest.

If such differences close to the origin of the curve are due to a non-uniform trap density, such non-uniformity is close to the interface between insulator and semiconductor.

The fact that such a good fit can be obtained with single values for the density and capture cross-section of the traps suggests that there is only a single population of traps which cause most of the trapping in the TFT. If there were more than one group of traps, with different cross-sections, it would not be possible to fit the data to a theoretical curve. Instead two or more curves, summed together, would be required.

Traps with a larger capture cross-section have most effect at low values of N_i, and those with a smaller cross-section at higher values of N_i. Thus it can be stated that if there were further groups of traps in the insulator material they must have capture cross-sections considerably larger or smaller, by two orders of magnitude, than the main group which is measured. It can also be said that any large cross-section traps must be present at a much lower density than the main group of traps, or else the larger trap would dominate the trapping process.

The devices used in these experiments have R.F. sputtered silicon dioxide insulator films, whereas the bulk of previous work has been concerned with thermally grown material on single-crystal silicon. Bearing in

mind the necessity to exercise caution in comparing results of measurements on materials made in different ways, previous results can be examined.

The properties of many trapping centres have been investigated in recent years. On this basis of experiments in which the trapped charge in MOS devices was found to be controllable by oxidation reduction treatments[6] oxygen vacancies were suggested as trapping species. The capture cross-section of traps whose concentration was varied in this way was found to be approximately $3 \times 10^{-17} m^2$.[7]
Trapping centres due to water in SiO_2 were found to have capture cross-sections much smaller than this[8].

Exact identification of the trapping species in the present devices has not been made. It will be recalled from the slow state measurement results described in Chapter 3 that the purer the gas used in sputtering, the smaller the degree of trapping. This suggests that an impurity in the gas mixture may be incorporated into the sputtered film and be responsible for trapping in the completed device. The impurities in the gas are caused by residual air in the vacuum system, which means there are many possible contaminants. This is further discussed in Chapter 6.

It is known that if silicon dioxide is sputtered in pure argon gas the resulting film is non stoichiometric, being deficient in oxygen[9]. It is necessary to add oxygen to the gas mixture in order to obtain a film which

is more nearly stoichiometric. It will of course be impossible to obtain a perfect film even if sputtering is carried out in pure oxygen, since there will always be an irreducible minimum thermodynamically determined concentration of defects. In practice, the amorphous structure of the film can be expected to introduce additional defects.

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CHAPTER 5 ADDITIONAL MEASUREMENTS

5.1 INTRODUCTION

This chapter describes the results of the remaining measurements made on the thin film transistors. Firstly, threshold voltage-time dependence measurements were made, from analysis of which the trapping state density was determined. These measurements are described in Section 5.2. Secondly, in Section 5.3, measurements of the low frequency noise characteristics of the TFT are discussed. This is largely qualitative, quantitative analysis of such measurements being uncertain.

Thirdly, some experiments were done on transistors made with an yttrium oxide (Y_2O_3) insulator film as an alternative to silicon dioxide and are described in Section 5.4. Finally, infra red absorption spectra measured on the silicon dioxide insulator films of the standard devices are described.

5.2 THRESHOLD VOLTAGE TIME-DEPENDENCE

In the experiments so far described the change of threshold voltage caused by slow-state trapping has not been considered as a function of time. In the slow state density measurements the change of threshold voltage in a fixed time was measured, and in the cross-section measurements the changing threshold voltage was measured as a function of the quantity of charge passing through the device. Much useful information can also be obtained from examination of the time dependence of the threshold

voltage. Such measurements and the results obtained and conclusions drawn from them are described in the following sections.

There are many processes which cause threshold voltage variation in field-effect devices. One such important process is the motion of electrically charged ions in the insulator material of the device under the influence of the gate field. The charged ions partially screen the semiconductor surface from the gate field, the magnitude of this effect varying with the location of the ions.

In silicon MOS devices sodium ions in particular are very troublesome, because they have a fairly high mobility in silicon dioxide and are a common environmental contaminant. Snow et al[1] examined the process of drift in MOS devices which had been deliberately contaminated with sodium during manufacture. To summarise briefly their findings, the change of threshold voltage under an applied gate field was found to be proportional to the half power of time, and to increase with gate field. Saturation of the drift occurred, at a value independent of gate field, the saturation value of the threshold voltage drift corresponding to the density of ions introduced into the insulator. These results were interpreted as supporting a diffusion model for the ion drift process.

The thin film transistors under investigation are n-channel devices. The threshold voltage drift is

always found to be in the same sense, a positive gate voltage causing the threshold voltage to become more positive. Sodium ions, being positively charged, would move towards the semiconductor under a positive gate voltage, causing a corresponding increase in the electron density in the semiconductor, and therefore a decrease of threshold voltage - the reverse of the effect observed. To cause drift in the sense observed, a negative mobile ion would be necessary.

Trapping of charge in localised states in the insulator can also cause threshold voltage changes, with electrons from the semiconductor reaching the insulator traps by tunneling through the potential barrier at the semiconductor-insulator interface. This was the mechanism suggested as being responsible for the effect in SiO_x/InSb thin film transistors by Sewell[2].

This process of tunneling into and out of localised states in an insulator is now of considerable technical importance, because it is fundamental to the operation of "memory" MOS transistors and has been extensively studied in such devices. Detailed investigations have been undertaken by, for example, Lundkvist et al[3] and Ross and Wallmark[4]. The devices investigated were MNOS (metal-nitride-oxide-semiconductor) double-insulator devices, in which charge tunnels through a very thin (approximately 20Å) oxide layer to traps in the silicon nitride. The theory developed to describe such devices is also applicable however to single insulator devices such as the TFT.

Theoretical investigation of the tunneling process shows that the change of threshold voltage is proportional to the logarithm of time. This relationship is derived in the papers cited.

In the following sections, the measurements undertaken on the thin film transistors are given and the results observed are described.

5.2.1 Measurements and Results

The measurements of the changing threshold voltage was made by observing the transistor's drain current, at a constant gate voltage, and converting the drain current change into the equivalent gate voltage change by means of the measured drain current/gate voltage curve as previously described. The drain current was plotted on a chart recorder for the initial part of the curve, whilst for times greater than approximately one minute the current was measured by means of a digital voltmeter. The response time of the chart recorder was such that the shortest time for which the current was accurately recorded was approximately one second. Accordingly, the drain current at this time was used as the reference value from which to calculate the change at later times.

The measurements were performed by simply applying a gate voltage at time t = o, which caused a step-function increase in drain current. The subsequent decrease of drain current with time was then observed and the corresponding change of threshold voltage calculated.

Many such measurements were made on different transistors, with similar results in each case. When plotted against time on a logarithmic scale, a close fit to a straight line was obtained in each case. A typical such results is shown in Fig. 5.1. In this particular measurement the experiment was continued for 1,000 seconds, but in some measurements the same linear dependence was observed to hold for much longer times, up to at least 2×10^4 seconds.

This time dependence is, as has been stated, characteristic of a tunneling process for the transfer of electrons from the semiconductor into trapping states in the insulator.

The simplest tunneling process is that in which the initial and final electron states are located at the same energy level and separated in space. An alternative is thermally assisted tunneling in which the initial and final electron states are separated in energy as well as in space[5]. During tunneling the energy difference is made up by the emission or absorption of a phonon. The tunneling process may be regarded as a thermal activation step followed by tunneling (or vice versa), see Fig. 5.2. The effect of this on the threshold voltage - time dependence will be to introduce a temperature dependence which does not exist in the case of simple tunneling.

The measurements described above were performed at different temperatures in order to observe the behaviour of the trapping process. A set of decay

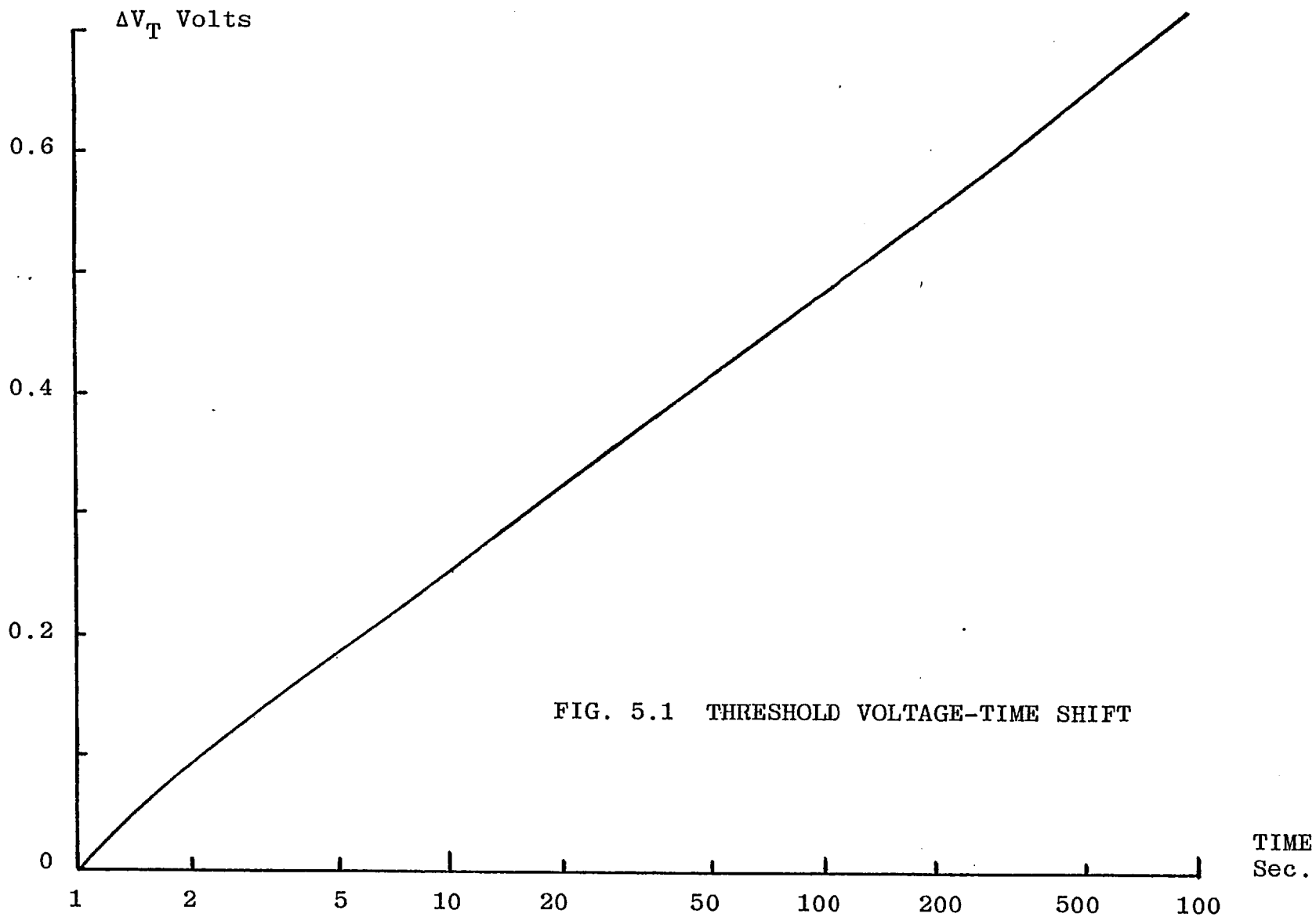


FIG. 5.1 THRESHOLD VOLTAGE-TIME SHIFT

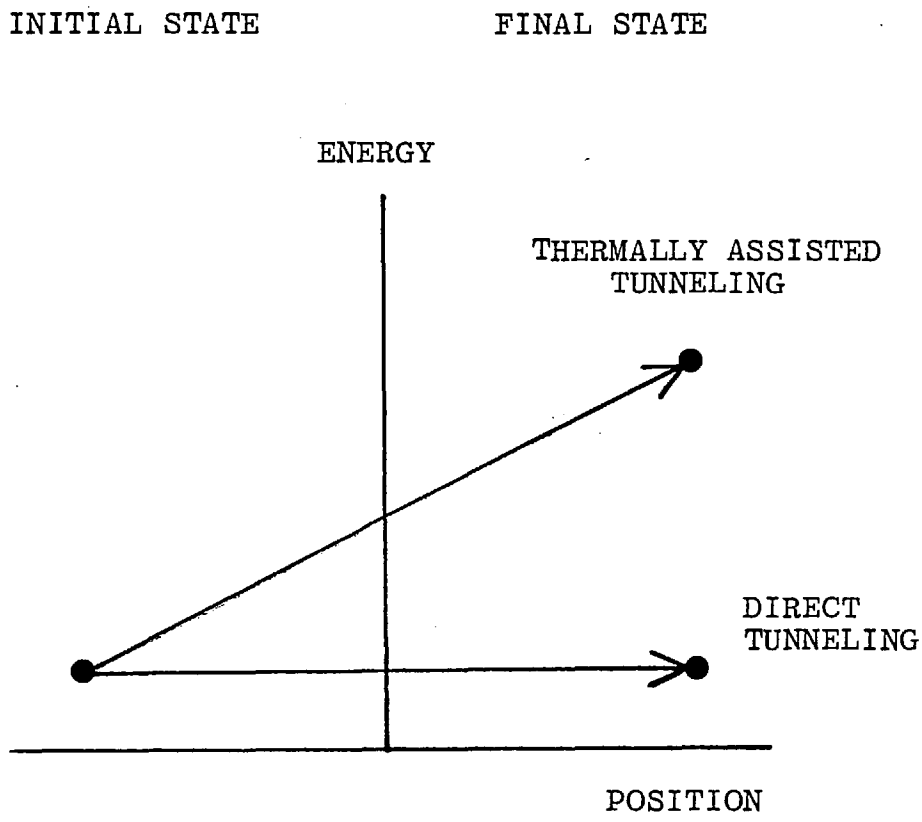


FIG. 5.2 QUANTUM MECHANICAL TUNNELING

plots of threshold voltage against time on a logarithmic scale, for various temperatures is shown in Fig. 5.3.

The data points for each temperature were fitted to a straight line by the standard least-squares method. From this analysis a value was obtained, for each temperature, for the decay rate r_d and its probable error, where r_d is defined as:

$$r_d = \frac{dV_t(t)}{d \log_{10} t} \qquad (5.1)$$

These values of r_d are plotted on an Arrhenius plot ($\ln r_d$ vs $1/T$) in Fig.5.4. The error bars on this plot denote the extent of the probable error for each value of r_d.

The finding of a straight line on this plot shows that the process is an activated one, being described by an equation of the form:

$$r_d = r_o \exp(-E/kT)$$

The data points were analysed by the least squares procedure as before, to determine the activation energy E. The value of the activation energy obtained in this way is $.12 \pm .01$ eV.

The equation describing the threshold voltage shift has therefore been found to be of the form:

$$V_T(t) = A_o\left[\exp(-\frac{E}{kT}) \ \ln\frac{t}{\tau} + B\right]$$

The first term $A_o \exp(-E/kT)$ contains within it the so-called supply function, that is, the density of

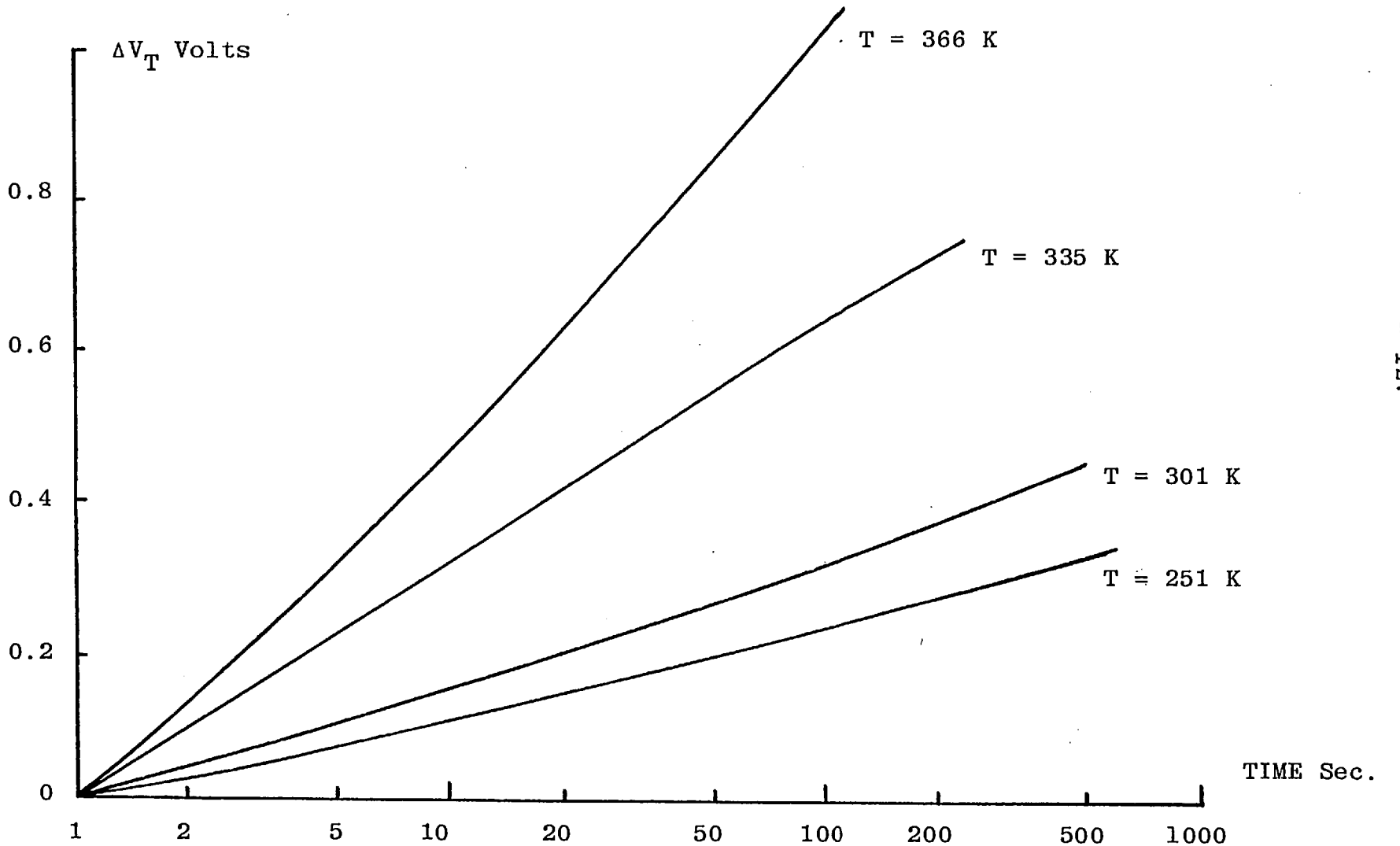


FIG. 5.3 THRESHOLD VOLTAGE-TIME/TEMPERATURE SHIFT

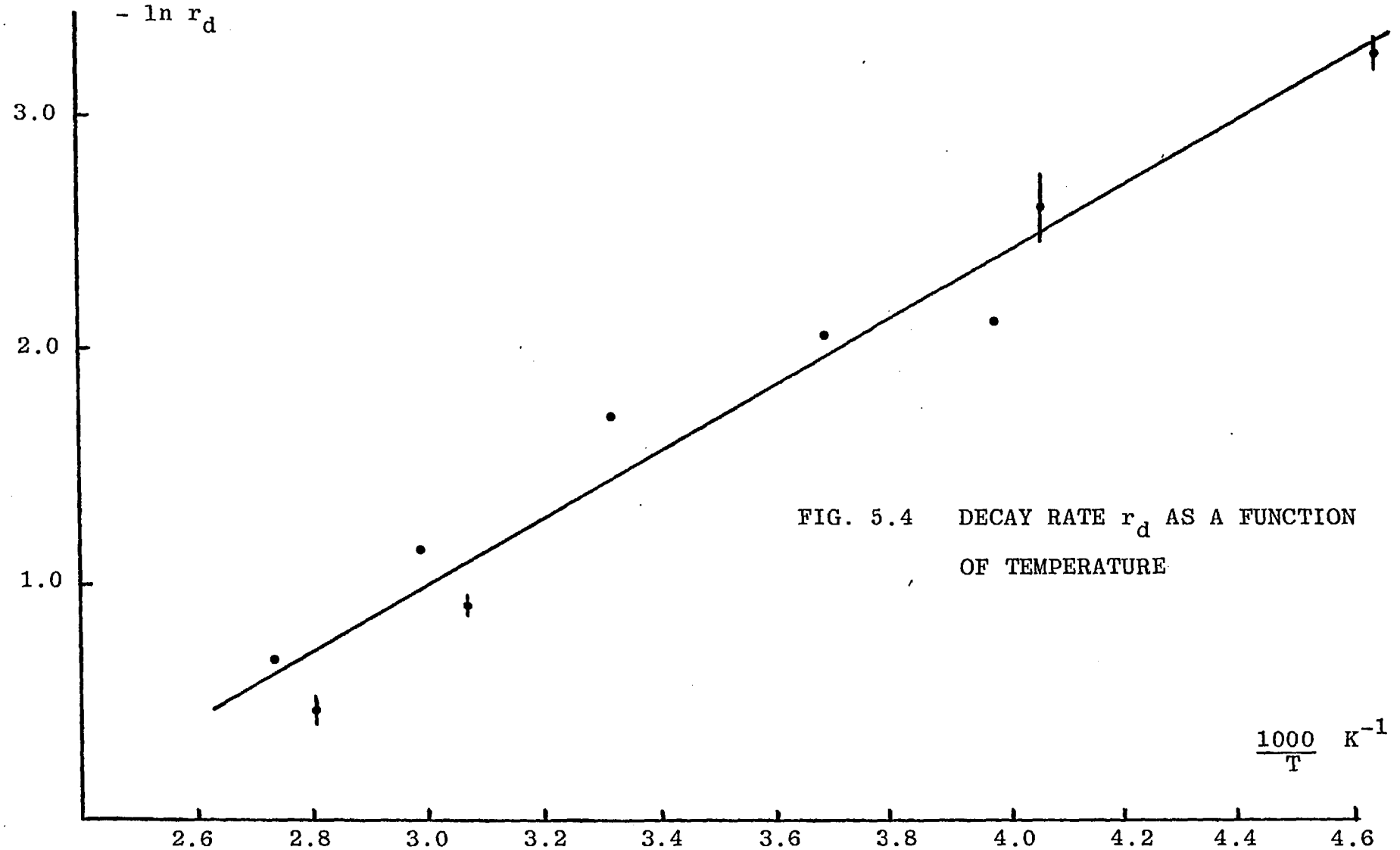


FIG. 5.4 DECAY RATE r_d AS A FUNCTION OF TEMPERATURE

electrons at the semiconductor-insulator interface which is available for trapping. The activation energy determined above is part of this quantity.

Measurement of the temperature dependence of the semiconductor conductivity results in the finding of a similar relationship of the same form, with a similar value of activation energy. This shows that the temperature dependence of the trapping process is caused by that of the carriers in the semiconductor.

Analysis of the trapping process assuming that a thermally assisted tunneling process is operating, in the same way as for the direct tunneling case considered in Section 2.3, results in an equation for the threshold voltage shift of the form:

$$V_T(t) = A_o \left[\ln \frac{t}{\tau} + \frac{E_A}{kT} + B \right]$$

where E_A is the difference between the energy levels of the initial and final states. This has a completely different temperature dependence to that actually found.

The variation of threshold voltage shift with temperature is attributable to the supply function variation with temperature, any thermally activated step being small. The tunneling process therefore appears to be direct.

The trapping states are therefore located at almost the same energy level as the conduction band edge of the semiconductor. The energy level of the semiconductor conduction band edge is varied by the applied gate voltage, and has itself a spread in energy, due to the

polycrystalline nature of the material. This in turn must mean that there exist trapping levels spread over a range of energies, rather than a discrete trapping level.

From the results of these measurements it is difficult to obtain quantitative information, because of the appearance of the supply function in the equation. Further measurements were performed in which a known quantity of charge was trapped, and then the process of de-trapping observed. These measurements are described in the next section.

5.2.2 Further Measurements

The basis of the measurements to be described is to inject a certain known quantity of charge into the insulator trapping states, causing an initial change of threshold voltage, and then to observe the time dependence of the threshold voltage as the device returns to its initial condition.

The initial shift of threshold voltage is produced by the application of a positive gate voltage pulse, which shifts the threshold voltage towards a more positive value. At the end of the pulse, the gate voltage is returned to its previous value. This gate pulse deposits charge into the insulator traps. The drain current of the transistor is then recorded on a chart recorder as a function of time. The changing drain current is converted into a threshold voltage change by use of the drain current-gate voltage curve. The initial shift of the threshold

voltage, immediately after the gate voltage pulse, corresponds to the quantity of charge deposited in the insulator traps. The time sequence of the measurement is shown in Fig.5.5.

The results of one typical such set of measurements are shown in Fig.5.6 in which the change of threshold voltage is plotted as a function of time on a logarithmic scale. As in the previous measurements linear plots are obtained, the data points falling in close proximity to the straight line drawn through them. The rate of decay of the threshold voltage (that is, the gradient of each of the Fig.5.6 plots) defined in equation 5.1, is found to vary with the initial threshold voltage shift. The first of these quantities is plotted as a function of the second in Fig.5.7. It is seen that an approximately linear relationship is found. This is in agreement with the theory of the experiment to be outlined below.

The behaviour of MNOS devices in this type of experiment has been considered in the paper by Lundkvist et al. The model used in this analysis is one of tunneling to localised trapping states in the insulator. Two limiting cases were considered in the analysis, according to whether the density of charge injected into the insulator is comparable with or smaller than the density of trapping states in the insulator.

The trapped charge distributions resulting in the two cases are shown in Fig.5.8. In the equations describing those distributions the quantity N_T is the density of insulator trapping states, N_O the density of

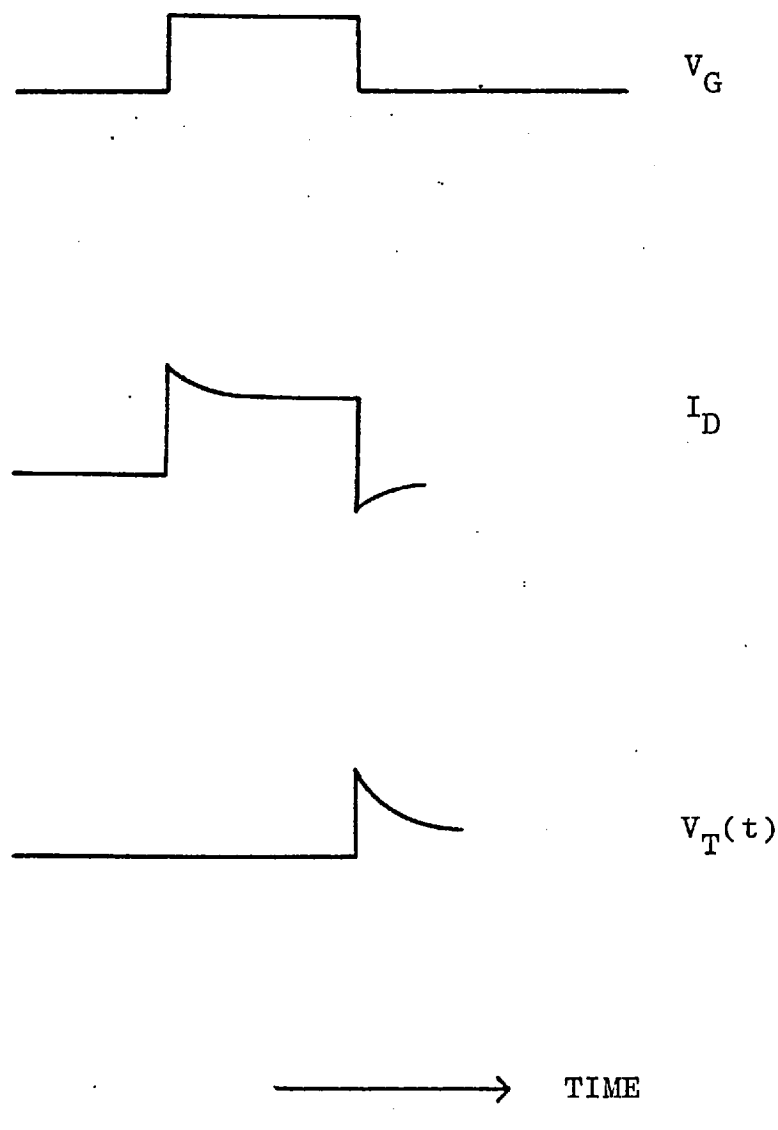


FIG. 5.5 TIME SEQUENCE OF THRESHOLD VOLTAGE MEASUREMENT

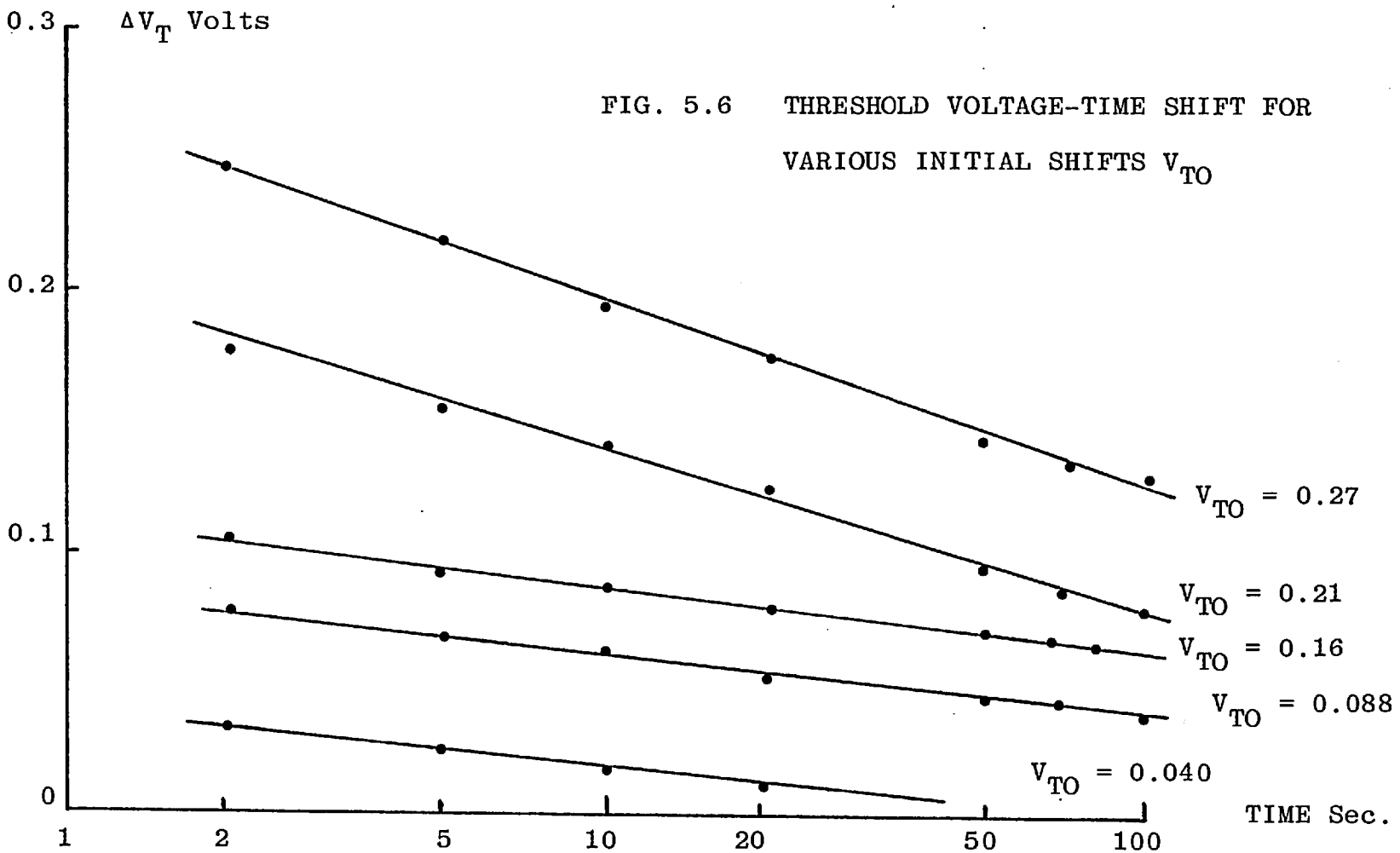


FIG. 5.6 THRESHOLD VOLTAGE-TIME SHIFT FOR VARIOUS INITIAL SHIFTS V_{TO}

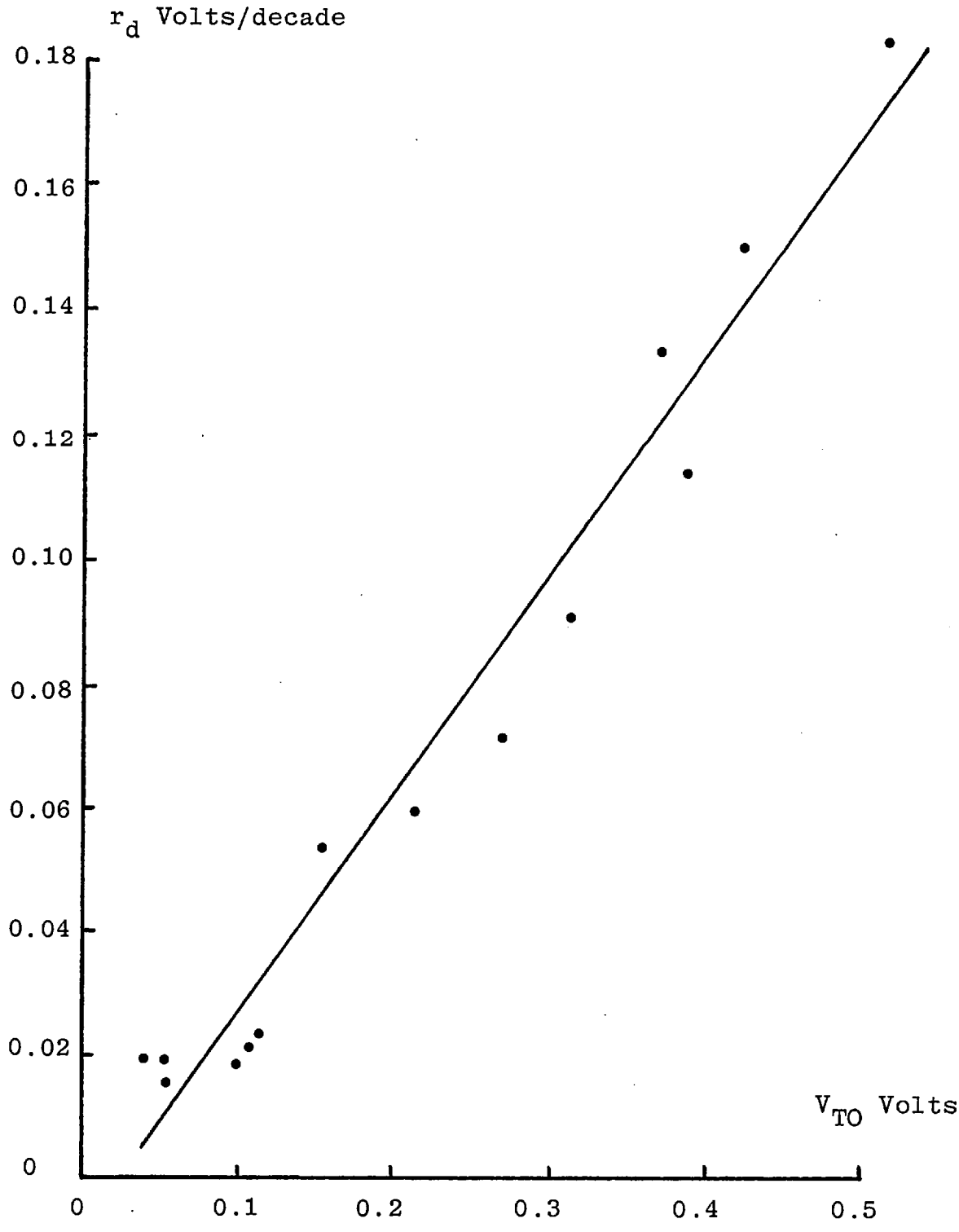
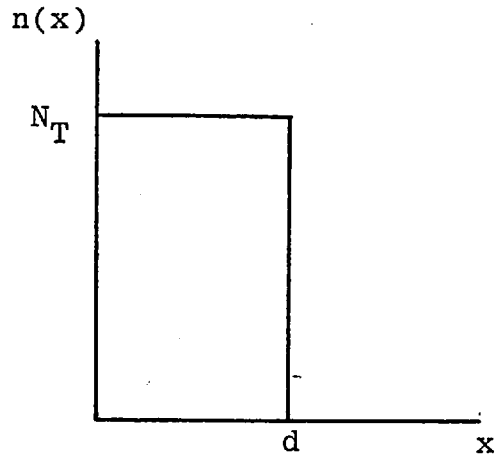
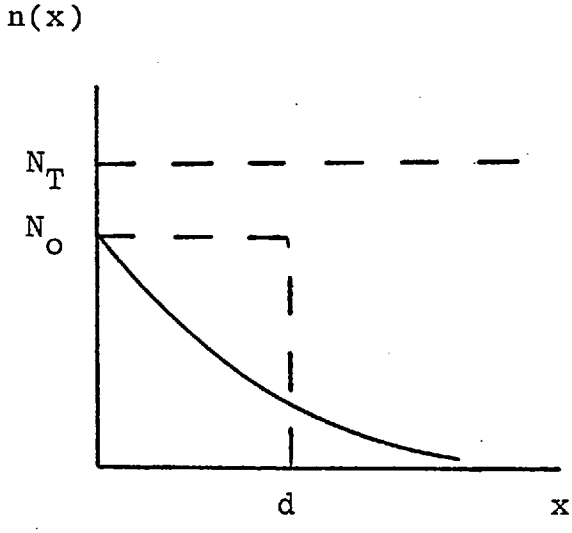


FIG. 5.7 DECAY RATE AS FUNCTION OF INITIAL THRESHOLD VOLTAGE SHIFT.



$$n(x) = N_T, \quad x < d$$
$$= 0, \quad x > d$$

$$V_{To} = \frac{q}{C_o} N_T d$$



$$n(x) = N_o \exp -\frac{x}{d}$$

$$V_{To} = \frac{q}{C_o} N_o d$$

FIG. 5.8 INSULATOR CHARGE DISTRIBUTIONS

filled states at the interface, and d a characteristic length describing the distribution.

Analysis of this model predicts the form of the threshold voltage change to be proportional to log (time) as observed. For the distribution of charge of Fig.5.8(ii) (low injected charge density) the decay rate r_d is found to be proportional to the initial threshold voltage shift V_{To} (which is of course proportional to the initially injected trapped charge). For the other charge distribution, that is for a large initial threshold shift, the decay rate is constant and does not vary with initial threshold shift. The results of Fig.5.7 therefore indicate that in this measurement the trapped charge density is much less than the trapping state density.

The theoretical analysis developed by Lundkvist et al will be briefly described in order to show what information may be obtained from the results of the measurements. For full details of the analysis the original paper should be consulted.

5.2.3 Analysis of Experiment

The energy level diagram of the model used in this analysis is shown in Fig.5.9. Electrons in trapping states in the insulator band gap "see" a barrier of height E_t through which they tunnel to the semiconductor conduction band. This situation is described by the quantum mechanical Schrodinger equation, the solution of which gives an expression for the probability of a trapped electron escaping from the localised state. The

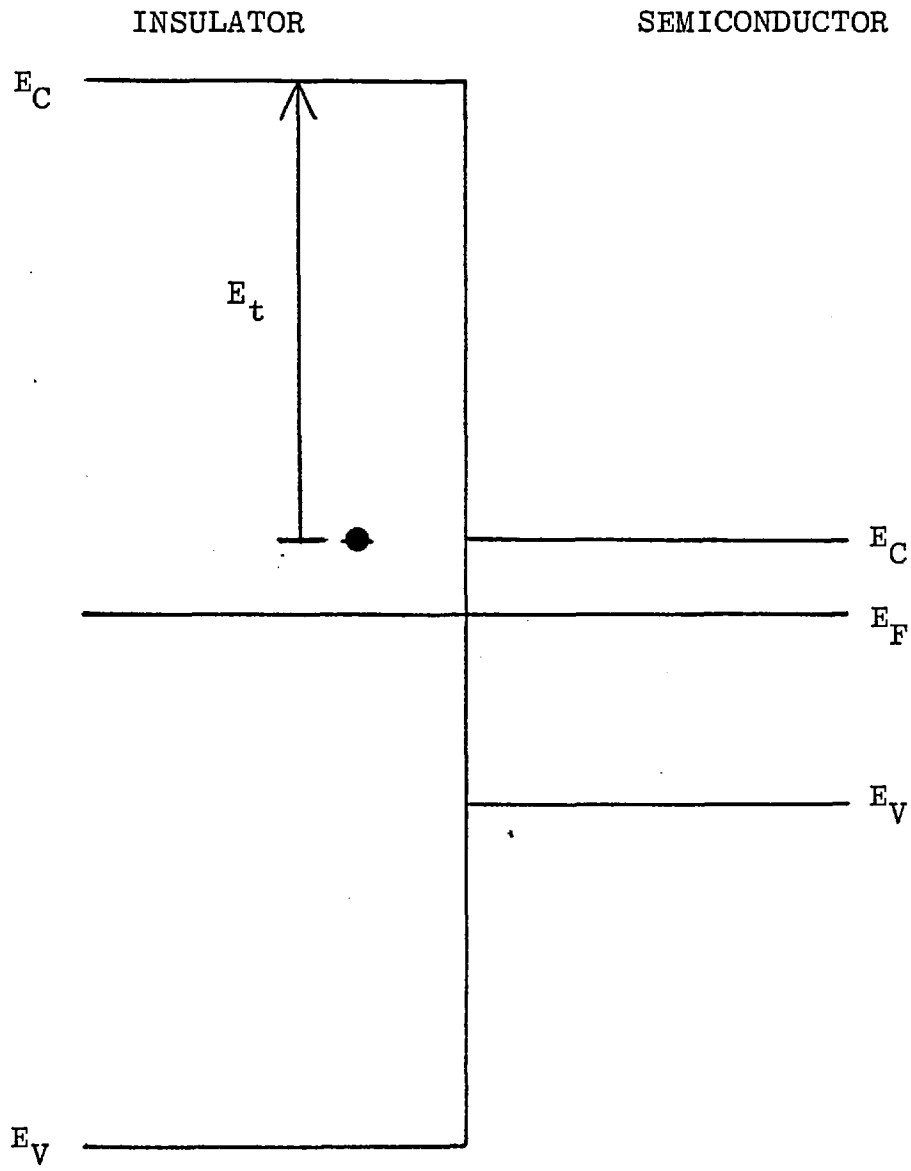


FIG. 5.9 ENERGY LEVELS IN INSULATOR

probability of tunneling out of a trapping state at depth x is given by:

$$P(x) = P_o \exp(-2K_o x)$$

where K_o the wave function decay constant is given by:

$$K_o(x) = \frac{(2m^* E_t)^{\frac{1}{2}}}{h} \left[1 - \frac{Fx}{2E_t}\right] \qquad (5.2)$$

in which F is the electric field in the insulator due to the gate voltage. Typically this will be of the order of 10^8 Vm^{-1} (10 volts across 1000Å). For tunneling, which is a short range process, the distances x will be small, of the order of 10Å. The trap depth E_t will be a few electron volts. Putting these figures into the equation, the field dependent term is found to be negligible.

The time constant for the emptying of filled traps is inversely proportional to the probability of the transition, so that:

$$\tau(x) = \tau_o \exp(2K_o x) \qquad (5.3)$$

and the time dependence of the trapped charge is:

$$n_t(x,t) = n_t(x,o) \exp(-t/\tau(x))$$

where $n_t(x,o)$ is the initial charge distribution. The threshold voltage shift, denoted by $V_T(t)$, is related to the trapped charge by:

$$V_T(t) = \frac{q}{C_o}\left(1 - \frac{\bar{x}}{x_o}\right)\int_o^{x_o} n_t(x,o) \exp(-t/\tau(x))\, dx$$

where $\bar{x}$ is the position of the centroid of the charge distribution and x_o the insulator thickness. For the short range runneling process the centroid is close to the interface, so $\bar{x}$ is much smaller than the insulator thickness x_o.

The variable of integration in the above equation is changed from x to τ using equation 5.3, obtaining

$$V_T(t) = \frac{q}{2C_o K_o} \int_{\tau_o}^{\tau_1} n_t(x,o) \exp(-t/\tau) \frac{d\tau}{\tau}$$

where $\tau_1 = \tau_o \exp(2K_o x_o)$

The initial threshold voltage shift V_{TO} is given by

$$V_{TO} = \frac{q}{C_o} \int_o^{x_o} n_t(x,o)\, dx$$

which, for the low injected charge density of Fig.5.8(ii) under consideration is:

$$V_{TO} = \frac{q}{C_o} N_o d$$

where N_o is the filled trap density and d the depth to which the traps are filled.

The equation for $V_T(t)$ is therefore:

$$V_T(t) = \frac{V_{TO}}{2K_o d} \int_{\tau_o}^{\tau_1} \exp(-t/\tau) \frac{d\tau}{\tau}$$

The integral in this equation is the exponential integral, which is tabulated[6]. Within limitations it may be approximated by a logarithmic function, so that the final

expression obtained for the threshold voltage shift is:

$$V_T(t) = V_{TO}\left[1 - \frac{1}{2K_o d}\ln(t/\tau_o) + 0.577\right] \qquad (5.4)$$

where 0.577 is Euler's constant.

The decay rate r_d as described in equation 5.1 is therefore:

$$r_d = \frac{1.15V_{TO}}{K_o d} \qquad (5.5)$$

so that r_d is proportional to V_{TO} as found experimentally. In conjunction with equation 5.4 measurements of r_d and V_{TO} allow determination of N_o and d, the two quantities which characterise the charge distribution in the insulator, provided that the wave function decay constant K_o is known.

5.2.4 Analysis of Results

The results of the measurements of section 1.2 were analysed in accordance with the theory of the previous section. Equations 5.4 and 5.5 are the relations used for this.

Figure 5.7 is a graph of the measured decay rate plotted against threshold voltage shift. A straight line is drawn through the points as shown. This linear relationship indicates that the trapped charge is much less than the trapping state density, as previously stated. Were this not so, the decay rate would not vary in this way but would be constant, with a value given by the combination of equations 5.4 and 5.5 with N_o replaced by N_T. Essentially this is because as the density of trapped charge becomes equal to the trap density, the

distribution spreads into the insulator rather than increasing at the interface.

To proceed further it is necessary to obtain a value for K_o, the wave function decay constant, given by equation 5.2 with the field dependence neglected for the reasons explained. The two unknown quantities are the electron effective mass in the silicon dioxide, m^*, and the trap depth E_t. The former has been determined for thermally grown silicon dioxide to be $0.4m$[7] and this value is assumed for the sputtered material also.

The measurements described above of trapping as a function of temperature showed the tunneling process to be direct, meaning that the trapping states are situated at the same energy level as the semiconductor conduction band edge, which is approximately 0.1 eV above the Fermi level. If it is assumed that the Fermi level in the SiO_2 is close to the centre of the gap, the trap depth E_t therefore has a value of approximately half the value of the SiO_2 band gap.

Various values are given in the literature for the band gap of silicon dioxide, ranging from 6.2 eV[8] to 10.6 eV[9]. For the purpose of these calculations Motts' value of 10.6 eV is used. With this value K_o is calculated to be:

$$K_o = 1.48 \times 10^{10}\ m^{-1}$$

Using this value of K_o for each measurement the value of N_o is determined using equations 5.4 and 5.5 Using equation 5.5 and the measured values for r_d and V_o the quantity d, the characteristic trapping length, can be calculated.

For the experiment described above, the results obtained are a mean value for d of 6Å and values for N_o, the occupied trap density at the interface, of 4×10^{23} - 2×10^{24} m^{-3} for values of V_{TO} in the range 0.1 - 0.4 volts. It should be emphasised that this is not the density of trapping states in the insulator, but the occupied trap density.

The equation describing the distribution of trapped charge in the insulator was given in Chapter 4 (equation 4.3) and is:

$$n_t(x,t) = \frac{N_T(\exp(SN_i(t)) - 1)}{\exp(SN_i(t)) - 1 + \exp(SN_T x)} \qquad (5.6)$$

where S is the trap capture cross-section, N_T the trap density and $N_i(t)$ the density of charges injected into the insulator. The quantity $n_t(x,t)$ is graphically illustrated in Fig.5.10 for various values of SN_i, that is, for various quantities of injected charge. For n_t/N_T approaching unity the shape of the distribution function approaches that of Fig.5.8(i), while for n_t/N_T much smaller than unity the exponential distribution of Fig.5.8(ii) is obtained.

For the latter situation equation 5.6 may be approximated by:

$$n_t = N_T SN_i \exp(-SN_T x)$$

from which, on comparing with the equation describing Fig.5.8(ii)

$$n_t = N_o \exp(-x/d)$$

the identity can be deduced

$$d = {}^{1}/_{SN_T}$$

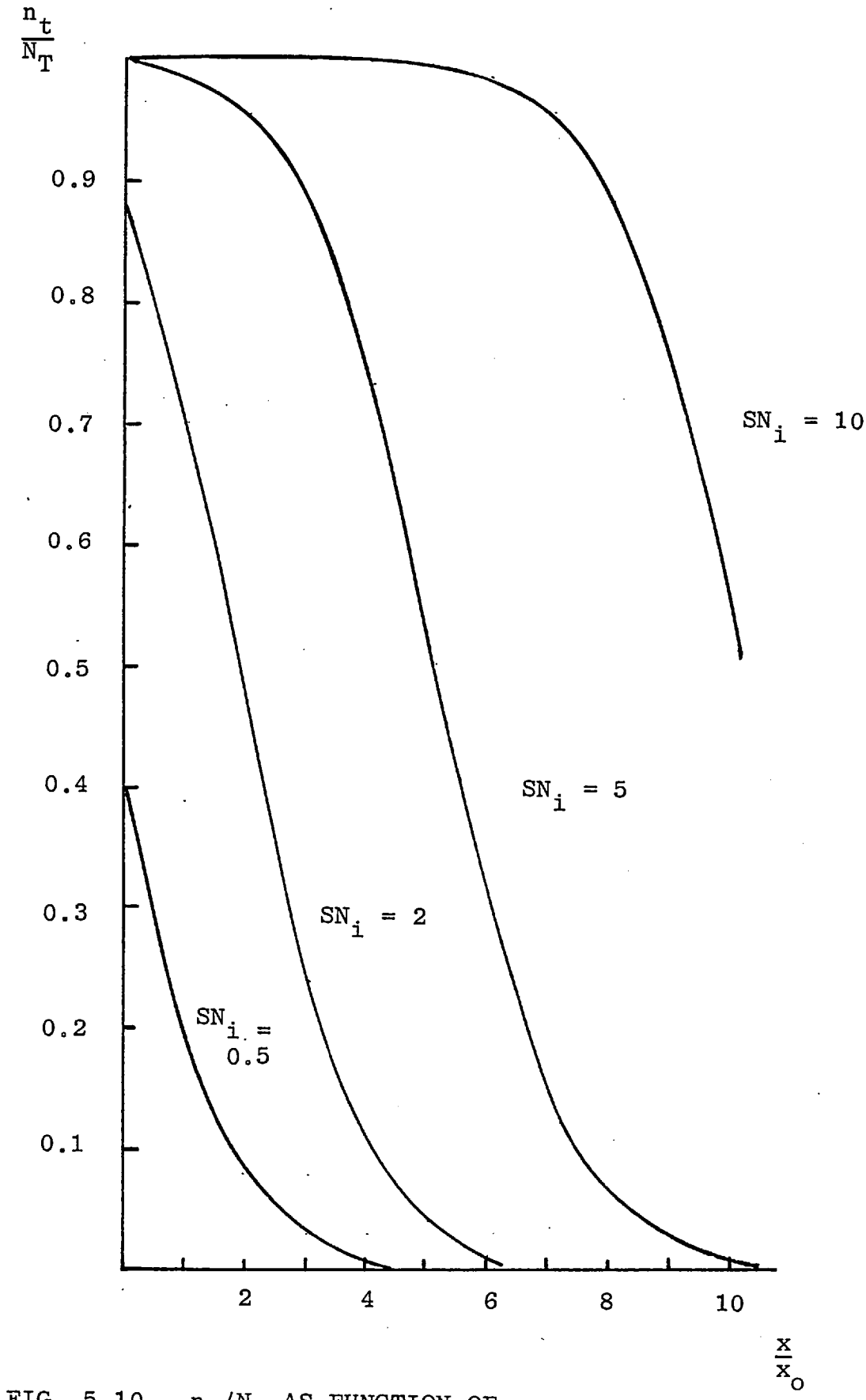


FIG. 5.10 n_t/N_T AS FUNCTION OF x/x_o AND SN_i (Equation 5.6)

The trap capture cross-section has been determined from the measurements of Chapter 4 to be approximately 3×10^{-16} m^2. With the value determined above of 6Å for the distance d, the corresponding trap density N_T can be calculated and is

$$N_T = 5.6 \times 10^{24} m^{-3}$$

This is comparable to or somewhat greater than trapping state densities found in thermal silicon dioxide[14]. In accord with this, the degree of threshold voltage drift in the TFT is somewhat larger than in MOS devices with thermally grown silicon dioxide as the insulator. Reduction of the trap density in the sputtered insulator film by approximately an order of magnitude would bring it within the same range as the thermally grown material. Further work is necessary to investigate the best means of achieving this end.

5.3 NOISE IN THIN FILM TRANSISTORS

All electronic devices are subject to the phenomenon of noise. Noise in this sense means random variations of the current flowing in the device. There are many sources of noise, some common to all devices and some specific to certain types of device. For example, Johnson or thermal noise occurs in all current-carrying devices. This type of noise is caused by the random thermal motion of the charge carriers in a material.

A fundamental characteristic of noise is the spread of frequencies encompassed by it, and the distribution of noise power within the frequency spectrum. Noise caused

by different mechanisms has power spectra of different forms, and may be characterised by the shape of the spectrum. Johnson noise, for example, is independent of frequency - that is, the noise power is constant across the spectrum.

In most electronic devices the noise power is found to increase progressively at low frequencies. This noise is known as flicker noise or, from the shape of the noise power spectrum, $\frac{1}{f}$ noise. It is found in a very wide range of devices - junction and MOS transistors, thermionic devices, cold cathode devices - which have few factors in common. The noise is thought to be a surface phenomenon, although the precise details are still unclear. For such $\frac{1}{f}$ noise, the power spectrum is of the form:

$$P(f) = Cf^{-1} \qquad (5.7)$$

The low frequency noise of TFTs has previously been measured by Anderson[10] and found to follow an approximate $\frac{1}{f}$ law. The noise power was found to increase with higher slow state densities. Measurements of the noise power spectra were made on the present TFTs and are described below:

5.3.1 Measurement of Noise Power

To determine the noise spectrum of a device it is necessary to measure the noise power within a narrow bandwidth about a centre frequency which may be moved to encompass the spectrum of interest. In these measurements this was done by using a wave analyser, the Hewlett-Packard type 3590A/3595A. The noise was measured

in the frequency range 100Hz - 100kHz, these being the effective limits of the equipment. The spectrum was scanned automatically, in three ranges, the sweep rate and bandwidth being adjusted as necessary for each scan.

For these measurements the transistors were connected into the circuit shown in Fig.5.11, in which the device was biased with a positive gate voltage of nine volts. The source-drain voltage was considerably less than this in order to ensure operation on the linear portion of its characteristics. The noise voltage appearing at the drain terminal was measured; this is the drain noise voltage. The noise voltages are given in decibels (dB). The decibel is a logarithmic ratio, the reference level chosen for these measurements being 1 volt r.m.s./$Hz^{\frac{1}{2}}$. Thus the noise voltages given are

$$\text{noise voltage in dB} = 20 \log_{10} \frac{V_{noise}}{V_{ref}}$$

The noise voltage spectra of a small number of TFTs was measured in this way, to determine the main features of the noise spectra.

The form of the spectrum varies considerably between devices, but in all cases the noise voltage decreases with increasing frequency. Some spectra have a constant rate of decrease, when plotted as noise voltage against log f while for others the rate of decrease varies. Two measured spectra are shown in Fig.5.12 in which two straight-line segments are observed. Also shown are lines whose slopes correspond to 1/f and $1/f^2$ respectively, by comparison with which the value of n for the measured

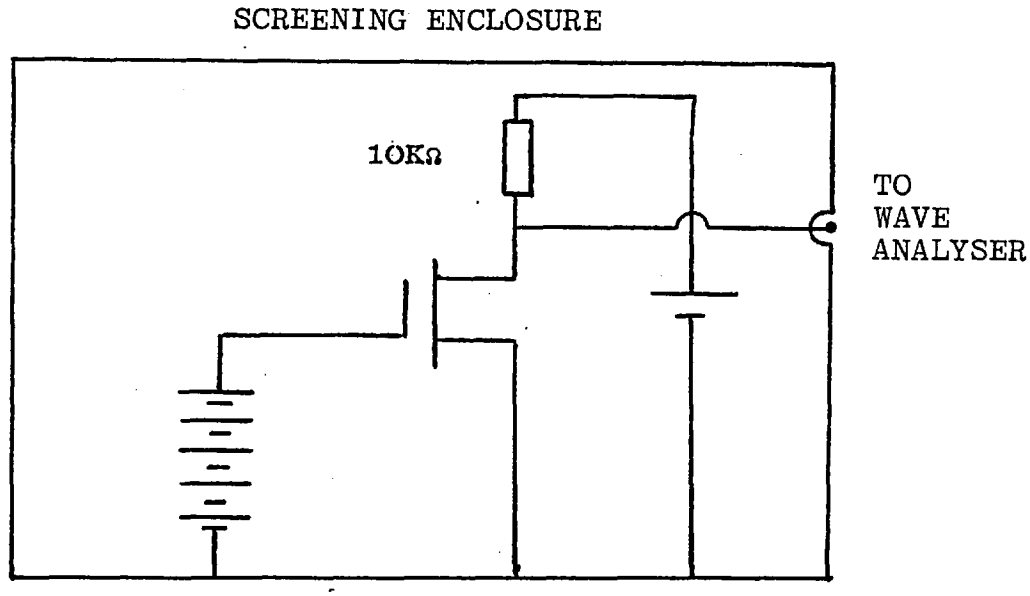


FIG. 5.11 LOW FREQUENCY NOISE MEASUREMENT CIRCUIT

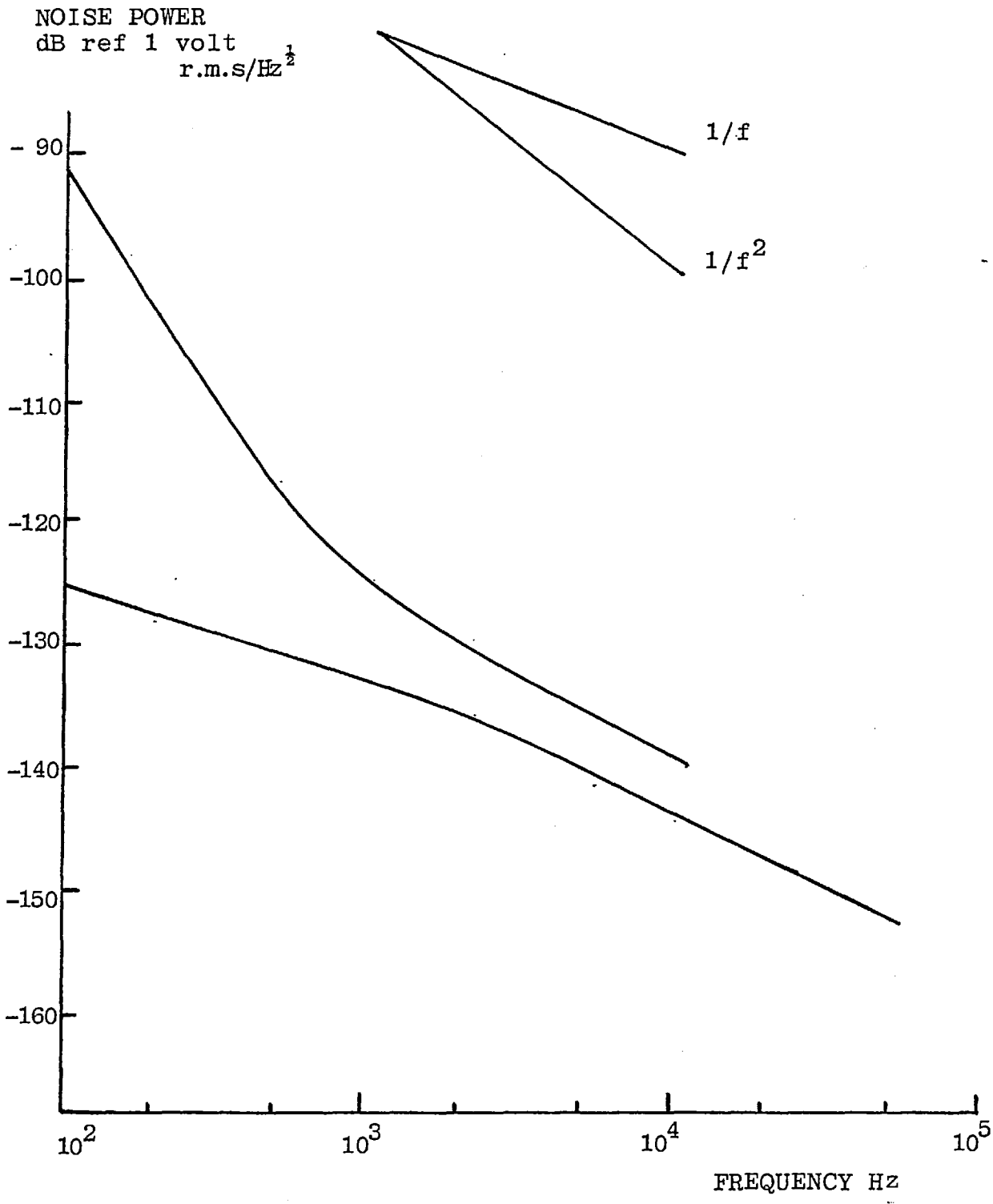


FIG. 5.12 TFT NOISE CHARACTERISTICS

curves is seen to be in the range 1 - 2. It is clear from the considerable variation found that the noise characteristics of the TFTs are not simple, and must depend on many parameters of the devices.

The slow trapping state densities of the transistor for which noise measurements were made were also examined. A correlation between the slow state density and noise voltage is found, a high slow state density device having a higher noise voltage than one with a low slow state density. Measurements on a much larger number of devices, with a wide range of trapping state densities would be needed to determine the exact relation between the two quantities, and the more general one stated is all that can be deduced at present.

5.3.2 Discussion

Much theoretical work has been done on the low frequency noise of MOS devices. To explain $\frac{1}{f}$ noise, a mechanism is necessary which can account for the extremely wide frequency range covered. An explanation, originally proposed by McWhorter[11] and since examined by others, is that the noise is due to fluctuations in the density of carriers immobilised in trapping states. A large spread of trapping time constants is required in order to produce wideband noise. This is ascribed, in the McWhorter model, to the semiconductor charge carriers tunneling to traps located in the insulator layer at the semiconductor surface. For a spatially uniform trap distribution, the model predicts $\frac{1}{f}$ noise. It also

predicts that the noise power will be proportional to the density of trapping states in the insulator.

Fu and Sah[12] proposed a noise mechanism in which the trapping which gives rise to the noise is a two stage process. Charge carriers from the semiconductor conduction band are in thermal equilibrium with localised states positioned at the interface with the insulator, and from those states they tunnel to the trapping states located in the insulator mobility gap. The noise power in this model is again proportional to the insulator trap density. The noise characteristics of silicon MOS devices were found by these authors to fit closely to this model.

The noise in the thin film transistors has been found to follow a $\frac{1}{f}$ law fairly closely in most devices. The noise voltage is a rather complicated quantity to calculate, so that no conclusions can be drawn from the deviations from this behaviour that do occur. It can be stated though that the noise spectra of the device are consistent with a tunneling process for charge trapping causing the noise, and thus with the mechanism invoked to explain the time dependence of the trap charging process causing changes of threshold voltage.

A description of the theories used to explain $\frac{1}{f}$ noise behaviour in MOS devices has not been given; such information is available in the papers cited. It will be shown in the following section however, that the noise characteristics and time dependent trapping behaviour are consistent with one another, and that therefore the same model is sufficient to explain both phenomena.

5.3.3 Relationship between Noise and Time Dependence

The two quantities frequency and time have a reciprocal relationship - processes occuring at low frequencies take a long time, those at high frequencies a short time. Because of this connection, the time-dependent behaviour of a system may be obtained, in principle at least, from its frequency dependent behaviour, and vice versa. The connection between the two is the Fourier transform, equations which relate the time-domain and frequency-domain responses of a system. The Fourier transform equations are of the form:

$$g(w) = \int G(t)\, e^{-jwt} dt$$

$$G(t) = \int g(w)\, e^{jwt} dw$$

There are alternative definitions sometimes used, differing from these by a constant factor of 2π. For the purpose required the above definitions will be used as they are the simplest. In these equations G(t) is the time-dependent system response, and g(w) the corresponding frequency response, w being the angular frequency.

A process of tunneling to insulator traps has been seen to result in a logarithmic time dependence for the charge trapping process, while the measured noise voltage has been found to follow a $\frac{1}{f}$ law. It can be shown that a $\frac{1}{f}$ frequency response is equivalent to a log (time) dependence by means of a Fourier transform.

It is assumed that the traps which cause changes in threshold voltage in the time domain also cause noise in the frequency domain, by random fluctuations in the density of trapped charges modulating the drain current. The frequency domain transfer function, assuming $\frac{1}{f}$ behaviour of the noise, is:

$$g(w) = \frac{A}{w}$$

so that the time domain transfer function is:

$$G(t) = A \int \exp(jwt) \frac{dw}{w}$$

by changing the variable of integration from w to τ, where:

$$w = \frac{1}{\tau}$$

the equation becomes:

$$G(t) = -A \int \exp(j\frac{t}{\tau}) \frac{d\tau}{\tau}$$

which has the form of the exponential integral, previously found in the analysis of the time dependence of trapping (Section 5.2.3).

The mathematical limits of integration are to be replaced by physically determined limits. The lower limit is determined by the consideration that the shortest time constant is the fundamental trap time constant τ_o. The longest time constant corresponds to that of traps at the gate-insulator interface, remote from the semiconductor,

for which the time constant is:

$$\tau_1 = \tau_o \exp(Kx_o)$$

Inserting these limits an equation is obtained which has the same form as that obtained in Section 5.2.3, equation 5.4. The result of the integration is:

$$G(t) = -A \ln\left(\frac{t}{\tau_o}\right)$$

This shows that any mechanism which results in a logarithmic time dependence also results in a $\frac{1}{f}$ frequency response. It also means that the two measurements give the same information, although one or the other may be preferred for various reasons. For example, very low frequency measurements are difficult, so measurements at long times may be used.

This is of relevance to the measurements done on the TFTs. The time measurements were carried out between 1 second and greater than 10^4 seconds, whereas the noise measurements were performed for frequencies of 10^2 - 10^5Hz, the corresponding times being 10^{-2} to 10^{-5} seconds, over which an approximate $\frac{1}{f}$ law is followed. Thus the same trap mechanism would appear to be operating at 10^4 seconds and 10^{-5} seconds, a wide range of nine orders of magnitude.

Few charge trapping mechanisms other than tunneling can result in such a wide range of time constants for the trapping process.

5.4 EXPERIMENTS WITH ALTERNATIVE INSULATOR

A set of experiments was done on devices with a different insulator. The material used was yttrium oxide, Y_2O_3. The dielectric constant of this material is greater than that of silicon dioxide, the measured value being $10 \pm .2$ compared with a value of 4 for SiO_2. The increased dielectric constant should produce an immediate improvement in the gain of the thin film transistors, all other factors being unchanged, because it means that more charge is transferred to the semiconductor for a given gate voltage. This is the reason for the interest in using higher dielectric constant materials for the insulator. The trapping behaviour of devices with a Y_2O_3 insulator was investigated and compared with that found in silicon dioxide devices.

The yttrium oxide was deposited by r.f. sputtering in a 95% argon - 5% oxygen gas mixture at a power level of 7.5 watts/cm^2. It was necessary to sputter the insulator in a different vacuum plant to the one used for the manufacture of the transistors. This meant that a vacuum break occurred before and after the deposition of the insulator film, while the substrate was transferred from one system to the other. This will have caused the formation of a layer of adsorbed gas at the semiconductor-insulator interface which would be expected to cause a degradation in the properties of the transistor. Before making any transistors, the yttrium oxide was first made into metal-insulator-metal capacitors, using evaporated

aluminium electrodes to check that a good insulator film was produced, and to measure the dielectric constant.

After fabrication of the transistors, they were annealed at 380°C for 1½ hours in a dry nitrogen ambient, the same treatment as given to the standard silicon dioxide devices; it was not attempted to determine whether this is the optimum anneal for transistors with Y_2O_3 as the insulator. After anneal, the transistors were found to work, although the full improvement in performance indicated above was not found. This is probably due to the formation of an interfacial layer between insulator and semiconductor.

5.4.1 Measurement of Trap Cross-section

The capture cross-section of the trapping states was measured in the same way as described for the silicon dioxide devices in Chapter 4. The results were calculated in the same way, allowance being made for the different value of dielectric constant. The results are fitted by a value for the capture cross-section of $2 \pm 1 \times 10^{-16} m^2$. This value is, within experimental error, the same as that found for the capture cross-section in the silicon dioxide insulator.

The trapping state density was higher than that found in the silicon dioxide insulator of the standard devices. This is almost certainly because the material was sputtered in a different vacuum system to the silicon dioxide. The sputtering conditions used were those which were found to produce a good quality insulator, but may not be the

optimum to produce material with a low trapping state density. It is likely that further work would enable the trap density to be reduced further.

The fact that the capture cross-sections of the trapping states in the two materials are so similar suggests that they may be caused by the same species. It is therefore necessary to consider what trapping species may be common to both the insulator materials Y_2O_3 and SiO_2.

The trapping species may be either extrinsic or intrinsic, that is, either a foreign impurity atom present in the material, or a defect of some kind in the material. In the former case it is of course perfectly possible for the same impurity to be present in the two materials and cause the trapping, while in the second a species must be found which can occur in both of the materials.

One possible extrinsic trapping state is a water molecule. This has been found to be capable of charge trapping in SiO_2, but with a capture cross-section much smaller than that found here, of order $10^{-22} m^2$.[13] Another possibility is a sodium ion, which was the species to which Ning and Yu[14] ascribed the traps found in SiO_2 with a capture cross-section of approximately $3 \times 10^{-17} m^2$, similar to that found here. Drift of mobile sodium ions has not been found to occur in these thin film transistors (Section 5.2), so that if sodium ions are the cause of the trapping states then they must be immobilised. Fowkes and Burgess[15] suggest that sodium ions can be localised

in oxygen deficient silicon dioxide when electrons are trapped at oxygen vacancies. In this case, the sodium ions would be de-trapped, i.e. become mobile once more, when the electrons are released from their trapping sites. Drift of the sodium ions would then be expected; as has been stated, no such drift has been observed.

An intrinsic trapping state common to the two materials SiO_2 and Y_2O_3 would be one connected with the oxygen atom which is present in both materials. One possibility is an oxygen vacancy. It is known that r.f. sputtered silicon dioxide is oxygen deficient[16], and the same is almost certainly true of yttrium oxide. Indeed, when suitable sputtering conditions for Y_2O_3 were being investigated, it was found that the loss factor of the material was greater when sputtered in gettered argon i.e. argon with a very low oxygen concentration, than when sputtered in an argon-oxygen mixture, and the same effect was found to occur in silicon dioxide. These observations suggest that oxygen vacancies in the insulator are electrically active and able to capture and release charge. Oxygen vacancies in these materials would be positively charged, that is they would be acceptor states. The observed capture cross-sections, characteristic of an attractive potential trap, are therefore consistent with the trapping sites being due to oxygen vacancies.

5.4.2 Threshold Voltage Time Dependence

The variation of the threshold voltage of yttrium oxide TFTs with time, as trapping occurred, was measured

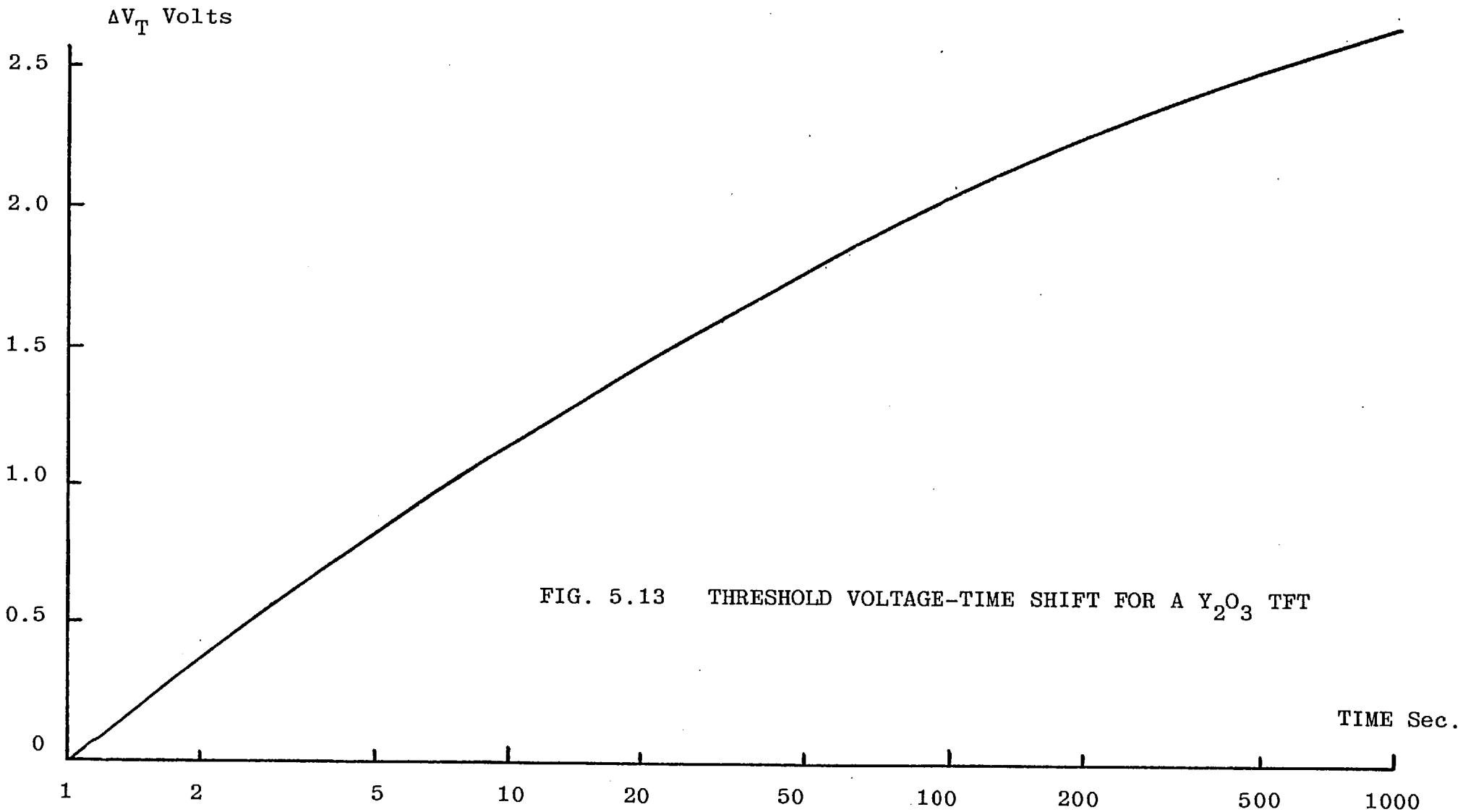


FIG. 5.13 THRESHOLD VOLTAGE-TIME SHIFT FOR A Y_2O_3 TFT

in exactly the same way as for the silicon dioxide devices. The result of such a measurement is shown in Fig.5.13. The result of the measurement is similar to that of the silicon dioxide devices, having the same approximate log time dependence. The actual amount of the drift is rather large, due to the somewhat higher trapping state density in this material as compared with the SiO_2.

This result means that the same process of tunneling to insulator traps occurs in yttrium oxide as in silicon dioxide. There is a slight curvature of the graph of Fig.5.13 the threshold voltage dropping below the expected value, which may be due to a small reduction of the trap density further into the insulator. Ion drift can be ruled out as a major factor in the drift of threshold voltage of these devices, as was found to be the case for the SiO_2 devices.

5.5 INFRA-RED ABSORPTION ANALYSIS OF DIELECTRIC

Measurements of infra-red absorption spectra have been much used for analysis of thermally grown silicon dioxide on silicon, and silica-based glasses. Information can be obtained about the stoichiometry of the material, and certain impurities such as water. Reviews of such measurements are given by Pliskin.[17] [18]

The absorption spectra of r.f. sputtered SiO_2 films, such as are used in the TFT, have been measured previously.[16] The spectra of the material used in the thin-film transistors was measured and the results are described in the following sections.

Much work has been done on thermally oxidised silicon. Such material has various absorption bands in its spectrum. Each absorption is caused by the excitation of a particular vibration mode (e.g. stretching, bending) in a molecular bond. Each bond has several vibration modes, and each mode a different resonance frequency, so the absorption spectrum of a material will generally have many bands. The relative strength of the absorption is a measure of the number of the particular molecular bonds present in the material.

The vibration frequency of each mode is slightly affected by the local field due to the other atoms surrounding it. An important effect of this is to make the exact resonance frequency of each absorption depend slightly on the overall stoichiometry of the material. Care is necessary however in interpreting changes in wavelength of absorption bands as being due to variation of stoichiometry, because other factors such as porosity and strain in the film cause similar effects. According to Pliskin[17], porosity and bond strain cause two of the SiO_2 absorption bands to shift in opposite directions respectively, whereas composition differences cause a movement in the same direction for each band.

The main absorption bands in thermal silicon dioxide occur at wave numbers of approximately 1080 cm^{-1} and 450 cm^{-1}. The positions of these bands in the infra-red absorption spectra of various silicon oxides are given by Cachard et al[19] and reproduced in Table 5.1. The variation of the wavenumber of each band with variation

T A B L E 5.1

Material	SiO	$SiO_{1.5}$	SiO_2
Si-O stretch	$960cm^{-1}$	$1020cm^{-1}$	$1085cm^{-1}$
Si-Si stretch		$790cm^{-1}$	$800cm^{-1}$
	$770-625cm^{-1}$	$770-625cm^{-1}$	
		$880cm^{-1}$	
Si-O bend	$500-330cm^{-1}$	$385cm^{-1}$	$450cm^{-1}$
		$500-330cm^{-1}$	

of oxygen content of the material is seen to be quite significant. Also noted in the table are the vibration modes to which each absorption is ascribed.

These absorption bands are intrinsic to the material, that is, they are caused by excitation of the molecular bonds present naturally in the material. However, additional absorption bands can be caused by extrinsic species incorporated into the structure of the material. Of possible importance in this context are water, which causes an absorption band at 3330cm^{-1} and the silanol group (Si-OH) which has an absorption band at 3650cm^{-1}. The presence of water may therefore be detected by the presence of these absorption bands.

5.5.1 Experimental Method

The absorption spectra of the sputtered films were measured by the technique of reflection absorption spectrometry by Mr. R. Chater of the Analytical Services Laboratory at Imperial College. It was not possible to measure the absorption of the films on the standard substrates on which the thin film transistors were made, because the refractive indices of the film and the glass substrate are too similar. For these measurements therefore, films were sputtered onto a different substrate.

The substrates used were single crystal silicon wafers 0.5mm thick, 2 ohm-cm doped n-type. The silicon dioxide was sputtered in the plant used for the manufacture of the thin film transistors, to a thickness of 5000Å. Apart from a longer sputtering time to obtain the increased

film thickness, the conditions used were the same as for the deposition of the dielectric layer of the thin film transistors.

Several sputtering runs were done, films from each being examined. The vacuum system base pressure before sputtering was not the same for each run, which may have resulted in varying degrees of impurity content of the sputtering gas mixture. After deposition the substrates were scribed and broken into approximate 1cm squares for the measurements.

No significant differences were found between the absorption spectra of the films made during different sputtering runs. For convenience therefore, the result of a single measurement only will be described and discussed. One of the absorption spectra is shown in Fig.5.14. In order to display it in reasonable detail it is split into sections. The transmittance is plotted on a linear scale from zero to 100%, so that absorption bands appear as downward dips in the plot. The abscissa is linear in wavenumber (reciprocal wavelength) and the corresponding wavelength is also shown.

The strongest absorption band is seen to occur at $1070cm^{-1}$, no absorption bands being found at greater wavenumbers, between $4000cm^{-1}$ and 1070^{-1}. The next absorption band is found at $810cm^{-1}$ - this band is much weaker than the first. A further weak absorption occurs at $740cm^{-1}$. Two further bands are seen at $610cm^{-1}$ and $440cm^{-1}$.

Absorption spectra were also measured on films which had been annealed, and on films which had been subjected

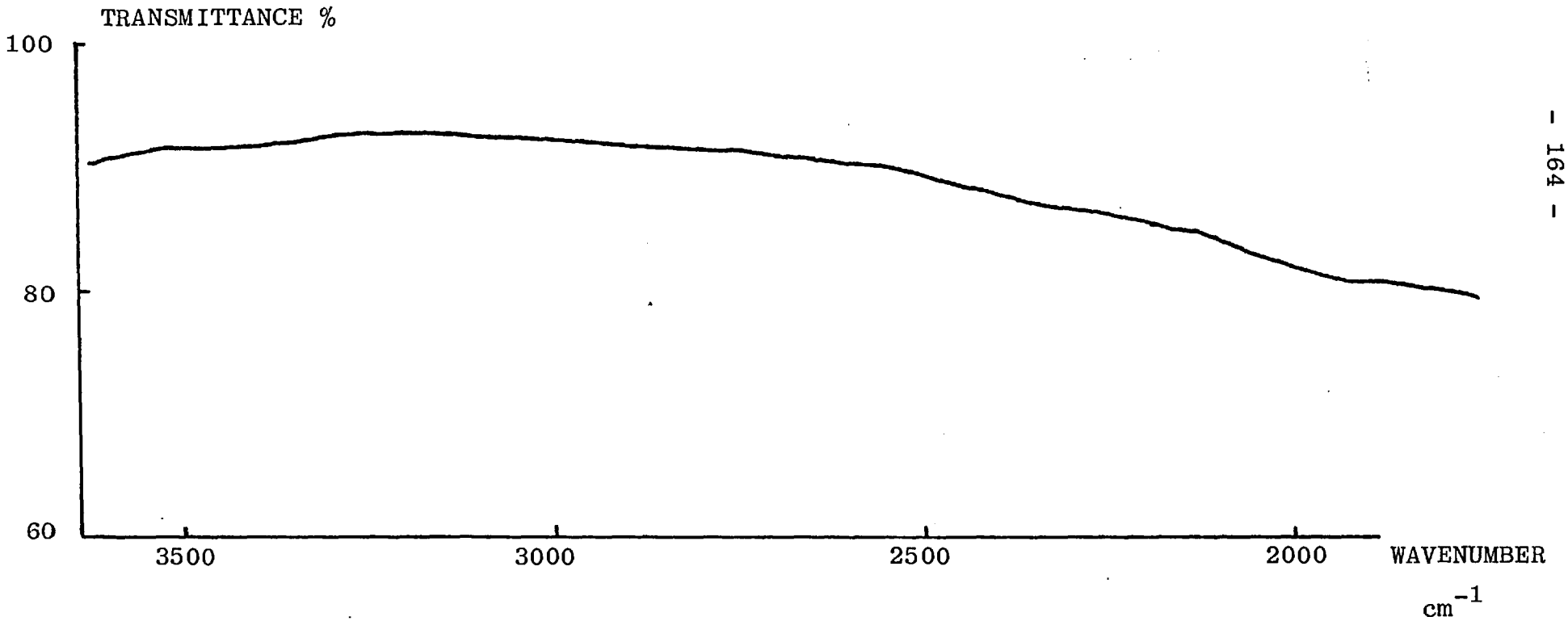
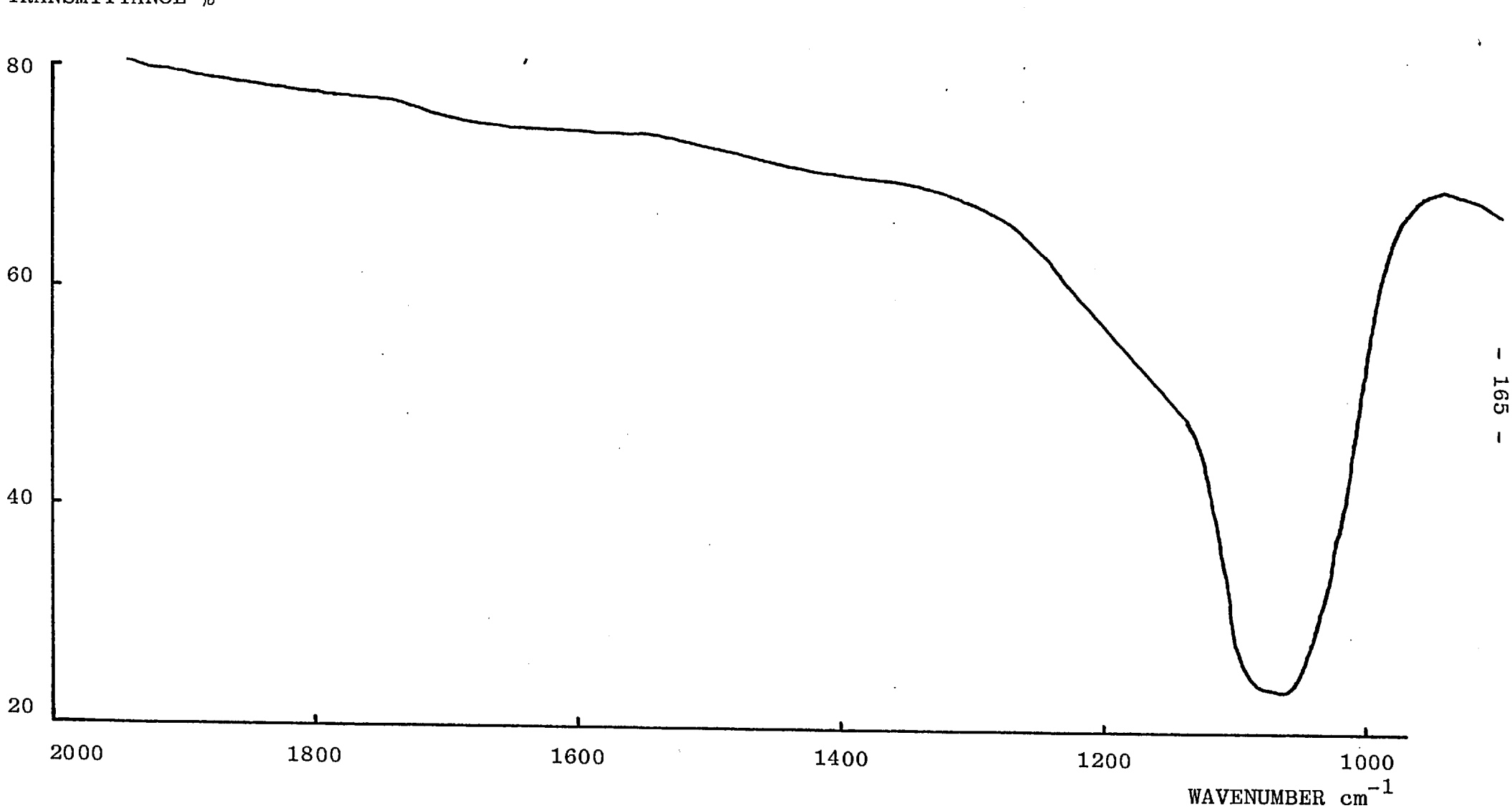
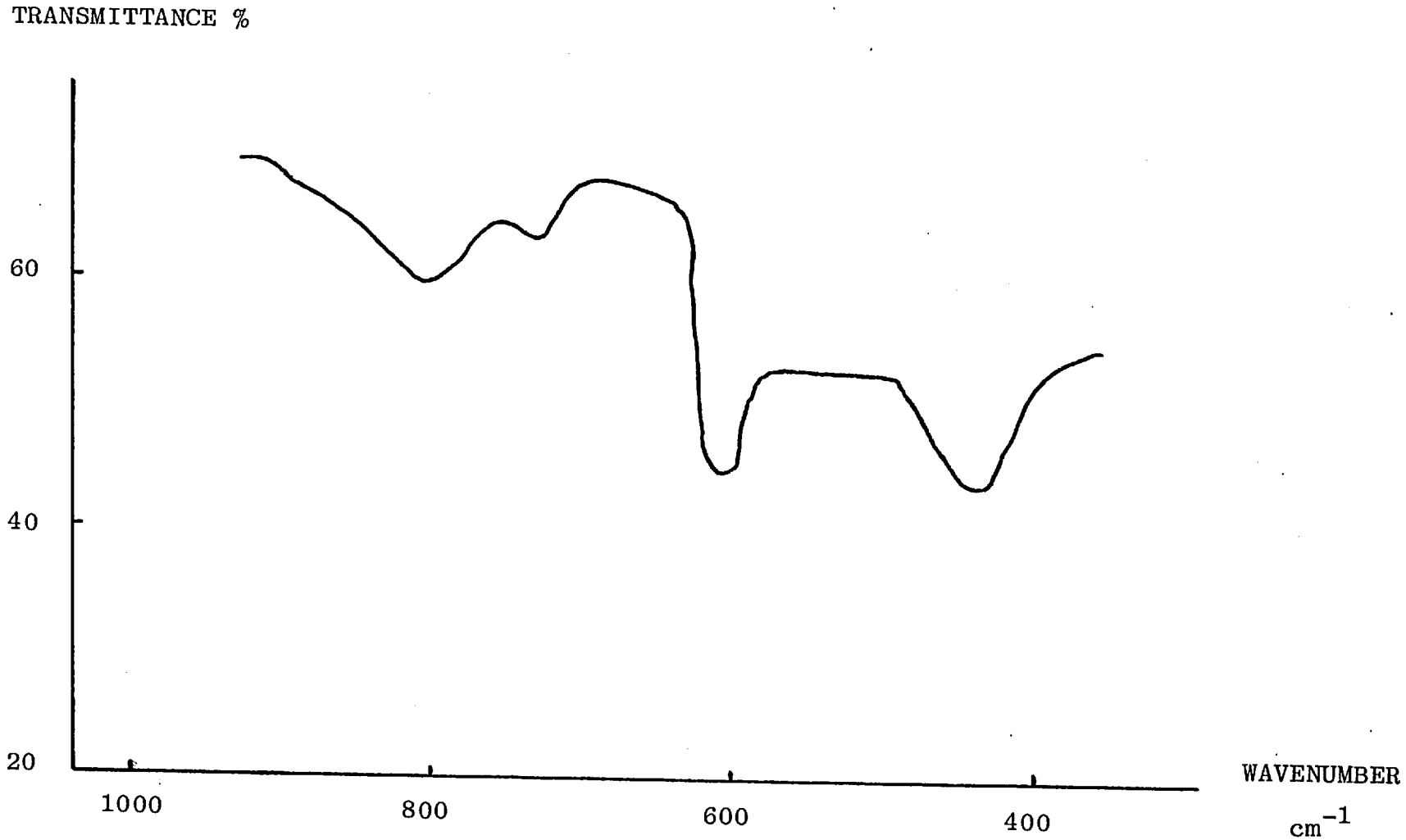


FIG. 5.14 SiO_2 INFRARED ABSORPTION SPECTRUM


TRANSMITTANCE %
80
60
40
20
2000
1800
1600
1400
1200
1000
WAVENUMBER cm-1


TRANSMITTANCE %
60
40
20
1000
800
600
400
WAVENUMBER
cm-1

to immersion in hot water. Some of these latter films were also annealed and then measured.

The anneal used in each case was at a temperature of 380°C for 1¼ hours in flowing nitrogen, as used for the thin film transistors. The water treatment consisted of immersion in hot distilled water at a temperature of approximately 85°C for 24 hours. Before measurement or anneal, the surface moisture was allowed to dry.

These measurements were done by a differential measurement technique, in which the difference in absorption of two samples is measured. By this means small differences in the spectra of the two films are amplified and may be more easily seen than by comparing the standard absorption spectra of the two films. For the reference film an untreated sample, from the same sputtering run as the treated sample, was used.

No significant differences were found in absorption spectra of the reference and treated samples in each case over the whole of the measured spectrum, from 200 - 4000cm^{-1}.

5.5.2 Discussion

The positions of the absorption bands in the infra-red absorption spectrum of the sputtered silicon dioxide films may be compared with the data given in Table 5.1. The three bands at 1100cm^{-1}, 800cm^{-1} and 450cm^{-1} may be distinguished in the measured spectra, with additional bands at 740cm^{-1} and 610cm^{-1}.

The bands at 740cm^{-1} and 610cm^{-1} are not present in stoichiometric SiO_2 but only in the oxygen-deficient forms,

and are related to the bond strain induced by the composition changes. No absorption band is seen at 835cm^{-1} which is the characteristic position of Si - N bands. This indicates that there is very little nitrogen incorporated into the film which, as explained earlier, would introduce additional trapping centres.

The strongest absorption in the measured spectra is found to be at 1070 $\pm$ 5cm^{-1} and can be identified with the Si-O stretch mode vibration. The position of this band is in between its positions for SiO_2 and $SiO_{1.5}$ given in Table 5.1.

The value of 1070cm^{-1} for the Si-O absorption band may be compared with that given in ref. 16 for r.f. sputtered material, where for a deposition temperature of 100^{o}C the band is positioned at 1057cm^{-1}, for 400^{o}C at 1071cm^{-1}, and the value for thermal SiO_2 is 1087cm^{-1} (20)

The 440cm^{-1} absorption feature in the spectrum is identified with the Si-O stretching mode resonance of Table 5.1 and is also at a frequency between those for the two compositions SiO_2 and $SiO_{1.5}$.

The positions of these two bands indicate that the material is oxygen deficient silicon dioxide. Assuming a linear relation between absorption band wavelength and oxygen content(21), as is seen to be the case for the 1100cm^{-1} band in Table 5.1 for the three material compositions considered, the oxygen deficiency of the material can be estimated.

As noted earlier, bond strain and porosity of the material also cause such changes in the position of the

absorption bands. It is not possible to say for certain therefore that the cause is a deficiency of oxygen. Measurements of the material's density would be needed, for example, to determine porosity. Previous work by Pliskin has, however, shown r.f. sputtered material to be oxygen deficient. Actually, of course, the three factors (oxygen deficiency, porosity, bond strain) are not independent of one another. Oxygen deficiency causes strain in the inter-atomic bonds by disturbance of the lattice structure for example. Equally porosity introduces bond strain and vice versa. Bearing these caveats in mind, the oxygen content is determined.

The figure obtained for the oxygen content of the material from the position of the absorption band is a deficiency of approximately 6% when compared with pure silicon dioxide (i.e. the material has a composition of $SiO_{1.94}$). In studies of r.f. sputtered SiO_2 Pliskin found oxygen deficiencies of somewhat less than this for material deposited at elevated temperatures, with an increasing deficiency as the deposition temperature was reduced. For a temperature of 50°C the deficiency was 2½% and for 400°C less than 1%. The figure obtained for the present material, which was deposited on an unheated substrate, does not therefore seem unreasonable.

Examination of the high frequency region of the spectrum shows that there are no absorption bands present in the 3330cm^{-1} and 3650cm^{-1} positions characteristic of water and silanol respectively. Indeed no absorption

bands appear above the 1070cm^{-1} SiO_2 band. This indicates that water is not present in significant quanties in the sputtered films.

Since the spectra of films which had been immersed in water for some time prior to measurement were indistinguishable from those of the as-sputtered films, it follows that significant quantities of water are not absorbed by the material. This is in contrast to the usual behaviour of low temperature deposited SiO_2 films, which generally absorb sufficient water to give easily discernible absorption bands in the infra-red spectra[18]. In studies of r.f. sputtered silicon dioxide Pliskin found that for a film deposited at a substrate temperature of 100°C, exposure to a high humidity ambient caused absorption bands at 3650cm^{-1} and 3400cm^{-1}. For a film deposited at 450°C, on the other hand, no such absorption of water occurred. In this respect the present material is closer in properties to the high than to the low temperature deposited material.

This lack of water absorption shows that the material is not very porous, and in this respect at least is similar to thermally grown material. Such a small degree of porosity suggests that the structure is largely "closed-up" with few large holes. This is probably a result of the low deposition rate (1000Å/hr) which allows time for the deposited atoms to attain their most favourable position before being overlaid by a further layer of material.

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CHAPTER 6 DISCUSSION AND CONCLUSIONS

6.1 INTRODUCTION

In previous chapters two important properties of the trapping states present in the insulator film of a TFT have been determined. These are the trap capture cross-section and the trap density. The value of the former is of the order of 10^{-16} m^2 and the latter 10^{24} m^{-3}. Having determined these parameters it is in order to consider the possible nature and origin of the trapping states.

As stated earlier this value of capture cross-section is consistent with the trapping species being a Coulombic attractive potential type of trap. If this is the case the trapping species is a positively charged centre, which exerts an attractive force on an electron, and localises it.

Trapping states in SiO_2 have many possible origins, but they may broadly be divided into two classes - structural defect states, and impurity-related states. The former are defects in the structure of the material which introduce localised trapping states into the band gap of the insulator. Such entities as oxygen and silicon vacancies, excess silicon, strained inter-atomic bonds, broken ("dangling") bonds and displaced atoms fall into this category.

The second group consists of foreign atoms or ions incorporated into the structure of the silicon dioxide. Important impurities which have been identified in silicon dioxide are sodium ions and water-related trapping centres.

One important group of structural defect states in silicon dioxide are those which appear on exposure of the material to radiation. These are discussed in the next section, which is followed by a section on impurity states.

6.2 STRUCTURAL DEFECTS

Many investigations have been made of the nature and properties of trapping states in silicon dioxide - almost exclusively in thermal silicon dioxide because of its technological importance. Many defect states which are known in SiO_2 appear on exposure of the material to radiation such as neutrons, electrons and X or gamma radiation. These damage states can change the electrical and optical properties of the material, sometimes quite drastically. The positions of these defect states in the silicon dioxide bandgap, and their other characteristics, have been determined. Amongst these are the B_2 band which appears at an energy level of 5.1 eV above the valence band edge, the E_1' band at 5.8 eV, the D band at 7.2 eV, and the E band located at 7.6 eV[1]. These energy levels are fairly deep in the band gap of the silicon dioxide, which is approximately 11eV, and so are located in the region of the band gap where the trapping states are presumed to exist, that is, close in energy to the semiconductor conduction band edge. Defect states of this kind are therefore plausible candidates for the trapping centres which cause the slow trapping effects in thin film transistors.

The insulator material in these devices is radio frequency sputtered - that is, it is deposited by bombardment of the surface of a quartz target by energetic atoms and ions through placing the target in a plasma, the plasma being initiated and sustained by a high frequency excitation potential. The plasma is a high radiation environment, so that the growing film is constantly bombarded as it is deposited by high velocity ions and electrons, high energy

neutral atoms, and X-ray and ultraviolet photons. The sputtered film would therefore be expected to contain defects of the type produced in initially defect-free material by irradiation.

Defect states in r.f. sputtered SiO_2 have been investigated by Hickmott[2]. The optical absorption bands which are present in the sputtered material were found to correlate with those present in irradiated thermal oxide, a number of which are listed above.

The electron-spin-resonance (ESR) spectra of these materials showed structures corresponding to those in the optical absorption spectra. The ESR spectra corresponding to the E_1' optical absorption band was found to correlate in density with the depth of the absorption band, and it was suggested, on the basis of the ESR data, that the E_1' centre is due to an electron trapped at an oxygen vacancy in the structure of the material[3] [4].

Hickmott has studied the behaviour of the E_1' band upon annealing, and found that the manner in which the surface states in a MOS device changed upon anneal was similar to that of the defect states, and on this basis a possible connection between the defect states and surface states has been suggested.

The positive charge centres at the silicon-silicon dioxide interface have been studied by Fowkes and Hess who found that oxidation-reduction treatments changed the density of these charge centres[5]. From these results, they suggested a relationship between the positive charge centres and oxygen vacancies in the silicon dioxide material.

Oxygen vacancies in SiO_2 can be either electron acceptor states or donor states, because silicon is amphoteric[6]. If oxygen vacancies are electron traps they can therefore be either attractive or repulsive potential traps, that is, they would be expected to have either a large ($10^{-16}m^2$) or a small (less than $10^{-22}m^2$) capture cross-section.

6.3 IMPURITY DEFECTS

Certain ions are known to form electron trapping centres in silicon dioxide, and these must also be considered as possible candidates for the trapping states in the TFT insulator. This does not mean mobile ions which drift under the influence of applied fields but charged impurities, fixed in the silicon dioxide structure, which can capture charge. Obviously any atom can be present as an impurity, but some are considerably more important than others. If the impurity atom has a different number of valence electrons than are necessary to satisfy the surrounding atomic bonds, then either a negative or positive charge will remain. This is the process that in a semiconductor leads to substitutional doping, making the material either n or p- type. Then the excess charge is loosely bound to the central atom core, so that its energy level is close to the conduction or valence band respectively, the charge is readily ionised and becomes free to move about in the crystal. If the excess charge is more tightly bound, that is to say if the energy level of the atom lies deep in the forbidden gap, then a recombination or trapping centre is formed. Similarly in an insulator, which can be regarded as a very

wide bandgap semiconductor, trapping states located deep in the forbidden gap can be introduced.

In the case of silicon dioxide, several species are known or suspected to form trapping states. Water is known to form trapping states in silicon dioxide which have been investigated by several workers[7] [8]. These have been found to have had very small capture cross-sections, for example a value of 2.4×10^{-23} m^2 was obtained by Ning and Yu[9]. This is characteristic of a neutral trap and is very much smaller than that found in the TFTs. In view of this result therefore water-related traps can be discounted as the cause of the slow trapping effects in the insulator of the TFT.

In the deposition and subsequent annealing treatment of the thin film transistors, great care is taken to exclude water vapour at each stage.

Tungsten (W) in silicon dioxide was found by Young et al[10] to form a trapping state with a capture cross-section of $10^{-19} m^2$.

Traps with a capture cross-section of $3 \times 10^{-17} m^2$ were suggested by Ning and Yu[9] to be the same sodium related states found by Feigl et al[11]. This is interesting inasmuch as it is within an order of magnitude of the capture cross-section measured in the thin film transistors.

These sodium-related centres do not mean mobile sodium ions of the type discussed earlier (Chapter 5) and investigated by Snow et al[12], and which it was seen are not significant in the behaviour of these thin film transistors. Rather these are sodium ions immobile in the silicon dioxide lattice which can trap electrons.

The lack of positive ion drift found in these devices is in fact rather surprising inasmuch as considerable effort is usually necessary when working with thermal silicon dioxide to reduce the concentration of sodium ions to a level sufficiently low that their effects are negligible. The sputtered films were deposited in a vacuum system under clean laboratory conditions, but these were by no means so rigorous as those usually found necessary to eliminate sodium. It is therefore somewhat surprising that no evidence of mobile ion drift has been found. A possible explanation is that any sodium which may be present in the material is somehow immobilised.

Fowkes and Burgess suggest that sodium is immobilised at oxygen vacancies in the structure of silicon dioxide[13]. As was seen from the results of the infra-red absorption spectra measurements on the sputtered material, it is oxygen deficient to some extent. There will be a high density of oxygen vacancies, just the conditions said by Fowkes and Hess to immobilise any sodium which is present.

6.4 DISCUSSION

Having reviewed the trapping states which may occur in silicon dioxide dielectrics an attempt can be made at a more certain identification of the species causing the slow state trapping in the thin film transistors. In the preceding two sections various possible trapping centres have been introduced and some of their properties discussed. Of the possible trapping states in the material the most likely candidates would appear to be either immobile sodium ions or oxygen vacancies. Both of these would be expected

to have capture cross-sections of the same order of magnitude as those observed, and also to be present in the material, the former because sodium is an omnipresent environmental contaminant, the latter because the r.f. sputtered material is oxygen deficient.

The oxygen vacancy is considered to be more likely to be the cause of the trapping states in the present devices. In the measurements of Chapter 5 it was seen that electrons from the semiconductor conduction band communicated with trapping states in the insulator by a quantum mechanical tunnelling process, with no thermally assisted step being apparent in the process. This means that the electrons are tunnelling to traps close in energy to the conduction band edge.

In Section 2 of this chapter it was seen that there are many defects present in sputtered silicon dioxide films and that one in particular, the E_1' has been found to have an ESR spectrum suggesting that it consists of an oxygen vacancy containing a trapped electron. The energy level of this defect is given as 5.8 eV above the SiO_2 valence band edge.

Sodium related trapping centres in SiO_2 have been examined by Di Maria et al who have determined their energy level as being 2.4 eV below the conduction band edge of the silicon dioxide. The energy levels of some of the defect states mentioned are shown in Fig. 6.1. In drawing up a diagram of this kind it is of course necessary to know the value of the band gap of the silicon dioxide. As stated previously this is uncertain, various values being given by

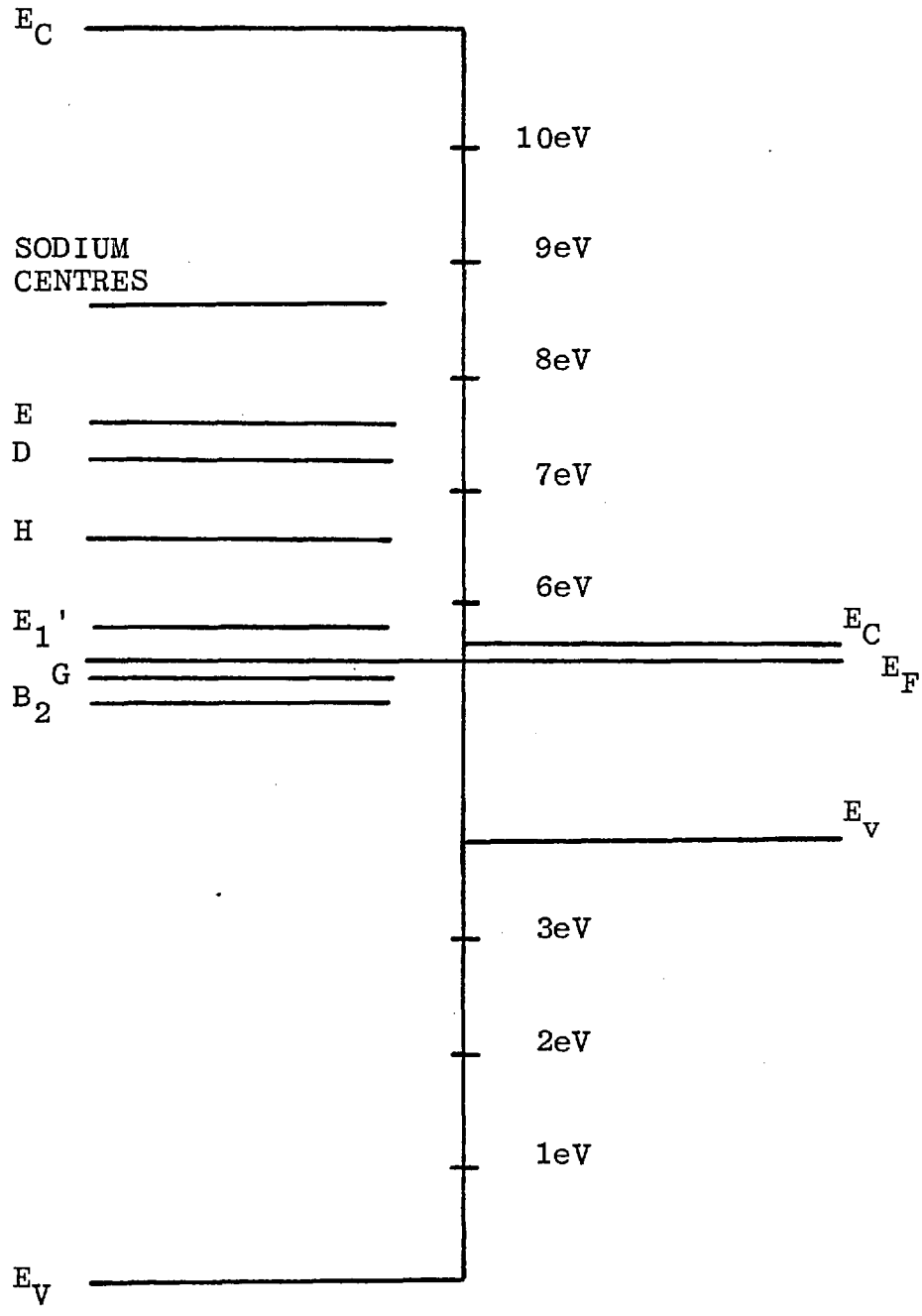


FIG. 6.1 DEFECT STATE AND INTERFACE ENERGY LEVELS IN CdSe-SiO_2

different workers. Part of the problem seems to be in defining precisely what is meant by the band gap in a non-single crystal material such as silicon dioxide.

In such a material the conduction and valence bands will not have sharp edges, but rather the density of states functions have long tails extending into the forbidden region, and there is a fairly sharp mobility edge. Mott has suggested that the true value of the forbidden gap for SiO_2 is close to 11eV, rather than the smaller values often given and this is the value assumed here.

The fermi level of the silicon dioxide is assumed to be in the centre of the gap, and of course lines up with the Fermi level in the CdSe semiconductor on the right. The conduction band edge in the semiconductor is at 0.084eV above the Fermi level[14]. In the case of the silicon-silicon dioxide interface, the distance between the semi-conductor valence band edge and the insulator conduction band edge has been determined by internal photo emission[15]. This measurement has not been performed on the CdSe-SiO_2 system, so there is some uncertainty in the energy levels here.

Although the semiconductor conduction band in Fig.6.1 has been shown as running straight up to the interface (the flat-band condition) there will generally be some band bending at the interface, which will vary with the applied gate field. Also, the defect levels have been shown as mono-energetic, which is not really correct, particularly in an amorphous material such as the sputtered film, where the levels may be expected to broaden out because of the random nature of the lattice.

From Fig.6.1 it is seen that the position of the E_1' band is very close in energy to the semiconductor conduction band edge - it is in fact at just about the required position for the putative trapping state. This fact is of course dependent on the particular value chosen for the insulator forbidden band gap, and in general exact coincidence of the energy levels will not occur. Depending upon the extent of the distribution in energy of the trapping states, however, some latitude is available in determining the levels. As the gate voltage is varied, the charge induced in the semiconductor varies - in other words the bands bend. The part of the trapping distribution opposite to the semiconductor conduction band edge changes and so, if the trapping distribution varies with energy, the degree of slow state decay will vary with gate voltage. This was the principle behind previous measurements to determine the trap state density as a function of energy[16]. To analyse these measurements it is necessary to calculate the variation of surface potential of the semiconductor with gate voltage.

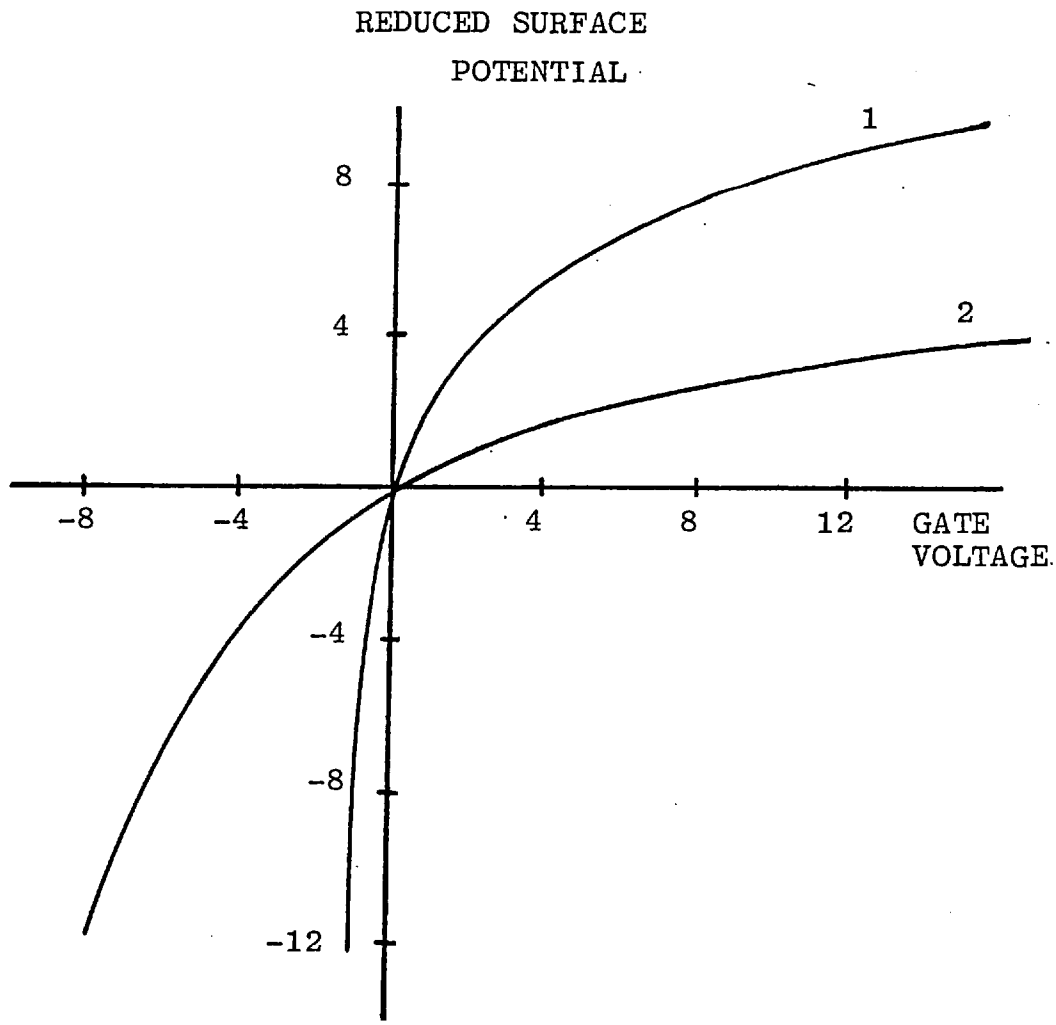
In the case of a single crystal semiconductor this procedure is straightforward. However, for a polycrystalline material the interaction with the gate field is far more complex because of the presence of the grain boundary trapping states in the material. This matter has been investigated by Anderson[17], who has shown that in polycrystalline materials the variation of surface potential is much reduced compared with single crystal. Rather than varying the surface potential, and hence carrier density, the gate field principally varies the carrier mobility by modulation of the intergranular potential barriers.

Calculation of the precise variation of surface band bending would require knowledge of the densities of trapping states at the grain boundaries, and also the carrier densities both in the bulk of the crystallites and at their surface. At present this detailed information is not available. A further complication is that there is not a single value of surface potential but rather a distribution over the interface, the potential being different where a grain boundary intersects the interface from its value elsewhere.

The slow state measurements of Chapter 3 cannot therefore be used to determine quantitatively the energy distribution of the trapping states. Qualitatively, however, a rise in slow state density at higher gate voltages is frequently seen; that is, as the band bending increases downwards. This could be taken to indicate an increasing density of trapping states at energies closer to the Fermi level. However, it is also possible that this reflects rather a variation of band bending with gate voltage.

If the surface potential variation of the semiconductor were directly proportional to the gate voltage, then the slow state density would be a direct reflection of the distribution in energy of the trapping states. In general, the relationship between these two quantities will not be so simple.

For the case of a single crystal semiconductor, the variation is of the form shown in Fig.6.2, the surface potential varying much less with gate voltage at higher gate voltages (i.e. in accumulation) than at low gate voltages (in depletion). The slow state density at the



CURVE 1 DOPING DENSITY 10^{22} m^{-3}
CURVE 2 DOPING DENSITY 10^{24} m^{-3}
SiO_2 THICKNESS 1000Å

FIG. 6.2 VARIATION OF SURFACE POTENTIAL WITH GATE VOLTAGE FOR CdSe - SiO_2 INTERFACE

higher gate voltages is therefore measured over a much narrower region of the trap distribution. The effect is to "stretch out" and compress the trap distribution as reflected in the slow state density.

Using a single crystal method of calculation, the slow state versus gate voltage curves of Chapter 3 result in trap density distributions showing a pronounced peak close to the Fermi level.

For the polycrystalline material there is not a single unique value of the surface potential. Due to the trapping states at the grain boundaries there exist space-charge regions at the grain boundaries. The semiconductor potential is therefore different where a grain boundary intersects the semiconductor surface from the value over the rest of the surface. The result of this is that different parts of the trap distribution are sampled in different regions of the interface, so that the trap distribution as reflected in the slow state density is smeared out. It is not possible to extract the original trap distribution with the information available.

6.5 CONCLUSIONS

The behaviour of $CdSe/SiO_2$ thin film transistors has been examined with particular reference to the slow-state instability effects. It has been found that the trapping process is due to a quantum mechanical tunneling process by means of which charge from the semiconductors is captured by trapping states located in the insulator forbidden gap.

The threshold voltage drift has been found to be caused by a single set of traps, with capture cross-section

and density of 3 x $10^{-16}m^2$ and $10^{24}m^{-3}$ respectively. The traps are distributed uniformly in the region close to the interface to which tunneling is possible.

A brief investigation was also made of the slow instabilities in transistors made with yttrium oxide as the dielectric layer, as an alternative to silicon dioxide. Generally the results obtained were similar in the two types of device. The capture cross-section of the traps is very similar to that found in the silicon dioxide devices.

Whilst the identity of the trapping states has not been conclusively determined, it is likely that electrically active oxygen vacancies in the insulator structure are the trapping species. The drift of mobile electrically charged ions, under the influence of the gate field has been found not to occur.

Certain aspects of the conduction process in the polycrystalline semiconductor film have been investigated briefly, and the results obtained were explained with reference to intercrystalline potential barriers in the material.

Several topics worthy of further investigation arise from this work. The first is a full analysis of the conduction and modulation processes in polycrystalline semiconductor films, taking account of the grain boundary and surface regions of the film, both experimental and theoretical investigation being necessary.

Examination of the energy level relationships at the $CdSe/SiO_2$ interface would be helpful in fixing energy levels of trapping states; such information has been

obtained in the case of the Si/SiO_2 interface by means of internal photoemission measurements, and similar experiments of $CdSe/SiO_2$ devices should be feasible. With this technique, it is also possible to investigate the variation of the semiconductor surface potential with the gate field applied to the device.

Finally, further investigation of the relationship between the density of slow trapping states in TFTs and the preparation of the device could be made - work so far has concentrated on making good devices, rather than systematically varying fabrication procedures and observing the effect in the completed TFT.

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