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IMPLEMENTATION OF A POWER SYSTEM DISTANCE RELAY USING MICROPROCESSORS

BY

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ABSTRACT

Using digital techniques for power system protection tasks has many advantages in terms of reliability, flexibility and better response matched to the conditions in the power network. Distance protection is one of the most important functions employed for transmission lines. Existing digital techniques employ a minicomputer for this purpose. Such implementation is helpful for testing different methods and studying the processing requirements, but its application in a power systems network is impractical for economic and technical reasons.

The purpose of this thesis is to implement a distance relay, which performs all the operations accomplished by existing distance relays, but with a dedicated digital microprocessor.

To achieve fast response, good stability, reliability and flexibility a careful and simple design of both, the hardware and software is required. From the hardware point of view the unit is divided into the data acquisition interface and the protection processor. The processor is composed of bit-slice, bipolar microchips with 16-bit integer arithmetic.

The software development is divided into two areas. Firstly the generation of an appropriate instruction set for the distance application and secondly the use of an algorithm which can cope with transient conditions occuring after a fault. The algorithm employed solves the differential equations of the protected line, considered as a simple R,L series circuit.

In addition the relay performs some other functions to ensure stability, discrimination and high availability. Some of them can be met in existing relays, while others are new features introduced by the modular design and programmability of the unit.

ΣΤΟΥΣ ΓΟΝΕΙΣ ΜΟΥ

To my parents

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CHAPTER 1

INTRODUCTION

1.1. Power systems relays

The role of relays in power systems is to detect any abnormal operating condition and either to initiate a trip command to the associated circuit breakers to isolate the faulty part or to inhibit a switch closure which might cause maloperation. Many different types of relays are available, which individually protect against different risks. The combination of relays is known as a protective system.

The main characteristics of a relay are:

i) an assurance of operation in the event of a fault in the protected zone of the primary system.

ii) to remain inert to all normal load conditions and external disturbances.

iii) to detect the fault, in the shortest possible time, such that loss of synchronism is avoided.

All the above requirements are met by employing reliable protection equipment and by a careful and suitable protection scheme design for a specific part of a power system.

1.2. Distance relays

One of the main tasks in protection is that of feeder protection i. e. overhead lines or cables. The

most popular form of high voltage overhead line protection is that of employing a distance relay. These relays measure the impedance or reactance of a line, which is assumed proportional to the distance between the relaying point and the fault.

Distance relays provide high speed fault detection for front line or main system protection and back-up facilities in a single scheme and overcome the need of pilot lines.

A simple illustration of the distance relay principle is given in fig. 1.1. The relay is supplied with two inputs, namely voltage (V) and current (I) at the relaying point. It then takes a decision based on a comparison of the voltage and the quantity $I Z_L$, where Z_L is the setting of the relay. It sends a trip command on the condition $V < I Z_L$ i. e. for measurement of an impedance from the relaying point to the fault point less than Z_L.

For many years electromechanical techniques have been used to construct relays, but as the complexity of power systems has increased, the need for a relay of higher performance with more sophisticated characteristics became apparent. The progress in semiconductors has made possible the construction of analogue relays. Therefore static- analogue electronic- relays, in many cases,have replaced the electromechanical ones[1,2].

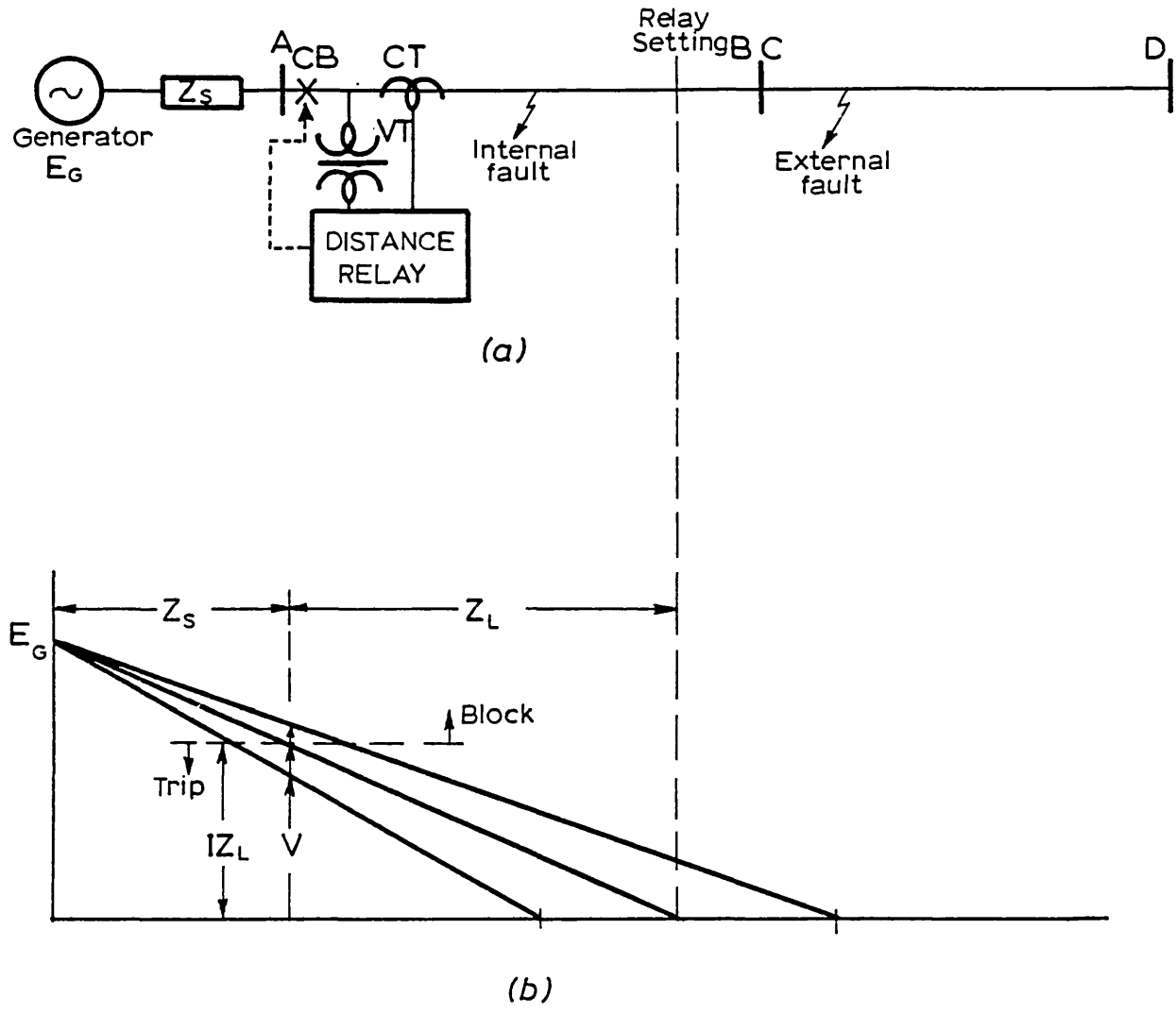


Fig. 1·1 Principle of the impedance distance measurement

(a) System schematic

(b) Relay trip zone

E_G = E.M.F.

Z_S = Source impedance

Z_L = Line impedance (setting of the relay)

CT = Current transformer

VT = Voltage transformer

CB = Circuit breaker

It has been shown by experience, that by choosing high- reliability components and by careful design, these static relays are superior to the electromechanical ones[3]. On the other hand, by employing analogue devices, some disadvantages are introduced, as have been discussed by Horne[4].

Briefly these are:

i) Initial and long term accuracy is unpredictable because of the offsets and gain adjustments of analogue elements.

ii) To ensure a reliable analogue relay, components of close tolerance have to be used, which increases the cost of the unit. However the reliability of an analogue functional unit can be calculated beforehand, as opposed to that of the electromagnetic designs.

iii) They offer poor flexibility, in cases where characteristic modification is necessary as the primary system changes.

iv) A basic problem in protection is to detect a failure of the relay unit early enough. Generally a failed component, in a static or electromechanical relay becomes apparent only after a primary fault occurs or during manual testing.

v) A short repair time is important. Usually the maintenance of analogue devices, with possible readjustment takes time.

Therefore the next step was to apply digital techniques for the protection task. The study of such systems started in the late 1960's. A digital device with its programmability can cope with greater performance and flexibility to solve protection problems. In the next sections, a discussion is given of the advantages and disadvantages of digital protection.

1.3. Advantages of digital protection

Some of the following advantages are common to all digital devices, others are dependent on the scheme applied. These are:

i) Greater flexibility.

By employing a suitable processor, which satisfies the protection requirements, the hardware is fixed for all the relaying applications. By calling different programs, different protection and control options can be accomplished. But the most striking attraction of a programmed device is that alterations or additions to the protection scheme can be done easily, without costly rewiring or hardware replacement.

ii) Enhanced reliability

A secure and stable operation of the protection apparatus depends on its reliability. Two kinds of reliability have to be achieved[5]. Firstly a high design reliability is necessary. It includes the design of the specific apparatus and the correct selection of the different

equipments to complete the protection system. Secondly a high technical reliability has to be ensured, which depends on the quality of the manufacturing process.

Digital equipment can improve both of them, by the inherent good reliability of the digital devices and by suitable software design.

The hardware reliability enhancement, stems from the following facts: i) Advances in the semiconductor manufacturing process, have improved the reliability of the digital integrated circuits (ICs) by a factor of 100 in the past 10 years[6]. ii) The failure rate of a digital device is lower than that of a linear one. iii) In a digital circuit, the use of passive components is reduced. Those components are prone to failure due to aging, therefore the reliability of the whole unit is increased. iv) If a semiconductor device has a deficiency due to the manufacturing process, then that should be detected during its commissioning period. v) The use of LSI components, leads to fewer interconnections, hence reducing one main source of failure in electronic circuits.

A digital processor is a dynamic device, because it is programmable. By employing software techniques we can cater for missing or erroneous data. Work has been published on this topic concerned with the input data

validation[7]. On the other hand the unit will be more reliable, if the software is as simple as possible.

Finally, because of the monitoring capability of the digital scheme, a failure of any apparatus in the protection network, can produce an alarm immediately for operator attention.

iii) Greater accuracy

In static relays, accuracy can be impaired by the drifting of analogue devices. Besides this fact, that some parts of the digital scheme, i.e. the interface, is still analogue, the accuracy can still be improved by using a processor of suitable word length with a proper type of number representation and with a powerful instruction set.

iv) Adaptive capability

By altering the software, the relay can be programmed such that to adjust its characteristic, according to some criteria, for example load conditions. Therefore more sophisticated responses can be fulfilled .

v) Modular construction

This benefit, does not affect directly the user. From the manufacturer's point of view, it is a great advantage to construct a single piece of apparatus, which can be applied for many applications. Changes of the protection scheme, such that to satisfy the customer's specifications, can be easily done. The assembly

process is simplified by using a limited number of components. The maintenance is becoming easier, with the use of LSI devices, and by the fact that recalibration is not necessary as with analogue equipment. At the same time, the availability of the unit is increased by reduction in the repair time.

vi) Response time

Detection times comparable with those for static relays can be achieved. Reduction of the operating time depends on factors, such as the speed and the processing power of the digital processor and the algorithm employed to fulfill the protection scheme.

vii) Reduced burden on current transformers(c.t's).

A c.t. must maintain its ratio, over a wide range of conditions. This ability depends on the impedance of the relay and the resistance of the leads. In the interest of the c.t. cost and space requirements, the relay power should be kept to a minimum. A digital scheme can fulfill this requirement because very little power is necessary on the input to the A/D circuits.

viii) Monitoring capability

In a complete digital protection scheme, depending on the hierarchical levels, a monitoring of all front- line relays is possible. Such monitoring can produce a full report during a fault, measurement of active and reactive power flows, or even a plot of the measured quantities.

This ability simplifies the installation and the testing of the relay.

All those arguments give a more reliable system, with high availability.

The economic benefits, in terms of capital expenditure are still not clear, caused partly by the fact that hardware costs are declining and partly on the software complexity involved in the specific application. A complex program will need skilfull programmers, which is going to increase the development cost. That depends on the type of programming language applied, the protection scheme employed and on the expected number of sales of a specific unit.

1.4. Disadvantages of digital protection

Besides the many advantages that can be gained by using a digital protection configuration, some disadvantages are introduced. These are:

i) Conversion to digital form is required for all the analogue measurements, with the input signals taken from conventional c.t's and v.t's. This increases the complexity of the unit and its cost.

ii) Interference problems

The digital relay, working in the substation environment needs to be carefully designed and installed, to avoid electromagnetic interference.
The origin of such noise is a result of sudden change in the circuit quantities caused by switching of circuit breakers

and isolators by lightning strikes or by insulation breakdown. Methods to reduce this interference on the relay are described by various authors[8,9].

iii) Training of personnel.

By introducing equipment of another technology, a retraining of personnel in its use and service becomes essential.

iv) Testing under all possible conditions.

To test the relay as an integral unit i.e. hardware and software together, becomes a difficult task. This is because an almost infinite number of combinations of tests parameters, from possible signal and clock levels, timing conditions, program patterns, power supplies voltages and operating conditions needs, to be taken into account[10].

1.5. Organisation of the Thesis

This thesis describes the design, construction and operation of a dedicated digital power systems distance relay.

Chapter 2 gives a brief description of a distance relay and reviews the characteristics of different protection schemes. It discusses the possible digital computer configurations. It examines the requirements for a dedicated digital distance relay in conjunction with the existing processing techniques.

Chapter 3 gives a brief description of the

data aquisition unit and its requirements from the line protection point of view. The processor structure in terms of hardware and software is discussed.
In this chapter the development aids and the testing facilities necessary for the construction and the testing of the relay are presented. In appendices the hardware and software implementations of this apparatus are given in more detail.

Chapter 4 deals with the distance algorithms. It explains what a distance program has to accomplish, and gives the available types. Then the algorithm chosen, along with the filtering process are discussed and a modified algorithm is presented.

Chapter 5 discusses the organisation of the distance program, in terms of the starting fault elements, and the trip decisions. The additional features of the relay, as the print-out report facilities, the active and reactive power measurement and others are given.

In chapter 6, the performance of the relay and the tests carried out, are reported and the results discussed.

The conclusions are presented in chapter 7.

The original contributions contained in this thesis are claimed as:

1. The selection of a digital line protection scheme, which combines fast response, reliability and flexibility at reasonable cost.

2. The modifications and expansion in the hardware and software design of a special purpose high-speed dedicated microprogrammed microprocessor to match the requirements of a distance algorithm.

3. The modification of an existing algorithm, to achieve a faster response.

4. A complete digital distance relay has been constructed working in real time, which operates in less than 20 ms using 16-bit integer arithmetic with no hardware multipliers. The relay can detect all possible types of internal faults occuring on a protected transmission line. It is of the three- zone stepped type and monitors continuously all six primary fault impedances, hence eliminating the need of a starting technique.

5. In addition to protection, it fulfills all desirable tasks which can be expected of an industrially produced relay (reference 11).

These are:

a) close-up directional discrimination

b) switch-on-fault

c) out-of-step blocking

d) autoreclose

6. Besides the above facilities, it provides:

a) Full fault report, in the monitoring computer, which can be of considerable assistance in system operation.

b) A simple self-test monitoring, which can improve the reliability of the whole protection system and its availability.

c) Measurement of active and reactive power in the transmission line, at any instant.

CHAPTER 2

DISTANCE PROTECTION

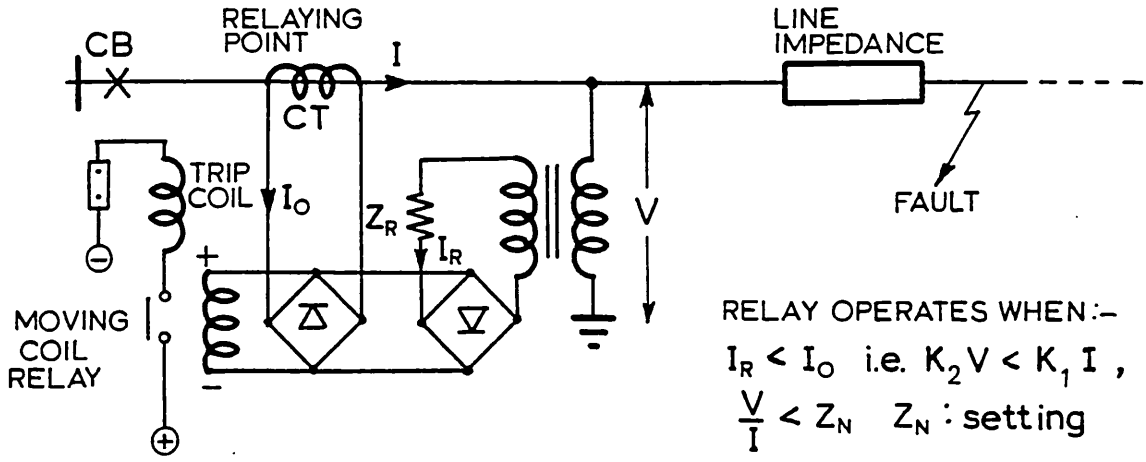
2.1. Present practice in distance relaying

The first application of distance relays was in early 1930's[12] based on the electromagnetic operating principle.

A simple form of a typical electromagnetic relay is shown in fig. 2.1. A rectifier - bridge current comparator is used, to compare V and I. Two alternating input- currents are applied to the comparator, i.e. the operating current $I_0=K_2I$, and the restraining current $I_R = K_1V$, where V,I are measured at the relaying point. The output of the comparator is applied to a sensitive d.c. polarized relay of the moving- coil type(fig.2.1b). The rectified currents, circulate round the inter-connecting leads when the a.c. input signals are equal, therefore the coil is de-energised. If one of the inputs is increased with reference to the other, then the difference current will flow in the relay. Depending on the input, the relay will operate, if $I_0>I_R$ or will restrain if $I_0<I_R$.

Other types of electromechanical relays exist, which use different principle, for example the induction disc and the induction cup[1].

Many duties performed by electromechanical relays have now been undertaken by static devices.



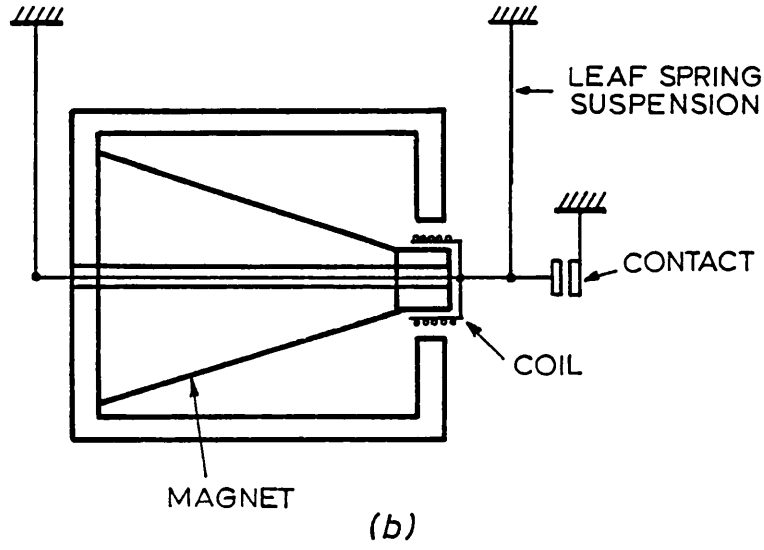


Fig. 2·1 A schematic diagram of an impedance distance relay

(a) The rectifier-bridge comparator and its connections with the C.t. and V.t.

(b) The moving coil relay

Their lack of moving parts improves the operating time. In addition other impedance characteristics can be obtained, which can cope with different power system configurations and types of faults.

For example, the implementation of the mho relay (discussed later in this chapter) by using linear integrated circuits is indicated in fig. 2.2 [1]. The polarity detectors determine the zero crossings of the a.c. inputs to be compared, i.e. they produce a square wave of the same frequency as the a.c. input. The coincidence detector provides a rectangular wareform having a negative level for both, positive and negative coincidence, and a positive level for non- coincidence. Therefore the shape of this wareform depends on the phase relationship of the inputs. The integrator is charged and discharged according to the duration of the positive and negative output of the coincidence detector. When this output stays more in the positive level than in the negative, the integrator output is increased, which finally becomes greater than the specified operate level. Then the level detector is energized, and a trip command is generated. The three possible operating conditions of this circuit are indicated in fig. 2.2b, c, d.

The ideal distance relay measures the impedance from the measurement point up to the fault point. But

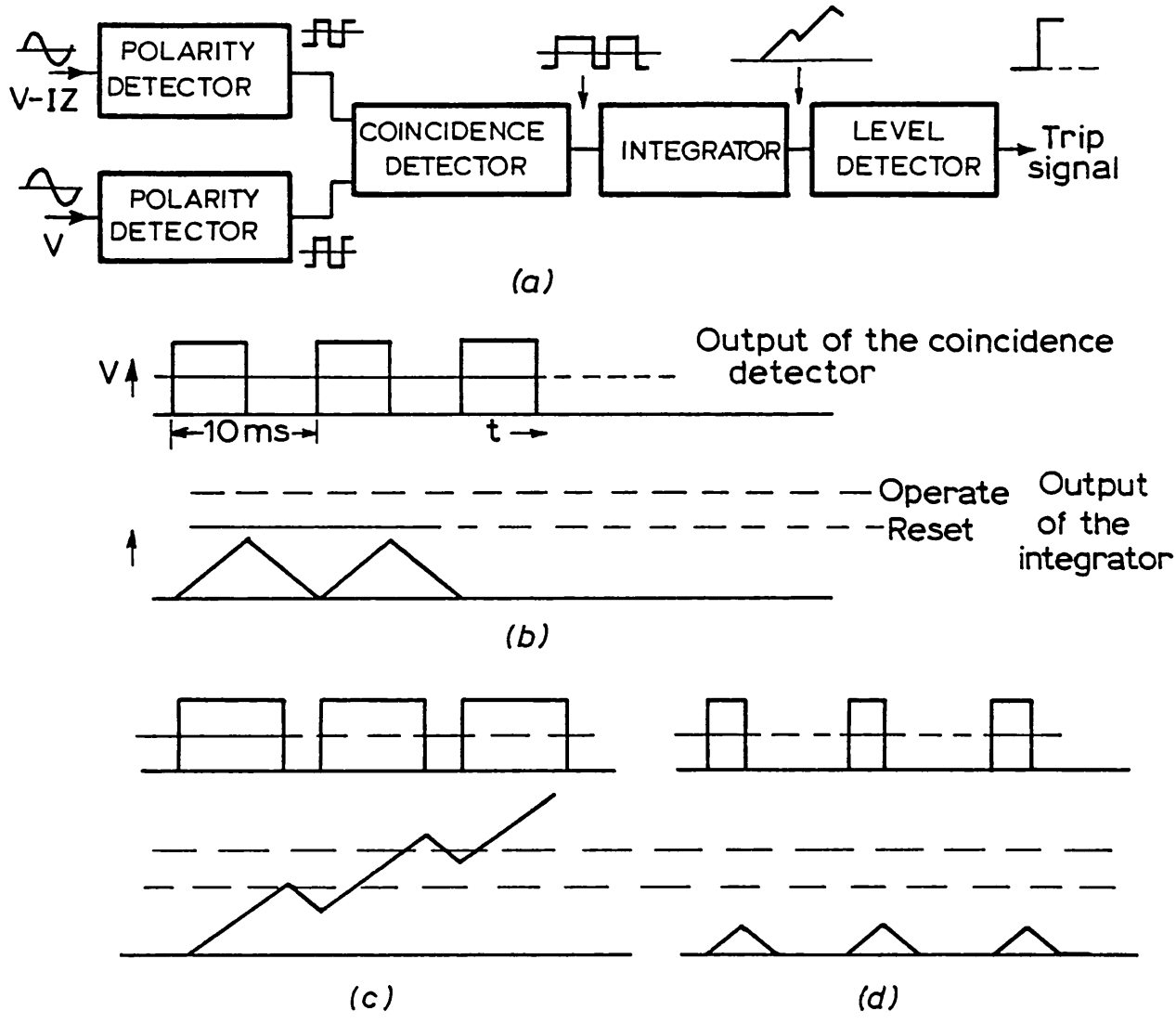


Fig. 2·2 Static mho distance relay

(a) Block diagram

(b) Boundary condition

(c) Operate condition

(d) Restrain condition

the circuit impedance can be affected by the fault arc resistance, the system load and other conditions external to the section being protected. A systematic analysis of the response of distance relays, under different operating conditions is given by Lewis and Tippett[13].

In the next section are presented the discrimination techniques used, the classification of distance relays and the distance schemes applied.

2.1.1. Discrimination

A distance relay should protect against faults only on its own feeder, but because of measurement errors in the current and voltage transformers, the relay tolerances and the changing operating conditions, the relay cannot cover the whole line with the specified accuracy. Therefore it is usually set to protect up to about 85% of the feeder length, denoted by zone 1 in fig. 2.3. The rest of the feeder is protected by zone 2, but this also covers part of the following feeder, hence providing back-up protection for this part. In fig. 2.3 to discriminate relay A from relay C, a time-lag is necessary between the issuing of a trip signal for zone 1 and for zone 2. This time-lag depends on the operating times of the relays and of the corresponding circuit breakers. Finally to complete the back-up for feeder CD and to include part of EF, zone 3 is used, which

operates after a further time-lag. This stepped distance/ time characteristic is that most commonly used.

The relay normally incorporates a directional unit, so that the above characteristic is valid only for faults in front of the relaying point.

2.1.2. Classification of distance relays

Relays are classified according to their threshold characteristics on a polar diagram which distinguishes between healthy and faulty conditions within each zone.

The right choice of characteristic depends on the types of faults, the fault arc resistance, the length of the line and the susceptibility to power swings.

In fig. 2.4 AB is the feeder impedance representation on the R-X plane, representing an ideal characteristic, while AP_1 is the " reach " of zone 1. Taking into account the fault arc resistance, the relay should operate only for those faults inside the shaded area. Also shown in fig. 2.4, are the tripping areas for zones 2 and 3.

Figure 2.5 shows some basic distance relay characteristics[14].

The impedance characteristic is the simplest and consists of a circle with centre at the origin. Tripping occurs in the shaded area, if a directional element is employed. Such a unit is necessary, because the relay can operate below a certain impedance threshold, which is independent of the phase angle between voltage

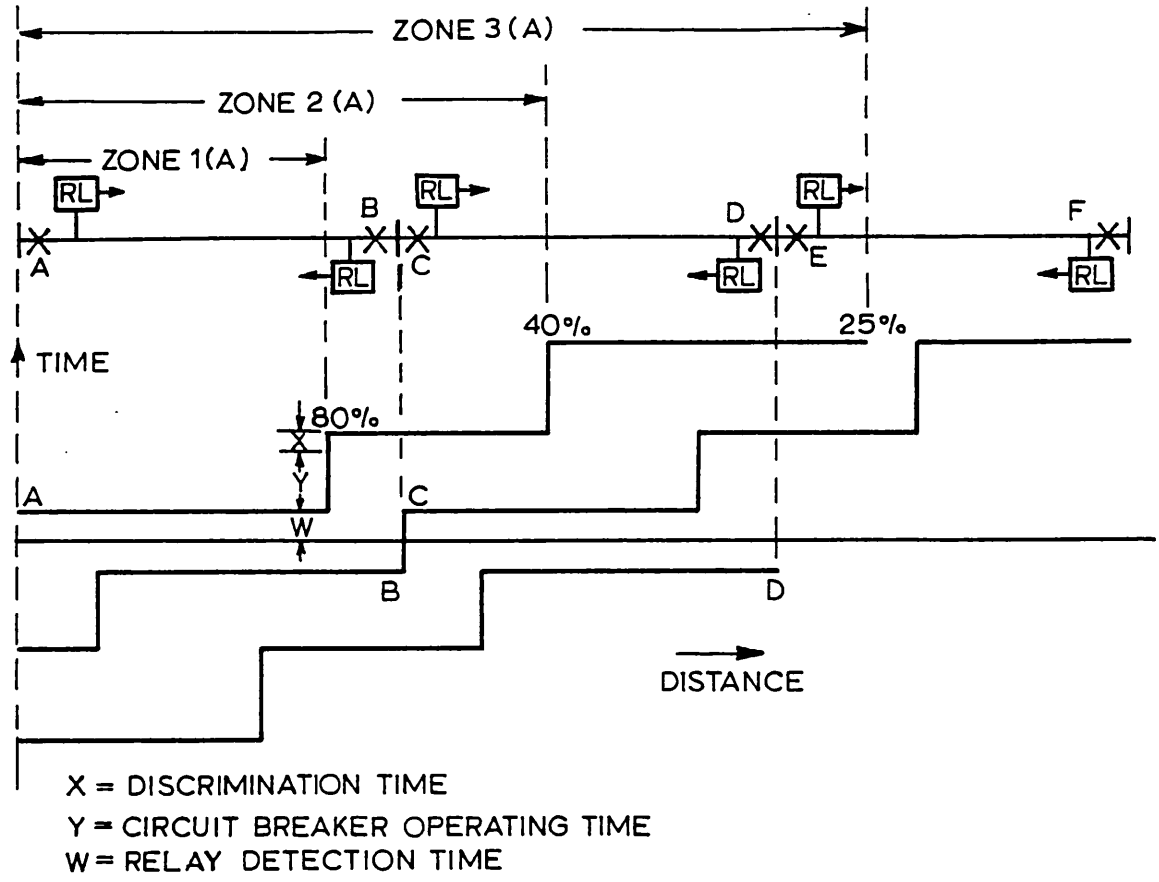


Fig 2·3 Time/distance characteristic for a three-stage distance relay (for clarity, the characteristics of A,B,C,D only are shown)

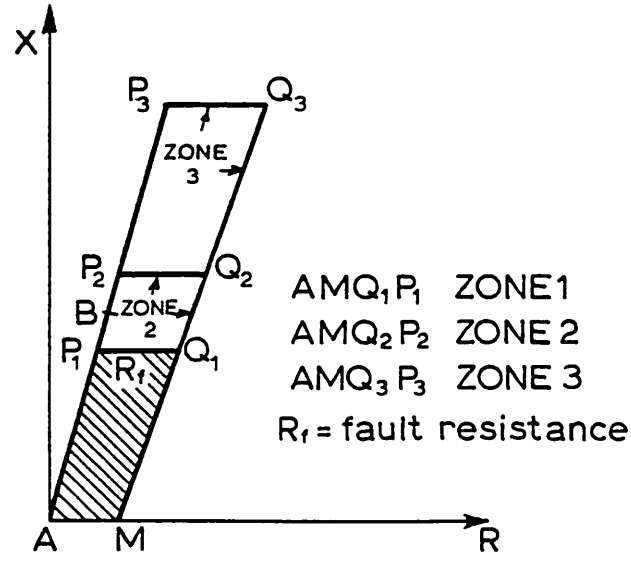


Fig. 2·4 The fault area on the impedance diagram

and current.

The mho relay has a circular characteristic too, but now passing through the origin.

The reactance relay polar characteristic is a straight line parallel to the resistance axis. Operation occurs for reactances less than the setting value.

Also shown in all diagrams of fig. 2.5 is the power swing locus PS. Following a transient disturbance in a power network, the operating point changes and PS is the locus of the impedance as seen by the relay under such conditions. The power swing locus, in general is a circle, but for simplicity it can be considered as a straight line in the operating region of the relay. As the phase displacement between the sending and the receiving ends increases, the locus passes through the relay tripping characteristic . To prevent maloperation the relay must be blocked under such conditions. This is achieved by using an additional relay, usually a mho, which embraces the zone 3 characteristic. Under fault conditions both, the measuring and the blocking relay will operate almost simultaneously. But under power swing conditions, the distance relay will operate after the blocking relay, therefore tripping can be prevented.

The conclusions from fig. 2.5 are:

i) The impedance and reactance relays need a directional element to inhibit operation for faults

behind them.

ii) The reactance relay has the greatest tolerance to variable fault resistances.

iii) The mho relay is less tolerant to fault resistances, but it has greater immunity to power swings.

iv) The impedance relay is a compromise between the mho and reactance relays.

In conclusion the reactance relays are useful for short lines, as the fault resistance is a considerable percentage of the line impedance. They are also preferable for ground fault detection, because the resistance of the return path can be high. On the other hand the mho relay is used for long lines, because of the small common part between its characteristic and the power swing locus.

Modifications of those characteristics, using the mho offset and the fully cross- polarized mho relay improve discrimination under different operating conditions.

The offset- mho relay has a circular characteristic too, but it is shifted to embrace the origin by introducing a current bias signal into the voltage circuit. This arrangement will cater for close-up faults, even if there is a complete collapse of the voltage at the relaying point. It also provides some back-up protection for the busbars. Usually it is used as a starter and

for the zone 3 measuring unit.

The fully cross-polarized relay uses as inputs to the comparator the quantities V-I Z_N and V_{pol}, where V_{pol} is a polarising voltage derived from one of the other healthy phases. As a result of this configuration, the mho characteristic extends its characteristic along the R axis for unbalanced faults. Therefore the mho relay can cope with greater values of arc resistance.

Another popular characteristic, which is close to the ideal one is the quadrilateral, shown in fig. 2.6. The area covered is greater than the fault area, such as to take into account errors in the measurement of a solid fault on the line or a resistive fault on the busbar.

2.1.3. Distance schemes

There are four types of shunt faults which can occur in a three-phase system. These are, three phase, double phase to earth, double phase and single phase to earth. A distance scheme should detect all of them, but as already mentioned, the measured impedance is a function of the type of fault[14]. To overcome this complication a means of compensation is necessary. This compensation technique is different for phase and earth faults. For the phase fault units, the relay should be fed with the line voltages and the line currents. In an earth fault, the current through the relay depends on the method of

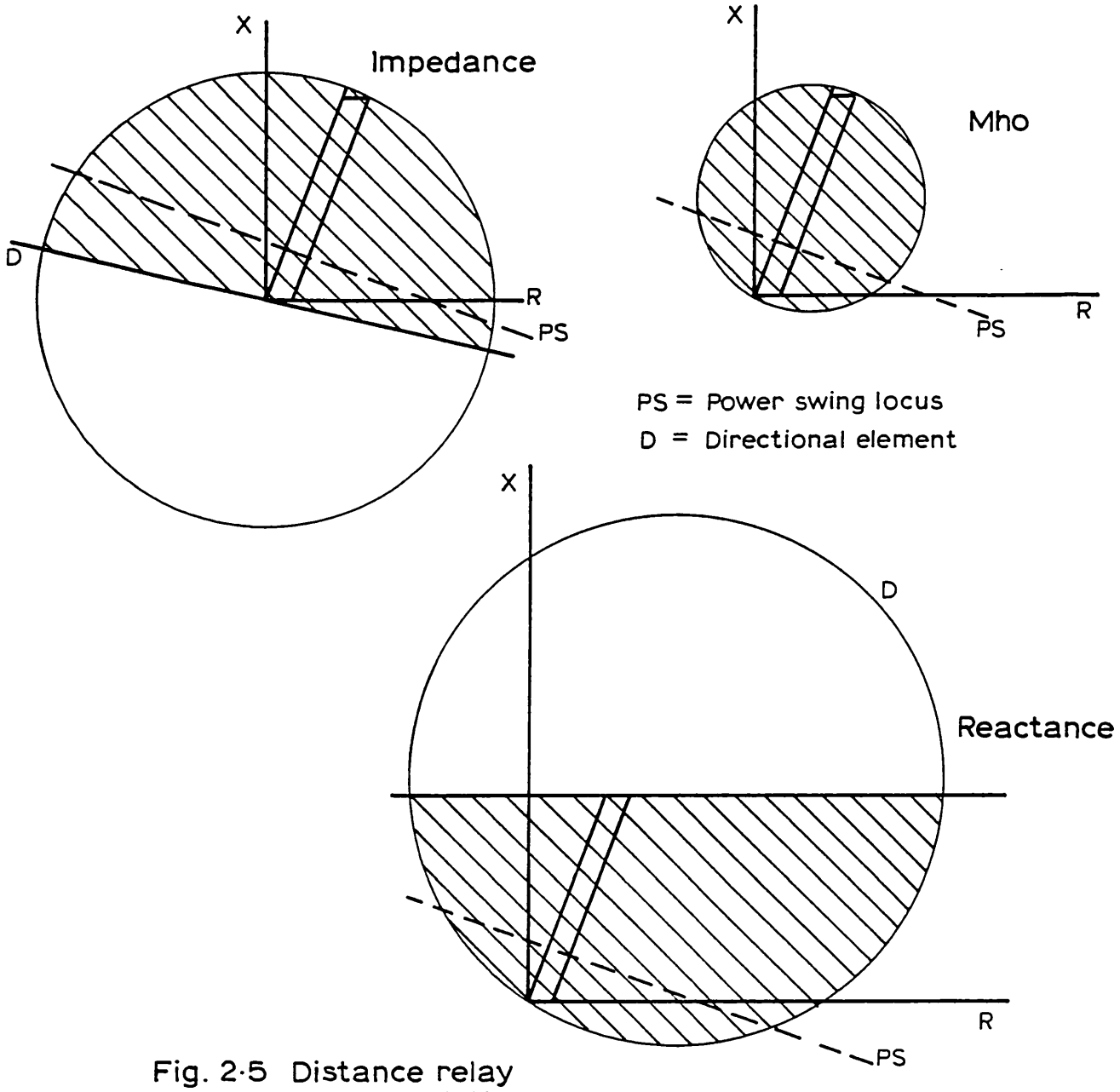


Fig. 2·5 Distance relay characteristics

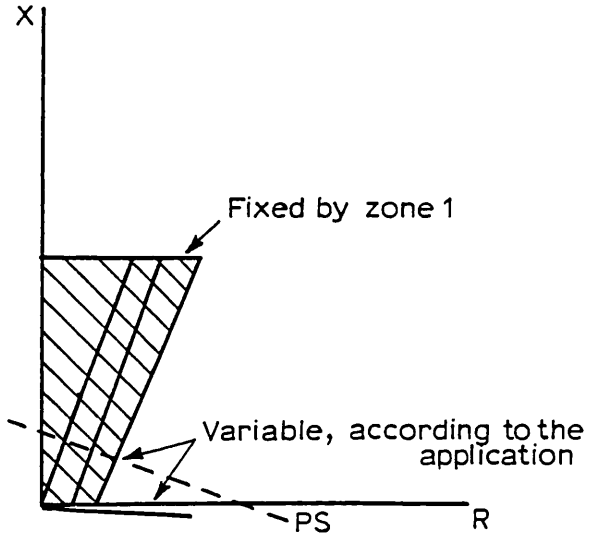


Fig. 2·6 Quadrilateral characteristic

earthing, the number of earthing points and the sequence impendances of the earth loop.

Two methods are used for earth fault distance relay compensation, called the residual and sound-phase compensation methods. The most popular is residual compensation which measures an impedance which is independent of the specific earthing connections of the system by adding a fraction of the residual current to the phase currents.

If $\dot{I}_R$ is the residual current, $\dot{Z}_{L1}$ and $\dot{Z}_{L0}$ the positive and zero sequence impedances of the line respectively (see fig. 2.7), then the fraction to be added is $\frac{K-1}{3}$, where $K = Z_{L0}/Z_{L1}$ [14]. Hence, for the phase(a)ground fault relay, the presented quantities are, $\dot{V}_a$ the phase voltage and $\dot{I}_a+\dot{I}_R\,(\frac{K-1}{3})$, where $\dot{I}_a$ is the phase current.

To protect the line against all possible phase and ground faults, one of the following schemes is applied:

i) the straight forward scheme, uses six distance measuring units, three for phase-phase faults (p.f.) and three for phase to ground faults (g.f.).

ii) the switched scheme, in which one measuring unit is employed with starting elements to apply the appropriate voltage and current to the measuring relay, according to the type of fault.

The starting elements are of the overcurrent or the under-impedance type. The overcurrent starters can be used in all cases where the fault currents are considerably higher than the maximum expected service current. For systems[5] where the minimum three-phase fault current is less than the maximum service current, under--impedance starting is employed. The reach of these relays is not a fixed impedance, but an increasing value as the voltage falls. Below a certain voltage level, it behaves as an overcurrent relay[1].

Use of the switched scheme reduces the relay cost and panel space required. However, it introduces the following disadvantages:

i) a small increase in the total time of measurement, because of the time required for the fault classification.

ii) if the under-impedance relays have to be used, then the cost of the unit is increased.

iii) there is a complete loss of protection, if the measuring unit fails.

iv) there is some inaccuracy because of different characteristics for p.f. and g.f.

v) if the fault changes, before tripping, a possible wrong switching can occur.

vi) its reliability is reduced, because the tripping decision is based on the operation of contacts

in series.

The above disadvantages lead to the conclusion, that the switched scheme can only be applied to middle range of voltages i.e. 11-132 KV.

One weakness of the straight forward system is that more than one relay might operate for one kind of fault, especially for a line with a high X/R ratio and a fault close to the busbar. A detailed examination of such cases is given in reference 15. In general none of the relays in the healthy (sound) phases overreaches i.e. the impedance presented in the relay is never less than the actual, but an occasional tripping by a relay on a close-up fault in another phase, will contribute to back-up protection, at the expense of a wrong flag indication. This action depends also on the relay polar characteristic.

2.2. Digital distance protection

Since 1963 the advantages of using mini-computers for control of substations[16], to on-line data acquisition and to processing at the national control centre[17] have become evident.

Taking into account disadvantages of static relays and advantages that can be gained by introducing digital processing techniques, as discussed in chapter 1, a study of digital methods for distance protection is an obvious area of research.

The first paper to be published on this subject,

was by Rockefeller[18] in 1969. It was concerned with the use of a process-control computer, to protect the equipment in a h.v. substation, and the lines radiating from it.

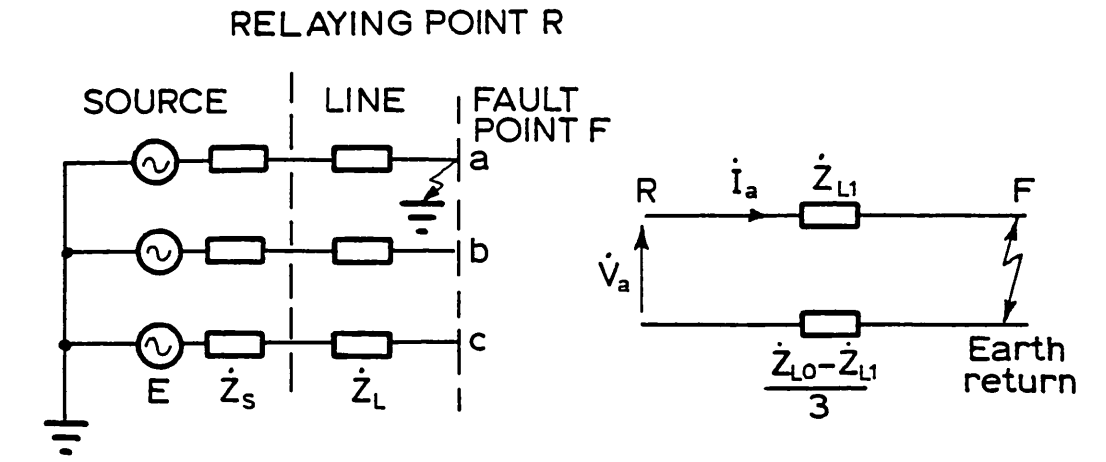
Most of the work done on digital distance protection has concentrated on the development of different algorithms, which compute the line resistance and reactance under transient conditions. These algorithms have been applied by using either a main frame computer or a minicomputer, and they will be reviewed in chapter 4.

The block diagram of a digital distance relay can be seen in fig. 2.8. Such a system can compete with existing relays only, if it can be shown to be more reliable and economical. Such justification can only come with further development and application.

The reliable and secure protection of a power system network depends on two factors.
Firstly the reliability of individual items that constitute the protection scheme(generator, line protection and so on) and, secondly, on the correct selection and interconnection of these items to produce a reliable system.

In a digital scheme, all these factors have to be taken into account. The possible configurations that can be used are:

i) an integrated scheme, consisting of a single



Actual circuit

Equivalent circuit for the faulted phase from the relaying point to the fault point

$\dot{V}_a$ = Relaying voltage

$\dot{I}_a$ = Fault current

Fig. 2·7 Earth-fault loop

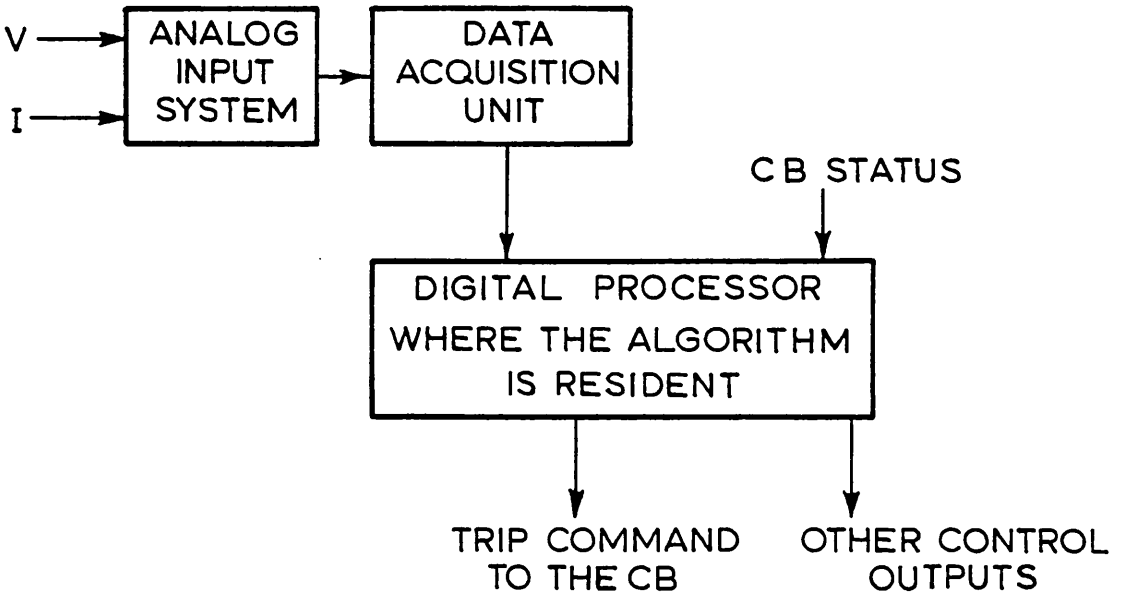


Fig. 2·8 A block diagram of a digital distance relay

computer programmed for multiple relaying functions. Such a processor has to be a powerful one, therefore a minicomputer has to be used.

ii) a dedicated scheme, utilising separate computers, each one with its own data acquisition unit, for each specific application. Such a processor need not be as powerful as a minicomputer, but it has to be fast enough to cope with the high-speed protection tasks.

Each of those schemes introduces advantages and disadvantages. A summary is given in table 2.1, which has been taken from reference 19. A proposed scheme, by the same authors, combines the advantages of these two solutions, to produce a comprehensive, reliable and cost effective protection network. This configuration is shown in fig. 2.9. As can be seen, the integrated digital scheme has its own interface and fulfills the back-up and monitoring requirements.

The purpose of the research reported in this thesis, is to perform front-line feeder protection by employing a dedicated, fast and cost-effective digital processor. This processor must be designed such that it is compatible with the configuration of the scheme shown in the fig. 2.9. In addition to increasing its reliability, it must be programmed by using simple software techniques. It must also perform all the duties expected of a present typical distance relay.

TABLE 2.1

DIFFERENCES BETWEEN THE DEDICATED AND THE INTEGRATED PROTECTION SCHEMES

	Dedicated	Integrated
Reliability	1.Smaller size gives greater hardware reliability per module. 2.Failure limited to one application.	1.Software complexity gives more errors. 2.Major hardware/software failure could affect all applications, hence redundancy must be adequate.
Data Validation	1.Limited data validation possible.	1.More data available in common data base to detect hardware software faults i.e.system is more tolerant of failures. 2.Central data base available for onward transmission of data.
Cost	1.Interface costs high for a multiplicity of applications.	1.Shared facilities make for more economic applications. 2.Software costs may be higher for a more complex system.
Speed	1.High processing speeds possible.	1.Careful system design necessary to ensure adequate speed of operation.
Flexibility	1.Each new application requires a separate computer system.	1.System is radial in concept and easily modified for additions or delitions of plant. 2.Common data base provides access to data for new application.
Maintenance	1.Only one function at a time need be taken out of service.	1.Adequate redundancy essential since all applications are affected by taking out one system. 2.Larger systems can support more comprehensive monitoring and diagnostics.
Software	1.Software is specific to each processor and is therefore modular and simpler. 2.Any intercommunications at high speed between dedicated machines will be difficult. 3.On-line development impractical	1.Software, other than for the application programs, is complex. 2.Communication between programs associated with items of plant is achieved via the common data. 3.On-line development possible.
Computer Hardware	1.Total configuration could be complex where intercommunication is required.	1.Basically implemented on radial principle with computer hardware at centre.

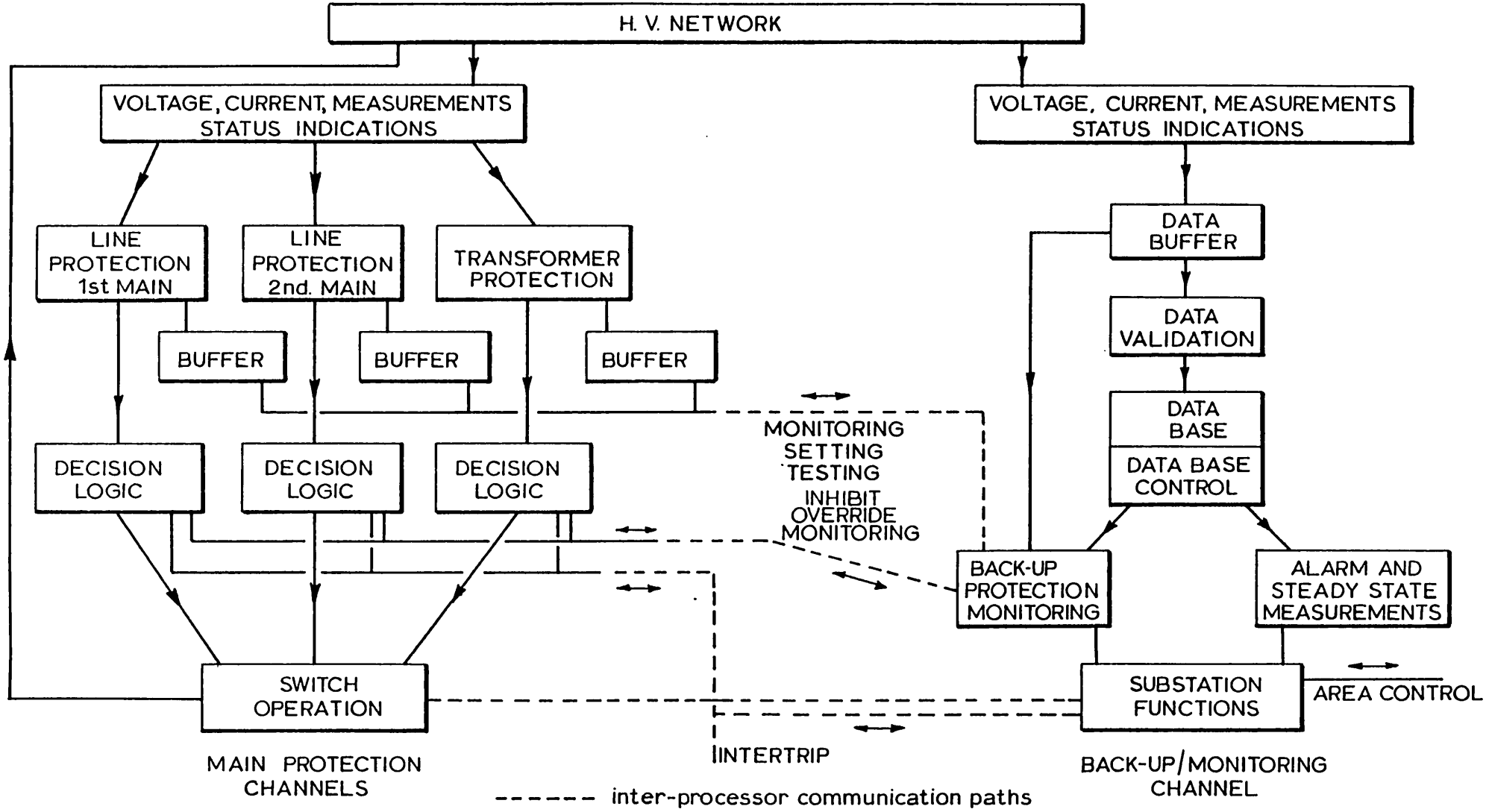


Fig. 2·9 A proposed configuration for the combined integrated/dedicated digital protection of a substation.

2.3. The dedicated digital distance relay

In chapter 4, a discussion about the devised distance algorithms will be given. Most of them have been tested in the laboratory, but very few of them have been actually tried in the substation environment. All of them employ a minicomputer as the processing element. Under such operating conditions, their performance has been examined.

The required digital distance relay should be of the dedicated type, therefore a microprocessor has to be employed.
To achieve operating characteristics, similar to those implemented by a minicomputer, the microprocessor must have comparable speed and processing accuracy.
Hence the choice of the most suitable family of microprocessors to implement the dedicated distance relay can be based on this criterion.

The performance of the digital relay depends on the way the analogue data are handled, on the actual microprocessor architecture employed and on the software techniques used to implement the distance algorithm.

The digital relay is divided into two units:
i) the data acquisition interface and ii) the protection processor. The reason for doing this is related to the differing nature of the two functions. Besides that, the processor does not have to control the input of the

analogue data. That reduces the hardware and software requirements of the processor and improves its speed.

A brief description of the operation of each unit will be given. A more detailed discussion is presented in chapter 3.

2.3.1. The data acquisition unit

The duty of this unit is to take regular samples of the three voltages and the three currents at the relaying point. Then those quantities have to be transmitted in a digital form to the processor.

In addition to the analogue inputs, it can accept direct digital data, which can be intertrip signals, circuit breaker status or switch status indicators. A block diagram of the data acquisition interface is given in fig. 2.10.

2.3.2. The distance protection processor

After the digital data have been transferred from the interface to the processor, the processor must select and process them in a manner according to the algorithm. A decision has to be taken, based on some criterion. Therefore sufficient data and program memory must be provided.

It is a basic requirement, that the algorithm must be run before the next block of samples arrives from the data acquisition unit. Otherwise an erroneous decision will be generated.

A means of sending the control signals to the associated circuit breakers is obvious.

Since this dedicated digital distance relay is going to be used in conjunction with a monitoring computer, a communication output to this computer has to be included.

Fig. 2.11 shows those essential functional blocks of the microcomputer.

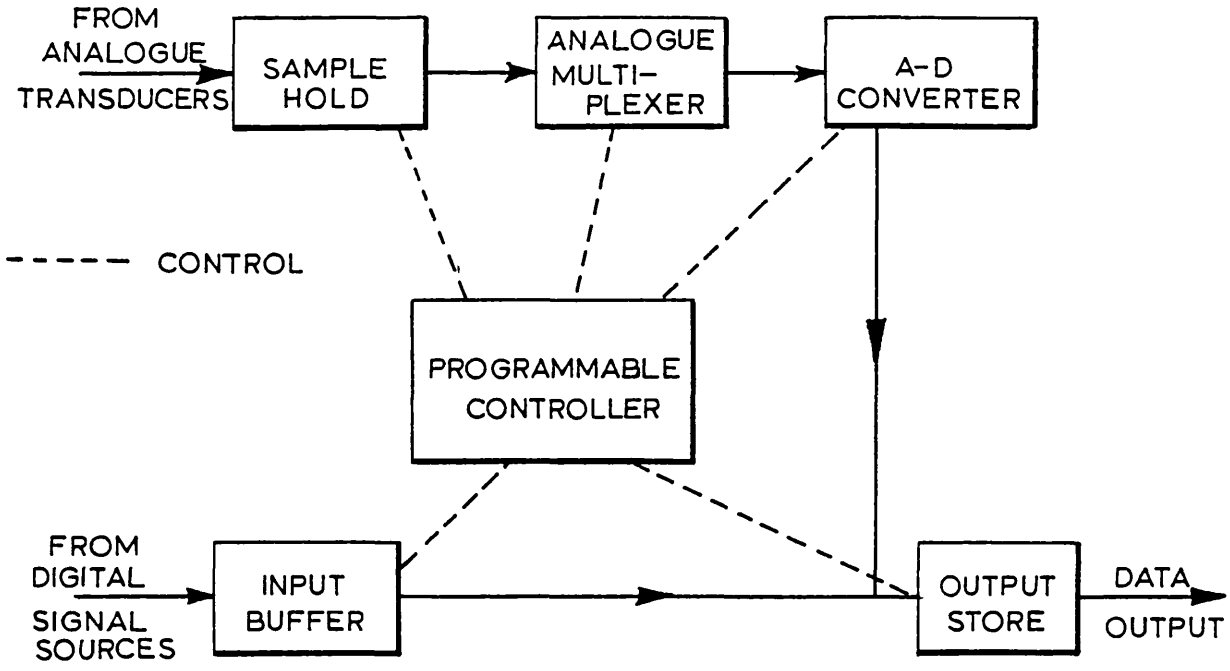


Fig. 2·10 Data acquisition unit outline configuration.

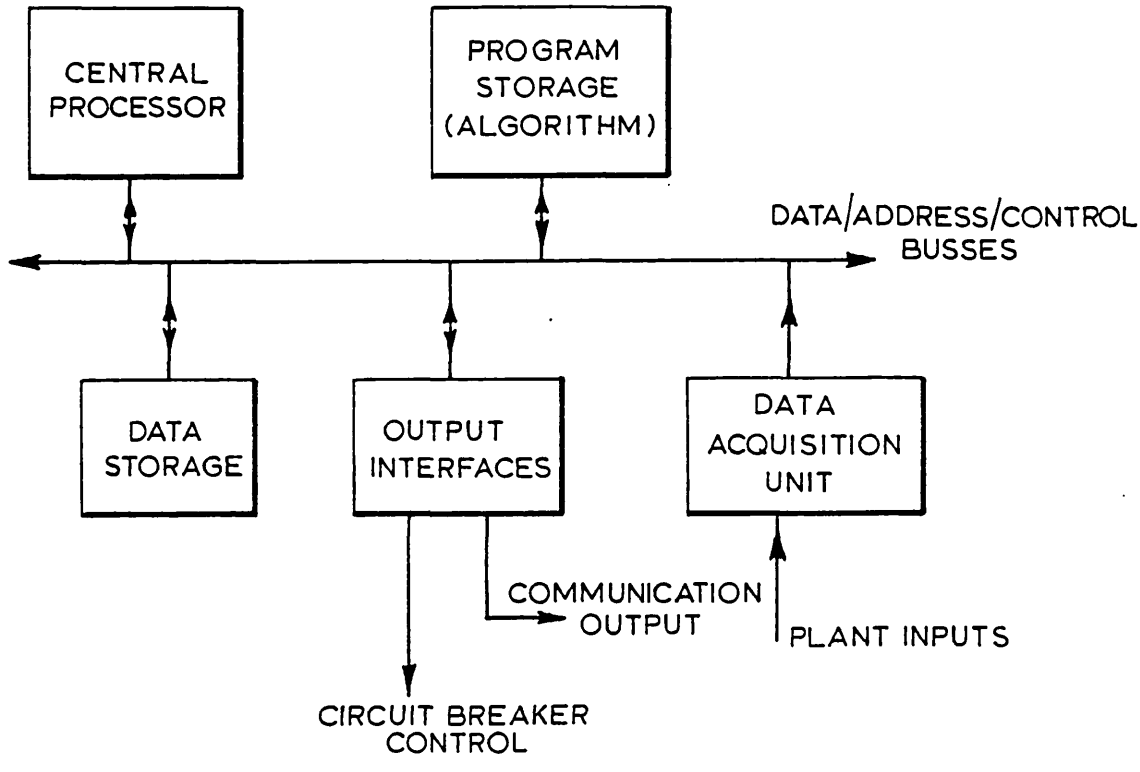


Fig. 2·11 Protection processor outline configuration.

CHAPTER 3

HARDWARE DESCRIPTION OF THE DEDICATED DIGITAL RELAY

3.1 Introduction

The two parts of the digital relay i.e. the data acquisition unit and the protection processor are here described. As the microprocessor employed is microprogrammable, the structure of the instruction set is vital for the overall performance. The instruction set is described and its limitations are discussed in this chapter.

Finally the hardware and software aids required for the development and testing of the digital processor as an integral unit are examined. The way these aids are implemented are essential in terms of cost, development, debugging time and flexibility.

3.2 The data acquisition unit (DAU)

The DAU design must fulfill two main requirements: i) accuracy of measurement with faithful digital representation of the primary network quantities and ii) flexibility for different protection schemes. A detailed description of the DAU design and its implementation has been given by Horne[4]. Here a brief description of this DAU will be given and in appendix 1 the circuit of each module is detailed.

Fig. 3.1 shows a block diagram of the DAU. In the left hand side of the diagram the analogue signals are

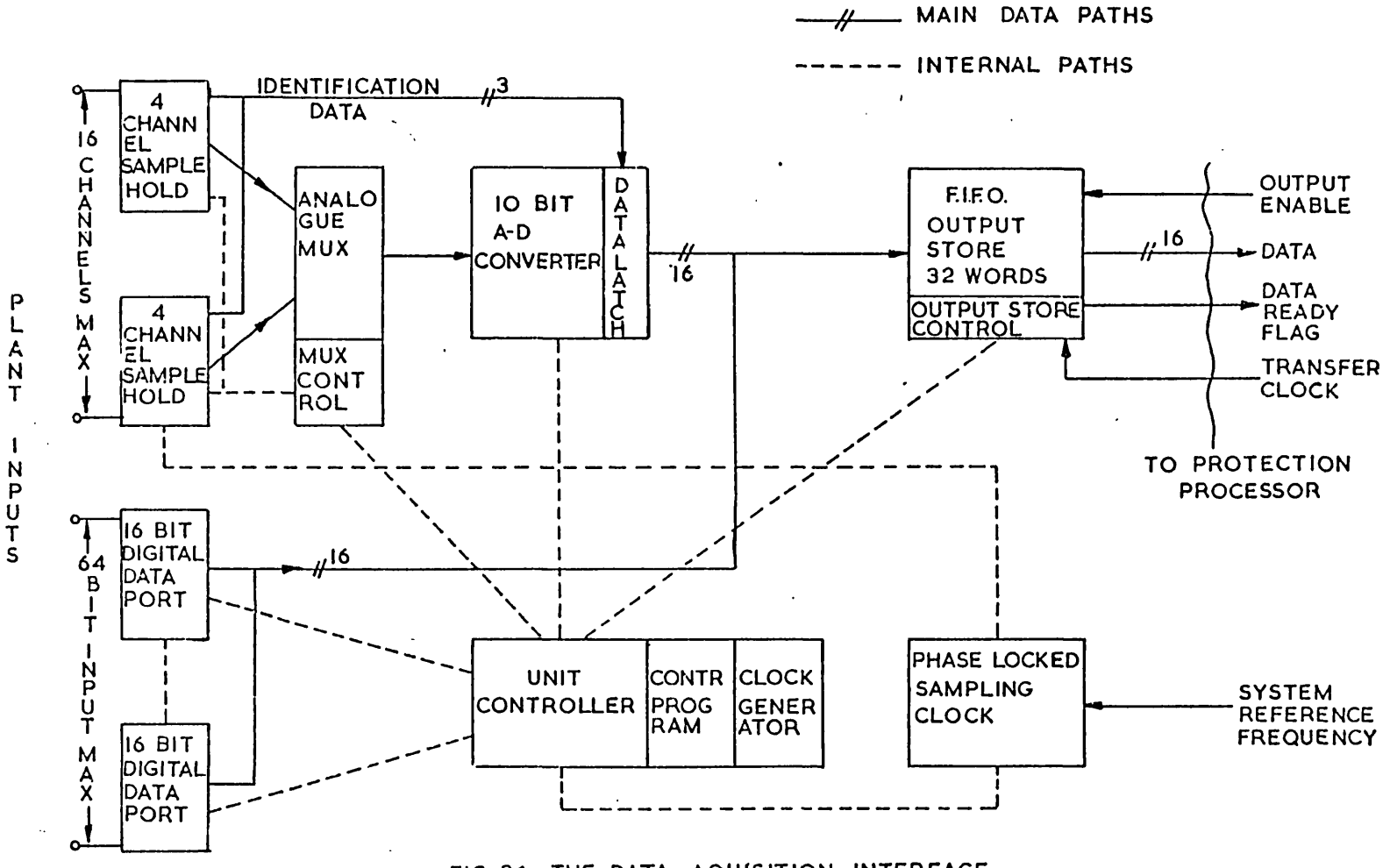


FIG 3.1 THE DATA AQUISITION INTERFACE

entered after analogue filtering and amplification. One problem needing attention is the way the signals are transmitted from the transducers to the digital relay inputs. Malfunctioning might occur from induced noise due to electromagnetic radiation. Fiber-optic data links with their immunity to electromagnetic interference, dielectric isolation, improved safety and increased bandwidth could be employed with advantage. The economics and choice of the required fibre-optic system are discussed in references 20, 21, 22. The analogue filtering is described later in chapter 4.

One other requirement is that of analogue signal ranging, as the power system signals will have a wide magnitude variation. It must be ensured that the relay signals are within the operating range of the DAU i. e. ± 10V. If the gains of the individual input amplifiers are set to these limits, then inaccuracies can be produced in low magnitude signals. Schemes to improve the relay performance at this stage are given in reference 4. The one which the author favours, in terms of processing flexibility and fast settling times, is that using gain ranging amplifiers, as shown in fig. 3.2. Four different gain factors are possible, by using four separate amplifiers. The comparators ensure the selection of the correct amplifier, such that the signal to the interface never exceeds ± 8V (giving a 20% margin). The range data

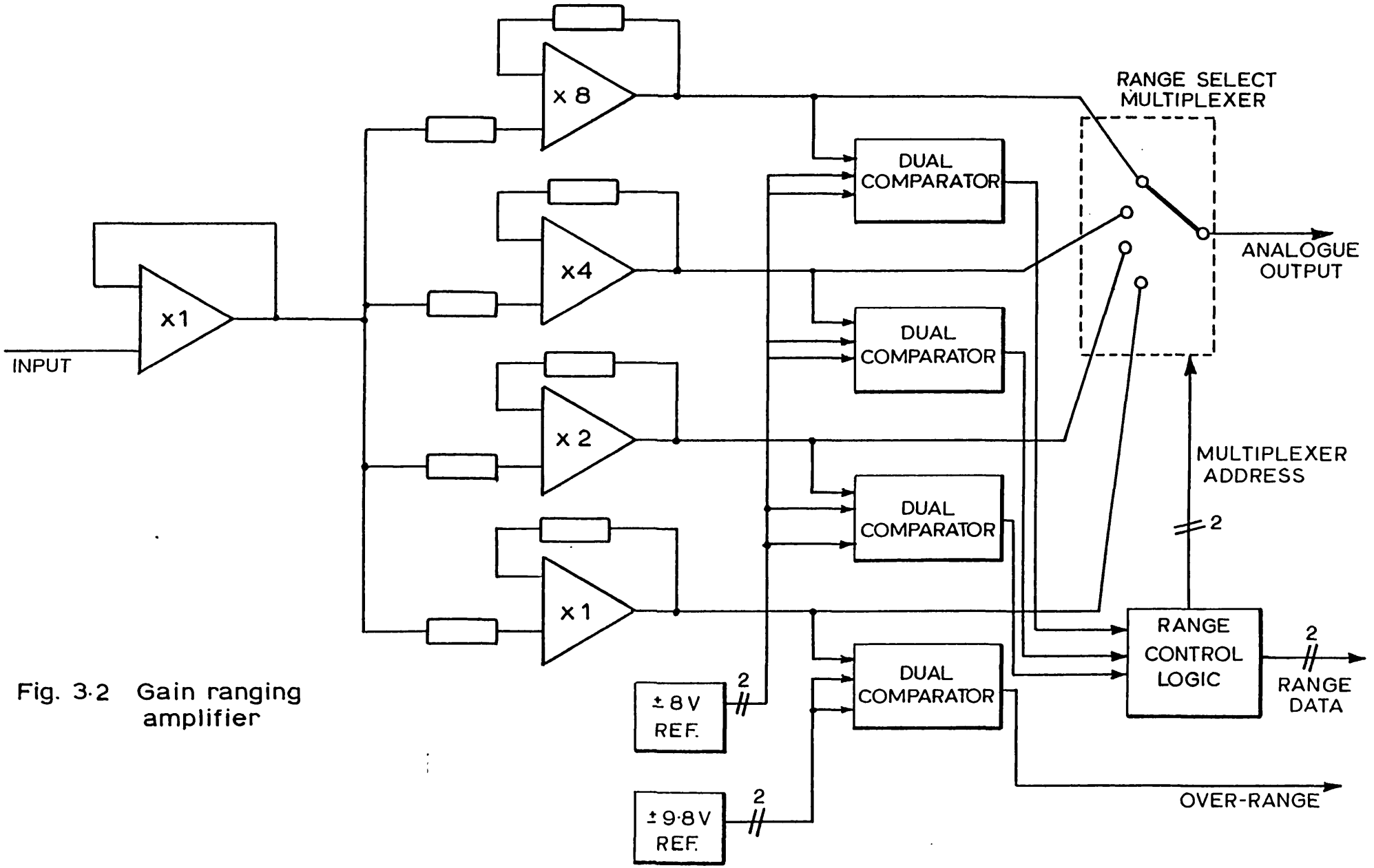


Fig. 3·2 Gain ranging amplifier

indicates which amplifier is being used at a particular instant and these range bits are used by the processor to reconstruct the real value of the signal.

3.2.1 The analogue- data channel

From the line protection point of view, seven analogue signals are required, namely the voltages and currents for the 3 phases and the reference voltage for the self- monitoring program to be discussed in chapter 5. Therefore seven sample/hold devices are needed. These devices are essential, otherwise the input signal would change during the conversion and the desired accuracy (defined by the A/D resolution) will be impaired. The alternative solution employing a faster more expensive A/D converter is not possible, when many channels are to be served.

Economics force us to use one only A/D converter, requiring an analogue multiplexer. Fig. 3.3 is the block diagram of the analogue multiplexer controller. Switches on the card module define the first and final analogue channels that are to be processed. The unit is capable of multiplexing a maximum of 16 channels.

The next task is to convert the analogue signals coming from the power system transducers to digital form. Here the A/D converter[23] has a conversion time of 6.4μs and a resolution of 10 bits. Such a choice is justified from the number of channels, the sampling rate and the

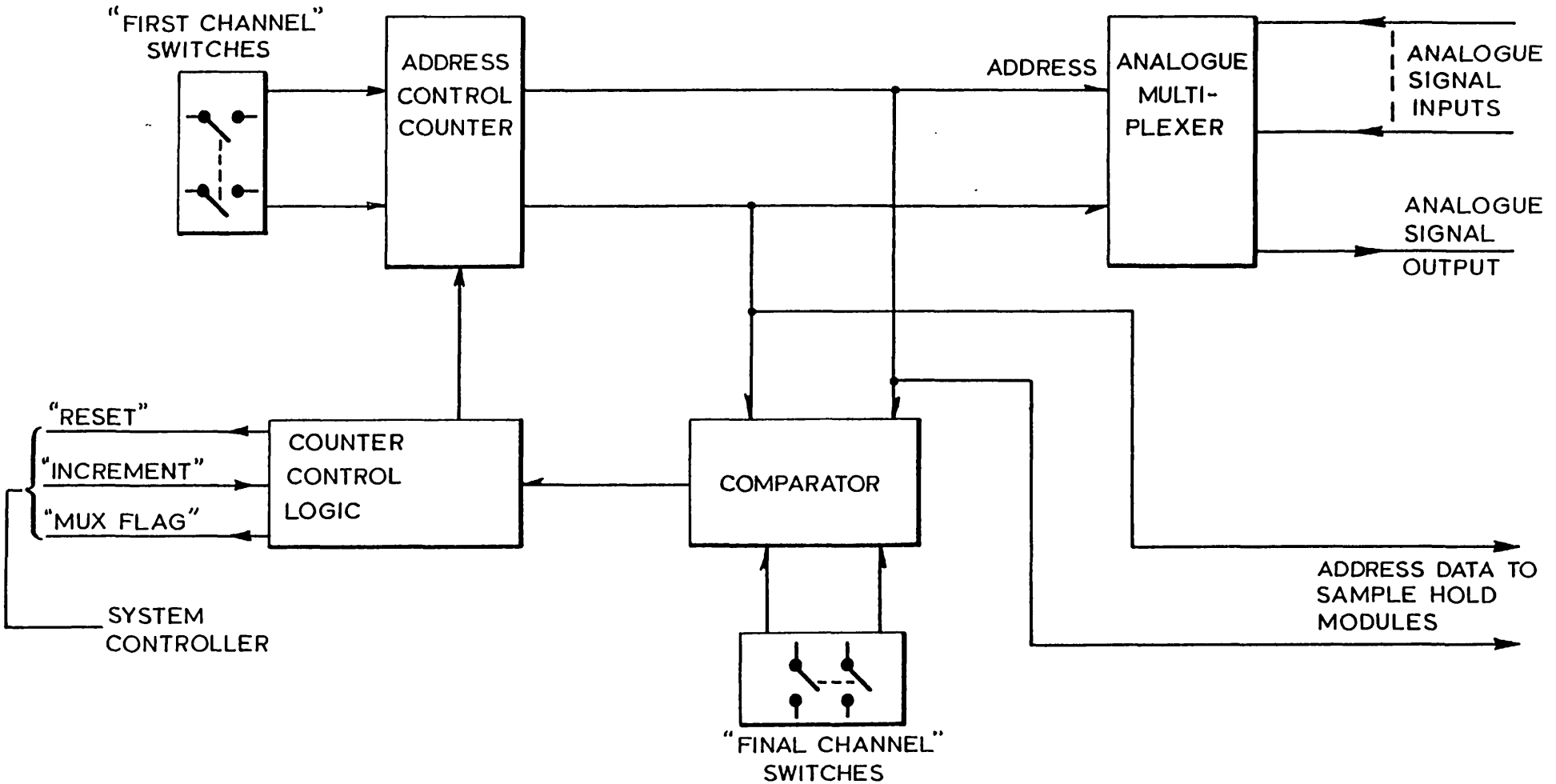
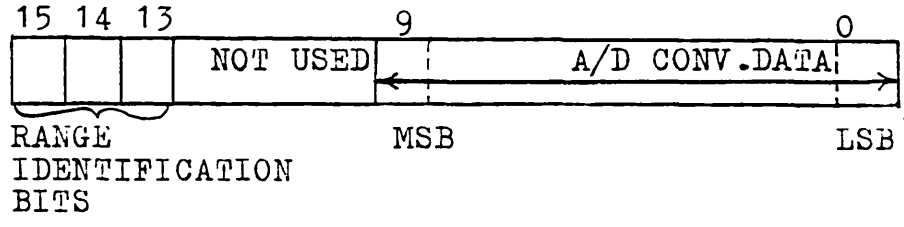


Fig. 3·3 Analogue multiplexer module

accuracy required, taking into account the accuracies of existing v.t. s and c.t.s.[4]. At the end of each conversion the digital form of the corresponding analogue signal is stored in the data latch (fig. 3.1). This latch reduces the conversion cycle timing by 18%, as the conversion and the data transfer to the F.I.F.O. output store can be accomplished in parallel. The format of the word written in the latch is:



3.2.2 The digital-data channel

In addition to analogue signals, digital data has also to be processed for a specific protection task. For example, for transfer tripping[1] the circuit breaker status and the trip signal from the far end of the transmission line might have to be used at the relaying point.

Another potential use of the digital input channels is to enter data from the monitoring computer or from a control panel.

In the present digital relay, the only digital word provided is the status of the 16 switches on the control panel, the functions being presented in table 3.1

3.2.3 The data output buffer

A FIFO has been used as the interface between the data acquisition unit and the protection processor.

TABLE 3.1

THE CONTROL PANEL

Bit	Function	Bit	Function
0	Fault applied switch	8	Check ref. voltage
1	RG Plot	9	Output V,I of relay
2	YG "	10	" filtered/unf. data
3	BG "	11	" 3 currents
4	YB "	12	" 3 voltages
5	RB "	13	Energise digital filtering
6	RY "	14	Start graphics
7	P-Q measurement	15	Input the relay settings

The stored words are transferred one at a time. When the buffer data memory contains valid data, the data ready flag (fig. 3.1) is set. This flag is checked by the processor using the instruction WFS, after which the first word can be fed to the micro-processor. To transfer the next word stored in the F.I.F.O block, a transfer clock signal is sent from the processor. The maximum transfer rate is one word every 1μs.

3.2.4 The Phase- locked sampling clock

The sampling clock provides sampling rates of

2, 3, 4, 6, 8, 12, 16, 24 times the reference frequency. It is designed to operate in synchronism with the a. c. system within the range 42 - 58 Hz, and it is implemented by employing the phase- locked oscillator principle. To select the desired sampling rate, the " rate select switches " have to be set as discussed in appendix 1. (Table A1.7).

3.2.5 The DAU controller

As the DAU has been designed to match differing protection tasks, the controller is quite flexible in providing configuration and timing control, achieved by a programmable architecture. The flowchart of the controller program is shown in Fig.A1.10. The program is resident in two 32-word, 8-bit PROMs, providing 32, 16-bit instructions. Another PROM (256 words of 8-bits) is used to implement the instruction decoder, which supplies the control signals to the modules described previously. The contents of this PROM are given in table A1.1.

Further information about the instruction format and the available instructions are available in ref. 4.

3.3. The protection processor (PP)

Experience from previous work at Imperial College[48] has shown that to implement protection methods with digital techniques, the employed processor must have an average instruction time of 1-2μs and a 16-bit accuracy.

Faced with selection of a microprocessor, the choice was between a fixed-instruction MOS chip, a bipolar bit-slice chip or a fixed-instruction bipolar chip[24]. The first family of MOS chips in 16-bit versions have now appeared on the market but they are slow, having a typical instruction execution time of 3-4μs.

The bipolar bit-slice devices are 2 or 4-bit segments of the central processing unit (CPU) of a microprocessor implemented with low power Schottky bipolar logic. They offer flexibility because they are microprogrammable and they are fast (typical cycle time of 150-200ns) and with a variable word length.

Fixed-instruction bipolar chips are also recently available, but they do not offer the flexibility of the bit-slice family.

Consequently the PP shown in fig. 3.4 has been built around the INTEL 3000 bit-slice family. As with most digital processors, it is divided into four parts, namely the arithmetic and logic unit (ALU), the control section, the memory and the input and output ports.

3.3.1 The ALU

The central processing element (CPE) of the INTEL 3000[25] contains all the circuits that represent a 2-bit wide slice of an ALU; therefore to build a 16-bit wide machine, eight such devices have been used.

To speed up the arithmetic operations, a carry-

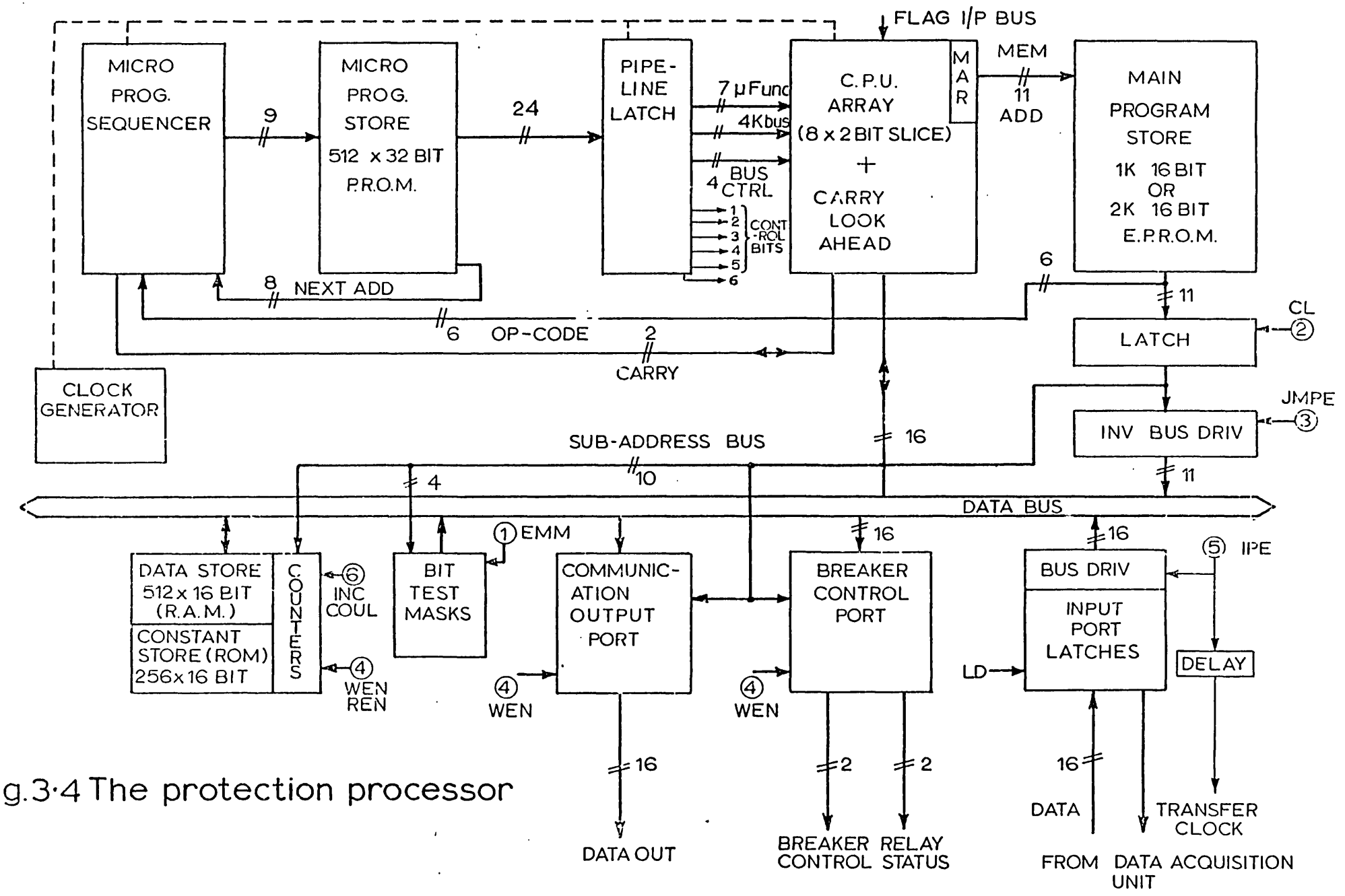


Fig.3·4 The protection processor

look- ahead generator[26] has been provided, which is capable of anticipating a carry-across a 16-bit word.

Each of the CPE's contains a full function accumulator (AC), an independent memory address register (MAR) and a scratchpad of eleven registers. Register T of this group has two of the AC qualities: i) it can be shifted to the right and ii) it can be loaded directly from the data bus or the flag input bus. Both of these features are quite convenient in implementing double-precision instructions.

The registers of the CPE's are allocated as follows:

i) Accumulator(AC) used for storing the result of an arithmetic and/or logical operation, and for outputting data to the data bus.

ii) R0 used as the program counter (PC) of the application program and stores the address of the next macroinstruction to be executed. This address is supplied to the MAR, which as can be seen in fig. 3.4 communicates directly with the main program store.

iii) R1 used as the loop counter for the multiplication (MUL) routine.

iv) R2 is a temporary store used: a) for the multiplicand in the MUL instruction and b) for the first word in a 3-word data block transfer (LMB,SMB).

v) R3 is a temporary store for the second word in

a 3-word data block transfer.

vi) R5 is the counter for the required number of multiple double precision shifts (DMR).

vii) R6 provides temporary storage for the most significant 16-bits of the product.

viii) R7 stores the return address during: a)sub-routine calls and b) indirect indexing addressing mode.

ix) R8 is used as a loop counter for multiple loops in a program. Instructions are provided: a) to load the number of counts required and b) to decrement its value and skip if zero.

x) R9 preserves the AC data for further operations. The final microinstruction in every AC manipulation macroinstruction performs a duplication of the AC data into R9. In the case of an instruction per - forming an operation which destroys the AC data, then the contents of R9 are restored back to the AC.

xi) T. This register is used for all double pre - cision instructions and for the multiplication routine.

3.3.2 The data buses connected to the ALU

The bit-slice processor employed provides five buses for communication with the memory and the I/O devices. To provide a flexible system but with fewer interconnections, the buses have been allocated as follows (see fig. 3.4):

i) The data bus

While the 3000 CPE provides independent buses for the data input and the data output, both have been combined in one bidirectional bus controlled by the microbit EDB (enable the output buffer of CPE, i. e. output data to the data bus).

ii) The memory address bus (MAB)

As will be discussed in subsection 3.3.4 the program store and the data/constant store are separate. The MAB transmits the MAR data to the address inputs of the main program memory. There is a facility to address 64K of store, but as the program size for a dedicated purpose relay is unlikely to exceed 2K, only 11 bits of the MAB have been used.

iii) The flag-input bus

The I-bus of the CPE is used to test status flags from peripheral equipment. Only the data ready flag of the data acquisition unit (fig. 3.1) is checked at the present relay.

The other buses shown entering the CPU in fig. 3.4 carry control signals from the microprogram and will be discussed in the next subsection.

3.3.3 The control section

In a typical microprocessor the control section, that is the part of the computer which generates the required timing pulses at the right instants and selects

the correct functions to control the different devices is fixed by hard- wired logic by the manufacturer.

In the 3000 series family, the control section is defined by microprogramming an idea originated by Wilkes[27]. Microprogramming is a technique for designing and implementing the control function of a computer as a sequence of control signals (microinstructions), to interpret data processing functions (macroinstructions). Many big computers[28] have been built around this principle.

The main merits of a microprogrammable machine are: a) customised instruction sets suited to a particular application. b) ability to change the system performance with less hardware modifications. c) higher speeds can be achieved and d) less macroprogram locations are used as subroutines can be implemented as one new instruction residing in the micromemory. Further information about microprogramming can be found in ref. 29.

In designing a microprogrammed system, the following design factors are involved:

i) The choice of a suitable microprogram sequencer (MPS), to generate microprogram addresses unconditionally or conditionally based on the flag status, to control the carry/shift data and the interrupts. Although many MPS s are available, the one chosen[30] needs the minimum number of microbits for its control but at

the expense of a more complicated architecture. Fortunately most of the microprograms required were comparatively short and by modular programming this limitation did not introduce any problems.

ii) The selection of the microinstruction word length so as to control efficiently all the available devices. To retain the high speeds available by the bipolar construction of the MPS, bipolar PROMs [31] were employed for the micromemory (fig. 3.5). It was found that 30 bits were needed to control the PP of figure 3.4.

iii) The size of the micromemory depending upon the number and type of the available macroinstructions. The employed MPS can address directly 512 locations. The micromemory is segmented into two parts. The first block of 256 words contains the standard instruction set while in the second block the extended set of instructions is stored.

iv) The way the microbits are grouped to form a field and the type of microprogramming employed, i.e. horizontal or vertical. Horizontal microprogramming is used when the microbits control a device directly, while vertical microprogramming is used when the bits are decoded. In most cases horizontal microprogramming is required. Vertical microprogramming is normally applied, when in a group of bits, only one output can be active

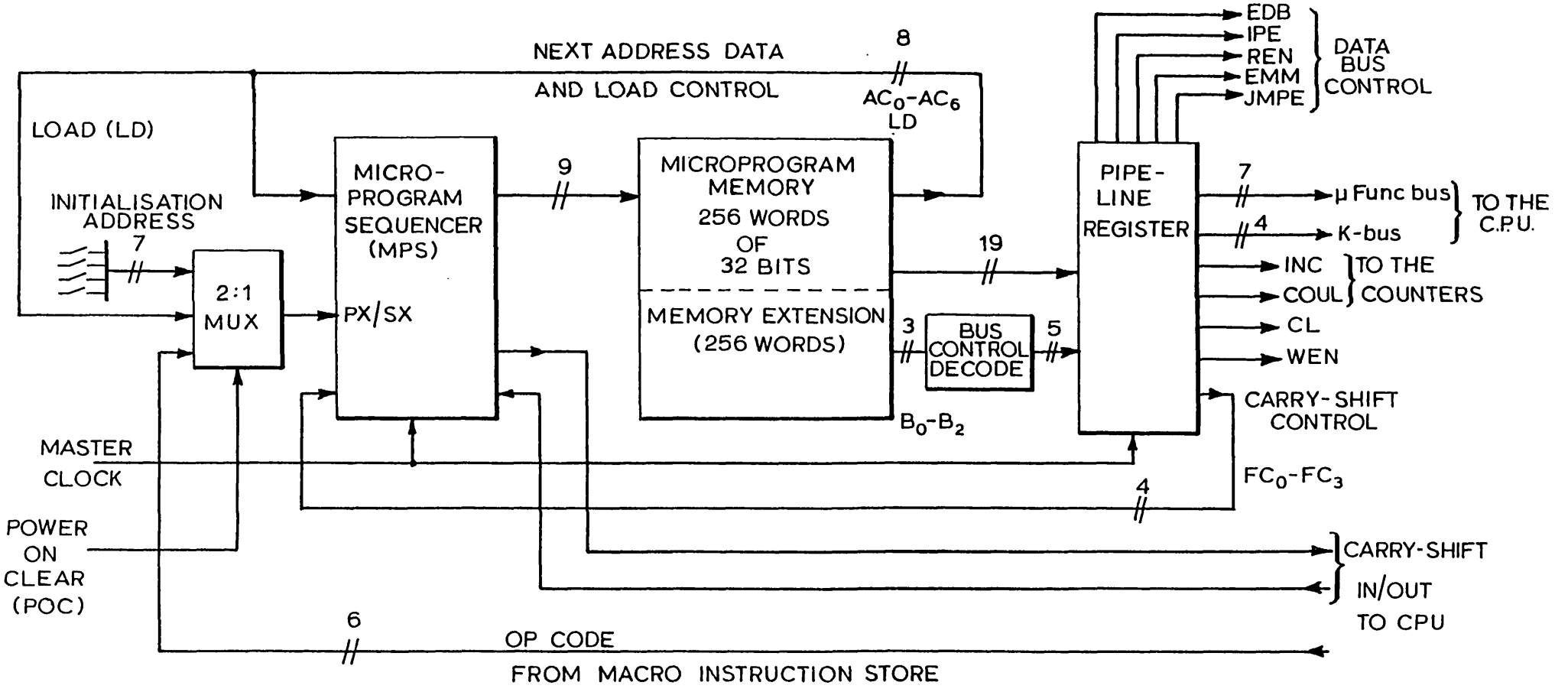


Fig. 3.5 Processor micro-program control module.

at any instant, thereby reducing the length of the microword. This has been used for the bus data control (see fig. 3.5), where only one device at a time can have access to the data bus. The microbit grouping can be seen from the table 3.2.

v) The choice of a pipeline or non-pipeline mode. In fig. 3.5 the pipeline registers are shown. By using them the processing time can be speeded up by 30%, as fetch and execution can be accomplished in parallel.

The way a typical macroinstruction is executed by a sequence of microinstructions can be obtained from ref. 4.

TABLE 3.2

DEFINITION OF THE MICROPROGRAM BITS

F_0-F_6	INC	K_1-K_4	CL	X	COUL	WEN	B_0-B_2	FC_0-FC_3	LD	AC_0-AC_6
31-25	24	23-20	19	18 17	16	15	13-12	11-8	7	6-0

F_0-F_6 The micro-function bus (μFunc. in fig.3.4) selects the ALU function. The possible binary values are fixed by the manufacturer and given in ref. 25.

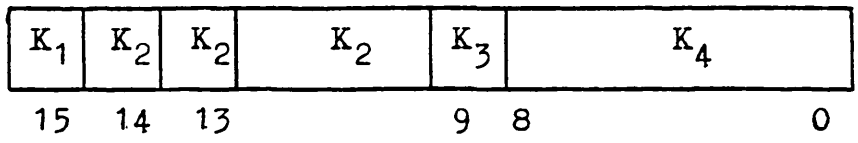
INC is used to increment the counters addressing the data store (subsection 3.3.5).

Table 3.2(cont'ed.)

K_1-K_4	The K-bus, which controls the ALU, but its length is defined by the user. Its purpose in the present design is to mask portions of the data word at the microprogram level. Its functions are given in table 3.3.
CL	Clock latch (signal ② in fig. 3.4), provides a clock to the macroprogram pipeline register, when a fetch is required (subsection 3.3.4).
X	Not used.
COUL	is used to load the data present in the subaddress bus into the counter by addressing the data store.
WEN	The write pulse for the data store and the output ports.
B_0-B_2	Data bus control enables one only device to be connected into the data bus. For its definition see table 3.4.
FC_0-FC_3	Flag logic control inputs to the MPS, defined by the manufacturer (see ref. 30).
LD	Load signal. When this signal is high, it forces the opcode from the macroinstruction store into the microprogram address register of the MPS. It is used to define the start of the next macroinstruction to be executed.
A_0-AC_6	Next address control function inputs to the MPS, fixed by the manufacturer. (see ref. 30).

TABLE 3.3

THE K- BUS DEFINITION



K_1	K_2	K_3	K_4	Function
0	0	0	0	Select the whole word (16 bits)
0	0	1	1	Extend sign of A/D data.
0	1	1	1	Select word sign or range bit 1.
1	0	0	0	Select magnitude of the word.
1	0	1	1	Select range bits 2,3.
1	1	0	1	Select sign of the A/D data.
1	1	1	0	Select A/D data magnitude

TABLE 3.4

THE DATA BUS CONTROL DEFINITION

B_0	B_1	B_2	Function
0	0	0	No device connected.
0	0	1	Enable the input port (IPE).
0	1	0	Enable the subaddress field of the macromemory (JMPE).
0	1	1	Enable data/constant store for read (REN).
1	0	0	Enable data output of the CPU (EDB).
1	0	1	Enable the masking memory (EMM).
1	1	0	Not used.
1	1	1	" "

3.3.4 The main memory section

In conventional computer architecture there is no distinction between the section of the memory where the instructions are stored and the section where data are stored. Such a structure involves a time consuming program counter control.

Taking into account the size of an application program (not exceeding 2K) and that no more than 1K of constant/data words are needed, then the most efficient and simplest way is to split the two memories as shown in fig. 3.4. To achieve this the instruction word has to be divided into 2 fields, one 6 bits wide to define the op code routed to the MPS and the other 10 bits long to define the address to the data store, and the next program address in a case of an unconditional jump. This procedure will be discussed in subsection 3.4.1. By this means the program counter controls only the main program sequence, while the addresses for constants and data are defined in the subaddress field.

As the main store is to be 2K x 16 bits a low cost, high density, low power memory is favoured. In addition a PROM has to be employed, otherwise the programs will be lost during power failures. The PROMs employed are the 2708 EPROMs [32], which provide erasing capability, so that reprogramming is possible, if changes are required. However, there is a time penalty introduced,

because these devices are of the MOS type. That is, at least 2 microcycles are needed to access them. For most of the instructions, during the program memory access time, 2 microcycles have already elapsed for the required control actions, but for short- lenght instructions and during skip instructions when the skip criterion is valid, a delay of 400 ns is introduced.

A pipeline register driven by the microbit CL, has been used to speed up the macroinstruction execution time (same action as in the micromemory).

For some of the instructions, the subaddress field contains data to be processed by the CPU, thus bus drivers have to be used for the 11 least significant bits. The drivers have access to the data bus when the signal JMPE is set. (fig. 3.4).

3.3.5 The data and constant store

The data/constant store is addressed by the 10 least significant bits of the macromemory, therefore a maximum of 1K data/constant words can be accessed. Some of these addresses have to be reserved for the I/O ports. The 1K store is split into data and constant memory depending on the application, but usually the data store size is greater than the constant store size.

As in the present design each data and constant store can address 256 locations, arranged in blocks of 64 words[33,31] the rest of the data/constant memory can

still be employed, but the locations 377, 777, 1377, 1777 cannot be used to address the data store, as these are reserved for the I/O ports.

Fig. 3.6 shows the data/constant store architecture. The primary address decoder shown, is implemented by a PROM, to reduce the number of components. Its purpose is to select one of the eight data/constant modules. The data of this PROM are shown in table 3.5.

Four control bits from the micromemory are needed. WEN and REN control the write and read modes. As the RAMs have an access time of 450 ns, during the microcoding care must be taken to leave sufficient time (3 microcycles) for this purpose. Because of the MOS RAM access time, in many cases the decoding of some microinstructions have to be delayed by one or two microcycles.

The signals COUL and INC control the 8-bit counter. The reason for introducing this counter is to enable addressing of more than one successive location by a single macroinstruction. Hence the subaddress field specifies the first address of the block to be accessed, while the following ones are fetched by successively incrementing the specified address stored in the counter. The number of words accessed is defined either inherently by the macroinstruction or it is defined previously by another instruction(see subsection 3.4.4.). An 8-bit counter has been used, permitting the address of the first

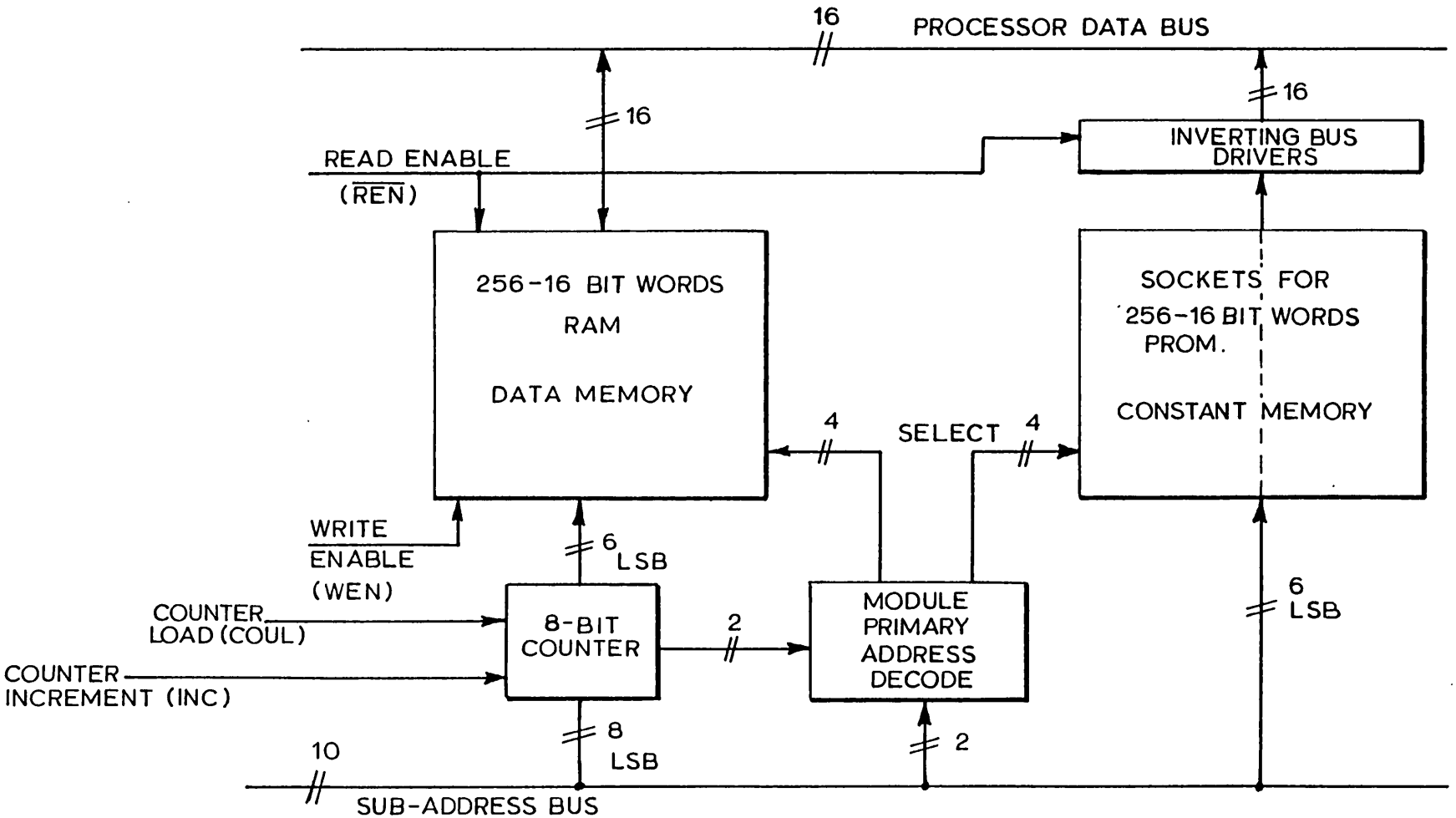


Fig. 3.6 Data-constant memory module.

256 locations, this limitation being taken into consideration when the application program was written.

TABLE 3.5

DATA/CONSTANT STORE DECODER

Address	Data	Function
0000	01111111	RAM 1
0001	11011111	RAM 2
0010	11110111	RAM 3
0011	11111111	Not valid
0100	11111101	RAM 4
0101	10111111	ROM 1
0110	11101111	ROM 2
0111	11111111	Not valid
1000	11111011	ROM 3
1001	11111110	ROM 4
1010	11111111	Not valid
⋮	⋮	⋮
1111	11111111	Not valid

3.3.6 The bit test masking memory

In fig. 3.4, next to the data/constant store, the masking memory is shown, which permits the masking of any of the 16 bits in the macromemory level. (to be distinguished from the masking K-bus at the micromemory level.). By introducing this additional memory, a bit can be tested and a decision can be taken depending on its value. This permits great flexibility and time saving in the application program.

The counters and the masking memory were not included in the initial processor design. They have been introduced later with no major hardware modifications at a very short time. This demonstrates the flexibility of this processor, stemmed from its microprogrammability.

3.3.7 The data input port

The purpose of this port, shown in fig. 3.4, is to input data from the DAU to the PP.

To speed-up the operation, another pipeline register has been used, controlled by the signal LD. Its operation has been discussed previously in the subsection 3.3.3.

Two types of instruction to input the data are possible: a) IDM inputs one word at a time in the location specified by the subaddress, while b) IDB, inputs a block of data (this instruction is discussed in the subsection 3.4.4.).

3.3.8 Circuit breaker control

At the end of each sampling interval a decision has to be taken according to the protection and processor status. These decisions are:

a) Trip relay healthy i. e. an internal fault has been detected and the processor is working properly.

b) No trip- relay healthy i. e. normal operating conditions.

c) No trip- relay failed i. e. the self-test monitoring program has found that there is a failure in the actual hardware.

To achieve better reliability at this critical stage, the following words have been assigned for each operation[4].

0101...01	Trip-relay healthy
1010...10	No trip-relay healthy
Any other	No trip-relay failed.

These words are stored in a 16-bit latch assigned to the address 377_8. The above words are decoded by a PROM, and the decision is stored in the CB status and in the relay status latches. The CB status is provided directly as a trip signal to the CB, while the relay status is transmitted to the monitoring computer for further processing according to the employed digital protection scheme.

3.3.9 The data output port to the monitoring computer

The purpose of this port is to output data to the monitoring computer, where further processing is continued. Therefore before outputing a block of data, an identification word is transmitted which selects the corresponding service program resident in the monitoring computer. With this facility, fault reports can be typed or the relay performance can be tested by plotting the primary circuit waveforms. The address assigned in the communication port is 1777_8.

3.3.10 The clock generator

The clock pulse generated is used to control the fetch and execution of the microinstructions. By taking into account the timing specifications of the CPE[25] and the MPS[30] the application note of reference 34 enables the clock pulse requirements to be found depending upon the design.

A microcycle takes 200 ns, being in the high state for 150 ns and in the low state for 50 ns whilst the write mode occurs in the CPE. For better stability, the clock generator has been built with a crystal controlled oscillator running at 19.6608 MHz. The clock generator provides a start-up facility i. e. following the initial switching-on it starts always from location 0 of the application program.

It also provides a single- step capability for

both, micro- and macrolevels, thus facilitating tests during the debugging stage.

Appendix 2 gives the circuit details of all the above discussed modules of the protection processor.

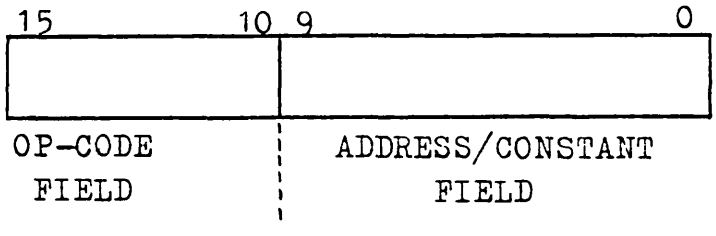
3.4 The instruction set

Because the processor is microprogrammable, the instruction set is defined by the user. The basic instruction set has been devised around a typical single Accumulator processor (PDP-15). In addition some other instructions, which by experience have been found useful to be included in the basic assembly instruction repertoire (like SBS, WFS, EXS) have been written.

The initial application program design has been started by employing these instructions, but during the program development, it has been found that new instructions could be introduced (the extended set), to improve performance, accuracy, timing and the number of memory locations.

3.4.1 Instruction format

In subsection 3.3.4, the reason for splitting the 16- bit word in two fields, as shown below have been discussed.



Therefore 64 ($=2^6$) instructions can be defined. This is not a serious limitation, as at the present time 52 instructions have been written, permitting 12 more to be added.

The address/constant field may contain:

a) a main program jump address. Ten bits permit addressing of 1K store, therefore two unconditional jump instructions have been written, i. e. JLP which addresses from $0-1777_8$ and JHP which addresses from $2000-3777_8$. During the execution of a jump to subroutine instruction (JSR), the first instruction of the subroutine must always lie in the low page ($0-1777_8$).

b) a data/constant memory address

c) an input/output port request.

d) a constant (immediate addressing).

The instruction set is divided into 4 groups according to the following operations:

a) <u>The control group</u>

These instructions control the processor status, i. e. Halt, Reset, etc.

b) <u>The operate group</u>

These modify the register contents, mainly the AC.

c) <u>The memory reference group (MRI group)</u>

These transfer data from/to the data store or

input/output ports and execute a logical or arithmetic operation. The final result might be left in the AC or stored in the same location in the data memory that the data originated.

d) Skip-jump group

Instructions in this group permit conditional or unconditional jumps to other parts of the main program.

Table 3.6 lists the available instructions in the 4 groups and gives their execution time.

3.4.2 Microcoding of the instructions

In fig. 3.5 the op-code bus is connected to the PX/SX-bus. The data on this bus defines the address of the first microinstruction of the corresponding macroinstruction. Because the microprogram address space is organised as a two- dimensional array, to keep the microprogram flexible all the macroinstructions are started from one of the columns 0,1,8,9 and from the rows 0 up to 15. Then the macroinstruction is decoded if possible to a single row, otherwise it continues to the next one, always keeping in mind the restrictions imposed by the selected MPS (see Ref. 30). The macroinstructions of the extended set start also from one of the above mentioned locations, but the rest of the microinstructions are contained in the second bank of the micromemory, i. e. from 256 to 511.

TABLE 3.6

THE INSTRUCTION SET

(in parenthese the execution time in μs is given)

CONTROL	OPERATE	MRI	SKIP/JUMP
HLT	CLA (0.8)	ADD(0.8)	JHP(0.8)
NOP(0.8)	COM (0.8)	AND(0.8)	JLP(0.8)
PAU(1000n)	CSL (1.2-1.4)	DPA(2.8)	JSR(1.2)
RST(1)	DEC (0.8)	DPS(2.8)	RET(0.8)
WFS(1+nx0.6)	DMR (2.6+(n-1)x0.8)	DSZ(1.4-2)	SAD(1.4-2)
	EXS (1)	DZM(1.0)	SBC(1-1.4)
	INC (0.8)	FMU(2.4+nx0.7)	SBS(1-1.4)
	MSL (1+(n-1)x0.6)	IDB(n+0.8)	SNA(0.8-1.4)
	MSR (1+(n-1)x0.6)	IDM(0.8)	SND(0.8-1.4)
	NEG (0.8)	ISZ(1.4-2)	SPA(0.8-1.4)
	SHL (0.8)	LDA(0.8)	SPD(0.8-1.4)
	SHR (0.8)	LDL(0.8)	SZA(0.8-1.4)
		LMB(2.4)	
		LTR(0.8)	
		LRA(1)	
		MUL(17)	
		SMB(2)	
		SRA(1)	
		STA(0.8)	
		STT(1)	
		SUB(1)	
		SUM(1.4)	
		XOR(1)	

n is specified in the subaddress field. In WFS, n depends on how many times the program stays in the loop, waiting for the flag to set. In FMU, n is the number of digits after the binary point.

Other design factors considered, when writing new macroinstructions are:

a) Two microcycles must elapse from the instant the MAR has been updated to the instant a new macroinstruction can be fetched.

b) Many macroinstructions can share the same microinstructions, therefore saving in the micromemory space can be achieved. By so doing the number of locations occupied in banks 1 and 2 are 162 and 123 respectively, hence only 285 of the 512 locations are used for the present set of the 52 instructions.

c) All the macroinstructions finish with a jump to location 15, 14 or 13, depending on the type of instruction (i.e. if saving or restoring of the AC is needed) and on the number of microcycles executed after the instant the MAR has been updated.

As the microprogram is resident in bipolar PROMs , erasing is not possible. Therefore great care has been taken during debugging (see also section 3.5), to ensure a correct set.

3.4.3 The basic instruction set

The basic instruction set includes addition, subtraction, logical addition, exclusive or, shifting and many conditional jumps. The only way of accessing the memories is by direct addressing and one level of subroutine only is permitted.

In appendix 3, the description format and microcode of this set are given.

3.4.4 The extended instruction set

This set contains more specialised and complicated instructions and a more detailed explanation is essential. This set is divided into three categories:

i) Double- precision arithmetic

Multiplication (MUL) of two 16-bit numbers will generally result in a product of more than 16 bits. The way the product is handled depends on the operation followed and on the accuracy required.

There are many methods available to implement binary multiplication[35] the most popular being Booth's algorithm[36] or " adds and shifts ". By taking into consideration the limitations of the CPE (multiple masking and shifts not available), then it has been found that by keeping track of the signs and magnitudes and by adding and shifting the multiplication of 2 16-bit numbers can be executed in 17 μs. This has been achieved by keeping the multiplication loop as short as possible having latched the multiplicand onto the data bus continuously.

As the processor handles only integer numbers, if multiplication is needed by a fractional constant (for example in digital filtering), then this needs to be implemented by adding and shifting to the right.

To avoid time- consuming operations, the fractional multiplication (FMU) instruction has been introduced. To improve the accuracy and to save still more processing time, the number of bits after the binary point is defined. The program needed is:

```
LTR  x      ; x=number of bits, after the binary point
              (as a negative 2's complement number)
LDA  y      ; y=Address where the positive fractional
              constant is stored.
FMU  z      ; z=Address of the data to be multiplied.
STA  w
```

To calculate the reactance and resistance of a transmission line, division is also needed. The most commonly employed method[35] is non-restoring, because it handles negative numbers without any modification. For this purpose, the processor should have the ability to shift to the left two registers, otherwise the division becomes time consuming. Such a facility is not provided in the employed microprocessor, therefore the division has not been implemented so far, but the trip decision is taken without division, as discussed in chapter 5.

In the application program there are successive multiplications, and it is possible to reach a point where a number greater than $2^{15}-1$ has to be multiplied by another. This problem has been solved by scaling, implemented by double-precision multiple shifts to the right (DMR).

The specified number of shifts depends on the size of the number, therefore accuracy is not impaired. The use of a multiplication routine which handles more than 16 bits will be the ideal solution, but as will be seen in chapter 5, the error introduced by the scaling is quite small.

Addition (DPA) and subtraction (DPS) are straightforward operations, therefore their implementation in double precision does not involve any complexity and accuracy is maintained.

ii) Transferring blocks of data

In many parts of the program, during execution of subroutines a block of 3-words has to be transferred in a common section addressable by the subroutine. For each such operation 6 program locations are needed. Improvements in the timing and in the number of locations has been achieved by using the instructions LMB, SMB where each data block consists of 3-words. A more flexible implementation, which handles a variable number of words from 2 - 6, increases the complexity of the microprogram, the size of the micromemory required and the execution time.

For comparison of the corresponding samples of successive cycles, the data samples are stored in different locations. The instruction IDB (input data block) accomplishes this by using the program:

LDA N ; N=number of data samples

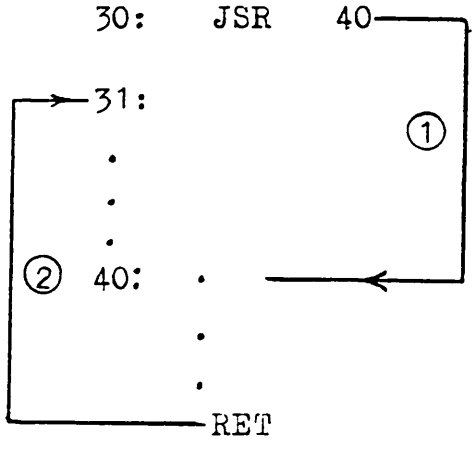
IDB A ; A=Address in the data store where the first data in the block sample will be stored.

The following addresses in the data store are accessed by incrementing the counter (fig. 3.6).

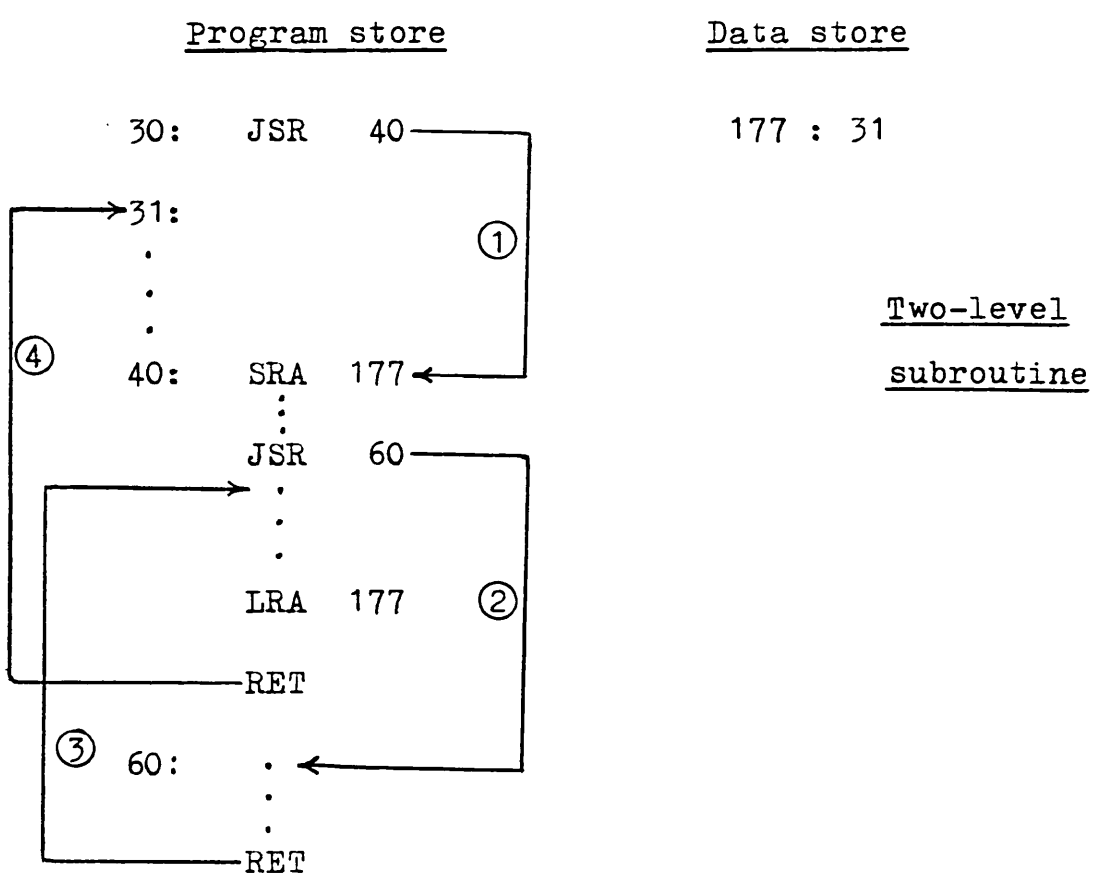
iii) Additional addressing modes

To execute nested subroutines, a method of storing the return address of the higher priority subroutine is needed. This is done by transferring the contents of R7 (subsection 3.3.1) to the data store (SRA), then executing the subroutines and finally reloading them back into R7 (LRA).

The operations for a single-level and a 2-level subroutines are shown below:



single- level



Indexed addressing[37] is quite useful for addressing different locations in the program memory arranged with equal spaces between them. For example such a program could be the accessing of successive data samples, as in the following program, i. e. in the first sample location X is addressed, while at the next one, location X + 2 is addressed and so on.

```
X:    LDA   2
      JLP 241      ; go back into the main program
X+2:  LDA   3
      JLP 421
```

For implementation a program which controls such

a procedure is produced by an indirect indexed addressing, thus:

```
ISZ     y   ;   y is a location in the data store with
ISZ     y       initial value X-2. Instead of assigning
                a separate index register to indicate the
                required step, the data is incremented
                and stored directly in the data location.
                Therefore the indexing has been accomp-
                lished.

LRA     y   ;   This is the indirect step, because the
RET             address/constant field specifies the
                address of the next jump address. When the
                instruction RET is executed, the program
                jumps to the location X.
```

To close the loop, the value of y has to be checked[37]. If it contains the last address in the program block, then location y has to be reset to its initial value.

The above group of instructions can be written in a microprogram, and one instruction can implement the indirect indexed addressing mode. Such a procedure has not been considered necessary for the present program, because it is not used extensively.

3.5 Development and testing support

The development and testing of a microprocessor-based system is quite different from that required for a simple digital circuit. The complexity involved at

this stage stems from the fact that 16 channels of data have to be checked simultaneously plus some other control signals. In addition the system has to be checked as an integral unit, i. e. hardware and software working together. Sometimes it is difficult to identify if the maloperation of the unit is caused by hardware or software errors.

To build-up the system, additional aids are needed as PROM simulators, PROM programmers and cross-assemblers.

In the following these aspects will be discussed. In this microprocessor, with its two levels of programming (micro- and macro-), the development stage becomes more complicated.

3.5.1 Development aids at the micro-level.

Once the actual hardware has been built and any wiring errors corrected, the power supplies have the specified polarity, level and ripple, there is no improper selection of components and no improper timing specifications, then the system is ready for testing.

To ease the testing of the microinstructions, a bipolar PROM simulator is necessary, having a RAM memory with access time similar to that of the PROMs for the micromemory. Data into the RAM is written by selecting suitable switches on the control panel. Loading of these data through a minicomputer is unnecessary as

most of the microprograms are short. For this reason the employed simulator is 16-word deep, 32-bit wide. By connecting the simulator through a cable to the sockets of the micromemory, the actual debugging of the microinstructions can be accomplished. Macroinstructions decoded in more than 16 microinstructions can be tested in parts.

The next step is to generate the 32-bit binary code corresponding to each microinstruction. A cross-- assembler has been written in the NOVA 1210, which permits the generation of the binary data for all the specified fields.

The final stage is to transfer the data into the PROM. For this purpose a bipolar PROM programmer has been constructed, which generates the required pulses to program the PROMs.[31] More details about the above aids are given in Appendix 4.

Needless to say that during the testing stage logic probes and a fast oscilloscope are necessary. If a logic analyser[38] is available, with its sophisticated timing analysis, then the fast solution of many logic problems is possible in a microprocessor-system.

In the present design, a single-step mode and a means of resetting the system and restarting its program, together with a display of the microaddress and data bus are provided.

3.5.2 Development aids at the macro-level

Once the microprocessor is working satisfactorily with some small test programs, most of the expected errors will be software errors in the main program.

A cross- assembler for the devised instruction set has been written which generates the 16-bit binary code. This assembler is of the pass one type, hence mnemonics for the address/constant field cannot be used. Finally the binary data generated have to be transferred into the EPROMs . To accomplish this another programmer driven by the NOVA 3 has been used, therefore the EPROMS[32] programming procedure is different from that of the bipolar PROMs, thus another type of programmer is necessary.

The employed EPROMs are guaranteed for 15 erasures but for a large program it is better first to test it by using a MOS PROM simulator. This simulator works on the same principle as the previous one, but its RAMs are of the MOS type having an access time of 450 ns. In addition the data can be loaded from the NOVA 3, which speeds-up the operation tremendously. Another advantage of a computer-driven simulator is that all the tested versions of the program can be stored in a diskette for future comparison.

If the program does not operate properly, then

breakpoints can be inserted at the suspected locations by storing there a HLT (modifications in the program already stored in the simulator can be done easily through its control panel.)When the processor halts, the data on the data bus is the contents of the accumulator. An additional display of the macroprogram address is provided.

If a minicomputer is available a more advanced development system[39,40] can be used, which tests more efficiently the performance of the microprocessor. The facilities provided by such a system are:

a) A part of the program already tested can be contained in the EPROMS, while the one tested for the first time can be resident in the simulator.

b) During a breakpoint, a printout of the microprocessor state is possible, therefore the programmer can have information about the program flow.

3.5.3 Aids needed for field service

There are many tools which can locate failures in the system, in the field. Some of them rely on signature analysis techniques[41], in which each mode of the processor is assigned a special state called signature. There is a possibility of 99.998% of detecting an erroneous data stream. But such a procedure needs some special features to be taken into account during the design stage. The great advantage of this technique

is that testing can be achieved by a simple portable device and with minimum personnel training.

Other methods are based on software testing techniques[42]. Using such methods the response of the processor can be compared with what it should be. These methods can be of the self- diagnostic type in which, for each module of the processor, a test is performed, e. g. CPU functions, I/O testing, memory testing.

The PROMs can be tested by comparing their contents with the contents of a master copy, while a RAM can be tested with algorithmic pattern generation.

In the present application program the following tests are executed during the normal protection calculations:

a) The correct operation of the data acquisition unit and its power supplies is checked every sampling interval.

b) The three voltages and currents are checked at the relaying point, which gives a rough idea about the integrity of the whole system.

c) If the power flow at the relaying point is known by other measurements, then by comparing the corresponding values computed by the relay, it can be seen, if the impedance algorithms are working properly.

Further diagnostics can be included. However

they cannot be executed during normal operation, because they need considerable processing time. If their execution takes less than a sampling interval, then one solution is to steal one sample during which the normal protection operation is replaced by the diagnostic execution. This can be done over regular intervals or upon a request from the operator.

CHAPTER 4

DISTANCE ALGORITHMS

4.1. Introduction

The purpose of a distance relay is to measure the impedance of a line up to the fault point. To achieve this by digital techniques, an algorithm has to be employed which calculates the line characteristics continuously.

When a disturbance occurs in a power system network, the digital distance relay should calculate the measured impedance in a short time interval, preferably less than 20 ms. This is difficult to achieve, because a sudden change in the state of a power system alters the network stored electrical and magnetical energies. As a consequence the voltage and current waveforms are considerably distorted.

The main transients components generated after a fault disturbance are:

i) a d.c. decaying exponential and

ii) a band of high frequency oscillations having varying amplitudes. These can appear in both, the voltage and the current waveforms, but in general (i) appears mostly in the current waveform and (ii) in the voltage.

4.1.1. The d.c. exponential component

When a fault occurs on a power system, a d.c. component is generated to satisfy the physical condition of zero current change at the instant of the fault.

If the capacitance in fig. 4.1 is neglected, the instantaneous value of the primary current is:[46]

$$i_p(t) = \frac{E}{Z}\left[\sin(\omega t+\alpha-\varphi)-e^{-t/T}\sin(\alpha-\varphi)\right] \qquad (4.1)$$

where $\dot{Z}=\dot{Z}_S+\dot{Z}_L = Z\angle\varphi = R+j\omega L$

α = angle after zero voltage, at which the fault occurs

and $T = L/R$ sec.

By referring to the secondary side of the c.t. (fig.4.2)

$$v=-\frac{N_2}{N_1}\frac{E}{Z}Z_a\left[\sin(\omega t+\alpha-\varphi+\varphi_a)+\frac{X_a}{Z_a}\left(\frac{R}{X}-\frac{R_a}{X_a}\right)e^{-Rt/L}\sin(\alpha-\varphi)\right] \qquad (4.2)$$

As can be seen from (4.1) and (4.2), when $\alpha-\varphi=90°$, the d.c. offset has a maximum value. As in h.v. systems φ is close to 90°, this condition corresponds to a fault applied at approximately zero voltage. On the other hand the d.c. component vanishes when $\alpha \simeq \pi \div 2$

Equation (4.2) produces the conclusion that, if the burden of the c.t. is selected such that:

$$\frac{X_a}{R_a} = \frac{X}{R} \qquad (4.3)$$

Then the exponential term becomes zero.
As R/L includes the source and the line up to the fault point, exact cancellation is not possible. But the following conditions have to be considered:

i) for h.v. lines, it can happen $X_L/R_L > X_S/R_S$ which makes the ratio X/R of the primary circuit impedance Z almost identical to that of the transmission line.

ii) for accuracy the critical point in terms of discrimination is at the far end of the line. Therefore, matching can be achieved reasonably well, if X/R is composed of the source and 85% of the line impedance.

iii) the majority of short circuits in h.v. systems occur close to the voltage maximum, because in a flashover, the line potential is raised by induction until the sum of the induced potential plus the phase voltage exceeds the line insulation limit, which obviously will occur first on the phase nearest to the voltage maximum.

iv) in digital protection, an algorithm can be employed, which takes into account the exponential term.

Hence the error caused by the d.c. offset in the impedance calculation can be considerably diminished.

A d.c. exponential can be apparent in the voltage signal too. This component is not as serious as the

corresponding one in the current, because it vanishes, when:

i) $\varphi = \varphi_L$ i.e. $X/R = X_L/R_L$ or

ii) $\alpha = \varphi$ i.e. zero voltage fault incidence angle.

4.1.2. High - frequency harmonics

If a fault occurs at a voltage maximum, the electrical energy stored in the line capacitance discharges through the short circuit and the source impedance. On a transmission line with distributed line capacitance, travelling waves are generated after a fault occurrence. The velocity of those travelling waves, which are propagated along the line and reflected at the source and at the fault point, determine the dominant high- frequency oscillation. The propagation velocity depends on the distributed inductance, capacitance and resistance of the line.[47]

The dominant frequency will lie approximately in the range:

$$f_{hf} = \frac{1}{4\tau} \cdots \frac{1}{2\tau} \text{ Hz} \qquad (4.4)$$

where $\tau = \frac{l}{v}$ = travel time of the wave between source and fault point.

l = length of the line

v = line's characteristic propagation velocity =

$$\frac{\omega}{\sqrt{zy}} \simeq \frac{\omega}{\sqrt{xy}}$$

where $\dot{z} = r+jx$ = Impedance of the line/mile

and r,x,y = resistance, reactance and shunt susceptance respectively of the line/mile.

These two limits of f_{hf}, depend on the source impedance $\dot{Z}_S$

In a three phase system the travel time for phase faults(p.f.) and ground faults (g.f.) are different and different frequencies are introduced for p.f. and g.f. The ground surge is slower, therefore it introduces a lower frequency oscillation, i.e. clòser to the fundamental one and hence more difficult to filter.

In addition non- harmonics are generated, caused by non- linearities in the transducers.

The electromechanical relays are inherently low- pass filters. For static relay a filtering process has to be implemented.

In digital distance relays there are two ways to filter these frequencies:

i) by a suitable choice of analog and digital filter combinations, or

ii) allowing the algorithm to take directly into account these harmonics.

In the next section, a brief discussion of the available types of algorithm for distance protection and their properties will be given.

4.2. Types of distance algorithms

Many types of distance algorithm have been proposed, but their performance depends on the sampling rate, the filtering provided and on the applied conditions.

An extensive study of their frequency- response, magnitude characteristics is given by Ranjbar.[48]

A survey of some of the present algorithms, which compares and evaluates them according to specific criteria, has recently been published by Gilbert et.al.[49]

Generally these algorithms can be divided into five categories, according to the way they perform the impedance calculation from samples of voltage and current waveforms. A brief discussion of these methods and their problems are given below.

4.2.1. The $\dot{V}=\dot{Z}_L\dot{I}$ method

One way to describe the transmission line parameters is by using phasors i.e. $\dot{V}=\dot{Z}_L\dot{I}$ (fig.4.3). Such a description is valid only for a steady- state condition. Under transient conditions, however, the presence of d.c. and high- frequency components will produce errors in the impedance calculations.

Such methods are:

i) The peak determination method.[50]

This method finds the magnitude and the angle of

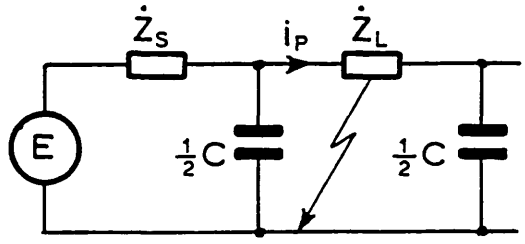
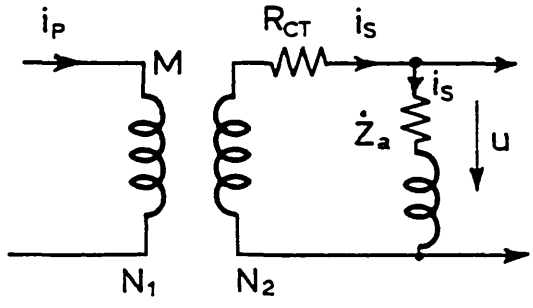


Fig.4·1 Equivalent circuit for one phase



R_{CT} = RESISTANCE OF THE C.T.

$\dot{Z}_a = R_a + j\omega L_a = Z_a \angle \Phi_a$ = BURDEN OF THE C.T.

Fig. 4·2 C.T. equivalent network

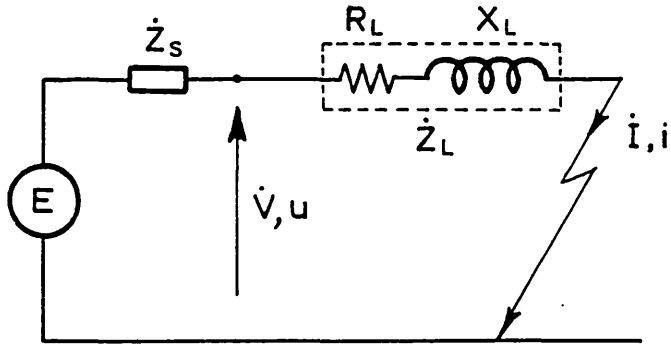


Fig. 4·3 Transmission line parameters

the line impedance, by the predictive calculation of peak voltage and peak current. To achieve this, the first derivative of voltage and current are calculated. This method is sensitive at the presence of high- frequency and d.c. components.

Rockefeller[51] suggested that the effect of the d.c. component can be reduced by using the first and second derivative of voltage and current.

To remove the high- frequency components, especially those close to the fundamental, a higher- - order filter with a low cut-off frequency has to be employed. Typically a third order 90 Hz filter has to be used.

ii) Fourier method[52,53]

By numerical computation of the Fourier series integrals, the complex value of the fundamental component of voltage and current can be extracted in rectangular form. The inherent filtering process of the Fourier analysis gives a slow but smooth and accurate response. While the Fourier method can remove the constant d.c., it cannot filter the exponential one, hence its accuracy is impaired.

Another approach to the online evaluation of the Fourier transform is described by Johns.[54] It needs a small window of information and is independent of the power system waveforms. In addition it enables the

measurement of the line impedance to be effected at any chosen frequency. The advantage of this method is that a trip decision can be reached in an interval of about 3/4 of a cycle after the fault inception, while the previous Fourier methods require about one cycle detection time.

iii) The square- wave method[55]

To reduce the arithmetic calculation, square waves (Walsh functions) can be used in place of the sinusoidal ones in the Fourier method. The response of this method is quite close to that of the Fourier approach.

4.2.2. The differential equation method

Another way to describe the transmission line parameters is by the equation:

$$v=R_L i+L_L \frac{di}{dt} \quad \text{(see fig. 4.3)} \qquad (4.5)$$

The great advantage of this method, compared with that of the section 4.2.1, is that eq.(4.5) is valid for both steady- state and transient conditions. Therefore d.c. offset and harmonic components are recognized as valid components. However, an error is introduced as eq.(4.5), neglects the shunt capacitive effect. For long transmission lines where the capacitance discharge becomes apparent as travelling waves, harmonics and nonharmonics are generated. In such a case a simple filter, which counts for these frequencies can

be used.

Some methods, which use this equation, are:

i) The McInnes and Morrison method.[56]

By integrating the equation (4.5) for the time intervals (t_0,t_1) and (t_1,t_2), where $t_1-t_0=t_2-t_1$ = 1/4 of a cycle, two equations can be obtained. From this pair of simultaneous equations, R_L and L_L can be calculated.

Another choice of the integration limits is mentioned by Ranjbar.[48] If the limits are $(t_k, t_k+T\frac{N}{2})$ and $(t_{k+1}, t_{k+1}+T\frac{N}{2})$, where T = 20 ms for a 50 Hz system and N the sampling rate, then all the harmonics can be considerably attenuated.

ii) The harmonic filtering method[57]

By selecting overlapping limits of integration chosen to eliminate low order harmonics and their multiples, a suppression of high frequencies can be achieved. For efficient and accurate calculation, the sampling rate must be a multiple of the positive harmonic order that is intended to be removed.

iii) Mean square error[58]

Equation (4.5) can be rewritten as:

$$L_L \frac{di}{dt} + R_L i - v = \varepsilon(t) \qquad (4.6)$$

Where $\varepsilon(t)$ is the error caused by shunt capacitance and noise. The principle of the method is to calculate R_L

and L_L by minimising the error function ε (t) over a period of time (0,t).

iv) Minimisation of errors over several intervals[58]

The same principle as above can be applied by dividing the interval into n parts and applying the same method. The final result is better than that of (iii), but the computation is time-consuming.

v) Solution of the differential equation by using first differences.[59,60]

In the McInnes method, equation (4.5) has been solved by integration. A simpler way to solve the differential equation is by converting it to a difference equation. This method requires the minimum of computation time of all previously mentioned methods and will be examined later in more detail.

4.2.3. Curve fitting methods

All previous methods have calculated R_L and L_L by using the raw samples of voltage and current with a possible prefiltering by analogue and/or digital methods. Instead, the samples could be fitted to a predefined waveform. Hence a new pair of voltage and current can be obtained, which are exact if the analogue signals change in the assumed manner. By employing different kinds of curve fitting, the following algorithms have been published:

i) Sinusodial curve fit[61]

This method fits the sampled data, to fundamental sinusoidal quantities, by using three consecutive samples. Hence it is sensitive to d.c. offsets and higher harmonics.

Another method proposed by Makino[62] uses two samples to calculate V^2, I^2 and $VI\cos\varphi$, where V and I are the magnitudes of voltage and current respectively and φ their phase difference. To achieve a better performance a combination of filters is employed to attenuate d.c. offsets and the higher harmonics.

ii) Least- squares fit

The real and imaginary parts of voltage and current can be calculated by using the sampled data being fitted to an offset sine wave with a second harmonic.[63]

Sanderson[64] employs a second order Polynomial curve fitting, prior to the inductance and resistance calculation. Equation (4.5) is used to calculate the impedance of the line.

4.2.4. Travelling wave method

After the occurence of a fault, transient travelling wave phenomena distort the waveforms of voltage and current . Some algorithms have been published based on travelling wave theory. Some of them rely on the relaying point data,[65] others on data from both ends of the line.[66]

The first paper by Vitins[65] derives the fault distance as a time delay between two quantities associated with the travelling waves at the relaying point. The other method by Takagi[66] derives an equation which is valid only for internal faults. Both methods seem promising because of the fast response, but they require a computation of some complexity.

4.2.5. Simulation of analogue relays

A recent paper by Mitani[67] simulates the conventional relay characteristics, such as mho or reactance, by employing digital techniques. A high-order digital filter is used to attenuate the d.c. offset and higher-frequency components.

4.3. Criteria for the choice of an algorithm resident in a microprocessor

The previous brief discussion indicates the large number of the available algorithms for distance protection. As has been mentioned the majority of them employ either a scientific or a process-contol computer.

Application of a distance algorithm in a fixed point arithmetic microprocessor implies some limitations. Firstly the accuracy of the computations will be impaired due to round- off errors. Techniques to improve these have been discussed in chapter 3. Secondly the program and data memory locations are limited. Extension of the memory is possible, but with a time penalty.

Thirdly its processing speed cannot be compared with that of large mainframe computers. The microprocessor employed here has a speed comparable to that of a minicomputer which affects the possible sampling rate.

Consequently a compromise has to be arrived at for the algorithm choice. From the point of view of microprocessor application, distance algorithms can be divided into two categories:

i) those that process a large number of samples covering a major portion of a fundamental cycle to extract information about the fundamental waveform. Although it takes longer to reach the new value of the impedance, it is reached smoothly because of the inherent filtering properties of the algorithm.

ii) those which have short data windows extending over a small portion of the cycle. As the number of the processed samples is small, they follow changes in the impedance faster than the methods of category (i). But as they might pass frequencies other than the fundamental one, their response is rather variable until they settle down to the correct value.

The most important aspect of a distance algorithm is how fast it will settle to the new operating conditions, after which the maximum permissible variations in the impedance must be about $\pm$ 5%. Its noisy response during the transient period will not

affect the trip decision, if a suitable strategy is applied. This will be discussed in the program organisation in chapter 5.

Methods belonging to category (i) need more processing time and more memory locations that those of category (ii). So for this application it was decided to employ an algorithm of the second category to accomplish distance measurement.

As time was not critical, a digital filter was used, to remove the higher harmonics. Instead of using another filter to remove the d.c. offset, it was better to use an algorithm which took it into account.

Two more reasons contributed to this decision:

i) The advantages of a non- switched distance scheme have been examined in chapter 2. These advantages apply also to a digital scheme. This implies that between two samples, six impedance algorithms have to be computed, producing continuous tracking of changes due to possible fault disturbances, to run this program in real time i.e. before the arrival of the next sample, a simple algorithm has to be applied.

ii) Experience has shown that considerable time is needed for the handling and modification of the data, in a form which can be used by the subroutines. So the calculation for the actual impedance has to be kept to a minimum.

4.4. The distance algorithms programmed in the dedicated microprocessor

A simple algorithm which can cope with the d.c. offsets can be obtained by solving the differential equation of the line using first differences.[59]

As has been mentioned earlier, for long h.v. transmission lines, a filter has to be used for any method based on this description because of errors introduced by travelling waves and other effects. Therefore instead of using the McInnes and Morrison-[56] method, which has inherent filtering properties due to the integrations, it was decided to use the simpler solution of the differential equation (4.5) with an appropriate filter.

At the next subsections the filter process and the algorithms employed are discussed.

4.4.1. The filtering process

A sampling rate which permits the execution of the algorithm has to be determined. The faster the sampling rate, fewer will be the numerical errors. It has been found that 8 samples/cycle[48] is a good compromise, as 2.5ms are available for the processing time.

It is well known in communication theory[68] that if an analogue signal is sampled, the conversion will be distortionless if the signal is bandlimited i.e. it does not contain frequencies greater than half the sampling

frequency. Otherwise an aliasing effect takes place which means that higher frequencies are folded back and appear as lower frequencies. This is caused by the sampling process at equally spaced points. Once the sampling has been performed, the effect cannot be mitigated.

The only way to avoid such a distortion is by ensuring that the analogue signal is bandlimited, by employing an analogue lowpass filter with a cutoff frequency less than the half of the sampling frequency, i.e. equal to the Nyquist frequency.

As the sampling rate is 400 times per sec., that means that the Nyquist frequency is 200 Hz, hence an analogue filter having a cutoff frequency of about 200 Hz has to be constructed. To ensure sufficient filtering, a second- order Butterworth active lowpass filter with a cutoff frequency of 180 Hz was implemented, using the design tables of ref. 69. The circuit details of the filter are shown in Appendix 5.

Such a filter was applied to all current and voltage waveforms sampled from the three-phase system. By using the group delay characteristics graphs of Butterworth filters[70], it can be shown that the group delay for the system fundamental frequency (50 Hz) is 1.376 ms.

The removal of the unwanted harmonics was accomplished by digital filtering. The voltage waveforms

are most seriously affected by the presence of higher harmonics, but both voltage and current have to be filtered by the same amount, otherwise a phase difference will be introduced. For the same reason, the filtering has to be done by digital, rather than analogue techniques. Analogue filters, because of the drift of the analogue components can have non- matched phase responses, i.e. different phase delays. To build analogue filter with low drift, expensive devices have to be used. As a digital filter is advantageous and processing time is available, digital filtering at this stage is preferable.

The filter used is a second- order Butterworth lowpass digital filter with a cutoff frequency of 120 Hz. The choice of such filter is based on the conclusions of reference 47 . By using equation (4.4) and the data of a typical 230 KV or 400 KV transmission line, it can be shown that for a line 300 miles long the highest minimum frequency will be about 124 Hz.

For a shorter line, this filter might be unnecessary, as the analogue antialiasing filter is present. Hence the relay has two options, i.e. if filtering is desirable, the digital filter routine is activated by a switch on the front panel of the relay. The group delay for a digital filter will be longer than that of an analogue equivalent. For the specific filter

the group delay at 50 Hz is 2.4 ms.

The transfer function of the digital filter is:

$$H(z)= a_o \frac{1+a_1 z^{-1}+a_2 z^{-2}}{1+b_1 z^{-1}+b_2 z^{-2}} = \frac{Y(Z)}{X(Z)} \qquad (4.7)$$

where $X(Z)$ = Z-transform of the input $x(t)$

$Y(Z)$ = Z-transform of the output $y(t)$

As the filter process has to be repeated six times for a three- phase system, a configuration which requires the minimum of data- memory locations was applied.
Such a configuration is shown in fig. 4.4., called " direct realization ". Its software realization in the microprocessor is shown in fig. 4.5.

The filter's coefficients have been calculated by using the bilinear techniques[72] and are:

a_o = 0.391336

a_1 = 2.000

a_2 = 1.000

b_1 = 0.369527

b_2 = 0.195816

Since most of the coefficients are fractional numbers, there are two ways of implementing them. One way is to generate them by multiple shifting additions and subtractions. The second way is by using the fractional multiplication command (see chapter 3). Both methods can only give approximated values of the

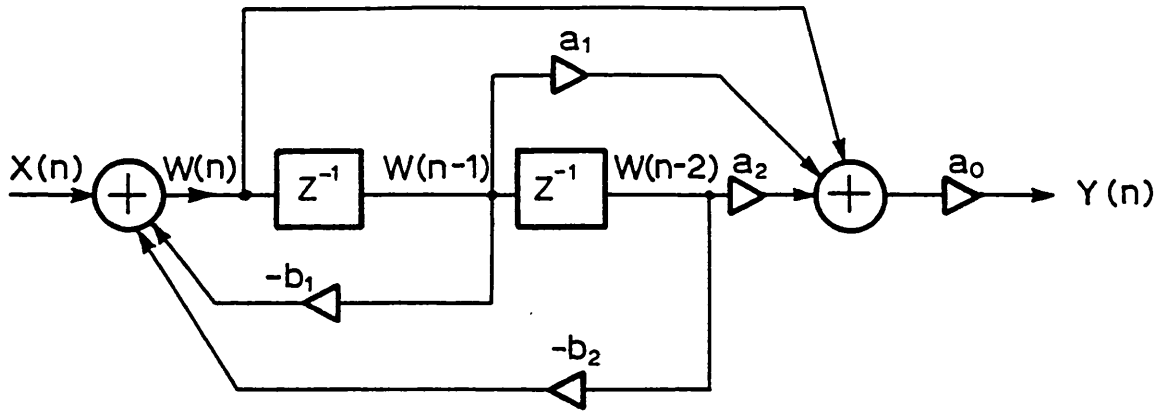


Fig. 4·4 Direct block diagram of the second-order digital filter

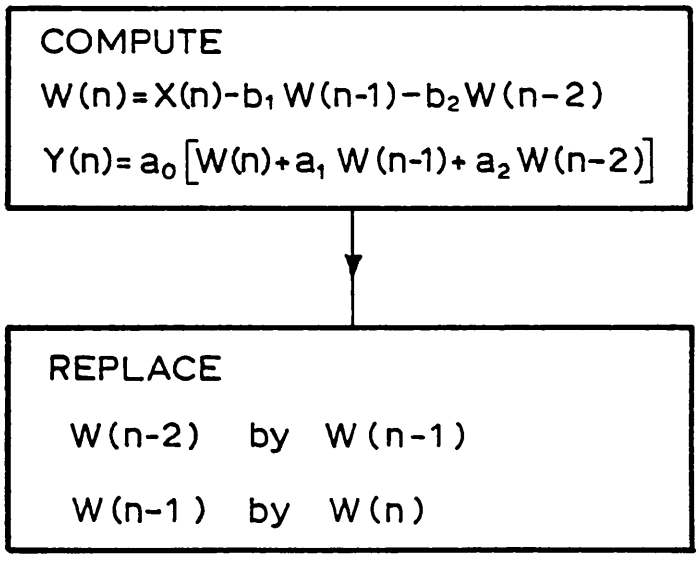


Fig. 4·5 Software realization of the digital filter shown in Fig. 4·4

coefficients. The second method is faster in execution, requires less memory locations and the approximated coefficients can be very close to the computed ones. The reason for trying to achieve a close approximation of the filter coefficients is that quantization of them is equivaltent to an additive source of noise. Such a process can affect the stability of the filter.[73] The filter's frequency response and impulse response can be seen in fig. 4.6, for the computed and the approximated coefficients. This approximation does not affect its performance significantly.

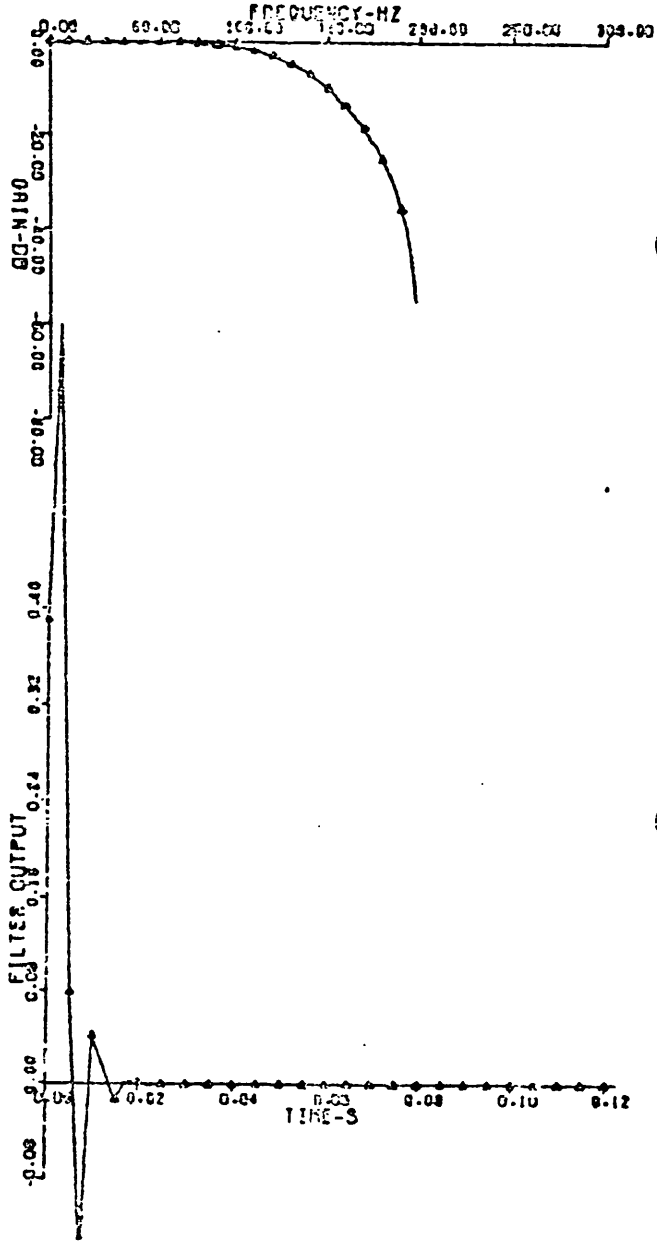
The approximated coefficients are:

$a_0 = 0.390625$

$b_1 = 0.369141$

$b_2 = 0.195313$

To demonstrate the ability of the filter to filter out higher harmonics, the oscillograms of fig. 4.7 have been taken by generating harmonics in the transmission line model used. The analogue signal is passed through the antialiasing filter, and then after the digital conversion is filtered by the digital filter implemented with the approximated coefficients in the microprocessor. It requires a processing time of about 45 μs for each signal at each sample. The harmonics shown in fig. 4.7 have been generated by connecting a 65 μF capacitor at the relaying point and applying a fault on



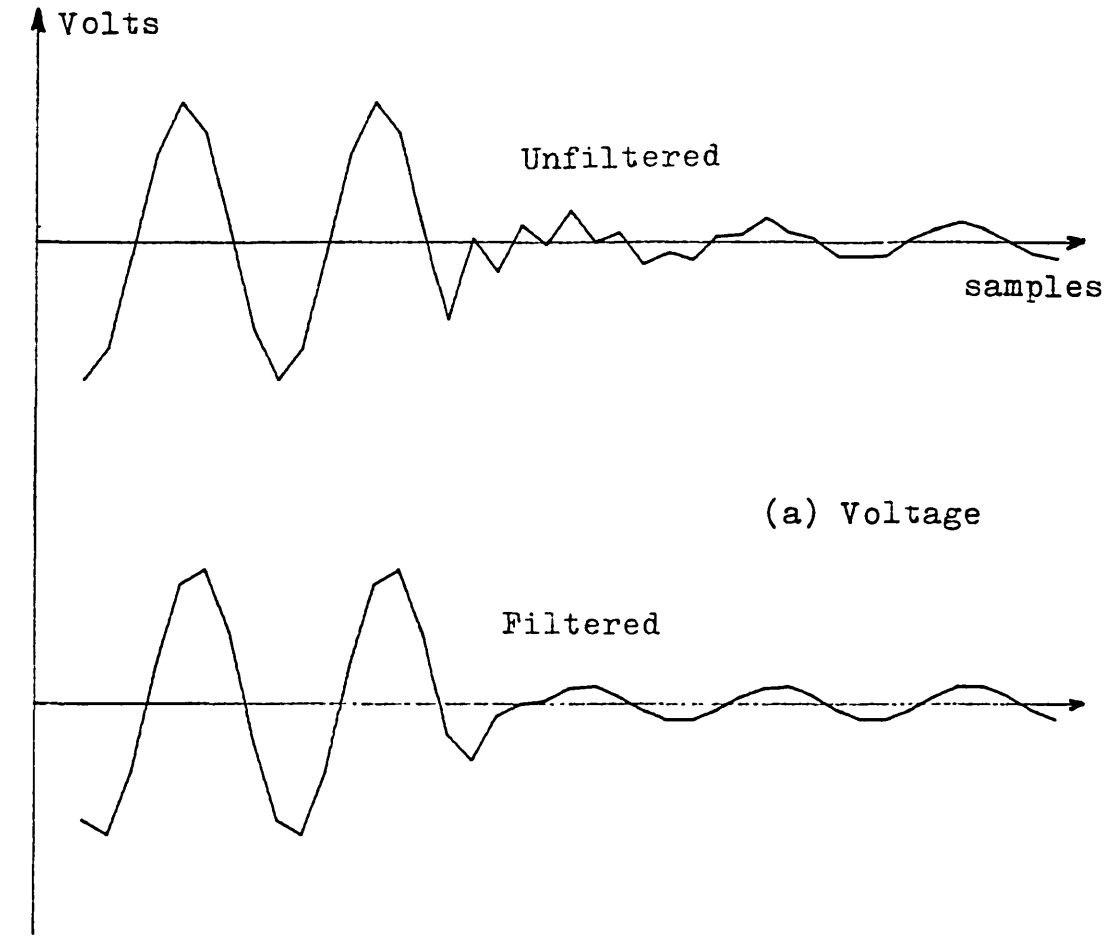
(a) Frequency- response

(b) Impulse- response

Fig. 4.6 The digital filter responses

—— Computed coefficients

▲▲ Approximated coefficients



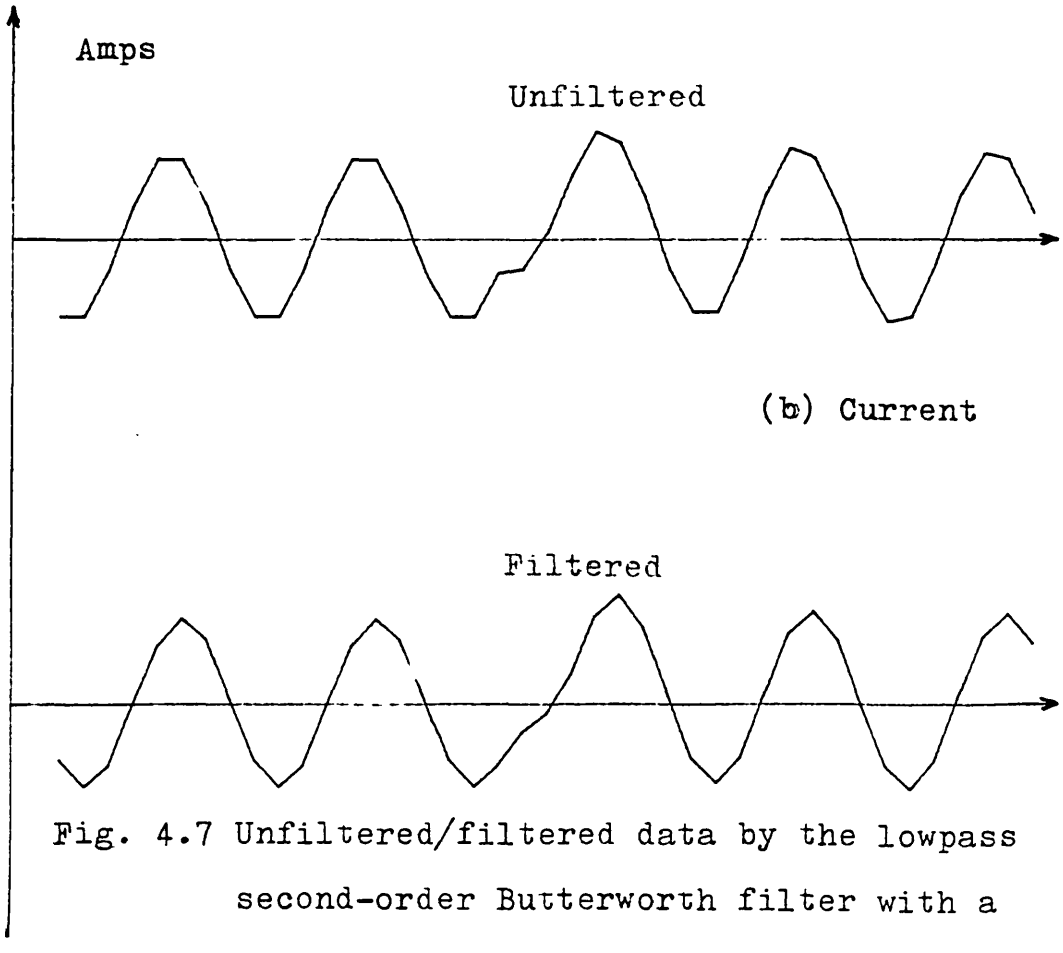


Fig. 4.7 Unfiltered/filtered data by the lowpass second-order Butterworth filter with a cutoff frequency of 120 Hz

the transmission line.

After the voltage and current filtering has been accomplished, the next step is to compute R_L and L_L as seen by the relay, by using the filtered samples.

4.4.2. Mathematical basis of algorithm

The differential equation (4.5) is used to describe the transmission line with the unknowns R_L and L_L .

In fig. 4.8 successive samples 1,2,3,4...of voltage or current are shown. There are three ways in selecting the points for which eq. (4.5) can be solved from these samples.

i) The midpoints formula

This method solves eq. (4.5) at the midpoints between two consecutive samples i.e. 1c,2c,3c..., by calculating v,i and di/dt at these instants.

By considering first differences, i.e. a straight line approximation between two consecutive sample points, the following quantities can be computed:

$$v_{1c}=\frac{v_1+v_2}{2} \quad i_{1c}=\frac{i_1+i_2}{2} \quad \frac{di_{1c}}{dt}=\frac{i_2-i_1}{t_2-t_1}=\frac{i_2-i_1}{h} \qquad (4.8)$$

Where $h=\frac{2\pi}{\omega N}$ is the sampling interval in secs, and N is the sampling rate in Hz.

The same procedure can be repeated for the midpoint 2c. Generally, the first midpoint is called A, and the second

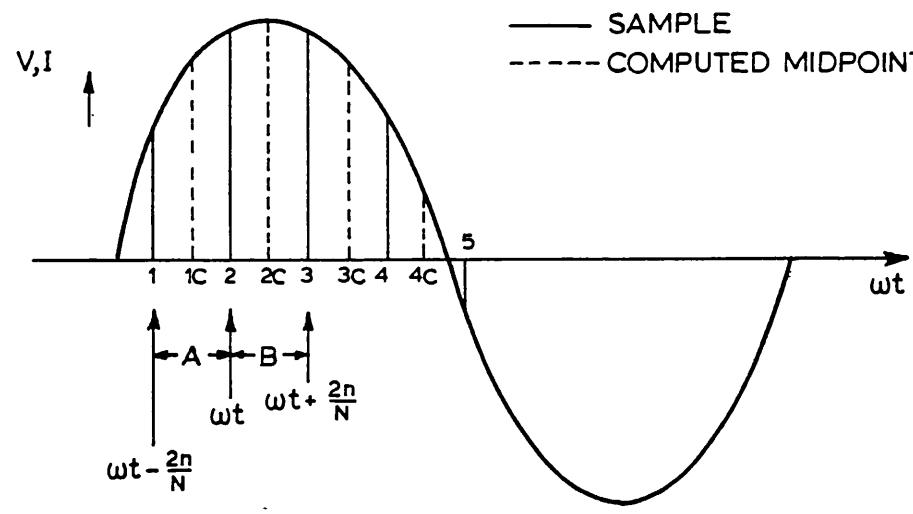


Fig. 4·8 Waveform of voltage or current and its samples

one B.

Consider as:

$$\left.\begin{aligned} VA&=v_1+v_2 & VB&=v_2+v_3\\ CA&=i_1+i_2 & CB&=i_2+i_3\\ DCA&=i_2-i_1 & DCB&=i_3-i_2 \end{aligned}\right\} \quad (4.9)$$

Then the following pair of simultaneous equations can be formulated by using equation (4.5) at the instants A and B.

$$\left.\begin{aligned} VA&=R_L CA+\frac{2L_L}{h}\,DCA\\ VB&=R_L CB+\frac{2L_L}{h}\,DCB \end{aligned}\right\} \quad (4.10)$$

By algebra, the values of R_L and L_L can be obtained, as follows:

$$R_L=\frac{VA\ DCB-VB\ DCA}{CA\ DCB-CB\ DCA}=\frac{N_R}{D} \qquad (4.11)$$

$$L_L=\frac{h}{2}\,\frac{VB\ CA-VA\ CB}{CA\ DCB-CB\ DCA}=\frac{h}{2}\,\frac{N_L}{D} \qquad (4.12)$$

If pure sinusoidal signals are considered, then it can be seen that the quantities present in (4.11) and (4.12) are not the true values of the analogue signals. Specifically they are:

$$\left.\begin{aligned} VA&=2\hat{V}\sin(\omega t+\varphi-\tfrac{\pi}{N})\cos\tfrac{\pi}{N} & VB&=2\hat{V}\sin(\omega t+\varphi+\tfrac{\pi}{N})\cos\tfrac{\pi}{N}\\ CA&=2\hat{I}\sin(\omega t-\tfrac{\pi}{N})\cos\tfrac{\pi}{N} & CB&=2\hat{I}\sin(\omega t+\tfrac{\pi}{N})\cos\tfrac{\pi}{N}\\ DCA&=2\hat{I}\cos(\omega t-\tfrac{\pi}{N})\sin\tfrac{\pi}{N} & DCB&=2\hat{I}\cos(\omega t+\tfrac{\pi}{N})\sin\tfrac{\pi}{N} \end{aligned}\right\} \quad (4.13)$$

where $\hat{V},\hat{I}$ are the voltage and current amplitudes

respectively and φ their phase difference.

Therefore because of the sampling process some constant terms are introduced in N_R, N_L, D, shown in eq.(4.14)

$$N_R = -(2\sin^2\frac{2\pi}{N})\,\hat{V}\hat{I}\cos\varphi$$
$$N_L = -(4\cos^2\frac{\pi}{N}\sin\frac{2\pi}{N})\hat{V}\hat{I}\sin\varphi \qquad (4.14)$$
$$D = -(1-\cos\frac{4\pi}{N})\,\hat{I}^2$$

For a sampling rate of 8 samples/cycle, these become:

$$N_R = -\hat{V}\hat{I}\cos\varphi \qquad (4.15a)$$

$$N_L = -2.414\,\hat{V}\hat{I}\sin\varphi \qquad (4.15b)$$

$$D = -\hat{I}^2 \qquad (4.15c)$$

But:

$$R_L = \frac{\hat{V}}{\hat{I}}\cos\varphi \quad \text{and} \quad X_L = \frac{\hat{V}}{\hat{I}}\sin\varphi \qquad (4.16)$$

comparing eq.(4.15) and eq.(4.16) it can be seen for the selected sampling rate, that the only term needing correction is N_L. As will be seen in chapter 5, this correction does not need the additional multiplication, as this term can be taken into account in the reactance limit.

This method needs a data window of 2 sampling intervals i. e. 3 samples. Referring to fig. 4.8, the calculations start after sample 3, by using the values at the midpoints 1c, 2c. Then the next sample (point 4) enters and the calculation is continued, by using the midpoints 2c and 3c and so on.

ii) The sample formula

Instead of evaluating eq.(4.5) at the midpoints 1c and 2c, the actual samples 2 and 3 can be used, then only di/dt has to be computed.Samples 1 and 3 are needed for$(di/dt)_2$ and samples 2 and 4 for $(di/dt)_3$.

Thus a data window of 3 sampling intervals is necessary. To avoid this, a new method has been devised which uses one sample and one midpoint, as shown next.

iii) The sample and midpoint formula.

The two points used are the sample point 2, and the midpoint 2c, hence point 1c of the midpoint formula has been replaced by sample point 2. That means that the computation moves faster to the postfault data.

By following the same nomenclature as previously, it can be seen from fig. 4.8 that:

$$VA=v_2 \qquad VB=v_2+v_3$$

$$CA=i_2 \qquad CB=i_2+i_3 \qquad (4.17)$$

$$DCA=i_3-i_1 \qquad DCB=i_3-i_2$$

Again if pure sinusoidal data are considered, the following corrections are needed, because of the sampling process:

$$\left.\begin{aligned} VA&=\hat{V}\sin(\omega t+\varphi) & VB\\ CA&=\hat{I}\sin(\omega t) & CB\\ DCA&=2\hat{I}\cos(\omega t)\sin\tfrac{2\pi}{N} & DCB \end{aligned}\right\} \text{ same as previously} \qquad (4.18)$$

To apply (4.18) in (4.11) and (4.12), DCB has to be multiplied by $4\cos^2\frac{\pi}{N}$. Therefore in place of DCB in (4.11) and (4.12), 3.414 DCB is used.This requires one more multiplication than method(i). By substituting the expressions (4.18) and the modified DCB, in (4.11) and (4.12) it can be found that for 8 samples/cycle:

$$N_R = -\hat{V}\hat{I}\cos\varphi \qquad (4.19a)$$

$$N_L = -(\sin\frac{2\pi}{8})\hat{V}\hat{I}\sin\varphi = -.707\ \hat{V}\hat{I}\sin\varphi \qquad (4.19b)$$

$$D = -\hat{I}^2 \qquad (4.19c)$$

This method needs again a data window of 2 sampling intervals. The calculations begin after sample 3, using points 2 and 2c, then at the next sample the points 3 and 3c are used and so on.

4.4.3. Response of the algorithms

To compare the response of these algorithms, data have been received from the model of the line and the program has been run off- line on a main- frame computer.

Fig 4.9 refers to the midpoints formula. It can be seen that the reactance during the prefault period is not steady caused by the numerical errors. The tests shown in the following figures have been carried out using a resistive load. The only reactance present in the model was that of the transmission line. The power factor for these tests was 0.997 i. e. $\varphi = 4.4^0$. As N_L is analogous to $\sin\varphi$, and $\sin\varphi$ is in the neighborhood of

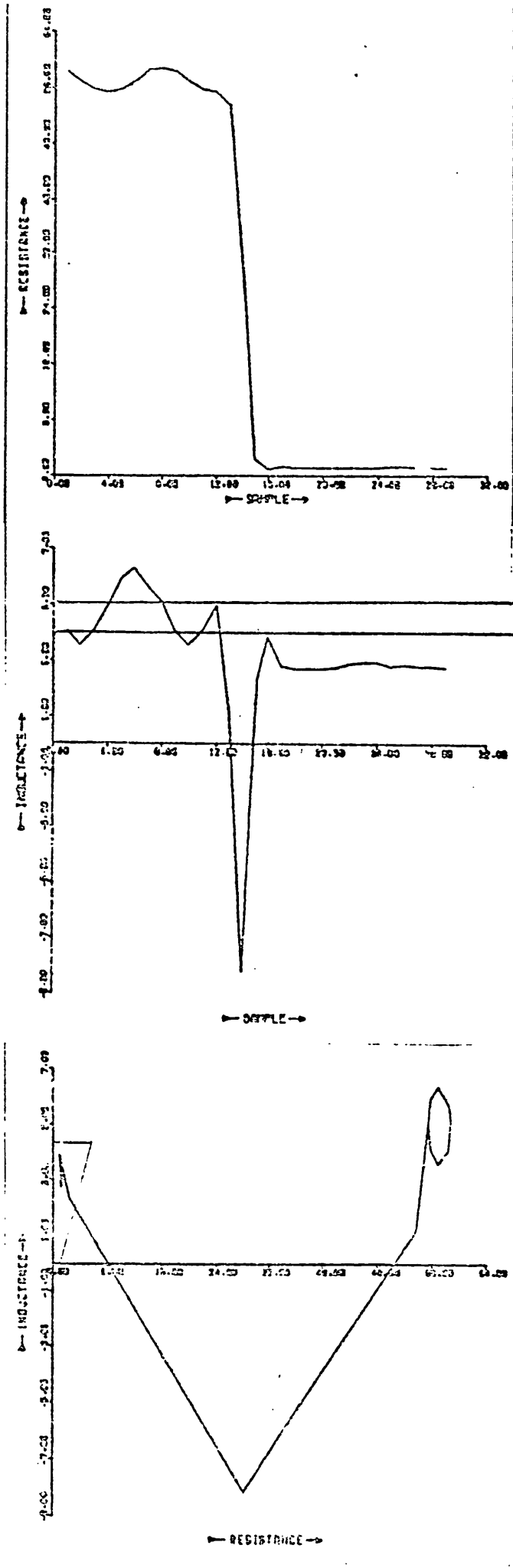
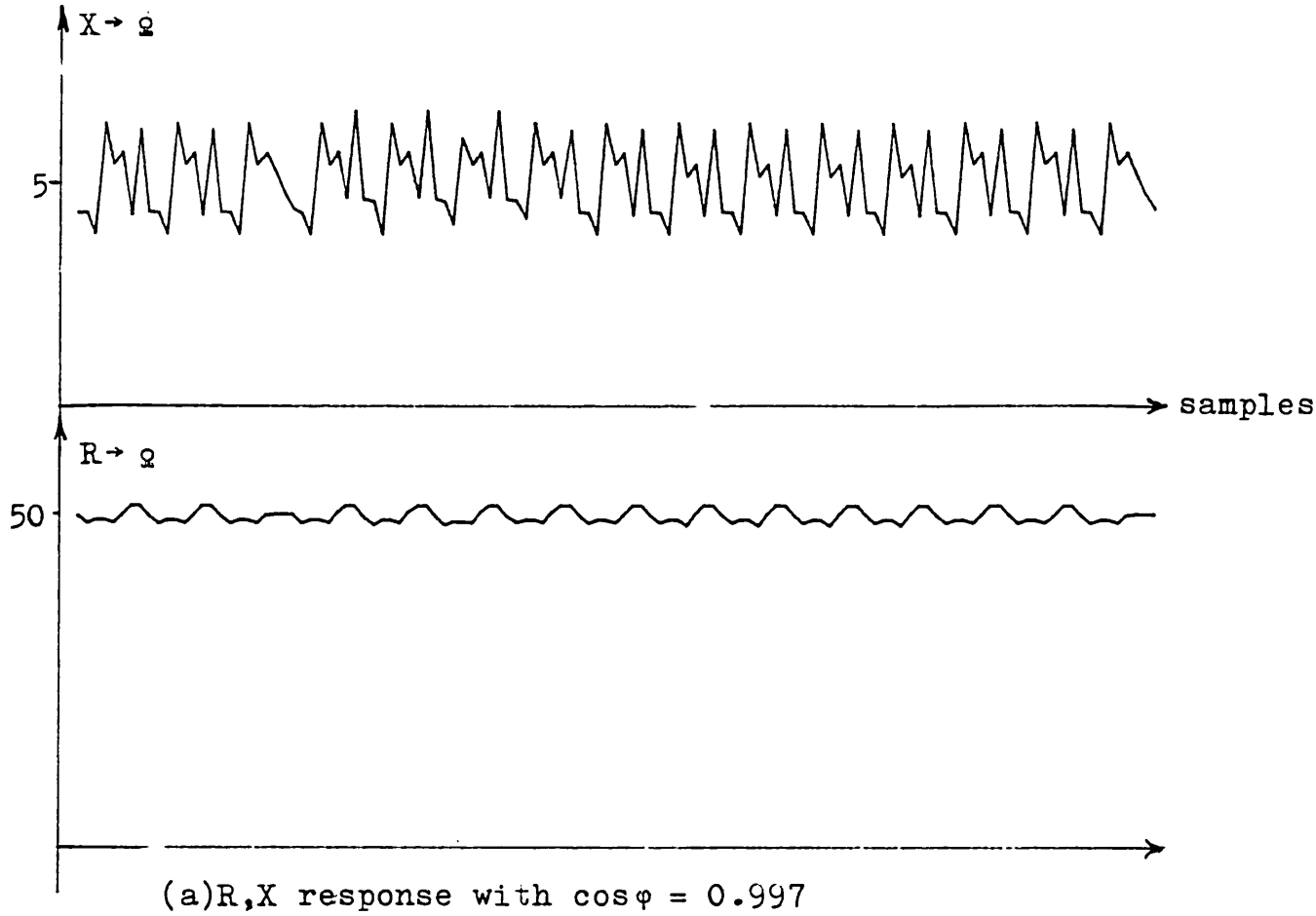


Fig. 4.9 Response of the midpoints formula

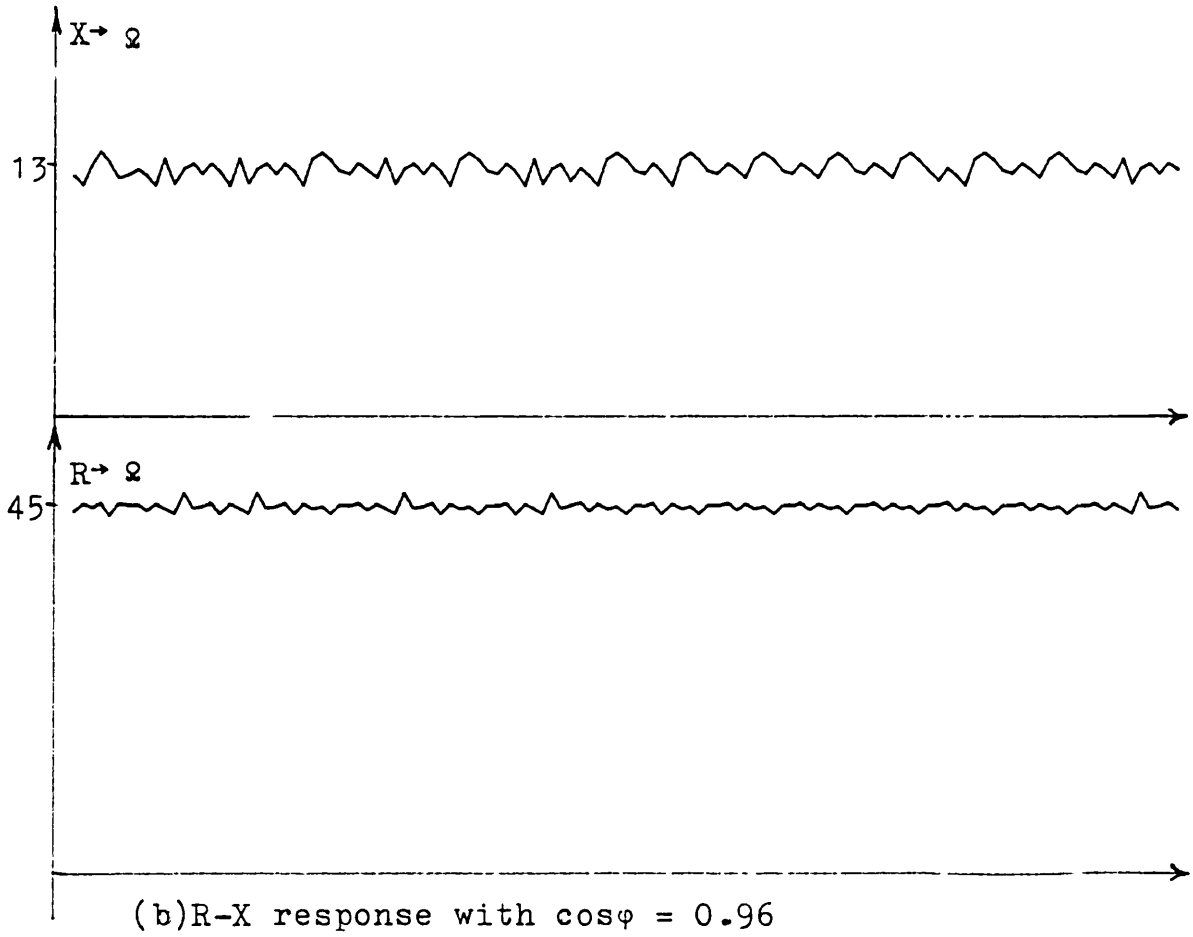
zero, it is almost linear with a very steep slope. Small changes in the angle will produce a big change in the value of $\sin\varphi$. Taking into account the A/D converter resolution and the fact that the prefault current is small, then errors are introduced because of the quantization of the current signal. The switching- gain amplifiers[4] will improve the results in such cases. In addition the offsets present in the antialiasing analogue filters, introduce further errors, especially in the region of zero current.

Tests have been carried out, by connecting a motor at the far end of the line lowering the power factor to 0.96 i. e. $\varphi = 17^{o}$. Fig. 4.10 compares the results under these two different types of load. It can be seen that the algorithm behaves within the specified accuracy, i. e. about $\pm$ 5.2% . The inaccuracy in the reactance calculation with resistive load is not critical because the resistance computed is accurate and well outside the trip area, therefore the relay is stable.

Fig. 4.9 shows that the resistance needs 6 sampling intervals to move inside the resistance limit, while the reactance needs 5 sampling intervals. Therefore a total time of 15ms is necessary for the fault to be detected at 8 s/c. It can be seen that the response is noisy during the first two intervals,



(a)R,X response with cosφ = 0.997



(b)R-X response with cosφ = 0.96

Fig. 4.10 Response of the algorithm under different loads.

because of the short data window.

Fig. 4.11 has been obtained for the same type of fault by using the midpoint and sample formula from which the detection time achieved is the same as previously. It will be seen later that for faults up to 50 % of the line, the detection time is less that the first method.

As method(iii) moves faster to the fault data, the response is more noisy. In fig. 4.11 it can be seen that after the fault inception, two spikes occur, which are outside the trip zone.

Fig. 4.12 has been recorded by using the same method as in fig. 4.11, but with a simple averaging of the reactance. By doing so, the response becomes smoother i. e. the spikes are not so large in amplitude. With the averaging, the fault is detected in 12.5 ms, i. e. faster response has been achieved for the far end of the line.

While the averaging process can show such an improvement, consider now fig. 4.13 computed by the microprocessor. The fault is at the end of zone 1 and there is a big spike in the positive direction. Averaging for this case will give a slower response than the one obtained by a direct application of the midpoint and sample formula.

The responses of fig. 4.11 and 4.13 have been

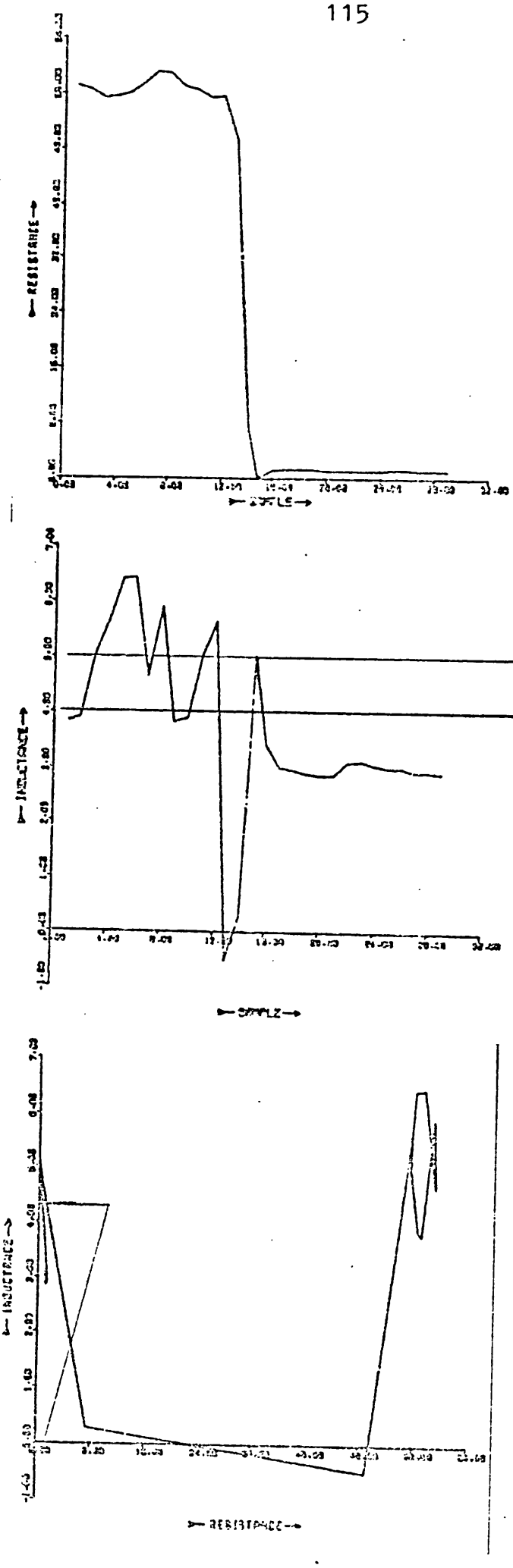
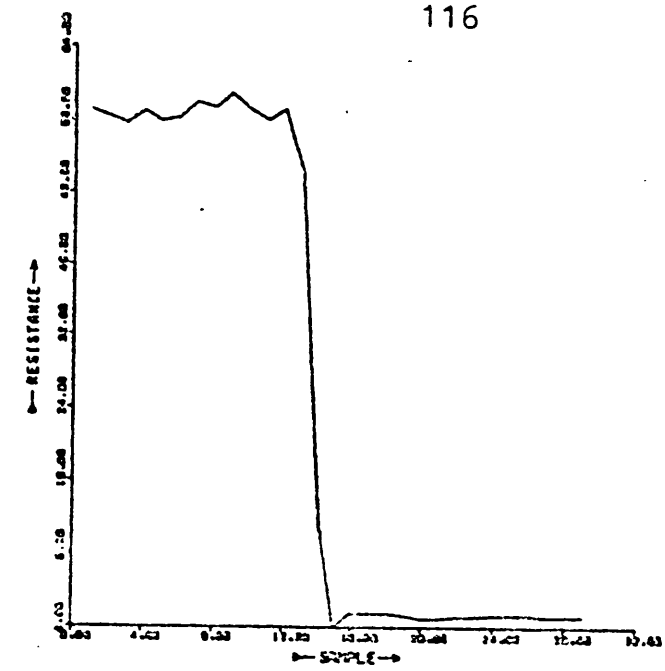
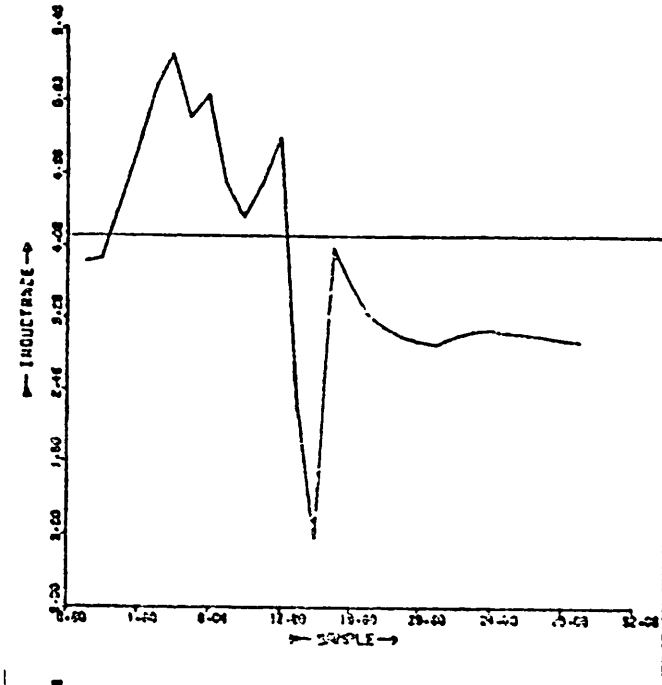


Fig. 4.11 Response of the sample and midpoint formula





Zone 1

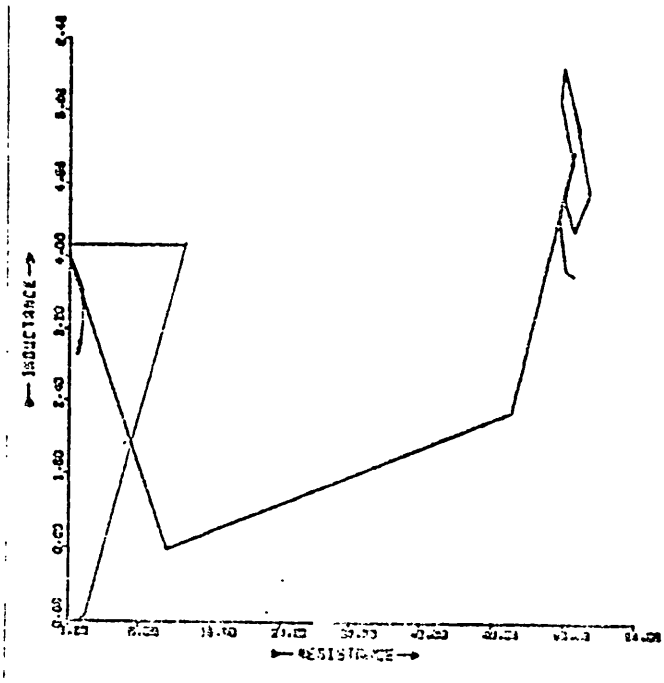


Fig. 4.12 Response of the sample and midpoint formula with reactance averaging

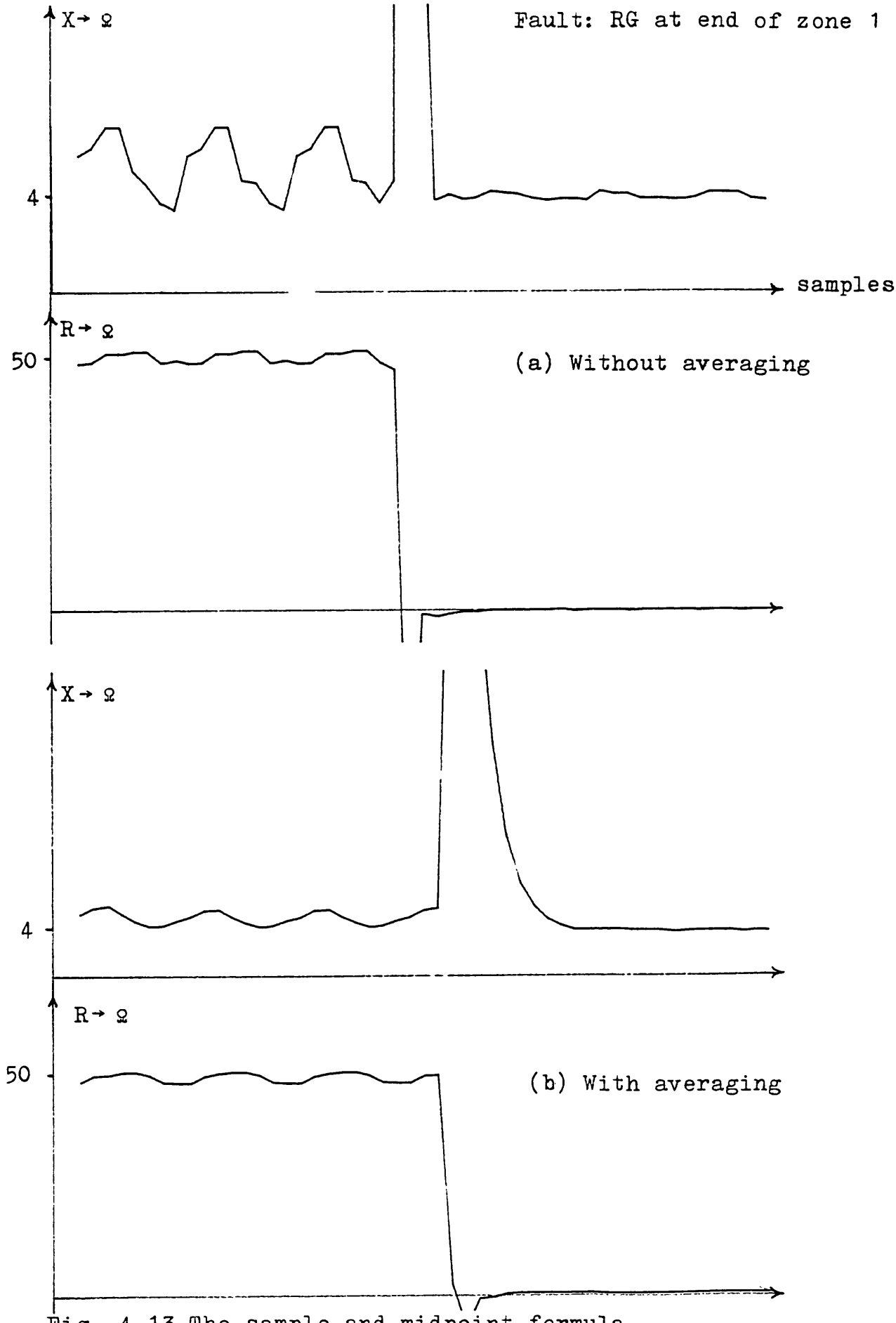


Fig. 4.13 The sample and midpoint formula

recorded under different inception angles. In fig. 4.11 the fault angle was 0^{o}, while in fig. 4.13 it was 90^{o}. In both cases digital filtering has not been used. Filtering will improve the response, but not dramatically, as the spikes are caused by the short data window. Therefore the averaging improves marginally the detection time for faults up to 75% of zone 1, and impairs it for faults at the far end of the line.

Hence two options are open:

i) The sample and midpoint formula without averaging, which gives the same detection time as the midpoints formula, but a faster response for faults up to 50% of the line.

ii) The same formula, but with reactance averaging.

In chapter 6, the performance of the dedicated relay by using the midpoints method and the sample and midpoint formula without averaging will be compared. But firstly, the way the output values are converted into a relaying decision will be described. This procedure, the program organisation and the additional features of the relay will be given in chapter 5.

CHAPTER 5

PROGRAM CONFIGURATION

5.1 Introduction

The performance of the relay depends on the way the software is organised. The main objective is to build a program which meets all the specifications as simple and as reliable as possible. In addition, all the calculations need to be performed before the arrival of the next data block, otherwise the unit will run out of synchronism. One final requirement is that the program length must be kept within the 2K limit. This suggests that the program has to be built in blocks of subroutines called by a main program. By doing so, although the execution time will be increased, as long as the algoritm runs in less than a sampling interval, no problems are introduced. By organising the software in such a way, the program remains quite general and modifications can be easily introduced by rewriting the subroutines.

Other advantages are:

i) tests on relay operation becomes easier as the program is building- up in blocks.

ii) in later versions of the relay, these subroutines can be coded in microinstructions producing faster response, fewer main program memory locations required and the generation of a higher - level protection

purpose- oriented language.

In this chapter the way the fault program is organised and the provision of other facilities are discussed.

5.2 Configuration of the main program

Fig. 5.1 presents the flowchart of the main program. It begins with the initialising routine, which resets or clears some flags and data- memory locations. In addition, the relay settings are specified by reading the switches of the control panel. Ideally the relay settings will be in the constant store, but as they are different for the two algorithms, it is better for testing purposes to store them in the data- memory. The way the relay settings are defined will be discussed in the subsection 5.4.2.

As has been examined in chapter 4, the employed algorithms have a data window of 2 sampling intervals. Therefore when the relay is switched on for the first time, the first two samples are used to calculate the quantities VA,CA,DCA,VB,CB,DCB. Impedance calculations start after the first two samples.

As the program has been arranged, such that no starting elements are necessary, all six impedances are evaluated with the sequence R-G, Y-G, B-G, Y-B, B-R, R-Y. When the program has finished with the execution of the six impedances, it goes back to the beginning of the

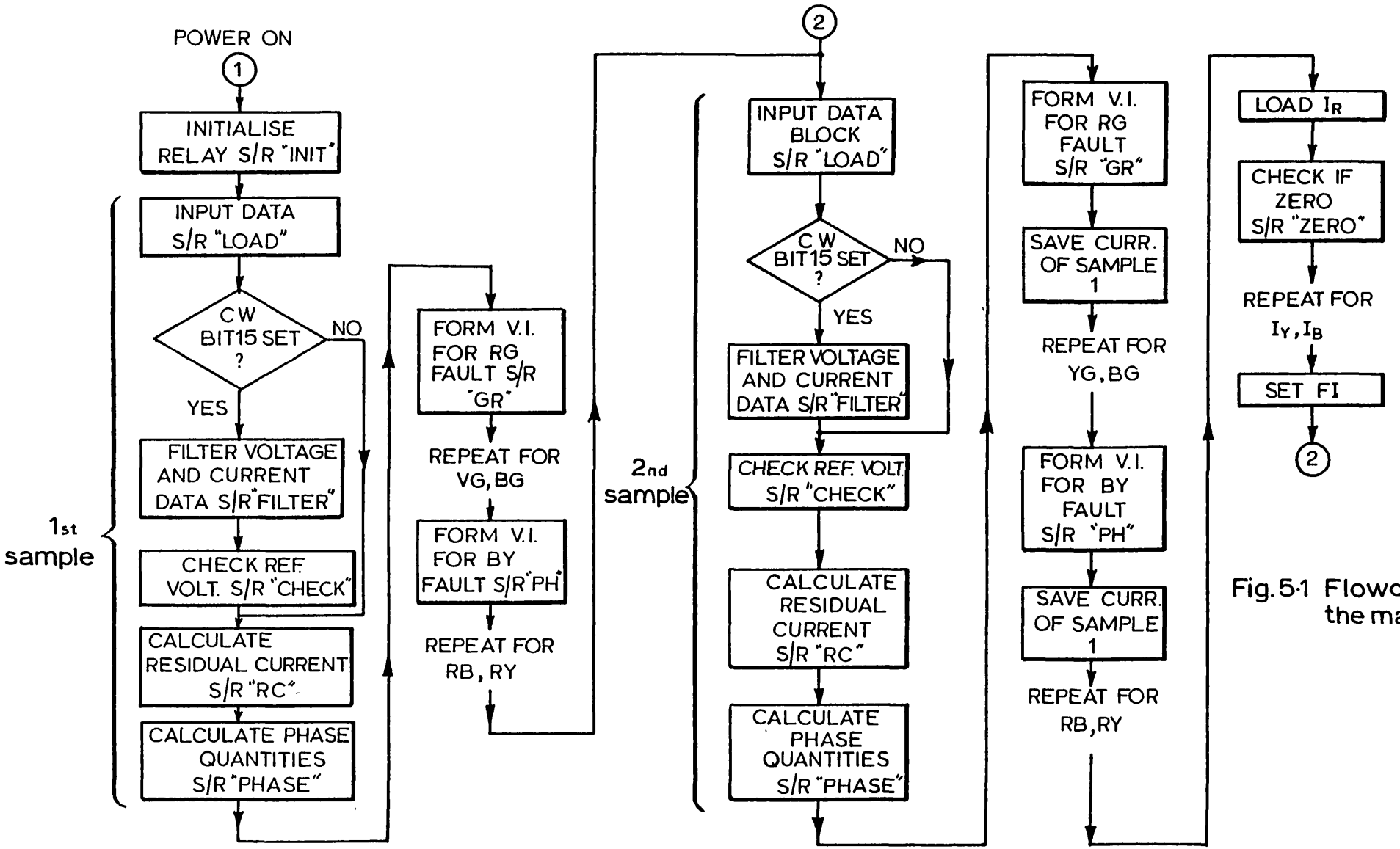
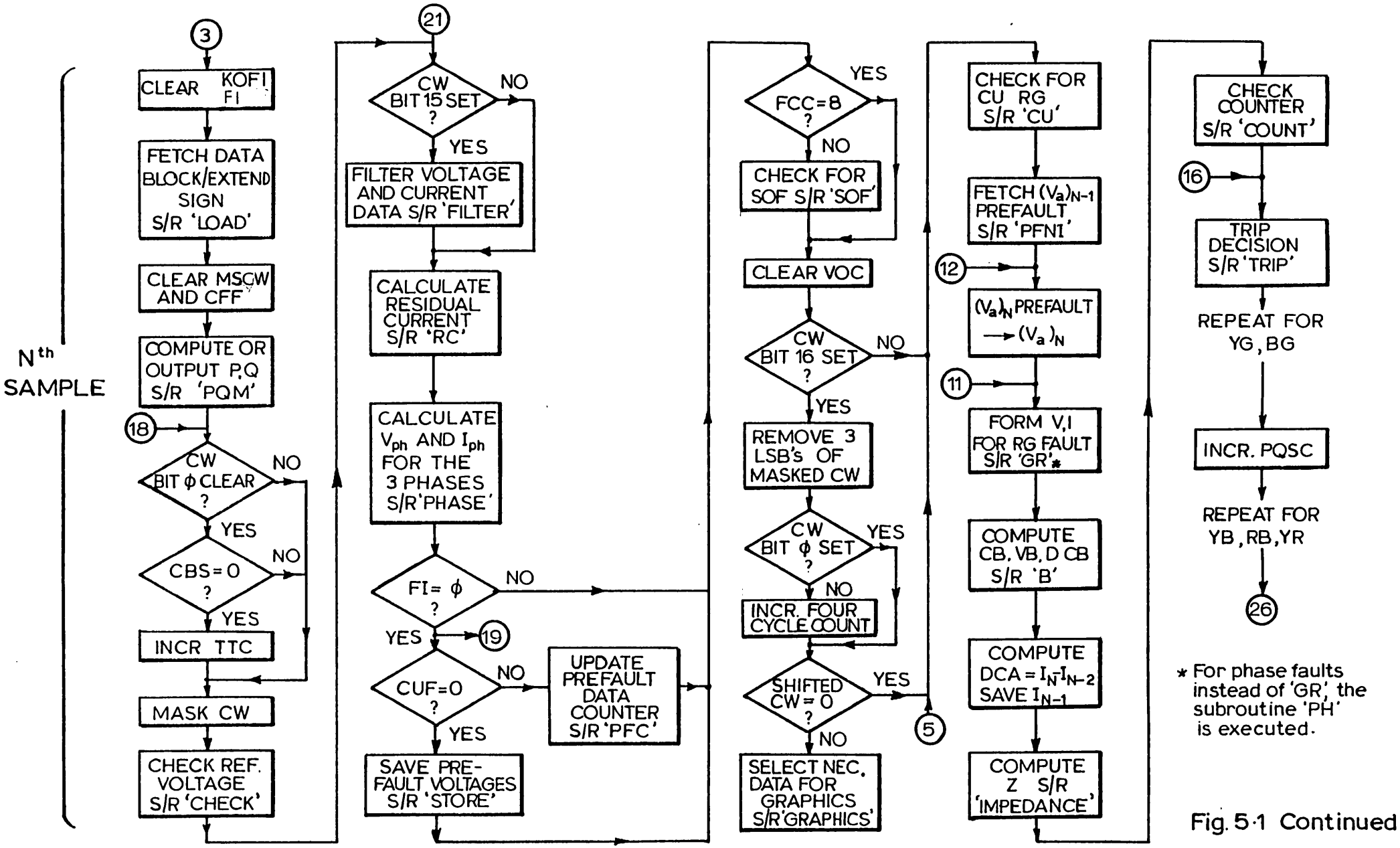


Fig. 5·1 Flowchart of the main program



* For phase faults instead of 'GR', the subroutine 'PH' is executed.

Fig. 5·1 Continued

N^{th} sample. The program stays inside this loop, until an internal fault has been detected, after which it jumps to the post- fault routine.

In appendix 6, the program listings, the data and constant store locations and the flags table are given.

In the next sections, the main facilities provided by the relay will be described.

5.3 Auxiliary subroutines

Fig. 5.2 shows the flowcharts of some subroutines, needed to form functions of the voltage and current samples. For example " LOAD " stores the samples, and converts the 10-bit data to 16-bit words, " INIT " resets some data locations and inputs the settings, " RC " calculates the residual current, " PHASE " computes the phase voltages, " GR " performs the zero- sequence compensation for the three line currents and voltages, while " PH " does the phase compensation, " B " calculates the quantities VB,CB,DCB and finally " ZERO " checks for a data sample of zero value. " FILTER " implements the digital filter discussed in chapter 4. This subroutine acts upon a request from the front panel (setting of the switch 15).

5.4 The impedance calculation

The purpose of this routine, shown in fig 5.3 is to calculate the quantities N_R , N_L and D. Afterwards

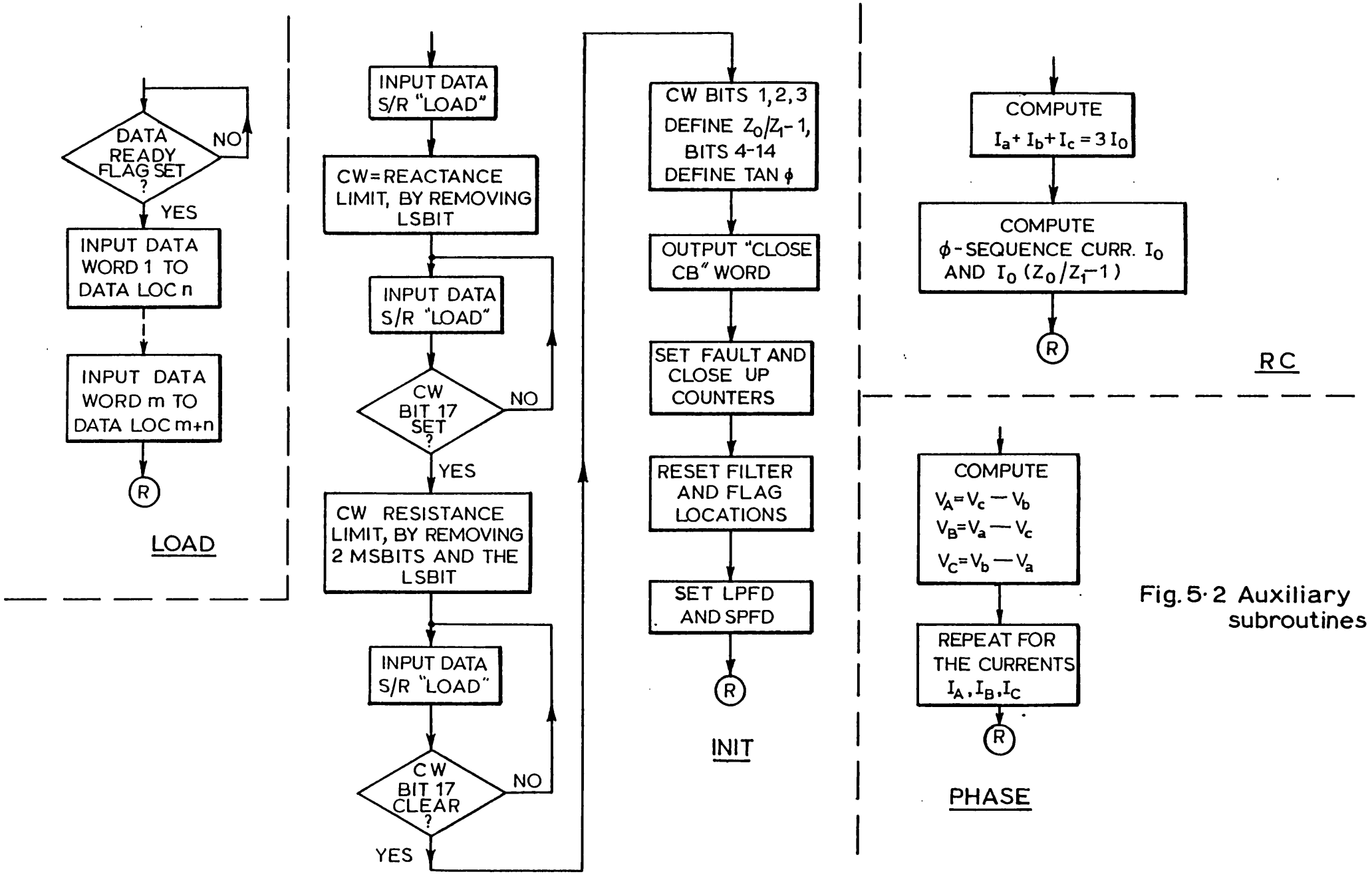
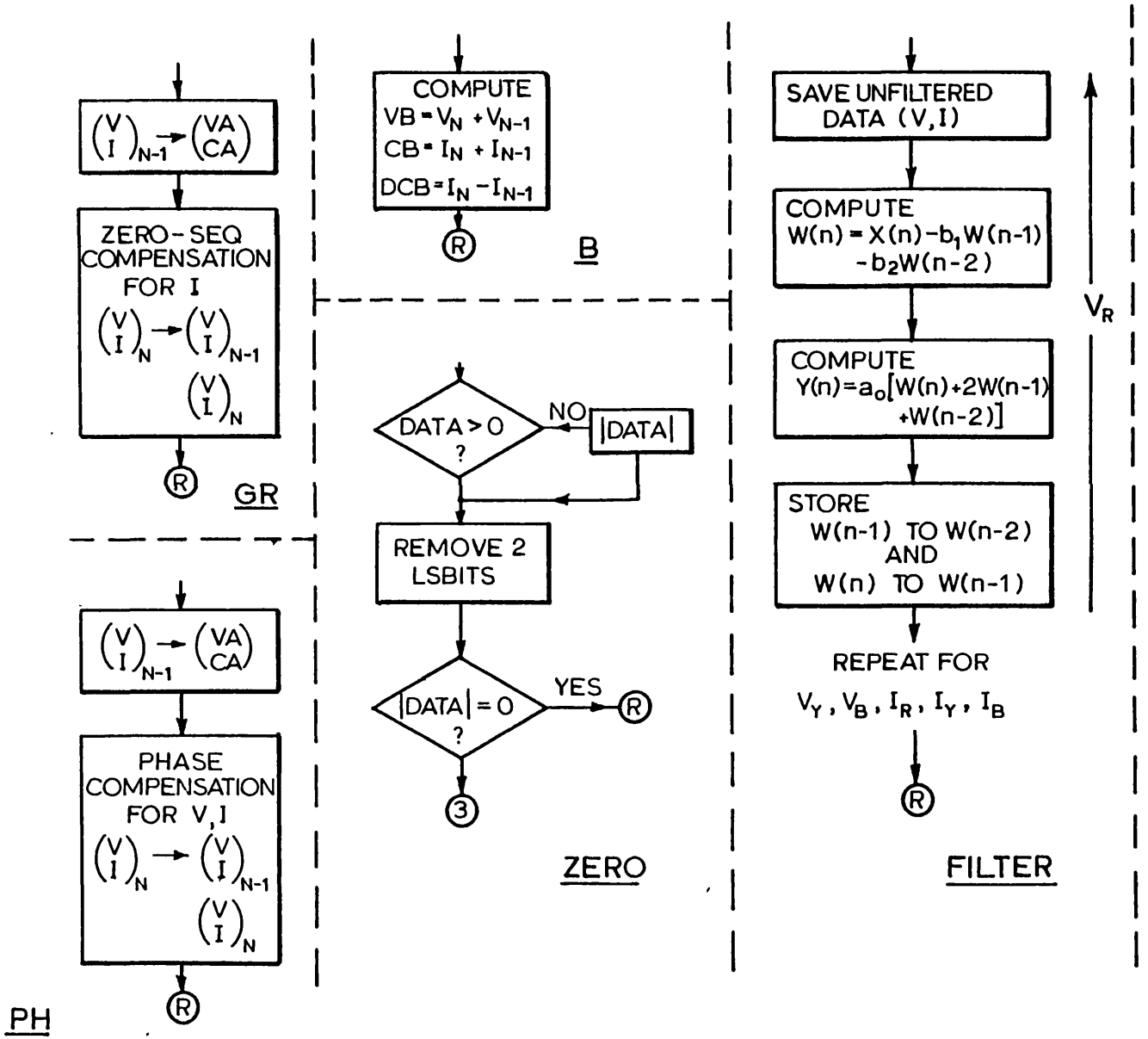


Fig. 5·2 Auxiliary subroutines



Note :-

(R) = Normal return

(N) = Return to main program entry point N

(IAN) = Return to the main program, indirectly entry point N

Fig. 5·2 Continued

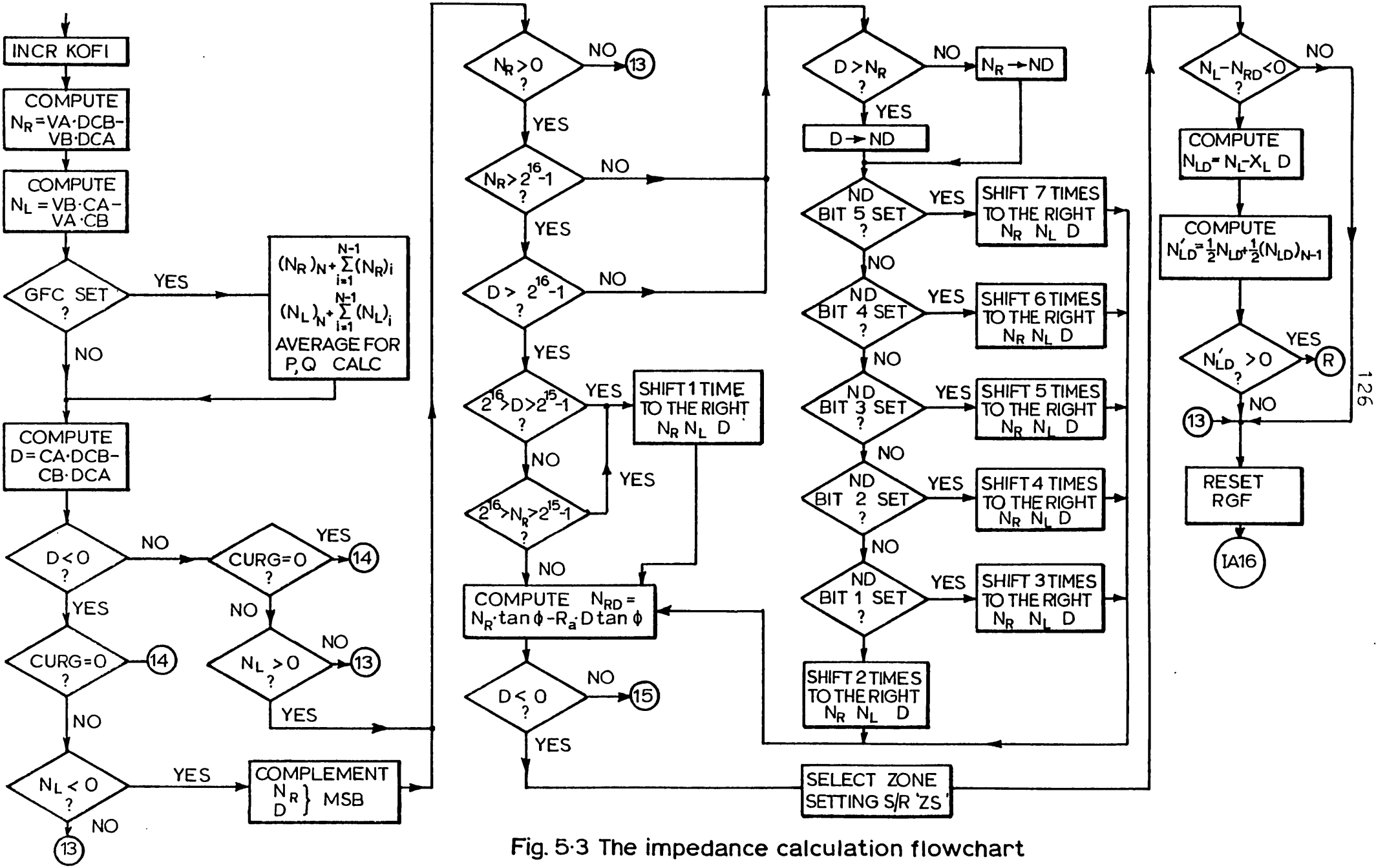


Fig. 5·3 The impedance calculation flowchart

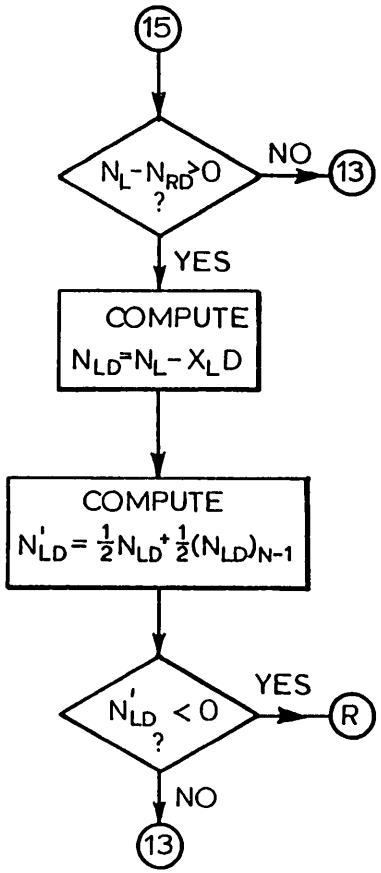


Fig. 5·3 continued

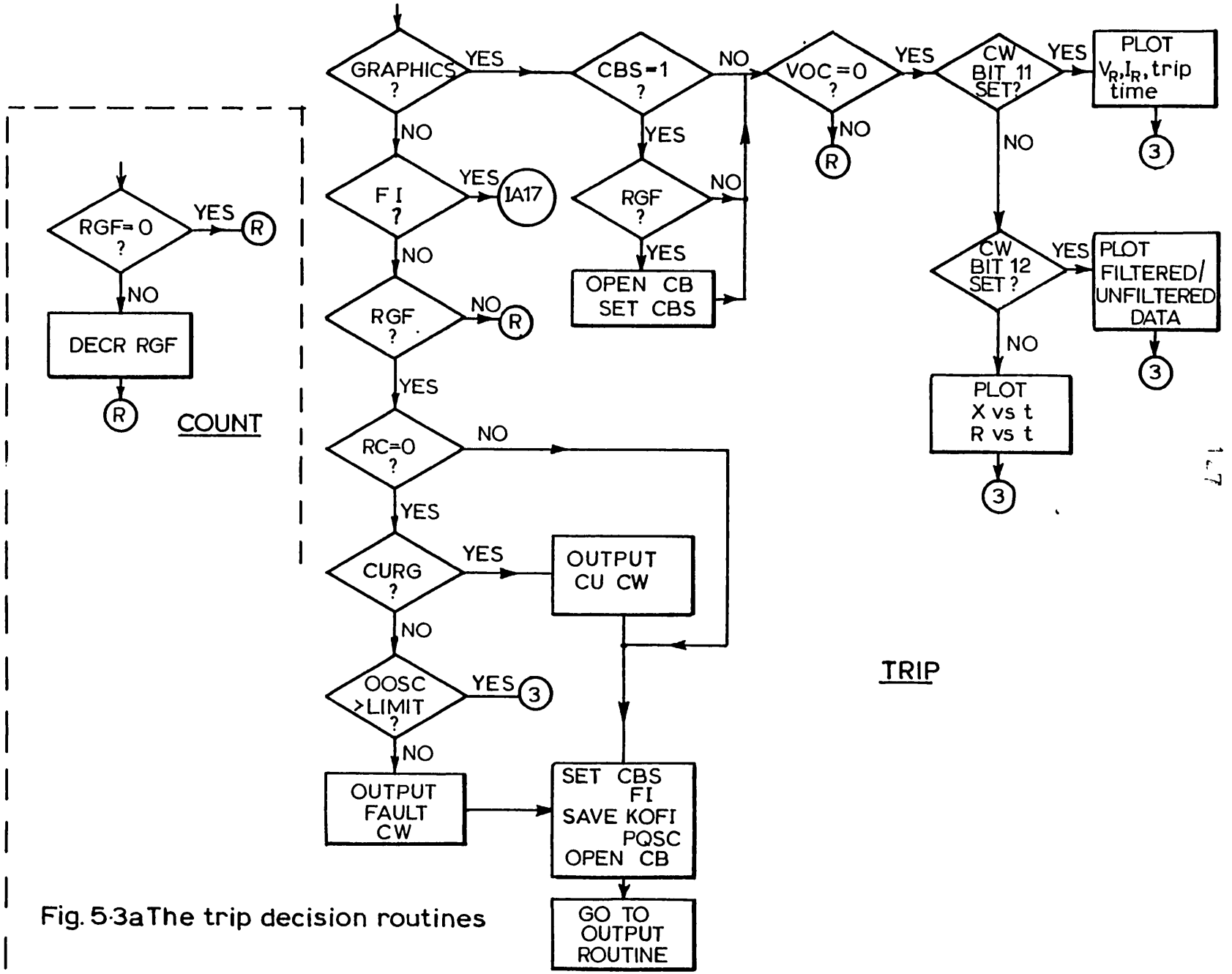


Fig. 5·3a The trip decision routines

the resistance and reactance is computed and compared with the corresponding limits.

In chapter 3, the difficulties involved in the microcoding of the division instruction have been discussed. Therefore, an alternative way to avoid division has been used.

The transmission line model, used for the tests does not have the same ratio X_L/R_L for the different taps, as can be seen in fig. 5.4. Therefore the line cc′ can be considered as a composition of the transmission line added to a resistive fault.

By employing this model the p. u. values of a system with a primary network ratio (X/R) of 6.5 can be simulated, i. e. a typical 230 KV system. The maximum lenght of the line simulated is 135 miles.

The chosen polar characteristic for zone 1, is the area ABCD.

Hence the following conditions have to be met:

$$0<X=\frac{N_L}{D}<X_L \qquad (5.1)$$

and $0<X<(R-R_a)\tan\varphi$ or (5.2)

$$0<\frac{N_L}{D}<(\frac{N_R}{D}-R_a)\tan\varphi \qquad (5.3)$$

If, instead of dividing by D, a multiplication is executed then

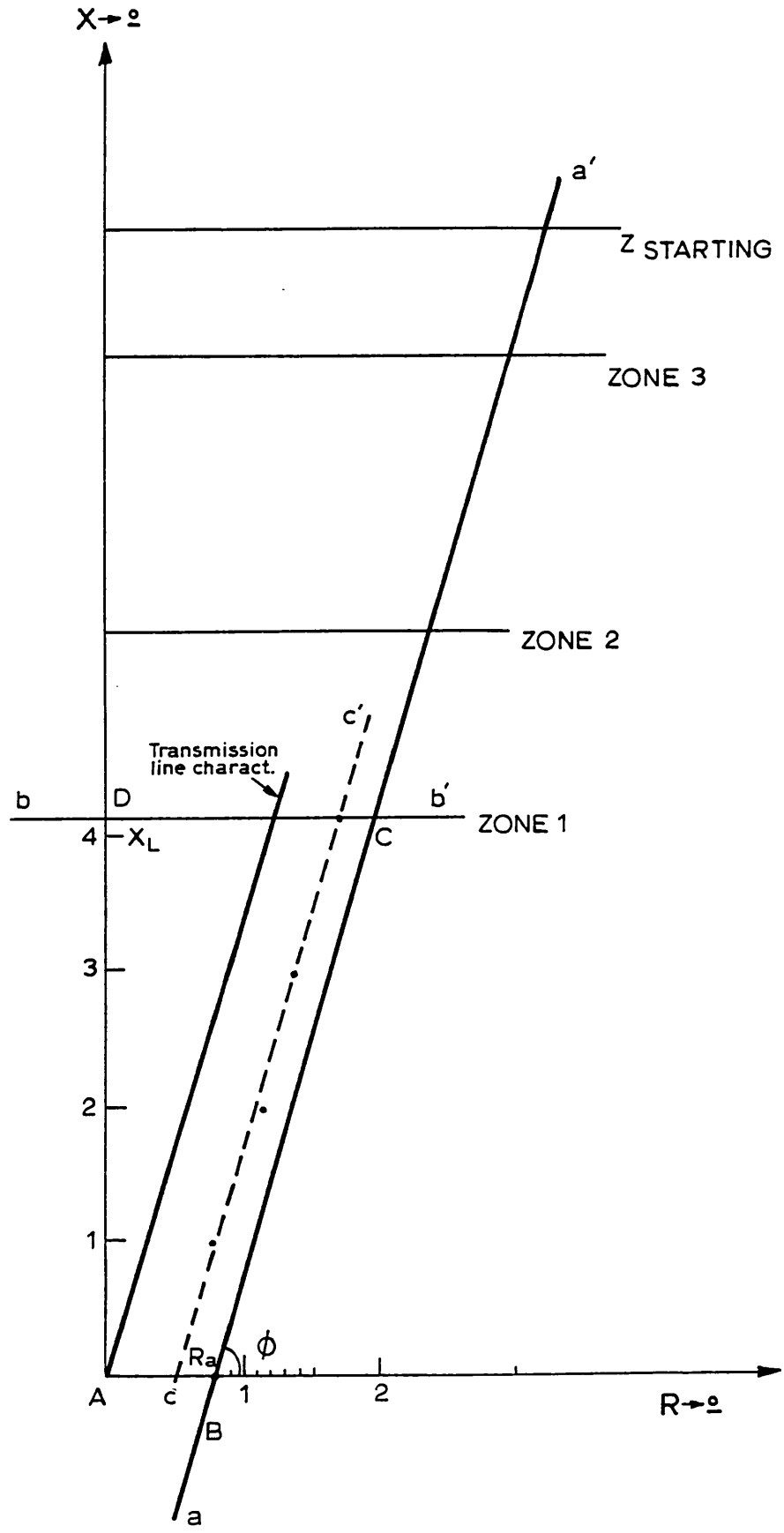


Fig. 5·4 The relay characteristic

eq. (5.1) and (5.3) become

$$N_L < 0 \qquad (5.4)$$

$$N_R < 0 \qquad (5.5)$$

$$N_L - X_L\, D > 0 \qquad (5.6)$$

$$N_L - N_R \tan\varphi + R_a D \tan\varphi < 0 \qquad (5.7)$$

} if $D < 0$

The above inequalities are reversed, if $D > 0$.

Therefore an internal fault will be detected, if the inequalities (5.4), (5.5), (5.6), (5.7) are valid. Such a procedure does not compute the resistance and reactance values, but it achieves an accurate and fast fault detection decision. This is not a drawback, as the dedicated relay communicates with a monitoring computer, in which the division can be executed off- line at a later time.

In (5.6) and (5.7), N_R and D must be 16-bit numbers, otherwise an erroneous result will be produced by the multiplication instruction. The double-precision instructions written can be useful in handling numbers bigger than $(2^{15}-1)$. The procedure followed can be seen in fig. 5.2, where by multiple double-precision shifting to the right, numbers smaller than $(2^{15}-1)$ are produced. By calculating the maximum number possible to be generated by computation, it is found that $D = 750\ 000$. The program as written can handle numbers

up to 4 194 303. The number of the required shifts is not fixed but variable according to the size of the quantities N_R and D.

The error introduced by scaling is very small. For example consider the inequality (5.6). By executing n shifts to the right, (5.6) becomes

$$\frac{N_L}{2^n} - X_L \frac{D}{2^n} > 0 \qquad (5.8)$$

As long as $N_L - X_L D > 2^n$ the inequality (5.8) will lead to the same result as (5.6).

If $N_L - X_L D = 2^{n-1}$, then $N_L - X_L D/2^n = 1/2$, which means that the processor will detect $(N_L - X_L D)/2^n = 0$, because it handles integer numbers. Such a case corresponds to:

$$X = \frac{N_L}{D} = X_L + \frac{2^{n-1}}{D} \qquad (5.9)$$

But as D is a large number, the error term $2^{n-1}/D$ is quite small. On the other hand, (5.9) suggests that (5.8) gives an erroneous result for faults close to the setting point. For such faults the current is comparatively small and D will also be small and so scaling was not considered necessary.

There are two exits from the impedance routine. The first corresponds to an internal fault and the second to an external fault or to normal operation. For each impedance calculation, a counter is assigned, the value of which controls the trip signal to the circuit breaker.

The counter is reset to 3 if no internal fault is detected, i. e. if the inequalities (5.4) - (5.7) are invalid, otherwise the counter is decremented by one. If the relay computes that an internal fault persists for 3 consecutive samples, it sends a trip signal to the CB. In addition, some other flags are set which will be useful for the fault output report. If graphics have been requested, the relay opens the CB and selects the corresponding data to be plotted. This process will be described later. Fig. 5.3a shows the flowcharts of the program followed, after a fault has been found.

5.4.1 The zone selection

The calculations previously discussed are referred to zone 1 settings. In addition, a starting element for the zone 2 and the zone 3 timers has to be included.

The starting element calculation is an impedance test similar to that for zone 1, but with a different setting, such as to embrace zone 3. To save processing time for other operations, only three starting calculations are executed in each sampling interval. So in one sampling interval, the starting calculations for g.f.s are executed, in the next the same procedure is repeated for the p.f.s and so on. Therefore, if the fault is in zone 1, it will be detected without any delay, while, if the fault lies somewhere in zone 2 or 3, it

might be detected 2.5ms later, but such an error is not critical.

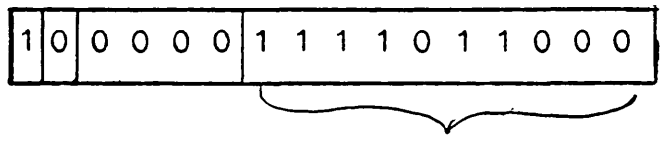
For each of the six impedances, an independent timer is provided. To make the program more efficient the following format has been assigned to the timers:

Bit 15 is the identification bit for zone 2

Bit 14 is the identification bit for zone 3

Bits 0 - 9 contain the negative of the time delay in multiple of 2.5ms.

For example, the initial value of a five cycles timer for zone 2 is:



- 40 i. e. 100 ms

The relay provides an independent 3- zone scheme for each impedance calculation. If the fault has been removed, then the starter is reset and computation continues in the normal mode, i. e. zone 1 for every sample and the starting zone for every other sample. The flowchart of this scheme is shown in fig. 5.5.

As can be seen in fig. 5.4, the right hand limit of the characteristic, for simplicity has been kept the same for all zones. The limits for zones 2,3 and starting depend on the specific application.

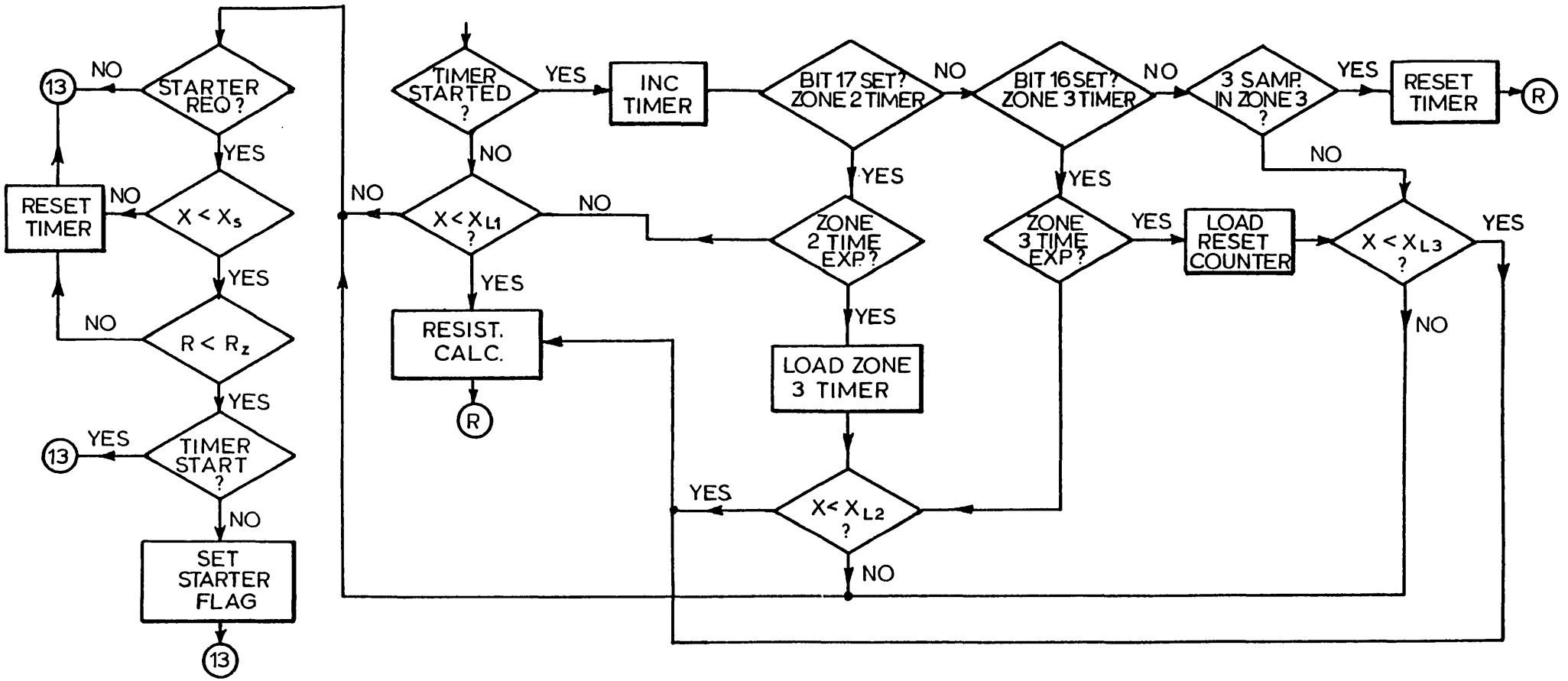


Fig. 5·5 Zone selection routine (ZS)

5.4.2 The relay settings

The zone settings are defined in exactly the same way as for conventional relays, i. e. in terms of the secondary reactance and resistance. The only difference is that now the secondary quantities are the outputs of the anti-aliasing analogue filters, therefore all the intermediate gains have to be taken into account. In addition the correction terms discussed in chapter 4, need to be included. It has been found that

$$(N_L)_{computed} = C(N_L)_{real} \qquad (5.10)$$

where C= 2.414 for the midpoint algorithm

C= 0.707 for the sample and midpoint algorithm.

From eq.(5.6) and (5.7) it can be seen that the quantities to be defined are X_L, $\tan\varphi$ and $(R_a \tan\varphi)$. Substituting (5.10) in (5.6) and (5.7) the quantities to be defined are:

$$C\,X_L,\ C\,\tan\varphi\ ,\ C\,R_a\tan\varphi \qquad (5.11)$$

Appendix 5 gives the attenuation of the voltage and the current signals as 82.87 and 6.05 respectively.

Therefore $$R_a = \frac{(R_a)_{primary}}{13.69752} \qquad (5.12)$$

and $$X_L = \frac{(X_L)_{primary}}{13.69752} \qquad (5.13)$$.

In the test rig used:

$$\left.\begin{aligned} (R_a)_{primary} \quad \tan\varphi &= 2.8417\,\Omega \\ \tan\varphi &= 3.67 \\ (X_L)_{primary} &= 4.1\,\Omega \end{aligned}\right\} \quad (5.14)$$

By substituting (5.14) in (5.12) and (5.13), gives

$$R_a = 0.2074609\,\Omega$$

$$X_L = 0.299324\,\Omega$$

Therefore the settings for the midpoints (A), and the sample and midpoint (B) algorithms are as in table 5.1.

TABLE 5.1

THE RELAY SETTINGS

Quantity	Algor.	Real	Approximated
C X_L	A	0.722568	0.722656 (8-binary bits)
	B	0.211622	0.2109375 (8-binary bits)
C $\tan\varphi$	A	8.85938	8.875 (3-binary bits)
	B	2.59469	2.625 (3-binary bits)
C $R_a \tan\varphi$	A	0.500811	0.5 (1-binary bit)
	B	0.146674	0.1484375 (7-binary bit)

5.5 Close-up faults

During a close- up fault, the voltage collapses to a very small value. As the A/D resolution is 19.57mv, the representation of this voltage to the relay cannot be accurate, unless the gain ranging amplifiers discussed in chapter 3, are used. Such a voltage representation might give an erroneous result because of numerical errors.

In the event of a close-up fault, the main function is to determine if the fault is in front of the relay or behind it. Accurate calculation of the impedance value is not necessary. In conventional relays, there are two ways to solve this problem employing cross- - polarisation or memory principles.

In the cross- polarisation scheme , a voltage called the " polarising voltage " is obtained from a pair of sound phases. But in the event of a close-up 3- phase fault, there is no polarising voltage, so this scheme fails to operate under 3- phase faults.

The memory principle employs a memory circuit which preserves the prefault voltage by a resonant circuit tuned to 50 Hz. The latter method will always work except in the case of closing the CB onto a line line already having a 3- phase fault. (e.g. earthing leads are not removed).

Although these methods have been extended to

digital protection,[74,75] there is a trade off on which method to choose. Cross- polarisation is easier to program as it does not need prefault samples, but it cannot be used in the event of a 3- phase fault. Therefore the memory principle has been applied here. To cover the case of switching-on to a 3- phase solid fault, another program i, e. the switch- on- fault has been written, which will be examined in the subsection 5.5.4.

5.5.1 Close-up detection

There are three ways which can be employed to identify a close-up fault:

i) by an over-current detector

ii) by checking for small values of reactances or

iii) by monitoring the voltage samples.

Method (i) is dependent on the loading conditions of the system. On the other hand, the current amplitude calculation will need extra processing time.

Method (ii) is reliable and independent of the network characteristics, but it needs considerable processing time, because the implemented algorithm does not compute the actual value of the reactance.

Method (iii) checks every voltage used in the six impedance calculations, i. e. V_a, V_b, V_c, $V_A=V_b-V_c$, $V_B=V_c-V_a$, $V_C=V_a-V_c$. If any of them has been found below

a predefined limit for two successive sampling intervals, then a close- up fault is diagnosed. The threshold voltage below which a fault is classified as close-up depends on the resolution of the A/D converter and on the attenuation of the voltage signal. Knowing these parameters, the minimum voltage, which leads to accurate impedance calculations can be found. Below this voltage the fault has to be classed as a close- up. Typical reach of the close- up detector is about 5 miles for a 100 miles long line.

In fig. 5.6 the subroutine " CU " detects the occurence of close-up faults. If one of the voltages collapses below the threshold limit, then a flag is set (CUF) and at the same time the corresponding close-up phase flag is set according to the table 5.2.

TABLE 5.2

Voltage < Threshold	Type of close-up fault
V_a	R-G
V_b	Y-G
V_c	B-G
V_A	Y-B
V_B	B-R
V_C	R-Y

Some other operations also take place, which are concerned with the setting of some pointers for calling the corresponding prefault voltages.

5.5.2 The voltage update routines

As has been discussed previously, the memory voltage principle has been applied, therefore a sub-routine which stores the samples over a cycle is needed. Because the incoming samples after the fault occurence will overwrite previous data, it is necessary to store the samples for two cycles. Such a process needs 48 data locations. The initial design of the processor however included 128 data locations, therefore a different method was required with less storage. As it takes less than a half cycle to classify a fault as a close-up, storage of voltage for 1 1/2 cycle will be sufficient. By following this procedure, the program becomes more complicated and more processing time is consumed.

Fig. 5.6 shows the flowcharts of the subroutines used by the close-up algorithm. The subroutine STORE saves the voltages of the 3 phases in a data block arranged in a ring mode.

Because of the direct addressing applied to the data store, modifications of the subaddress bus are not possible. A pointer is assigned to address different sections of the main program, each one specifying explicitly the addresses of the voltage samples data store. The control of this pointer is implemented by an indirect indexing mode as discussed in chapter 3.

When a fault is classified as close-up, the

STORE routine is disabled, and the routines PFNI, PFC are used to control the substitution of the sample voltages by the corresponding prefault voltages. These two programs would be much simpler if the voltages are stored for two cycles. Fortunately the next version of the digital relay will include 512 data locations, this procedure becomes possible, thus simplifying the program.

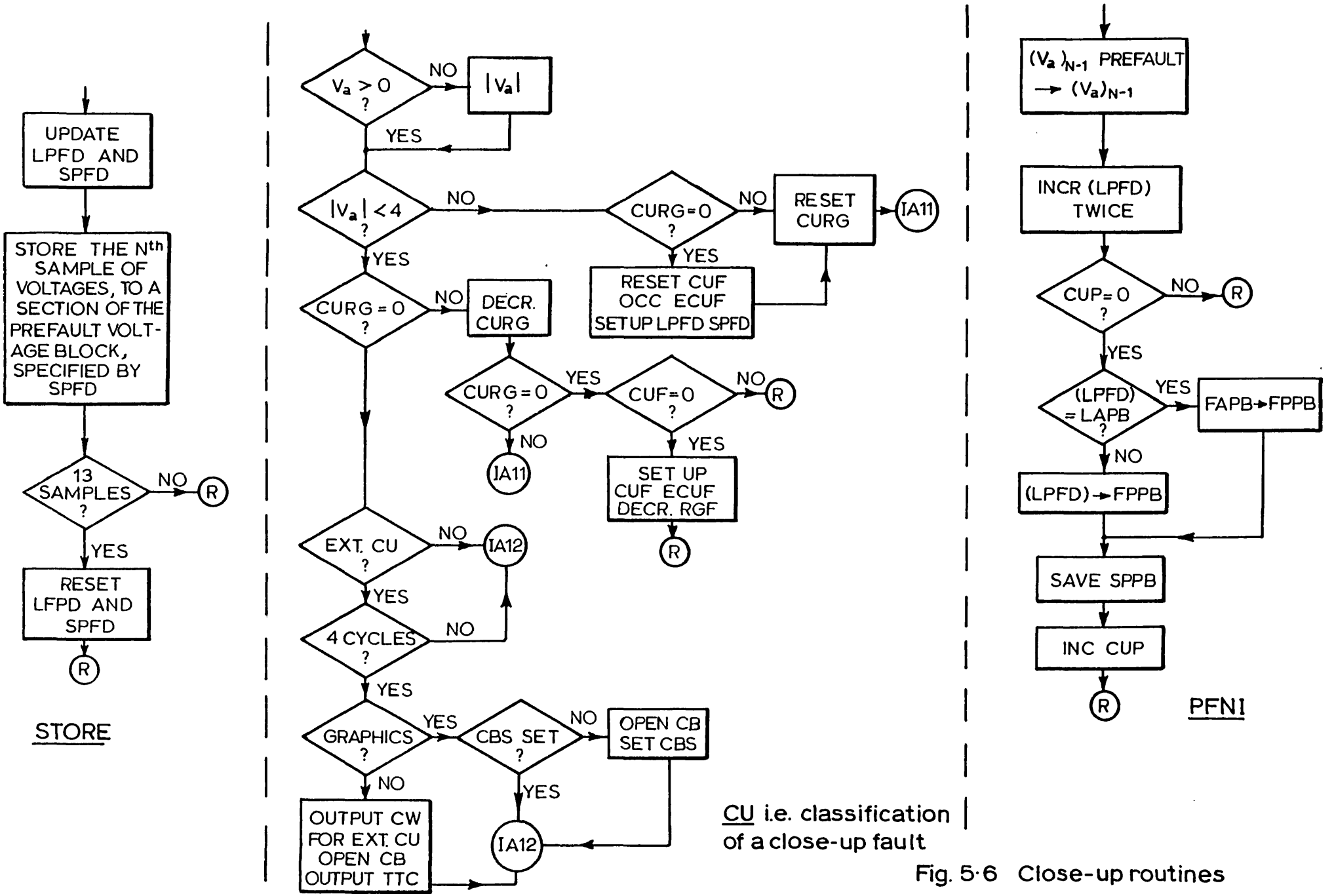
5.5.3 The impedance calculation for close-up faults

Holden and Morrison[74] have shown that by using the corresponding prefault voltage samples in place of the real ones, a pseudo - impedance can be calculated. This value is meaningless, but its sign defines the position of the fault i. e. in front or behind the relay.

In the impedance calculation routine, a check is made, if the close-up fault flag is set, following which the signs of the quantities N_L and D are checked. If N_L and D have the same signs, then the fault is internal, while for N_L and D with different signs, the fault is external and the ECUF (external close-up flag) is set. As a back-up facility, the relay opens the CB, if the external fault persists for a specified number of cycles.

5.5.4 Switch- on- fault (SOF)

The " SOF " subroutine, shown in fig. 5.6 runs only for the first cycle after the instant of the CB



CU i.e. classification of a close-up fault

Fig. 5·6 Close-up routines

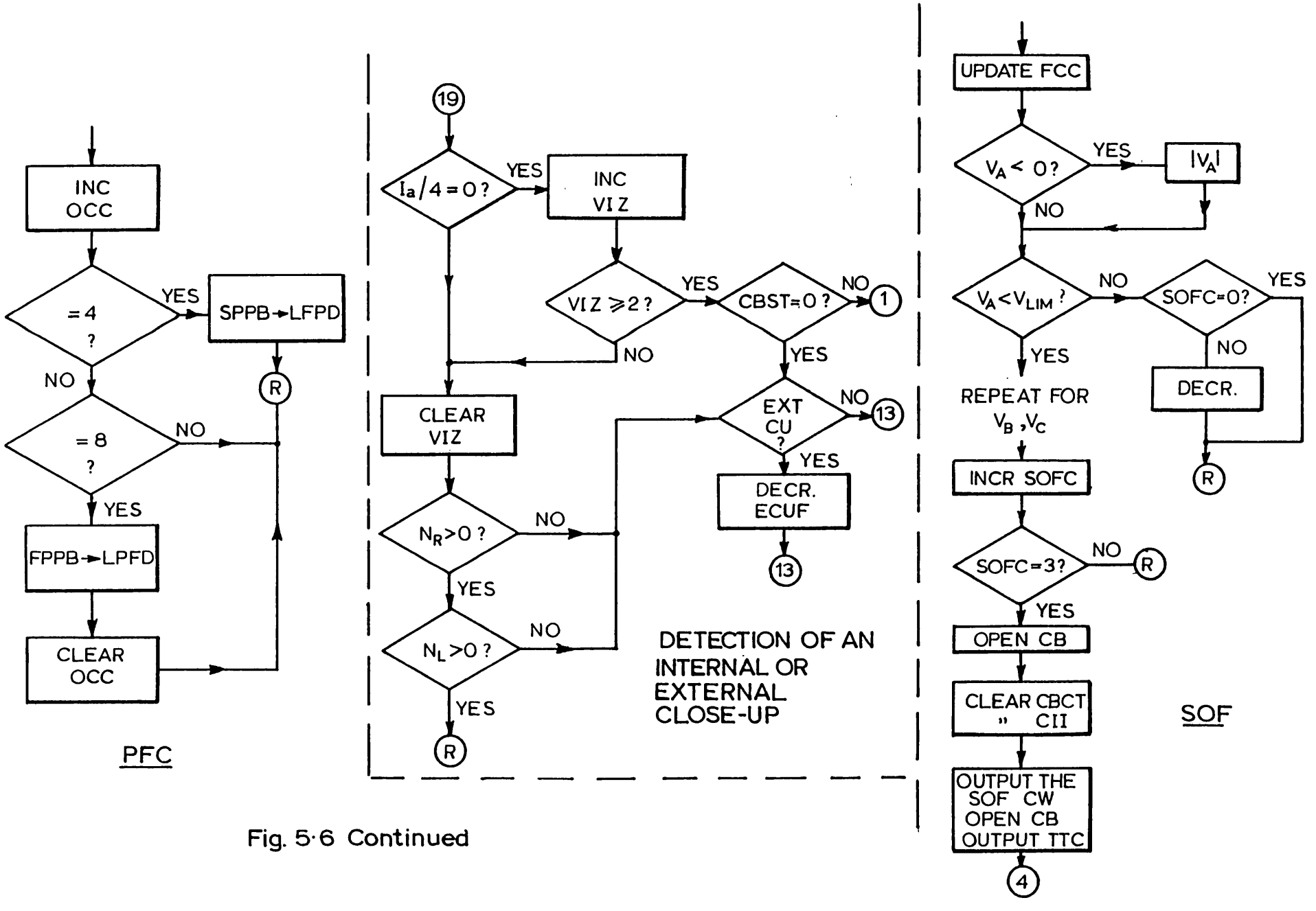


Fig. 5·6 Continued

switching-on. If the voltages V_A, V_B, V_C are below a limit, then a 3- phase close-up fault is present on the line. Identification of such a condition for 3 consecutive instants, generates a trip signal to the CB and the message of fig. 5.13e is typed on the teletype.

5.6 Out-of-step blocking

In chapter 2, the problem of blocking the CB under a power swing condition has been discussed. Discrimination between a fault and a power swing is achieved because the impedance seen by the relay during a power swing varies slowly. Therefore in fig. 5.7 the impedance during a fault moves from A to B almost instantly, while a predefined time delay is normally associated with the same movement during a power swing. Two settings have to be specified i. e. R_b and φ . Point A corresponds to a machine angle which must not encroach the steady-state load conditions of the system. Therefore for the specific source impedances and e.m.f's, R_b can be defined. The angle φ can be the same as that for the right- hand side of the trip characteristic. The second limit of the power swing locus is the right-hand side of the quadrilateral characteristic.

According to the mean speed of swing between the points A and B, the mean time required to traverse between these two points can be defined. Fig. 5.8 shows the flowchart of the out-of-step blocking program. The

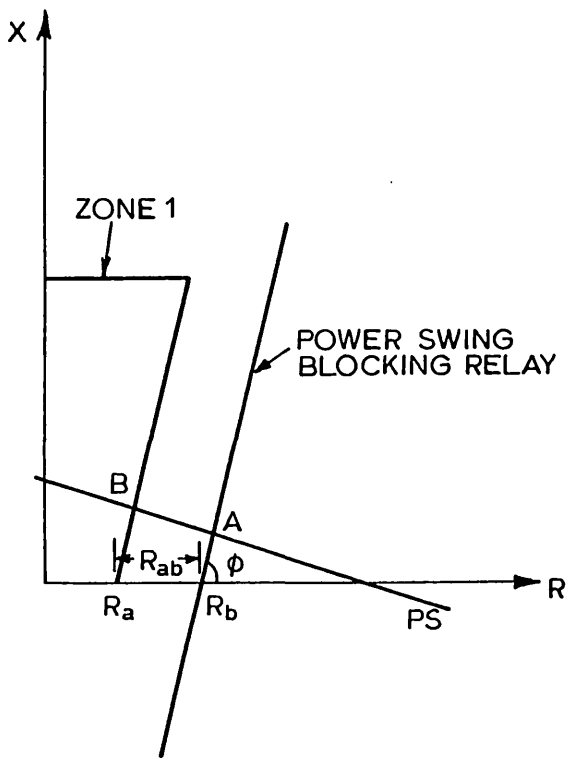


Fig. 5·7 The out-of-step blocking relay

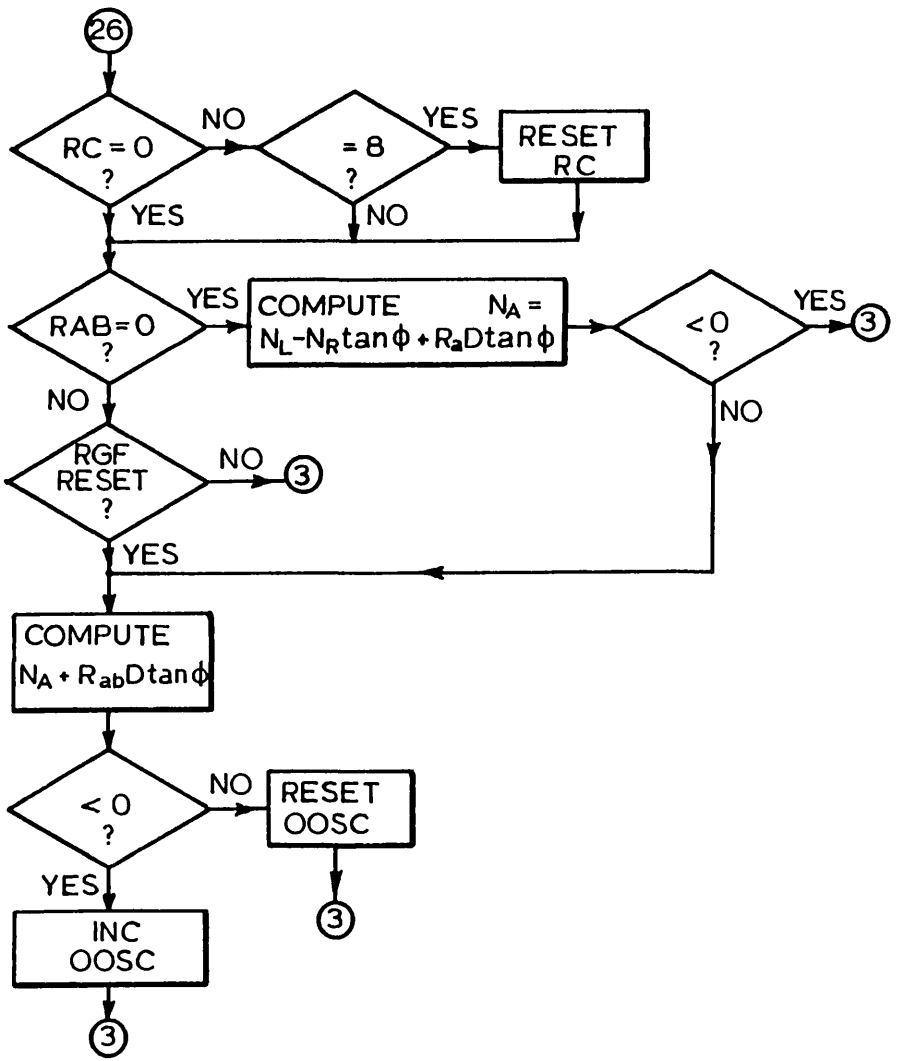


Fig. 5·8 Out-of-step blocking program

OOSC (out-of-step counter) is incremented as long as the operating point lies somewhere between A and B. The two checks are:

$$N_A = N_L - N_R \tan\varphi + R_a D \tan\varphi > 0 \qquad (5.15)$$

for $D < 0$

and

$$N_L - N_R \tan\varphi + R_b D \tan\varphi < 0 \qquad (5.16)$$

To save computation time, as $R_b = R_a + R_{ab}$, eq. (5.16) is written:

$$N_A + R_{ab} D \tan\varphi < 0 \qquad (5.16a)$$

As can be seen in fig.5.3a, when the operating point moves inside the polar characteristic the value of OOSC is checked. If it is smaller than the predefined limit the relay trips, otherwise the trip decision is blocked and the program continues its normal looping.

The out-of-step blocking relay has been implemented for one phase only, because a power swing is a three-phase condition.

5.7 Active and reactive power measurement

In chapter 4 it has been found that:

$$N_R = -\hat{V}\hat{I}\cos\varphi$$

$$N_L = -C\hat{V}\hat{I}\sin\varphi \qquad (5.17)$$

where C is the correction factor.

If eq. (5.17) are divided by -2, then the r.m.s. active (P) and reactive (Q) power flowing from or to the

relaying point can be computed. To obtain the 3-phase power values, the corresponding values of N_R and N_L for the RG, YG and BG calculations have to be added.

In chapter 4, the variation of N_L with loads having power factors close to unity has been discussed. To achieve a reliable measurement of P and Q, the average of N_R and N_L is taken over a cycle.

Fig. 5.9 shows the routine PQM, which controls the computation of P and Q. Information required in the fault report includes the prefault values of P and Q for which, these values have to be stored for three consecutive cycles. Fig. 5.9 shows, how the relay outputs to the monitoring computer values of P and Q upon a request from the operator.

5.8 The post-fault routine

After a fault has been detected, the relay sends a command to the CB , but the CB contacts remain closed for the next 2 cycles. Therefore during the first cycle after fault detection, reliable computations can be still carried out thus obtaining a more accurate result.

During this cycle a more accurate calculation of the position of the fault is determined. The subroutine " SELECT ", shown in fig. 5.10 runs the impedance algorithm calculation initiating the trip command, and its average is taken over one cycle.

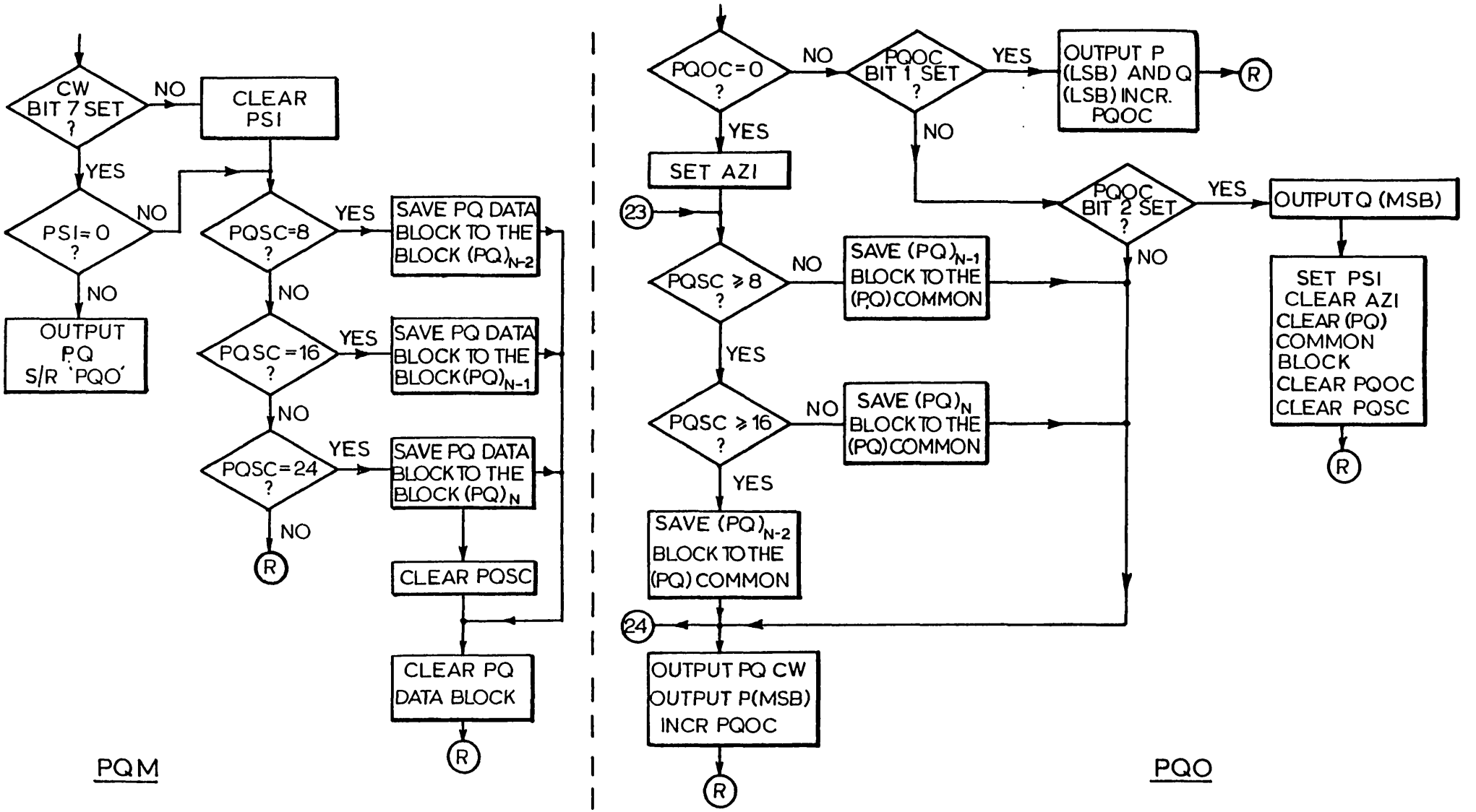


Fig. 5·9 The flowcharts for the P and Q measurements

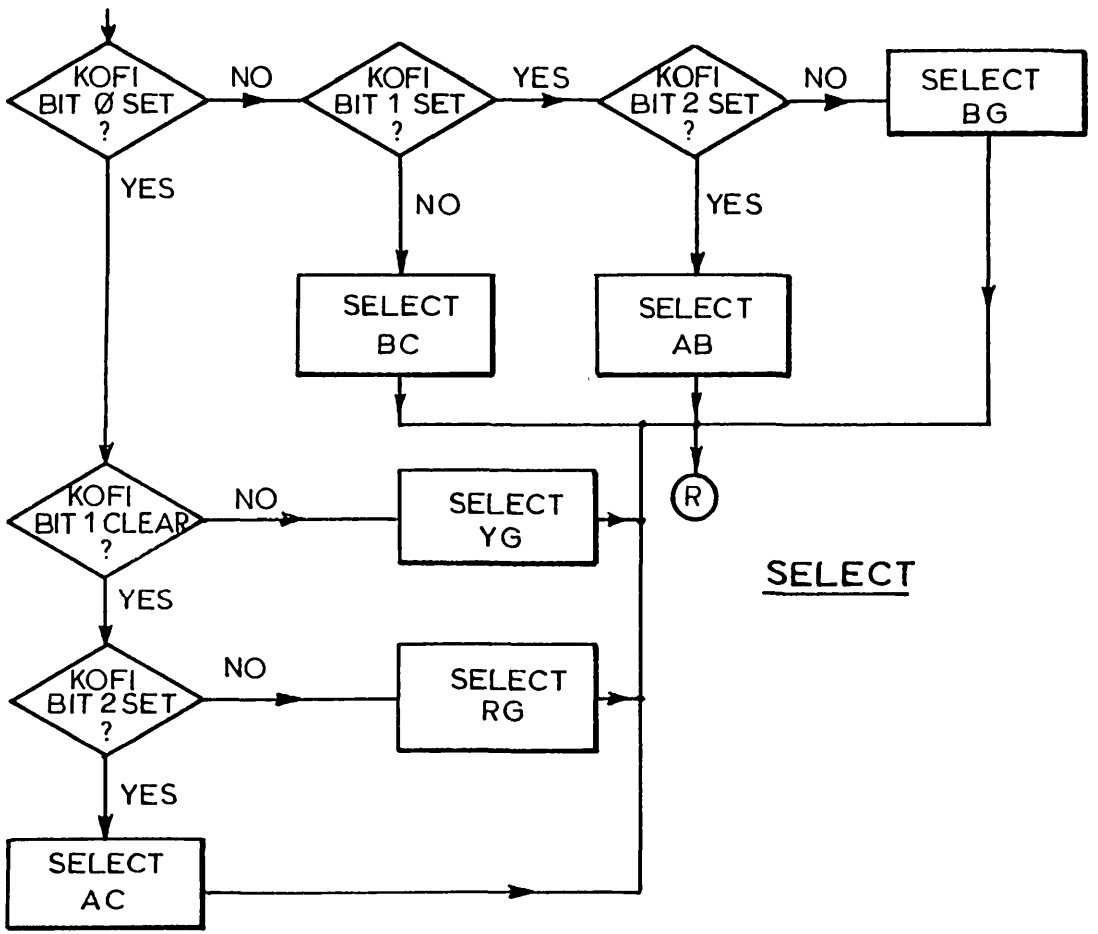


Fig. 5·10 Identification of the impedance algorithm, which has initiated the trip command.

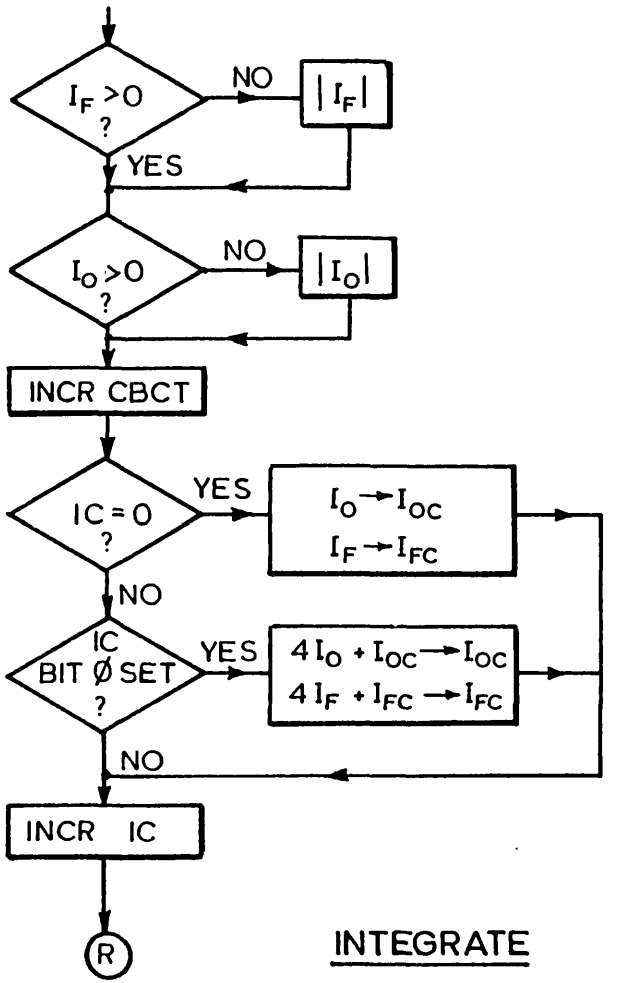


Fig. 5·11 Simpson's integration routine.

At the same time the r.m.s values of the fault current at the relaying point and the residual current are computed, from the equation (5.18)

$$I_{rms} = \frac{\pi}{T\sqrt{2}} \int_0^{T/2} \hat{I} \sin\omega t \, dt \qquad (5.18)$$

For a more accurate calculation of these currents, the integration is performed using Simpson's method[76] i.e.

$$\int_a^{a+2hn} f(x)\,dx = \frac{h}{3} \{f(a)+4f(a+h)+2f(a+2h)+4f(a+3h)+\cdots+f(a+2hn)\} \qquad (5.19)$$

where a is the starting sample,

h the sampling interval = $\frac{\pi}{4}$ for 8 s/c and

f(x) is defined by equation (5.18).

Fig. 5.11 shows how this integration has been implemented in the microprocessor. Finally the type of fault is classified, according to the values of the six counters assigned to each of the six impedance calculations, and identified according to table 5.3.

The post-fault program is organised as in fig. 5.12. At the end of this post-fault cycle, the dedicated relay outputs to the monitoring computer the information shown in fig. 5.12, to be used by the report program, discussed in the following section. After that, the program waits in a loop, until the CB opens its contacts, stopping the CB clearance time counter, so the CB

TABLE 5.3

CLASSIFICATION OF THE FAULT TYPE

COUNTER / FAULT	R-G	Y-G	B-G	B-Y	R-B	Y-R
R-G	✓					
Y-G		✓				
B-G			✓			
B-Y				✓		
R-B					✓	
Y-R						✓
B-Y-G		✓	✓	✓		
R-B-G	✓		✓		✓	
Y-R-G	✓	✓				✓
R-Y-B				✓	✓	✓
R-Y-B-G	✓	✓	✓	✓	✓	✓

Note: ✓ means corresponding counter = 0

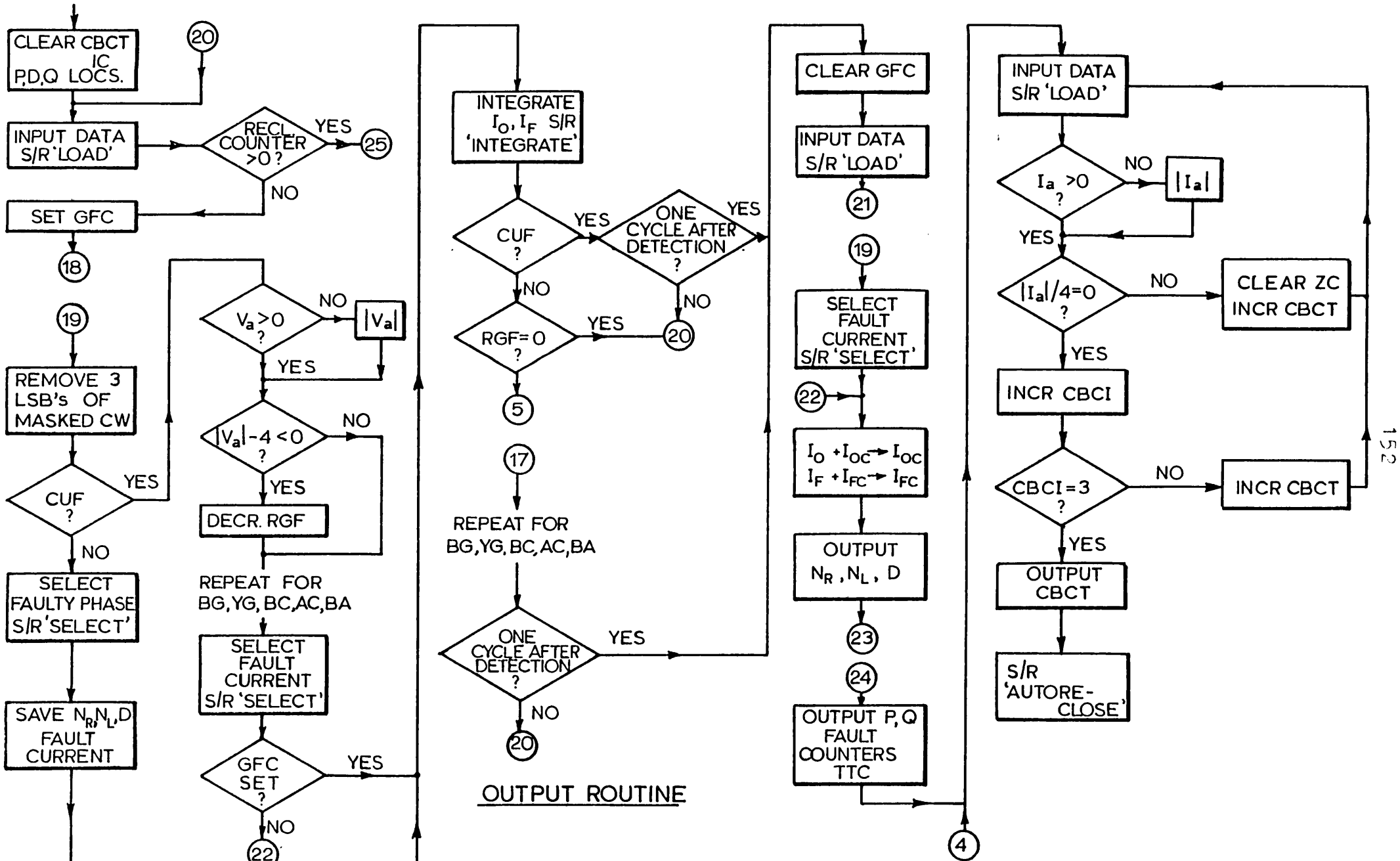


Fig. 5·12 The post-fault routine

operating time can be reported. The program then exits from this routine to the autoreclosing program discussed in the section 5.10.

5.9 The report program

One of the advantages of digital protection is the information that can be obtained about the status of the power network as seen at the relaying point.

This information is processed offline by the monitoring computer. The available reports printed on the teletype are shown in fig. 5.13.

In fig. 5.13a, b, c typical reports for a fault inside the line are shown. Fig. 5.13d indicates that the autoreclose has functioned once, and found that the fault was permanent. Fig. 5.13e has recorded a fault caused by closing the CB onto a line submitted to a 3-phase close-up fault. In the case of a close-up fault, two reports are available, fig. 5.13f refers to an internal fault, while fig. 5.13g applies to an external close-up fault cleared by the line protection after some delay. Therefore operators can be kept fully informed of all conditions concerning the fault inception.

Fig. 5.13h is typed to an operators request for the active and reactive power measurement.

In case of failure of the relay hardware, the message of fig. 5.13i concerned with the measurement of the reference voltage is outputed.

```
***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
LINE FAULT
RESISTANCE=     0.898 OHMS     REACTANCE=     1.912 OHMS
DISTANCE=     64.75 MILES
FAULT:RED/BLUE
FAULT CURRENT=    10.749 AMPS RMS
RES.CURRENT=     0.195 AMPS RMS                                    (a)
P=      2468.0 W
Q=       256.7 VA
TRIP TIME=            15.00 MSECS
CB CLEARING TIME=    217.50 MSECS
DATE  3/12/78   TIME 11:51:12
TYPE 1 TO ACKNOWLEDGE 1


***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
LINE FAULT
RESISTANCE=     0.675 OHMS     REACTANCE=     0.943 OHMS
DISTANCE=     31.95 MILES
FAULT:RED/BLUE/GROUND
FAULT CURRENT=    11.460 AMPS RMS
RES.CURRENT=    10.087 AMPS RMS                                    (b)
P=      2471.9 W
Q=       263.4 VA
TRIP TIME=            10.00 MSECS
CB CLEARING TIME=   257.50 MSECS
DATE 3/12/78   TIME 11:53:45
TYPE 1 TO ACKNOWLEDGE
```

Fig. 5.13 Reports from the dedicated digital distance relay.

```
***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
LINE FAULT
RESISTANCE=     1.155 OHMS     REACTANCE=     2.878 OHMS
DISTANCE=     97.49 MILES
FAULT:RED/GROUND
FAULT CURRENT=    10.879 AMPS RMS
RES.CURRENT=     8.786 AMPS RMS                              (c)
P=      2492.7 W
Q=       250.6 VA
TRIP TIME=            15.00 MSECS
CB CLEARING TIME=    360.00 MSECS
DATE  3/12/78   TIME 11:35:22
TYPE 1 TO ACKNOWLEDGE 1


***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
CIRCUIT BREAKER LOCKEDOUT BY AYTORECLOSE                    (d)
DATE  3/12/78   TIME 11:39: 8
TYPE 1 TO ACKNOWLEDGE
```

Fig. 5.13 Cont'ed

```
***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
SWITCH ON FAULT
TRIP TIME=              7.50 MSECS
CB CLEARING TIME=     300.00 MSECS
DATE  2/12/78   TIME  7:32:12
TYPE 1 TO ACKNOWLEDGE 1
```

(e)

```
***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
CLOSE UP
FAULT:RED/GROUND
FAULT CURRENT=     11.785 AMPS RMS
RES.CURRENT=      8.818 AMPS RMS
P=       1688.0 W
Q=        238.4 VA
TRIP TIME=             15.00 MSECS
CB CLEARING TIME=     175.00 MSECS
DATE  2/12/78   TIME  7:33:54
TYPE 1 TO ACKNOWLEDGE 1
```

(f)

```
***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
EXT. CU CLEARED BY LINE PROTECTION
TRIP TIME=            100.00 MSECS
CB CLEARING TIME=     370.00 MSECS
DATE  2/12/78   TIME  7:35:49
TYPE 1 TO ACKNOWLEDGE
```

(g)

Fig. 5.13 Cont'ed.

```
***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
PQ MEASUREMENT
P=      2471.4 W
Q=       257.6 VA                                    (h)
DATE  2/12/78   TIME  6:56:33
TYPE 1 TO ACKNOWLEDGE 1

***RELAY MONITOR 11/9/78***
DISTANCE RELAY NO=1
MEASUREMENT ERROR
REF.VOLTAGE=-10.00 CORRECT VALUE=+6.19              (i)
DATE  2/12/78   TIME  6:57:32
TYPE 1 TO ACKNOWLEDGE
```

Fig. 5.13 Cont'ed.

5.10 Autoreclosing

Statistics of faults on overhead lines show that 80 - 90 % of them are transient, so that after the deionization of the fault, reenergisation of the line will restore healthy conditions. Therefore, if the CB is tripped out, and reclosed again after some delay, then the transient fault will be cleared succesfully. If the fault is permanent, the reclosing operation will be unsuccesful, and the CB must trip again. Usually in EHV lines, only one reclosure is permitted (single-shot autoreclosing), the CB being locked out after an unsuccesful reclosure.

For autoreclosing the following five parameters need to be defined:

i) The dead time, equal to the CB operating time plus the deionization time of the fault. Fig. 5.14 shows that during this time delay, the program stays idle inside a loop. After this time has been expired, a command to switch-on the CB is sent.

ii) The reclosing impulse time, which depends on the CB closing time. After that time the program starts again.

iii) The reclaim time. As can be seen in fig. 5.8, if no fault has been found during the first cycle, after the CB has reclosed its contacts, the flag RC is cleared (autoreclose is reset).

This time interval is the reclaim time. Fig. 5.3a, 5.12 and 5.14 show that,if a fault is found during this interval, the CB opens again and is locked out.

iv) The implemented scheme permits a single-shot autoreclosing. In a multi-shot scheme the locking-out happens after the CB has opened for the specified number of times.

v) Single- phase of poly- phase tripping. In the case of a single-phase fault, it would be better if only the faulted phase is tripped, such that interchange of power can take place through the healthy phases. Such a configuration is implemented easily, as there is no starting element.

The program written in the digital distance relay implements a simple three-phase, single- shot autoreclosing scheme.

5.11 The self- test monitoring program

The analogue data sampled by the data acquisition unit includes a reference voltage derived from a resistive network to all four power supplies. This value is 6.19V. The processor tests if the reference input stays between ±5% of the correct value. The flowchart of this program is shown in fig. 5.15.

In an event of a failure the report of fig. 5.13i is outputed to the monitoring computer. After that the program enters a wait loop until the failure has been

acknowledged.

5.12 The graphics routine

This routine can be used for testing the relay performance. It is not necessary as a standard feature of the relay, unless it is desired to be used as a diagnostic to check the correct operation of the microprocessor. Different types of data can be plotted according to the way the switches are set on the control panel. Table 5.4 gives the available features of the graphics routine.

TABLE 5.4

SELECTION OF THE REQUIRED PLOT

PLOT	SET SWITCHES
Trip signal and V,I as seen by the algorithm.	A§, 11, 16
V or I of the three phases	14(13), 16
Filtered/unfiltered data	B§, 12, 16
R and X versus time	A§, 16

§ A and B is 1 or 2 or 3 or 4 or 5 or 6, where

1 corresponds to R-G for A and V_a for B
2 " " Y-G " " " V_b " "
3 " " B-G " " " V_c " "
4 " " Y-B " " " I_a " "
5 " " R-B " " " I_b " "
6 " " R-Y " " " I_c " "

Fig. 5.16 describes in a flowchart the way the above plots are serviced.

Using these graphics the relay performance has been tested, the result being shown in the following chapter.

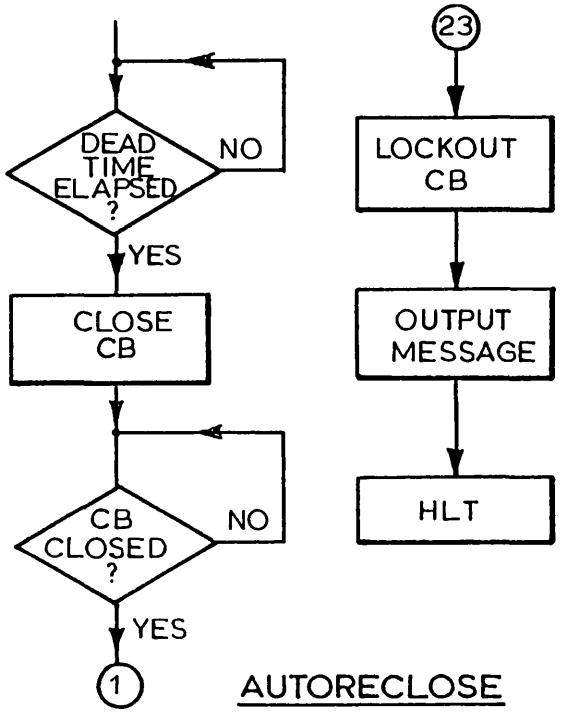


Fig. 5·14 The autoreclose routine

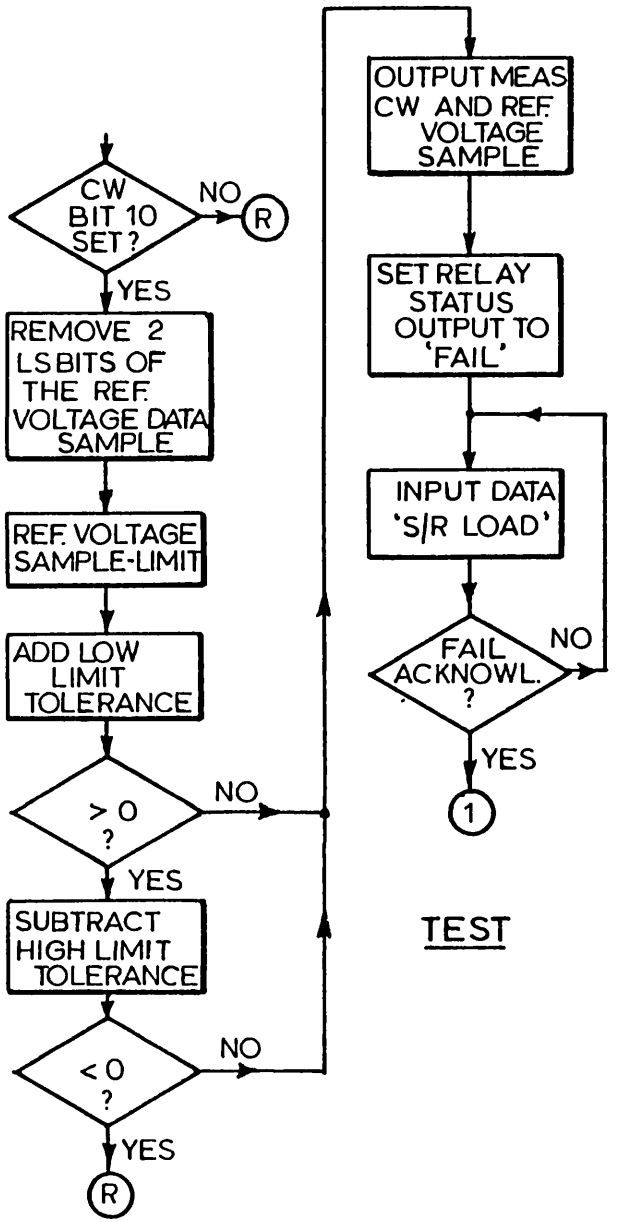


Fig. 5·15 The self-test monitoring program

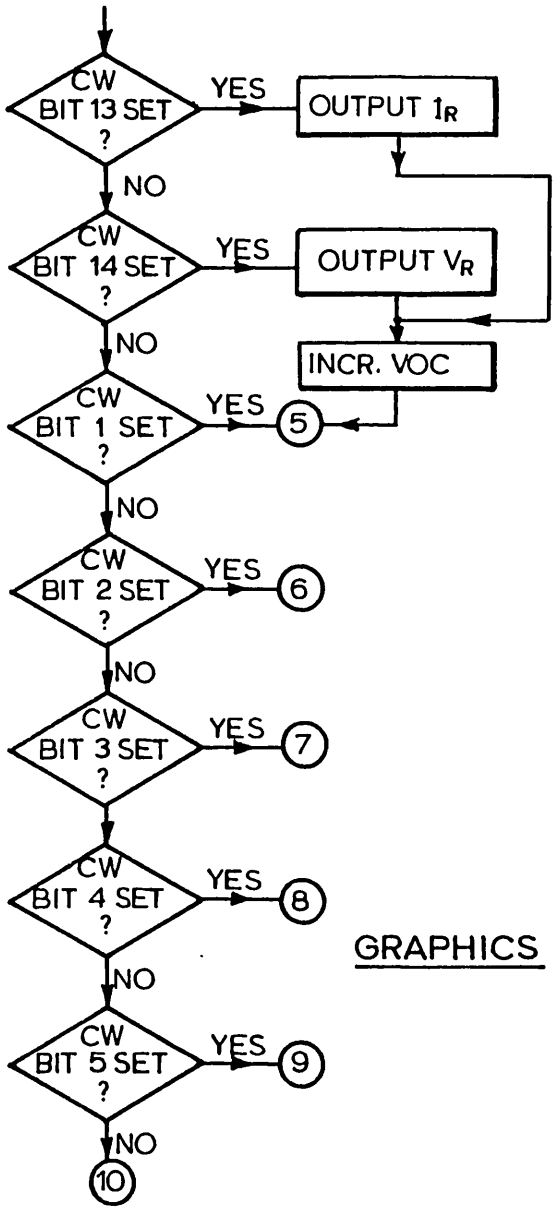


Fig. 5·16 Graphics routine

CHAPTER 6

EXPERIMENTAL RESULTS

6.1. Introduction

A digital distance relay should be satisfactory if it fulfills the following qualities:

i) Reliability

The advantages in terms of reliability of employing digital techniques have been discussed in chapter 1. Software in this relay has been kept as simple as possible by choosing a simple algorithm and by eliminating the need of starting elements. In addition a monitoring program has been written which checks the correct operation of the digital relay.

ii) Selectivity

The relay should only trip for faults inside its defined zone. For single-phase autoreclosing, the correct detection of the faulty phase is essential. As discussed in chapter 5, this goal has been achieved by ensuring that the reactance and resistance seen by the relay are inside the specified polar characteristic. Care has been taken to avoid unnecessary tripping during a power swing.

iii) Reach accuracy and fast response

Ideally a distance relay should operate at the shortest possible time (less than a cycle) with an accuracy of $\pm$ 5% of its reach. In addition its reach should be

independent of the actual values of voltage and current at the relaying point i.e.independent of the fault position and the source impedance. On the other hand, the most serious faults are those close up to the relaying point. Therefore a small increase in its operating time as the fault moves towards the far end of the line is permissible.

Existing distance relays are specified in terms of a basic operating time, but these times vary depending upon the fault position and the values of voltage and current i. e. on the ratio Z_S/Z_N, where Z_N is the nominal setting of the relay and Z_S the source impedance. Therefore curves of the form of fig. 6.1 are produced, which show that for a short line with a large source impedance behind it, the operating time increases due to the low voltage present at the relay terminals, when Z_S/Z_N is large. Existing relays can be sensitive down to about 3 V, with a normal secondary source voltage of 110 V.

The following sections describe the tests carried out on the digital relay for a fixed source impedance and a variable fault position.

The main characteristics to be considered are the detection time, discrimination and the correct fault type classification. Tests have been performed with the midpoints formula and the sample and midpoint method,

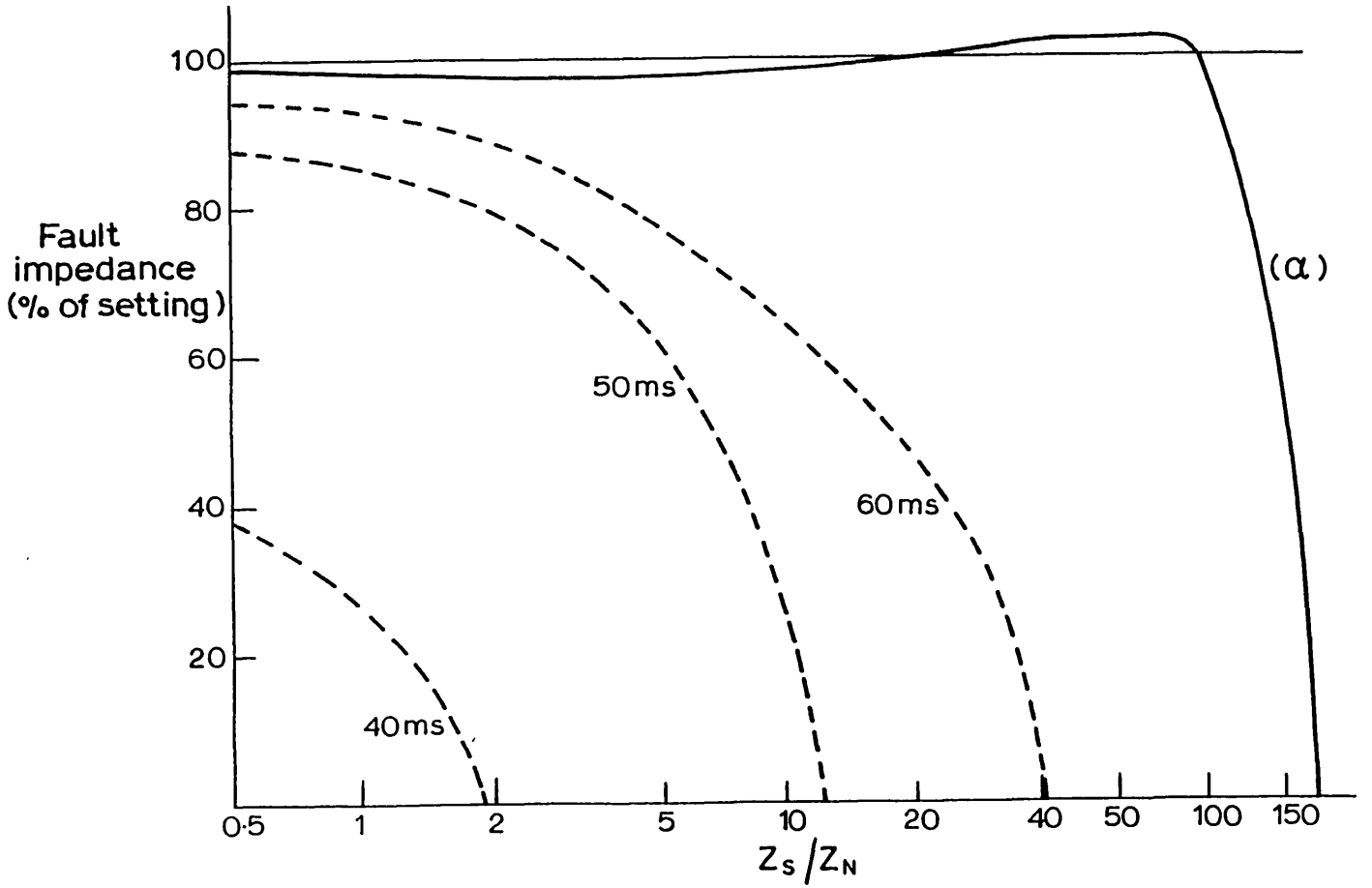


Fig. 6·1 Performance graph of a distance relay

and their relative performance compared.

For the shown tests $Z_S/Z_N = 5$ and an increase in this ratio, will produce a slight increase in the operating time, which can be kept small than that of existing relays by using the gain ranging amplifiers mentioned in chapter 3.
So the operating times achieved will be of the same order as those presented below. Such tests have not been carried out, because the initial design of the data- acquisition unit did not incorporate signal ranging amplifiers although the processor provides the necessary capabilities for handling the range bits.

6.2. The relay performance under different types of fault

Initially performance for distant, faults has been examined because there accurate performance is more critical. Later on the performance for faults at different positions along the line will be examined.

During these tests, the values of Z_S and Z_L were $(2.6+19.6j)\Omega$ and $(1.15+4.2j)\Omega$ respectively, therefore the $\frac{X}{R}$ was equal to 6.35, implying that the exponential reaches 1/3 of its value in a little more than a cycle.

Higher harmonics were not possible to be generated on the test equipment, but the performance of the analogue and digital filters used, should have

eliminated them, as has been demonstrated in chapter 4.

The detection times mentioned are in multiples of samples.

In the following figures, the nomeclature is as follows:

1 - Result using the first algorithm with a $\cos\varphi = 0.997$

2 - " " " second " " " "

3 - " " " first " " " $= 0.966$

4 - " " " second " " " "

The small letter following means:

a: Fault detection time: This signal is zero during normal operation. When the fault is applied, it goes high and it goes down again, when the processor has detected the fault.

b: The current waveform, in compensated form used by the algorithm. The d.c. offset can be seen in this curve and the relative ratio of prefault and fault current.

c: The compensated voltage waveform.

d: The reactance variation with time. The prefault variation of the reactance, as discussed in chapter 4 , can be seen. When the fault occurs, a large spike occurs and finally the value settles down to the new value.

e: The resistance variation with time.

Unfortunately, throughout the tests the point--on-wave apparatus was not working reliably and so the faults have been applied manually by a switch. But from the voltage and current waveforms, the inception angle can be found and is given in the diagrams.

Fig. 6.2 refers to a R-G fault at the end of zone 1. It can be seen that both algorithms give almost the same detection time. There is no difference in the detection time for loads of different power factor. During normal operating conditions with a power factor close to unity, it can be seen that the reactance might move inside the limit, but the relay will still be stable as:

a) Three successive points inside the limit are required for a trip decision.
b) The resistance will be well outside the trip characteristic.

Similar results have been recorded for different types of faults. The R-Y fault in fig. 6.3 shows similar behaviour.

Fig. 6.4 gives the result of a R-Y-G fault. During such a fault, three impedance calculations see the fault i.e.the R-G, the Y-G and the R-Y. Although it may take different times for each one to detect the fault, the relay trips on the one which first moves inside the tripping area. As it has been discussed in

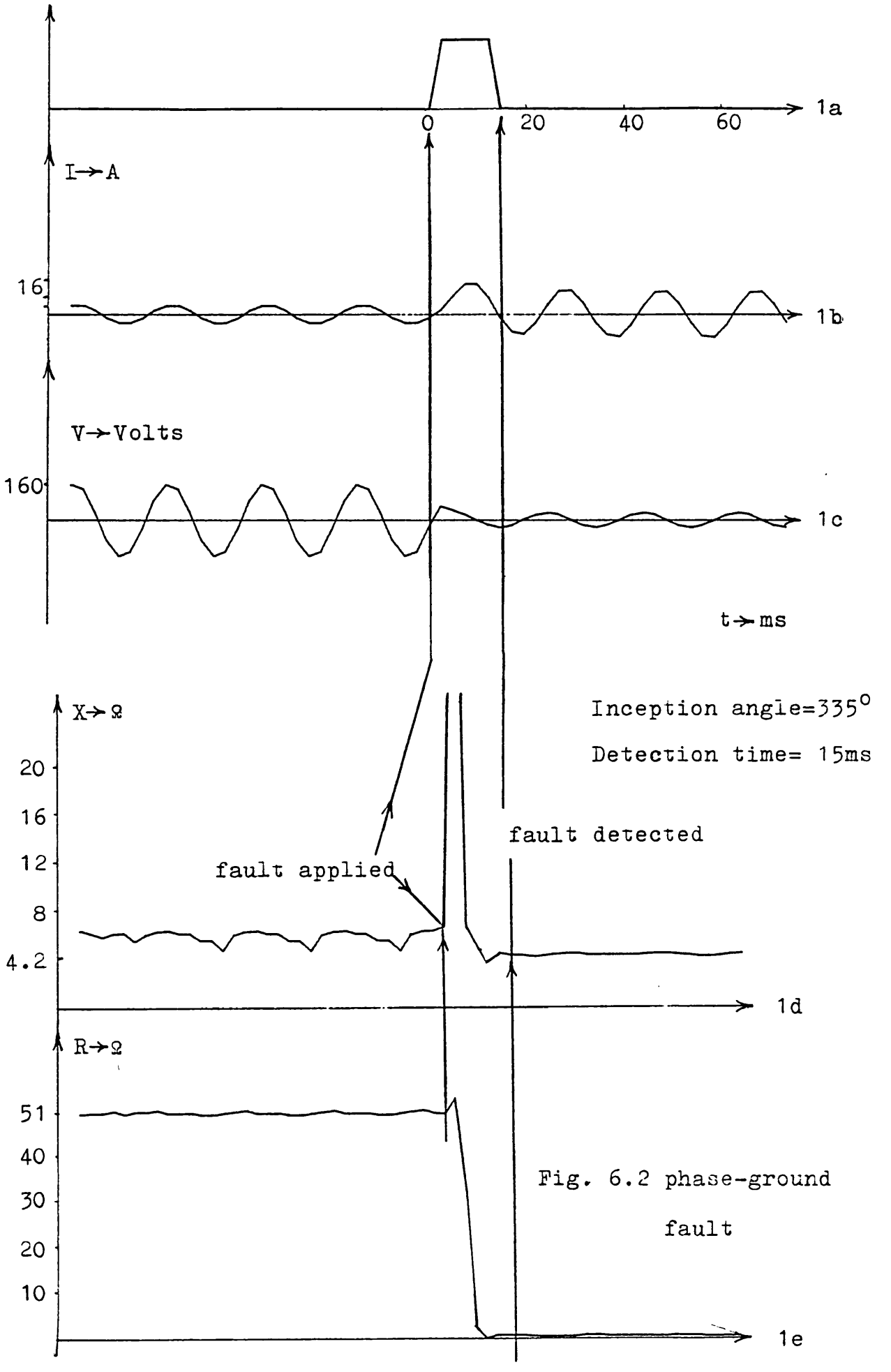


Fig. 6.2 phase-ground fault

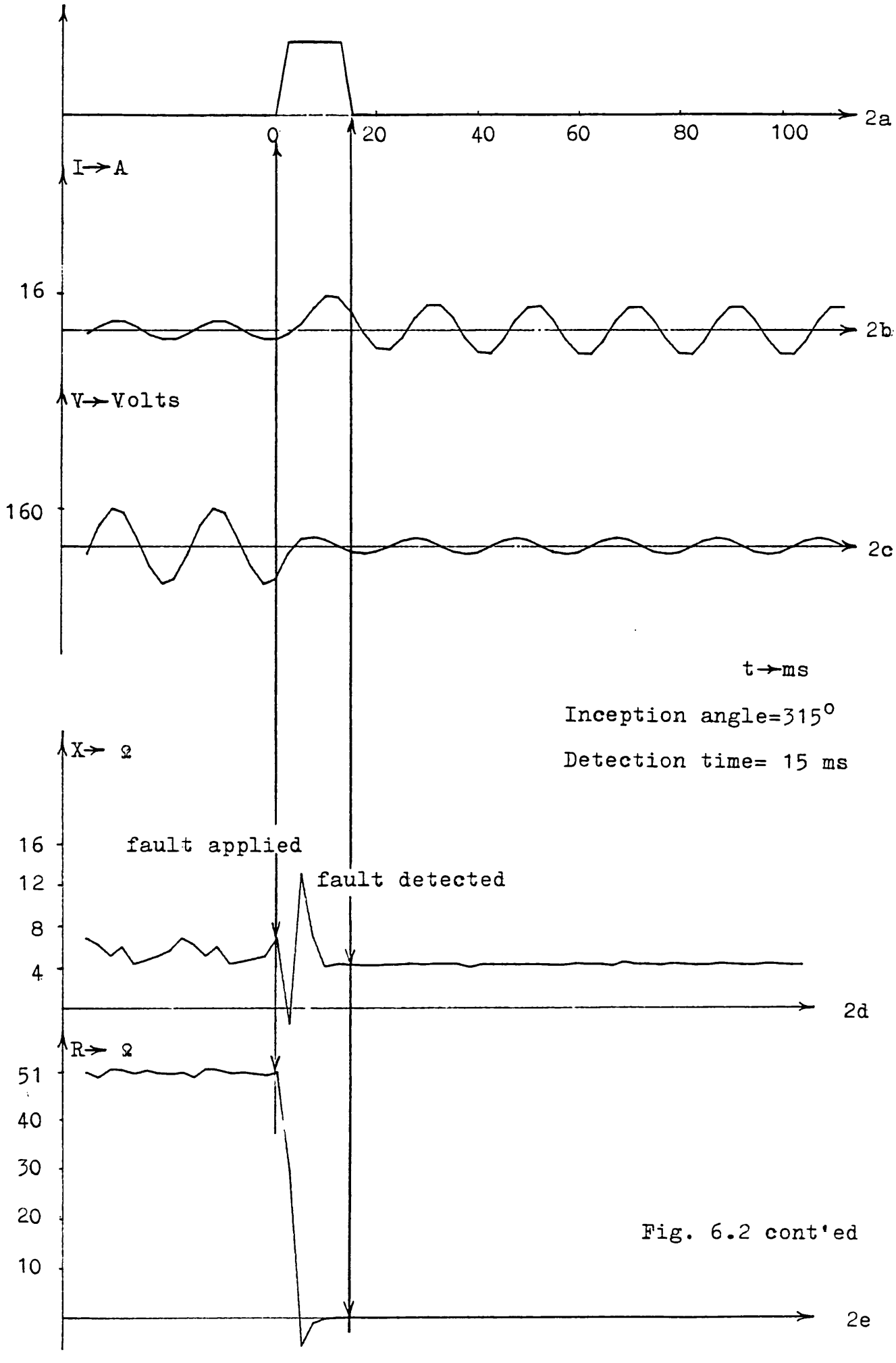


Fig. 6.2 cont'ed

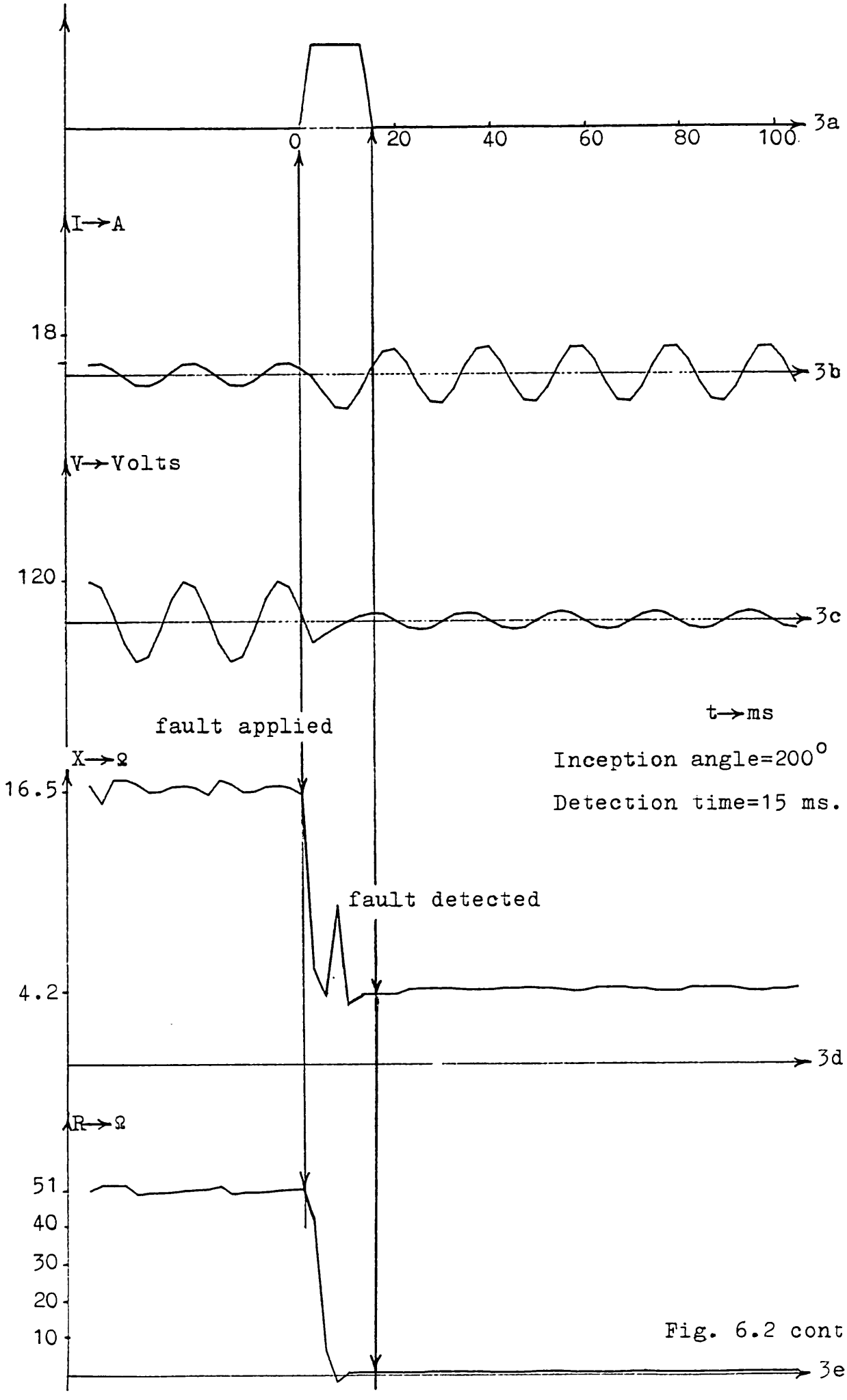


Fig. 6.2 cont'ed

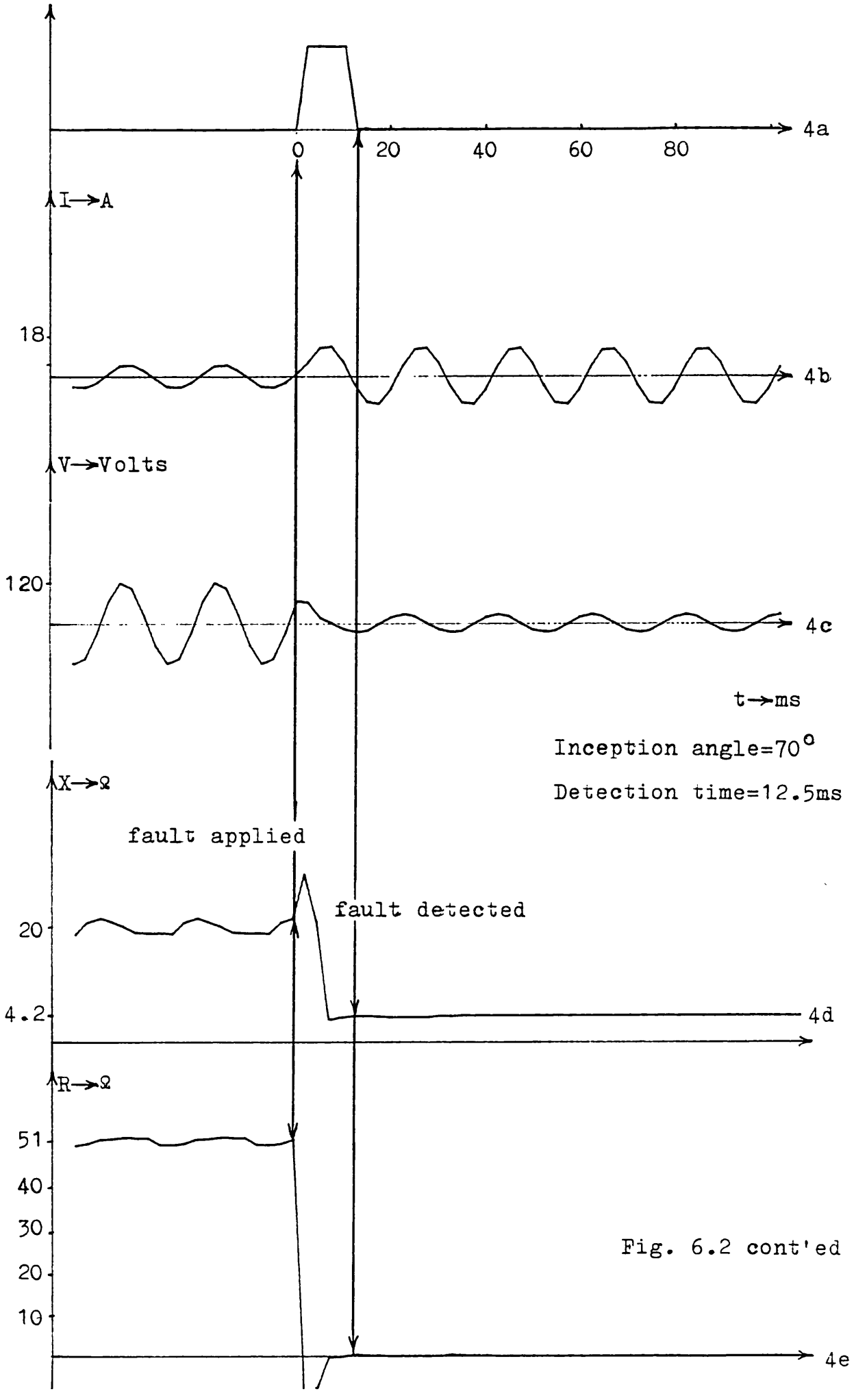


Fig. 6.2 cont'ed

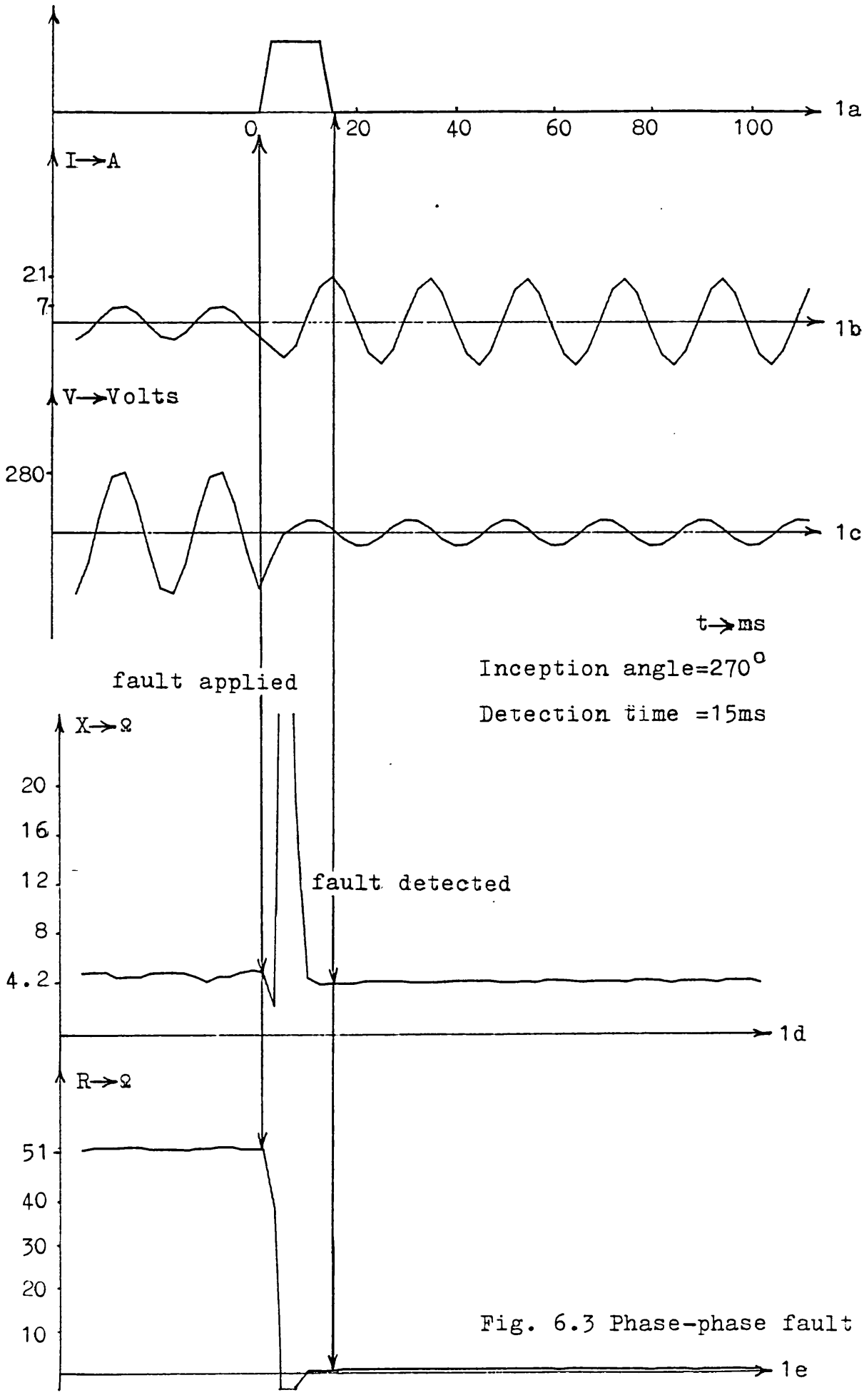


Fig. 6.3 Phase-phase fault

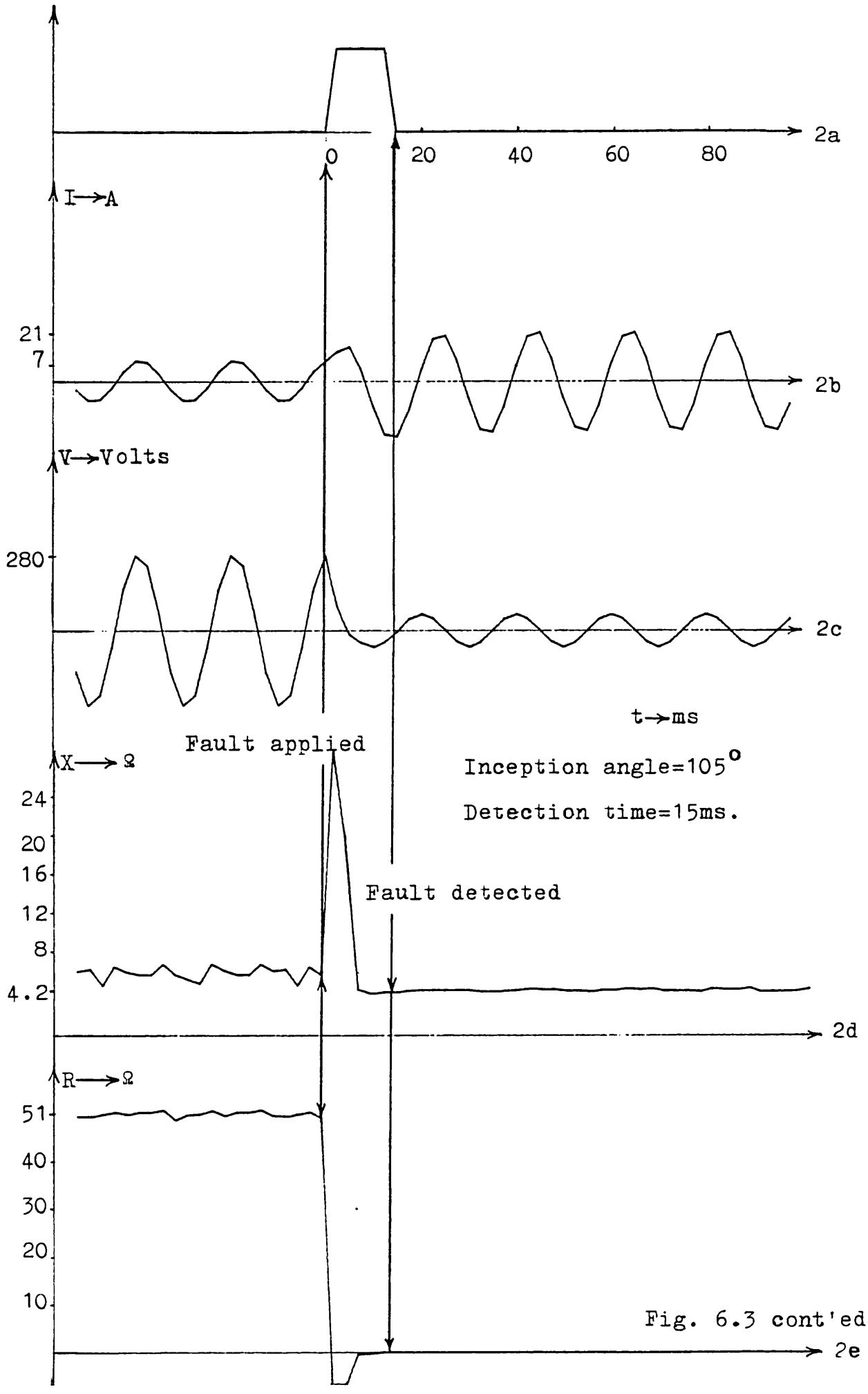


Fig. 6.3 cont'ed

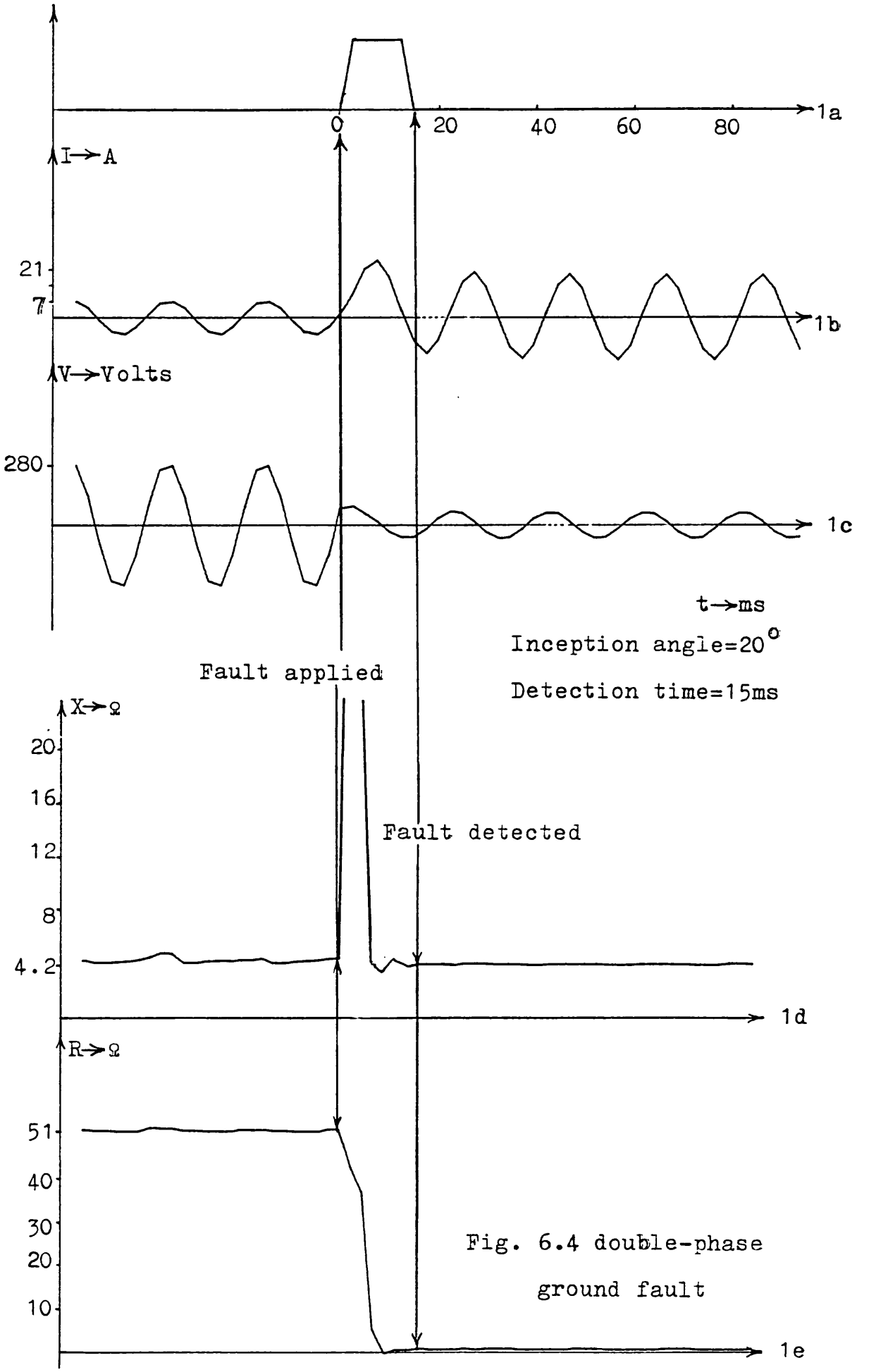


Fig. 6.4 double-phase ground fault

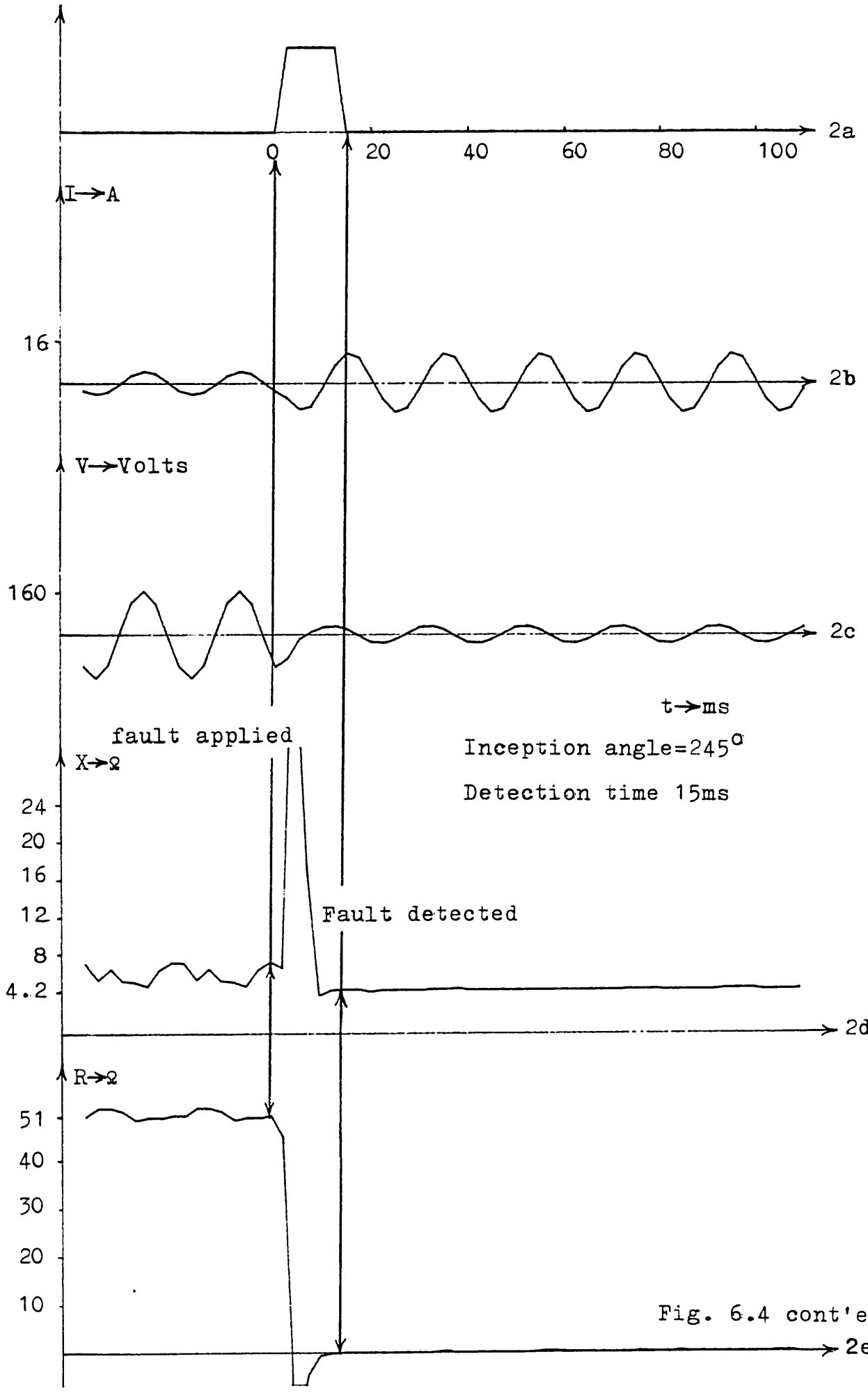


Fig. 6.4 cont'ed

chapter 5, the calculations continue for one cycle after the fault, therefore a correct classification of the type of the fault present on the line is achieved. Fig. 6.4.1 has been recorded as a R-Y fault, while 6.4.2 as Y-G fault.

Fig. 6.5 shows a three phase fault, in which the same comments apply.

Fig. 6.6 shows the case of a three-phase fault, but this time with digital filtering applied. An increase of about 2.5ms in the detection time can be noticed.

6.3. Close-up faults

The curves shown in fig. 6.7 apply to the case of a close-up fault at the relaying point. In fig. 6.7a the fault was in front of the c.t., where the voltage exhibits severe collapse.

The instant, the fault is classified as close-up, the prefault voltages are used in the subsequent calculations. The detection time was 10ms.

Fig. 6.7b applies to a fault behind the c.t., where current reversal can be noted. The relay remains inoperative, but as a back-up facility has been included, the relay trips in 4 cycles, because the busbar protection relay has failed to clear the fault.

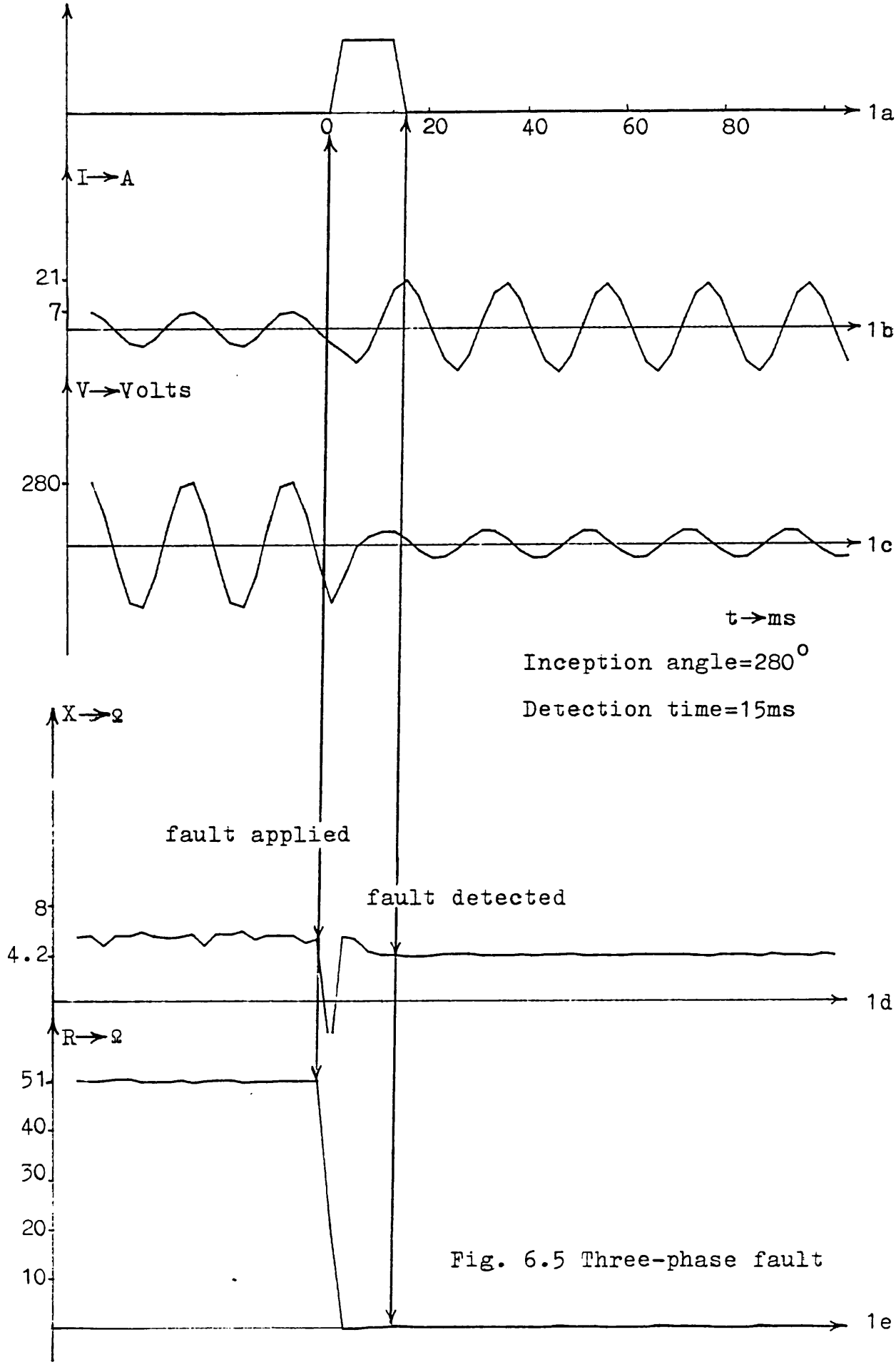


Fig. 6.5 Three-phase fault

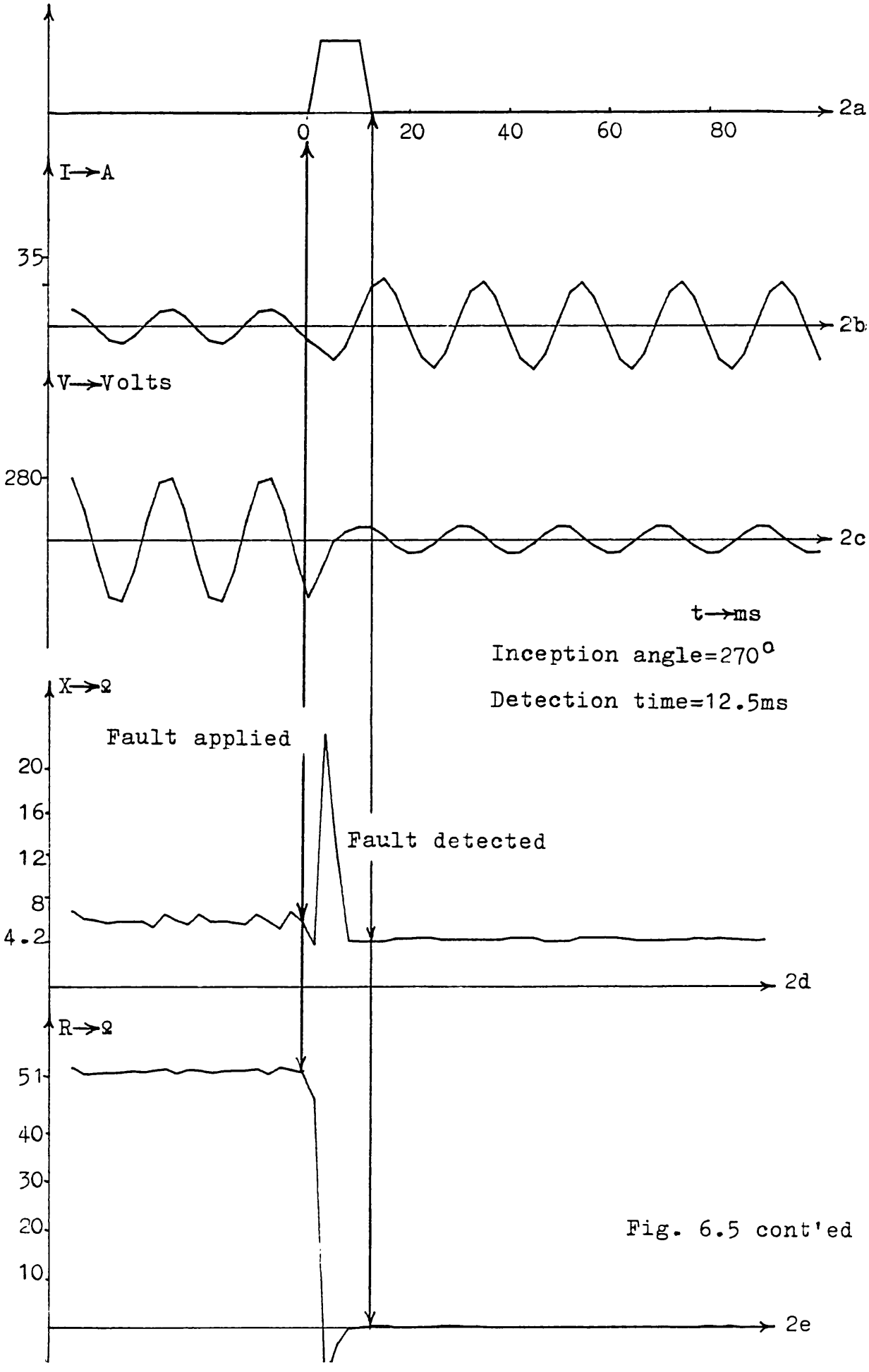


Fig. 6.5 cont'ed

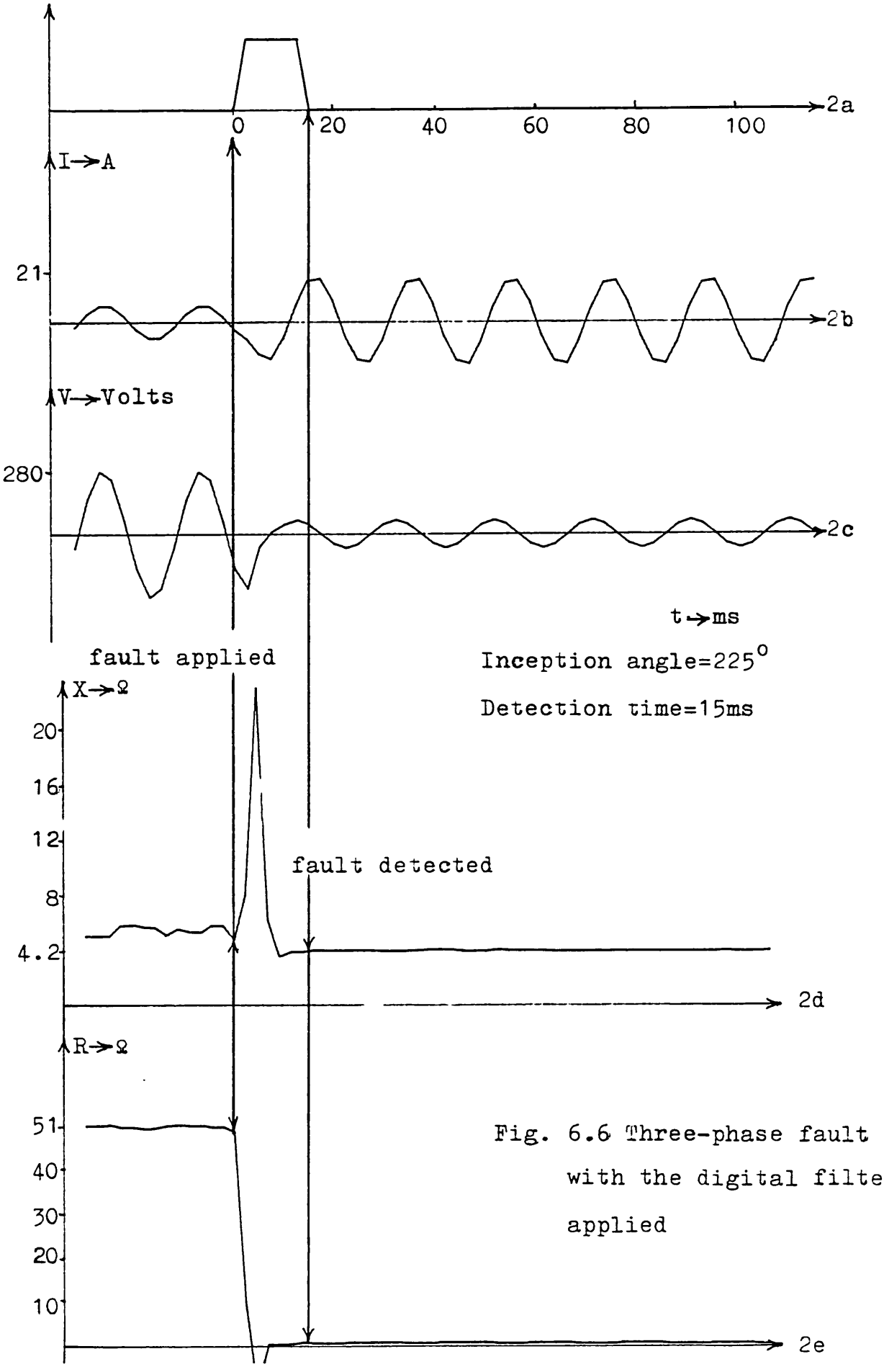
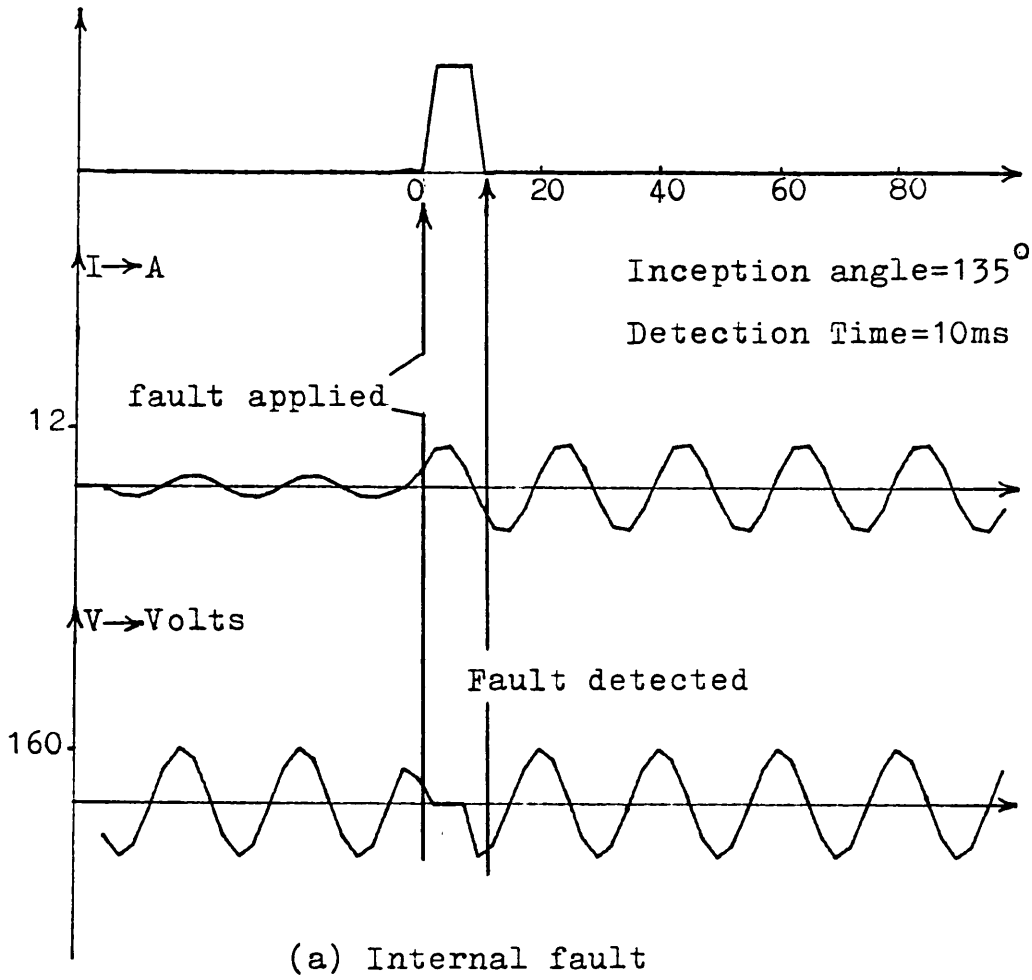
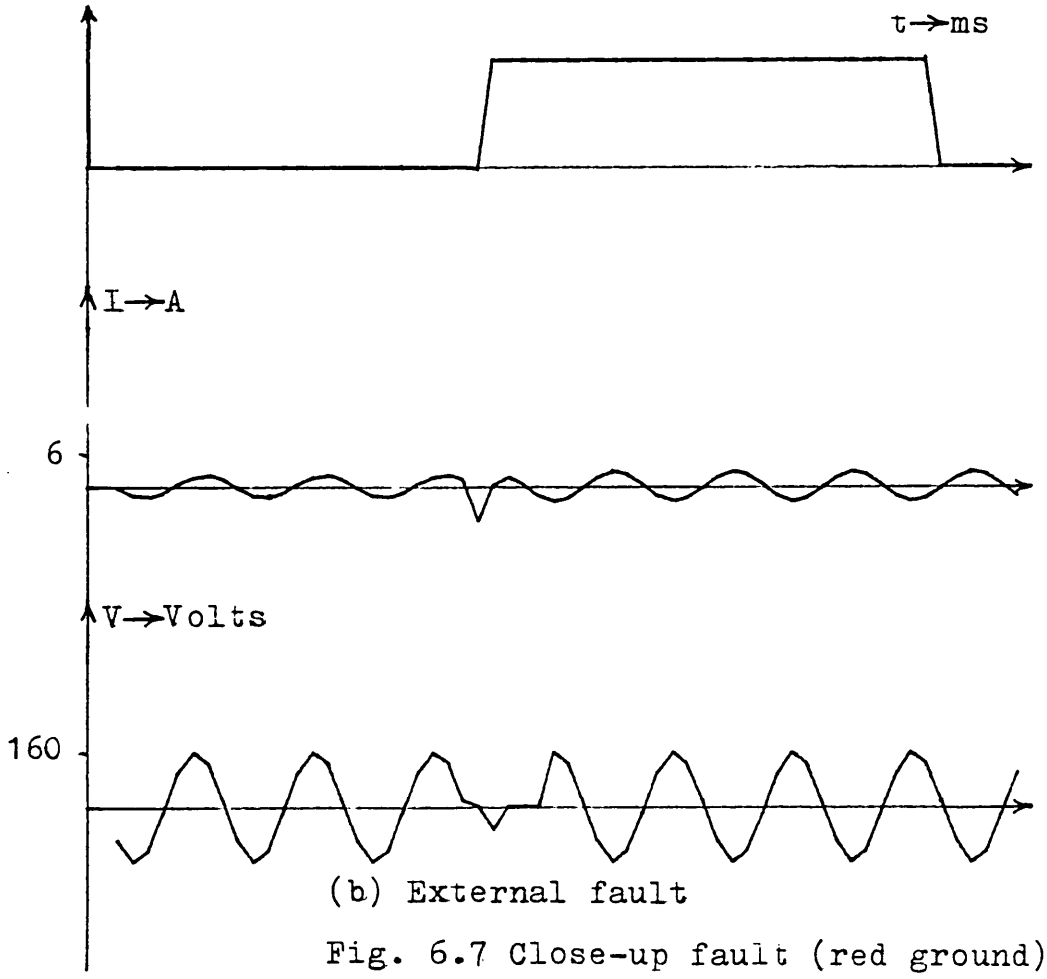


Fig. 6.6 Three-phase fault with the digital filter applied



(a) Internal fault



(b) External fault

Fig. 6.7 Close-up fault (red ground)

6.4. Performance of the relay with varying fault positions

The two algorithms can be compared by plotting the detection time versus fault position. The results shown in figs. 6.8 and 6.9 are average times with 30 measurements taken at each point. If filtering was applied, the detection would have been increased by an average of 2.5ms maximum.

Fig. 6.8 refers to g.f., while fig. 6.9 is concerned with p.f. It can be seen that the sample and midpoint algorithm has slightly faster operating times. The detection times for g.f. and p.f. are almost the same.

There is a slight improvement in the operating time of both algorithms as the fault moves closer to the relaying point.

6.5. Conclusions

The digital relay detects all types of internal fault in less than a cycle. Because of the short data-window, its initial response (the first 3 samples after the fault) contains spikes, but it moves fast enough into the tripping area and it stays within the permissible accuracy of ± 5%.

In addition close-up faults, even at the relaying point are correctly discriminated. The switch-on-fault facility trips the circuit breaker in 7.5ms, in a case

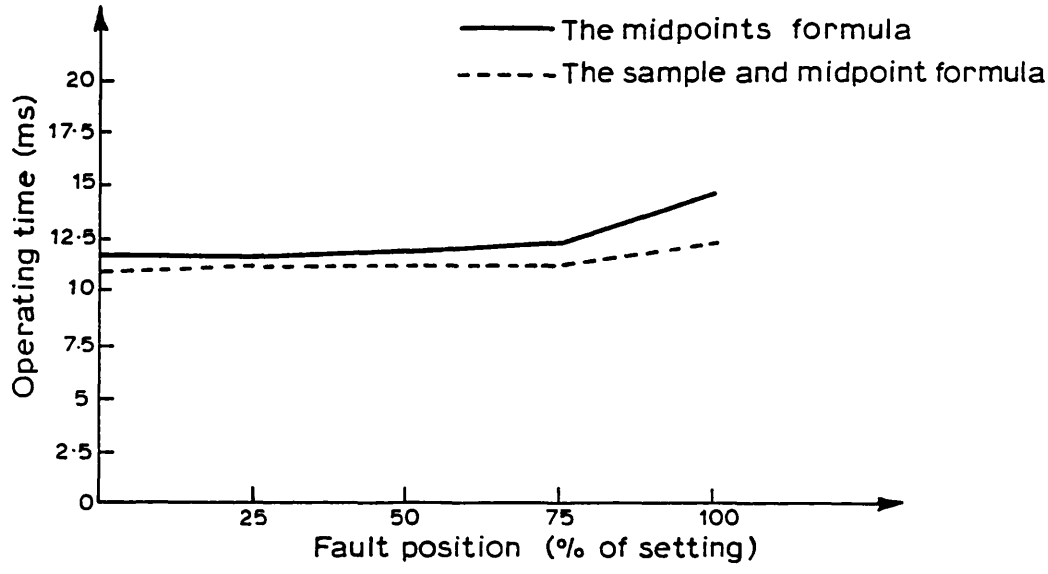


Fig. 6·8 Detection times for phase-ground faults

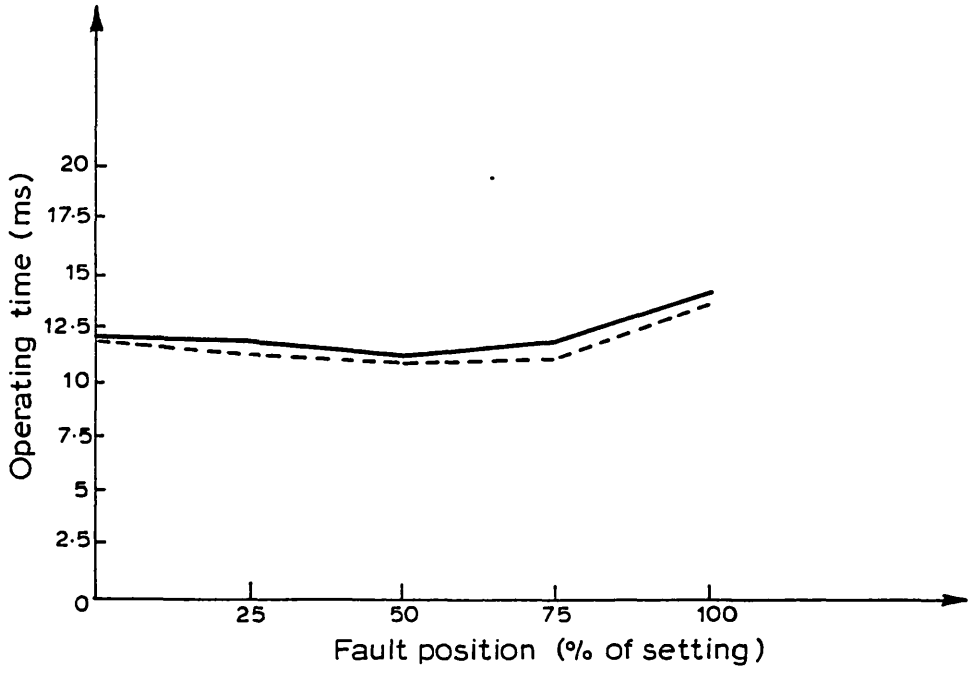


Fig. 6·9 Detection times for phase-phase faults

the earth leads are still present when the relay is switched on.

CHAPTER 7

CONCLUSIONS

7.1 General conclusions

This thesis has described a new approach to distance relaying using digital techniques. The combination of a hardware configuration implemented by a cost-effective microprocessor and of a software structure to cope with the transient conditions occuring after a fault, can produce a distance relay offering many benefits in terms of flexibility.

In chapter 1, a discussion about the advantages and disadvantages of digital protection in general was given and in chapter 2 the problems involved in distance protection were discussed. The development of the described distance relay is based on the digital protection scheme proposed by Cory, Dromey and Murray[19], in which the front-line protection is accomplished by inexpensive, efficient and fast microprocessors (dedicated scheme) communicating with a monitoring minicomputer (integrated scheme) to implement back-up protection.

Such a scheme when examined overall, has the potential of achieving the required high reliability and availability demanded of a protection system, but to achieve it, all the individual parts of the scheme must be carefully selected and designed. Hence the specifications of the desired front-line distance relay were

defined i. e. fast, cost- effective, compatible with the configurations of other protection items included in the scheme, reliable and with simple, efficient and dynamic software.

For these purposes, the dedicated digital distance relay has been divided into two units, namely the data acquisition interface and the protection processor.

The requirements of the interface for a distance relay were presented in chapter 3, where a brief description of the unit was given.

The heart of the digital relay is the processor, therefore its efficient design was important. Based on previous experience in the digital distance protection domain, it has been found that a 16-bit processor with an instruction execution time of about 1 μs was needed. In addition 2K of program store and at least 200 data memory locations were sufficient for programming a distance algorithm. The processor has been designed with great flexibility and to give a fast response. This has been achieved by its microprogrammability, the extensive pipeline configuration used and the restricted size of the program and data memories.

Because the employed microprocessor is micro-programmable it is equally important to pay great attention to the instruction set. The basic instruction set and the extended set introduced to improve the

distance algorithm performance, were also presented in chapter 3.

Finally the development aids required for testing and commissioning the dedicated distance relay as an integral unit were described.

In chapter 4, the existing distance algorithms were discussed. The algorithm finally chosen was of the short data window type, so as to reduce the size of the program and the data memories. The algorithm can cope with the d.c. exponential component present in a fault waveform on a long transmission line. A combination of analogue and digital filtering was provided for the high- frequency harmonics. To evaluate the performance of the algorithm, the same program has been run off-line on a main - frame computer. The recorded results were similar to those obtained by the microprocessor.

Software organisation for the application program is critical for a real-time application and that used here was presented in chapter 5. It was shown that by executing all six impedance calculations at every sampling interval, a switched distance scheme has been avoided with its attendant difficulties of starting a phase selection. The polar characteristic adopted is the quadrilateral one. For close-up faults, discrimination has been achieved by using the prefault voltages to calculate the sign of the impedance.

Care has been taken in providing information to the monitoring computer, such that the relay performance can be recorded as shown in chapter 6. The relay has responded with a great selectivity to all kinds of faults applied in the test rig. It took 7.5ms to enter the trip zone for the first time, but the trip decision taken when 3 consecutive calculations are inside the zone, to ensure discrimination. The tests have shown that the relay operates within 15 ms, with an a accuracy of ± 5% of its reach for all types of faults.

7.2 Original contributions

The original contributions presented in this thesis are:

a) A digital feeder protection scheme which combines flexibility, fast response and of a cost comparable with that of analogue relays.

b) Modifications in the hardware and software design of a special purpose microprogrammed microprocessor to match and improve the requirements of a distance protection specification.

c) The modification of an existing algorithm, which gives a faster response as it moves quicker into the post fault data.

d) The development of a dedicated digital distance relay having operation times of about 15ms. The relay is of the non- switched three-zone stepped type.

e) The provision of all features expected by existing distance schemes, e. g. close-up directional discrimination, switch-on-fault, out-of-step blocking and autoreclosing facilities.

f) Additional features, not available in present relays which improve availability and the operation of the protection scheme in general have been included e. g. a full fault report, a self-test monitoring and measurement of active and reactive power at the relaying point.

7.3 Further research

Since a digital system has almost unlimited possible configurations, the final choice depends on its application to a specific transmission line. By keeping to a modular software organisation such a procedure is possible.

Other types of algorithm can be used in place of the present one to calculate the fault position. Methods such as curve fitting[63,64] and travelling waves[65,66] look promising in terms of faster response. However, with more complex software involved in conjunction with a possible higher sampling rate, will make it more difficult to run the distance algorithm in real time. Time can be saved by having starting elements of the overcurrent type or by executing only the three phase-phase fault impedance calculations at every sample, until

the residual current is above a threshold limit, when the three ground-fault impedances can be calculated. Such a scheme provides saving in processing time while its performance in terms of selecting the faulty phase is between that of a switched and non-switched configuration. Therefore it can be employed only if the application program is time consuming.

Time can be saved by abandoning the calculations for the additional features provided, but that reduces the versatility of the distance relay.

One of the main advantages of digital protection is its capability to adjust the characteristic according to load conditions. Such a feature has not be included in the present design. It is even possible to have different types of characteristics for ground and phase faults, such that the problems introduced by the arc resistance can be taken into account.

In addition, special compensation or calculations needed for the installation of distance relays in parallel or teed lines could be included in the digital distance relay.

Such a relay, to be competitive with existing analogue ones, needs extensive testing under different operating conditions, especially for different ratios of Z_S/Z_L, power swings and fault types.

Testing techniques which use a digital computer to generate fault conditions will ease the testing task[79].

Further research can also be oriented to the subject of generating a special purpose protection language, such that testing and operating of the relay can become considerably easier.

The development of a more advanced system for testing a new software program is essential for a fast development time.

Replacement of the processor by a more modern fast microprocessor might reduce the number of devices used, hence the cost of the unit, but it is unlikely to produce any improvement in performance. On the other hand, a new design would be necessary and some flexibility may be lost, if a non- microprogrammable, bipolar- - microprocessor is used.

A careful watch on new microprocessor developments is required to maintain digital protection practices at their best within the design principles laid down in this thesis.

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APPENDIX 1

THE DATA ACQUISITION UNIT

This appendix gives the detailed circuit diagrams for the data acquisition unit.

Further information about the ICs are given by the data sheets of the manufacturers. For the 74 series TTL chips, the TTL data book for design engineers by Texas Instruments can be referred to.[78]

Resistors nomenclature

100 value in ohms

4.7K value in kohms

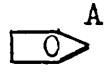
3.9M value in Mohms

Capacitors nomenclature

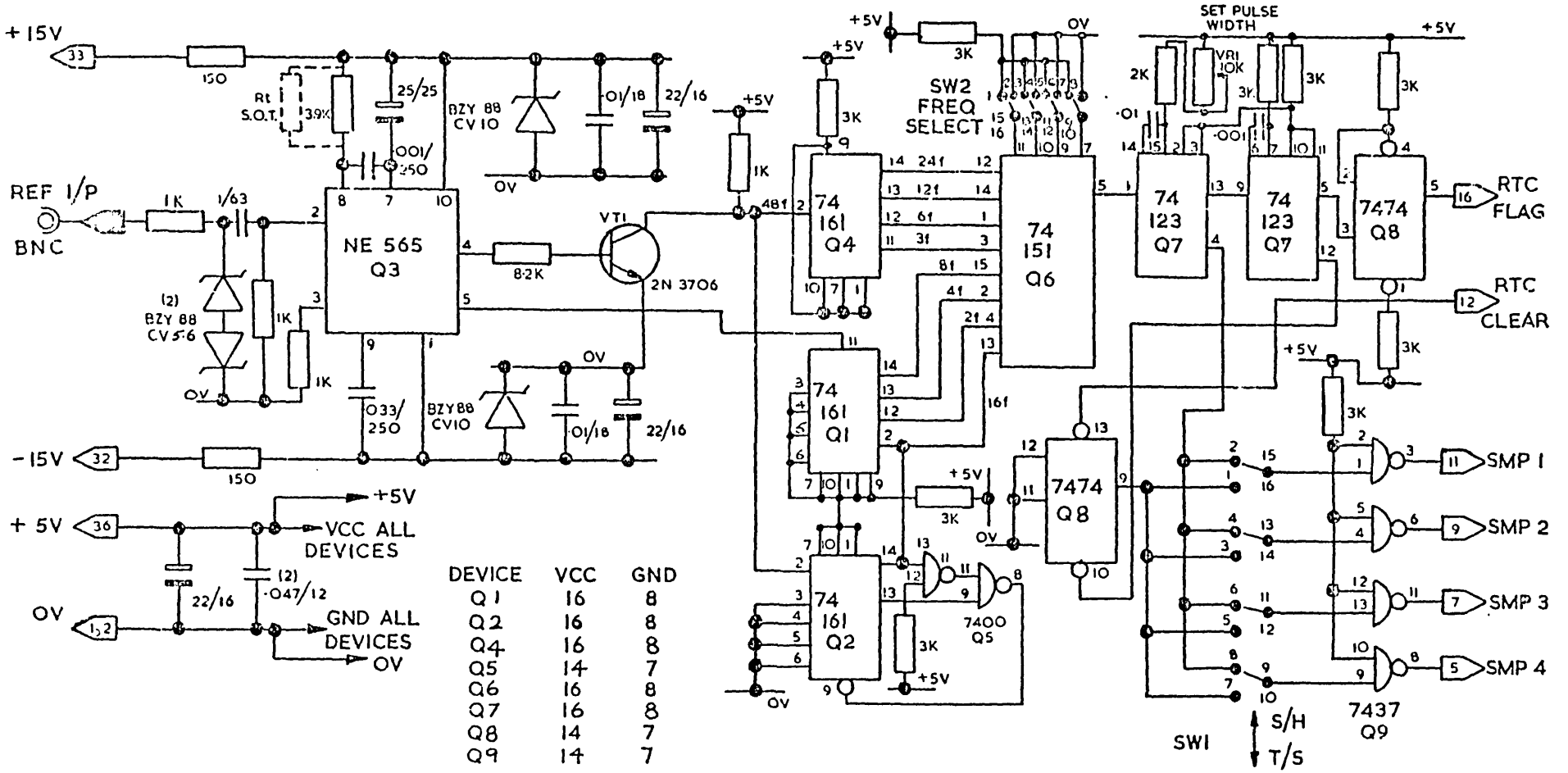
The form A/D stands for value in microfarads/working voltage (volts).

Symbols nomenclature

indicates a printed circuit edge connector

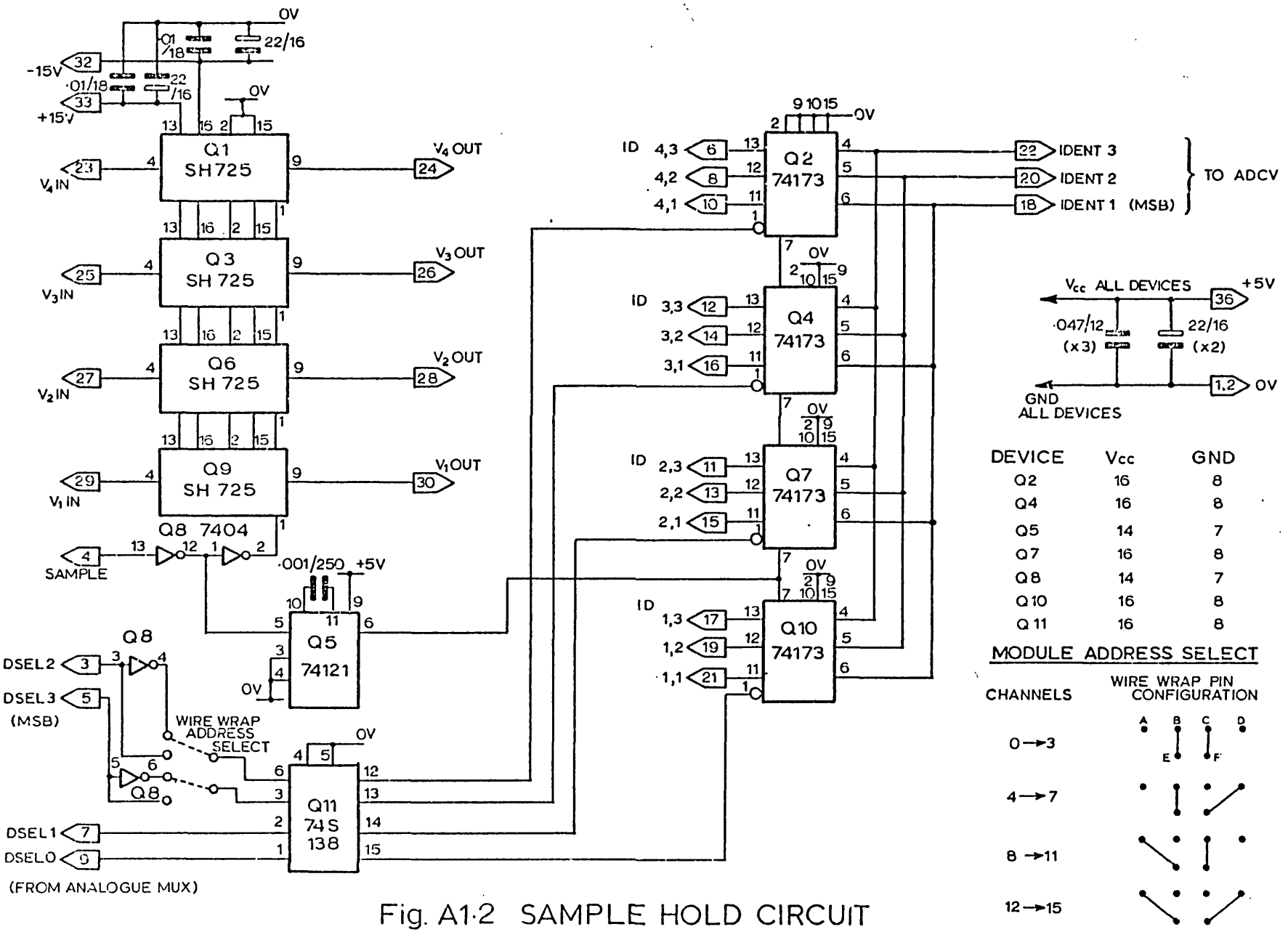


indicates a wire link from the printed circuit board.



DEVICE	VCC	GND
Q1	16	8
Q2	16	8
Q4	16	8
Q5	14	7
Q6	16	8
Q7	16	8
Q8	14	7
Q9	14	7

FIG A1.1 PHASE LOCKED SAMPLING CLOCK CIRCUIT

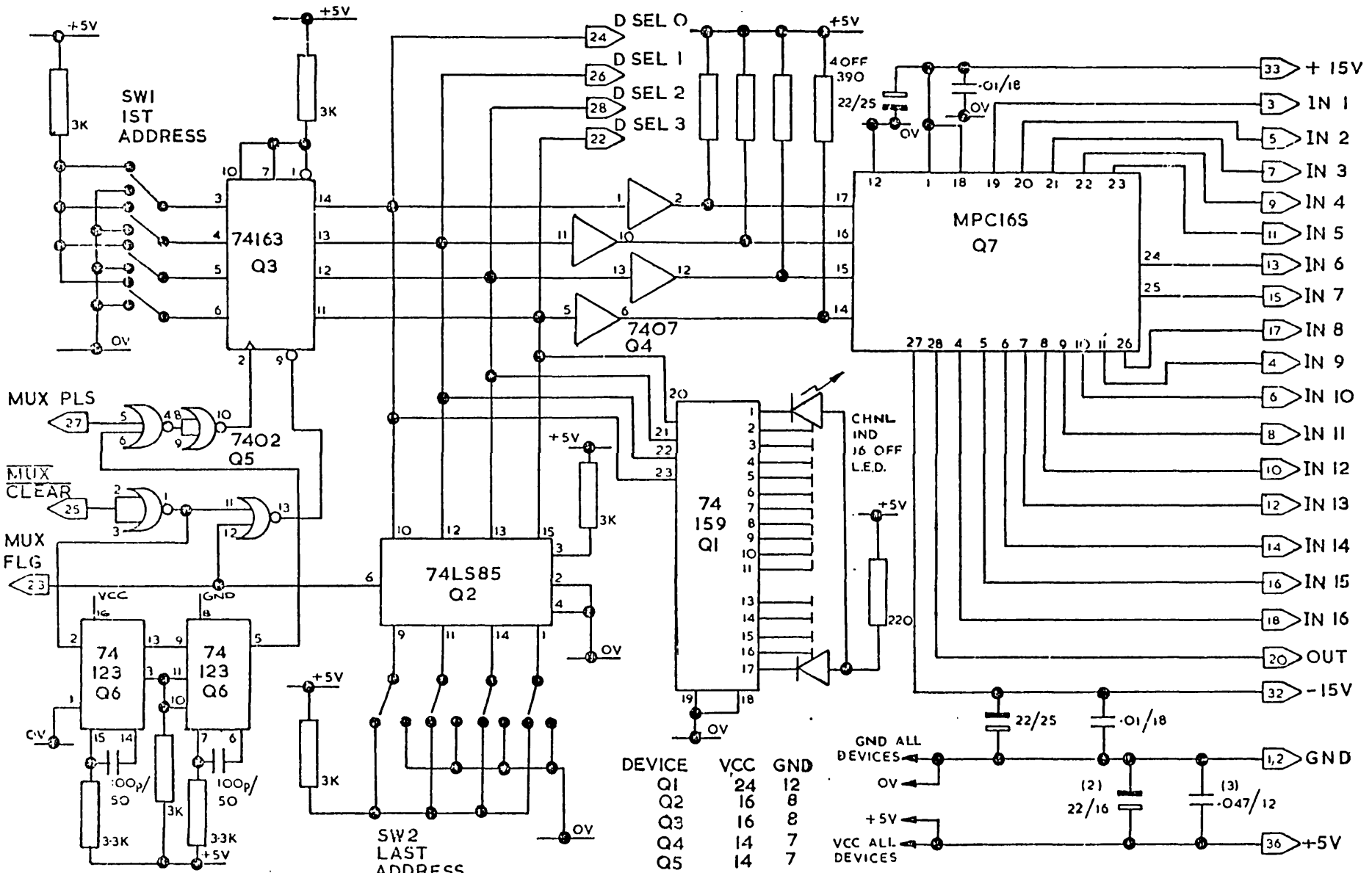


DEVICE	Vcc	GND
Q2	16	8
Q4	16	8
Q5	14	7
Q7	16	8
Q8	14	7
Q10	16	8
Q11	16	8

MODULE ADDRESS SELECT

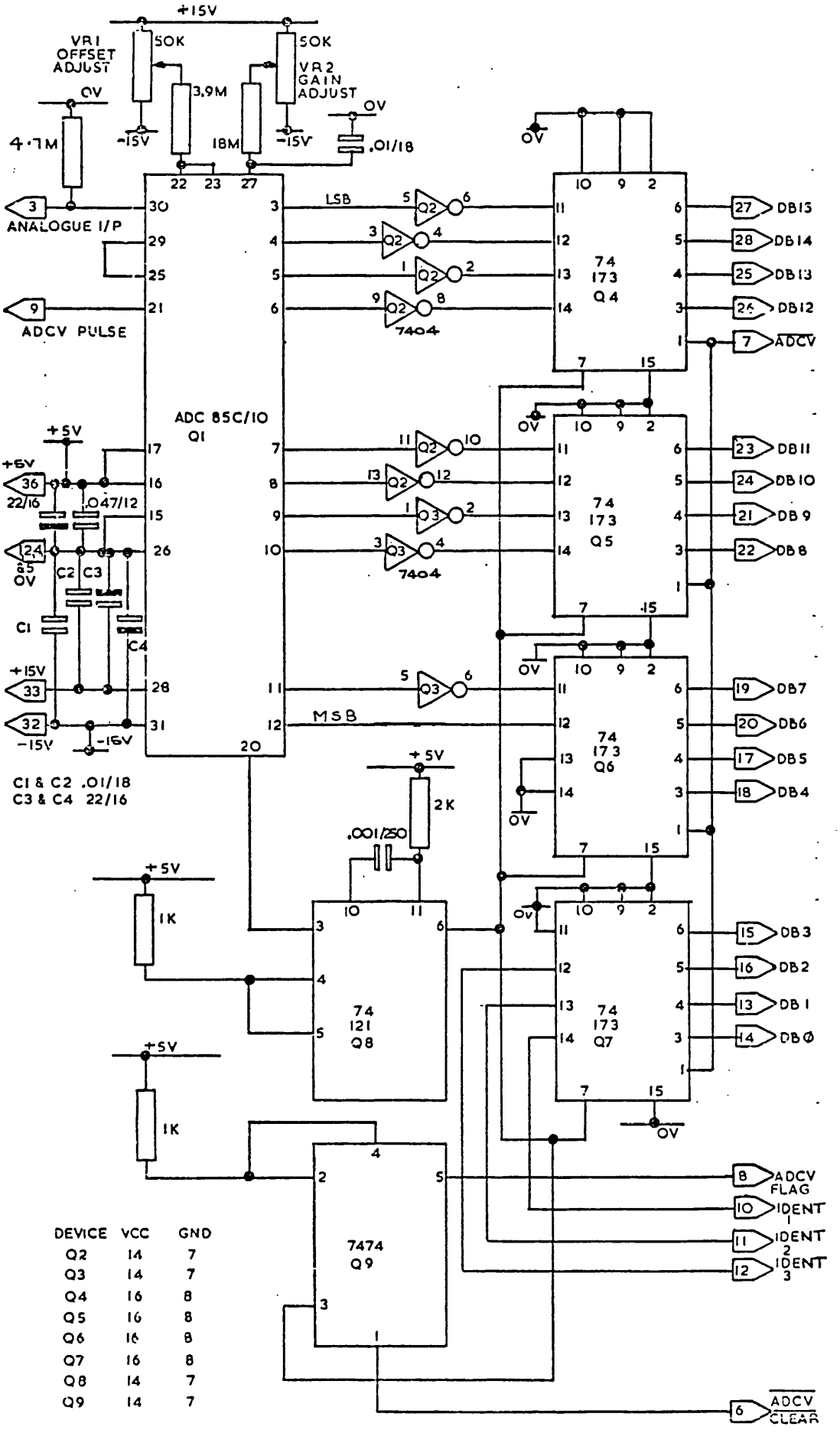
CHANNELS	WIRE WRAP PIN CONFIGURATION
0 → 3	
4 → 7	
8 → 11	
12 → 15	

Fig. A1·2 SAMPLE HOLD CIRCUIT



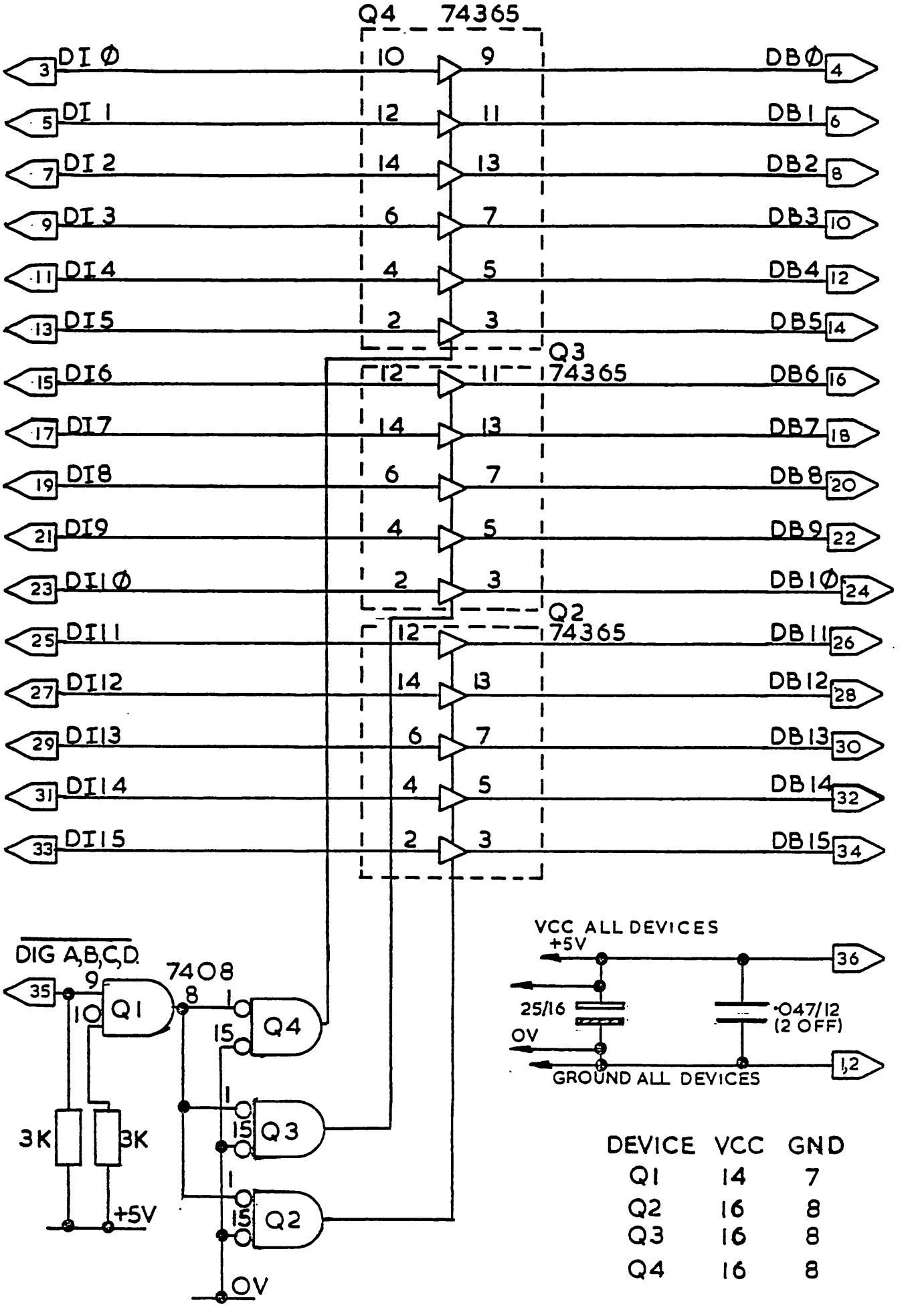
DEVICE	VCC	GND
Q1	24	12
Q2	16	8
Q3	16	8
Q4	14	7
Q5	14	7

FIG A1,3 ANALOGUE MULTIPLEXER CIRCUIT



DEVICE	VCC	GND
Q2	14	7
Q3	14	7
Q4	16	8
Q5	16	8
Q6	16	8
Q7	16	8
Q8	14	7
Q9	14	7

FIG. A1.4 ANALOGUE DIGITAL CONVERTER CIRCUIT.



DEVICE	VCC	GND
Q1	14	7
Q2	16	8
Q3	16	8
Q4	16	8

FIG.A1,5 DIGITAL INPUT BUS DRIVERS CIRCUIT

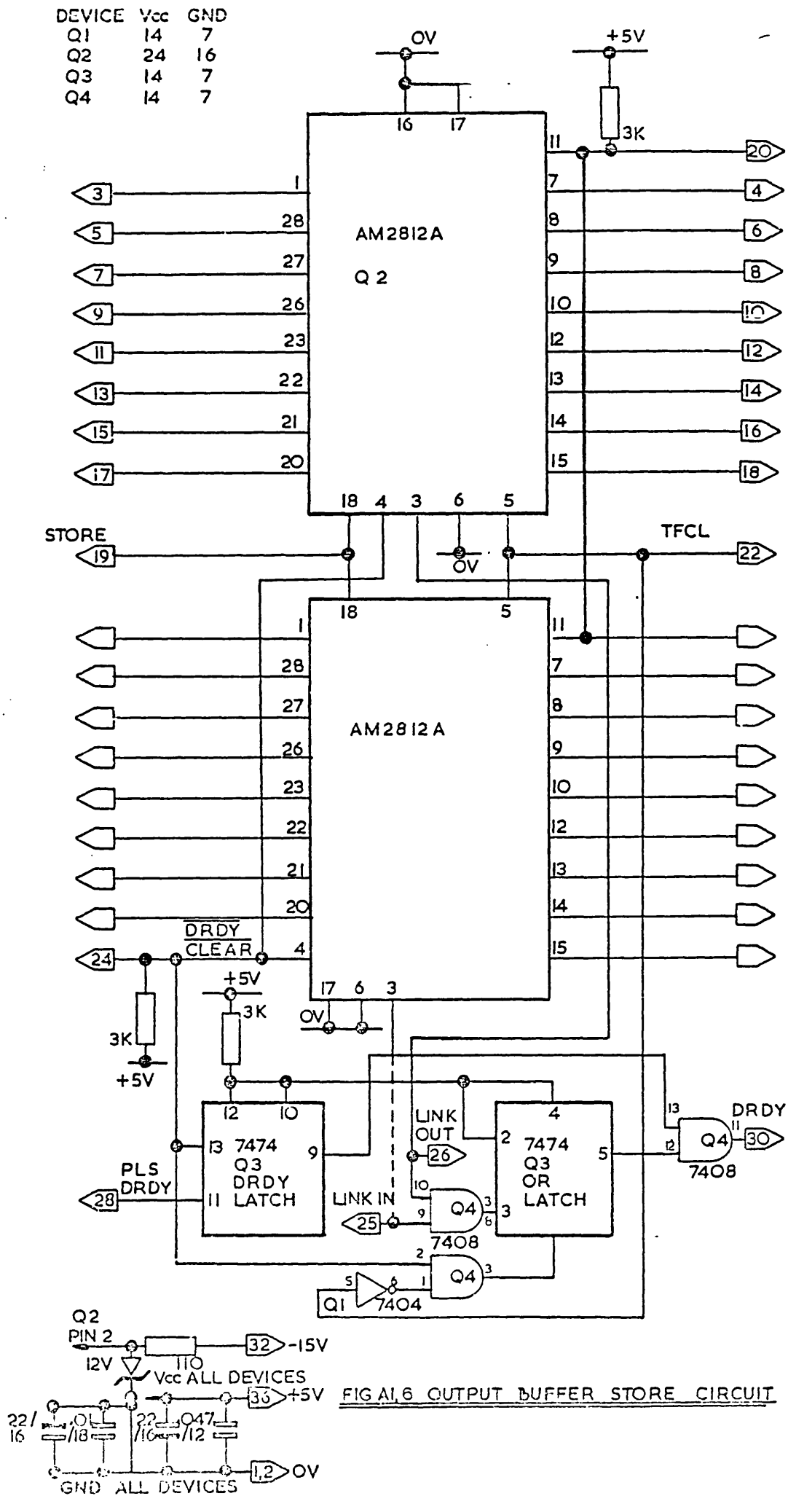


FIG A1.6 OUTPUT BUFFER STORE CIRCUIT

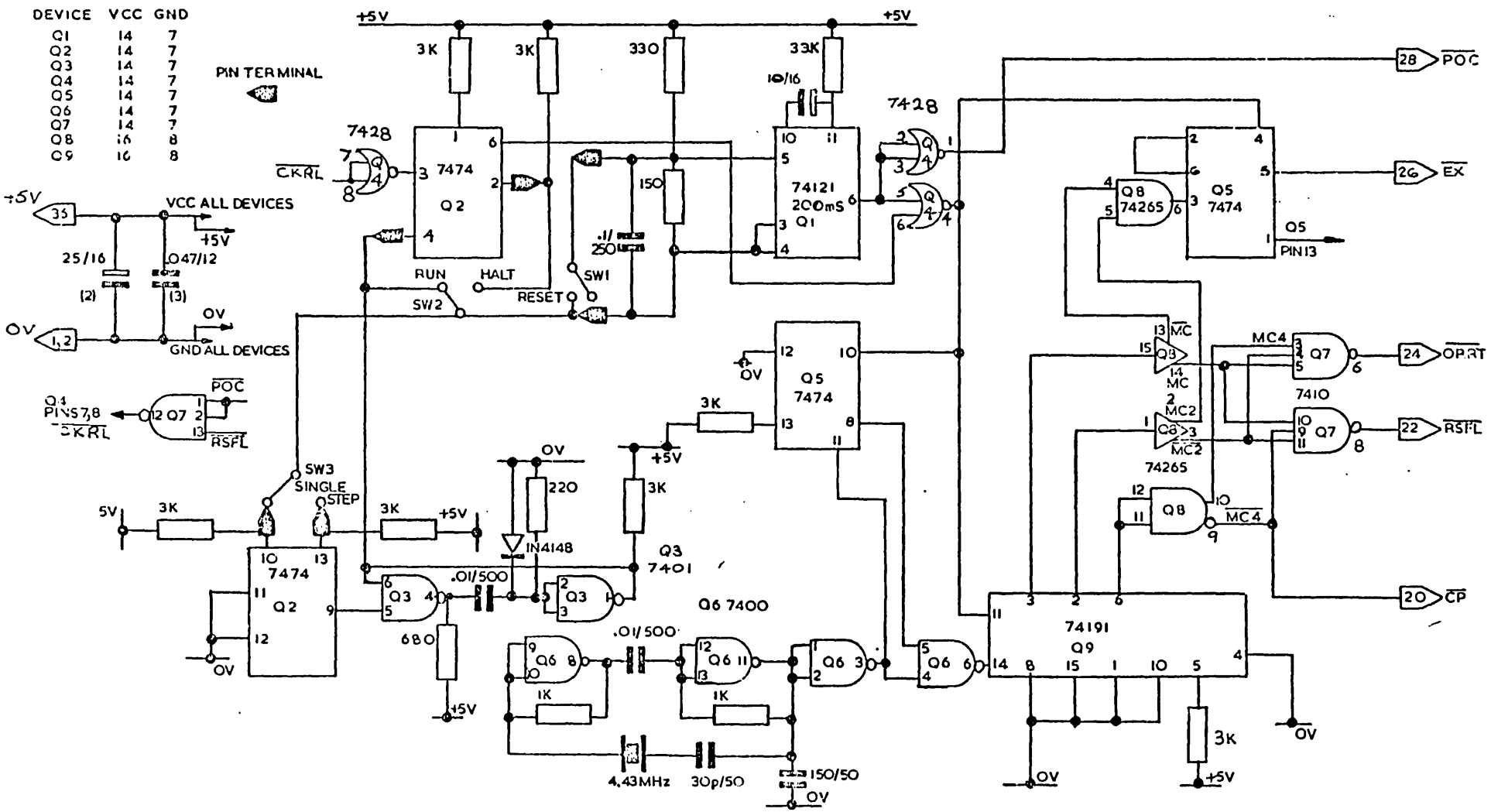
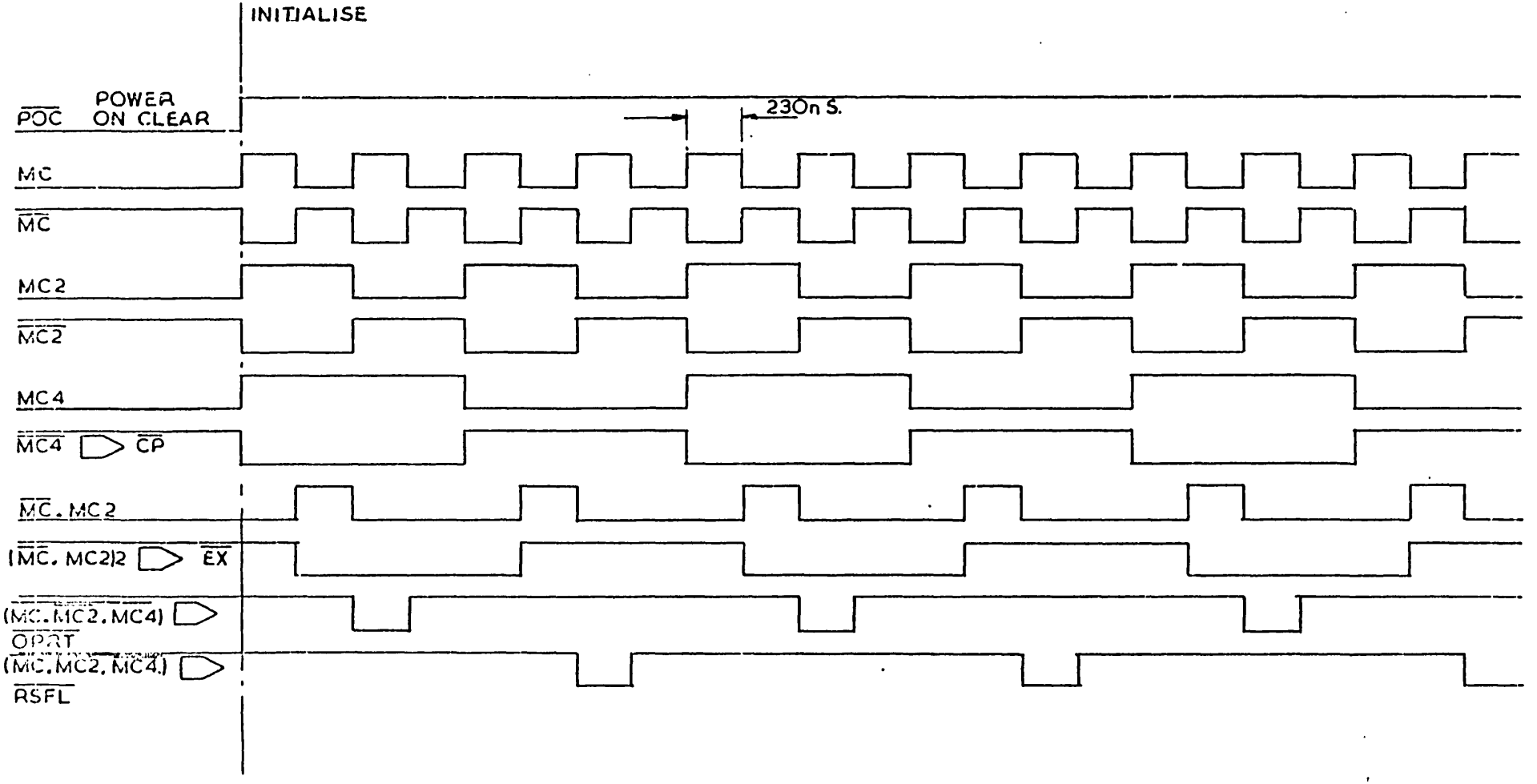


FIG A1.7 ACQUISITION SYSTEM CLOCK GENERATOR CIRCUIT



FIGAI.8 ACQUISITION SYSTEM TIMING

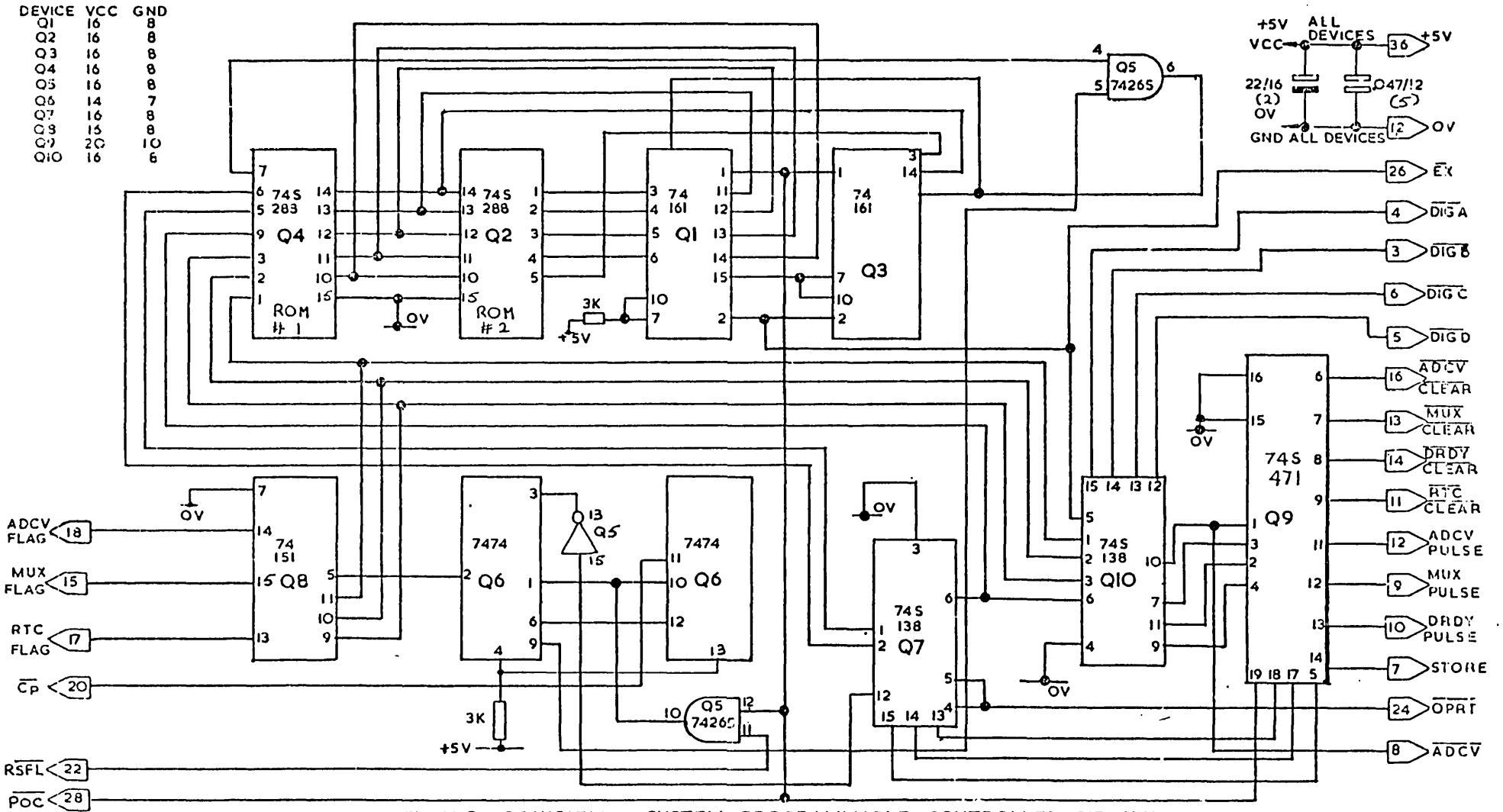


FIG A1.9 ACQUISITION SYSTEM PROGRAMMABLE CONTROLLER CIRCUIT

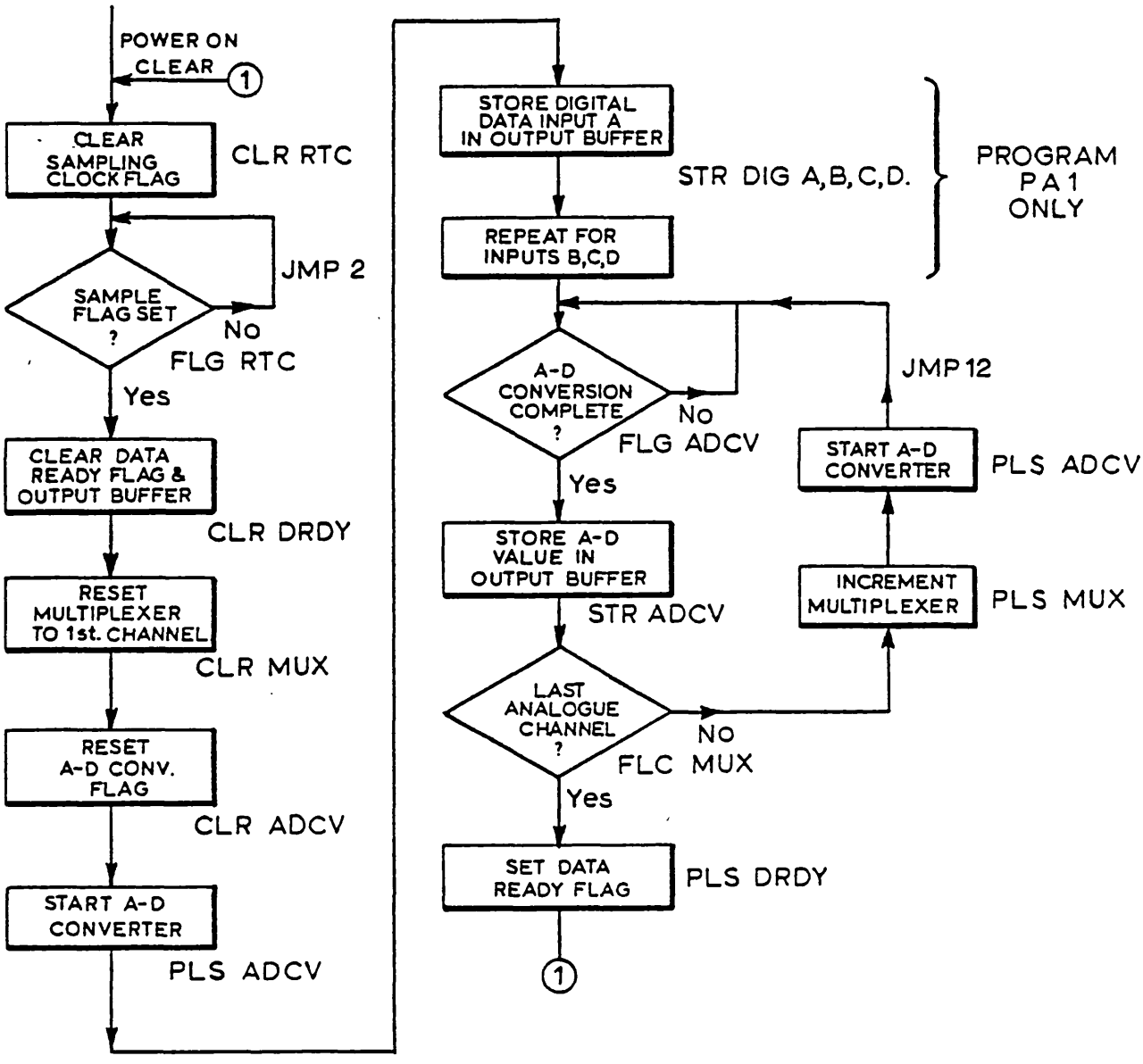


Fig. A1.10 Program flow chart for data acquisition interface controller.

ADDRESS						DATA															INSTRUCTION
DECIMAL	BINARY					ROM# 1								ROM # 2							
	A4	A3	A2	A1	A0	O8	O7	O6	O5	O4	O3	O2	O1	O8	O7	O6	O5	O4	O3	O2	O1	
0	0	0	0	0	0	0	0	0	0	X	0	0	0	X	X	X	0	0	0	0	1	JMP 1
1	0	0	0	0	1	1	1	0	0	X	1	1	0	X	X	X	0	0	0	0	0	CLR RTC
2	0	0	0	1	0	1	1	1	1	X	1	1	0	X	X	X	0	0	1	0	0	FLG RTC
3	0	0	0	1	1	0	0	0	0	X	0	0	0	X	X	X	0	0	0	1	0	JMP 2
4	0	0	1	0	0	1	1	0	0	X	1	1	1	X	X	X	0	0	0	0	0	CLR DRDY
5	0	0	1	0	1	1	1	0	0	X	1	0	0	X	X	X	0	0	0	0	0	CLR MUX
6	0	0	1	1	0	1	1	0	0	X	1	0	1	X	X	X	0	0	0	0	0	CLR ADCV
7	0	0	1	1	1	1	1	0	1	X	1	0	1	X	X	X	0	0	0	0	0	PLS ADCV
8	0	1	0	0	0	1	1	1	0	X	0	0	0	X	X	X	0	0	0	0	0	STR DIG A
9	0	1	0	0	1	1	1	1	0	X	0	0	1	X	X	X	0	0	0	0	0	STR DIG B
10	0	1	0	1	0	1	1	1	0	X	0	1	0	X	X	X	0	0	0	0	0	STR DIG C
11	0	1	0	1	1	1	1	1	0	X	0	1	1	X	X	X	0	0	0	0	0	STR DIG D
12	0	1	1	0	0	1	1	1	1	X	1	0	1	X	X	X	0	1	1	1	0	FLG ADCV
13	0	1	1	0	1	0	0	0	0	X	0	0	0	X	X	X	0	1	1	0	0	JMP 12
14	0	1	1	1	0	1	1	1	0	X	1	0	1	X	X	X	0	0	0	0	0	STR ADCV
15	0	1	1	1	1	1	1	1	1	X	1	0	0	X	X	X	1	0	1	0	0	FLG MUX
16	1	0	0	0	0	1	1	0	1	X	1	0	0	X	X	X	0	0	0	0	0	PLS MUX
17	1	0	0	0	1	1	1	0	0	X	1	0	1	X	X	X	0	0	0	0	0	CLR ADCV
18	1	0	0	1	0	1	1	0	1	X	1	0	1	X	X	X	0	0	0	0	0	PLS ADCV
19	1	0	0	1	1	0	0	0	0	X	0	0	0	X	X	X	0	1	1	0	0	JMP 12
20	1	0	1	0	0	1	1	0	1	X	1	1	1	X	X	X	0	0	0	0	0	PLS DRDY
21	1	0	1	0	1	0	0	0	0	X	0	0	0	X	X	X	0	0	0	0	1	JMP 1

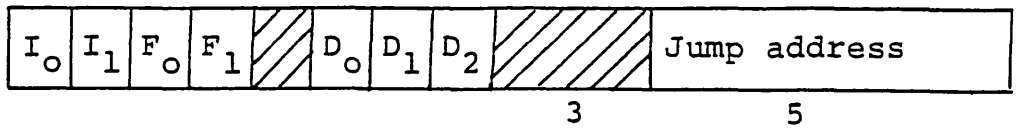
FIG. AI.11 ACQUISITION SYSTEM PROGRAM PAI. ROM. MAP

ADDRESS						DATA															INSTRUCTION
DECIMAL	BINARY					ROM #1								ROM #2							
	A4	A3	A2	A1	A0	O8	O7	O6	O5	O4	O3	O2	O1	O8	O7	O6	O5	O4	O3	O2	O1	
0	0	0	0	0	0	0	0	0	0	X	0	0	0	X	X	X	0	0	0	0	1	JMP 1
1	0	0	0	0	1	1	1	0	0	X	1	1	0	X	X	X	0	0	0	0	0	CLR RTC
2	0	0	0	1	0	1	1	1	1	X	1	1	0	X	X	X	0	0	1	0	0	FLG RTC
3	0	0	0	1	1	0	0	0	0	X	0	0	0	X	X	X	0	0	0	1	0	JMP 2
4	0	0	1	0	0	1	1	0	0	X	1	1	1	X	X	X	0	0	0	0	0	CLR DRDY
5	0	0	1	0	1	1	1	0	0	X	1	0	0	X	X	X	0	0	0	0	0	CLR MUX
6	0	0	1	1	0	1	1	0	0	X	1	0	1	X	X	X	0	0	0	0	0	CLR ADCV
7	0	0	1	1	1	1	1	0	1	X	1	0	1	X	X	X	0	0	0	0	0	PLS ADCV
8	0	1	0	0	0	1	1	1	1	X	1	0	1	X	X	X	0	1	0	1	0	FLG ADCV
9	0	1	0	0	1	0	0	0	0	X	0	0	0	X	X	X	0	1	0	0	0	JMP 8
10	0	1	0	1	0	1	1	1	0	X	1	0	1	X	X	X	0	0	0	0	0	STR ADCV
11	0	1	0	1	1	1	1	1	1	X	1	0	0	X	X	X	0	1	1	1	0	FLG MUX
12	0	1	1	0	0	1	1	0	1	X	1	0	0	X	X	X	0	0	0	0	0	PLS MUX
13	0	1	1	0	1	0	0	0	0	X	0	0	0	X	X	X	0	0	1	1	0	JMP 6
14	0	1	1	1	0	1	1	0	1	X	1	1	1	X	X	X	0	0	0	0	0	PLS DRDY
15	0	1	1	1	1	0	0	0	0	X	0	0	0	X	X	X	0	0	0	0	1	JMP 1

FIG A1.12 ACQUISITION SYSTEM PROGRAM XA1
ROM MAP

ADDRESS (INPUTS)								DATA (CONTROL OUTPUTS)								FUNCTION
H	G	F	E	D	C	B	A	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Power on clear Gives $\overline{\text{ADCV CLR}}$
						REPEATED TO										
0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	$\overline{\text{MUX CLR}}$ $\overline{\text{RTC CLR}}$ $\overline{\text{DRDY CLR}}$
1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	Invalid inputs. Outputs inactive.
						REPEATED TO										
1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	
1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	STORE with ADCV selected
1	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	STORE digital inputs.
1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	Invalid inputs Outputs inactive.
						REPEATED TO										
1	1	0	1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	1	1	0	1	0	0	1	1	1	1	DRDY PULSE
1	1	0	1	1	1	0	0	0	0	0	0	1	1	1	1	Invalid input
1	1	0	1	1	1	0	1	0	0	1	0	1	1	1	1	MUX PULSE
1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	1	ADCV PULSE
1	1	0	1	1	1	1	1	0	0	0	0	1	1	1	1	Invalid inputs Outputs inactive.
						REPEATED TO										
1	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1	
1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	1	$\overline{\text{RTC CLR}}$
1	1	1	0	1	0	0	0	0	0	0	0	1	1	1	1	Invalid inputs Outputs inactive
1	1	1	0	1	0	0	1	0	0	0	0	1	1	1	1	
1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	1	0	1	0	1	1	0	0	0	0	1	0	1	1	$\overline{\text{DRDY CLR}}$
1	1	1	0	1	1	0	0	0	0	0	0	1	1	1	1	Invalid input
1	1	1	0	1	1	0	1	0	0	0	0	1	1	0	1	$\overline{\text{MUX CLR}}$
1	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	$\overline{\text{ADCV CLR}}$
1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	Invalid inputs.
						REPEATED TO										Outputs inactive.
1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	

TABLE A1.1 Programmable controller output decoding ROM (Q9) contents map.



Device address group;

Device	Mnemonic	D_o	D_1	D_2
Digital input port 1	DIG A	0	0	0
" " " 2	DIG B	0	0	1
" " " 3	DIG C	0	1	0
" " " 4	DIG D	0	1	1
Analogue Multiplexer	MUX	1	0	0
Analogue-Digital conv	ADCV	1	0	1
Phase locked clock	RTC	1	1	0
Data ready flag	DRDY	1	1	1

Function group:

Function	Mnemonic	I_o	I_1	F_o	F_1
Program jump	JMP	0	0	0	0
Clear device or flag	CLR	1	1	0	0
Clock device	PLS	1	1	0	1
Transfer data	STR	1	1	1	0
Test device status	FLG	1	1	1	1

TABLE A1.2 Interface controller instruction formats.

Interface programming examples.

The following programs demonstrate the application of the interface instruction set in two cases:

i) acquisition of digital and analogue data,

ii) analogue data only

The flow chart, Fig. A1.10 is applicable to both programs, and the corresponding controller program R.O.M. maps are illustrated in Fig.A1.11 , A1.12 .

Control program identification

The pairs of P.R.O.M's which contain the controller programs are identified by four character codes:

X	X	X	1(2)
Digital data	Analogue data	Number of samples per block	R.O.M number

i) Digital data

The first character of the code indicates the digital input channels used, if any, and is an alphabetic sequence from A to P

e.g. A - input A only

K - inputs ABC

P - inputs ABCD

The letter X indicates that the digital inputs are unused.

ii) Analogue data

The second character is the letter A if analogue channels are included in the data block, otherwise the letter X is used. The channel numbers in use will depend on the multiplexer switch settings and thus can not be indicated in the program code.

iii) Number of samples per block

This figure is an indication of the number of samples stored in the output buffer prior to the setting of the data ready flag. In most applications it is unlikely to exceed 1.

iv) R.O.M. number

The final digit i.e. -1 or -2 corresponds to the numbered program memory sockets on the controller module. ROM - 1 contains the function and device address groups of the instructions, whilst ROM -2 holds jump address information.

INPUT SOCKETS (McMURDO RED-RANGE 16 WAY).

PIN NO	DIGITAL INPUTS	ANALOGUE INPUTS
1	DATA IN 15 MSB	ANALOGUE IN 1
2	" 14	IDENT DATA 2 (MSB)
3	" 13	" 1
4	12	" 0 (LSB)
5	11	ANALOGUE IN 2
6	10	IDENT DATA 2
7	9	" 1
8	8	" 0
9	7	ANALOGUE IN 3
10	6	IDENT DATA 2
11	5	" 1
12	4	" 0
13	3	ANALOGUE IN 4
14	2	IDENT DATA 2
15	1	" 1
16	0 (LSB)	" 0

TABLE A1.3 Acquisition interface input plug details.

OUTPUT SOCKET (McMURDO RED-RANGE 24 WAY).

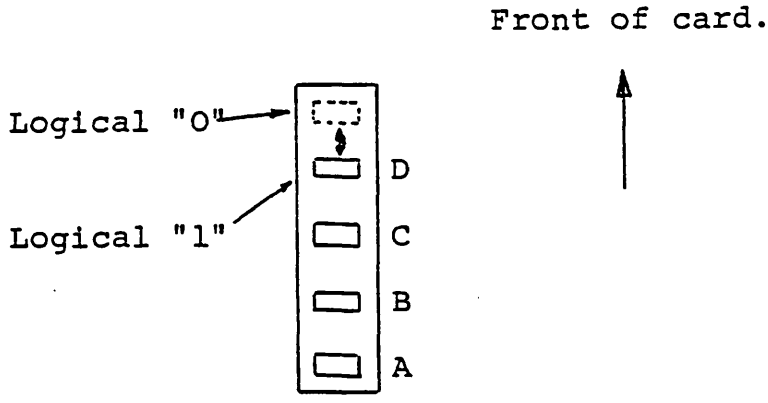
PIN NO	FUNCTION	PIN NO	FUNCTION
1	DATA OUT 0(LSB)	13	DATA OUT 12
2	" 1	14	" 13
3	" 2	15	" 14
4	" 3	16	" 15(MSB)
5	" 4	17	NC
6	" 5	18	DATA READY FLAG
7	" 6	19	NC
8	" 7	20	DATA TRANSFER CLOCK
9	" 8	21	NC
10	" 9	22	OUTPUT ENABLE
11	" 10	23	NC
12	" 11	24	POWER-ON CLEAR (O/P)

NC = NOT CONNECTED.

POWER PLUG (McMURDO RED-RANGE 8 WAY).

PIN NO	FUNCTION
1 & 5	- 15V
2 & 6	+ 15V
3 & 7	+ 5V
4 & 8	OV (GND)

TABLE A1.4 Acquisition interface output socket and power plug details.



First (SW1)/Last (SW2) channel address switches.

First/Last channel.	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TABLE A1.5 Analogue multiplexer channel control switches.

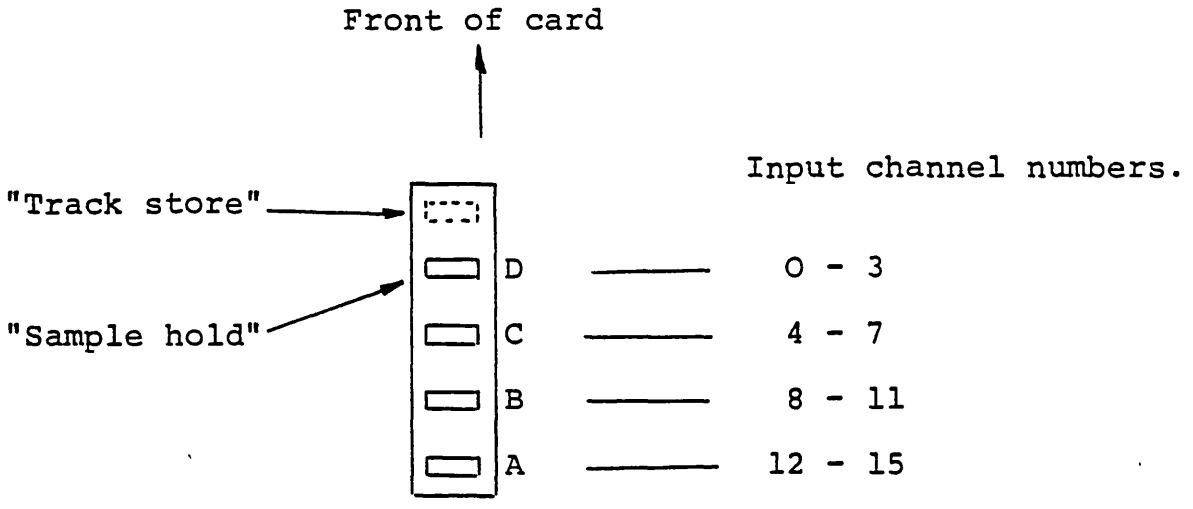
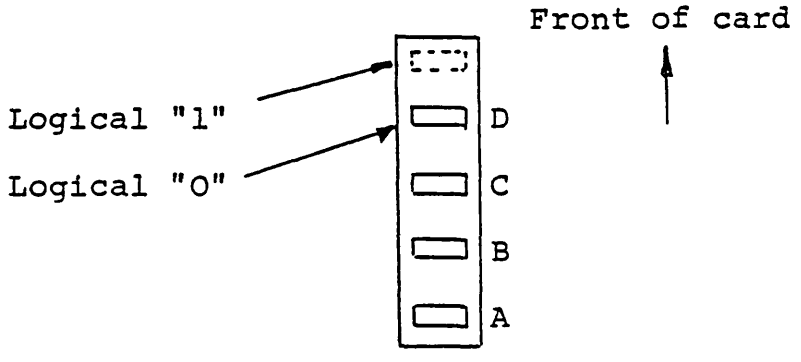


TABLE A1.6 Phase locked sampling clock, mode select switches (SW1).



Sampling rate (s.c)	D	C	B	A
Clock off	X	X	X	1
2	0	0	0	0
3	1	0	0	0
4	0	1	0	0
6	1	1	0	0
8	0	0	1	0
12	1	0	1	0
16	0	1	1	0
24	1	1	1	0

TABLE A1.7 Phase locked sampling clock, clock rate select switches (SW2).

APPENDIX 2

THE PROTECTION PROCESSOR

The circuit diagrams for the protection processor are given. For comments see Appendix 1.

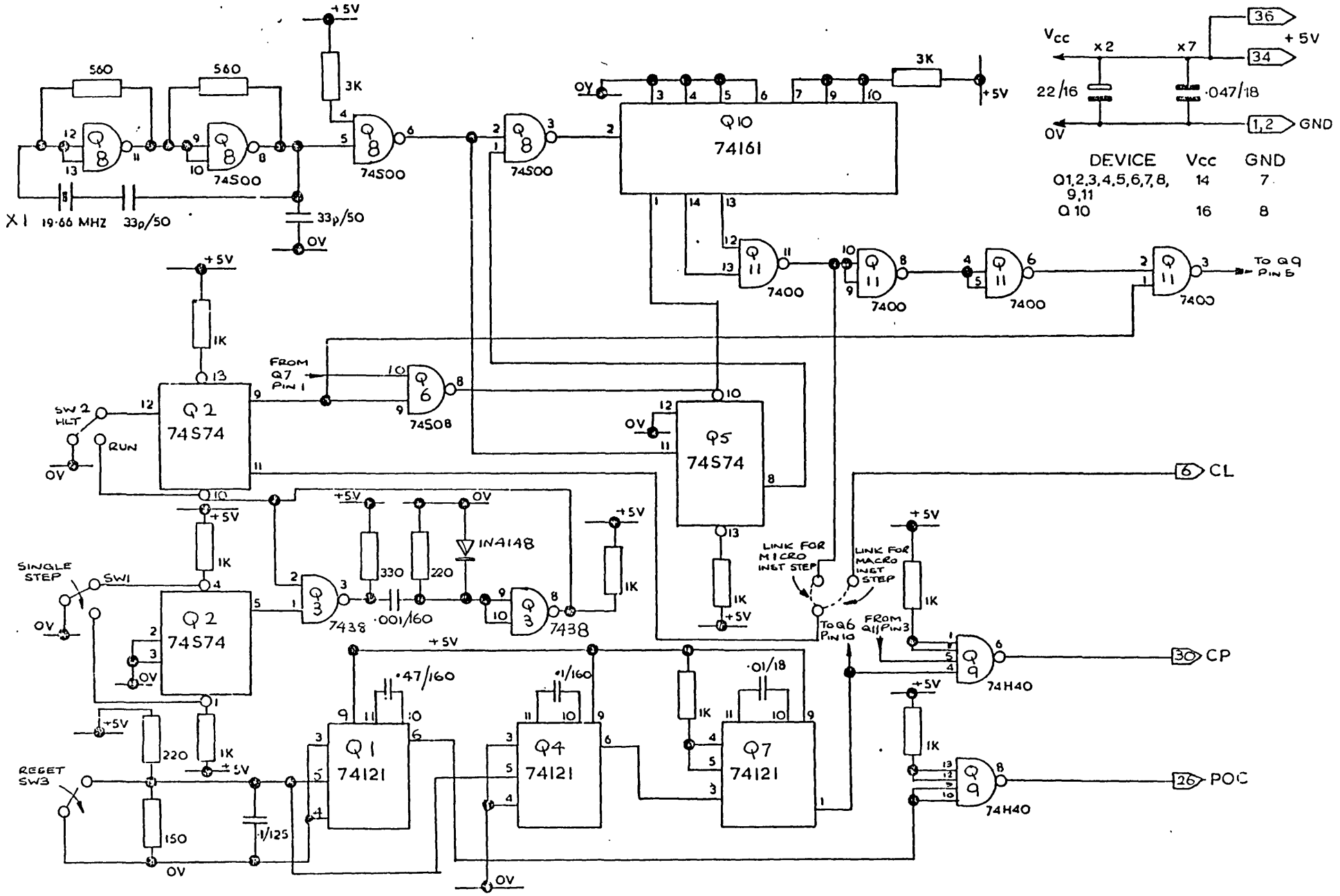


Fig. A2·1 PROTECTION PROCESSOR CLOCK GENERATOR CIRCUIT

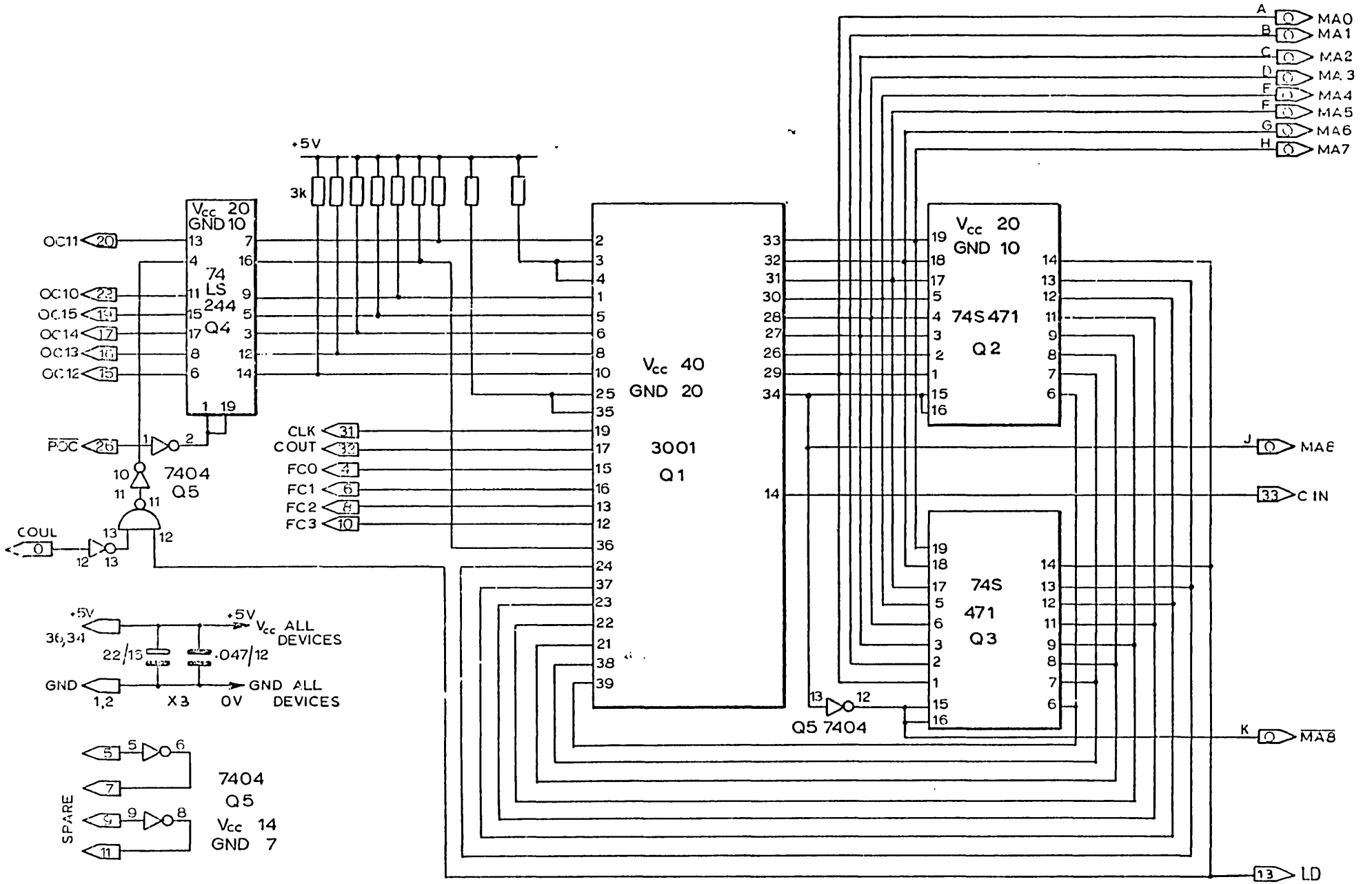
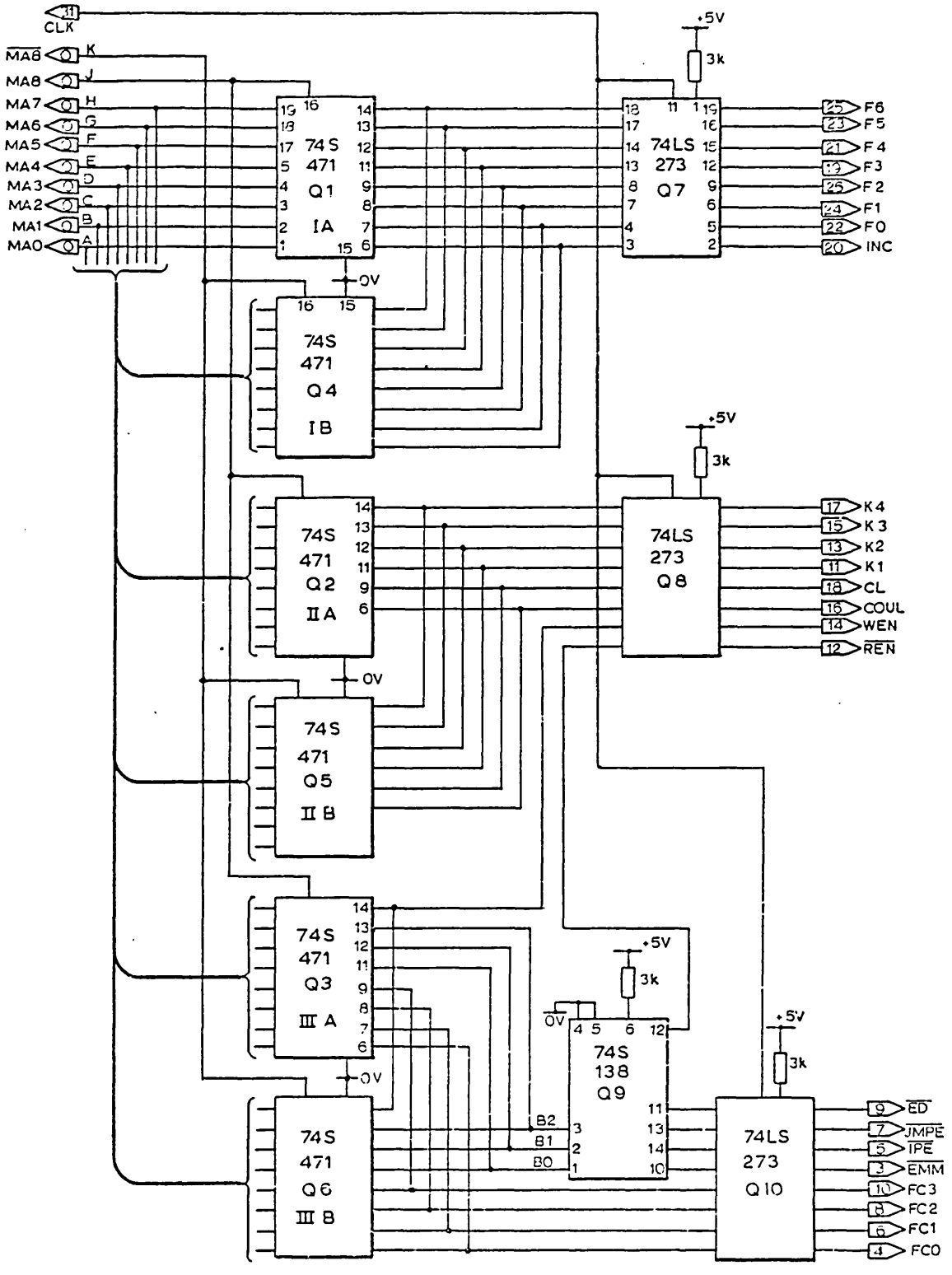
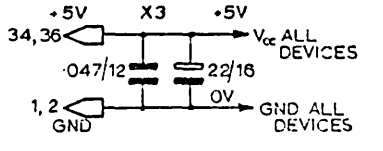


Fig. A2.2 MICROPROGRAM SEQUENCER CIRCUIT





DEVICE	V_{cc}	GND
Q 1,2,3,4,5, 6,7,8,9,10	20	10
Q 9	16	8

Fig A2.3 MICROMEMORY CIRCUIT

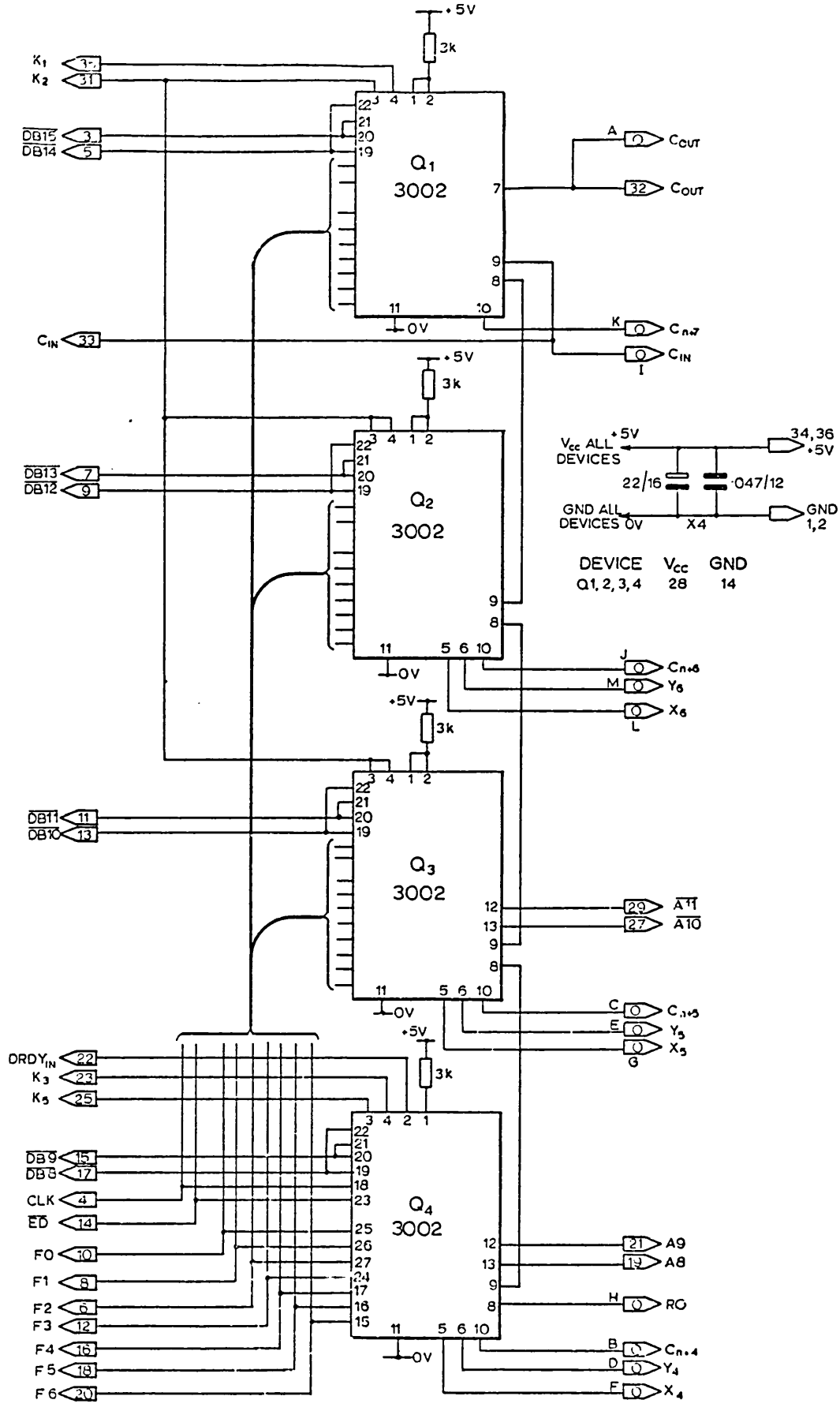


Fig. A2.4 CPU HIGH BYTE CIRCUIT

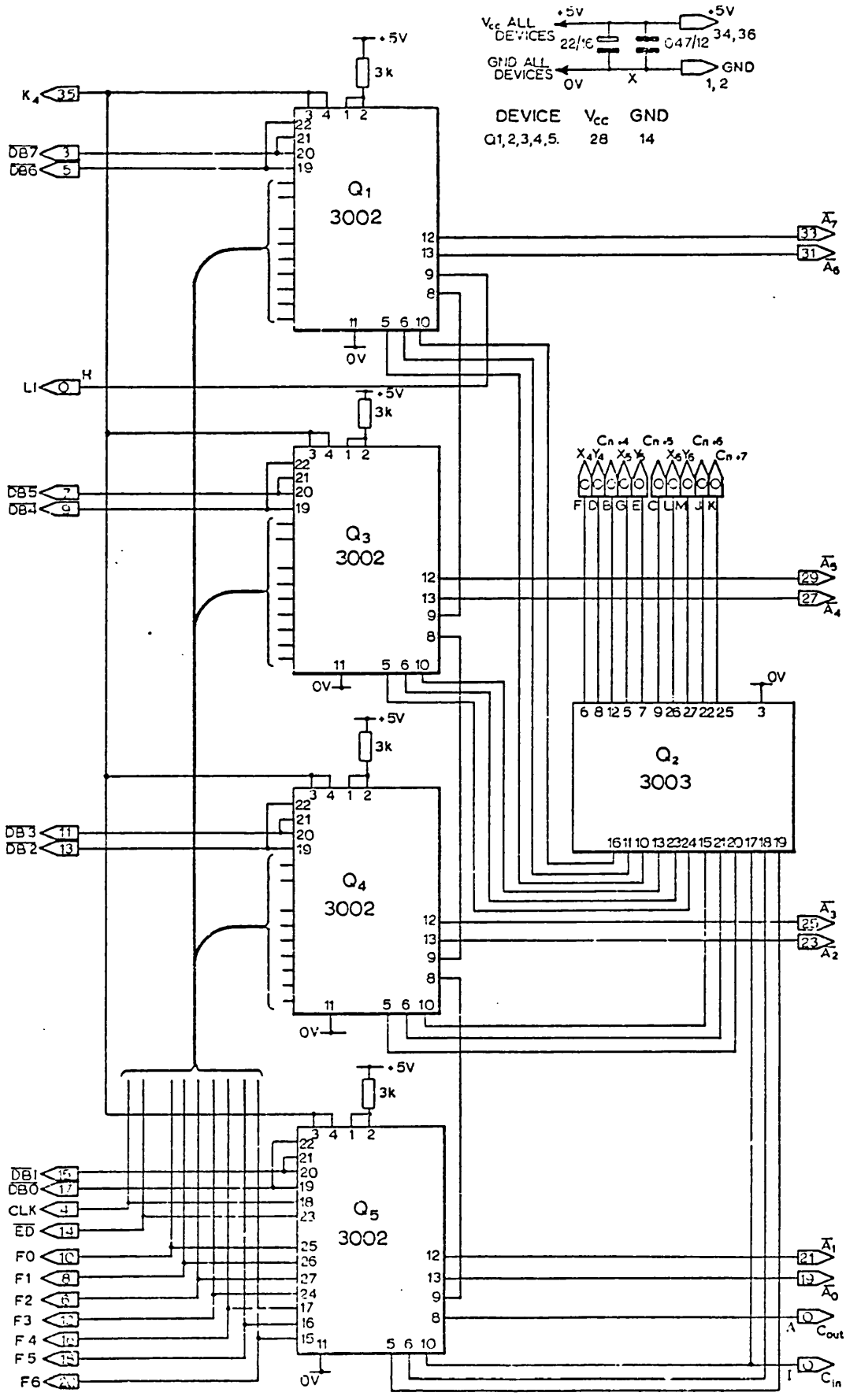


Fig. A.2.5 CPU LOW BYTE CIRCUIT

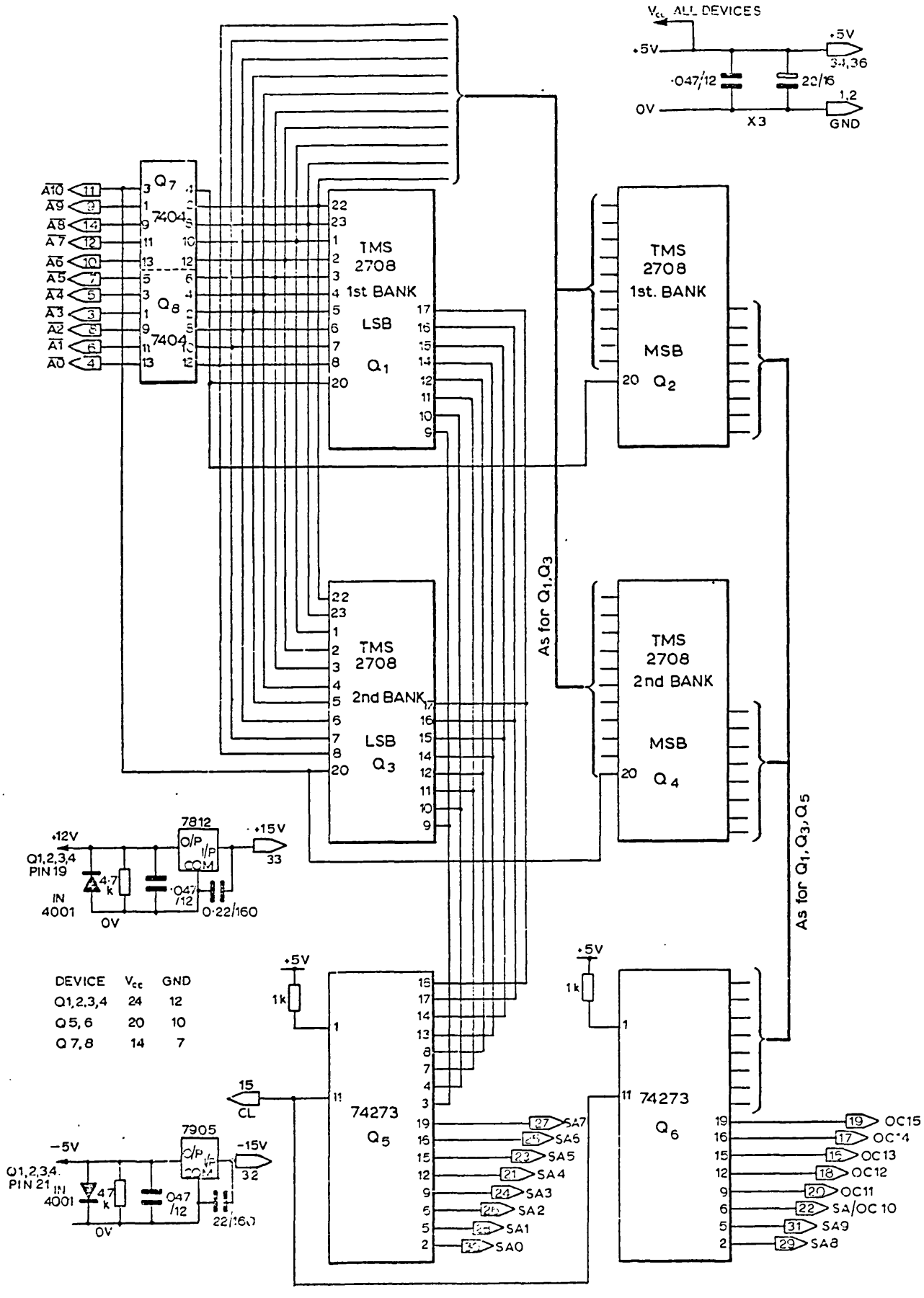


Fig A2.6 MACROMEMORY CIRCUIT

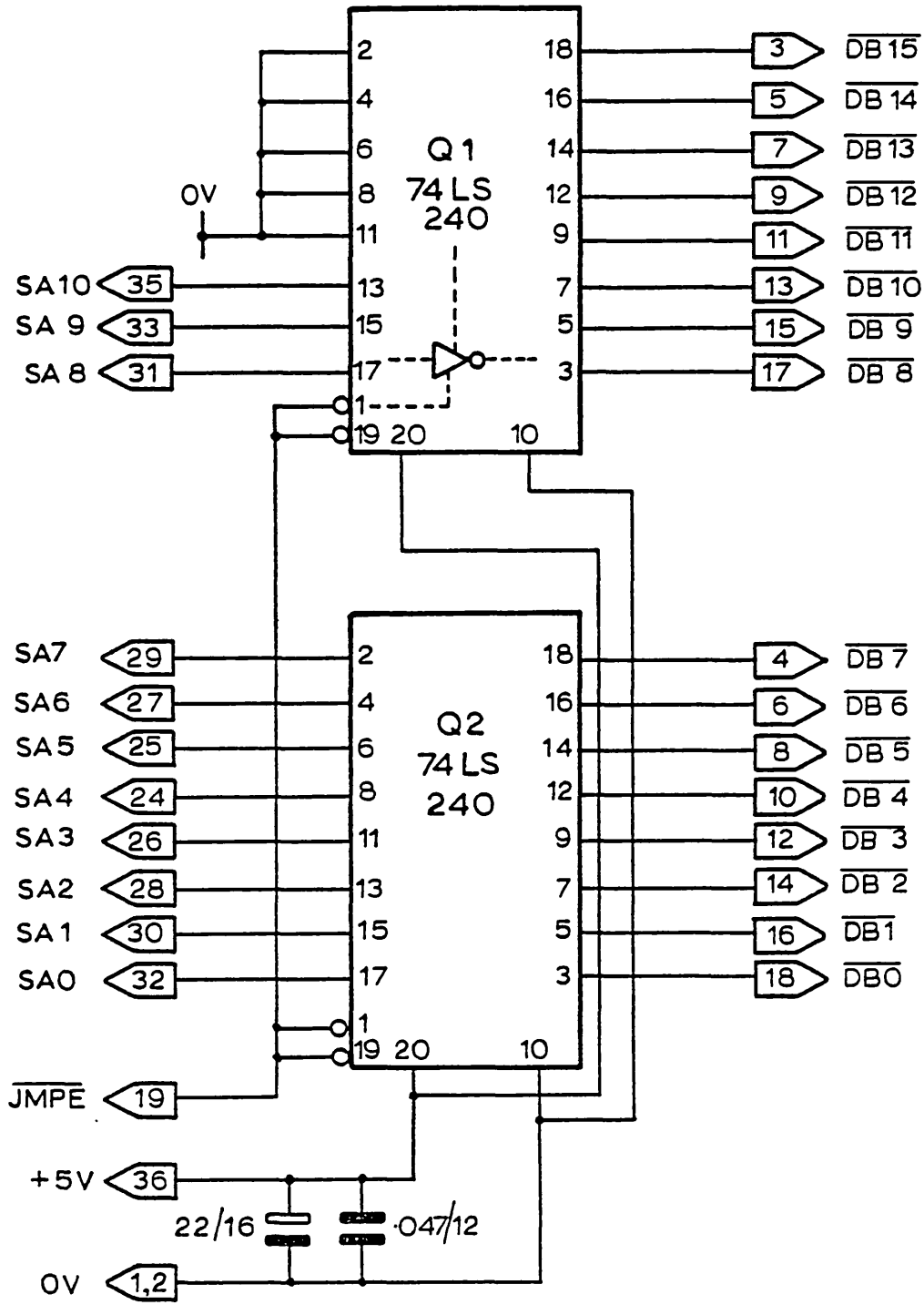


Fig. A2·7 MACROMEMORY BUS DRIVERS CIRCUIT

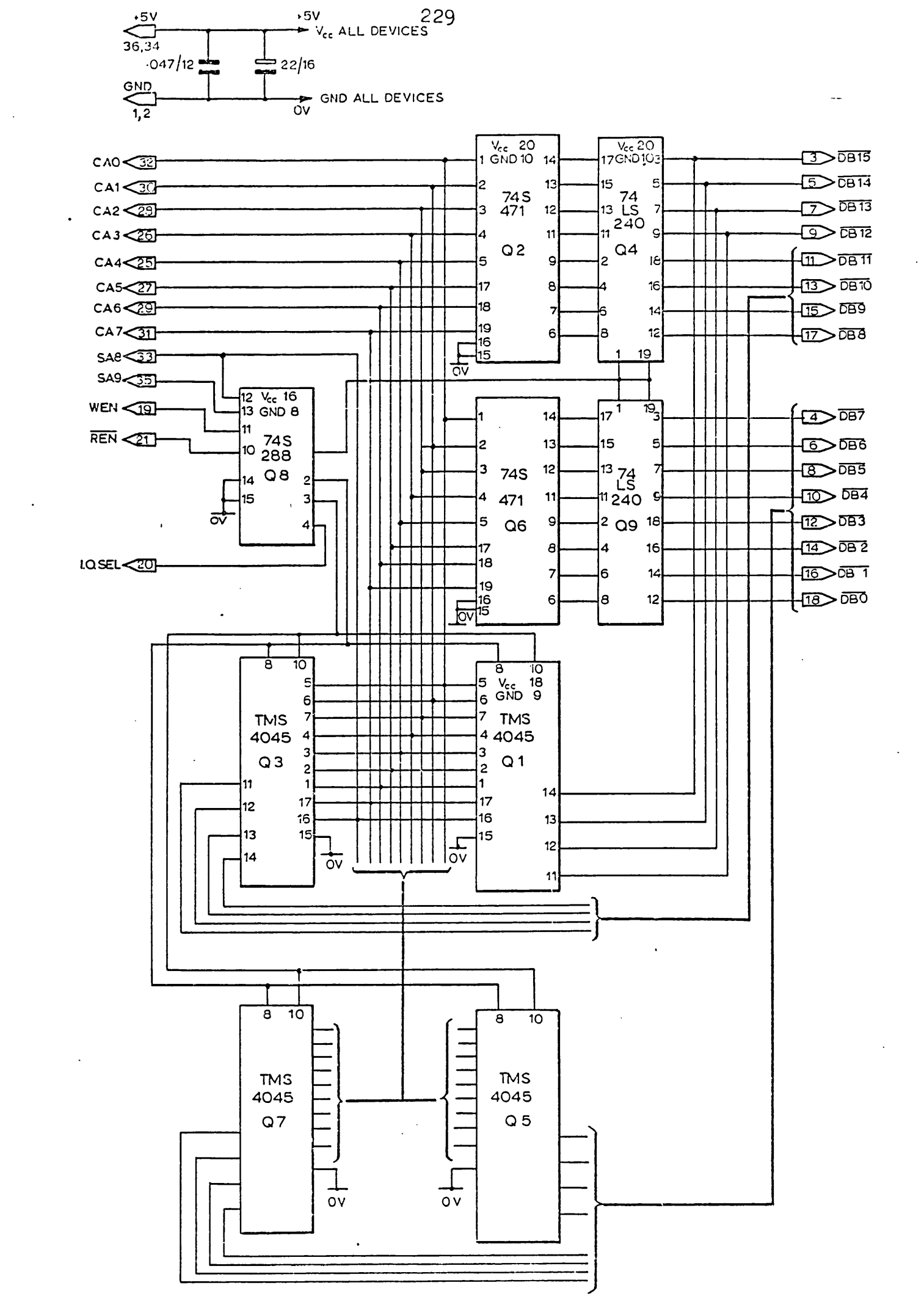


Fig. A2·8 DATA-CONSTANT MEMORY CIRCUIT

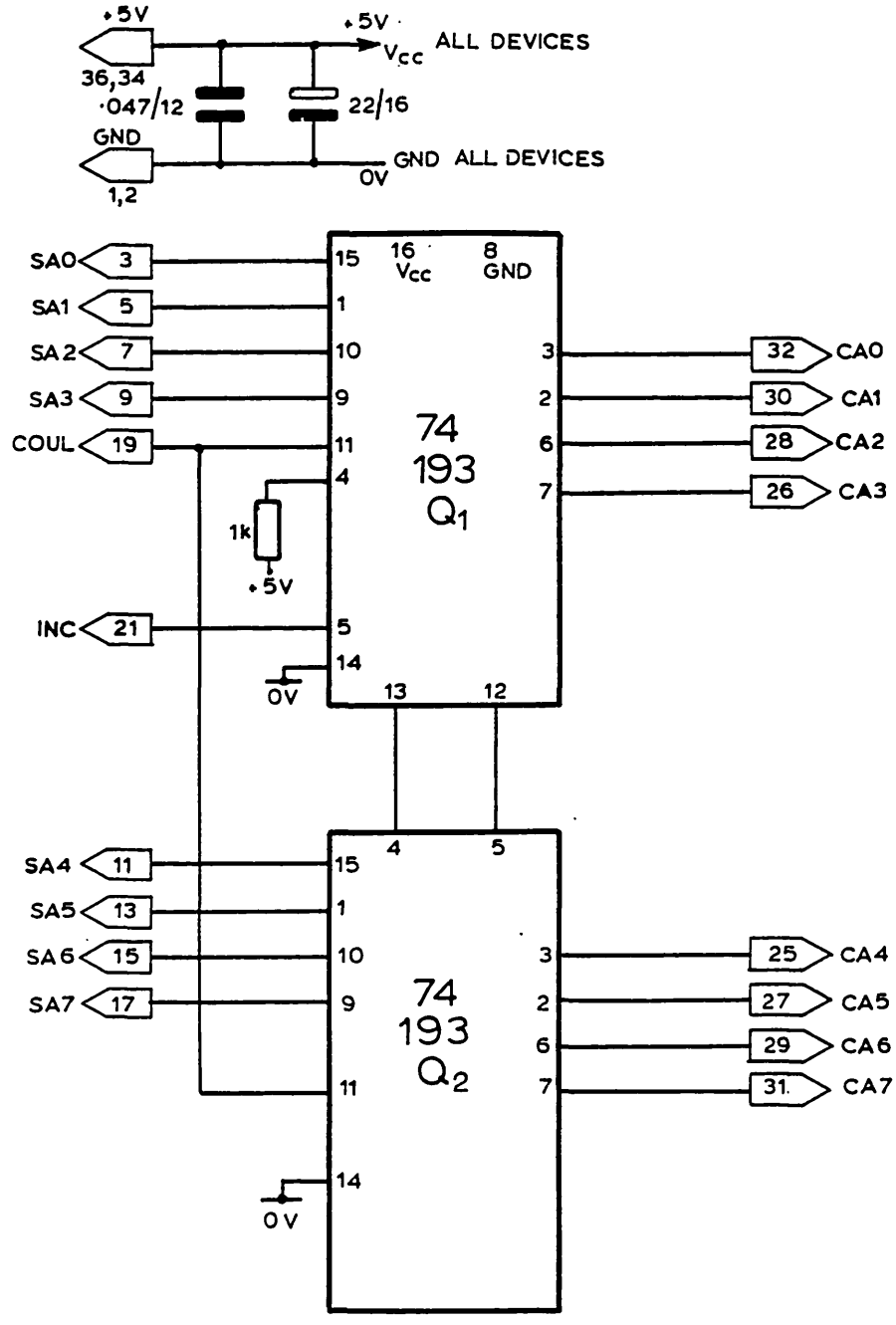


Fig. A 2·9 The data memory counters

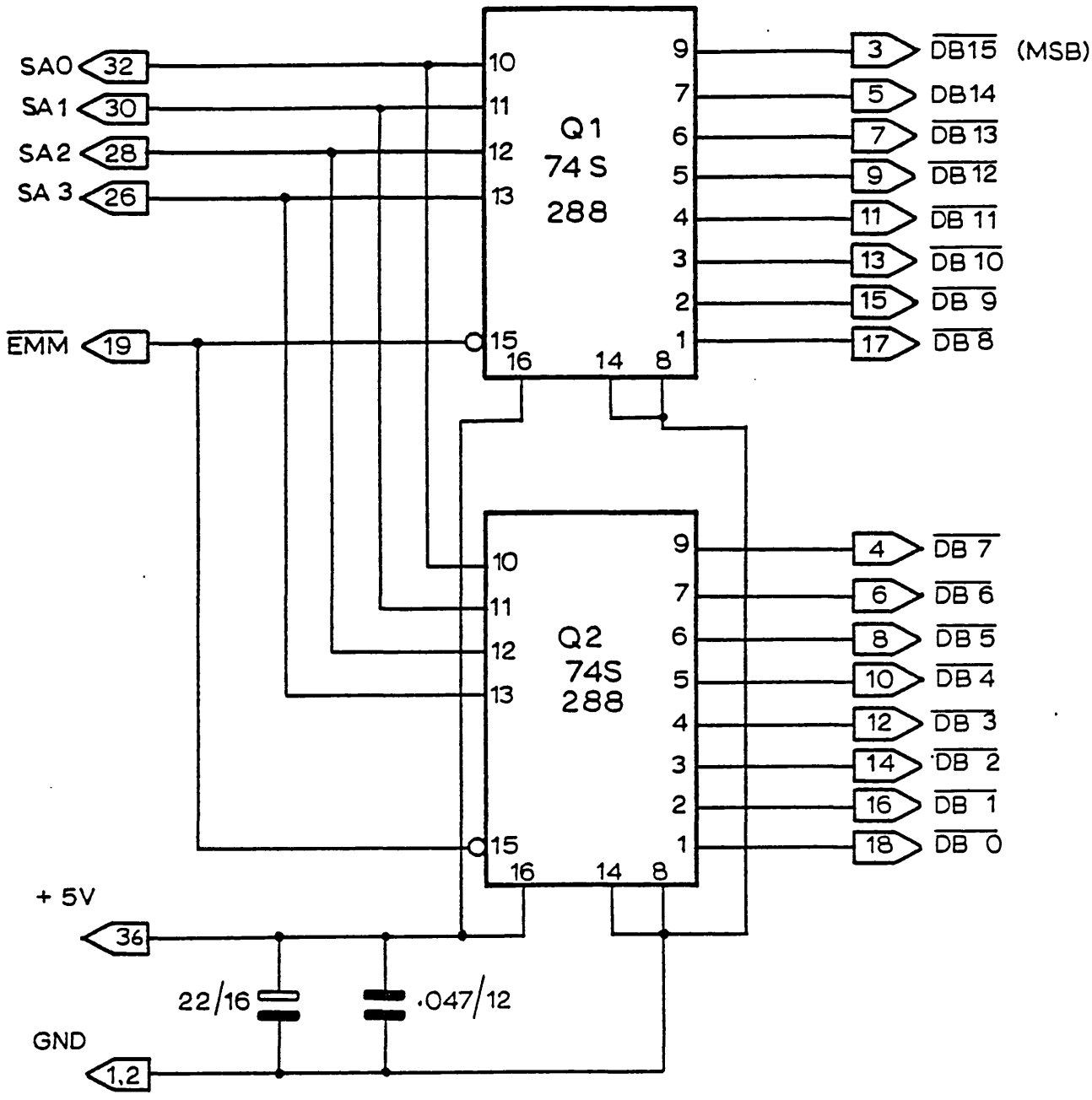


Fig. A2·10 BIT MASKING MEMORY CIRCUIT

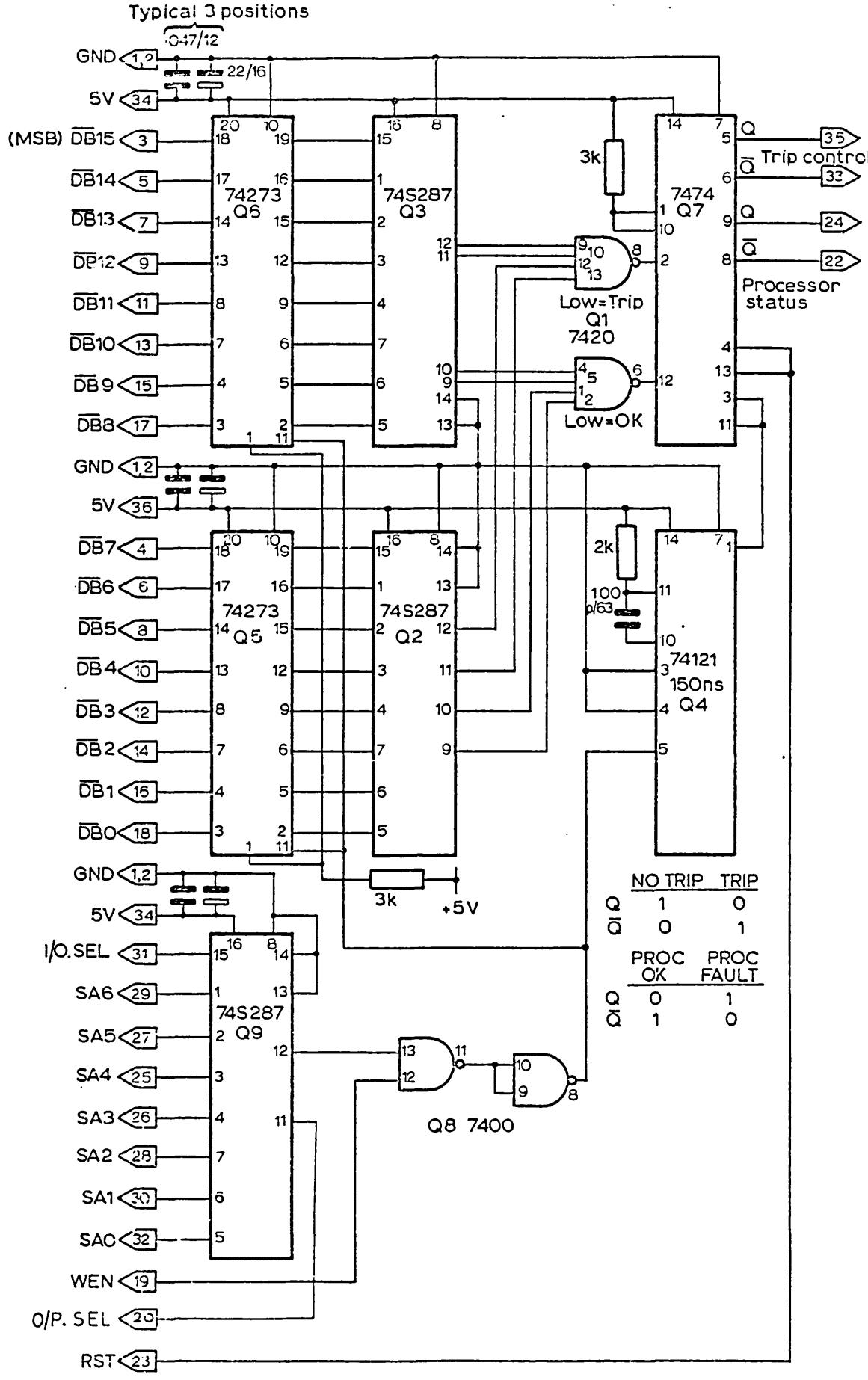


Fig. A2·11 CIRCUIT BREAKER CONTROL PORT CIRCUIT

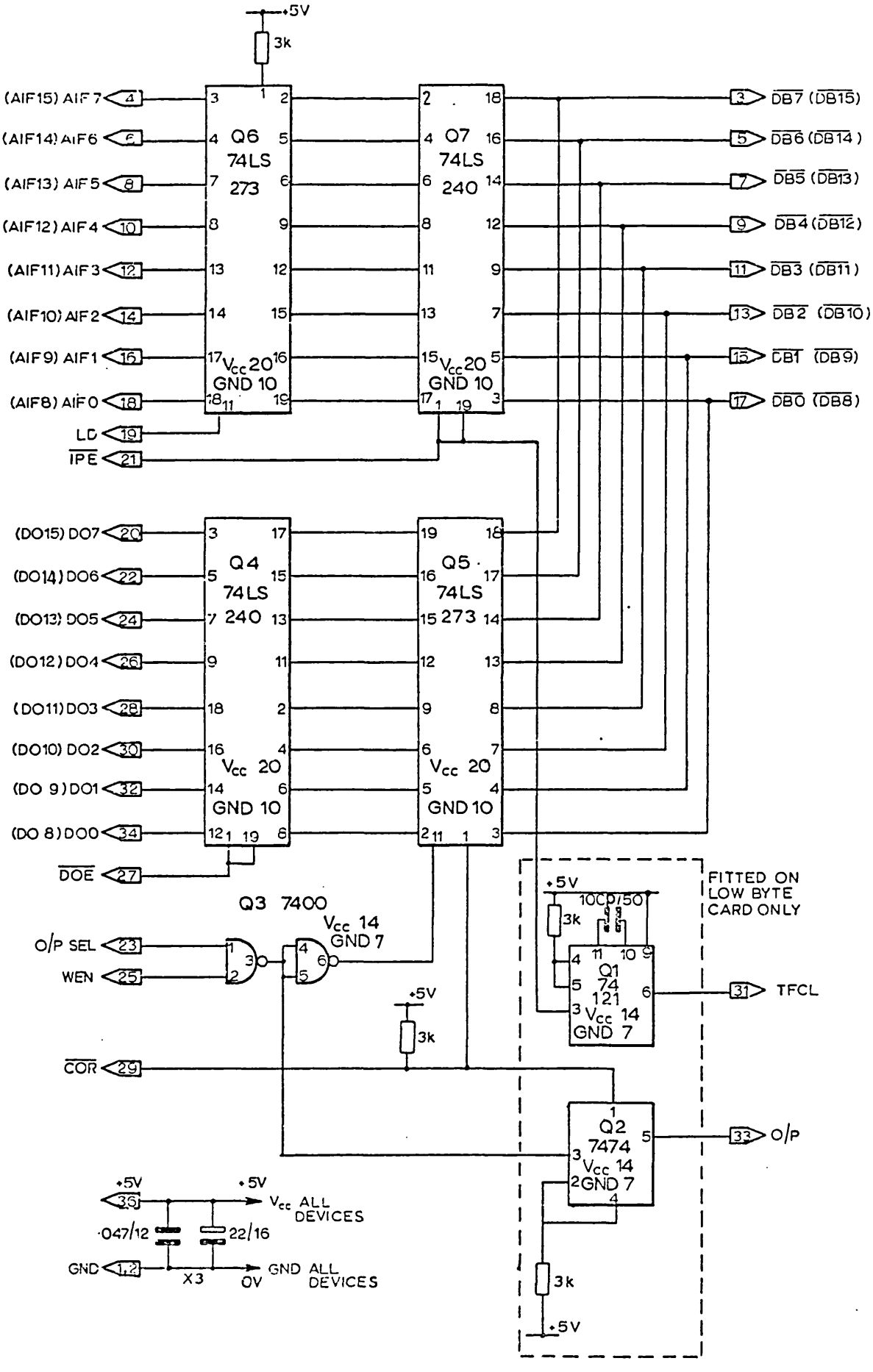


Fig. A2.12 INPUT/COMMUNICATION OUTPUT PORT LOW BYTE (HIGH BYTE) CIRCUIT

ADDRESS	DATA ROM 1	DATA ROM 2	MASK BIT
D----A	8---------1	8---------1	
0000	11111111	11111110	0
0001	11111111	11111101	1
0010	11111111	11111011	2
0011	11111111	11110111	3
0100	11111111	11101111	4
0101	11111111	11011111	5
0110	11111111	10111111	6
0111	11111111	01111111	7
1000	11111110	11111111	8
1001	11111101	11111111	9
1010	11111011	11111111	10
1011	11110111	11111111	11
1100	11101111	11111111	12
1101	11011111	11111111	13
1110	10111111	11111111	14
1111	01111111	11111111	15

Address E set to "0"

Table A2.1 Bit masking memory ROM contents map.

ADDRESS	DATA ROM 1	DATA ROM 2
H------A	O_1 O_2 O_3 O_4	O_1 O_2 O_3 O_4
10101010	1 1 1 1	1 1 1 1
01010101	0 0 1 1	0 0 1 1
ALL OTHER ADDRESSES	0 0 0 0	0 0 0 0

Table A2.2 Breaker control port, control word decoding ROM (Q2,3) map.

ADDRESS	DATA	FUNCTION
H--------A	O_2 O_1	
111 111 11	0 1	Breaker control Port enable .
101 111 11	1 0	Communication port enable.
ALL OTHER ADDRESSES	0 0	

Table A2.3 Breaker control port, address decoding ROM (Q9) map.

OUTPUT SOCKET (Mc MURDO RED-RANGE 24 WAY).

PIN NO	FUNCTION	PIN NO	FUNCTION
1	DATA OUT 0 (LSB)	13	DATA OUT 12
2	" 1	14	" 13
3	" 2	15	" 14
4	" 3	16	" 15 (MSB)
5	" 4	17	NC
6	" 5	18	OUTPUT READY FLAG
7	" 6	19	NC
8	" 7	20	CLEAR FLAG
9	" 8	21	NC
10	" 9	22	OUTPUT ENABLE
11	" 10	23	NC
12	" 11	24	NC

NC = NOT CONNECTED.

POWER PLUG (Mc MURDO RED-RANGE 8 WAY)

PIN NO	FUNCTION
1 & 5	- 15V
2 & 6	+ 15V
3 & 7	+ 5V
4 & 8	OV(GND)

Table A2.4 Protection processor data output socket and power plug details.

INPUT PLUG (McMURDO RED-RANGE 24 WAY)

PIN NO	FUNCTION	PIN N	FUNCTION
1	DATA IN 0 (LSB)	13	DATA IN 12
2	" 1	14	" 13
3	" 2	15	" 14
4	" 3	16	" 15 (MSB)
5	" 4	17	NC
6	" 5	18	DATA READY FLAG IN
7	" 6	19	NC
8	" 7	20	TRANSFER CLOCK OUT
9	" 8	21	NC
10	" 9	22	GROUND (OV)
11	" 10	23	NC
12	" 11	24	POWER ON CLEAR IN

NC = NOT CONNECTED

BREAKER CONTROL SOCKET (Mc MURDO RED-RANGE 8 WAY)

PIN NO	FUNCTION
1	Q TRIP CONTROL
2	Q " "
3	Q RELAY STATUS
4	Q " "
5	RESET RELAY STATUS
6,7,8	NC

Table A2.5 Protection processor data input plug and breaker control socket details.

APPENDIX 3

THE INSTRUCTION SET

The instruction repertoire of the 52 instructions implemented is presented here. A brief description of the instruction function, the mnemonic used as it is recognised by the cross assembler and the binary code are given.

Then the sequence of the microinstructions which implement each instruction is given as in the example:

110 ACMA FF1 REN JCR13 00010110 11110000 00110011 00111101
(i) (ii) (iii) (iv) (v) (vi) (vii) (viii)

where

(i) is the micromemory location address

(ii) is the mnemonic for the ALU array control. These are defined by the manufacturer(ref.25). The first 3 letters represent the ALU function and the following number or letter represents the register used. When there is no fourth character, then by default R0 is specified.

(iii) This group contains any special functions to control the different modules of the processor. It can be one or more of the followings:

a) K-bus definition (see table 3.3)

b) Carry/shift flag output control, specified in ref. 30.

c) Data bus control (see table 3.4).

d) Carry/shift flag input control, specified in ref. 30.

(iv) The microprogram jump address or the LD signal when a new macroinstruction is going to be fetched (see ref. 30).

(v) Contents of the PROMS IA or IB in fig. A2.3

(vi) " " " " IIA " IIB " " "

(vii) " " " " IIIA "IIIB " " "

(viii) " " " " Q_2 " Q_3 " " A2.2

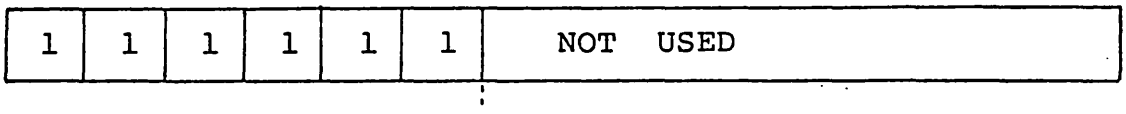
Section A3.1 gives the basic instruction set, while in A3.2 the extended set is presented.

A3.1 THE BASIC INSTRUCTION SET

INSTRUCTION — Restart the processor at main memory location Ø.

MNEMONIC — RST

FORMAT



MICRO-CODE

Ø	CLR JZR6	10000000	11110000	00000000	00100110
6	LMI FF1 JZR7	00100000	11110000	00000011	00100111
7	CLAA JZR15	10010110	11110000	00000000	00101111

Loc 15 is the start of a short fetch, whilst 14 is an extended fetch for use with short micro-code routines which are executed before macro memory access is possible.

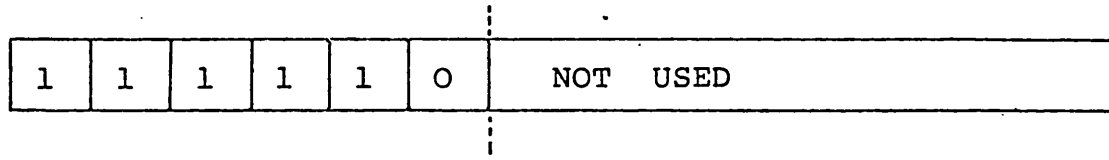
14	SDR9 FF1 CL LD	01010010	00001000	00000011	10000000
15	SDR9 FF1 JZR14	01010010	00000000	00000011	00101110

The SDR9 instruction is used for accumulator restoration purposes.

INSTRUCTION Halt the processor.

MNEMONIC HLT.

FORMAT



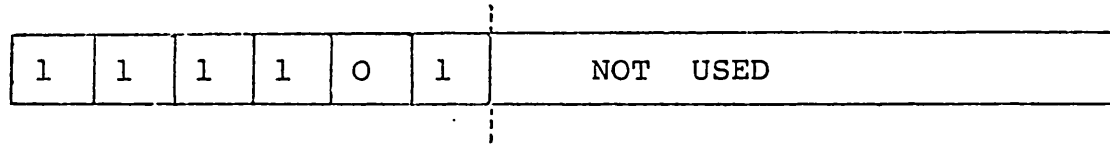
MICRO-CODE

```
1   NOP  JZR1   11000000   11110000   00000000   00100001
```

INSTRUCTION Wait until the input data ready flag is set (i.e. logical 1).

MNEMONIC WFS

FORMAT



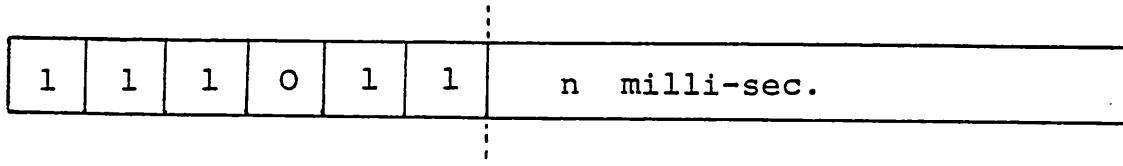
MICRO-CODE

```
8   LMI  FF1  JZR5    00100000   11110000   00000011   00100101
5   ORIT K1101 JZR4   11011100   11010000   00000000   00100100
4   NOP JFL 0         11000000   11110000   00000000   01000000
3   NOP  JZR5         11000000   11110000   00000000   00100101
2   NOP  JZR13        11000000   11110000   00000000   00101101
```

INSTRUCTION — Wait for n milli-secs., where n is specified by the contents of the data field. This instruction must be preceded by loading the accumulator with the constant 1664. i.e. LDA loc where (loc) = 1664.

MNEMONIC — PAU.

FORMAT



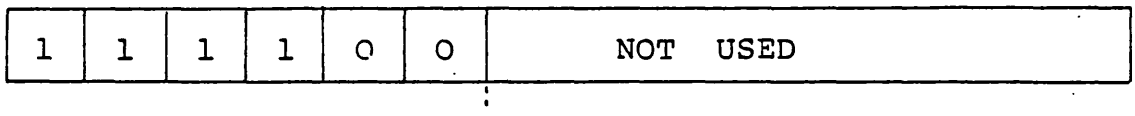
MICRO CODE

```
16  LDMT JMPE JCR6    00110100 00000000 00100000 00110110
22  LMI  FF1  JCR3    00100000 11110000 00000011 00110011
19  DCAA      JCR4    00111110 00000000 00000000 00110100
20  TZAA      JCR5    10111110 00000000 00000000 00110101
21  NOP       JFL1    11000000 11110000 00000000 01000001
18  TZRT K1100 JCR15  10111100 11000000 00000000 00111111
31  ILR9      JFL1    00010010 11110000 00000000 01000001
26  SDR9 FF1 CL LD    01010010 00001000 00000011 10000000
27  DCAT      JCR3    00111100 00000000 00000000 00110011
```

INSTRUCTION No operation.

MNEMONIC NOP

FORMAT



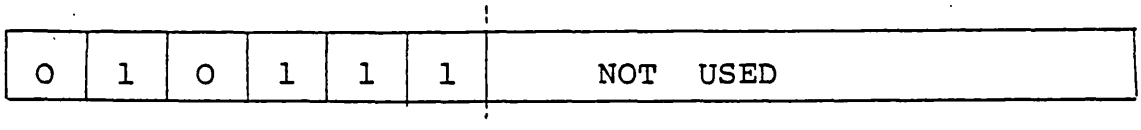
MICRO-CODE

9	LMI FF1	JZR10	00100000	11110000	00000011	00101010
10	NOP	JZR15	11000000	11110000	00000000	00101111

INSTRUCTION Decrement the loop counter and skip the following instruction if the result is zero. (count skip loop).

MNEMONIC C S L

FORMAT



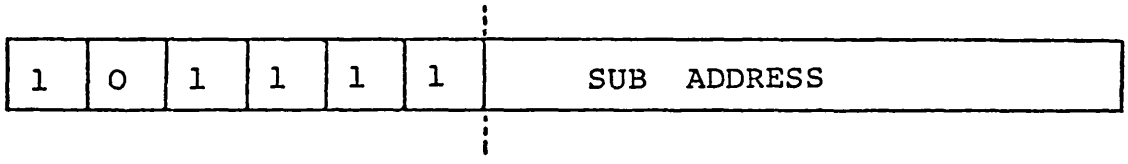
MICRO-CODE

160	DSM8	JCR4	00110000	00000000	00000000	00110100
164	TZR8	JCR5	10110000	00000000	00000000	00110101
165	LMI FF1	JFL10	00100000	11110000	00000011	01001010
162	LMI FF1	JCR3	00100000	11110000	00000011	00110011
163	NOP	JZR15	11000000	11110000	00000000	00101111

INSTRUCTION Load the accumulator from the data/constant store as specified by the sub address.

MNEMONIC LDA

FORMAT



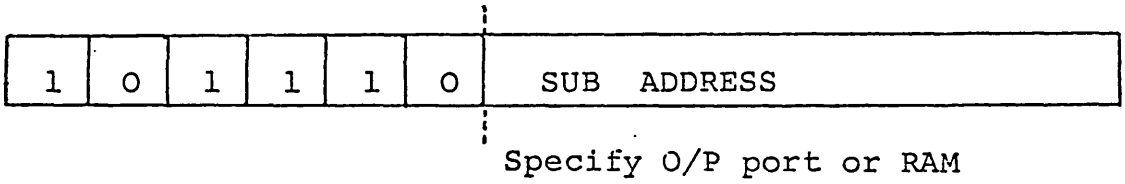
MICRO-CODE

64	LMI FF1 REN JCR6	00100000	11110000	00110011	00110110
70	NOP REN JCR 7	11000000	11110000	00110000	00110111
71	LMFA REN JZR 14	11010110	11110000	00110000	00101110

INSTRUCTION Store the accumulator in the data store location or output port as specified by the sub-address.

MNEMONIC STA

FORMAT



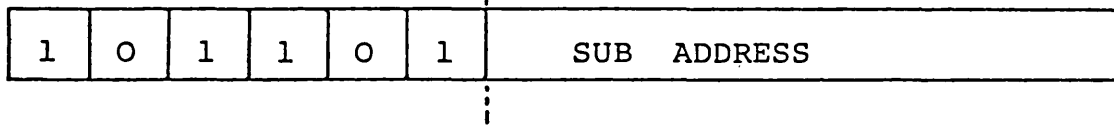
MICRO-CODE

65	LMI FF1 EDB JCR4	00100000	11110000	01000011	00110100
68	NOP EDB WEN JCR5	11000000	11110000	11000000	00110101
69	NOP EDB WEN JZR14	11000000	11110000	11000000	00101110

INSTRUCTION Add (2's complement) the data in the constant/data store location as specified by the sub-address to the contents of the accumulator.

MNEMONIC ADD

FORMAT



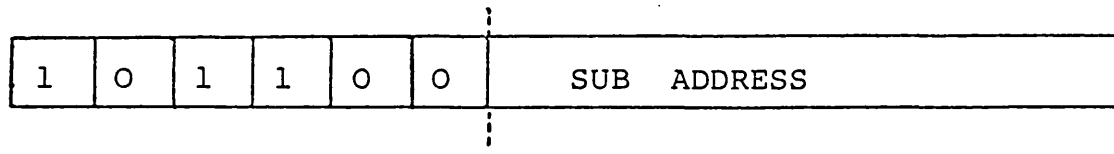
MICRO-CODE

72	LMI	FF1 REN	JCR14	00100000	11110000	00110011	00111110
78	NOP	REN	JCR15	11000000	11110000	00110000	00111111
79	AMAA	REN	JZR14	00010110	00000000	00110000	00101110

INSTRUCTION Logically 'and' the contents of the constant/data store location as specified by the sub-address to the contents of the accumulator.

MNEMONIC AND.

FORMAT



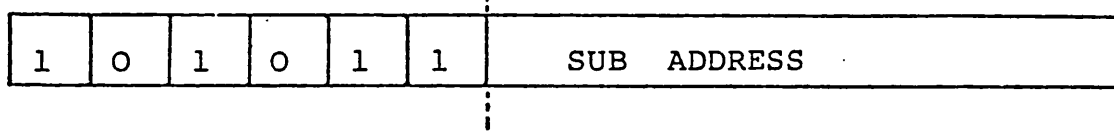
MICRO-CODE

73	LMI	FF1 REN	JCR12	00100000	11110000	00110011	00111100
76	NOP	REN	JCR13	11000000	11110000	00110000	00111101
71	ANMA		JZR14	10010110	00000000	00110000	00101110

INSTRUCTION Exclusive or the contents of the data/constant store location as specified with the contents of the accumulator.

MNEMONIC XOR

FORMAT



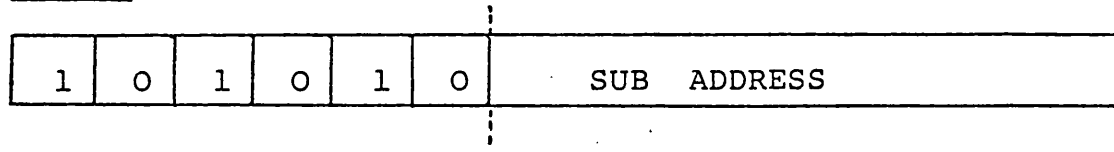
MICRO-CODE

80	LMI	FF1 REN	JCR5	00100000	11110000	00110011	00110101
85	NOP	REN	JCR6	11000000	11110000	00110000	00110110
86	XNMA	REN	JCR7	11110110	00000000	00110000	00110111
87	CMAA	JZR 14		11111110	11110000	00000000	00101110

INSTRUCTION Subtract the contents of the data/constant store location as specified from the contents of the accumulator.

MNEMONIC SUB

FORMAT



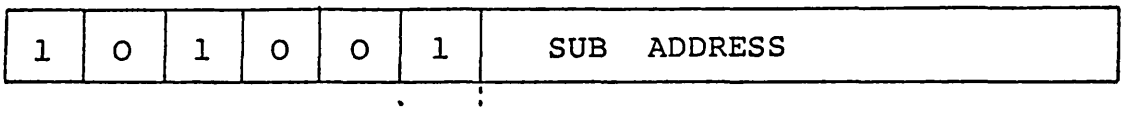
MICRO-CODE

81	LMI	FF1 REN	JCR2	00100000	11110000	00110011	00110010
82	NOP	REN	JCR3	11000000	11110000	00110000	00110011
83	LCMT	REN	JCR4	11110100	11110000	00110000	00110100
84	ALRT	FF1	JZR14	00011000	00000000	00000011	00101110

INSTRUCTION Decrement the contents of the data store location as specified and skip the following instruction if the result is zero.

MNEMONIC DSZ

FORMAT



Specify RAM

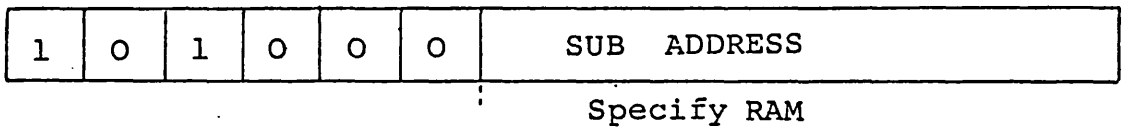
MICRO-CODE

88	NOP REN JCR15	11000000	11110000	00110000	00111111
95	NOP REN JCC6	11000000	11110000	00110000	00000110
111	LDMA REN JCR13	00110110	00000000	00110000	00111101
109	LMI FF1 JCC5	00100000	11110000	00000011	00000101
93	TZAA EDB WEN JCR12	10111110	00000000	11000000	00111100
92	NOP EDB WEN JFL5	11000000	11110000	11000000	01000101
91	ILR9 CL LD	00010010	11111000	00000000	10000000
90	LMI FF1 JCC6	00100000	11110000	00000011	00000110
106	ILR9 JZR15	00010010	11110000	00000000	00101111

INSTRUCTION — Increment the contents of the data store location as specified and skip the following instruction if the result is zero.

MNEMONIC — ISZ.

FORMAT



MICRO-CODE

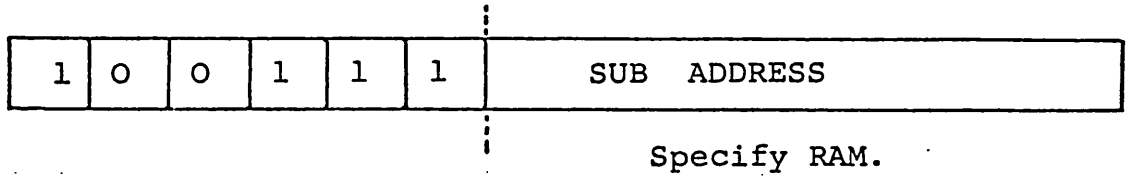
89	NOP REN JCR14	11000000	11110000	00110000	00111110
94	NOP REN JCC6	11000000	11110000	00110000	00000110
110	ACMA FF1 REN JCR13	00010110	11110000	00110011	00111101
109	LMI FF1 JCC5	00100000	11110000	00000011	00000101
93	TZAA EDB WEN JCR12	10111110	00000000	11000000	00111100
92	NOP EDB WEN JFL5	11000000	11110000	11000000	01000101
91	ILR9 CL LD	00010010	11111000	00000000	10000000
90	LMI FF1 JCC6	00100000	11110000	00000011	00000110
106	ILR9 JZR15	00010010	11110000	00000000	00101111

Shares μ code with instruction DSZ

INSTRUCTION Deposit zero in the data store location as specified by the sub-address.

MNEMONIC DZM

FORMAT



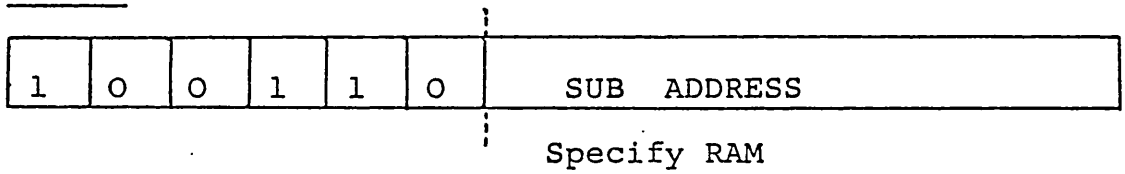
MICRO-CODE

96	LM1 FF1 JCR2	00100000	11110000	00000011	00110010
98	CLAA EDB JCC2	10010110	11110000	01000000	00000010
34	NOP EDB WEN JCR3	11000000	11110000	11000000	00110011
35	NOP EDB WEN JZR13	11000000	11110000	11000000	00101101

INSTRUCTION Sum the accumulator data in the memory location specified.

MNEMONIC SUM

FORMAT



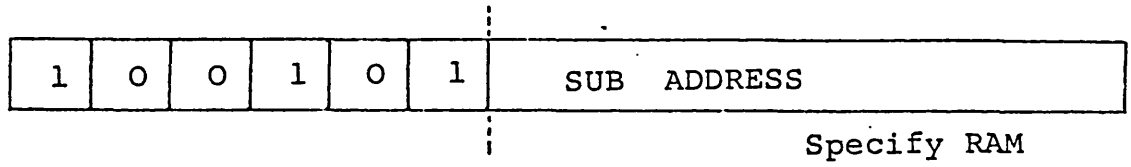
MICRO-CODE

97	LMI FF1 REN JCR3	00100000	11110000	00110011	00110011
99	NOP REN JCR4	11000000	11110000	00110000	00110100
100	AMAA REN JCR5	00010110	00000000	00110000	00110101
101	NOP JCR6	11000000	11110000	00000000	00110110
102	NOP EDB WEN JCC7	11000000	11110000	11000000	00000111
118	NOP EDB WEN JZR13	11000000	11110000	11000000	00101101

INSTRUCTION Transfer data from input port to data store location as specified.

MNEMONIC IDM.

FORMAT



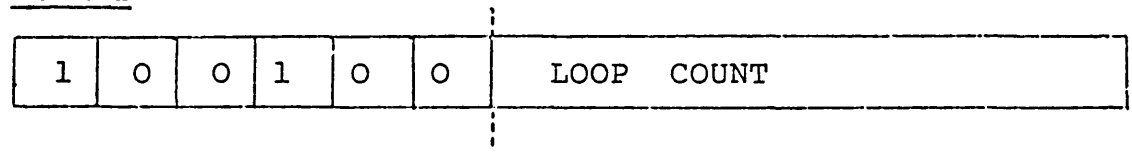
MICRO-CODE

104	LMI	FF1	IPE	JCR11	00100000	11110000	00010011	00111011
107	NOP	IPE	WEN	JCR12	11000000	11110000	10010000	00111100
108	NOP	IPE	WEN	JZR14	11000000	11110000	10010000	00101110

INSTRUCTION Load the loop counter with the data specified in the 10 least significant bits of the instruction.

MNEMONIC LDL

FORMAT



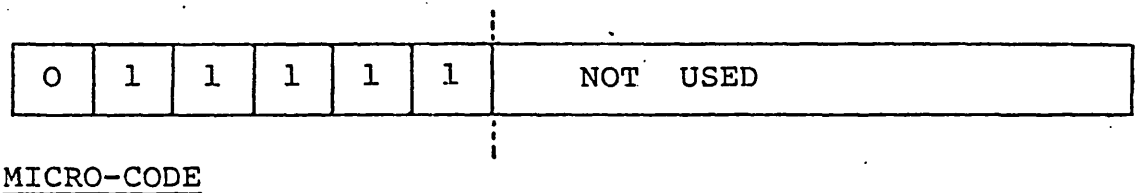
MICRO-CODE

105	LM1	FF1	JMPE	JCR7	00100000	11110000	00100011	00110111
103	ACMA	JMPE	JCC7		00010110	11110000	00100000	00000111
119	SDR	FF1	JZR13		01010000	00000000	00000011	00101101

INSTRUCTION Form the 1's complement of the accumulator contents.

MNEMONIC COM.

FORMAT



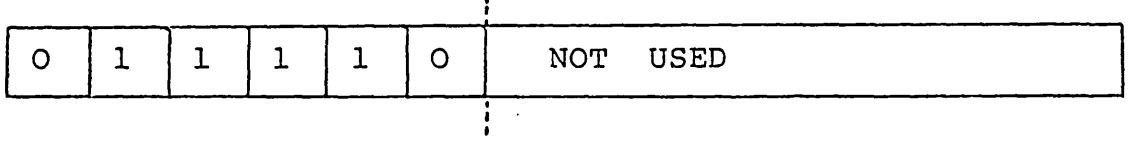
MICRO-CODE

```
128  LMI  FF1  JCR7  00100000   11110000   00000011   00110111
135  CMAA JZR15     11111110   11110000   00000000   00101111
```

INSTRUCTION Clear the accumulator.

MNEMONIC CLA

FORMAT



MICRO-CODE

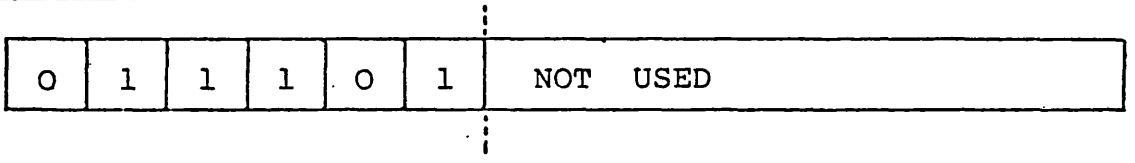
```
129  LMI FF1  JZR7    00100000   11110000   00000011   00100111
```

NOTE: Shares μ-code with instruction RST.

INSTRUCTION Form the 2's complement of the accumulator contents.

MNEMONIC NEG

FORMAT



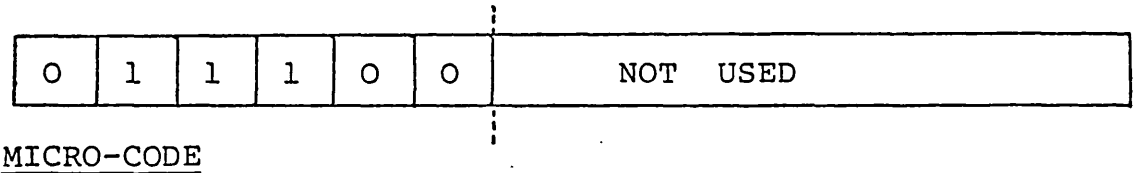
MICRO-CODE

```
136  LMI   FF1  JCR15    00100000   11110000   00000011   00111111
143  CIA   FF1  JZR15    00111110   11110000   00000011   00101111
```

INSTRUCTION Extend the sign of the A-D converter input data through the M.S.Bs of the accumulator.

MNEMONIC EXS

FORMAT



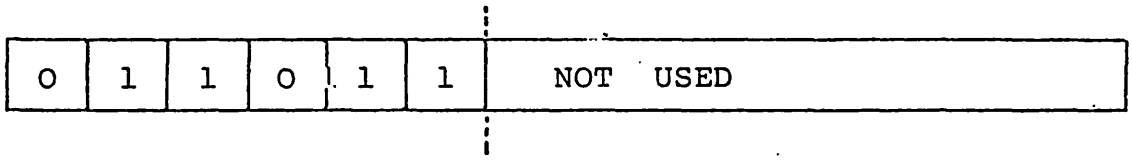
MICRO-CODE

```
137  TZAA  K1101  JCR14    10111110   11010000   00000000   00111110
142  LMI   FF1   JFL8      00100000   11110000   00000011   01001000
138  TZR9  K1110  JCR13    10110010   11100000   00000000   00111101
139  CSAA  JCR12           01010110   11110000   00000000   00111100
140  ORR9  K0011  JZR13    11010010   00110000   00000000   00101101
141  ILR9  JZR 14          00010010   11110000   00000000   00101110
```

INSTRUCTION Decrement the accumulator.

MNEMONIC DEC

FORMAT



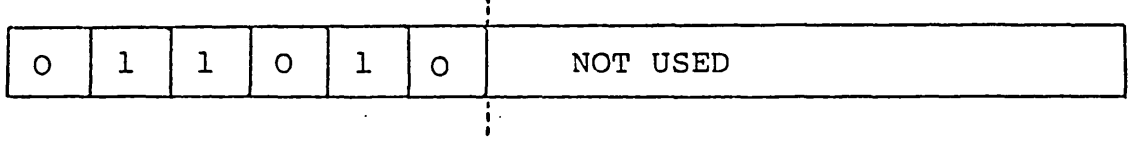
MICRO-CODE

```
144  LMI   FF1  JCR6    00100000   11110000   00000011   00110110
150  SDAA  JZR15        01010110   00000000   00000000   00101111
```

INSTRUCTION Increment the accumulator.

MNEMONIC INC

FORMAT



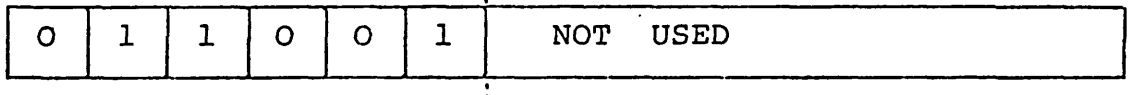
MICRO-CODE

```
145  LMI   FF1  JCR7    00100000   11110000   00000011   00110111
151  INAA  FF1  JZR15   01111110   11110000   00000011   00101111
```

INSTRUCTION Shift the contents of the accumulator one place left and fill the L.S.B. with zero.

MNEMONIC SHL

FORMAT



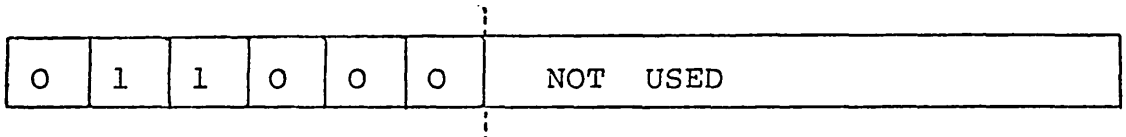
MICRO-CODE

```
152  LMI   FF1  JCR15   00100000  11110000  00000011  00111111
159  ALRA       JZR15   00011010  00000000  00000000  00101111
```

INSTRUCTION Shift the contents of the accumulator one place right and fill the M.S.B. with zero.

MNEMONIC SHR

FORMAT



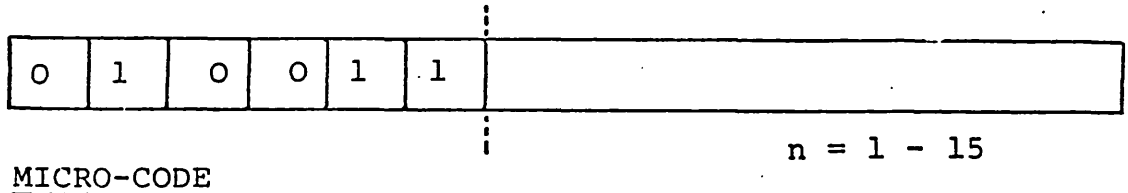
MICRO-CODE

```
153  LMI   FF1  JCR14   00100000  11110000  00000011  00111110
158  SRAA       JZR15   00011110  11110000  00000000  00101111
```

INSTRUCTION Shift the contents of the accumulator left n times, where n is specified by the 4 least significant bits of the address field.

MNEMONIC MSL

FORMAT



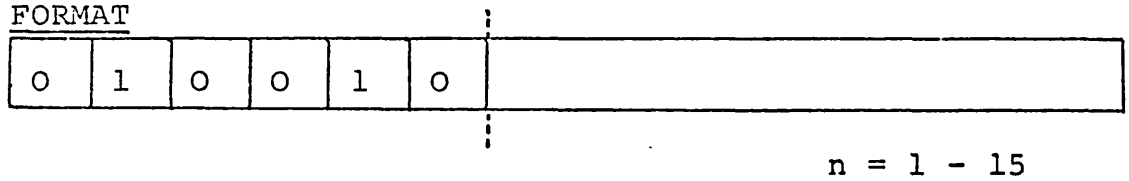
MICRO-CODE

176	LDMT JMPE JCR7	00110100	00000000	00100000	00110111
183	LMI FF1 JCR6	00100000	11110000	00000011	00110110
182	TZRT JCR4	10111000	00000000	11100000	00110100
180	ALRA JFL11	00011010	00000000	00000000	01001011
178	SDR9 FF1 CL LD	01010010	00001000	00000011	10000000
179	DCAT JCR6	00111100	00000000	00000000	00110110

INSTRUCTION Shift the contents of the accumulator right n times, where n is specified by the 4 least significant bits of the address field.

MNEMONIC MSR

FORMAT



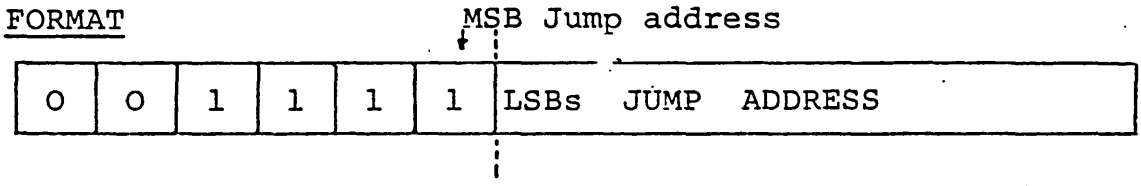
MICRO-CODE

177	LDMT JMPE JCR5	00110100	00000000	00100000	00110101
181	LMI FF1 JCC12	00100000	11110000	00000011	00001100
197	TZRT JCR4	10111000	00000000	00000000	00110100
196	SRAA JFL12	00011110	11110000	00000000	01001100
194	SDR9 FF1 CL LD	01010010	00001000	00000011	10000000
195	DCAT JCR5	00111100	00000000	00000000	00110101

INSTRUCTION Jump in high page i.e. fetch the next instruction from the location specified within the range 1024→2047.

MNEMONIC JHP

FORMAT



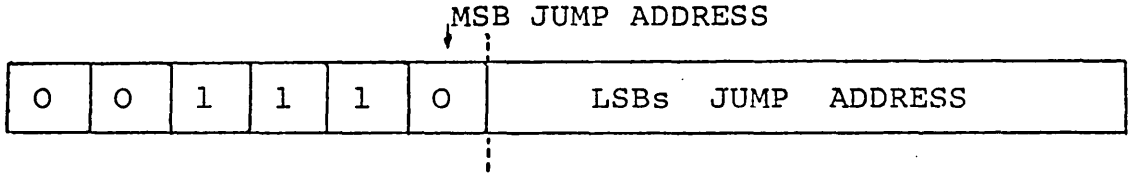
MICRO-CODE

192	LMMA JMPE	FF1	JCR6	00110110	11110000	00100011	00110110
198	SDR	FF1	JCR7	01000000	00000000	00000011	00110111
199	ILR9		JZR14	00010010	11110000	00000000	00101110

INSTRUCTION Jump in low page. i.e. fetch next instruction from the location specified within the range 0 → 1023.

MNEMONIC JLP

FORMAT



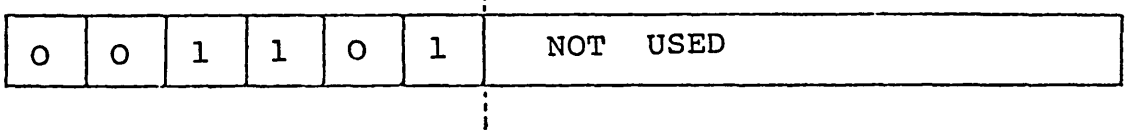
MICRO-CODE

193	LMMA JMPE	FF1	JCR6	00110110	11110000	00100011	00110110
198	SDR	FF1	JCR7	01000000	00000000	00000011	00110111
199	ILR9		JZR14	00010010	11110000	00000000	00101110

INSTRUCTION Return from subroutine to instruction following subroutine call.

MNEMONIC RET

FORMAT



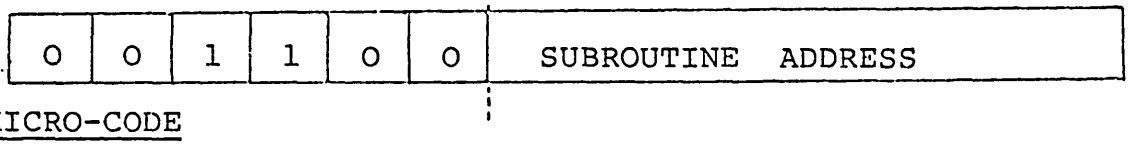
MICRO-CODE

200	LMI7 FF1	JCR15	00101110	11110000	00000011	00111111
207	ILR7	JCR14	00001110	11110000	00000000	00111110
206	SDR FF1	JZR13	01000000	00000000	00000011	00101101

INSTRUCTION Jumpt to subroutine starting at the address specified.

MNEMONIC JSR

FORMAT



MICRO-CODE

201	ILR JCR10		00000000	11110000	00000000	00111010
202	SDR7 FF1 JCR11		01001110	00000000	00000011	00111011
203	LMMA JMPE FF1	JCR12	00110110	11110000	00100011	00111100
204	SDR FF1	JCR13	01000000	00000000	00000011	00111101
205	ILR	JZR14	00010010	11110000	00000000	00101110

INSTRUCTION Skip the following instruction if the contents of the accumulator differ from the contents of the data/constant store location as specified.

MNEMONIC SAD

FORMAT

0	0	0	1	1	0	SUB ADDRESS

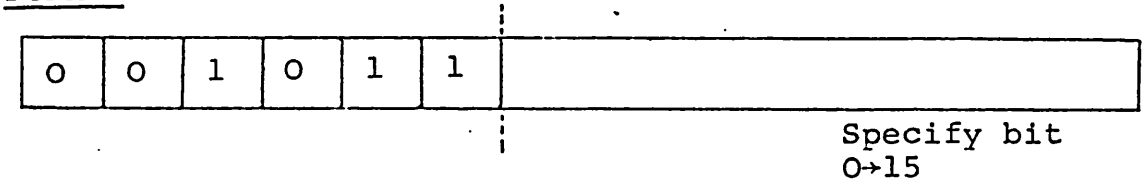
MICRO-CODE

225	LMI FF1 REN JCR2	00100000	11110000	00110011	00110010
226	NOP REN JCR3	11000000	11110000	00110000	00110011
227	XNMA REN JCR4	11110110	00000000	00110000	00110100
228	CMAA JCR5	11111110	11110000	00000000	00110101
229	TZAA JCR15	10111110	00000000	00000000	00111111
239	NOP JFL14	11000000	11110000	00000000	01001110
234	ILR9 CL LD	00010010	11111000	00000000	10000000
235	LMI FF1 JCR12	00100000	11110000	00000011	00111100
236	ILR9 JZR15	00010010	11110000	00000000	00101111

INSTRUCTION Skip the following instruction if the accumulator bit, specified by the 4 LSBs of this instruction, is clear.

MNEMONIC SBC

FORMAT



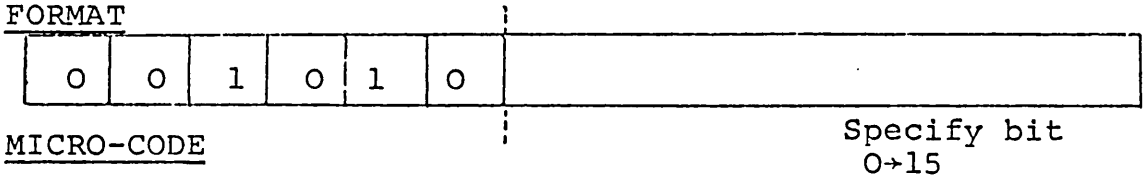
MICRO-CODE

208	LMI	FF1	EMM	JCR7	00100000	11110000	01010011	00110111
215	ANMA		EMM	JCR13	10010110	00000000	01010000	00111101
221	NOP		JFL13		11000000	11110000	00000000	01001101
218	LMI	FF1		JCR12	00100000	11110000	00000011	00111100
219	ILR9	CL	LD		00010010	11111000	00000000	10000000
220	ILR9			JZR15	00010010	11110000	00000000	00101111

INSTRUCTION Skip the following instruction if the accumulator bit specified by the 4 LSBs of this instruction is set.

MNEMONIC SBS

FORMAT



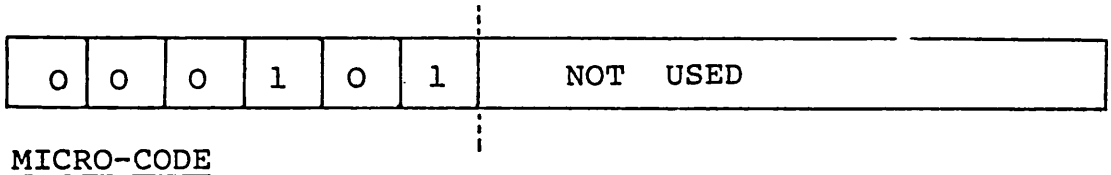
MICRO-CODE

209	LMI	FF1	EMM	JCR6	00100000	11110000	01010011	00110110
214	ANMA		EMM	JCR5	10010110	00000000	01010000	00110101
213	NOP		JFL13		11000000	11110000	00000000	01001101
210	ILR9		CL	LD	00010010	11111000	00000000	10000000
211	LMI	FF1	JCR4		00100000	11110000	00000011	00110100
212	ILR9		JZR15		00010010	11110000	00000000	00101111

INSTRUCTION Skip the following instruction if the converter data is positive i.e. sign bit = 0.

MNEMONIC SPD

FORMAT



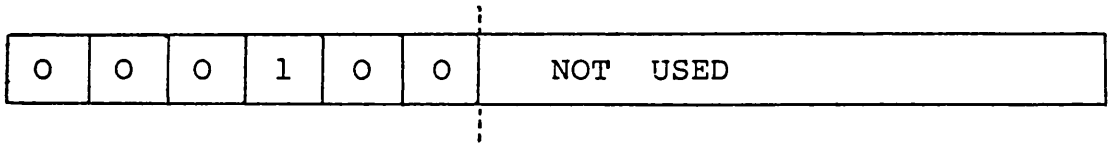
MICRO-CODE

232	LMI FF1 JCR13	00100000	11110000	00000011	00111101
237	TZAA K1101 JCC13	10111110	11010000	00000000	00001101
221	NOP JFL13	11000000	11110000	00000000	01001101
218	LMI FF1 JCR12	00100000	11110000	00000011	00111100
219	ILR9 CL LD	00010010	11111000	00000000	10000000
220	ILR9 JZR15	00010010	11110000	00000000	00101111

INSTRUCTION Skip the following instruction if the converter data is negative i.e. sign bit = 1.

MNEMONIC SND

FORMAT



MICRO-CODE

233	LMI FF1 JCR14	00100000	11110000	00000011	00111110
238	TZAA K1101 JCR15	10111110	11010000	00000000	00111111
239	NOP JFL14	11000000	11110000	00000000	01001110
234	ILR9 CL LD	00010010	11110000	00000000	10000000
235	LMI FF1 JCR12	00010000	11110000	00000011	00111100
236	ILR9 JZR15	00010010	11110000	00000000	00101111

INSTRUCTION Skip the following instruction if the contents of the accumulator are negative.

MNEMONIC S N A

FORMAT

0	0	0	1	1	1	NOT USED

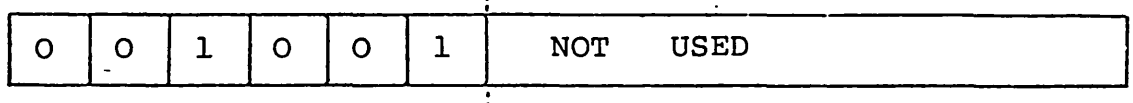
MICRO-CODE

224	LMI	FF1	JCR7	00100000	11110000	00000011	00110111
231	TZAA	KO111	JCR15	10111110	01110000	00000000	00111111
239	NOP	JFL14		11000000	11110000	00000000	01001110
234	ILR9	CL	LD	00010010	11111000	00000000	10000000
235	LMI	FF1	JCR12	00100000	11110000	00000011	00111100
236	ILR9	JZR15		00010010	11110000	00000000	00101111

INSTRUCTION Skip the following instruction if the contents of the accumulator are zero

MNEMONIC SZA

FORMAT



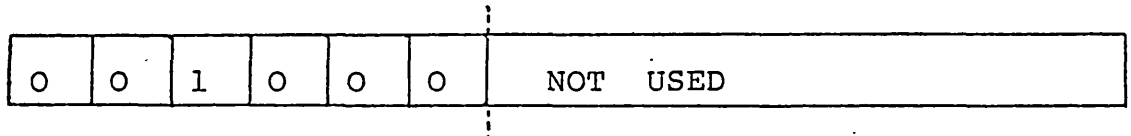
MICRO-CODE

```
216  LMI   FF1   JCR15   00100000  11110000  00000011  00111111
223  TZAA        JCR13   10111110  00000000  00000000  00111101
221  NOP         JFL13   11000000  11110000  00000000  01001101
218  LMI   FF1   JCR12   00100000  11110000  00000011  00111100
219  ILR9  CL    LD      00010010  11111000  00000000  10000000
220  ILR9        JZR15   00010010  11110000  00000000  00101111
```

INSTRUCTION Skip the following instruction if the contents of the accumulator are positive

MNEMONIC SPA

FORMAT



MICRO-CODE

```
217  LMI   FF1   JCR14        00100000  11110000  00000011  00111110
222  TZAA  KO111 JCR13        10111110  01110000  00000000  00111101
221  NOP   JFL13              11000000  11110000  00000000  01001101
218  LMI   FF1   JCR12        00100000  11110000  00000011  00111100
219  ILR9  CL    LD           00010010  11111000  00000000  10000000
220  ILR   JZR15              00010010  11110000  00000000  00101111
```

A3.2 THE EXTENDED INSTRUCTION SET

INSTRUCTION — Multiply the contents of the accumulator by the contents of the data/constant store location specified. The signed 32 bit product is in Accumulator (MSB's) and Register T (LSB's).

MNEMONIC — MUL

FORMAT

1	0	0	0	1	1	SUB ADDRESS

MICRO-CODE

```
112    TZAA   KO111   JCC16
256    ILR9   REN     JFLO
259    CIA A FF1  REN JCR2
258    SDRT   FF1  REN JCR1
257    LTMA KO111  REN  JCC19
305    ACMA   REN  JFL3
307    SDR2   FF1  JCR7
311    CIAA   FF1  EDB  JCR4
308    NOP  EDB  WEN  JCR5
309    NOP  EDB  WEN  JCRO
306    SDR2   FF1  JCRO
304    CSRA   JCR6
310    ALRA   JCC16
262    ALRA   JCR5
261    ALRA   JCR4
260    ALRA   FF1  JCR7
263    SDR1   FF1  EDB  JCR8
264    CLAA   STZ  JCR9
265    SRAT   REN  HCZ  JCR1O
```

MUL (Contd.)

```
266    INR1  FF1  REN  STC  JFL 3
315    AMAA  REN  HCZ  JCR10
314    SRAA   REN  STZ JCR9
313    SRAT  FFZ  REN  HCZ  JCFO
267    SRAA  STZ  JCR12
268    SRAT  FFZ  HCZ  JCR13
269    SDR6  FF1  EDB  JCR14
270    ILR2  EDB  JCR15
271    NOP  EDB  WEN  JCC23
383    LMI  FF1  EDB  WEN  JCR14
382    ALR9  KO111 EDB  JCR13
381    TZAA  KO111  EDB  JCR12
380    ILR6  EDB  JFL5
347    CIAT  FF1  STZ  JCR12
348    CIAA  FFZ  EDB  JCR10
346    SDR9  FF1  CL  LD
```

ROM CONTENTS.

112	10111110	01110000	00000000	00010000
256	00010010	11110000	00110000	01000000
259	00111110	11110000	00110011	00110010
258	01011000	00000000	00110011	00110001
257	10110110	01110000	00110000	00010011
305	00010110	11110000	00110000	01000011
307	01000100	00000000	00000011	00110111
311	00111110	11110000	01000011	00110100
308	11000000	11110000	11000000	00110101
309	11000000	11110000	11000000	00110000
306	01000100	00000000	00000011	00110000

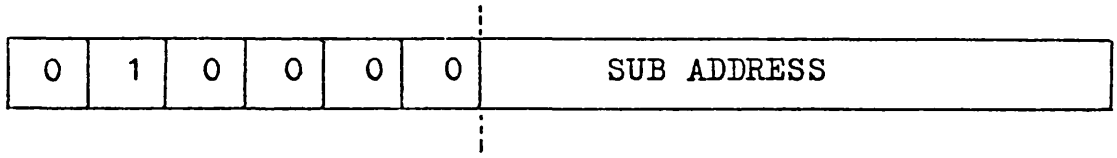
ROM CONTENTS (Contd.)

304	01011010	11110000	00000000	00110110
310	00011010	00000000	00000000	00010000
262	00011010	00000000	00000000	00110101
261	00011010	00000000	00000000	00110100
260	00011010	00000000	00000011	00110111
263	01000010	00000000	01000011	00111000
264	10010110	11110000	00001000	00111001
265	00011100	11110000	00111100	00111010
266	01100010	11110000	00110111	01000011
315	00010110	00000000	00111100	00111010
314	00011110	11110000	00111000	00111001
313	00011100	11110000	00111101	01010000
267	00011110	11110000	00001000	00111100
268	00011100	11110000	00001101	00111101
269	01001100	00000000	01000011	00111110
270	00000100	11110000	01000000	00111111
271	11000000	11110000	11000000	00010111
383	00100000	11110000	11000011	00111110
382	00010010	01110000	01000000	00111101
381	10111110	01110000	01000000	00111100
380	00001100	11110000	01000000	01000101
347	00111100	11110000	00001011	00111100
348	00111110	11110000	01000001	00111010
346	01010010	00001000	00000011	10000000

INSTRUCTION Load R7 from the data store as specified by the sub address(i.e.load the return address)

MNEMONIC LRA

FORMAT



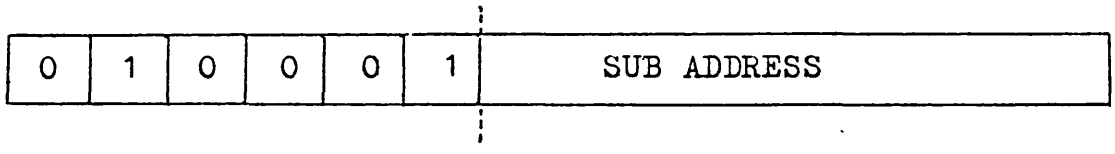
MICRO-CODE

185	LMI FF1 REN JCC25	00100000	11110000	00110011	00011001
409	NOP REN JCR10	11000000	11110000	00110000	00111010
410	LMFA REN JCR11	11010110	11110000	00110000	00111011
411	SDR7 FF1 JZR13	01001110	00000000	00000011	00101101

INSTRUCTION Store R7 (i.e. the return address of the S/R), in the data store location as specified by the sub address.

MNEMONIC SRA

FORMAT



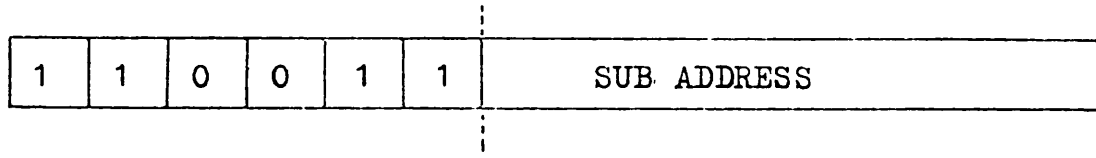
MICRO-CODE

184	LMI FF1 JCC25	00100000	11110000	00000011	00011001
408	ILR7 EDB JCR15	00001110	11110000	01000000	00111111
415	NOP EDB WEN JCR14	11000000	11110000	11000000	00111110
414	NOP EDB WEN JZR13	11000000	11110000	11000000	00101101

INSTRUCTION Load Reg. T from the data/constant store as specified by the sub address.

MNEMONIC LTR

FORMAT



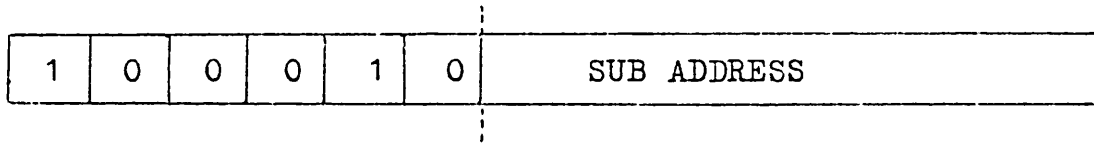
MICRO-CODE

```
 48  LMI FF1 REN JCC22 00100000  11110000  00110011  00010110
352  NOP REN JCR7      11000000  11110000  00110000  00110111
359  LMFT REN JZR14    11010100  11110000  00110000  00101110
```

INSTRUCTION Store Reg. T in the data store location as specified by the sub address.

MNEMONIC STT

FORMAT



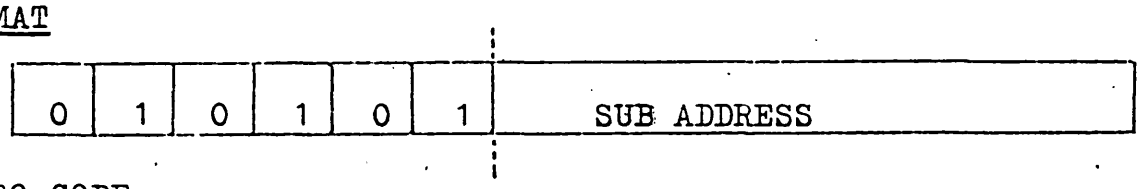
MICRO-CODE

```
113  LMI FF1 JCC18     00100000  11110000  00000011  00010010
289  ILRT EDB JCR2     00011000  11110000  01000000  00110010
290  NOP EDB WEN JCR3  11000000  11110000  11000000  00110011
291  NOP EDB WEN JZR13 11000000  11110000  11000000  00101101
```

INSTRUCTION Load R2,R3 and AC with three consecutive data words from the data store. The sub-address specifies the address of the first word.

MNEMONIC LMB

FORMAT



MICRO-CODE

168	NOP	REN	JCC23		
376	NOP	REN	JCR11		
379	LMFA	REN	COUL	JCR0	
368	SDR2	FF1	INC	COUL	JCR1
369	NOP	REN	COUL	JCR2	
370	NOP	REN	COUL	JCR3	
371	LMFA	REN	COUL	JCR4	
372	SDR3	FF1	INC	COUL	JCR5
373	LMI	FF1	REN	COUL	JCR6
374	NOP	REN	COUL	JCR7	
375	LMFA	REN	COUL	JZR14	

ROM CONTENTS.

168	11000000	11110000	00110000	00010111
376	11000000	11110000	00110000	00111011
379	11010110	11110001	00110000	00110000
368	01000101	00000001	00000011	00110001
369	11000000	11110001	00110000	00110010
370	11000000	11110001	00110000	00110011
371	11010110	11110001	00110000	00110100
372	01000111	00000001	00000011	00110101

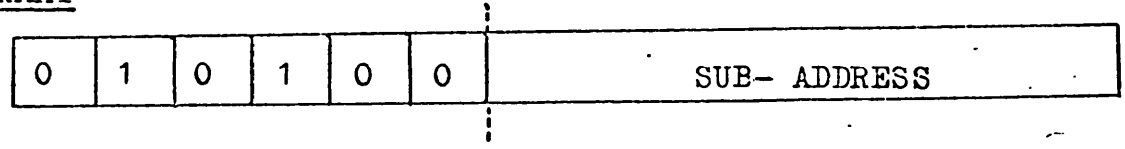
LMB (Contd.)

373	00100000	11110001	00110011	00110110
374	11000000	11110001	00110000	00110111
375	11010110	11110001	00110000	00101110

INSTRUCTION Store R2,R3 and AC in three consecutive locations in the data store. The subaddress specifies the address where the first word has to be stored.

MNEMONIC SMB

FORMAT



MICRO- CODE

169	ILR2	JCC23			
377	NOP	EDB	WEN	JCR10	
378	NOP	EDB	WEN	COUL	JCC24
393	ILR3	INC	COUL	JCR0	
384	NOP	EDB	WEN	COUL	JCR1
385	LMI	FF1	EDB	WEN	COUL JCR2

SMB (contd.)

386	ILR9	INC	COUL	JCR3	
387	NOP	EDB	WEN	COUL	JCR4
388	NOP	EDB	WEN	COUL	JZR14

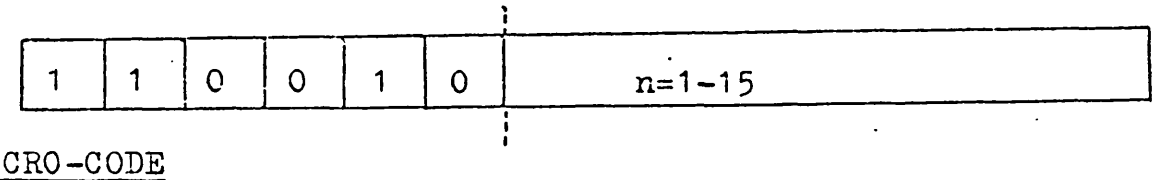
ROM CONTENTS

169	00000100	11110000	00000000	00010111
377	11000000	11110000	11000000	00111010
378	11000000	11110001	11000000	00011000
393	00000111	11110001	00000000	00110000
384	11000000	11110001	11000000	00110001
385	00100000	11110001	11000011	00110010
386	00010011	11110001	00000000	00110011
387	11000000	11110001	11000000	00110100
388	11000000	11110001	11000000	00101110

INSTRUCTION Shift the contents of the 32-bit word contained in AC, T=MSB, LSB, right n times, where n is specified by the 4 least significant bits of the address field. The final result is in AC,T with extended sign.

MNEMONIC DMR

FORMAT



MICRO-CODE

49	SDR6	FF1	JCC26	
417	LDMA	JMPE	JCR15	
431	SDR5	FF1	JCR14	
430	ILR6	JCR13		
429	TZR6	KO111	STC	JCR12

DMR (contd.)

428	NOP	HCZ	JFL10	
427	SRAA	FF1	STZ	JCR8
426	SRAA	STZ	JCR8	
424	TZR5	HCZ	JCR9	
425	SRAT	FFZ	HCZ	JFL11
442	LMI	FF1	JCR7	
439	NOP	JZR15		
443	DSM5	HCZ	JCF2	

ROM CONTENTS

49	01001100	00000000	00000011	00011010
417	00110110	00000000	00100000	00111111
431	01001010	00000000	00000011	00111110
430	00001100	11110000	00000000	00111101
429	10101100	01110000	00000100	00111100
428	11000000	11110000	00001100	01001010
427	00011110	11110000	00001011	00111000
426	00011110	11110000	00001000	00111000
424	10101010	00000000	00001100	00111001
425	00011100	11110000	00001101	01001011
442	00100000	11110000	00000011	00110111
439	11000000	11110000	00000000	00101111
443	00101010	00000000	00001100	01010010

INSTRUCTION Store in the data store n words from the I/P port, starting from the address specified by the subaddress field. (The number of the words is specified by a LDA instruction which proceedes IDB in the program).

MNEMONIC IDB

FORMAT

1	0	0	0	0	1	SUB- ADDRESS

MICRO- CODE

120 NOP IPE JCC20

328 DCAA IPE WEN COUL JCR7

327 TZAA IPE WEN COUL JCR6

326 NOP LD INC COUL JFL5

338 LMI FF1 JCR1

339 NOP COUL JCR8

344 NOP IPE COUL JCC20

337 NOP JZR15

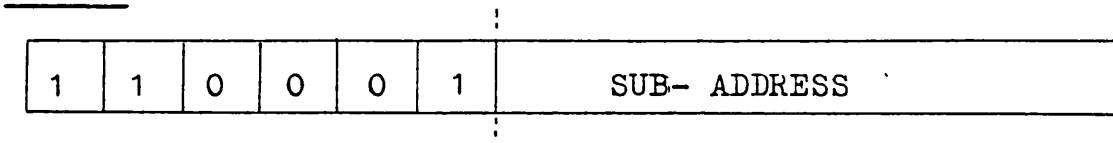
ROM CONTENTS

120	11000000	11110000	00010000	00010100
328	00111110	00000001	10010000	00110111
327	10111110	00000001	10010000	00110110
326	11000001	11110001	00000000	11000101
338	00100000	11110000	00000011	00110001
339	11000000	11110001	00000000	00111000
344	11000000	11110001	00010000	00010100
337	11000000	11110000	00000000	00101111

INSTRUCTION Add (2's complement) a 32-bit data word stored in two consecutive locations in the data store (the subaddress specifies the least significant 16-bits) to the contents of a similar size word contained in AC and T. The result is stored back as a 32-bit word in the 2 consecutive locations specified by the subaddress.

MNEMONIC DPA

FORMAT



MICRO- CODE

56	NOP	REN	JCC28			
456	ILRT	REN	JCR10			
458	LMFT	REN	JCR11			
459	ALRT	STZ	JCR12			
460	NOP	EDB	WEN	HCZ	JCR13	
461	NOP	EDB	WEN	HCZ	COUL	JCR14
462	NOP	INC	HCZ	COUL	JCR15	
463	NOP	REN	HCZ	COUL	JCR2	
450	LMI	FF1	REN	HCZ	COUL	JCR3
451	LMFA	REN	HCZ	COUL	JCR4	
452	ALR9	FFZ	COUL	JCR5		
453	NOP	EDB	WEN	COUL	JCR6	
454	NOP	EDB	WEN	COUL	JZR14	

ROM CONTENTS

56	11000000	11110000	00110000	00011100
456	00011000	11110000	00110000	00111010
458	11010100	11110000	00110000	00111011
459	00011000	00000000	00001000	00111100
460	11000000	11110000	11001100	00111101
461	11000000	11110001	11001100	00111110

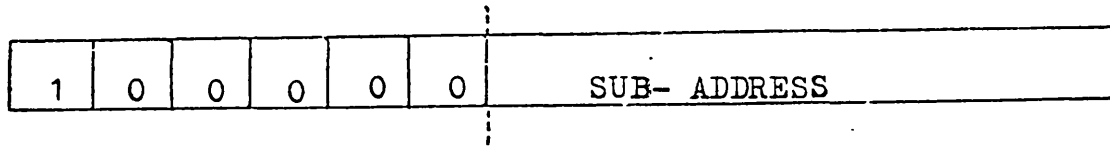
DPA (contd.)

462	11000001	11110001	00001100	00111111
463	11000000	11110001	00111100	00110010
450	00100000	11110001	00111111	00110011
451	11010110	11110001	00111100	00110100
452	00010010	00000001	00000001	00110101
453	11000000	11110001	11000000	00110110
454	11000000	11110001	11000000	00101110

INSTRUCTION — Subtract a 32-bit word stored in two consecutive locations in the data store(the subaddress specifies the least significant 16--bits) from the contents of a similar size word contained in AC and T. The result is stored back as a 32-bit word in the two consecutive locations specified by the subaddress.

MNEMONIC — DPS

FORMAT



MICRO- CODE

121	NOP	REN	JCC22			
361	ILRT	REN	JCR10			
362	LCMT	REN	JCR11			
363	ALRT	FF1	STZ	JCR12		
364	NOP	EDB	WEN	HCZ	JCR13	
365	NOP	EDB	WEN	HCZ	COUL	JCR14

DPS (contd.)

366	NOP	HCZ	COUL	INC	JCR15	
367	NOP	REN	HCZ	COUL	JCR2	
354	LMI	FF1	REN	HCZ	COUL	JCR3
355	LCMA	REN	HCZ	COUL	JCR4	
356	ALR9	FFZ	COUL	JCR5		
357	NOP	EDB	WEN	COUL	JCR6	
358	NOP	EDB	WEN	COUL	JZR14	

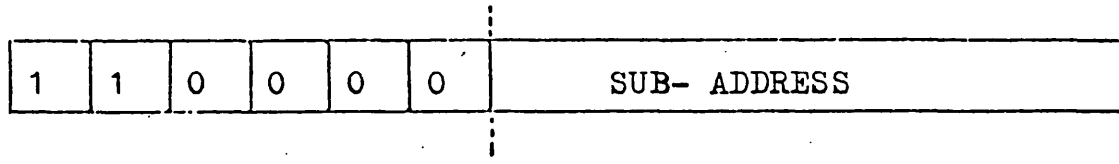
ROM CONTENTS

121	11000000	11110000	00110000	00010110
361	00011000	11110000	00110000	00111010
362	11110100	11110000	00110000	00111011
363	00011000	00000000	00001011	00111100
364	11000000	11110000	11001100	00111101
365	11000000	11110001	11001100	00111110
366	11000001	11110001	00001100	00111111
367	11000000	11110001	00111100	00110010
354	00100000	11110001	00111111	00110011
355	11110110	11110001	00111100	00110100
356	00010010	00000001	00000001	00110101
357	11000000	11110001	11000000	00110110
358	11000000	11110001	11000000	00101110

INSTRUCTION Multiply the AC by a positive fractional constant of the constant store as specified (The number of bits after the binary point is stored in T). The result is scaled to the nearest integer and stored to AC.

MNEMONIC FMU

FORMAT



MICRO- CODE

57	ILRT	EDB	JCC29		
434	NOP	JCR4			
435	INRA	JCR4			
436	NOP	JZR14			
466	INR1	FF1	REN	STC	JFL14
467	TZRT	KO111	JCR4		
468	LMI	FF1	JFL11		
473	SDR1	FF1	JCR12		
474	SRAT	REN	HCZ	JCC30	
475	SRAT	REN	HCZ	JCR2	
476	ILR9	REN	JCR13		
477	SDRT	FF1	REN	JCR14	
478	LTMA	KO111	REN	JCR15	
479	CLAA	REN	JFL13		
481	SRAT	FFZ	HCZ	REN	JCF5
482	SRAA	FF1	STZ	REN	JCR1
483	AMAA	REN	HCZ	JCR2	
484	LMI	FF1	JFL11		
490	INR1	FF1	REN	STC	JFL15
491	TZRT	KO111	JCR4		

FMU (contd.)

505	SRAT	FFZ	HCZ	REN	JCF6
506	SRAA	STZ	REN	JCR9	
507	AMAA	REN	HCZ	JCR10	

ROM CONTENTS

57	00011000	11110000	01000000	00011101
434	11000000	11110000	00000000	00110100
435	01111010	11110000	00000011	00110100
436	11000000	11110000	00000000	00101110
466	01100010	11110000	00110111	01001110
467	10111000	01110000	00000000	00110100
468	00100000	11110000	00000011	01001011
473	01000010	00000000	00000011	00111100
474	00011100	11110000	00111100	00011110
475	00011100	11110000	00111100	00110010
476	00010010	11110000	00110000	00111101
477	01011000	00000000	00110011	00111110
478	10110110	01110000	00110000	00111111
479	10011010	11110000	00110000	01001101
481	00011100	11110000	00111101	01010101
482	00011110	11110000	00111011	00110001
483	00010110	00000000	00111100	00110010
484	00100000	11110000	00000011	01001011
490	01100010	11110000	00110111	01001111
491	10111000	01110000	00000000	00110100
505	00011100	11110000	00111101	01010110
506	00011110	11110000	00111000	00111001
507	00010110	00000000	00111100	00111010

APPENDIX 4

OFF-LINE SUPPORT

A4.1 Software support

The first cross- assembler written, produces the binary code for the 32- bit microword. Fig. A4.1 shows the different fields, as have been defined in table 3.2. The user has to type the required mnemonic for each field, but in a case of a field defined by default, a carriage return is typed. When all the program has been typed, then a tape is punched with the data for the micromemory. After that, the listings of these data can be obtained in the format shown in fig. A4.2.
For corrections, modifications or extension of the micro- program, the binary tape is loaded into the computer, and the same process is repeated to produce the new program.

The second cross- assembler in principle works at the same way as the previous one, but with a change in the symbol table and some additional support.
Fig. A4.3 shows the listings provided by the cross-assembler. Because the EPROM programmer is driven by the computer, the program is arranged such that to transfer directly the produced binary code into the EPROMs.

```
MICROIN CPU*******
LOC     000
FUNCTION BUS    CLR
REGISTER        ZERO
INC COUNTERS
KBUS
CLOCK LATCH
LOAD COUNTERS
WR CONTROL
DATA BUS
FLAG IP CON
FLAG OP CON
LOAD
MCU ADDR CON    JZR 006
```

Fig. A4.1 The fields for the microinstruction in the corresponding cross- assembler

```
COMMAND ? LIST
NO OF ROM 1
00  00  000  000000000     10000000
00  06  006  000000110     00100000
00  07  007  000000111     10010110
NO OF ROM 2
00  00  000  000000000     11110000
00  06  006  000000110     11110000
00  07  007  000000111     11110000
NO OF ROM 3
00  00  000  000000000     00000000
00  06  006  000000110     00000011
00  07  007  000000111     00000000
NO OF ROM 4
00  00  000  000000000     00100110
00  06  006  000000110     00100111
00  07  007  000000111     00101111
(a) (b) (c)    (d)          (e)
```

ROM1: Bits 31-24
ROM2: Bits 23-17
ROM3: Bits 16- 8
ROM4: Bits 7-0
(a): Number of row
(b): Number of column
(c): Decimal address
(d): Binary address
(e): Contents

Fig. A4.2 The micromemory contents generated by the cross- assembler

(a)	(b)		(c)	(d)	(e)
000000	JLP	000550	034550	000071	000150
000550	LDA	000571	136571	000275	000171
000551	STA	000377	134377	000270	000377
000552	LDL	000002	110002	000220	000002
000553	STA	000000	134000	000270	000000
000554	DSZ	000000	122000	000244	000000
000555	JLP	000554	034554	000071	000154
000556	CSL		056000	000134	000000
000557	JLP	000553	034553	000071	000153
000560	LDA	000572	136572	000275	000172
000561	STA	000377	134377	000270	000377
000562	JLP	000550	034550	000071	000150
COMMAND?					

Fig. A4.3 Output listings provided by the cross--assembler for the application program.

a): Address

b): Mnemonic of the instruction

c): Binary code of the 16-bit word

d): Contents of the ROM1 i. e. 8 most significant bits

e): Contents of the ROM2 i. e. 8 least significant bits.

Note: All numbers are in octal

Additional facilities are:

a) Reading of the data contained in the EPROM.

b) Verification of the EPROM data, with those contained in the minicomputer.

c) Copy of the EPROM data, into the minicomputer

d) If few instructions have to be changed, it is easier to type them in a binary form, than to go through the assembler, therefore this facility is provided.

e) Other commands provide deleting and interleaving data locations and moving data blocks in other locations.

A4.2 PROM programmers

The programmer for the bipolar PROMS is operated manually through switches. The operator has to select some switches to define the type of the PROM used, then selects the address and the data to be programmed there and finally presses the clear and start push buttons. When the programming procedure has finished, the interrupt light comes on. The above operation is then repeated for the remaining locations to be programmed. A block diagram of this programmer is shown in fig. A4.4.

The specified address and data are latched,

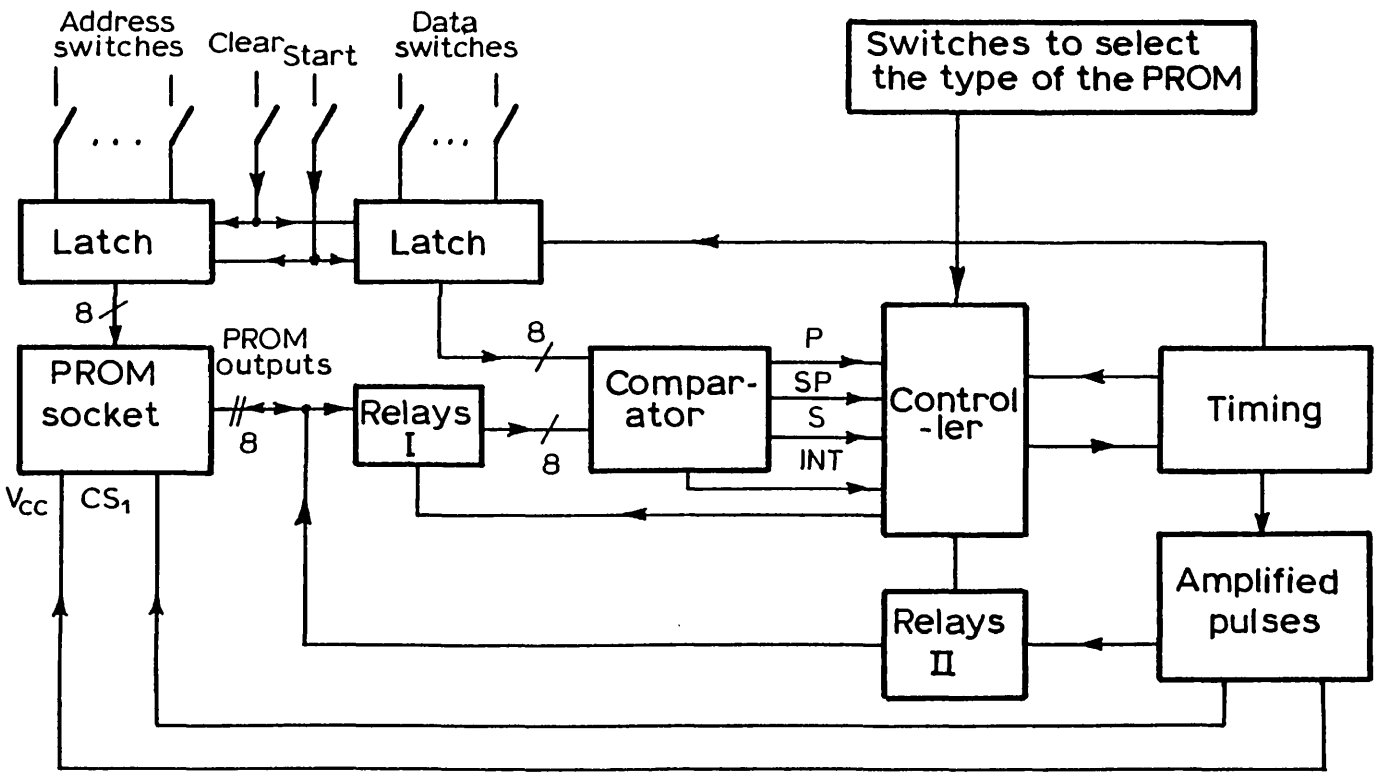


Fig. A4·4 The block diagram for the bipolar PROM programmer

then the relays (I) are closed to compare the contents of the PROM with the data entered through the switches. The four possible states of the comparator are:

a) P corresponds to programming

b) SP means that programming is not necessary

c) The bipolar PROMs are of the fusible link type, therefore an already programmed bit cannot change back.To inform the user of such operation, signal S comes on.

d) INT signals the end of programming.

These signals together with some others which define the type of the PROM, are decoded by the controller, such that the right timing pulses are generated. These are amplified accordingly, relays(I) open, while Relays (II) close, and the programming of one bit at a time occurs.

The types of PROMs which can be programmed are:

a) Texas Instruments 74188, 74S287, 74S471, 74S472[31].

b) Intel 3601[43].

c) National DM 7573/DM 8573[44].

d) Signetics 82S123[45].

The EPROM programmer is driven by the computer, therefore its control pulses are defined by software.

The only hardware needed is to generate the amplified pulses.

A4.3 PROM simulators

The necessity for the PROM simulators has been discussed in chapter 3. Fig. A4.5 shows the block diagram of the EPROM simulator driven from the NOVA 3. The RAMs can be addressed either by the NOVA(load mode) of by the processor (read mode). In the load mode the data are fed from the NOVA to a buffer and a timing circuit generates the write pulses. The address is controlled by a counter. In the read mode, the processor supplies the address to the simulator and the data then are fed back to the processor.

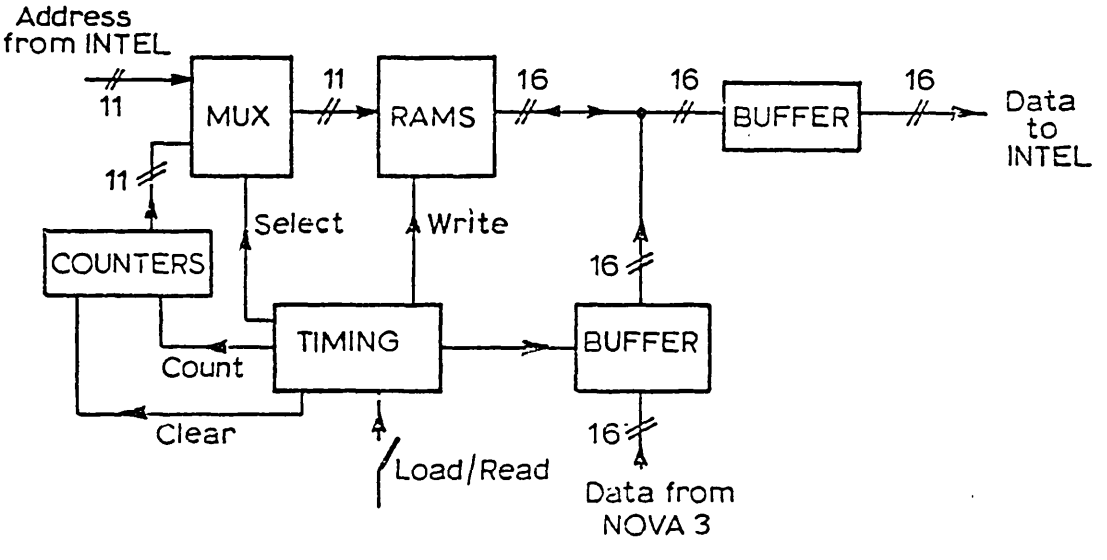


Fig. A4.5 The block diagram for the EPROM simulator

APPENDIX 5

THE TEST RIG

A5.1 The transmission line model

The digital relay performance has been tested by using the rig described in reference 77.A schematic diagram is given in fig. A5.1. Variable source and line impedances are provided. Because of unbalances in these impedances, only the value of Z_S=20 Ω has been used. By connecting the fault link in different phases and at different positions, the relay performance under different fault conditions has been tested.

The c.t.s used are of the bar- primary design with 400/1 secondaries. The class of these c.t.s is 15S10 and have 1.52Ω secondary winding resistance. As the maximum current in the model is about 60 A, the primary contains 20 turns, to give a more accurate measurement. To avoid high voltage occuring in the secondary, when it is accidentally open- circuited, while the primary is still energised, a low burden of 0.5Ω has been applied. At the same time, as the secondary output of the c.t. feeds the high impedance input of the analogue filter operational amplifier, a transformation of the current to voltage is achieved.

The v.t.'s used have a ratio of 240/24 and maximum burden 25 VA. A voltage divider is necessary

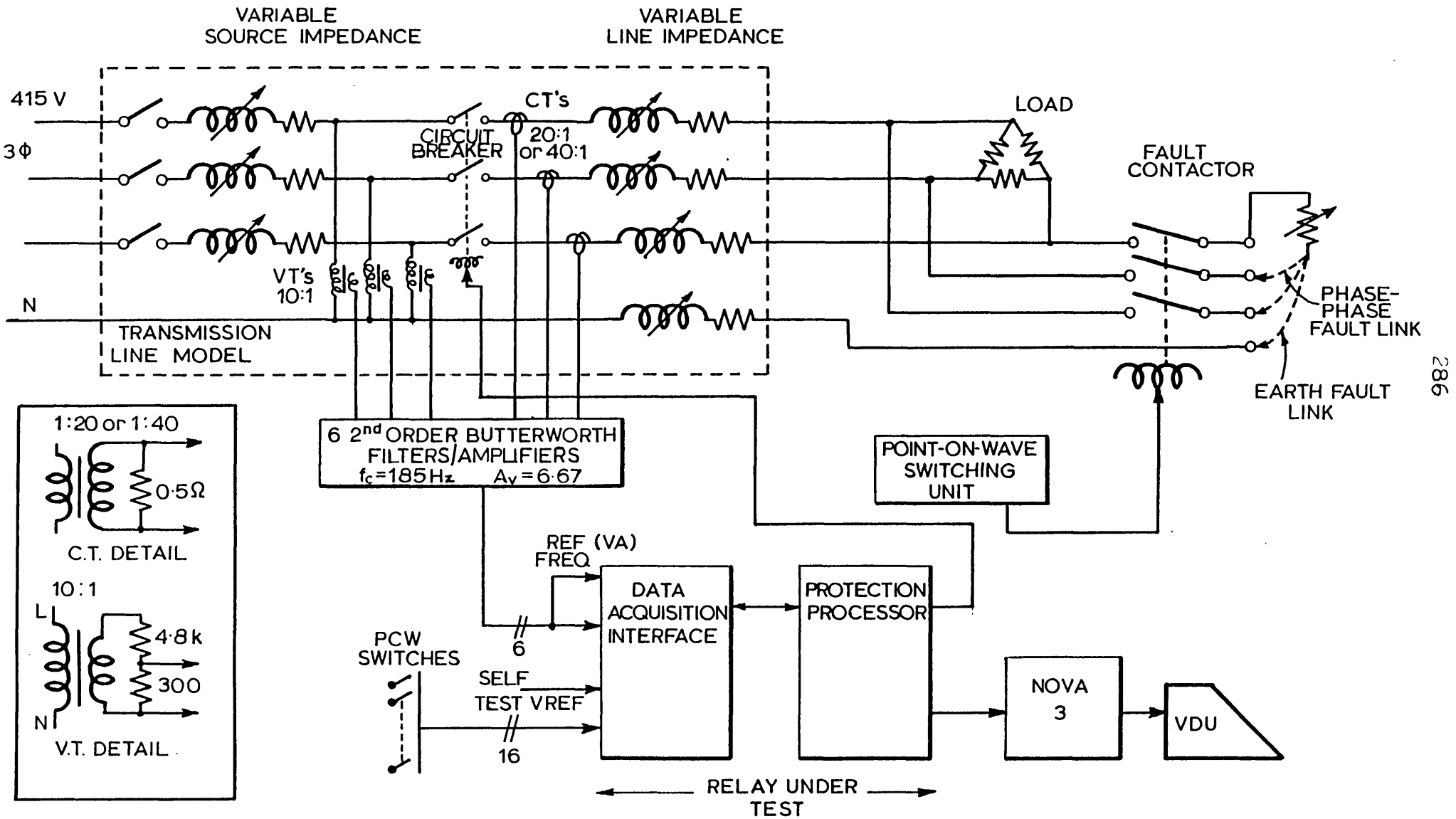


Fig. A 5·1 The distance relay test rig

in the secondary of the v.t., such that the maximum signal fed to the filters is approximately ± 10 V.

A5.2 Filter and amplifier design

Fig. A5.2 gives the circuit details for the antialiasing analogue filters and the corresponding amplifiers. The filter design has been discussed in chapter 4.

The amplification has been selected such that for the maximum possible values in the primary network, saturation does not occur in the signals fed to the data acquisition unit.

Offset and gain adjustments are provided. By taking into account all the intermediate attenuating factors between the primary network quantities and the outputs of the filter/amplifier it has been found that for the system used the voltage attenuation is 82.87 while the current is 6.05. Small variations of negligish effect have been found due to unbalances in the system and inaccuracies in the transformers. Such errors correspond to a maximum error of 2 lsbits in the A/D.

A5.3 The rig- relay connections

In fig. A5.1, the way the dedicated relay is connected to the filters/amplifiers is shown. NOVA 3 is the monitoring minicomputer used, connected to a VDU .

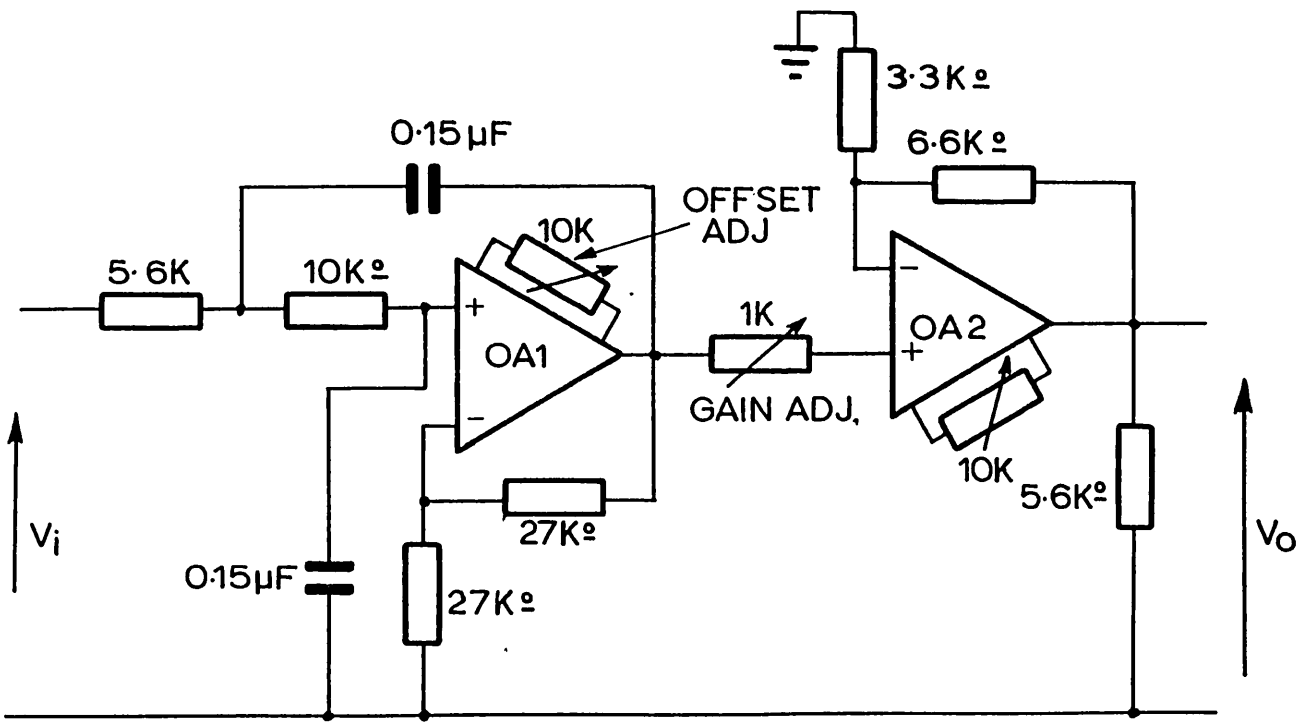


Fig. A5·2 2nd order Butterworth low pass filter and amplifier

APPENDIX 6

THE PROGRAM LISTINGS

Appendix 6.1 refers to the low page i.e. the first 1K locations for the sample and midpoint formula.

In appendix 6.2 the listings for the high page (common to both methods) are given.

Because the software has been kept modular, the low page for the midpoints method is the same, except that part of the program which manipulates the data such that the quantities VA, CA, DCA, VB, CB and DCB to be derived. Therefore the empty or missing locations in appendix 6.3 are the same as the corresponding ones for the sample and midpoint formula.

Appendices 6.4, 6.5 and 6.6 present the contents of the data and constant store.

A6.1 LOW PAGE (THE SAMPLE AND MIDPOINT FORMULA)

```
000  JLP   16      033  JLP 1760      066  LDA   12
001  LDA  572      034  STA   33      067  STA  106
002  STA  377      035  JLP  532      070  JSR 1062
003  DZM  423      036                 071  LDA   12
004  DZM  426      037  WFS           072  STA  107
005  LDA  543      040  JSR  477      073  JSR 1102
006  STA  140      041  LDA  415      074  LDA   12
007  STA  136      042  SBC   15      075  STA  110
010  STA  137      043  JSR 1677      076  JSR 1120
011  LDA  542      044  JSR  532      077  JSR 1160
012  STA  100      045  JSR 1013      100  LDA   12
013  STA  101      046  JSR 1044      101  STA  111
014  STA  102      047  JSR 1062      102  JSR 1176
015  JHP 1703      050  JSR 1102      103  LDA   12
016  WFS           051  JSR 1120      104  STA  112
017  JSR  477      052  JSR 1160      105  JSR 1220
020  LDA  415      053  JSR 1176      106  LDA   12
021  STA   73      054  JSR 1220      107  STA  113
022  WFS           055  JLP   56      110  JLP  142
023  JSR  477      056  WFS           111  LDA  104
024  LDA  415      057  JSR  477      112  STA  414
025  SBS   17      060  LDA  415      113  LDA  157
026  JLP   22      061  SBC   15      114  JSR 1263
027  LDA  415      062  JSR 1677      115  JLP 1442
030  MSL    2      063  JSR  465      116  JLP 1451
031  MSR    3      064  JSR 1013      117  STA  104
032  STA   56      065  JSR 1044      120  JSR 1176
```

```
121  JSR 1243
122  LDA  112
123  JSR 1152
124  STA  112
125  LDA  410
126  STA  275
127  LDA  411
130  STA  276
131  JSR 1571
132  JSR 1571
133  JHP   50
134  DZM   52
135  LDA  415
136  JLP  157
137  SZA
140  JLP  164
141  JLP  207
142  JHP  415
143
144  DZM   22
145  JLP  146
146  WFS
147  JSR  405
150  DZM   34
151  JSR  410
152  SBC   15
153  JSR 1677
154  JSR 1013
155  JSR 1120
156  JLP  134
157  SBS   16
160  JLP  207
161  LDA   33
162  MSL    3
163  JLP  653
164  LDA  415
165  SBC   16
166  JLP  677
167  SBS   14
170  JLP  174
171  LDA    0
172  STA 1177
173  JLP  745
174  SBC    1
175  JLP  207
176  SBC    2
177  JLP  243
200  SBC    3
201  JLP  307
202  SBC    4
203  JLP  340
204  SBC    5
205  JLP  111
206  JLP  455
207  LDA  100
210  STA  414
211  LDA    0
212  JSR 1263
213  JLP 1364
214  JLP 1372
215  STA  100
216  JSR 1044
217  JSR 1243
220  LDA  106
221  JSR 1152
222  STA  106
223  LDA  400
224  STA  275
225  LDA  401
226  STA  276
227  JSR  661
230  JSR 1561
231  JHP   12
232  LDA  275
233  STA  400
234  LDA  276
235  STA  401
236  LDA    0
237  STA   65
240  LDA  167
241  STA   66
242  JSR  517
243  LDA  101
244  STA  414
245  LDA    1
246  JSR 1263
247  JLP 1377
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250  JLP 1405
251  STA  101
252  JSR 1062
253  JSR 1243
254  LDA  107
255  JSR 1152
256  STA  107
257  LDA  402
260  STA  275
261  LDA  403
262  STA  276
263  JSR  661
264  JSR 1563
265  JHP   20
266  LDA  275
267  STA  402
270  LDA  273
271  STA  403
272  LDA  415
273  SBC   13
274  JLP  751
275  SBS   14
276  JLP  302
277  LDA    1
300  STA 1177
301  JLP  307
302  LDA    1
303  STA   65
304  LDA  117
305  STA   66
306  JSR  517
307  LDA  102
310  STA  114
311  LDA    2
312  JSR 1263
313  JLP 1412
314  JLP 1420
315  STA  102
316  JSR 1102
317  JSR 1243
320  LDA  110
321  JSR 1152
322  STA  110
323  LDA  404
324  STA  275
325  LDA  405
326  STA  276
327  JSR  661
330  JSR 1565
331  JHP   35
332  LDA    2
333  STA   65
334  LDA  171
335  STA   66
336  JSR  517
337  JLP  666
340  LDA  103
341  STA  414
342  LDA  156
343  JSR 1263
344  JLP 1425
345  JLP 1434
346  STA  103
347  JSR 1160
350  JSR 1243
351  LDA  111
352  JSR 1152
353  STA  111
354  LDA  406
355  STA  275
356  LDA  407
357  STA  276
360  JSR  577
361  JSR 1567
362  JHP  151
363  LDA  275
364  STA  406
365  LDA  276
366  STA  407
367  LDA  415
370  SBC   13
371  JLP  753
372  SBS   14
373  JLP  377
374  LDA    2
375  STA 1177
376  JLP  111
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377 LDA   3
400 STA   65
401 LDA   172
402 STA   66
403 JSR   570
404 JLP   111
405 CLA
406 STA   23
407 JLP   477
410 JHP   176
411 JHP   430
412
413 LDA   275
414 STA   404
415 LDA   276
416 STA   405
417 JLP   332
420
421 LDA   546
422 SAD   151
423 JLP   437
424 ISZ   151
425 LDA   156
426 JSR   1004
427 LDA   157
430 JSR   1004
431 LDA   160
432 JSR   1004
433 ISZ   145
434 LDA   543
435 SAD   145
436 JHP   1441
437 LRA   420
440 LDA   415
441 RET
442 JHP   1044
443 DZM   436
444 LDA   275
445 STA   410
446 LDA   276
447 STA   411
450 LDA   4
451 STA   65
452 LDA   173
453 STA   66
454 JSR   470
455 LDA   105
456 STA   414
457 LDA   160
460 JSR   1263
461 JLP   1457
462 JLP   1466
463 STA   105
464 JLP   625
465 LDA   415
466 SBC   0
467 JLP   474
470 LDA   146
471 SZA
472 JLP   474
473 ISZ   147
474 LDA   415
475 AND   540
476 JLP   34
477 IDM   415
500 IDM   0
501 IDM   1
502 IDM   2
503 IDM   3
504 IDM   4
505 IDM   5
506 IDM   76
507 LDA   0
510 EXS
511 STA   0
512 LDA   1
513 EXS
514 STA   1
515 LDA   2
516 EXS
517 STA   2
520 LDA   3
521 EXS
522 STA   3
523 LDA   4
524 EXS
525 STA   4
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526 LDA    5
527 EXS
530 STA    5
531 RET
532 LDA  415
533 SBS   10
534 RET
535 LDA   76
536 EXS
537 STA   76
540 MSR    2
541 EXS
542 JHP  357
543 LDA  573
544 JSR  777
545 LDA   76
546 STA 1177
547 CLA
550 STA  377
551 WFS
552 IDM  415
553 IDM    0
554 IDM    0
555 IDM    0
556 IDM    0
557 IDM    0
560 IDM    0
561 IDM   76
562 LDA  415
563 SBC   10
564 JLP  551
565 JLP    1
566 ISZ   23
567 JHP  566
570 LDA   34
571 SZA
572 JHP  441
573 LDA   22
574 SZA
575 JLP 1100
576 LDA  262
577 SZA
600 RET
601 LDA  423
602 SZA
603 JLP  757
604 JHP 1771
605 JHP  401
606 JSR  777
607 LDA  415
610 SBC    0
611 JLP  617
612 LDA  146
613 SZA
614 JLP  617
615 LDA  571
616 JLP  726
617 CLA
620 JLP  726
621 LDA   65
622 JSR  777
623 LDA   66
624 JLP  726
625 JSR 1220
626 JSR 1243
627 LDA  113
630 JSR 1152
631 STA  113
632 LDA  412
633 STA  275
634 LDA  413
635 STA  276
636 JSR  566
637 JSR 1573
640 JHP    0
641 LDA  275
642 STA  412
643 LDA  276
644 STA  413
645 LDA    5
646 STA   65
647 LDA  174
650 STA   66
651 JSR  570
652 JHP 1113
653 STA   34
654 LDA  415
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655  LBS    0
656  ISZ  144
657  LDA   34
660  JLP  137
661  ISZ  123
662  LDA   57
663  SZA
664  JHP  566
665  JHP  636
666  ISZ   25
667  ISZ  437
670  JLP  340
671  JLP  340
672  LDA  145
673  SZA
674  DSZ  145
675  JLP  437
676  JLP  437
677  LDA    3
700  JLP  172
701  LDA  415
702  SBC   11
703  JLP  707
704  SBC   12
705  JLP  621
706  JLP  713
707  LDA   10
710  JSR  777
711  LDA   11
712  JLP  606
713  LDA  162
714  JSR  777
715  LDA  161
716  JSR  777
717  LDA  164
720  JSR  777
721  LDA  163
722  JSR  777
723  LDA  166
724  JSR  777
725  LDA  165
726  STA 1177
727  LDA  557
730  SUB  144
731  SNA
732  JLP  146
733  LDA  146
734  SZA
735  JLP  743
736  LDA  571
737  STA  377
740  LDA  146
741  INC
742  STA  146
743  DZM  144
744  JLP  146
745  CLA
746  INC
747  STA   52
750  JLP  207
751  LDA    4
752  JLP  300
753  LDA    5
754  JLP  375
755  LDA  546
756  STA 1177
757  LDA  146
760  INC
761  STA  146
762  STA   22
763  LDA   23
764  STA   32
765  LDA   25
766  STA   31
767  LDA  571
770  STA  377
771  DZM  265
772  DZM  266
773  JHP 1467
774
775
776  JLP 1000
777  STA 1177
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1000  LDL   67
1001  CSL
1002  JLP 1001
1003  RET
1004  SNA
1005  JLP 1007
1006  NEG
1007  SUB  542
1010  SNA
1011  JLP 1173
1012  RET
1013  LDA    3
1014  ADD    4
1015  ADD    5
1016  STA  152
1017  LTR  564
1020  LDA  570
1021  FMU  152
1022  STA  152
1023  MUL   67
1024  STT  416
1025  RET
1026  SPA
1027  NEG
1030  MSR    2
1031  SZA
1032  JLP  144
1033  RET
1034  LDA  146
1035  SZA
1036  JLP 1276
1037  LDA  571
1040  STA  377
1041  DZM  146
1042  ISZ  146
1043  JLP 1276
1044  LDA  122
1045  STA   14
1046  LDA  123
1047  STA   12
1050  LDA    0
1051  STA  122
1052  STA   10
1053  LDA    3
1054  ADD  416
1055  STA   11
1056  STA  123
1057  LDA  427
1060  STA  435
1061  RET
1062  LDA  124
1063  STA   14
1064  LDA  125
1065  STA   12
1066  LDA    1
1067  STA  124
1070  STA   10
1071  LDA    4
1072  ADD  416
1073  STA   11
1074  STA  125
1075  LDA  430
1076  STA  435
1077  RET
1100  LRA  267
1101  RET
1102  LDA  431
1103  STA  435
1104  LDA  126
1105  STA   14
1106  LDA  127
1107  STA   12
1110  LDA    2
1111  STA  126
1112  STA   10
1113  LDA    5
1114  ADD  416
1115  STA   11
1116  STA  127
1117  RET
1120  SRA  420
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1121  JLP  1124
1122  LDA   414
1123  JLP  1236
1124  LDA     2
1125  SUB     1
1126  STA   156
1127  LDA     0
1130  SUB     2
1131  STA   157
1132  LDA     1
1133  SUB     0
1134  STA   160
1135  LDA     5
1136  SUB     4
1137  STA   153
1140  LDA     3
1141  SUB     5
1142  STA   154
1143  LDA     4
1144  SUB     3
1145  JHP   155
1146  LDA    21
1147  SZA
1150  JLP  1452
1151  JLP  1475
1152  STA     7
1153  LDA    11
1154  SUB     7
1155  STA    13

1156  LDA    12
1157  RET
1160  LDA   130
1161  STA    14
1162  LDA   131
1163  STA    12
1164  LDA   156
1165  STA    10
1166  STA   130
1167  LDA   153
1170  STA    11
1171  STA   131
1172  LDA   432
1173  STA    45
1174  RET
1175
1176  LDA   433
1177  STA   435
1200  LDA   132
1201  STA    14
1202  LDA   133
1203  STA    12
1204  LDA   157
1205  STA    10
1206  STA   132
1207  LDA   154
1210  STA    11
1211  STA   133
1212  RET

1213  LMB   100
1214  SMB   103
1215  DZM   146
1216  DZM   147
1217  JLP  1705
1220  LDA   134
1221  STA    14
1222  LDA   135
1223  STA    12
1224  LDA   160
1225  STA    10
1226  STA   134
1227  LDA   155
1230  STA    11
1231  STA   135
1232  LDA   434
1233  STA   435
1234  RET
1235  LDA   542
1236  SRA   421
1237  ISZ   421
1240  ISZ   421
1241  LRA   421
1242  RET
1243  LDA    14
1244  ADD    10
1245  STA    17
1246  LDA    12
1247  ADD    11
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1250  STA   15
1251  LDA   11
1252  SUB   12
1253  STA   16
1254  LTR  506
1255  LDA  511
1256  FMU   16
1257  ADD   16
1260  SHL
1261  STA   16
1262  RET
1263  SPA
1264  NEG
1265  SUB  544
1266  SNA
1267  JLP 1653
1270  LDA  414
1271  SZA
1272  JLP 1302
1273  LDA  264
1274  SAD  557
1275  JLP 1667
1276  SRA  421
1277  ISZ  421
1300  LRA  421
1301  RET
1302  DSZ  414
1303  JLP 1122
1304  LDA   21
1305  SZA
1306  RET
1307  ISZ   21
1310  ISZ  264
1311  LDA  542
1312  RET
1313  ADD  550
1314  SAD  516
1315  LDA  550
1316  STA  443
1317  ISZ  444
1320  RET
1321  SRA  273
1322  ISZ  272
1323  ISZ  272
1324  LRA  272
1325  RET
1326  LMB  206
1327  JLP 1361
1330  LMB  211
1331  JLP 1361
1332  LMB  214
1333  JLP 1361
1334  LMB  217
1335  JLP 1361
1336  LMB  222
1337  JLP 1361
1340  LMB  225
1341  JLP 1361
1342  LMB  230
1343  JLP 1361
1344  LMB  233
1345  JLP 1361
1346  LMB  236
1347  JLP 1361
1350  LMB  114
1351  JLP 1361
1352  LMB  117
1353  JLP 1361
1354  LMB  200
1355  JLP 1361
1356  LDA  550
1357  STA  272
1360  LMB  203
1361  SMB  265
1362  LRA  273
1363  RET
1364  STA  136
1365  JSR 1321
1366  LDA  265
1367  STA  122
1370  JSR 1575
1371  JLP  214
1372  LSR 1321
1373  LDA  265
1374  STA    0
1375  CLA
1376  JLP  215
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1377  STA  137
1400  JSR 1321
1401  LDA  266
1402  STA  124
1403  JSR 1575
1404  JLP  250
1405  JSR 1321
1406  LDA  266
1407  STA    1
1410  CLA
1411  JLP  251
1412  STA  140
1413  JSR 1321
1414  LDA  267
1415  STA  126
1416  JSR 1575
1417  JLP  314
1420  JSR 1321
1421  LDA  267
1422  STA    2
1423  CLA
1424  JLP  315
1425  STA  141
1426  JSR 1321
1427  LDA  267
1430  SUB  266
1431  STA  130
1432  JSR 1575
1433  JLP  345
1434  JSR 1321
1435  LDA  267
1436  SUB  266
1437  STA  156
1440  CLA
1441  JLP  346
1442  STA  142
1443  JSR 1321
1444  LDA  265
1445  SUB  267
1446  STA  132
1447  JSR 1575
1450  JLP  116
1451  JSR 1321
1452  LDA  265
1453  SUB  267
1454  STA  157
1455  CLA
1456  JLP  117
1457  STA  143
1460  JSR 1321
1461  LDA  266
1462  SUB  265
1463  STA  134
1464  JSR 1575
1465  JLP  462
1466  JSR 1321
1467  LDA  266
1470  SUB  265
1471  STA  160
1472  CLA
1473  JLP  463
1474
1475  ISZ  272
1476  ISZ  272
1477  ISZ  176
1500  ISZ  176
1501  LRA  176
1502  LMB    0
1503  RET
1504  SMB  200
1505  JLP  421
1506  SMB  203
1507  JLP  421
1510  SMB  206
1511  JLP  421
1512  SMB  211
1513  JLP  421
1514  SMB  214
1515  JLP  421
1516  SMB  217
1517  JLP  421
1520  SMB  222
1521  JLP  421
1522  SMB  225
1523  JLP  421
1524  SMB  230
1525  JLP  421
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1526  SMB  233
1527  JLP  421
1530  SMB  236
1531  JLP  421
1532  SMB  114
1533  JLP  421
1534  SMB  117
1535  LDA  565
1536  STA  176
1537  LDA  550
1540  STA  272
1541  JLP  421
1542  ISZ  271
1543  LDA  271
1544  SUB  544
1545  SZA
1546  JLP 1552
1547  LDA  443
1550  STA  272
1551  JLP  437
1552  SUB  544
1553  SZA
1554  JLP  437
1555  LDA  274
1556  STA  272
1557  DZM  271
1560  JLP  437
1561  LDA  136
1562  JHP   66
1563  LDA  137
1564  JHP   66
1565  LDA  140
1566  JHP   66
1567  LDA  141
1570  JHP   66
1571  LDA  142
1572  JHP   66
1573  LDA  143
1574  JHP   66
1575  LDA  444
1576  SZA
1577  RET
1600  LDA  272
1601  SAD  516
1602  LDA  550
1603  STA  274
1604  SUB  516
1605  ADD  523
1606  SNA
1607  JLP 1313
1610  ADD  522
1611  JLP 1314
1612
1613  STA  175
1614  LTR  564
1615  LDA  503
1616  FMU  275
1617  NEG
1620  SUM  175
1621  LTR  504
1622  LDA  505
1623  FMU  276
1624  NEG
1625  SUM  175
1626  LDA  275
1627  SHL
1630  ADD  175
1631  SUM  276
1632  LTR  506
1633  LDA  507
1634  FMU  276
1635  RET
1636  SRA  267
1637  JLP  207
1640  SRA  267
1641  JLP  243
1642  SRA  267
1643  JLP  307
1644  SRA  267
1645  JLP  340
1646  SRA  267
1647  JLP  111
1650  SRA  267
1651  JLP  455
1652  JHP 1703
1653  LDA  414
1654  SZA
```

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1655  JLP  1235
1656  DZM   150
1657  DZM    21
1660  DZM   264
1661  LDA   565
1662  STA   176
1663  LDA   550
1664  STA   272
1665  DZM   271
1666  JLP  1235
1667  LDA   144
1670  SUB   556
1671  SZA
1672  JLP  1276
1673  LDA    34
1674  SZA
1675  JLP  1034
1676  JHP   135
1677  LMB     0
1700  SMB   167
1701  LMB     3
1702  SMB   172
1703  JLP  1704
1704  JHP   457
1705  DZM   403
1706  DZM   404
1707  DZM   276
1710  DZM   271
1711  DZM   275
1712  LDA    73
1713  SHR
1714  STA    73
1715  DZM   264
1716  DZM    74
1717  DZM    57
1720  DZM    60
1721  LMB   147
1722  SMB    61
1723  SMB   241
1724  SMB    21
1725  DZM   400
1726  DZM   401
1727  DZM   402
1730  DZM   405
1731  DZM   244
1732  DZM    64
1733  DZM   146
1734  DZM    47
1735  DZM    24
1736  DZM    25
1737  DZM   145
1740  JLP  1653
1741  AND   555
1742  STA    53
1743  LDA    75
1744  MSR     3
1745  STA    50
1746  JLP     1
1747  DZM   151
1750  DZM    74
1751  DZM    57
1752  LDA   565
1753  STA   176
1754  DZM   144
1755  LDA   567
1756  STA   272
1757  JHP   124
1760  WFS
1761  JSR   477
1762  LDA   415
1763  SBC    17
1764  JLP  1760
1765  LDA   415
1766  MSL     2
1767  MSR     3
1770  STA    75
1771  AND   565
1772  STA    67
1773  LDA    75
1774  MSR     3
1775  STA    75
1776  JLP  1741
1777  RET
```

A6.2 HIGH PAGE

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0  STA  143      33  JLP  144      66  STA  262
1  STT  434      34  JHP 1467      67  SZA
2  JLP  641      35  STA  140      70  JHP   72
3  LDA    3      36  STT  431      71  RET
4  SPA           37  JLP  413      72  SUB  560
5  NEG           40  LTR  435      73  STA  262
6  MSR    3      41  RET           74  RET
7  JHP 1454      42  DZM   57      75  LDA  262
10 STA   35      43  JHP  246      76  SAD  543
11 JHP   23      44  DZM   26      77  JHP  101
12 STA  136      45  DZM   74     100  JLP  144
13 STT  427      46  LDA  571     101  LTR  563
14 JLP  232      47  JHP 1444     102  LDA   56
15 SBS    1      50  STA  142     103  FMU   36
16 JHP  325      51  STT  433     104  STA   70
17 JHP  317      52  JLP  443     105  LTR   70
20 STA  137      53            106  LDA  557
21 STT  430      54  ISZ   57     107  DPA   40
22 JLP  266      55  JHP  254     110  SNA
23 LDA  163      56            111  JHP   32
24 STA   36      57  LTR  435     112  ISZ  422
25 LDA  165      60  SRA  270     113  JLP  144
26 STA   37      61  ISZ  270     114  LDA  151
27 LDA  166      62  LDA  543     115  SAD  546
30 STA  420      63  LRA  270     116  DZM  423
31 JHP 1023      64  STA  262     117  JHP 1743
32 DZM  422      65  RET           120  LDA  560
```

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121  STA   47
122  DZM   24
123  JHP   42
124  DZM   444
125  DZM   445
126  DZM   406
127  DZM   407
130  DZM   410
131  DZM   411
132  DZM   412
133  DZM   413
134  JHP   162
135  LDA   556
136  INC
137  STA   1177
140  JHP   44
141  STA   11
142  JSR   411
143  LDA   57
144  SZA
145  JHP   1542
146  LDA   11
147  SUM   266
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157  SZA
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A6.3 LOW PAGE(THE MIDPOINTS FORMULA)

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213  JLP 1364
214  JLP 1372
215  STA  100
216  JSR 1044
217  JSR 1250
220  LMB  100
221  SMB   12
222  LMB   15
223  SMB  100
224  JSR  661
225  JSR 1563
226  JHP   12
227  JSR 1160
230  JSR 1250
231  JLP  240
232  LDA    0
233  STA   65
234  LDA  167
235  STA   66
236  JSR  570
237  JLP  243
240  LMB  111
241  SMB   12
242  JLP  263
243  LDA  101
244  STA  414
245  LDA    1
246  JSR 1263
247  JLP 1377
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250  JLP 1405
251  STA  101
252  JSR 1062
253  JSR 1250
254  LMB  103
255  SMB   12
256  LMB   15
257  SMB  103
260  JSR  661
261  JSR 1563
262  JHP   20
263  LMB   15
264  SMB  111
265  JLP  267
266  JLP  272
267  JSR 1176
270  JSR 1250
271  JLP  327
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307  LDA  102
310  STA  414
311  LDA    2
312  JSR 1263
313  JLP 1412
314  JLP 1420
315  STA  102
316  JSR 1102
317  JSR 1250
320  LMB  106
321  SMB   12
322  LMB   15
323  SMB  106
324  JSR  661
325  JSR 1565
326  JHP   35
327  LMB  114
330  SMB   12
331  JLP  360
332  LDA    2
333  STA   65
334  LDA  171
335  STA   66
336  JSR  570
337  JLP  340
340  LDA  103
341  STA  414
342  LDA  156
343  JSR 1263
344  JLP 1425
345  JLP 1434
346  STA  103
347  JSR 1160
350  JSR 1250
351  LMB  111
352  SMB   12
353  LMB   15
354  SMB  111
355  JSR  566
356  JSR 1567
357  JHP  151
360  LMB   15
361  SMB  114
362  JLP  364
363  JLP  367
364  JSR 1220
365  JSR 1250
366  JLP  452
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443  DZM  436
444  LDA    4
445  STA   65
446  LDA  173
447  STA   66
450  JSR  570
451  JLP  455
452  LMB  117
453  SMB  112
454  JLP  636
455  LDA  105
456  STA  414
457  LDA  160
460  JSR 1263
461  JLP 1457
462  JLP 1466
463  STA  105
464  JLP  625
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567 JHP 564
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625 JSR 1220
626 JSR 1250
627 LMB 117
630 SMB 12
631 LMB 15
632 SMB 117
633 JSR 566
634 JSR 1573
635 JHP 0
636 LMB 15
637 SMB 117
640 JLP 142
641 LDA 5
642 STA 65
643 LDA 174
644 STA 66
645 JSR 570
646 JHP 1113
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664 JHP 564
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1043
1044  LDA   122
1045  STA     6
1046  LDA   123
1047  STA     7
1050  LDA     0
1051  STA   122
1052  STA    10
1053  LDA     3
1054  ADD   416
1055  STA    11
1056  STA   123
1057  LDA   427
1060  STA   435
1061  RET
1062  LDA   124
1063  STA     6
1064  LDA   125
1065  STA     7
1066  LDA     1
1067  STA   124
1070  STA    10
1071  LDA     4
1072  ADD   416
1073  STA    11
1074  STA   125
1075  LDA   430
1076  STA   435
1077  RET
1100
1101
1102  LDA   431
1103  STA   435
1104  LDA   126
1105  STA     6
1106  LDA   127
1107  STA     7
1110  LDA     2
1111  STA    10
1112  STA   126
1113  LDA     5
1114  ADD   416
1115  STA    11
1116  STA   127
1117  RET
1120
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1121
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1160   LDA   130
1161   STA     6
1162   LDA   131
1163   STA     7
1164   LDA   156
1165   STA    10
1166   STA   130
1167   LDA   153
1170   STA    11
1171   STA   131
1172   LDA   432
1173   STA   435
1174   RET
1175
1176   LDA   433
1177   STA   435
1200   LDA   132
1201   STA     6
1202   LDA   133
1203   STA     7
1204   LDA   157
1205   STA    10
1206   STA   132
1207   LDA   154
1210   STA    11
1211   STA   133
1212   RET
1213
1214
1215
1216
1217
1220   LDA   134
1221   STA     6
1222   LDA   135
1223   STA     7
1224   LDA   160
1225   STA    10
1226   STA   134
1227   LDA   155
1230   STA    11
1231   STA   135
1232   LDA   434
1233   STA   435
1234   RET
1235
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1250   LDA   6        1305                    1342
1251   ADD   10       1306                    1343
1252   STA   17       1307                    1344
1253   LDA   7        1310                    1345
1254   ADD   11       1311                    1346
1255   STA   15       1312                    1347
1256   LDA   11       1313                    1350
1257   SUB   7        1314                    1351
1260   STA   16       1315                    1352
1261   RET            1316                    1353
1262                  1317                    1354
1263                  1320                    1355
1264                  1321                    1356
1265                  1322                    1357
1266                  1323                    1360
1267                  1324                    1361
1270                  1325                    1362
1271                  1326                    1363
1272                  1327                    1364
1273                  1330                    1365
1274                  1331                    1366
1275                  1332                    1367
1276                  1333                    1370
1277                  1334                    1371
1300                  1335                    1372
1301                  1336                    1373
1302                  1337                    1374
1303                  1340                    1375
1304                  1341                    1376
```

A6.4 CONTENTS OF THE DATA STORE

Addr.	Data	
0	V_a	V,I samples or their filtered values if the digital filter is applied
1	V_b	
2	V_c	
3	I_a	
4	I_b	
5	I_c	
6	V_{N-1}	
7	I^1_{N-1} , I^2_{N-2}	compensated
10	V_N	
11	I_N	
12	CA	
13	DCA	
14	VA	
15	CB	
16	DCB	
17	VB	
20	$(V_a)_{N-1}$	
21	CUF	
22	FI	
23	KOFI	
24	PQOC	
25	PQSC	

Addr.	Data	
26	CBCT	
27	IC	
30	Temp. storage	
31	Duplicate of 25	used by the fault report
32	" " 23	
33	MCW	
34	MSCW	
35	N_R	After shifting, to obtain single-precision numbers.
36	D	
37	N_L	
40	LSB	$N_L - N_R \tan\varphi + R_a D \tan\varphi$
41	MSB	
42	-	
43	$(V_a)_{N-2}$	
44	Identification bit for P,Q output (=1)	
45	D	Duplicate of MSB
46	N_R	
47	PSI	
50	$\tan\varphi$	
51	-	
52	VOC	
53	$(V_b)_{N-1}$	

Note: 1: The midpoints algorithm

2: The sample and midpoint formula

54 LSB
55 MSB } D duplicate

56 $R_a \tan\varphi$

57 GFC

60 $(V_b)_{N-2}$

61 $(V_c)_{N-1}$

62 $(V_c)_{N-2}$

63 $(I_a)_{N-1}$

64 $(I_a)_{N-2}$

65 Filtered data
66 Unfiltered data } common locs for graphics

67 K-1

70 Temp. Storage

71 -

72 $(I_c)_{N-1}$

73 X_L

74 CBCI

75 Temp. Storage

76 Measured V_{ref}

77 -

100 $CURG^2$
101 $CUYG^2$
102 $CUBG^2$
/ CA / DCA / VA } RG^1

103 $CUYB^2$
104 $CURB^2$
105 $CURY^2$
/ CA / DCA / VA } YG^1

106 I_a
107 I_b
110 I_c
/ 2_{N-2} / CA / DCA / VA } BG^1

111 I_A
112 I_B
113 I_C
/ 2_{N-2} / CA / DCA / VA } YB^1

114 V_a
115 V_b
116 V_c
/ 12th / CA / DCA / VA } RB^1

117 V_a
120 V_b
121 V_c
/ 13th / CA / DCA / VA } RY^1

122 V_a
123 I_a
124 V_b
125 I_b
126 V_c
127 I_c
} compensated N-1 sample

130 V_A
131 I_A
132 V_B
133 I_B
134 V_C
135 I_C
} compensated N-1 sample

136 RGF

137 YGF

140	BGF		
141	YBF		
142	RBF		
143	RYF		
144	4 cycles timer		
145	SOFC		
146	CBS		
147	TTC		
150	VIZ		
151	FCC		
152	I_o		
153	I_A	phase quantities	
154	I_B	phase quantities	
155	I_C	phase quantities	
156	V_A	phase quantities	
157	V_B	phase quantities	
160	V_C	phase quantities	
161	LSB	N_R	
162	MSB	N_R	
163	LSB	D	
164	MSB	D	
165	LSB	N_L	
166	MSB	N_L	
167	V_a	unfiltered	
170	V_b	unfiltered	
171	V_c	unfiltered	
172	I_a	unfiltered	
173	I_b	unfiltered	
174	I_c	unfiltered	
175	N sample for filtering		
176	SPFD		
177	-		
200	V_a	1st	
201	V_b	1st	
202	V_c	1st	
203	V_a	2nd	
204	V_b	2nd	
205	V_c	2nd	
206	V_a	3rd	
207	V_b	3rd	
210	V_c	3rd	
211	V_a	4th	
212	V_b	4th	
213	V_c	4th	
214	V_a	5th	
215	V_b	5th	
216	V_c	5th	
217	V_a	6th	
220	V_b	6th	
221	V_c	6th	
222	V_a	7th	
223	V_b	7th	

224	V_c	7th
225	V_a	8th
226	V_b	
227	V_c	
230	V_a	9th
231	V_b	
232	V_c	
233	V_a	10th
234	V_b	
235	V_c	
236	V_a	11th
237	V_b	
240	V_c	
241	LSB	P common
242	MSB	
243	LSB	Q common
244	MSB	
245	LSB	P_{N-2}
246	MSB	
247	LSB	Q_{N-2}
250	MSB	
251	LSB	P_{N-1}
252	MSB	
253	LSB	Q_{N-1}
254	MSB	
255	LSB	P_N
256	MSB	

257	LSB	Q_N
260	MSB	
261	-	
262	Common fault counter	
263	$(I_c)_{N-2}$	
264	ECUF	
265	V_a	Prefault common Block / I_o rms I_F rms Return address
266	V_b	
267	V_c	
270	Return address for imped. calc.	
271	OCC	
272	LPFD	
273	RA for loading pre-fault voltages	
274	FPPB	
275	N-1 sample for filtering	
276	N-2 " " "	
277	—	
400	LSB	a
401	MSB	
402	LSB	b
403	MSB	
404	LSB	c
405	MSB	
406	LSB	A
407	MSB	
410	LSB	B
411	MSB	
412	LSB	C
413	MSB	

N_L-X_LD

414	CCUF
415	CW
416	$I_o(K-1)$
417	--
420	Return address
421	" "
422	OOSC
423	RC
424	DTC
425	CBCTC
426	LOUTC
427	RG } Z2-Z3 timers
430	YG }
431	BG }
432	YB } Z2-Z3 timers
433	RB }
434	YR }
435	Common timer
436	RAB
437	SIS
440	--
441	--
442	--
443	SPPB
444	CUP
445	$(I_b)_{N-1}$
446	$(I_b)_{N-2}$

A6.5 TABLE OF THE MNEMONICS

The used mnemonics are grouped according to their function and are listed in alphabetical order. In parenthesis the address of the data location, where the corresponding flag stored, is given in octal.

A6.5.1 The following flags, initially are set to 3. They are decremented by one, on the condition described, otherwise they are reset.

BGF(140): Internal blue-ground line fault
BRF(142): " blue-red " "
RGF(136): " red-ground " "
RYF(143): " red-yellow " "
YBF(141): " yellow-blue " "
YGF(137): " yellow-ground " "
CFF(262): Common loc. for the above 6 counters

A6.5.2 The next group of flags is functioning as above, but their initial value is equal 2.

CUBG(102): Internal red-ground close-up fault
CUBR(104): " blue-red " "
CURG(100): " red-ground " "
CURY(105): " red-yellow " "
CUYB(103): " yellow-blue " "
CUYG(101): " yellow-ground " "

A6.5.3 The next words are used to control the operations described.

CW(415): The digital word, which controls the the graphics routine.

IC(27) : Controls the Simpson's integration routine.

MCW(33) : The digital word with the msbit and the lsbit being masked.

MSCW(34): Same as above, but shifted 3 times to the left.

A6.5.4 The following locations are used as counters. Counting starts on the condition given.

CBCI(74): It is incremented, when the current is zero for successive samples. Indicated the CB interruption instant.

CBCT(26): Counting starts when a fault has been detected, and stops, when the contacts of the CB have opened, i. e. CB clearence time.

CBCTC(425): Indicates the time required by the CB , to close its contacts.

DTC(424): The dead time for the autoreclosing scheme.

FCC(151): Is incremented for the first cycle, after the switching-on of the CB.

OCC(271): One cycle counter

OOSC(422): Out-of-step timer

PQOC(24) : Counts the number of data transmitted

to the monitoring computer for a P-Q measurement.

PQSC(25): Three-cycle timer, used to store the P-Q values for 3 consecutive cycles.

SOFC(145): Is incremented when a switch-on-fault has been detected.

TTC(147) : Counting begins when the fault has been applied and it stops when the fault has been detected, i. e. detection time counter.

A6.5.5 The following data locations are used to indicate the starting address of a program block, which is going to be addressed indirectly by indexing. The function of each of these locations is given below.

FAPB(516): First address of the prefault voltage block.

FPPB(274): The starting address of the prefault voltage block, for reading.

LAPB(550): Last address of the prefault voltage block.

LPFD(272): Pointer to the address of the corresponding prefault voltage block, for reading.

SPFD(176): Pointer to the address of the corresponding prefault voltage block, for writing.

SPPB(443): The last address of the prefault voltage block, for reading.

A6.5.6 The next group of flags is set on the condition described.

CBS(146) : When the command to open the CB has been sent.

CCUF(414): Common close-up flag

CUF(21) : If a fault has been classified as close-up.

CUP(444) : If more than one phase is involved in a close-up fault.

ECUF(264): In a case of an external close-up fault.

FI(22) : When an internal fault has been detected.

GFC(57) : When a ground-fault impedance is executed.

KOFI(23) : Indicated which of the six impedance calculations has detected the fault. It is 1 for RG, 2 for YG, 3 for BG, 4 for YB, 5 for BR, 6 for RY.

LOUTC(426): If a permanent fault is on the line, i. e. CB has locked out.

PSI(47) : If the operators request for a P-Q measurement report has been accomplished.

RAB(436): If the resistance calculation for a RY fault has been executed.

RC(423) : Indicates the number of times the autoreclose has operated.

SIS(437): Is incremented during every sampling interval. If the resulting number is even then the ground fault starting elements are executed, while for an odd number the phase fault starters are run.

VIZ(150): When both voltage and current are zero.

VOC(52) : When a plot of the three voltages or currents has been requested.

A6.6 CONTENTS OF THE CONSTANT STORE

Address	Data	Address	Data
503	b_1	557	-1
504	-7	560	1
505	-6	561	0
506	a_o	563	-8
511	0.703125	564	-9
516	1356(octal)=FAPB	565	1502(octal)
522	1360(octal)	567	1322(octal)
523	18	570	1/3=0.33398437
524	Zone 2 timer	571	} CB Control words
525	Zone 3 timer	572	
526	Zone 2 setting	573	16
527	Zone 3 setting	574	79
530	Zone 3 time limit		
533	Dead time		
534	R_{ab}		
540	-130		
542	2		
543	3		
544	4		
545	5		
546	8		
550	1324(octal)=LAPB		
554	-2		
555	7		
556	31		

Papers presented:

1) L. Petrou, E. Horne, B. J. Cory: " Micrc-computer applications in protection relaying ". 12th UPEC conference, April 1977.

2) L. Petrou, E. Horne, B. J. Cory: " A microprocessor power system protection relay ". MECO'78, Athens.

Micro-computer applications in protection relaying.

L. Petrou, E. Horne, B.J. Cory.
Imperial College, London SW7.

1.1 Introduction

The application of digital computing techniques to the task of power system protection has been a topic of research by power utilities, industry and universities for several years. The advent of the relatively inexpensive "mini" computer provided a great impetus to studies in this field, and the majority of schemes which have been proposed or implemented are based on processors of this type.

Work undertaken at Imperial College using a multi-mini computer system (Fig 1) for protection and control of one corner in a mesh type substation has demonstrated that schemes of this nature are subject to inter-related economic and technical constraints which may prove unacceptable for widescale application.

1.2 Disadvantages of mini-computer protection

Inevitably in any type of main protection scheme a duplication or triplication of the relaying equipments involved is necessary if the stringent reliability criteria of the task are to be satisfied. From an economic viewpoint, therefore, a multi-minicomputer solution will represent a substantial investment, despite the reductions in cost which have been achieved for these machines. As a result, the tendency, evident in literature published by research groups, has been to develop the concept of integrated protection methods in which multiple relaying functions are embodied in a single computer. Whilst this integrated approach ensures maximum utilisation of the installed computing power, it also gives rise to several intractable technical difficulties. The major problems are summarized as:-

a) Complex Software

The software required for the integrated protection system may be classified into two distinct groups, (i) the algorithms capable of performing the required protective functions, and (ii) the "operating system" for these routines. As the extent of integration increases, the complexity of the operating system software also increases and its operational reliability deteriorates.

b) Initalisation

The initalisation of protective routines is basically a function of the operating system mentioned above. In this context the correct identification of the appropriate plant protection routine at the onset of a fault condition entails a difficult programming task.

c) Response time

Due to the sequential nature of the digital computer the time consumed by the organisational software during a fault may well result in a degredation of clearance speeds, particularly in cases of incorrect initalisation selection. This factor obviously assumes increasing importance as the transmission system load approaches its maximum.

d) Reliability

A high level of hardware and software reliability is

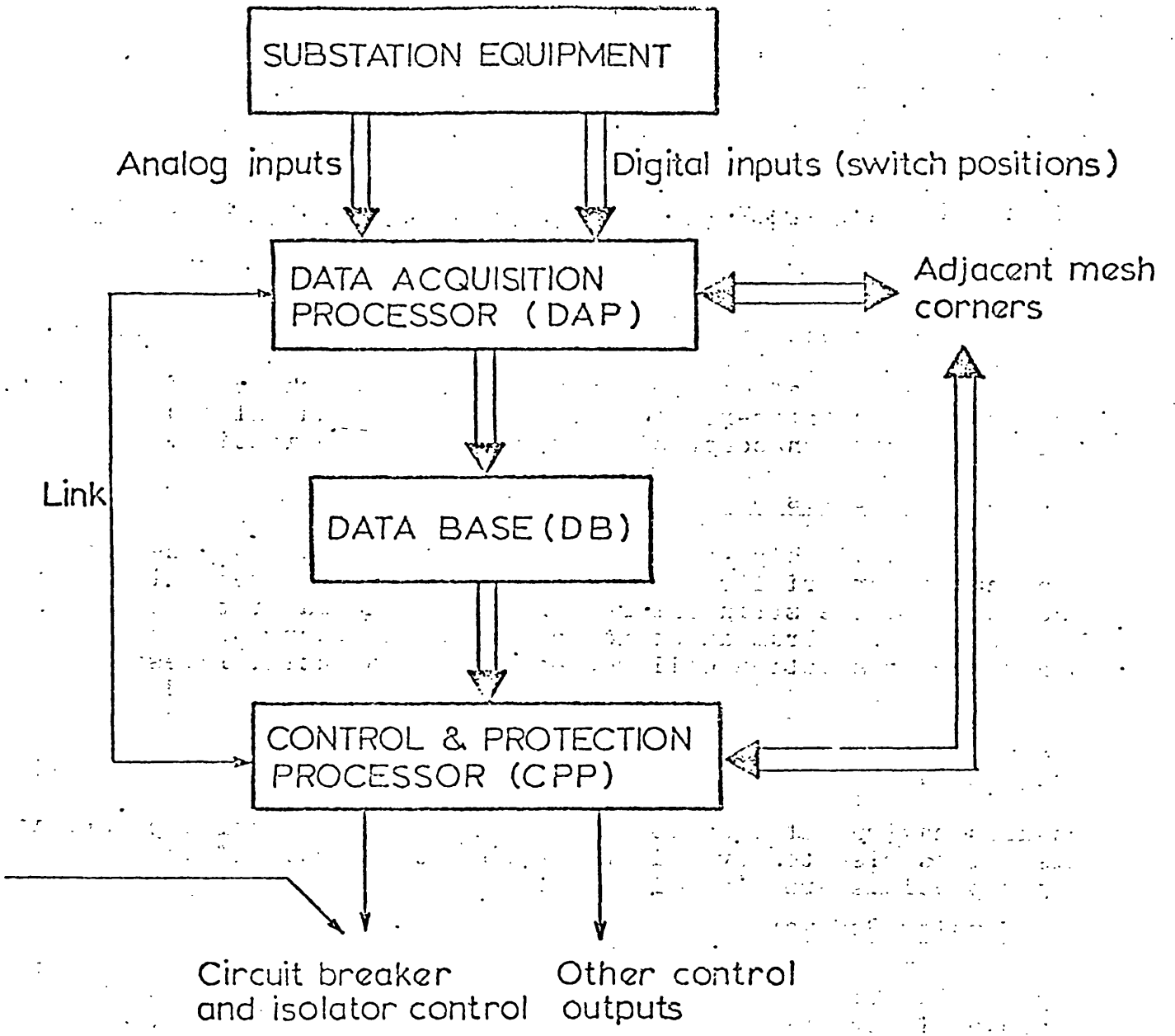

Fig. 1 Proposed hardware configuration for mesh corner protection and control.

required in the integrated system since any major failure in either area will affect a substantial portion of the protection facilities. The provision of high reliability systems would impose further economic penalties.

From the foregoing it is seen that the major limitations of the mini-computer oriented scheme largely originate as a consequence of the integration of the protection processes.

2.1 The Microcomputer dedicated relay

To overcome the difficulties outlined above, an alternative approach has been adopted which, in common with current electromechanical and static analogue relaying practice, proposes a dedicated parallel unit organisation.

The rapid advance of semiconductor technology has made economically possible the employment of a dedicated digital relay for each task, based upon low cost computing devices which fall within the general term "microprocessor". A single relay will consist of two component sub-systems broadly similar to the mini computer configuration, these being the data acquisition or measurement sub-system, and the protection computation processor. Irrespective of the relaying task to be performed, each unit can comprise common hardware but allows for considerable flexibility in use.

2.2 The Measurement sub-system

The function of this sub-unit is primarily one of data collection. This requires that at intervals the a.c. quantities required for the protection algorithm are simultaneously sampled and held at the appropriate transducer outputs and the sampled values are then multiplexed from the sample-holds to an analogue-digital converter, as shown in Fig 2. The resulting digital values are loaded into a first-in-first-out buffer store with breaker/isolator status information which may be required to await the demand of the protection processor.

The timing and configuration control of these elements is provided by an 8 bit micropocessor of the MOS type. Although of low speed, the 8 bit devices which are available are more than adequate for the requirements of the unit, and enable a simple stored program controller to be implemented with a minimum number of integrated circuits whilst providing a flexibility of data acquisition which would not be available in a hard wired arrangement. It should, however, be noted that in this scheme the primary multi-bit data paths are independent of the control processor and thus no provision is made for data pre-processing.

2.3 The Protection Processor

The task of the second portion of the relay differs widely from that of the processor application in the measurement unit. For each block of sampled data provided by the measurement unit, the protection processor must solve the particular fault detection algorithms to which it is dedicated. In this respect the protection algorithm is regarded as including any data filtering which may be required, the fault detection routines, and output switching commands.

An emphasis must thus be placed in this unit upon the ability to perform logical and arithmetic operations, and in order to satisfy these requirements several factors must be considered in

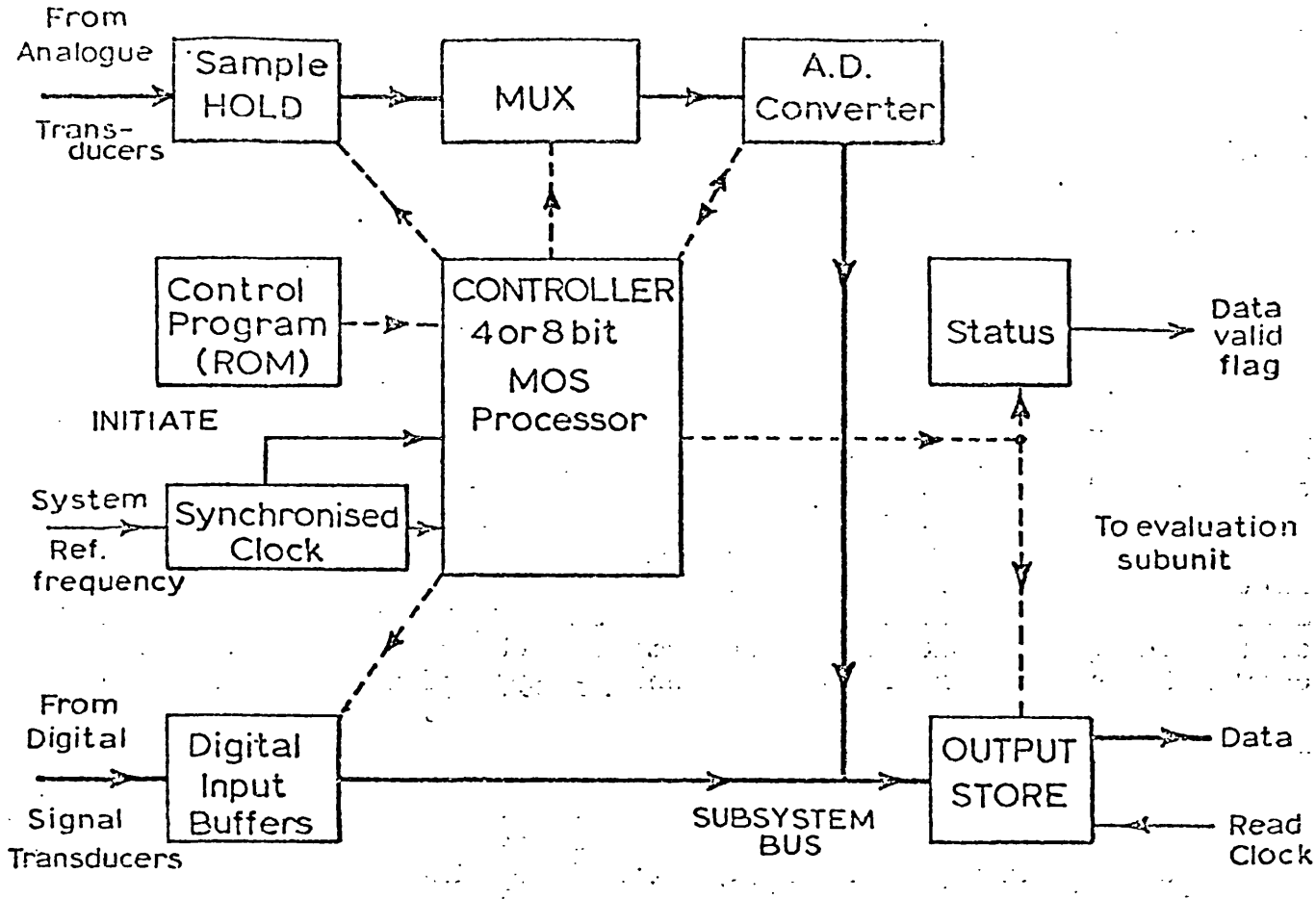

Fig. 2 The Measurement Subsystem

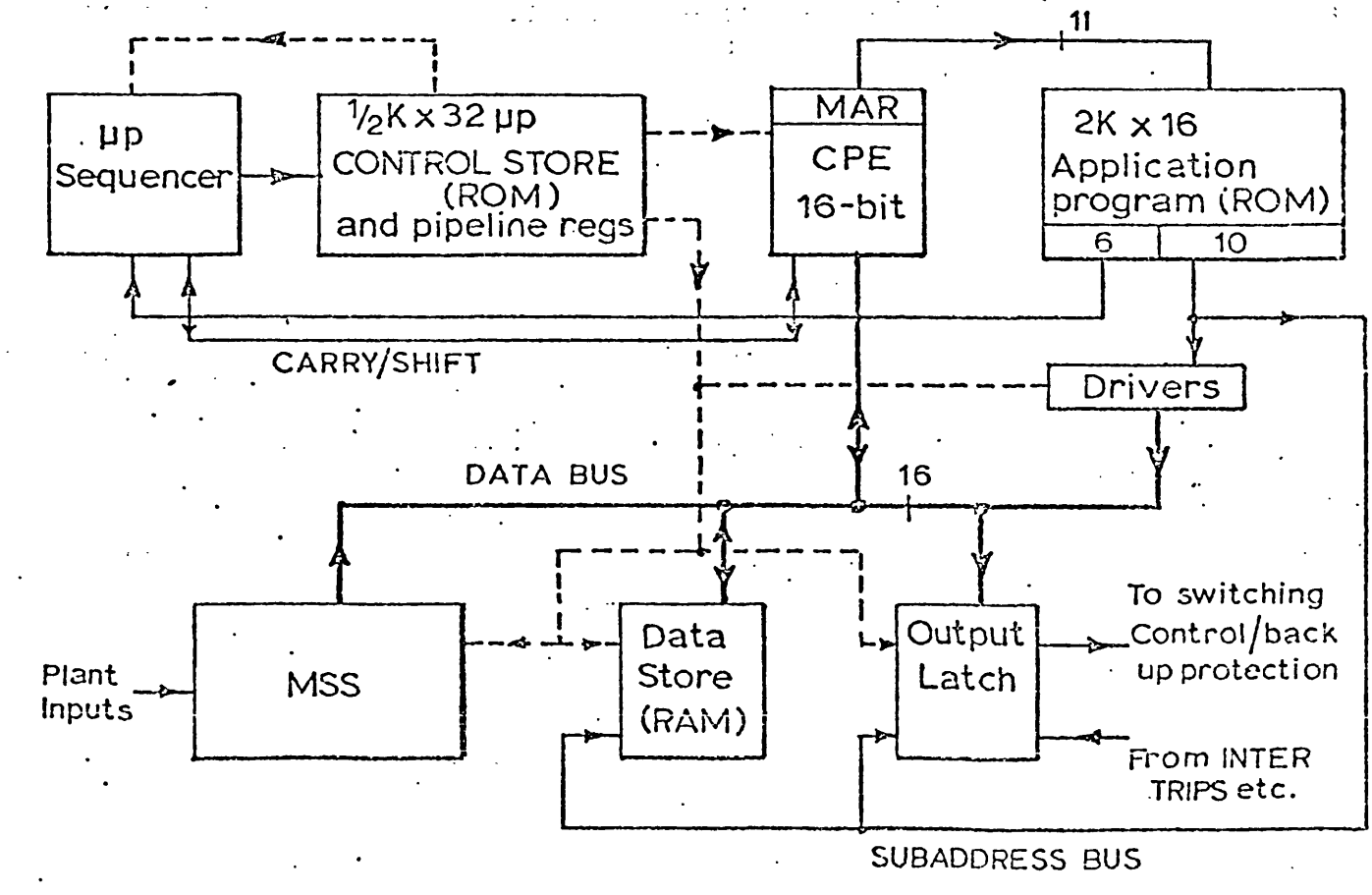

Fig. 3 The Protection Processor

the choice of processor. The most important of these are outlined below, and they indicate that the bipolar bit-slice family of micro-processors can provide a satisfactory solution.

a) Word length

For arithmetic operations employing an 8 bit word length consistent with that commonly found in the single chip microcomputer great care must be taken to avoid a serious degredation of accuracy due to rounding and truncation errors. The bit slice devices allow a great freedom of word length in 2 or 4 bit multiples and the processor shown in Fig 3 has a 16 bit structure.

b) Operating speed

Previous work has shown that in order to achieve a complete evaluation of the a.c. system data between consecutive samples (i.e. 2.5 ms), an instruction cycle time of mini computer standard (i.e. 1-2μS) is desirable. Once again this requirement is satisfied by a bipolar design, whereas with existing M.O.S. devices these speeds are not realizable, particularly if multiple byte operations are involved to maintain accuracy, or to provide a usable instruction format.

c) Powerful Software and Architecture

Although the bit-slice devices are more primitive basic components than their single chip counterparts, they do thereby allow the overall processor architecture to be closely matched to its proposed function. The system of Fig 3 bears only a superficial resemblance to a conventional computer architecture providing as it does only limited read-write storage which is separated for address purposes from the main program memory. This structure combined with extensive pipelining in the control paths and a modified form of Direct Memory Access for input data from the measurement sub-system serves to optimise the unit performance.

Finally from a software viewpoint the micro-programmable organisation of the processor allows a highly efficient dedicated macro-language to be developed for the description of fault detection algorithms.

3. Conclusions

It is well known that in order to achieve optimum results from micro-computers they should be used to perform limited and closely defined tasks. Extension to multiple task or general purpose use negates many of the valuable attributes which the devices possess, and a more parallel structure is desirable (i.e. multi-processor) beyond a certain task complexity. This implies that for power system protection use they are ideally employed as dedicated single function first and second main relays, and the major advantages which may be obtained from such an implementation are:-

a) Standardisation

Since the component sub-units of a relay are constructed with standard hardware features, individual relays for specific functions can be assembled by inclusion of appropriate control algorithms. A considerable easing of the difficulties encountered when an equipment manufacturer is confronted with special requirements, which currently require design changes in conventional electromechanical or state relays, is thus achieved. For the

relay user, standardisation of many items provides a considerable simplification of testing and maintenance operations, and reduces the burden of personnel training.

b) Flexibility

The micro-computer based relay offers the great adaptability which characterises all stored program digital machines. Alterations to the power system plant configuration or parameters may thus be easily reflected in corresponding relaying modifications avoiding protracted and costly re-wiring or re-setting.

c) Reliability

Although the basic components relibilities within a micro-computer relay are only comparable with those used, for example, in a static analogue relay, the dynamic nature of the device enables many of the well proven error detection and self test routines to be incorporated in the operating programs. Thus the possibility of a coincident system/relay fault is minimised and the overall protective equipment reliability enhanced.

d) Compatibility

As a final consideration it is possible to examine the role of the dedicated digital relay within a hierarchical sub-station control scheme. It is envisaged that the microcomputer front line equipment would be provided with a back-up system incorporated in a mini-computer based integrated protection system. The software limitations of the integrated solution mentioned in Section 1.2 would not be critical in a back up mode, and the sophisticated mini machine would provide a constant monitoring service for the front line relays, in addition to communication with controlling stations. For such an implementation the value of a uniform digital device structure is obvious and the micro-computer relay reduces the problems of equipment compatibility.

Currently, effort at Imperial College is directed towards the construction of a protection relay based on the principles outlined in this paper, and it is hoped that the performance of the equipment will be evaluated for several typical relaying tasks in the near future.

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A MICROPROCESSOR POWER SYSTEM PROTECTION RELAY

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ABSTRACT

First a brief discussion is given outlining the reasons for developing the digital protection scheme described. Next the design of a dedicated digital protection relay is considered, from the hardware and software points of view.

In the last chapter some applications of the relay for different protection schemes are examined.

1. INTRODUCTION

Digital computers are already well established in several areas of power system control. They are widely employed in network control and dispatch centres and in power stations.

An extension of digital techniques in power system protection, is an obvious area of development. Digital protection offers improved accuracy, enhanced reliability, better protection characteristic matching, greater flexibility and modular construction. However it introduces some disadvantages, for example, the need to convert the analogue measurements of the system to digital quantities, interference problems and difficulty in completely testing the system under all possible operating conditions.

The first applications of digital protection, used a minicomputer as the processing device. However the use of minicomputers imposes inter-related economic and technical constraints upon the schemes proposed, most of which are encountered when a scheme of this type was constructed at Imperial College. For reliability a duplication or triplication of the relaying equipment used in a multi-minicomputer scheme is required, which represents a considerable cost. As a compromise of this, "integrated protection" schemes have been proposed, in which multiple protection functions are embodied in a single computer to maximize usage of the installed computer power. It has been found that the integrated scheme suffers from several difficulties, such as complex software, critical initialisation, degredation of clearance speeds and reliability[3]. An alternative approach[2] is to replace the existing electromechanical or static analogue relays by dedicated digital relays constructed with microprocessors. Back-up protection and monitoring of the dedicated relays are provided by a mini or microcomputer. Our paper concentrates on the design of a microprocessor based relay.

2. THE MICROCOMPUTER DEDICATED RELAY

In each relay the data acquisition and processing functions are separated. Thus two units comprise a relay, they are: i) the data acquisition interface and ii) the protection processor. This division of the relay components, is dictated by the differing nature of the two functions.

2.1 The data acquisition interface

This unit is concerned with data collection, and has been designed to fulfill the requirements of many different protection schemes. It is a self-contained unit, controlled by a programmable device. The interface can handle up to 16 analogue channels and 4 digital channels. A block diagram of the unit is shown in "Fig. 1". The analogue signals are the a.c. quantities of the system and the digital inputs determine circuit breaker (CB) and isolator status. The analogue signals are derived from the power system by the configuration shown in "Fig. 2". These signals are filtered by second-order Butterworth anti-aliasing filters with a cutoff frequency dependent on the sampling rate. The analogue signals are sampled simultaneously and held on the corresponding sample-hold devices. They are then multiplexed to an analogue-digital converter (ADC). The A/D conversion takes 6μs and has a resolution of 10 bits. The resulting digital values are stored in an output buffer, together with the CB/isolator status (digital inputs). A data ready flag is generated, which indicates to the protection processor that data have been prepared. The timing control of the unit is implemented by counters & PROMs. Another pair of PROMs defines the configuration control i.e. the number of analogue and digital channels, to be used. The sampling rate is variable within the range of 2-24 samples per fundamental system cycle, corresponding to a period of 20ms at 50 Hz and 16.7 ms at 60 Hz.

The unit thus has good flexibility and its internal interface controller relieves the main protection processor of the simple, but time consuming, data acquisition control overheads.

2.2 The protection processor

Studies of existing algorithms for protection, indicate that a processor with a speed close to that of a minicomputer is required. In addition accuracy requirements demand the use of a 16-bit machine. It would be also desirable to construct a flexible system which could be tailored to specific applications.

All the above requirements are met by using a bit-slice bipolar microprocessor. The processor is constructed using the INTEL 3000 device, block diagram of the microcomputer scheme being given in "Fig. 3". In the following sections some critical design factors are described.

2.2.1 Processor control

The INTEL 3000 is a microprogrammable processor meaning that the control portion of the processor is not hard-wired but is software defined by instructions stored in the micromemory. Micro-programmable control permits a flexible instruction set to be defined for specific applications. Additionally it simplifies hardware design.

The control module consists of the microsequencer which controls the execution of the microinstructions, stored in the micromemory. Pipeline registers are used to permit a parallel fetch/execution cycle, which improves the microcycle time by 30%.

Each microinstruction controls the CPU, the memories, the I/O ports and defines the address of the next microinstruction to be fetched. A microinstruction word of 32 bits satisfies those requirements. Each main program instruction (macroinstruction), is thus executed by a sequence of microinstructions.

A max. of 512 locations can be addressed by the microsequencer but on average each macroinstruction is executed by just five microinstructions.

2.2.2 The CPU

The 16 bits CPU of the processor, comprises an array of 8 2-bit slice elements. It provides one accumulator, eleven internal registers and a macro-memory address register (MAR). The accumulator is connected directly to the data bus of the processor. The macromemory is addressed by a separate bus which is defined by the MAR. Some of the internal registers have been designated as program counter, loop counter, subroutine return address register, as well as for other special operations such as multiplication and multiple shifts.

2.2.3 Data buses

The macromemory address bus has been discussed above. The data bus is bidirectional, through which the CPU communicates with the memories and I/O ports. Some other buses, for example the masking (bit testing) bus and flag input bus which improve the system timing are used only at the microinstruction level.

2.2.4 Main memory (macromemory)

Although the CPU can address a maximum of 64 K of memory, this is greatly in excess of the requirements for dedicated protection purposes. From existing algorithms, is found that a 2 K memory is adequate. By employing a 6-bit operation code, we can address the whole memory directly which saves time and leads to a simpler design. The relay application program must be stored in a nonvolatile memory, for which EPROMs have been used. These devices offer high storage density, low cost, low power consumption and they are erasable. A pipeline architecture is employed in the macromemory to provide speed improvements.

2.2.5 Data and constant store

Typically less than 200 locations are required for the storage of data and constants. As the data storage is limited, a complete separation of the program and data memories produces reduction of program counter manipulations. Addresses for the data memory are supplied via the subaddress bus of "Fig. 3", from the 10 lsbits of the macroinstructions. 1024 locations of storage or I/O ports can thus be directly addressed. The data memory consists of banks of RAMs, each 128-word deep and of PROMs each 32-word deep.

2.2.6 Input - output (I/O) ports

The input port provides an interface between the processor data store and the output buffer of the data acquisition unit.

The data output module is dedicated to communication with a supervisory, back-up/monitoring computer. I/O communications are controlled by flags.

For CB control an additional output port is provided with three states, namely: i) trip/relay healthy, ii) no trip/relay healthy and iii) no trip/relay failed. The trip signal is used to control CBs, whilst the relay status signal is decoded by back-up equipment.

2.2.7 Processor timing

In the design presented a complete microcycle takes 200 ns. The clock circuit has been specifically designed to have a stable and predictable start-up performance following initial switch-on or a transient disturbance of the relay power supply.

3. INSTRUCTION SET

Since the processor is microprogrammable the instruction set is not fixed, but can be defined by the user to satisfy a specific application. A basic set of typical minicomputer assembler level instructions has been used. Additionally, several instructions required by the protection algorithms have been included. The instruction set can be divided into 4 groups i.e. control, memory reference, operate and jump/skip instructions. Each instruction consists of 2 fields, a 6-bit operation-code and a 10 bit address/constant field. Therefore a maximum of 64 instructions can be defined. The average instruction execution time is approximately 0.8-1 μs, which

indicates that the main objective i.e. to construct a microprocessor with speed similar to a mini-computer has been satisfied. This performance was only achievable by employing a bipolar micro-programmable processor with an extensive pipeline configuration.

As multiplication is one of the main features that must be included in the processor, a micro-programmed implementation rather than a hardware one has been chosen. This approach reduced both cost and power requirements. Typically the multiplication routine handles two signed 16-bit numbers and produces a 32-bit product in 17 µs.

4. DEVELOPMENT AIDS

To facilitate development of protection processor software, an assembler for the processor language and an EPROM programmer control package have been written. These aids are resident in a host mini-computer (NOVA 3). Another PROM programmer has been built, for programming the bipolar PROMs used in the micromemory and in the constant store.

For the initial testing and development of the microinstructions a bipolar PROM simulator was employed. Development time can be reduced if application routines are first tested using a MOS PROM simulator. For this purpose another PROM simulator has been built which can accommodate up to 512 16-bit words.

Finally extensive programs have been written in the monitoring computer, to enable the relay performance to be assessed. Additionally a monitoring program, which types fault reports has been written.

5. APPLICATIONS

The great advantage of a digital relay is that common hardware can be used for different protection purposes, simply by changing EPROMs, which contain the protection algorithms.In the following sections, a brief discussion of some protection schemes is given.

5.1 Generator negative sequence protection

The protection of expensive generating plant is an important area of relay application. Specifically, prolonged asymmetrical loading of a generator can produce considerable heating within the machine, through negative sequence current generation in the rotor. A digital negative sequence protection relay has been developed using the microprocessor equipment described. The relay algorithm employs symmetrical component techniques to determine the magnitude of the negative sequence components present in the generator load currents. Vector rotation required by symmetrical component analysis is readily available if the a.c. quantities are sampled at 12 times per power system cycle.

A further portion of the algorithm then evaluates a tripping characteristic from the expression:

$$I_2^2 t = K$$

where I_2 = negative sequence current magnitude

t = time to trip

K = constant dependent upon the heating characteristics of a particular machine type.

Laboratory tests have shown that the digital implementation fully satisfies the requirements of the protection function. In several areas, particularly those of alarm facilities and reduced frequency sensitivity in the digital negative sequence filter, the microprocessor relay represents an improvement on existing static analogue equipments.

5.2 Distance relay

A distance protection algorithm, is now being implemented. It uses the McInnes and Morrison concept of a transmission line composed of R and L only[4]. A simple algorithm can be written which solves the equation $Ri + L\,di/dt = V$, using first differences[5].

The computed R and L are compared with the nominal values and a decision is taken according to the conditions: i) no fault, ii) external fault and iii) internal fault. For this algorithm the primary system quantities are sampled eight times per cycle. Between each sampling point i.e. 2.5ms, the relay executes 6 impedance calculations, i.e. three to detect phase-phase faults, and three more for phase-earth faults.

Tests have been carried out for a phase-phase fault which indicate a detection time of about 3/4 cycle "Fig.4".. For close-up faults a directional element is needed to discriminate between line faults and faults behind the relay. A voltage memory principle is easy to apply, as the prefault voltages are available. The same relay structure has been used for overcurrent, earth faults, transformer and generator unit protection.

6. CONCLUSIONS

An hierarchical digital protection scheme can be implemented, with an improved reliability and reasonable cost, by using front line relays of the type described. The system offers good flexibility and compatability in a complete digital protection scheme. From the manufacturers point of view standardisation of relay hardware is an attractive feature.

Further, differing protective functions, can be easily implemented with characteristics to accommodate changes in the power system. The fault report produced by the monitoring computer, is also a very useful addition in the system operation.

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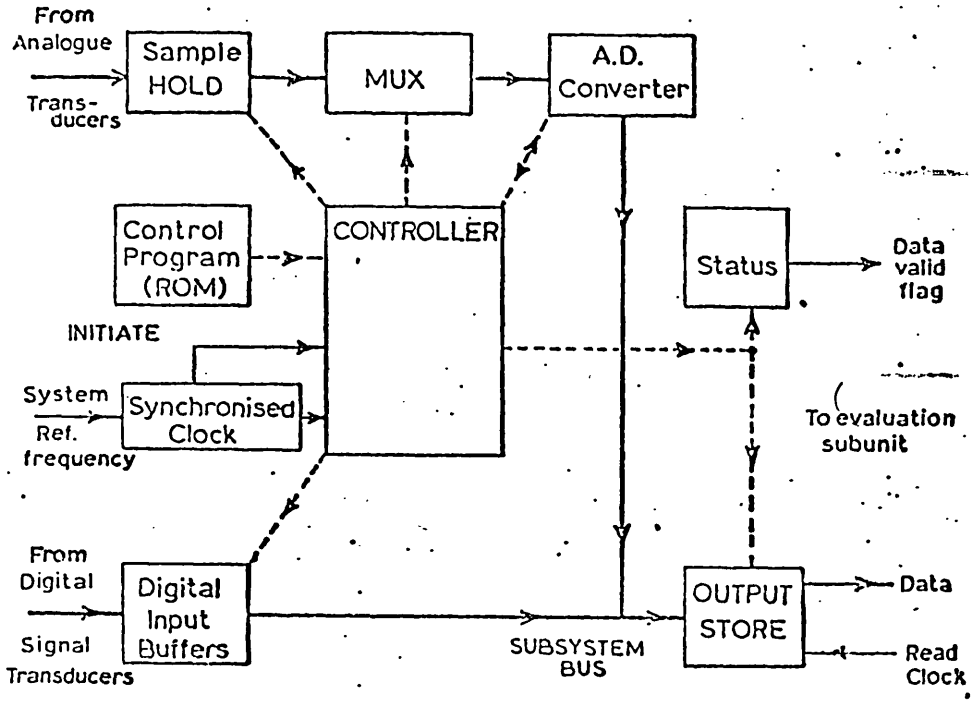

Fig.1 The data aquisition interface

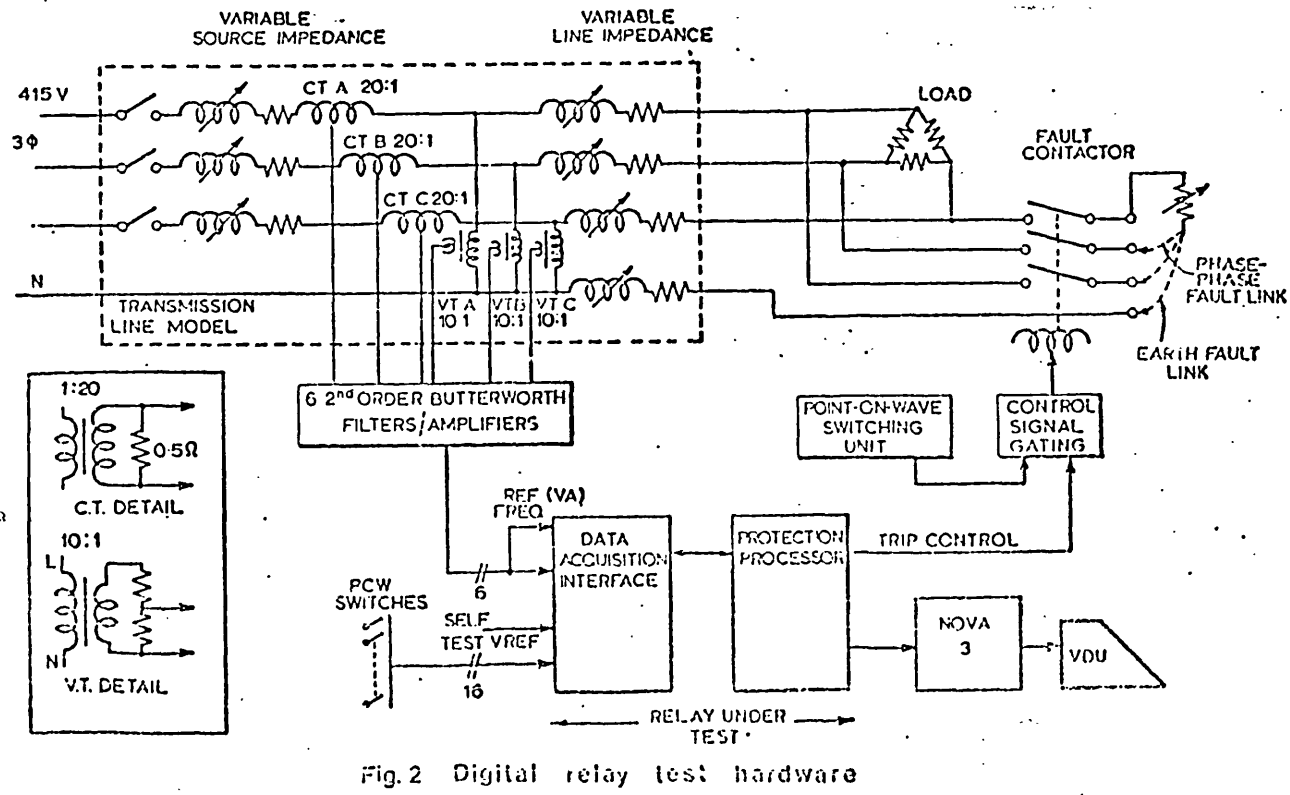

Fig. 2 Digital relay test hardware

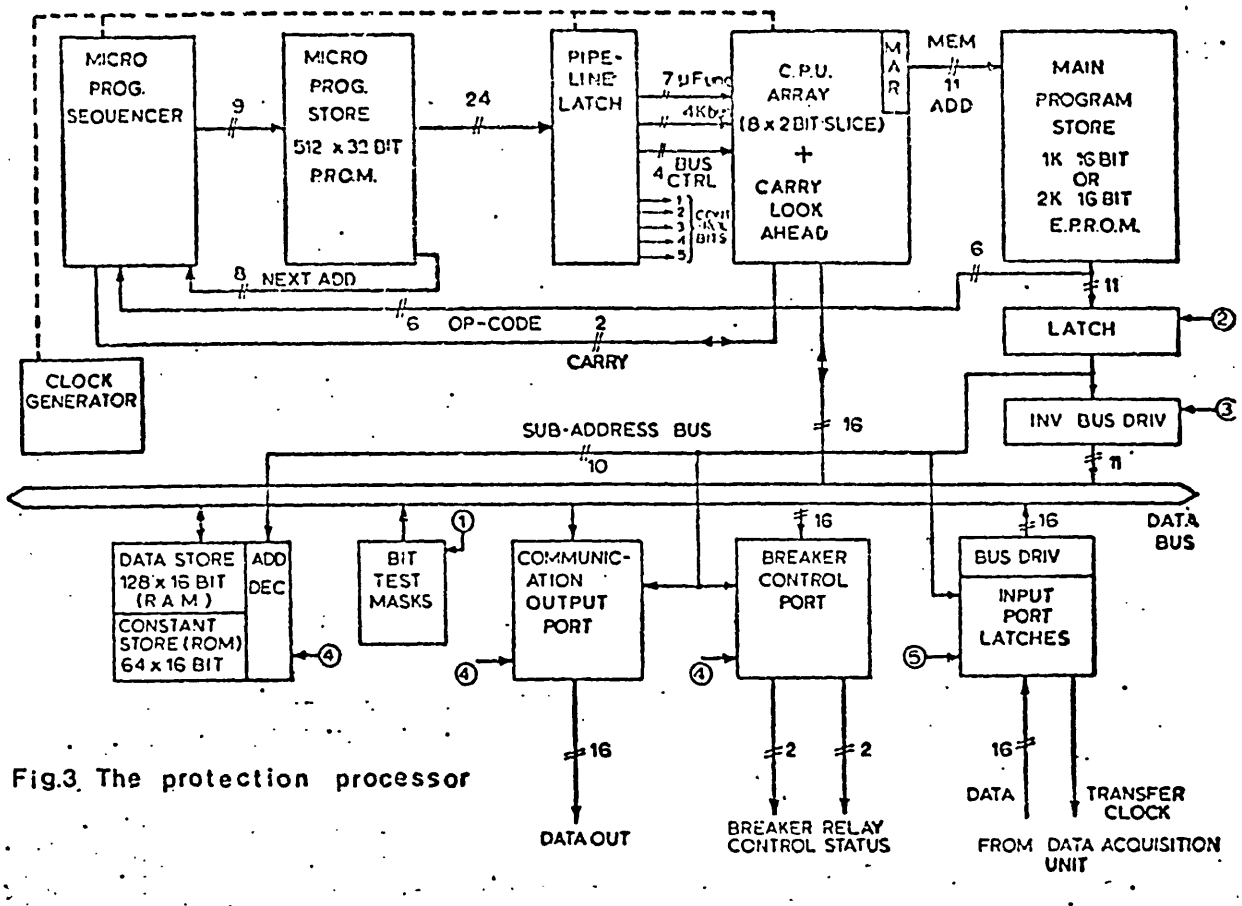

Fig.3 The protection processor

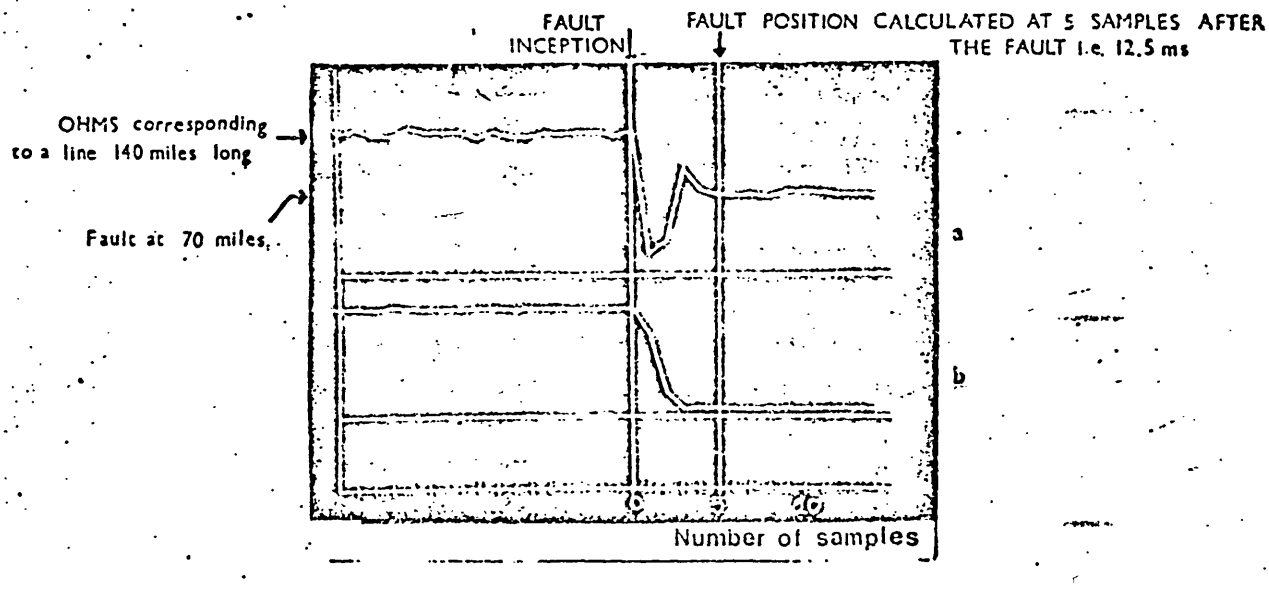

Fig.4 (a)reactance,(b)resistance for double phase fault calculated by the processor